Wafer Fault detection in manufacturing using Machine Learning

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***Abstract*—Wafer diagrams, marked by distinctive failure patterns, provide essential insights for engineers investigating wafer design glitches. Traditional approaches like Wafer Map Failure Pattern Recognition (WMFPR) and Wafer Map Similarity Ranking (WMSR) often rely on raw data, overlooking feature extraction. However, as sensor data usage in semiconductor manufacturing grows, current strategies may struggle with extensive datasets.**

To overcome this, we propose a novel set of features, both rotation- and scale-invariant, aiming for a more concise representation of wafer charts. These features are crucial for WMFPR and WMSR when scrutinizing large-scale datasets. In addition, our system incorporates a Convolutional Autoencoder (CAE) model to enhance the dataset further. To assess effectiveness, we compiled the world's most extensive publicly available wafer chart dataset, totaling 811,457 real-world instances. Experimental results underscore the efficiency of the suggested features and the overall system, aligning with the demands of modern semiconductor manufacturing.

***Index Terms*—Wafer diagrams, failure patterns, semiconductor manufacturing, feature extraction, Wafer Map Failure Pattern Recognition (WMFPR), Wafer Map Similarity Ranking (WMSR), rotation-invariant features, scale-invariant features, large-scale datasets, Convolutional Autoencoder (CAE) model, dataset enhancement, real-world instances, experimental outcomes, modern semiconductor manufacturing.**

I. Introduction

In the dynamic realm of semiconductor manufacturing, a critical aspect lies in the analysis of wafer diagrams to identify and rectify design glitches. These diagrams, characterized by distinctive failure patterns, offer engineers crucial insights into the origins of potential issues.[1] Conventional methods like Wafer Map Failure Pattern Recognition (WMFPR) and Wafer Map Similarity Ranking (WMSR) often rely on raw data, neglecting the nuanced information that could be extracted through feature analysis.

The integration of sensor data in semiconductor manufacturing brings about a heightened level of complexity in the analysis of wafer diagrams. [25]Current strategies, initially designed for more traditional datasets, may fall short when confronted with the scale and intricacies of modern sensor-driven datasets.[6]Recognizing this challenge, our solution revolves around introducing innovative features that are both rotation- and scale-invariant. This approach aims to distill a more concise representation of wafer charts, proving particularly advantageous when combined with WMFPR and WMSR for the scrutiny of large-scale datasets.

To address the limitations of conventional approaches, our innovative solution involves the introduction of rotation- and scale-invariant features. These features seek to enhance the analysis of wafer diagrams, providing a more comprehensive understanding of failure patterns. [26]When integrated with established methods like WMFPR and WMSR, our approach demonstrates efficacy in scrutinizing large-scale datasets, presenting a promising avenue for advancing semiconductor manufacturing processes.[27]We'll be using the Convolutional Autoencoder(CAE model to expedite the process of Semiconductor manufacturing

Undertaking a monumental task, we compiled the world's most extensive publicly available dataset of wafer charts, totaling 811,457 real-world instances. The results of our experiments underscore the effectiveness of the proposed features and the overall system, showcasing its capability to meet the demands of modern semiconductor manufacturing by effectively handling the intricacies of large-scale datasets. This abstract sheds light on the significance of our novel features and their potential impact on advancing the field of wafer diagram analysis.

II. Existing Works

Machine learning and deep learning (ML/DL) technologies are transforming wafer defect identification and categorization in semiconductor manufacturing. ML/DL surpass traditional rule-based methods by adeptly managing intricate patterns, learning autonomously from data, and adapting to novel

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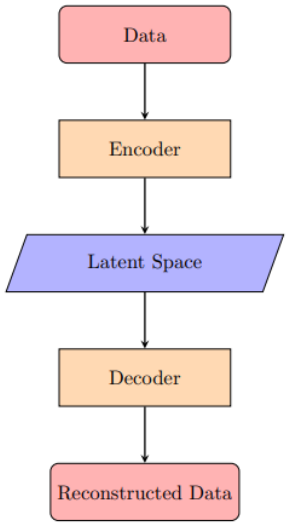

Fig. 1. Flowchart explaining the CAE model

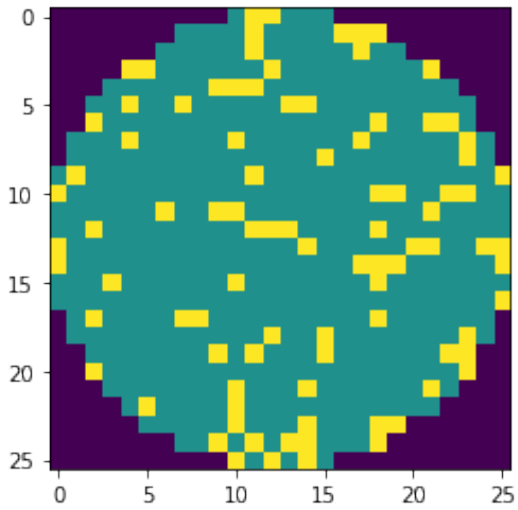

Fig. 2. Example of a wafer map failure pattern

scenarios. Recent investigations explore ML/DL applications in wafer defect detection. Cheng et al. [1] proposed a pioneering ML-based technique for recognizing wafer test-induced defects. Kim and Behdinan [2] conducted an exhaustive review of ML/DL applications for wafer map defect recognition. Lee et al. [3] developed a robust DL model for wafer fault monitoring, handling sensor measurement noise effectively. Fan et al. [4] introduced innovative variational autoencoder-based generative models for imbalanced fault detection data. Gorman et al. [5] demonstrated the potential of localized reconstruction errors from 1-D convolutional autoencoders for anomaly detection in batch manufacturing. Tchatchoua et al. [6] applied a 1D ResNet architecture for superior fault detection in semiconductor sensor data. Lang et al. [7] reviewed AI-based techniques for fault detection in EV motors. Wu et al. [8] proposed a DL-based defense against cyber-physical attacks. Li and Wang [9] presented an improved Mask R-CNN for defect detection on wafer maps. These studies underline ML/DL effectiveness in wafer defect detection, promising advancements in semiconductor quality control. In semiconductor manufacturing, minimizing anomalies during wafer production is vital for enhanced yield and product quality. Fault detection, analyzing parameters like pressure and voltage, is pivotal. Addressing this, [11] introduces an ensemble anomaly detector, validated using real semiconductor industry datasets.

Defect pattern classification in semiconductor manufacturing relies on static data models. [12] introduces incremental learning for wafer surface defect detection using Resnet and the WM811K wafer dataset, achieving heightened accuracy. [13] assesses recent research in wafer surface defect detection, categorizing defects and reviewing methods in image signal processing, machine learning, and deep learning. [14] proposes the Micro-defect Classification System (MDCS) for micro-defect detection, combining defect detection and classification with bionic vision-inspired attention modules for enhanced accuracy.

III. Methodology

A. Dataset Description

1. Data Collection: The dataset amalgamates tabular data with intricate wafer maps, constituting a crucial asset for training semiconductor wafer defect detection models. Wafer images were meticulously extracted from a compressed ZIP file, ensuring a seamless integration with corresponding failure labels incorporated into a Pandas DataFrame.

2. Data Preprocessing: To optimize model training and evaluation, the dataset was partitioned into two distinct groups: training and testing sets. This deliberate segregation guards against overfitting, enabling the model to adeptly handle novel and unseen data instances.

B. Preprocessing

1. Data Augmentation using CAE: Pioneering innovation, the integration of a Convolutional Autoencoder (CAE) for data augmentation was initiated. This neural network, comprising both an encoder and decoder, collaborates to enhance the dataset. The encoder condenses wafer images into a latent space, while the decoder reconstructs them, amplifying diversity and quality essential for robust defect-detection model training.
2. Mitigating Risks: Addressing challenges associated with data quality and augmentation, rigorous preprocessing measures were employed. Stringent quality control procedures ensure the generated data authentically reflects wafer defects,

while concurrently preventing the introduction of any misleading or irrelevant noises.

C. Proposed Method

The devised approach revolves around a Convolutional Neural Network (CNN) meticulously engineered to concurrently process both wafer images and tabular data. This intricately designed architecture comprises an Input Layer, serving as the genesis for wafer images to commence their journey into the neural network. Following this, Convolutional Layers meticulously extract features, unraveling patterns within the captivating tapestry of wafer images. Acting as sentinels, the Pooling Layers judiciously oversee feature map dimensions, orchestrating a reduction process that distills the essence while retaining vital information and discarding extraneous details. This symphony of dimensionality reduction ensures efficiency without compromising the crux of significance in the integrated processing of wafer images and tabular data.

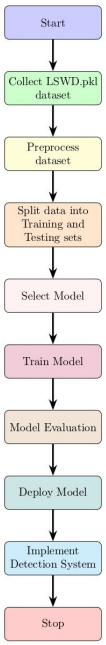

Fig. 3. A simple flowchart explaining the proposed methodology

Adam, a highly esteemed algorithm in deep learning, assumes the pivotal role of an optimizer with skillful management of adaptive learning rates. This adaptive quality empowers Adam to navigate the intricate landscape of parameters, guiding the model towards convergence with remarkable deftness and efficiency. The dynamic adjustment of learning rates contributes to the model's ability to efficiently converge on optimal solutions, establishing Adam as a stalwart ally in the optimization process within the dynamic field of deep learning. In the realm of multi-class classification, the chosen loss function is the wise and well-suited Categorical Cross Entropy. This particular loss function emerges as a sage choice, meticulously assessing the dissonance between predicted probabilities and actual labels. Serving as a guiding compass for the model, it aids in refining its predictive prowess. Categorical Cross Entropy plays a pivotal role in the intricate process, ensuring that the model hones its ability to make accurate predictions by closely aligning with the actual class labels.

D. Performance Evaluation

The model underwent a transformative journey through rigorous training on an enriched dataset, with the collaborative efforts of the Convolutional Neural Network (CNN) components—encoder and decoder—within the CAE. This ensured that augmented data significantly enhanced the model's proficiency in defect detection. Subsequently, facing a crucible during the intensive evaluation on the test set, the model demonstrated its capacity to generalize to previously unseen data. Accuracy, a pivotal measure of performance, was meticulously calculated, serving as a numerical testament to the model's classification accuracy and its adeptness in effectively discerning defects during the testing phase.

IV. Results

The objective of this exploration was to advance wafer fault detection by delving into the intricate realm of semiconductor manufacturing, utilizing a novel strategy that integrates wafer maps and tabular data. A notable feature of this project is the innovative application of Convolutional Autoencoders (CAEs) for data augmentation, adding a unique and valuable dimension to the methodology.

Despite notable advancements in automating defect detection and visualizing anomalies on wafer maps, challenges persist. The quality of data and the intricate interplay between tabular and image datasets remain central concerns. Striking the right balance with the CAE model to effectively augment data while preventing the introduction of irrelevant information remains an ongoing consideration.

Additionally, the complexity of defect types and variations in manufacturing processes presents persistent hurdles. Ensuring the adaptability of these models to diverse defect scenarios requires continuous refinement. In essence, as the project concludes, we acknowledge the progress made while recognizing the dynamic nature of challenges that demand ongoing attention and refinement in the pursuit of advancing wafer fault detection in semiconductor manufacturing. The confusion matrix, signaling a remarkable 99.6 accuracy in testing, highlights precision with minimal occurrences of false positives and negatives. The substantial 98.7 training accuracy further underscores the model's proficiency in effectively learning from the dataset. In the normalized confusion matrix, metrics are presented as percentages relative to total samples. The model achieves an impressive 99.6 testing accuracy, indicating robust correctness. The 98.7 training accuracy signifies consistent learning with a balanced precision-recall trade-off, highlighting the dataset's overall robustness.

In the depicted figure, the model demonstrates remarkable accuracy, registering 99.6 in testing and 98.7 in training, coupled with minimal testing and training losses (2 and 0.3 respectively). This showcases the model's efficiency

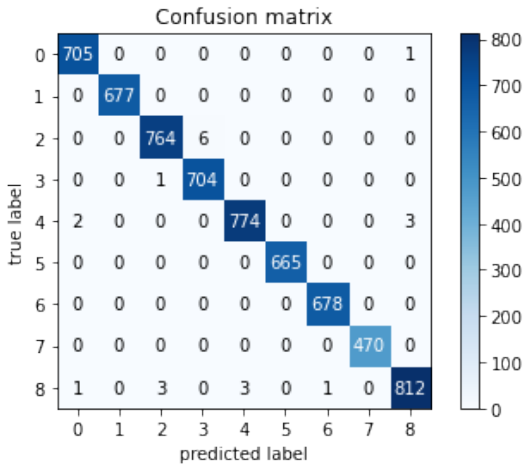

Fig. 4. Confusion matrix

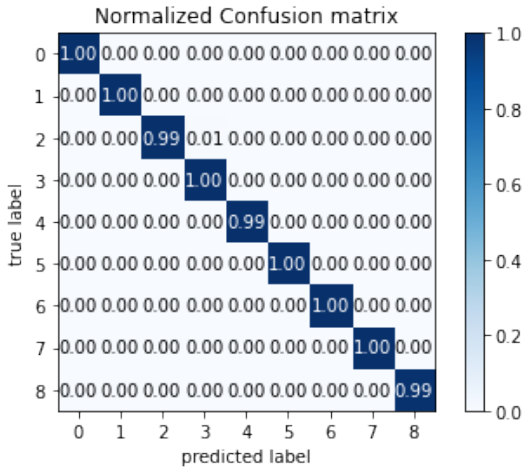

Fig. 5. Normalized Confusion matrix

in minimizing errors effectively. The balanced precision-recall trade-off within the context of minimal training loss emphasizes the model's robust adaptation to the dataset, affirming its overall effectiveness.

In the depicted figure, the accuracy plot accentuates the model's robust performance, attaining an impressive 99.6 in testing accuracy. This underscores the model's proficiency in effectively generalizing to new, unseen data, demonstrating strong correctness. The training accuracy, registering at 98.7, signifies consistent learning and emphasizes a balanced precision-recall trade-off. This equilibrium highlights the model's capacity to maintain high correctness levels while mitigating the risks of overfitting or underfitting during the training process.

V. Conclusion

In conclusion, this study introduces a groundbreaking method that seamlessly integrates sophisticated Convolutional

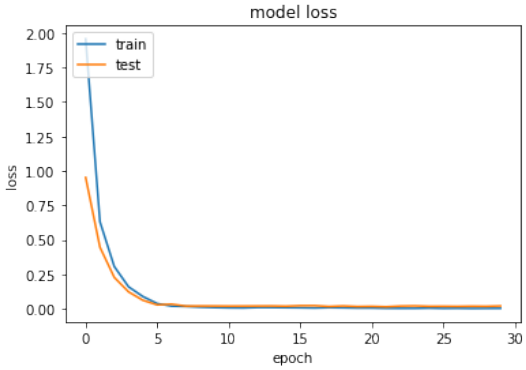

Fig. 6. Normalized Confusion matrix

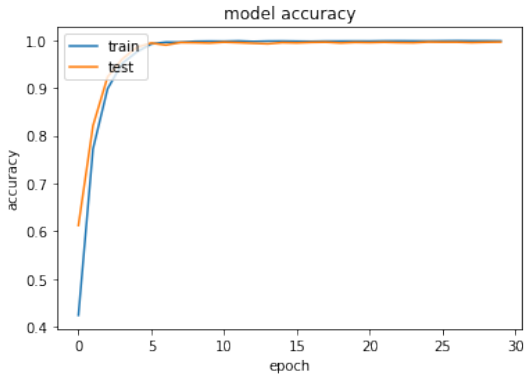

Fig. 7. Normalized Confusion matrix

Autoencoder (CAE) architectures with meticulous data analysis to elevate the identification of faults in semiconductor wafers. Fundamental objectives include accurate defect prediction from tabular data by leveraging historical insights and deploying CAE models for data augmentation to diversify the dataset effectively. Significantly, the proposed solution holds the potential to transform semiconductor manufacturing. Through the automation of defect detection, it streamlines operations, minimizes delays, and reduces waste, thereby enhancing manufacturing efficiency. The strategic implementation of CAE models aims to decrease the production of faulty wafers, leading to substantial cost savings in manufacturing. Furthermore, the assurance of defect-free wafers directly contributes to heightened product quality, positively influencing manufacturers' reputations and ensuring adherence to rigorous industry standards. In this integrated strategy, harmonizing AI models for tabular data analysis with CAE-driven data augmentation has yielded substantial advancements in more efficient and precise wafer fault detection. Future enhancements may involve refining the CAE model, exploring advanced data augmentation techniques, and expanding the scope to address the evolving challenges in semiconductor manufacturing. This research represents a pivotal stride in optimizing semiconductor manufacturing processes, mitigating defects, and elevating the overall quality of semiconductor

A comparative Analysis of our Findings

#	Model/method	Testing Accuracy
1	Proposed	99.6%
2	SVM[23]	94.63%
3	Deep Learning[24]	89.64%

Fig. 8. Accuracy Comparison

products.

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