FAIRCHILD

SEMICONDUCTOR®

August 2009

FSUSB42 — Low-Power, Two-Port, Hi-Speed, USB2.0 (480Mbps) Switch

Features

- Low On Capacitance: 3.7pF Typical
- Low On Resistance: 3.9Ω Typical
- Low Power Consumption: 1µA Maximum
  - 15µA Maximum I_{CCT} over an Expanded Voltage Range (V_{IN}=1.8V, V_{CC}=4.3V)
- Wide -3db Bandwidth: > 720MHz
- Packaged in:
  - 10-Lead UMLP (1.4 x 1.8mm)
  - 10-Lead MSOP
- 8kV ESD Rating, >16kV Power/GND ESD Rating
- Over-Voltage Tolerance (OVT) on all USB Ports Up to 5.25V without External Components

Applications

- Cell phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-Top Box

IMPORTANT NOTE:

For additional performance information, please contact analogswitch@fairchildsemi.com.

Description

The FSUSB42 is a bi-directional, low-power, two-port, Hi-Speed, USB2.0 switch. Configured as a double-pole, double-throw switch (DPDT) switch, it is optimized for switching between two Hi-Speed (480Mbps) sources or a Hi-Speed and Full-Speed (12Mbps) source.

The FSUSB42 is compatible with the requirements of USB2.0 and features an extremely low on capacitance (C_{ON}) of 3.7pF. The wide bandwidth of this device (720MHz) exceeds the bandwidth needed to pass the third harmonic, resulting in signals with minimum edge and phase distortion. Superior channel-to-channel crosstalk also minimizes interference.

The FSUSB42 contains special circuitry on the switch I/O pins for applications where the V_{CC} supply is powered-off (V_{CC}=0), which allows the device to withstand an over-voltage condition. This device is designed to minimize current consumption even when the control voltage applied to the SEL pin is lower than the supply voltage (V_{CC}). This feature is especially valuable to ultra-portable applications, such as cell phones, allowing for direct interface with the general-purpose I/Os of the baseband processor. Other applications include switching and connector sharing in portable cell phones, PDAs, digital cameras, printers, and notebook computers.

Ordering Information

Part Number	Top Mark	Operating Temperature Range	🍃 Eco Status	Package
FSUSB42UMX	HE	-40 to +85°C	Green	10-Lead, Quad, Ultrathin Molded Leadless Package (UMLP), 1.4 x 1.8mm
FSUSB42MUX	FSUSB42	-40 to +85°C	Green	10-Lead, Molded Small Outline Package (MSOP) JEDEC MO-187, 3.0mm Wide

🍃 *For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.*

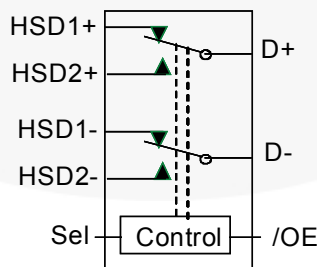MicroPak™ is a trademark of Fairchild Semiconductor Corporation.
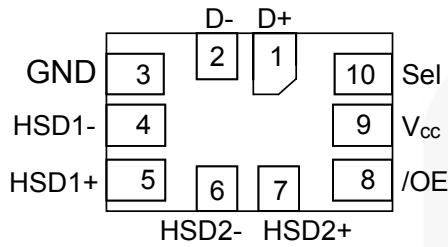

Figure 1.   Analog Symbol

Pin Assignments

D- D+
GND 3 | 2 | 1 | 10 Sel
HSD1- 4 | 9 Vcc
HSD1+ 5 | 6 | 7 | 8 /OE
HSD2- HSD2+

**Figure 2. Pin Assignment 10L UMLP
(Top Through View)**

V_CC — 1 | 10 — /OE
Sel — 2 | 9 — HSD2+
D+ — 3 | 8 — HSD2-
D- — 4 | 7 — HSD1+
GND — 5 | 6 — HSD1-
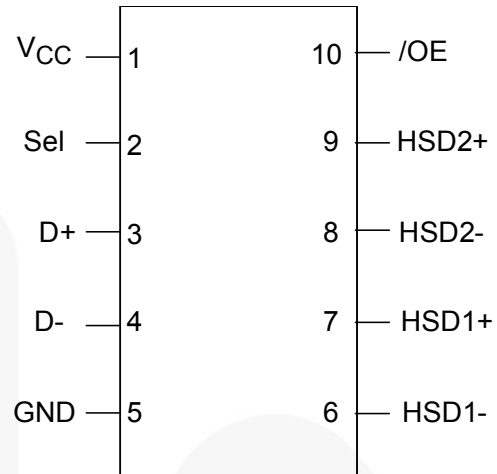
**Figure 3. Pin Assignment 10L MSOP
(Top Through View)**

Pin Definitions

UMLP Pin#	MSOP Pin#	Name	Description
1	3	D+	USB Data Bus
2	4	D-	USB Data Bus
3	5	GND	Ground
4	6	HSD1-	Multiplexed Source Inputs
5	7	HSD1+	Multiplexed Source Inputs
6	8	HSD2-	Multiplexed Source Inputs
7	9	HSD2+	Multiplexed Source Inputs
8	10	/OE	Switch Enable
9	1	V_{CC}	Supply Voltage
10	2	Sel	Switch Select

Truth Table

Sel	/OE	Function
X	HIGH	Disconnect
LOW	LOW	D+, D-=HSD1+, HSD1-
HIGH	LOW	D+, D-=HSD2+, HSD2-

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	5.6	V
V_{CNTRL}	DC Input Voltage (S, /OE)[1]		-0.5	V_{CC}	V
V_{SW}	DC Switch I/O Voltage[1]		-0.50	5.25	V
I_{IK}	DC Input Diode Current		-50		mA
I_{OUT}	DC Output Current			100	mA
T_{STG}	Storage Temperature		-65	+150	°C
MSL	Moisture Sensitivity Level (JEDEC J-STD-020A)			1	Level
ESD	Human Body Model, JEDEC: JESD22-A114	All Pins		7	kV
		I/O to GND		8	
		Power to GND		16	
	Charged Device Model, JEDEC: JESD22-C101			2	

Note:
1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	3.0	4.3	V
V_{CNTRL}[2]	Control Input Voltage (S, /OE)	0	V_{CC}	V
V_{SW}	Switch I/O Voltage	-0.5	4.5	V
T_A	Operating Temperature	-40	85	°C

Note:
2. The control input must be held HIGH or LOW and it must not float.

DC Electrical Characteristics

All typical value are at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V$_{CC}$ (V)	T$_A$=- 40ºC to +85ºC			Units
				Min.	Typ.	Max.	
V$_{IK}$	Clamp Diode Voltage	I$_{IN}$=-18mA	3.0			-1.2	V
V$_{IH}$	Input Voltage High		3.0 to 3.6	1.3			V
			4.3	1.7			V
V$_{IL}$	Input Voltage Low		3.0 to 3.6			0.5	V
			4.3			0.7	V
I$_{IN}$	Control Input Leakage	V$_{SW}$=0 to V$_{CC}$	0 to 4.3	-1		1	µA
I$_{OZ}$	Off State Leakage	0 ≤ Dn, HSD1n, HSD2n ≤ 3.6V	4.3	-2		2	µA
I$_{OFF}$	Power-Off Leakage Current (All I/O Ports)	V$_{SW}$=0V to 4.3V, V$_{CC}$=0V Figure 5	0	-2		2	µA
R$_{ON}$	HS Switch On Resistance[3]	V$_{SW}$=0.4V, I$_{ON}$=-8mA Figure 4,	3.0		3.9	6.5	Ω
ΔR$_{ON}$	HS Delta Ron[4]	V$_{SW}$=0.4V, I$_{ON}$=-8mA	3.0		0.65		Ω
I$_{CC}$	Quiescent Supply Current	V$_{CNTRL}$=0 or V$_{CC}$, I$_{OUT}$=0	4.3			1.0	µA
I$_{CCT}$	Increase in I$_{CC}$ Current per Control Voltage and V$_{CC}$	V$_{CNTRL}$=2.6V, V$_{CC}$=4.3V	4.3			10.0	µA
		V$_{CNTRL}$=1.8V, V$_{CC}$=4.3V	4.3			15.0	µA

Notes:
3. Measured by the voltage drop between HSDn and Dn pins at the indicated current through the switch.
   On resistance is determined by the lower of the voltage on the two (HSDn or Dn ports).
4. Guaranteed by characterization.

AC Electrical Characteristics

All typical value are for V_{CC}=3.3V at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=- 40°C to +85°C			Units
				Min.	Typ.	Max.	
t_{ON}	Turn-On Time S, /OE to Output	R_L=50Ω, C_L=5pF V_{SW}=0.8V Figure 6, Figure 7	3.0 to 3.6		13	30	ns
t_{OFF}	Turn-Off Time S, /OE to Output	R_L=50Ω, C_L=5pF V_{SW}=0.8V Figure 6, Figure 7	3.0 to 3.6		12	25	ns
t_{PD}	Propagation Delay[5]	C_L=5 pF, R_L=50Ω Figure 6, Figure 8	3.3		0.25		ns
t_{BBM}	Break-Before-Make	R_L=50Ω, C_L=5pF V_{SW1}=V_{SW2}=0.8V Figure 10	3.0 to 3.6	2.0		6.5	ns
O_{IRR}	Off Isolation	R_L=50Ω, f=240MHz Figure 12	3.0 to 3.6		-30		dB
Xtalk	Non-Adjacent Channel Crosstalk	R_L=50Ω, f=240MHz Figure 13	3.0 to 3.6		-45		dB
BW	-3db Bandwidth	R_L=50Ω, C_L=0pF Figure 11	3.0 to 3.6		720		MHz
		R_L=50Ω, C_L=5pF Figure 11			550		MHz

Note:
5. Guaranteed by characterization.

USB Hi-Speed-Related AC Electrical Characteristics

Symbol	Parameter	Conditions	Vcc (V)	T_A=- 40°C to +85°C			Units
				Min.	Typ.	Max.	
$t_{SK(P)}$	Skew of Opposite Transitions of the Same Output[6]	C_L=5pF, R_L=50Ω Figure 9	3.0 to 3.6		20		ps
t_J	Total Jitter[6]	R_L=50Ω, C_L=5pf, t_R=t_F=500ps (10-90%) at 480Mbps (PRBS=2^{15} – 1)	3.0 to 3.6		200		ps

Note:
6. Guaranteed by characterization.

Capacitance

Symbol	Parameter	Conditions	T_A=- 40°C to +85°C			Units
			Min.	Typ.	Max.	
C_{IN}	Control Pin Input Capacitance	V_{CC}=0V		1.5		pF
C_{ON}	D+/D- On Capacitance	V_{CC}=3.3V, /OE=0V, f=240MHz Figure 15		3.7		
C_{OFF}	D1n, D2n Off Capacitance	V_{CC} and /OE=3.3V Figure 14		2.0		

Test Diagrams
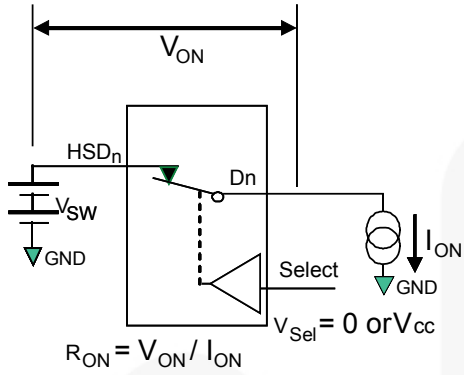
Figure 4.   On Resistance
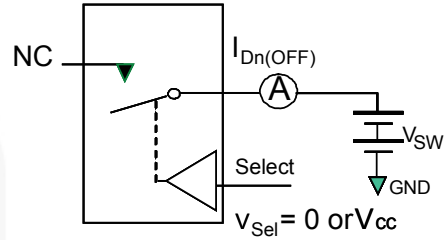
**Each switch port is tested separately

Figure 5.   Off Leakage
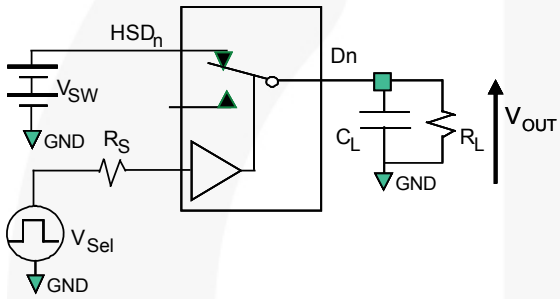
R_L, R_S, and C_L are functions of the application environment (see AC Tables for specific values)
C_L includes test fixture and stray capacitance.

Figure 6.   AC Test Circuit Load
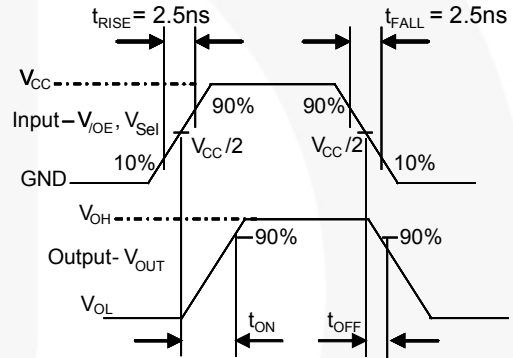
Figure 7.   Turn-On / Turn-Off Waveforms
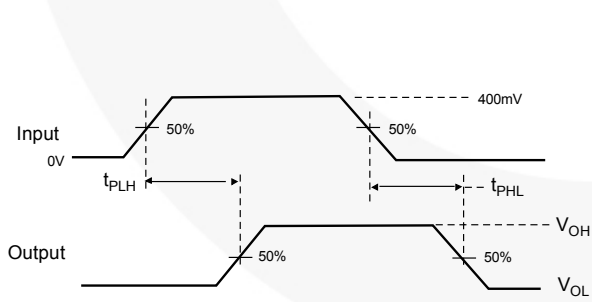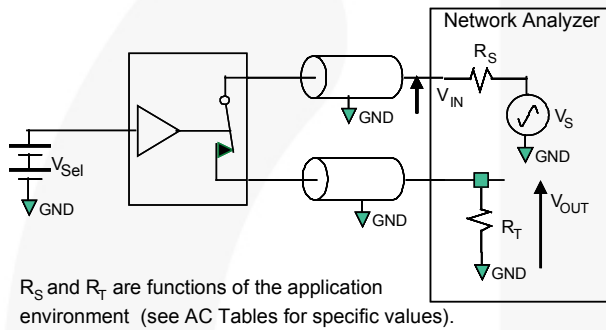

Figure 8.   Propagation Delay ($t_R t_F$ – 500ps)
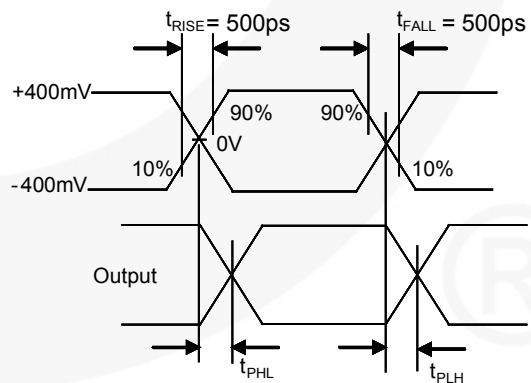
Figure 9.   Intra-Pair Skew Test $t_{SK(P)}$

Test Diagrams (Continued)
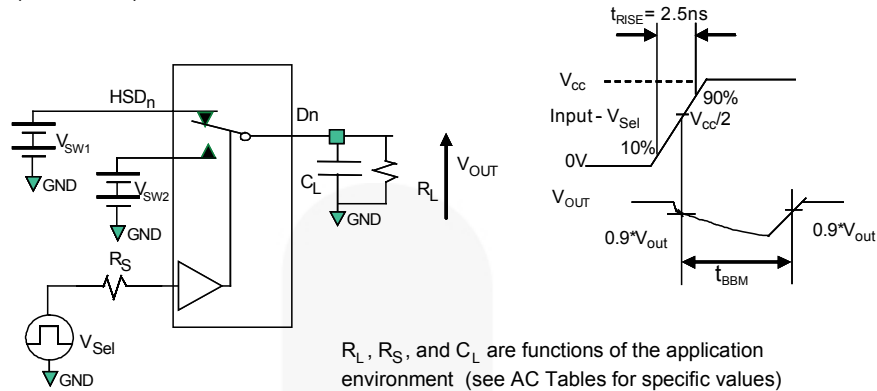
R_L, R_S, and C_L are functions of the application environment (see AC Tables for specific values)
C_L includes test fixture and stray capacitance.

Figure 10. Break-Before-Make Interval Timing

R_S and R_T are functions of the application environment (see AC Tables for specific values).

Figure 11. Bandwidth
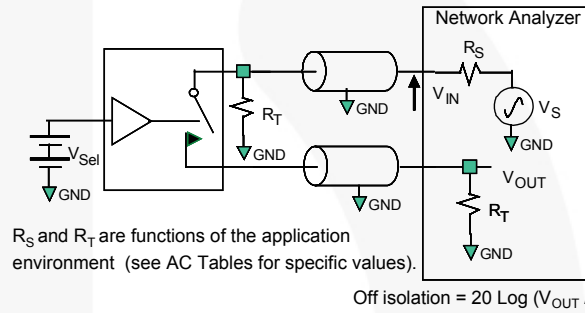
R_S and R_T are functions of the application environment (see AC Tables for specific values).

Off isolation = 20 Log (V_{OUT} / V_{IN})

Figure 12. Channel Off Isolation
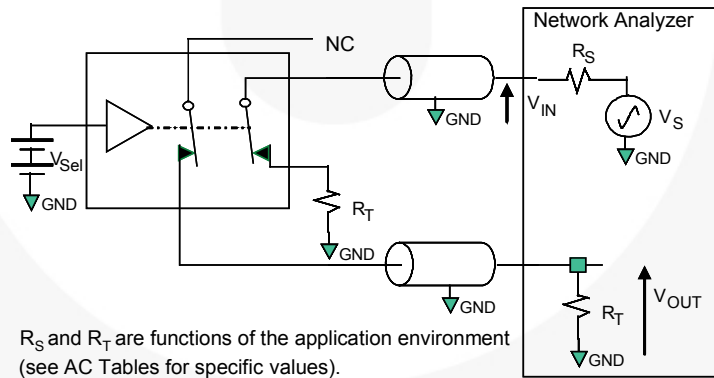
R_S and R_T are functions of the application environment (see AC Tables for specific values).

Crosstalk = 20 Log (V_{OUT} / V_{IN})

Figure 13. Non-Adjacent Channel-to-Channel Crosstalk
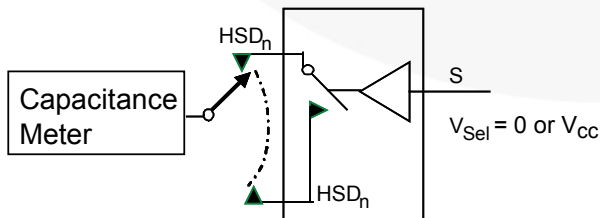
Figure 14. Channel Off Capacitance
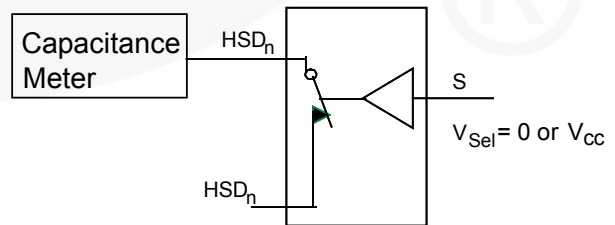
Figure 15. Channel On Capacitance

Physical Dimensions

TOP VIEW

SIDE VIEW

DETAIL A

BOTTOM VIEW

RECOMMENDED LAND PATTERN

OPTIONAL MINIMIAL TOE LAND PATTERN

DETAIL A
PIN #1 TERMINAL
SCALE: 2X
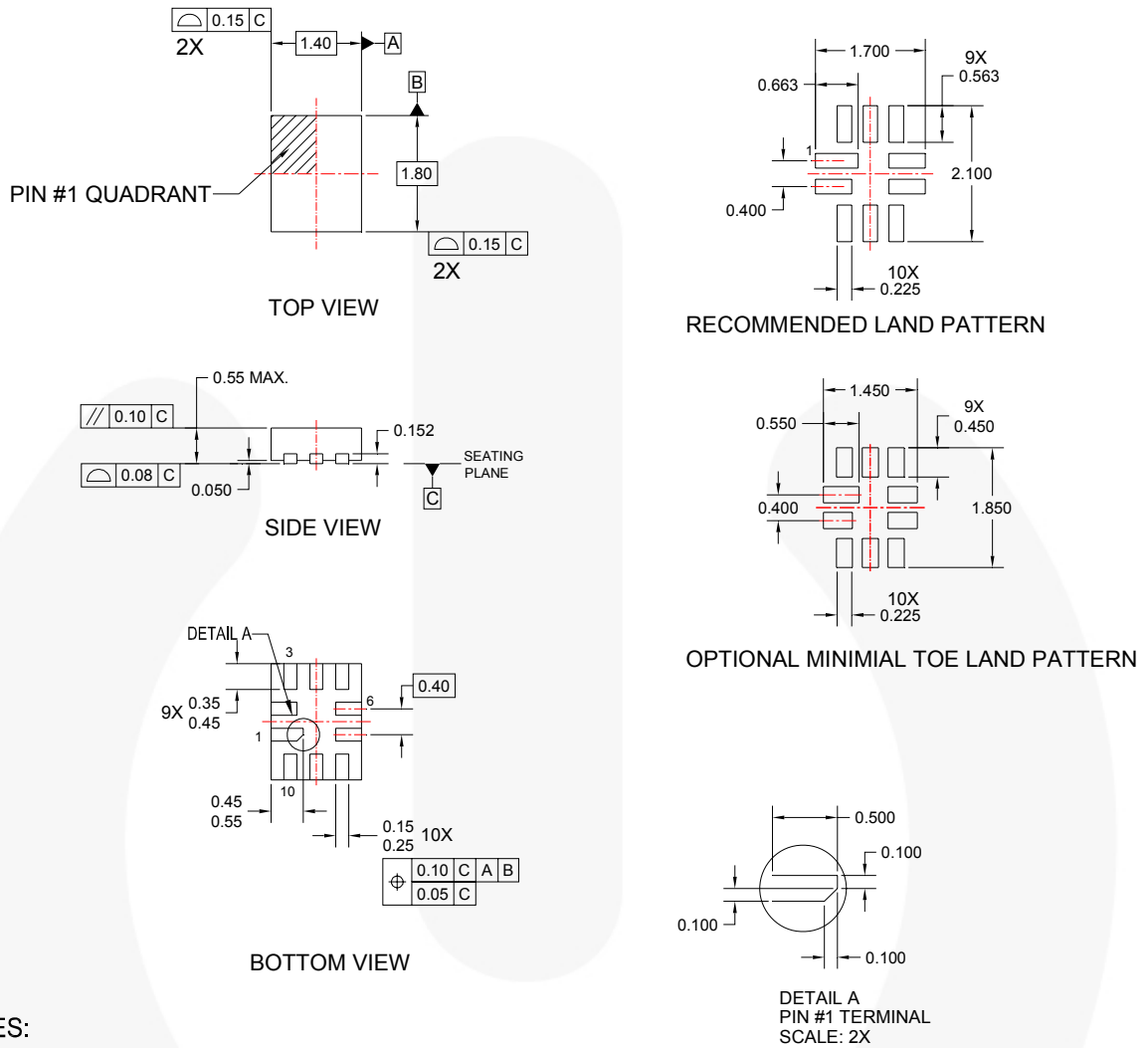
NOTES:

A. DIMENSIONS ARE IN MILLIMETERS.
B. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
C. DRAWING FILENAME: UMLP10Arev2

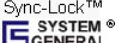**Figure 16. 10-Lead, Ultrathin Molded Leadless Package (UMLP)**

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Physical Dimensions (Continued)

3±0.1 A

B

4.9

3±0.1

2.45

PIN #1
IDENT

0.381 TYP

10   6

2.5

5.4

1.45

1   5

0.5 TYP   0.3 TYP
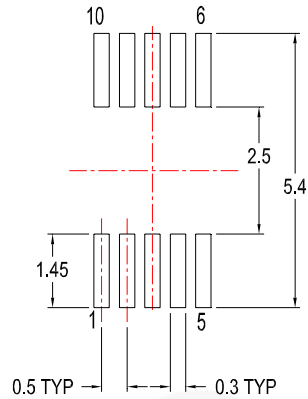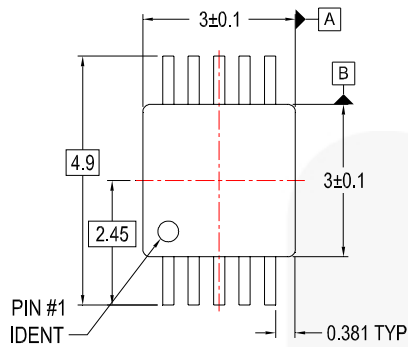
LAND PATTERN RECOMENDATION

0.1 C
ALL LEAD TIPS

1.1 MAX

0.85±0.10

C

0.00-0.15

0.50

0.17-0.27

⊕ 0.08 Ⓜ A B Ⓢ C Ⓢ

DIMENSIONS ARE IN MILLIMETERS

SEE DETAIL A

0.08-0.23

12° TOP & BOTTOM

R.13 TYP

GAGE PLANE

R0.13 TYP

0.25

0°-8 °

0.60±0.20

(0.95)

SEATING PLANE
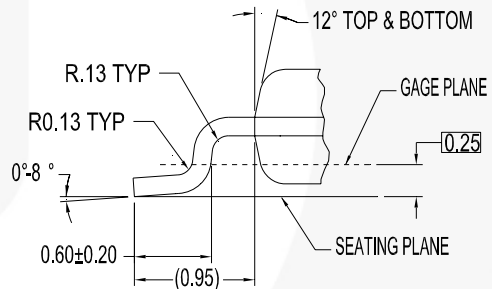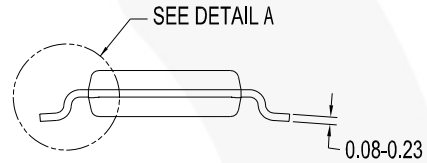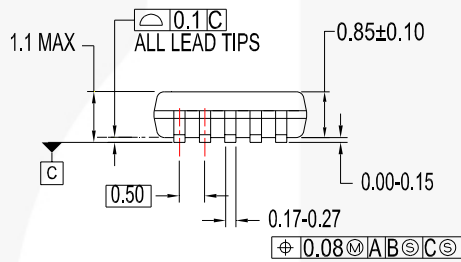
DETAIL A

NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO-187, VARIATION BA,
REF NOTE 6, DATE 11/00.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH,
AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

MUA10AREVA

Figure 17. 10-Lead, Molded Small Outline Package (MSOP)

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SPM®
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SuperSOT™-6
SuperSOT™-8
SupreMOS™
SyncFET™
Sync-Lock™

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I42