History

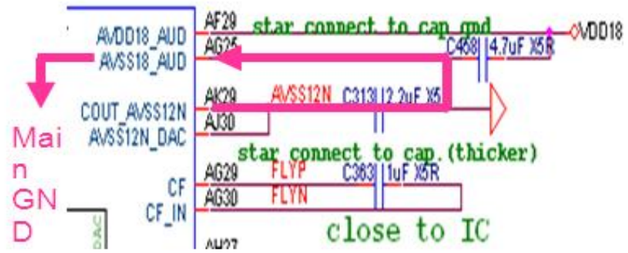
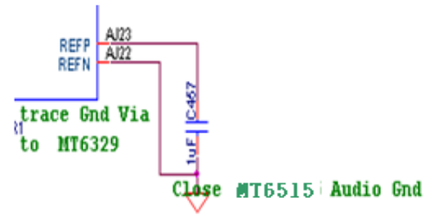
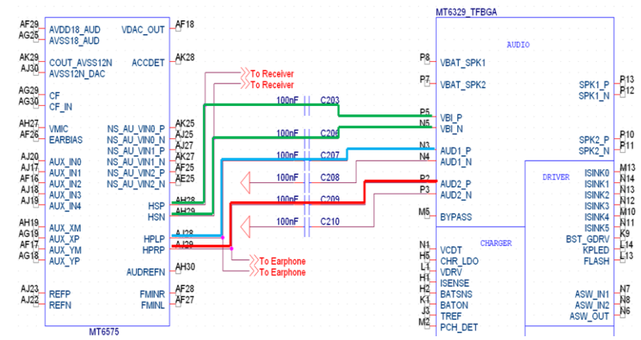
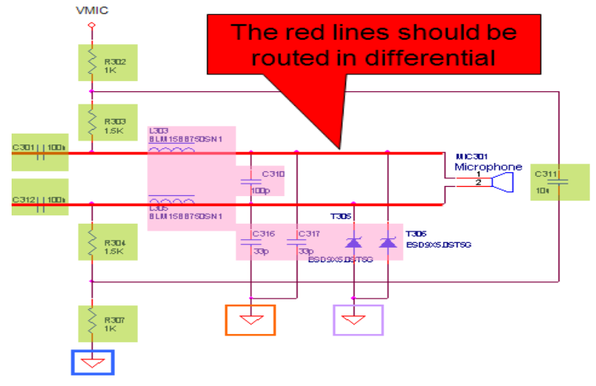
Date	Version	Descripion
W1150.1205	V0.1	Draft, Summary all function item in one excel file; Update 3 function part: 1.LCD add 3 items: -当使用DPI连接CPU LCM时，Write 讯号接到 MT6515 DPIVSYNC (pin L5) -当使用DPI连接CPU LCM时，Read 讯号接到 MT6515 DPIHSYNC (pin M5) -当使用DPI连接CPU LCM时，RS 讯号接到 MT6515 DPIDE (pin N5) 2.SD.eMMC add 5 items:
W1151.1214	V0.2	-Reverse the damping resistor position on the CLK, CMD, DAT to fine tune the AC timing. -If pull-up resistor is needed, please pull up to MT6515 side power. Do not pull up to SD card side power. -Reserve a damping resistor position on the eMMC CLK interface -eMMC core power(VCC) is suggest to be 3.3V -eMMC I/O power(VCCQ) is suggest to be 1.8V Update Placement Guide : 1. ATV_V0.2 Schematic/PCB/Placement checking list are added 2. PMIC_V0.2 Schematic/PCB/Placement checking list are added 3. Connectivity_V0.2 Schematic/PCB/Placement checking list are added 4. AUDIO.SPEECH PCB/Placement list are updated to V0.2 version
W1207.0216	V0.3	5. DRAM Schematic/PCB/Placement checking list are updated to V0.2 version 6. ESD-EMI_V0.2 Placement checking list is added 7. LCD_V0.2 Placement checking list is added 8. Modem_V0.2 PCB/Placement checking list are updated 9. TP_V0.2 Placement checking list is updated 10. USB.Camera.Sensor_V0.2 Placement checking list is updated

		Done	Item
SCH	General	□	TESTMODE pull low
		□	FSOURCE pull to AVDD18_DIG
	Safety	□	PWRKEY, HOMEKEY and BAT_ON靠近IC串聯1K電阻
		□	VBAT connect 5.1V Zener Diode (500mW) with AVL
	DC/DC	□	VBAT input pin reserve bead for de-sense and low power de-bug
		□	Reserve enough bypass capacitors to obtain good system stability.
		□	VPROC is recommended to reserve for remote sense or local sense option, default is suggesting to remote sense, Reserve bypass cap near by MT6329
		□	Buck inductor follow selection guideline to select enough inductor current rating
		□	All DC/DC need near-end Cap 4.7uF as close as possible to PMIC (VPA=2.2uF)
		□	The VCORE output cap is included 2*100nF+1*2.2uF+1uF+22uF combination, place close to MT6515.
		□	The VPROC output cap is included 2*100nF+1*2.2uF+1uF+22uF combination, place close to MT6515.
		□	Connect one schottky diode between VPA_SW to VBAT_VPA that is necessary and should follow selection guideline to select enough rating.
		□	Reserve one 1nF capacitor pad between VPA_SW to GND that is recommended.
		□	MT6329 PMU GND is connected together first, and than single trace connect to GND layer
	LDO	□	VBAT input pin reserve bead for de-sense and low power de-bug
		□	VCAMA need near-end cap 1uF + far-end cap 1uF or 2.2uF
		□	Reserve enough bypass capacitors to obtain good system stability. (Follow design note)
	Driver	□	MT6329支持serial/parallel mode 背光。 Serial mode最多支持10 LEDs, check Output cap voltage rating. Cout=1uF
		□	Inductor, NMOS and Schottky diode should meeting current and voltage rating. It depends on LEDs number
		□	使用 Boost controller時, 請確認要將 VLED_N 接至BLFB and current setting R.
		□	Reserve RC low pass filter from BLDRV to NMOS GATE for de-sense de-bug.
	Charger	□	If support VCHG up to 30V, please change CAP to 1uF/50V
		□	Shunt regulator for charger block resistance change to 3.3Kohm
		□	Charger BJT selection should follow BJT Power Dissipation
	General	□	VREF bypass cap.一定要靠近IC
		□	Vbat在電池連接器出分爲星形線，各路寬度遵守reference design要求；
		□	VBAT 走線經過 Zener Diode and 22uF 再到 Chip VBAT pin
		□	Vbat的Zener Diode、22uf靠近連接器
		□	Vbat，PWRKEY，SYSRST等務必遠離板邊。
	safy	□	For 2nd source parts concern, Zener diode co-layout is flexible to select parts vender.

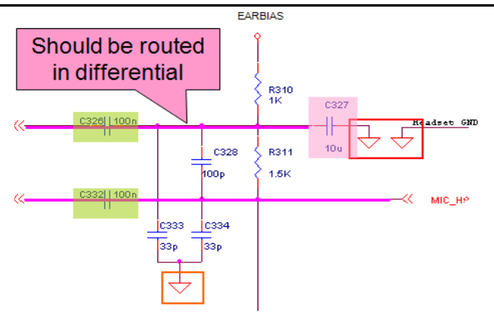
PCB	DC/DC	□	Layout the shortest layout trace from output to inductance to bypass capacitor.
		□	VCORE/VRF18/VIO18/VPA_FB trace要走4mil，且直接從bypass capacitor上拉出來
		□	VPROC_FB layout trace is recommended using GND shielding to avoid noise coupled.
		□	The width of power traces in PCB are recommended as design note
		□	VDDK trace should over 40mil
		□	The GND of switching converter should be merge to power GND before connect to system common GND.
	LDO	□	Keep input cap as close as possible to MT6329
	Driver	□	Please keep boost external component closer to MT6329 and put in shield case..
		□	Layout the shortest layout trace from inductor to NMOS to Schottky diode to output CAP
		□	Trace BLDRV to NMOS GATE is recommended as short as possible for better EMI
	Charger	□	Rsense尽量靠近电池连接器。CHR_LDO decouple请靠近IC，BJT良好舖銅
		□	充電線路不要和其它走線平行
		□	ISENSE and BATSNS should be routed as differential with 4mil and far away from noisy signal
	Fual Gauge	□	FGN_IC/FGP_IC 4mil differential to RFG
Placement	General	□	VREF bypass cap.一定要靠近IC
		□	Vbat的Zener Diode、22uf靠近連接器
	DC/DC	□	inductance and bypass cap closer to MT6329 and put in shield case.
	LDO	□	VCAMA bypass cap closer to MT6329 and put in shield case.
	Driver	□	Please keep boost external component closer to MT6329 and put in shield case..
	Charger	□	Rsense尽量靠近电池连接器
		□	CHR_LDO bypass cap closer to MT6329

		Done	Item
SCH	Audio	□	Serial a bead with power line spec at SPK_P and SPK_N closed to speaker is recommend for EMI reduce
		□	Class AB output (SPK_P/ N)的total bypass cap需小于330pF
		□	Earphone detection changed to EINT + ACCDET - When use standard earpiece , please use the earphone jack with switch pin - Add 470k pull up at L_Switch pin and 10K pull low at L/R - connect L_switch to EINT with 47k ohm resistor is required - connect ACCDET to HP_MIC with 1k resistor
		□	Audio buffer output是DC-coupled, 因此在ESD保护组件上的不能采用uni-directional ESD protection component
		□	In line-in playback scenario, 51k ohm pull low resistor at line-in is required to avoid pop
	Speech	□	MT6515有两组mic bias - VMIC for Main Mic. and 2nd Mic, 1uF cap. at VMIC output - EARBIAS for Earphone Mic, EARBIAS上不需也不要加挂电容
		□	2-in-1 application时, 请参考MT6515 design中"2 -1 SPK application"
PCB	Audio	□	MIC和听筒的滤波器件，TVS的GND要连接一起后通过via连接到主地，不能直接连接表层GND，容易耦合RF noise；
		□	MIC和RCV走线要差分平行；
		□	- The trace width of SPK_P and SPK_N should be larger than 25 mil to min. the IR drop - The Net of SPK_P and SPK_N should be tread as diff. pair and shielded by GND
		□	Star connection from C313 to COUT_AVSS12N and AVSS12N_DAC is required, 请参照"图例解释Layout 细节"
		□	Audio trace 上下包的GND , 要避开使用Switching 原件正下的GND ex. LCD blacklignt 放在Top ; layer2 is GND ; Audio trace 不要经过这个区块的layer3
		□	Take care of the audio trace between MT6515 & MT6329, audio signal should be shielded by GND as well, 请参照"图例解释Layout 细节"
Placement	Audio	□	MIC 摆放位置应远离RF PA及VBAT trace , 避免零件震动音透过MIC 传递
		□	The Cap. connect to REFP and REFN please as close as passable to MT6515
		□	C363 connect to CF and CF_IN is the Flying capacitor, 需要尽可能放靠近AG29/AG30这两个ball
		□	The Cap. connect toAVSS12N_DAC及COUT_AVSS12N please as close as passable to MT6515
		□	The Cap. connect toAVDD18_AUD及AVSS18_AUD please as close as passable to MT6515
		□	Take care of the audio trace between MT6515 & MT6329, audio signal should be shielded by GND as well, 请参照"图例解释Layout 细节"

图例解释Layout 细节			
			Description
			Audio Power and reference point - C363 is the Flying capacitor, 需要尽可能放靠近AG29/AG30这两个ball - C313到AVSS12N_DAC及COUT_AVSS12N需作star connection - C468到AVDD18_AUD及AVSS18_AUD需作star connection - AUD_REFN须直接透过单一个via连接至Main GND (不能接表层的GND)

AUDIO	Keep the current return path back to AVSS18_AUD than through Via to Main GND 
	- The Cap. connect to REFP and REFN please as close as passable to MT6515 - REFP and REFN is the reference voltage generator for over all audio block used ; the trace must shielded with GND 
	Take care of the audio trace between MT6515 & MT6329, audio signal should be shielded by GND as well 
SPEECH	- R302, R303, R304, R307, C311, C301 and C312 should be put close to the BB chip - R302, R303, R304, R307, C311 should be put as close as possible - L303, L305, C310, C316, C317, T305 and T306 should be close to the microphone - GND of C316 and C317 should be connected together and then to the GND - GND of T305 and T306 should be connected together and then to the GND - GND of R307should connect to the main GND by a single via 

- C326, C332, R311, R310 should be put close to BB
- The GND of C333 and C334 should connect together and then connect to the GND
- The GND of C327 and headset should connect together and then to the main GND by single via
- C327 should be put close to microphone



		Done	Item
SCH	Memory(LPDDR)	□	Memory务必使用MTK验证过的, 请务必参照MTK的AVL。
		□	for BB VDD_EMI pins, 务必放四颗bypass电容(2.2uFx1+0.1uFx3), 位置必须靠近BB chip
		□	for MCP LPDDR VDDQ & VDD pins, 务必各放一颗2.2uF之bypass电容, 位置必须靠近MCP
		□	LPDDR之/EDQSx pins, x=0~3, 请直接接GND
	Memory(LPDDR2)	□	Memory务必使用MTK验证过的, 请务必参照MTK的AVL。
		□	for BB VDD_EMI pins, 务必放四颗bypass电容(2.2uFx1+0.1uFx3), 位置必须靠近BB chip
		□	for MCP LPDDR2 VDD1 pins, 务必放一颗2.2uF之bypass电容, 位置必须靠近MCP
		□	for MCP LPDDR2 VDD2 & VDDQ/VDDCA pins, 务必各放一颗2.2uF之bypass电容, 位置必须靠近MCP
		□	EVREF分压电阻是否为(1~10)Kohm
	General	□	Reserve 0ohm over power path of MCP_DRAM (ex. DVDD_EMI) for MVG ETT tuning
PCB	EMI	□	建议的LPDDR/LPDDR2 讯号走线于第1 & 2层走完，第3层为讯号的reference plane(Power plane), 第4层为GND plane(时钟线 & data strobe & EVREF走第4层用GND包), 第5层为Power plane,第6层为GND plane,其余层面与非memory走线区域则don't care
		□	注意BB与LPDDR/LPDDR2 IO power pins到IO Power plane之盲埋孔通道, 大孔至少6颗, 小孔至少9颗, 略为平行交错排列,
		□	注意power pin附近, 各层Power/GND大小孔略呈成对排列, 并注意他层plane通道是否因此变窄, 若有此情况,
		□	Capacitor Power/GND via部份:MCP cap小孔与BB cap大小孔数量尽量维持pad:via=1:2, 且via位置"必须"尽可能靠近pad, 大孔位置必须直接下到power/GND plane, 不能有额外走线的情况
		□	所有EMI 讯号走线包含时钟线&data strobe, 必须要在上下层Power/GND plane投影范围内, 不允许有走线超出范围
		□	尽可能缩短1.2V(LPDDR2 IO power) or 1.8V(LPDDR IO power) from MT6329走到EMI power plane的距离, 换层至少打两个大孔或小孔, trace width>25mils, 并在进power plane时放稳压电容
Placement	EMI	□	原理图定义4颗BB IO power capacitor(1x2.2uF+3x0.1uF)位置必须尽量靠近BB power pin, 第一优先放在BB power pin下方背层处, 若BB下方背层不可摆件, 最少将两颗电容(2.2uF+0.1uF)放在BB与MCP中间位置
		□	MCP是否已经尽可能靠近BB IC
		□	MCP capacitor是否已放在MCP周围

Memory(LPDDR/LPDDR2)

1.EDCLK & EDQSx 走L4, 用IO power 包覆, 其上下层(L3&L5) 为GND
2.其余讯号在L1, L2走完
3.L3 为GND plane(讯号参考地)
4.L4为IO power plane
PS:图例为LPDDR2
请务必follow MTK high speed memory layout rule

		Done	Item
Placement	LCM	□	建议预留ESD/EMI防护组件在靠近LCM connector端, 并联组件默认可不上件 (单一讯号上的等效电容值需小于30pF)
		□	若为MIPI界面, 则ESD/EMI防护器件的等效电容值需小于2pF
		□	走线需从LCM connector先经过ESD/EMI防护组件后再接回BB IC端
	RTP	□	建议预留ESD/EMI防护组件在靠近RTP connector端(在XP/XM/YP/YM上), 并联组件默认可不上件 (单一讯号上的等效电容值需小于100pF)
		□	建议预留 0ohm电阻在XP/XM/YP/YM至TP connector的中间, 如果遇到ESD/EMI问题可改上Bead
		□	走线需从RTP connector先经过ESD/EMI防护组件后再接回BB IC端
	CTP	□	建议预留ESD/EMI防护组件在靠近CTP connector端(在SCL/SDA/RESETB/EINT上), 并联组件默认可不上件 (单一讯号上的等效电容值需小于100pF)
		□	走线需从CTP connector先经过ESD/EMI防护组件后再接回BB IC端
	Sensor (G, M, P, ALS, Gyro)	□	建议预留ESD/EMI防护组件在靠近sensor器件或connector端(在SCL/SDA/RESETB/EINT上), 并联器件预设可不上件 (单一讯号上的等效电容值需小于100pF)
		□	走线需从sensor器件或connector端先经过ESD/EMI防护组件后再接回BB IC端
	Camera	□	建议预留ESD/EMI防护组件在靠近Camera connector端, 并联组件默认可不上件 (单一讯号上的等效电容值需小于30pF)
		□	若为MIPI界面, 则ESD/EMI防护器件的等效电容值需小于2pF
		□	走线需从Camera connector先经过ESD/EMI防护组件后再接回BB IC端
		□	建议使用LC type的ESD/EMI filter with low DCR, 因为Camera MCLK, PCLK是高速时钟信号
	USB2.0	□	建议预留ESD/EMI防护组件在靠近USB connector端, 并联组件默认可不上件 (单一讯号上的等效电容值需小于3pF)
		□	走线需从USB connector先经过ESD/EMI防护组件后再接回BB IC端
	Memory Card	□	建议预留ESD/EMI防护组件在靠近T-Card connector端, 并联组件默认可不上件 (单一讯号上的等效电容值需小于30pF)
		□	走线需从T-Card connector先经过ESD/EMI防护组件后再接回BB IC端
	SIM	□	建议预留ESD/EMI防护组件在靠近SIM connector端(在SIMDATA/SIMRST/SIMCLK上), 并联组件默认可不上件 (单一讯号上的等效电容值需小于22pF)
		□	走线需从SIM connector先经过ESD/EMI防护组件后再接回BB IC端
	Keypad	□	建议预留ESD/EMI防护组件在靠近实体Keypad(Metal Dome) 或者Sidekey端
		□	走线需从实体Keypad(Metal Dome) 或者Sidekey端先经过ESD/EMI防护组件后再接回BB IC端
	Safety	□	所有外露的I/O connector建议都预留ESD防护组件(TVS/Varistor)
		□	走线需从I/O connector先经过ESD防护组件后再接回BB IC端
		□	保留40-50mils的PCB outline copper并且增加足够的GND via
		□	RST讯号(例如/SYSRET, /WATCHDOG, BBWAKEUP, LRSTB, SIMRST)要远离版边超过50mil
	PMU	□	BATSNS需预留1uF 0402的电容并靠近IC端, 避免ESD打到UVLO
		□	走线需先经过1uF 0402的电容后再接回BB IC端
	VBAT	□	建议预留ESD防护组件在靠近Battery connector端(在VBAT/NTC/BATON上)
		□	走线需从Battery connector先经过ESD防护组件后再接回BB IC端
	Vibrator	□	建议预留Schottky Diode在靠近Vibrator器件端, 预设可不上件
		□	走线需从Vibrator端先经过Schottky Diode后再接回BB IC端
		□	建议预留ESD/EMI防护组件在靠近Receiver器件/Earphone Jack/Speaker器件端

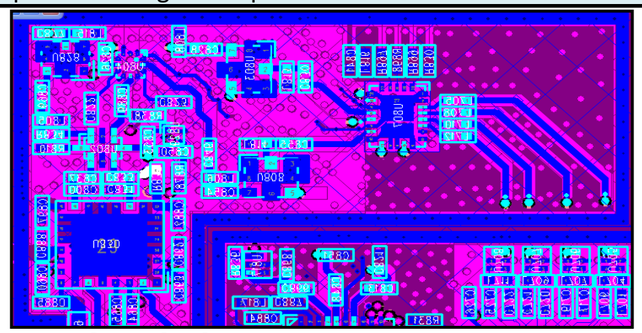
	Receiver / Earphone / Speaker	□	走线需从Receiver器件/Earphone Jack/Speaker器件先经过ESD/EMI防护组件后再接回BB IC端
		□	针对DC coupled的平台(MT6573, MT6515)只能使用Varistor或者是双极性TVS, 不能使用单极性TVS
		□	音频功率放大器的输出端务必预留一组Bead滤波并且靠近喇叭
		□	音频功率放大器的输出端的等效电容值需小于330pF
	MIC	□	建议预留ESD/EMI防护组件在靠近MIC器件端
		□	走线需从MIC器件先经过ESD/EMI防护组件后再接回BB IC端
	Antenna (RF, BT, WiFi, GPS, FM, ATV, CMMB)	□	建议预留ESD防护组件在靠近所有的Antenna端, 并预留匹配电路, 默认不上件
		□	FM天线使用耳机座时, FM_ANT上需预留串接0R可以上Bead做调整, 并且需预留ESD防护组件(等效电容值需小于5pF, 例如: TVM0G180M030R, 3pF) 靠近耳机接口的GND, 并且直接打GND via下到大地
		□	Series bead(Bead resistance at 100MHz should be higher than 1000ohm, ex BLM18BD252SN1) close to earphone jack for each audio trace (Audio-L, Audio-R, MIC) ; Well GND shielding for these traces, especially between bead and earphone jack

		Done	Item
SCH	LCM (CPU IF)	□	LCM选用，请用具有独立脚为 IOVCC(IOVDD)，可以 Program IO Level 之模块，并将其接至1.8v level
		□	LCM选用，请用具有F_mark or LPTE 的模块，并将其接至BB dedicated pin LPTE
		□	如果LCM模块 data pin 预留9bit以上 (16/18/24 bit)，请确认8/9 bit正确的出pin位置
		□	LCM 模拟电源供给(VCI)之 Bypass 电容请选用至少 1uF 以上
		□	LCM IO 电源供给(IOVCC or IOVDD)之 Bypass 电容请选用至少 1uF 以上
		□	LCM 背光电供给请预留一个 Bypass 电容，电容值请选用至少 1uF 以上
		□	EMI filter for LCD is recommand for better de-sense performance
		□	NAND IF 总电容Loading 必须低于75pF
		□	当使用DPI连接CPU LCM时，Write 讯号接到 MT6515 DPIVSYNC (pin L5)
		□	当使用DPI连接CPU LCM时，Read 讯号接到 MT6515 DPIHSYNC (pin M5)
		□	当使用DPI连接CPU LCM时，RS 讯号接到 MT6515 DPIDE (pin N5)
	LCM (MIPI DSI IF)	□	EMI filter / Common Choke for MIPI IF cap loading need to under 2pF
		□	LCM选用，请用具有独立脚为 IOVCC(IOVDD)，可以 Program IO Level 之模块，并将其接至1.8v level
		□	LCM选用，请用具有F_mark or LPTE 的模块，并将其接至BB dedicated pin LPTE
		□	LCM 模拟电源供给(VCI)之 Bypass 电容请选用至少 1uF 以上
		□	LCM IO 电源供给(IOVCC or IOVDD)之 Bypass 电容请选用至少 1uF 以上
		□	LCM 背光电供给请预留一个 Bypass 电容，电容值请选用至少 1uF 以上
		□	Common choke for LCD is recommand for better de-sense perforamcne
PCB	LCM (CPU IF)	□	LWRB 讯号线layout, 结构允许情况下 , 请尽量同一层左右包地
		□	LCM 模拟电源供给(VCI)之 Bypass 电容请靠近LCM，并确保电原先先经过Bypass 电容再接到LCM
		□	LCM IO 电源供给(IOVCC or IOVDD)之 Bypass 电容请靠近LCM，并确保电原先先经过Bypass 电容再接到LCM
		□	LCM 背光电源供给之 Bypass 电容请靠近LCM，并确保电原先先经过Bypass 电容再接到LCM
		□	LCM 背光电源正极走线，至少留 6mil以上
		□	使用PMU iSINK做为并联背光时, LED Anode VBAT直接从 Battery connector 走线，避免IR drop而增加VBAT低压造成屏闪的机率
	LCM (MIPI DSI IF)	□	MIPI DSI 差分讯号线需根据 PCB 迭构，计算出符合 差分 100 ohm 阻抗的 trace space and width 进行 layout
		□	MIPI DSI 差分讯号线需要上下左右包地 (建议走内层，并可同时达到降 EMI 干扰问题)
		□	MIPI DSI 差分讯号线 总长不能超过 3000mil
		□	MIPI DSI 差分讯号线 Pair-to-pair 差不能超过 500mil
		□	MIPI DSI 差分讯号线 Line+ / Line- 差不能超过 200mil
lacemer	LCM	□	LCM EMI Filter (or Common Choke) 放靠近LCM connector
		□	LCM 模拟电源供给(VCI)之 Bypass 电容请靠近LCM
		□	LCM IO 电源供给(IOVCC or IOVDD)之 Bypass 电容请靠近LCM
		□	LCM 背光电源供给之 Bypass 电容请靠近LCM
		□	LCM FPC在机构设计尽量避免和RF组件交错，若有交错，建议FPC增加 GND layer做Shielding
		□	LCM MIPI DSI差分讯号如有预留ESD diode，须靠近LCM connector之对应pin摆放。

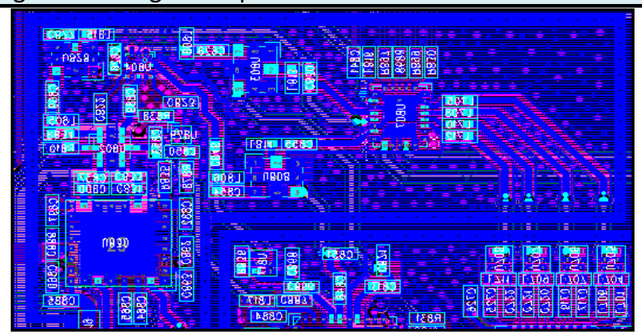
	Done	Item
SCH	□	务必使用MTK验证的RF部分的26MHz晶体, Duplexer, SAW, PA, ASW或TXM
	□	GSM Rx可以选择是否和WCDMA co-banding,以降低BOM cost与layout面积,但会牺牲约0.5dB的sensitivity,
	□	WCDMA 如果只有一个High band,优先使用LNA3
	□	MT6575 RX trace 连接到 RX SAW和duplexer 之间要保留 differential Pi-matching network 增加调适弹性,如果是WCDMA B1/B2,还要预留common mode trap circuit增加WCDMA HB Blocking performance
	□	RX SAW filter, duplexer 到 ASW或TXM 之间要保留L或Pi-matching network , 并且串接DC-block电容 (若确认使用的ASW或TXM不需要 DC-block 电容 , 可以视情况移除)
	□	MT6575和MT6162间的 RxIQ 线路请加 10pF到GND
	□	MT6162 TX trace 到 PA或TXM 之间预留 pi-matching network , 增加调适弹性
	□	MT6162的WCDMA以及EDGE with closed loop需要用到power detector, 请参考Design note的讲解,利用power combiner和attenuator搭配coupler将detector input power设计在0~-35dBm的使用范围之间
	□	3G PA的电源可以选择使用VPA或是VBAT,但建议使用VPA以节省电流
	□	2G PA的VAPC电路上RC filter, C值为1nF,请勿更动
	□	如果使用ASM,请将ASM的电源连接到VRF_PMU (2.8V),而非BPI
	□	所有 BPI trace连接到 ASM或是TXM 的所有 control pin 都必须要串接 1K Ohm
	□	MT6162 CLK buffer没有用到的请直接floating
	□	Thermal sensor线路请连接到MT6575 Pin.AJ18(AUX_IN3)
	□	请参考design note里面关于schematic的详细说明
PCB	□	PA VBAT should go star connection and individual routing. PA VBAT bypass cap 22uF should be close to PA as possible.
	□	VCC_PA trace width should at least 50mils from PMIC to PA and 30 mil in RF room. VBAT should be at least 80mil from Battery Connector to PA and 50mil in RF room. Give as many vias as possible when switching layers for VCC_PA and VBAT.
	□	Do not put power trace in top layer without any shielding
	□	Use inner layer and ground to protect RF, VTCXO, system clock, Tx/RxIQ and VAPC trace, and do not parallel with other trace.
	□	BPI control line need good ground shielding
	□	Keep out second layer of RF trace and TCXO to minimize the capacitance
	□	Keep susceptible circuit (RF trace, IQ, Clock) away high power(PA output), high current(VBAT, VCC_PA) ,high speed circuit(Flash) region
	□	Differential net pairs such as I, IB (or Q and QB) should be parallel to each other
	□	Keep good isolation between OH 2G Tx output and coupling feedback path
	□	For Rx trace, keep out the L2 ground plane below the pads of matching components to minimize the capacitance and keep the ground plane in L2 between the LNA and matching components. It make the 50ohm trace thin to reduce cross coupling between LNA lines.
	□	Trace and components at duplexer RX port should be perpendicular to ANT and TX traces to minimize the coupling between them. PA output trace and TRX trace must be kept away from the Rx trace.
	□	Keep trace from coupler to power detector as RF 50Ω trace
	□	To make good L1 to L3 GND connection GND in L1 is copied to L2 around the DPX in order to make room for L1-2 vias and L2-5 vias. Outside the DPX area L1-6 vias are used to connect the L1 GND to L3 GND. Please refer design note.
	□	add GND well between RXIQ and LNA1
	□	Drop through hole GND via surrounded the PCB, and drop as many as possible GND via near Battery connector and switching layers.
	□	GND plane in L1 & L2 should not keep out and drop ground vias as many as possible!
	□	For Camera, LCM, and MSDC, the clock and data should have better GND protection. Avoid power trace or other trace routing parallel with clock and data.
	□	VCTCXO place as far as possible from thermal source, like PA
	□	Put Battery CONN close to 2G PA for reducing the voltage drop in max output power

Placement	□	The thermistor sensor placement should be close to 3G PA
	□	Keep PA far away OH LNA input trace
	□	Place the resistors between coupler and Pdet together
	□	Keep RF matching circuit placement are similar to our ref design and with good impedance control

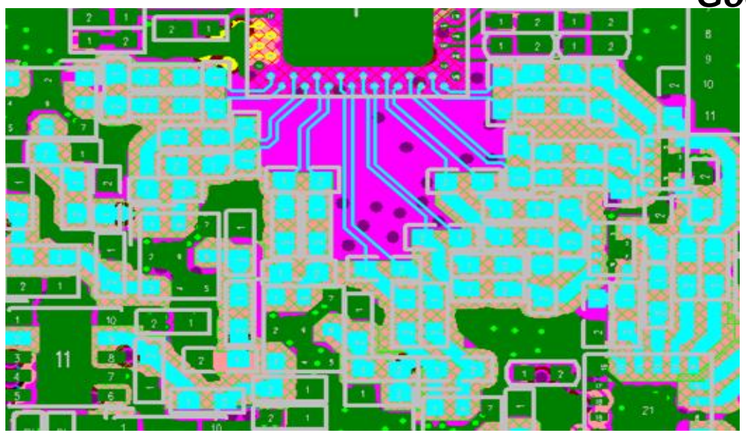
RF area Layer1 and Layer2 GND

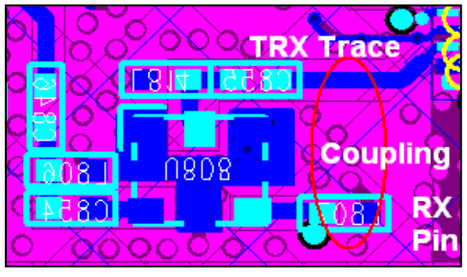


Bad Isolation

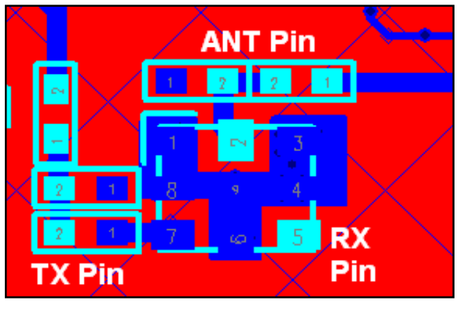


Good Isolation



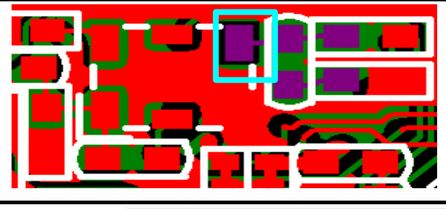


Bad Isolation

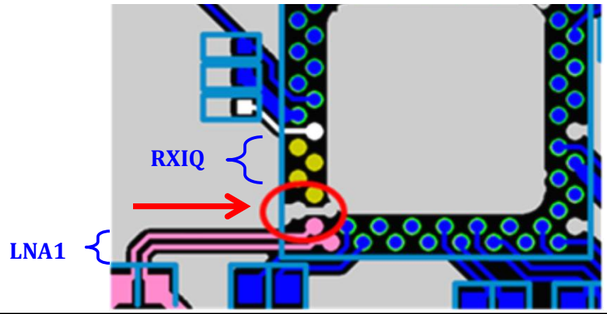


Good Isolation

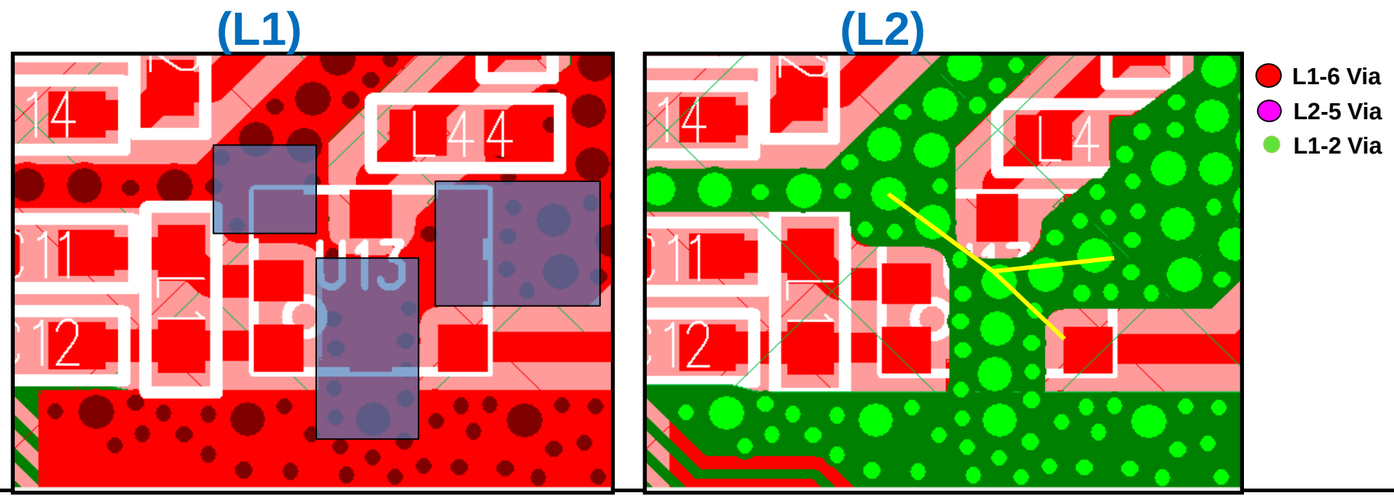
Keep out second layer of TCXO to minimize the capacitance



add GND well between RXIQ and LNA1



Avoid the coupling between the T/RX trace and component



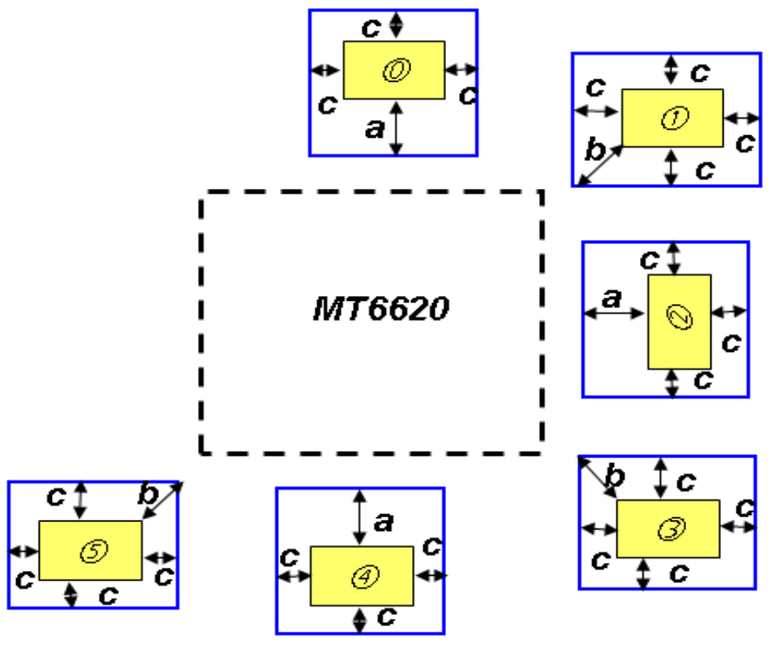
		Done	Item			
SCH	General	□	2rd source 请使用MTK QVL中的			
		□	RTC_clock请使用always on、2.8V domain的有32K output function 的GPIO，6620_VRTC power接BB的VRTC电源			
		□	Fsouce请接地			
	WiFi	□	WIFI TX 和SPDT之间请预留π型匹配			
		□	WIFI RX 与SPDT之间预留下地电感位置调整匹配			
		□	GPS/WIFI/BT建议预留39nH电感提升ESD性能，若ANT RF trace走线比较好的话，可以使用π匹配位置			
		□	WIFI T/RX SPDP控制 pin建议添加8.2pf电容下地			
		□	BPF后端、SPDT的output和in(out，RF1，RF2)请务必添加18pf隔直电容以防有直流到RF 通路影响RF performance			
		□	天线处预留π型匹配			
		□	SPDT Logic	ANTSEL_1		ANTSEL_0
			TX	1		0
			RX	0		1
		□	clock setting	XTEST	EEDI	ANTSEL_3
			2.8V TCXO or OSC	0	0	0
			1.8V TCXO or OSC	0	1	0
		□	WIFI host interface setting	XTEST	ANTSEL_2	ANTSEL_1
			SDIO1	0	0	0
			SDIO2	0	0	1
		□	EEDI 建议预留0ohm上拉至MT6620_2V8,以方便兼容1.8V TCXO or OSC			
		□	For MT6573/MT6515 platform，SDIO不需要上拉电阻，For external platform需要预留上拉电阻。			
		□	WIFI 使用SDIO1，power domain是DVDD_SDIO1(2.8V),速率最高可到50M，所以clock需要FB，clock FB务必上下左右包地保护并且从6620			
		□	WIFI_INT_B、Reset是1.8V power domain，BB端interface的power domain应与之一致			
		□	WIFI RF Part、PA、及I/O电源部分请按照ref.design添加 bypass CAP。			
		□	WIFI 使用SDIO1 power			
		□	若使用external LDO为6620 I/O供电，LDO enable建议使用6620 PMU enable(2.8V、default PD)或者使用其他reset时为PD，power			
	BT	□	BGF_INT_B power domain是1.8V，请接到BB 1.8V的EINT上			
		□	SYSRST_B请接到BB的DARST			
		□	BT PCMOUT接到BB PCMIN,PCMIN接到BBPCMOUT，请务必不要接反			
		□	BT UTXD对于BB URXD，URXD对应BB UTXD，请保证连接的正确性			
		□	BT I/O、RF电源输入pin请按照ref.design添加bypass电容			
		□	BT/common host interface setting	XTEST		ANTSEL_0
			UART1	0		0
	GPS	□	GPS_SYNC(F13)请接到BB对应pin上，ex;MT6573,BPI8			
		□	TCXO使用MTK QVL中的并使用TCXO_LDO供电			
		□	TCXO与clock in需要添加1nf隔直电容			
		□	RF_INN_GPS(B13)接地			
		□	若需要过AGPS IOT认证，需要添加外部LNA，电路图请参考ref.design并default使用TCXO作为power及enable, For			
		□	GPS I/O、RF电源输入pin请按照ref.design添加bypass电容			
		□	GPS天线处预留39nf位置提高ESD性能			

	FM	□	FM_TX_OUT上靠近MT6620处预留72nH电感做匹配，建议使用高Q值电感
		□	FM TX建议使用FPC天线
		□	FM De-sense: Series bead for PMU internal boost input VBAT path ; Series bead for external boost PWM signal path. Bead is put close to radiation
		□	[MT6620]Audio R/L trace both add one more bead(ex. BLM18BD252SN1) close to BB chip to solve 104MHz desense.
		□	Please series R1029/R1031 200K resistors in FM_TX audio path to prevent signal distortion.
		□	Please shunt 50K resistors near the 6573 for the FM_RX audio path .
		□	使用耳机地当天线，FM_ANT路径靠近耳机接口端需要预留TVS管，CpF<5pF
		□	FM RX_N接到耳机端的audio_GND,靠近耳机端预留0ohm电阻以方便layout
		□	若没有ATV function，建议使用analog audio interface，I2S多耗电。
	PMU	□	PMU_EN请使用power domain 为2.8V，default PD的GPIO,并添加910K电阻下地，以防止误动作enable PMU
		□	6620 PMU 电源VBAT建议添加4.7uf bypass 电容
		□	6620 LDO output请按照ref.design 添加输出电容
		□	FM_LDO(N3)、BT_PA_LDO(M2)bypass电容是2.2uf
		□	LXBK上电感是Buck的功率电感，请使用SMD type 功率电感并确保其过流大于400mA。
PCB	WIFI	□	WIFI T/RX匹配需靠近chip摆放。TX,RX走线需要做50ohm阻抗控制。
		□	WIFI SDIO i速率最高会达到50M，SDIO clock需要上下左右包地保护，SDIO data线因速率比较高请注意远离易被干扰的走线
		□	SDIO clock FB请直接接到6620，并上下左右包地保护，远离强干扰源
		□	RX_2G_IN请直接打孔到主地
		□	6620 power input处电容建议靠近6620摆放并且接入主地，ex:WIFI_AVDD13、WF_PA_VCC，请星型走线
		□	WIFI的BPF，switch 请放在屏蔽框内
	BT	□	BT_TRXIN请直接打孔到主地，TRX_IP若不用可以floating
		□	BT power input bypass 电容请靠近6620 摆放并且接入主地
	GPS	□	GPS RF_INP_GPS 匹配尽可能靠近6620摆放，RF_INN_GPS直接打孔到主地
		□	TCXO 电源bypass电容可能靠近TCXO VCC
		□	TCXO的GND请在L1连接在一起后一起打孔入主地，TCXO下面请挖空到主地，另外TCXO周围也需要挖空. 且TCXO placement 远离3G/2G PA
		□	若添加external LNA，请靠近Antenna端
	FM	□	FM_TXOUT(N13)短天线，72nh电感靠近IC,做50ohm阻抗匹配。
		□	Keep FM Antenna RF path away from power source.
		□	[MT6620]Keep FM Antenna(audio jack/ usb/FPC) away from other Antenna like WLAN/BT/GSM Antenna, to avoid desense.
		□	FM_RX_IN_P,FM_RX_IN_N,(L13,M13),长天线，差分走线，包地，可以不做阻抗匹配。
		□	FM audio input (L10,L11) ,FM_AUIN_L,FM_AUIN_R分开包地，且两根走线尽量隔远一些，一定不要走成差分形式。
		□	[MT6620]FM Long Antenna/ Short Anteena RF trace, should keep away from VBAT and other power source.
	PMU	□	VREF下地电容建议直接打孔入主地，不要和其他GND相连
		□	电源AVDD55_SMPS(L2),最大电流350mA, 线宽尽可能粗(>=14mil)
		□	VBAT bypass电容尽可能靠近6620，并且GND_SMPS(K1)出线后先和bypass CAP连接后再单点下地
		□	电源AVDD55_MISC(M1),最大电流450mA, 线宽尽可能粗（>=18mil）
		□	电源BUCK(L1&M4) ，最大电流400mA, 线宽尽可能粗（>=15mil） ,bypass电容请靠近M4
		□	WIFI_AVDD33(K2,A1,C2,E1),最大电流450mA，
		□	电源CLDO(N4,J5,F8),最大电流200mA，N4是输出Pin，J5,F8是输入端Pin,滤波电容放在靠近电源Pin的地方。
		□	电源WIFI_AVDD13(N5,G1,C4,E4,E6,E7),最大电流150mA，N5是输出Pin，G1,C4,E4,E6,E7是输入Pin,滤波电容放在靠近电源pin的地方

	General	□	电源BT_AVDD13(N6,A9,B7),最大电流50mA，N6是输出端，A9,B7是输入端，相应的滤波电容要靠近电源Pin。
		□	电源GPS_AVDD13(K5,A12,C12),最大电流50mA，K5是输出端，A12,C12是输入端，相应的滤波电容要靠近电源Pin
		□	电源FM_AVDD13(K6,M11),最大电流50mA，K5是输出端，M11是输入端，相应的滤波电容要靠近电源Pin。
		□	所有电源走线请按照1A/40mil规则来走
Placement	WIFI	□	WIFI T/RX匹配需靠近chip摆放。TX,RX走线需要做50ohm阻抗控制。
		□	6620 power input处电容建议靠近6620摆放并且接入主地，ex:WIFI_AVDD13、WF_PA_VCC，请星型走线
		□	WIFI的BPF，switch 请放在屏蔽框内
	BT	□	BT power input bypass 电容请靠近6620 摆放并且接入主地
	GPS	□	TCXO 电源bypass电容可能靠近TCXO VCC
		□	TCXO的GND请在L1连接在一起后一起打孔入主地，TCXO下面请挖空到主地，另外TCXO周围也需要挖空. 且TCXO placement 远离3G/2G PA
		□	GPS external LNA，请靠近Antenna端
	FM	□	Keep FM Antenna RF path away from power source.
		□	[MT6620]Keep FM Antenna(audio jack/ usb/FPC) away from other Antenna like WLAN/BT/GSM Antenna, to avoid desense.
		□	FM audio input (L10,L11) ,FM_AUIN_L,FM_AUIN_R分开包地，且两根走线尽量隔远一些，一定不要走成差分形式。
		□	[MT6620]FM Long Antenna/ Short Anteena RF trace, should keep away from VBAT and other power source.
	PMU	□	VREF下地电容建议直接打孔入主地，不要和其他GND相连
		□	电源AVDD55_SMPS(L2),最大电流350mA, 线宽尽可能粗(>=14mil)
		□	VBAT bypass电容尽可能靠近6620，并且GND_SMPS(K1)出线后先和bypass CAP连接后再单点下地
		□	电源AVDD55_MISC(M1),最大电流450mA, 线宽尽可能粗（>=18mil）
		□	电源BUCK(L1&M4) ，最大电流400mA, 线宽尽可能粗（>=15mil） ,bypass电容请靠近M4
		□	WIFI_AVDD33(K2,A1,C2,E1),最大电流450mA，
		□	电源CLDO(N4,J5,F8),最大电流200mA，N4是输出Pin，J5,F8是输入端Pin,滤波电容放在靠近电源Pin的地方。
		□	电源WIFI_AVDD13(N5,G1,C4,E4,E6,E7),最大电流150mA，N5是输出Pin，G1,C4,E4,E6,E7是输入Pin,滤波电容放在靠近电源pin的地方
		□	电源BT_AVDD13(N6,A9,B7),最大电流50mA，N6是输出端，A9,B7是输入端，相应的滤波电容要靠近电源Pin。
		□	电源GPS_AVDD13(K5,A12,C12),最大电流50mA，K5是输出端，A12,C12是输入端，相应的滤波电容要靠近电源Pin
		□	电源FM_AVDD13(K6,M11),最大电流50mA，K5是输出端，M11是输入端，相应的滤波电容要靠近电源Pin。

Case1: If TCXO and Main PAs Distance > 5cm

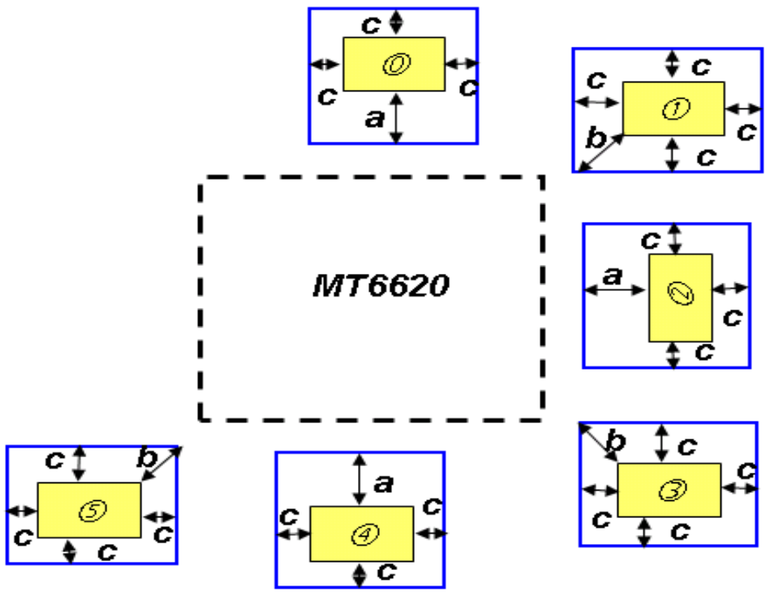
1.⓪①②③④⑤ is TCXO possible placement related to MT6620
2.GND clearance "a ": 3 mm
3.GND clearance "b" : 2 mm
4.GND clearance "c" : 1.5 mm



1.TCXO placement is 1st priority when MT6620 placement starts in portable device
2.TCXO had better locate in less traces routing area for each PCB layer. This will make layout rule implantation easier
3.The blue frame around TCXO is PCB forbidden area for L1 to Ln-1. n is PCB total layer No. GND clearance suggestions are shown as left.
4.Avoid other signal traces passing TCXO forbidden area
5.Avoid other heat sources putting on opposite PCB surface layer nearby TCXO
6.To put R/L/C components in TCXO forbidden area is allowed
7.Recommend TCXO package size : 2520 or 2016
8.Any signal trace/power trace/GND trace route to TCXO with 4mil trace width
9.Route TCXO clock trace with well GND shielding as possible
10.TCXO should be in the shielding cover
11.TCXO PCB footprint with 4 pads is better than that with 6 pads for thermal isolation consideration
12. Use 4mil trace to connect TCXO GND pad and then using 4 mil trace connect to surface GND layer with less heat .
13. Put TCXO VCC bypass cap near forbidden area edge in TCXO VCC pad direction and to be grounding via surface layer. Then using 4mil trace connect to TCXO VCC pad.
14.The lower percentage layout rule realization, the poorer GPS thermal immunity. i.e. GPS performance will degrade to some extent

Case2 : If TCXO and Main PAs Distance < 5cm

1.⓪①②③④⑤ is TCXO possible placement related to MT6620
2.GND clearance "a ": 3 mm
3.GND clearance "b" : 2 mm
4.GND clearance "c" : 2 mm



1.Main PAs and other heat sources that operation current over 200mA has to be 2cm at least away from TCXO
2.The blue frame around TCXO is PCB forbidden area for L1 to Ln. n is PCB total layer No. GND clearance suggestions are shown as left.
3.Reserve a surface solder layer with trace width 0.8mm along forbidden area peripheral opposite TCXO side for conductive cloth/copper foil paste
4. Conductive cloth has better thermal isolation ability than PCB GND layer
5.Other heat sources should be put outside forbidden area
6.Other layout rule please refer to previous page "MT6620 TCXO Layout Guide (Main PAs Distance > 5cm) " except item 3.

	Done	Item
SCH + PCB	□	DAT, CMD, CLK in a group, priority is (DAT + CLK) + CMD
	□	CLK must be grounded in both sides to reduce interference
	□	Keep trace difference of DAT, CMD, CLK to be < 500mil
	□	Check eMMC spec for VDDi cap value
	□	Add ESD device (TVS or varistor <15pF) on CLK/CMD/DAT/MCINS paths
	□	Reverse the damping resistor position on the CLK, CMD, DAT to fine tune the AC timing.
	□	If pull-up resistor is needed, please pull up to MT6515 side power. Do not pull up to SD card side power.
	□	Reserve a damping resistor position on the eMMC CLK interface
	□	MSDC 若沒有接 SD INS pin請在機構設計確認不可以熱差拔SD card
	□	eMMC core power(VCC) is suggest to be 3.3V
	□	eMMC I/O power(VCCQ) is suggest to be 1.8V

Android系统请不要使用SD卡热插拔的设计

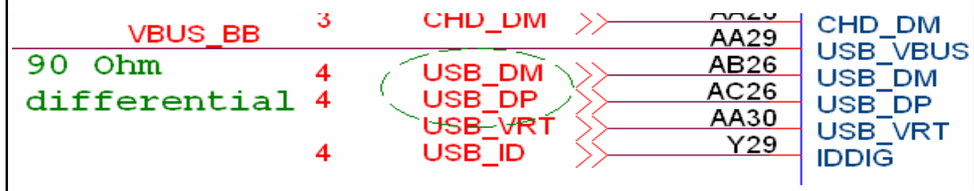
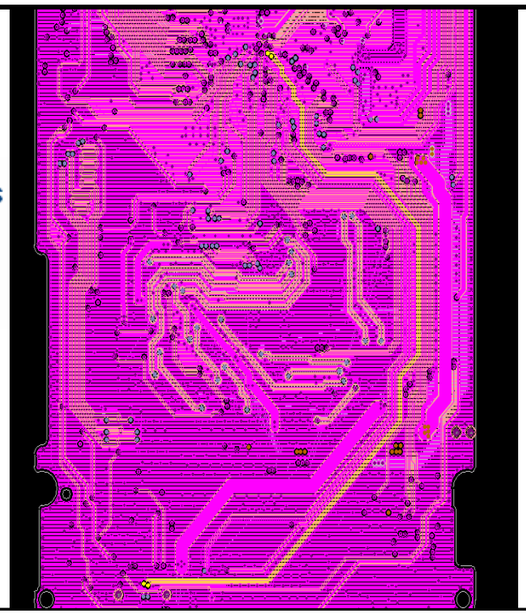
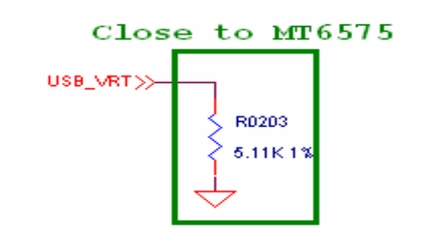
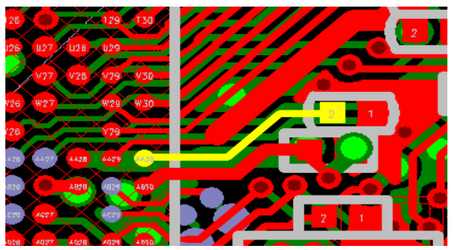
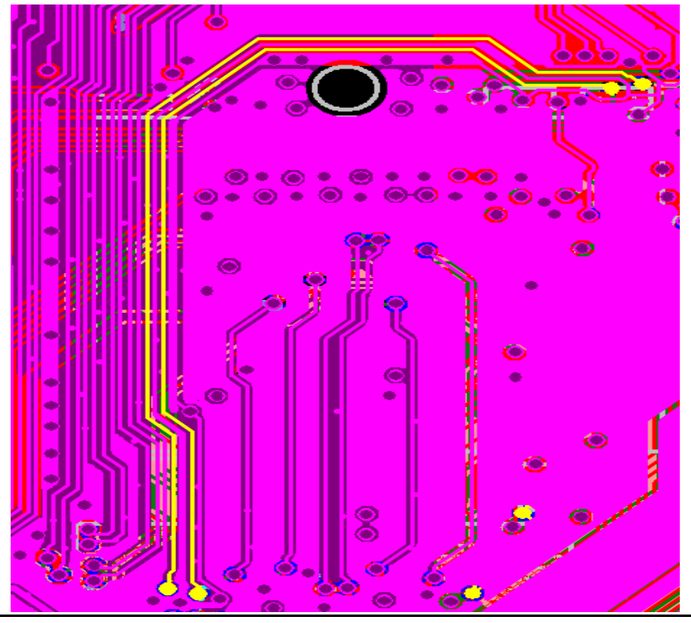
- 以市面上的HTC Sensation举例，它也完全跟MTK目前一樣是Google default行為 ， 在一些SD卡熱插拔操作下，會导致文件系統损坏 reboot or crash. 所以HTC sensation 都有特別注明： you must first "un-mount" the storage card before removing, it to prevent corrupting or damaging the files in the storage card.
- Android本身是不建议支持熱插拔， 在插拔SD卡期间， 應用如果沒access SD卡大概就不會有事， 以HTC G13或Sensation的設計，需打開背蓋才能取出T卡， 這時user大概也不會開什麼應用， 如果正在run 的AP是装在SD卡上， 或者正在access SD卡，就会导致文件系統损坏
- 如果因ID或ME限制，讓user有機會熱插拔SD卡， 請在手機或說明書上加註警示， 避免user錯誤使用，並且在硬件上仍舊把MCINS接上， 降低不當使用而導致系統不正常狀況發生.

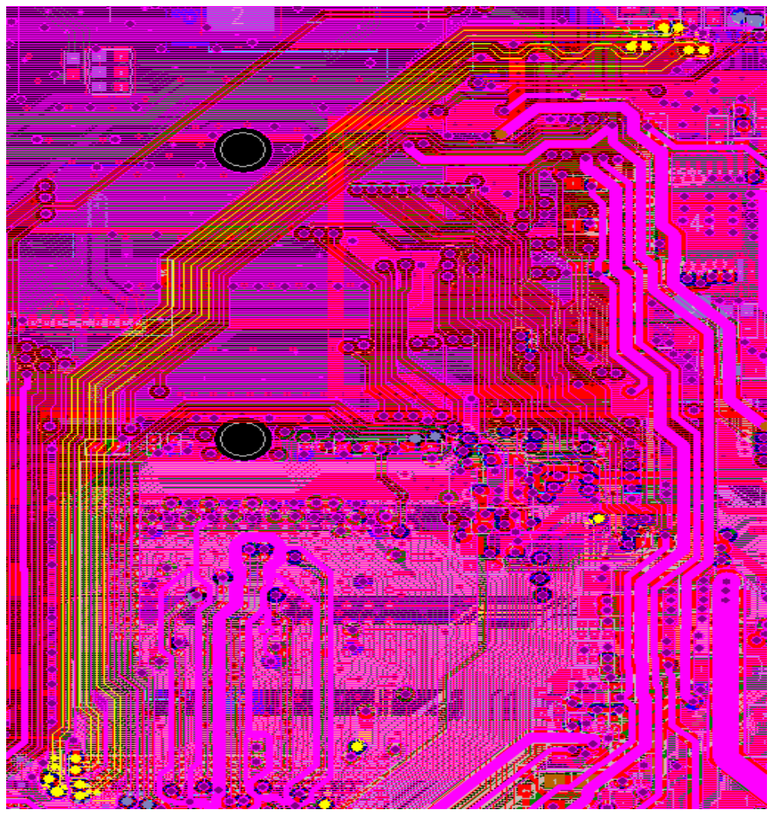
•Please put the SD card connector under the battery. If the SD card will be removed, the battery should be removed first.

		Done	Item
SCH	RTP	□	确认主芯片的XP/XM连接至TP的XL/XR，YP/YM连接至TP的YU/YD。除非有特别设计，一般接法为XP=XR, XM=XL, YP=YU, YM=YD。
		□	在XP/XM/YP/YM上，建议预留ESD diode，但预设不上件。
		□	ESD diode的电容值建议小于100pF
		□	可在XP/XM/YP/YM至TP connector的中间留0ohm电阻，如有与TP相关的EMI干扰，可改上bead。如无干扰问题，第二版可移除。
	CTP	□	确认I2C的I/O voltage level与CTP controller I/O voltage level是匹配的
		□	确认I2C的pull up 电阻至少4.7Kohm
		□	确认各GPIO的I/O voltage level与CTP controller I/O voltage level是匹配的
		□	若所选用的CTP controller在system sleep时必须断电，则须确认 CTP_RESETB, EINT_CTP的GPIO在system sleep时，可以被配置成input with pull-down enabled或是output low。
		□	可在SCL/SDA/RESETB/EINT上，预留ESD diode，但预设不上件。
		□	如果选择在system sleep时，让CTP controller进入power off mode，CTP controller 所连接之1.8V/2.8V power必须在system sleep时可以被关闭。如现有PMU无法支持，须采用外部LDO，建议使用单颗two channel的LDO with enable pin。
		□	确认CTP controller的DVDD(1.8V)和AVDD (2.8V)各自连接至少1uF的电容，并靠近TP connector摆放。实际所需的电容值，依各家CTP controller而定。如无法确定，建议摆放1uF for DVDD和 2.2uF for AVDD。
		□	如采用Goodix COB solution，务必另外参考Goodix提供的COB reference design。
PCB	RTP	□	XP/XM/YP/YM应尽可能并排走线，避免与其他AC信号(尤其是频率在10KHz到10MHz之间)交会或平行。
		□	如果空间允许，XP/XM/YP/YM走内层，上下左右都包GND。
		□	XP/XM/YP/YM出IC后，线宽至少4mil。
		□	如有预留ESD diode，diode须靠近TP connector之对应pin摆放。
		□	TP connector尽可能远离RF天线区域，避免RF干扰。
	CTP	□	如有预留ESD diode，diode须靠近TP connector之对应pin摆放。
		□	TP connector尽可能远离R天线F区域，避免RF干扰。
		□	Bypass capacitor须靠近TP connector之对应pin摆放。
		□	AVDD/DVDD的power trace，线宽至少8mil。
		□	如采用外部LDO，相关power circuit须远离RF天线区域。
		□	如采用Goodix COB solution，务必另外参考Goodix提供的COB layout rule。
Placement	RTP	□	TP connector尽可能远离RF天线区域，避免RF干扰。如果RF天线在手机下端，建议TP connector放置在手机上端。
		□	如有预留ESD diode，diode须靠近TP connector之对应pin摆放。
		□	如有预留串接0ohm(或bead)，须靠近TP connector之对应pin摆放。
	CTP	□	CTP controller和TP connector尽可能远离RF天线区域，避免RF干扰。如果RF天线在手机下端，建议CTP controller和connector放置在手机上端。
		□	Bypass capacitor须靠近TP connector之对应pin摆放。
		□	如有预留ESD diode，diode须靠近TP connector之对应pin摆放。
		□	如采用外部LDO，相关power circuit须远离RF天线区域。
		□	如采用Goodix COB solution，controller建议置放在shielding cover里。
		□	如采用Goodix COB solution，务必另外参考Goodix提供的COB layout rule。

		Done	Item
SCH	Camera	□	MT6515有四组LDO给摄像头供电，务必注意VCAMA, VCAMD, VAMIO及VCAMAF的设置连接正确
		□	靠近sensor connector端务必有100nF与2.2uF (Reserve)的decouple 电容于摄像头供电端
		□	EMI filter for Camera is recommand for better de-sense performance
		□	Parallel EMI filter cap. maximum loading < 30pF
		□	MIPI EMI filter cap. maximum loading < 3pF
		□	Suggest to use LC type EMI filter with low DCR, 因为Camera MCLK, PCLK是高速时钟信号
	USB	□	选用小于3pF的TVS在DP, DM路径上
		□	USB_VBUS不可floating, 仅使用device mode, 请接至VUSB_6575
		□	DP, DM不需要串电阻, 如要串请优先上0-ohm
		□	使用OTG或host时, 确认EINT26~29不可使用
	MEMS and light sensor	□	Sensor供电端请预留0R及decouple电容的RC滤波线路
		□	请确认同组I2C上的device address是否有相冲突
		□	TAOS的psensor和BOSCH的gsensor 若有共享,需再 Psensor和Gsensor 的SCL SDA线上均串联300Ω电阻
		□	I2C总在线须留4.7K pull high电阻
PCB	Camera	□	VCAMA电源需左右包GND；维持较少的换层结构连接到sensor connector
		□	VCAMA 与VCAMD的滤波电容放置靠近sensor connector端并电容接地端需直接有个大Via接到main ground layer；
		□	CMMCLK 与 CMPCLK各需左右两侧包GND并维持较少的换层结构连接到sensor connector与baseband； serial sensor则为CMCLK 与CSK各需左右包GND
		□	非相关讯号走线请勿走在其pad的L2层面下, 降低noise-couple的影响；
		□	尽可能保持connector旁的GND完整性, 减少表层走线距离
		□	确认main/sub camera的长边与LCM的长边摆放一致
		□	MIPI走线,每对需走100 ohm差分,上下左右包地, 并减少换层
		□	MIPI走线长度小于3000mil
		□	MIPI走线,对与对之前长度差要小于100mil
	USB	□	TVS 靠近USB connector
		□	USB走线必须阻抗为90-ohm差分, 上下左右包地, 并减少换层
	MEMS and light Sensor	□	M sensor的摆放须远离磁性物质, 以免对地磁的感应受影响, 可请vendor做磁场分析
		□	玻璃印刷穿透率高于55% for IR与10% for可见光
Placement	Camera	□	Camera sensor摆放位置请远离RF天线, 避免TX功率干扰
		□	EMI filter摆放位置尽量靠近camera connector
		□	Power 稳压电容靠近connector摆放
		□	确认main/sub camera的长边与LCM的长边摆放一致
	USB	□	TVS diode 靠近connector摆放
		□	USB connector摆放位置远离高EMI组件, 如RF天线. Camera sensor
	MEMS and light Sensor	□	M sensor的摆放须远离磁性物质, 如speaker. Vibrator或软磁LCM背盖, 以免对地磁的感应受影响
		□	Ambient light sensor尽可能远离LCM, LCM的漏光可能造成可见光环境参数的变异

MT6515 走线重点部分图示

USB	**USB走线需左右下包地, 并维持90-ohm差分阻抗**	 
	VRT 5.11K 1%靠近MT6515摆放	 
	MCLK. PCLK需上下左右包地,避免干扰	

Camera	**MIPI走线做100 ohm阻抗控制，长度小于3000mil，对与对间长度差小于100mil**	

	Done	Item
SCH	□	Reset(pin38), PAD_PU(pin10)接到BB GPIO上，一定不要与其它模组共享，且建议使用默认为PD的GPIO。pin10 为Vcore LDO enable pin,只接受2.8V GPIO control
	□	I2C(pin36/37)建议与Camera共享， pull high 电阻也可与Camera I2C 共享
	□	使用Vcore LDO时，pin11请接1.5/1.8/2.8V，pin12为Vcore LDO 1.2V输出。如欲使用external Vcore LDO时，P11/12/26接至外部1.2V电源。ATV输出的电源不能供给ATV以外的其它Module使用。
	□	pin 11/12是Vcore LDO输入/输出pin，每1pin都需要1uF滤波电容。Pin21/31为IO power pin，每1pin都需要1uF滤波电容。pin2/9/13/40各用1颗0.1uF滤波电容。
	□	VIO 有如下使用状况,请接 a. 如CAM bus/I2S 都是在 2.8V VIH时, ATV_VIO 接BB 2.8VIO b. 如CAM bus/I2S 都是在 1.8V VIH时, ATV_VIO 接BB 1.8VIO
	□	务必使用MTK验证过的RF部分的inductor与Xtal
	□	天线需要放置防静电TVS管，并预留匹配电路；如FM module需要共享拉杆天线，接入点应在匹配电路之后
	□	GPIO0(pin20)需预留电阻到地，作为CLK模式选择。电阻NC时，采用XTAL；电阻0ohm时，为共CLK模式。当使用外部CLK输入时需要使用二阶阻容滤波器，当使用XTAL时请将该滤波器NC。
	□	采用I2S输出时，pin16-18连接到BB，不使用时pin16-18 NC，采用Analog声音输出必须使用下二阶LPF(请留意组件值是否正确),不使用时请删除此电路，pin14/15 NC。
PCB	□	Co-clock: MT6256给MT5193的26M 走线对应的参考地 尽量完整，尽量作好走线的保护与隔离，并且多打GND VIA，平行走线需要有GND VIA隔离。
	□	Camera D0~D7, PCLK/HSYNC/VSYNC等信号应尽量走在内层，相邻表层包地包覆，PCLK走在表层请用GND线保护，减少EMI。
	□	ANT到RF匹配之间的走线应尽量短（减少信号损失，避免引入干扰），阻抗应控制在 50ohm
	□	RF区域的下方请不要走信号线, 如果要走线，至少要隔两层GND（4层板建议不要有线跨过RF区)
	□	ATV模组下面那层地是作为ATV的主地，这层地要尽量完整（为保证这层地完整建议 Camera bus/VCCRF/VIO走在其它层，Crystal 如果要预留,下面那一层不需割地 ），EPAD 应多打GND VIA 增加接地性，尽量不要有影响EPAD打地孔的走线穿过EPAD
	□	ATV的供电线路尽量遵循星形原则
	□	Bypass CAP尽量靠近电源pin, 每个Bypass CAP要有单独的GND VIA到主地层，并且靠近Bypass CAP，Pin 12&13 Bypass CAP GND有独立的GND via打到主地且用keep out区隔开不铺铜
	□	在layout四层板的PCB, 电源走线请走Top layer与Layer 3, 让Layer 2的GND尽量完整， 四层通孔板要注意 LCD/Camera FPC 不要盖到ATV上下或附近，防止通过通孔辐射干扰
	□	layer 1 ATV IC下方区域不铺铜，防止出现“死铜”，pin5的地请直接打孔到地层，不要在顶层直接与E-pad连接
Placement	□	手机上LCM 模组的connector & FPC 应尽量远离ATV RF input及天线,并尽量不要与ATV放在同一层，在LCM的背面及FPC的下方与周围的GND上应开大片solder mask,增强LCM and FPC 接地，降低EMI
	□	手机上Camera 模组的connector & FPC应尽量远离ATV RF input 及天线,并尽量不要与ATV放在同一层，减少EMI干扰
	□	pin 14/15 所接LPF应尽量靠近IC摆放，如实在放不下，至少第1级RC应靠近IC摆放。此LPF电路请尽量远离RF区域
	□	天线PAD应尽量放在PCB的四角，PAD周围3mm内不能放组件，5mm内建议不放喇叭、电池、麦克风等金属件
	□	天线PAD下方所有层都不能铺铜及走线，以免造成信号损失；但如果天线PAD离LCM Connector太近则仅在LCM Connector所在层铺铜。