MT6329 PMIC Data Sheet

Version: 0.4
Release date: 2012/01/20

Revision	Date	Author	Description
0.1	2011/09/30	Trevor Chou	Initial
0.2	2011/12/16	Trevor Chou	1. Update Package Dimensions 2. Update Electrical Characteristics 3. Update Register table
0.3	2011/12/28	Trevor Chou	1. Modify VRF LDO functional description 2. Update Buck Converter Un-Use application note
0.4	2012/01/20	Trevor Chou	1. Modify Figure 3: Power-on/off control sequence

Lists of Figures

Lists of Tables

- Handles all 2G/3G/smart phone baseband power management
- Input range: 3.4 ~ 4.3V
- Charger input of up to 10V
- 5 buck converters and 21 LDOs optimized for specific 2G/3G/smart phone subsystems
- Dual-channel, 3.7V 0.7W into 8Ω Class AB/D audio amplifiers
- Flexibility for various configurations of backlight LED drivers: 6ISINK/10WLED boost controller
- I2C interface
- Pre-charge indication
- Li-ion battery charging function
- Multi-purpose pins support either current sinks or analog switches
- Multi-purpose pins support either an RGB LED driver or an audio receiver
- VPROC with DVFS control
- Over-current and thermal overload protection
- Programmable under voltage lockout protection
- Watchdog timer
- Flexibility hardware PMIC reset function
- Power-on reset and start-up timer
- Precision voltage, temperature, and current measurement fuel gauge
- 155-pin TFBGA package

Ideal for power management of 2G, 3G, smart phones and other portable systems.

MT6329 for MediaTek 3G smart phone platform, MT6575.

MT6329 is a power management system chip optimized for 2G/3G handsets and smart phones, especially those based on the MediaTek MT6575 system solution. MT6329 contains 15 buck converters and 21 LDOs, which are optimized for specific 2G/3G/smart phone subsystems.

MT6329 provides dual-channel, 0.7W into 8Ω, high efficiency Class AB/D audio amplifiers and flexibility for various applications of backlight LED drivers. It supports up to 6 WLEDs in parallel or alternative series 10WLED configurations. Flexible control keeps high power efficiency while supporting multiple drivers.

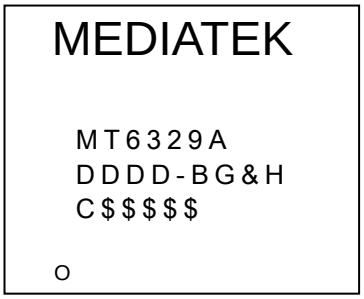
Sophisticated controls are available for power-up, battery charging and the RTC alarm. MT6329 is optimized for maximum battery life. The selectable 1-step or 2-step RTC LDO design makes MT6329 suitable for different RTC modules in BB chips. It allows the RTC circuit to stay alive without a battery for several hours. The battery charger in MT6329 supports lithium- ion (Li-ion) battery and provides pre-charge indication. The charger input voltage can be up to 10V and allows USB charging, too.

Some multi-purpose pins enable MT6329 to be configured in various applications. MT6329 implements dedicate analog switches, KPLED and 450mA FLASH LED driver.

MT6329 adopts I2C interface to control buck converters (dedicate 2 pins DVFS control and 3 pins PA_SEL control), LDOs, Class AB/D, various drivers and charger. Besides, it provides enhanced safety control and protocol for handshaking with BB.
MT6329 is available in a 155-pin TFBGA package. The operating temperature ranges from -25 to +85°C.

Order #	Marking	Temp. range	Package
MT6329A		-25 ~ +85°C	TFBGA - 155L

MT6329A



DDDD: Date code
$$$$$: LOT No.

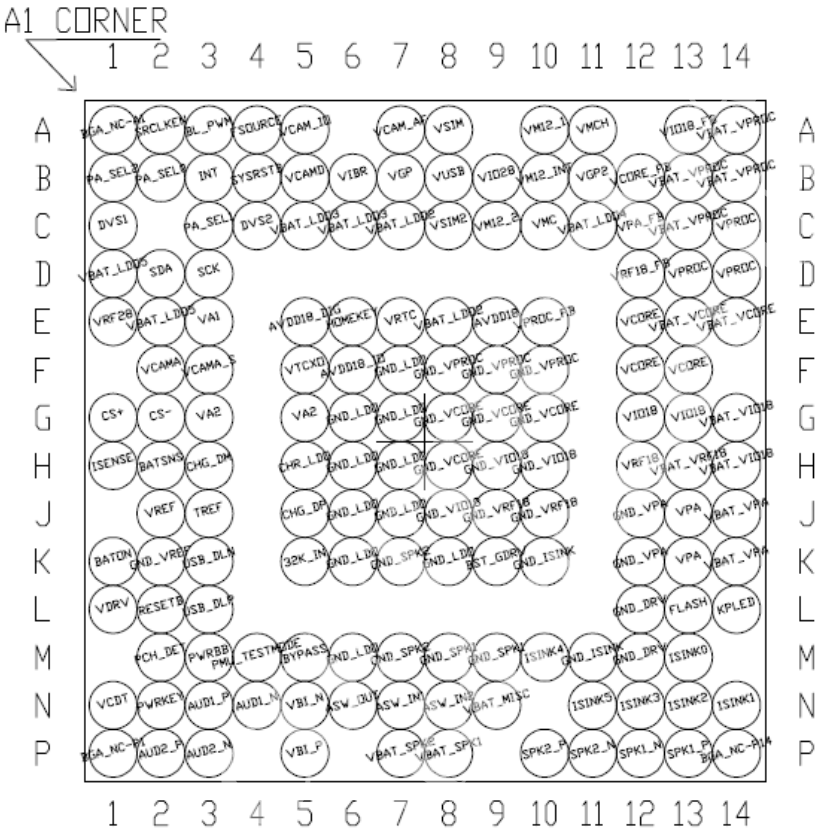


Figure 1: MT6329 TFBGA 155 (7.1x7.1mm) pin assignment

Table 2: MT6329 pin descriptions

Ball	Symbol	I/O	Description
A1	BGA_NC-A1	I/O	NC
A2	SRCLKEN	I	Source clock enabling signal
A3	BL_PWM	I	External backlight CABC PWM control input signal
A4	FSOURCE	I	Connects to AVDD18_DIG in normal mode
A5	VCAM_IO	O	LDO output used for camera IO
A7	VCAM_AF	O	LDO output used for camera auto-focus
A8	VSIM	O	LDO output used for SIM card
A10	VM12_1	O	LDO output used for 1.2V DRAM
A11	VMCH	O	LDO output for SD 3.0 memory card
A13	VIO18_FB	I	VIO18 feedback input
A14	VBAT_VPROC	PWR	VBAT for VPROC
B1	PA_SEL2	I	PA output voltage selection
B2	PA_SEL0	I	PA output voltage selection

Ball	Symbol	I/O	Description
B3	INT	O	Interrupt output
B4	SYSRSTB	I	External system reset input pin (active low)
B5	VCAMD	O	LDO output used for camera digital
B6	VIBR	O	LDO output used for vibrator
B7	VGP	O	LDO output reserved for further system use
B8	VUSB	O	LDO output used for USB
B9	VIO28	O	LDO output used for 2.8V IO
B10	VM12_INT	O	LDO output used for 1.2V SRAM
B11	VGP2	O	LDO output reserved for further system use
B12	VCORE_FB	I	VCORE feedback input
B13	VBAT_VPROC	PWR	VBAT for VPROC
B14	VBAT_VPROC	PWR	VBAT for VPROC
C1	DVS1	I	VPROC output voltage selection
C3	PA_SEL1	I	PA output voltage selection
C4	DVS2	I	VPROC output voltage selection
C5	VBAT_LDO3	PWR	VBAT for VIBR, VCAM_IO, VCAMD, VRTC and IBIAS_DLDO1
C6	VBAT_LDO3	PWR	VBAT for VIBR, VCAM_IO, VCAMD, VRTC and IBIAS_DLDO1
C7	VBAT_LDO2	PWR	VBAT for VIO28, VSIM, VSIM2, VUSB, VGP and VCAM_AF
C8	VSIM2	O	LDO output used for 2nd SIM card
C9	VM12_2	O	LDO output for 1.2V DRAM or AST3002
C10	VMC	O	LDO output for memory card
C11	VBAT_LDO4	PWR	VBAT for VMC, VMCH, VGP2 and IBIAS_DLDO2
C12	VPA_FB	I	VPA feedback input
C13	VBAT_VPROC	PWR	VBAT for VPROC
C14	VPROC	O	VPROC switching output
D1	VBAT_LDO5	PWR	VBAT for VA1, VA2, VCAMA, VTCXO, VRF28 and IBIAS_ALDO
D2	SDA	I	I2C serial data
D3	SCK	I	I2C serial clock
D12	VRF18_FB	I	VRF18 feedback input
D13	VPROC	O	VPROC switching output
D14	VPROC	O	VPROC switching output
E1	VRF28	O	LDO output for RF
E2	VBAT_LDO5	PWR	VBAT for VA1, VA2, VCAMA, VTCXO, VRF28 and IBIAS_ALDO
E3	VA1	O	LDO output for analog baseband
E5	AVDD18_DIG	O	LDO output bypass pin
E6	HOMEKEY	I	Homekey
E7	VRTC	O	LDO output for RTC

Ball	Symbol	I/O	Description
E8	VBAT_LDO2	PWR	VBAT for VIO28, VSIM, VSIM2, VUSB, VGP and VCAM_AF
E9	AVDD18	PWR	1.8V power input for VM12_1, VM12_2 and VM12_INT
E10	VPROC_FB	I	VPROC feedback input
E12	VCORE	O	VCORE switching output
E13	VBAT_VCORE	PWR	VBAT for VCORE
E14	VBAT_VCORE	PWR	VBAT for VCORE
F2	VCAMA	O	LDO output for camaera analog
F3	VCAMA_S	I	Sense input for VCAMA LDO
F5	VTCXO	O	LDO output for TCXO
F6	AVDD18_IO	PWR	1.8V IO power input for internal GPIO
F7	GND_LDO	GND	GND for LDO
F8	GND_VPROC	GND	GND for VPROC
F9	GND_VPROC	GND	GND for VPROC
F10	GND_VPROC	GND	GND for VPROC
F12	VCORE	O	VCORE switching output
F13	VCORE	O	VCORE switching output
G1	CS+	I	Fuel gauge positive current sense point
G2	CS-	I	Fuel gauge negative current sense point
G3	VA2	O	LDO output for analog baseband
G5	VA2_BUF	O	LDO output for analog baseband
G6	GND_LDO	GND	GND for LDO
G7	GND_LDO	GND	GND for LDO
G8	GND_VCORE	GND	GND for VCORE
G9	GND_VCORE	GND	GND for VCORE
G10	GND_VCORE	GND	GND for VCORE
G12	VIO18	O	VIO18 switching output
G13	VIO18	O	VIO18 switching output
G14	VBAT_VIO18	PWR	VBAT for VIO18
H1	ISENSE	I	Charging current sense input
H2	BATSNS	I	Battery voltage sense input
H3	CHG_DM	I	USB D- for BC1.1 standard
H5	CHR_LDO	O	Charger LDO output bypass pin
H6	GND_LDO	GND	GND for LDO
H7	GND_LDO	GND	GND for LDO
H8	GND_VCORE	GND	GND for VCORE
H9	GND_VIO18	GND	GND for VIO18
H10	GND_VIO18	GND	GND for VIO18
H12	VRF18	O	VRF18 switching output
H13	VBAT_VRF18	PWR	VBAT for VRF18
H14	VBAT_VIO18	PWR	VBAT for VIO18

Ball	Symbol	I/O	Description
J2	VREF	O	Internal reference bypass
J3	TREF	O	Battery thermal detection reference voltage
J5	CHG_DP	I	USB D+ for BC1.1 standard
J6	GND_LDO	GND	GND for LDO
J7	GND_LDO	GND	GND for LDO
J8	GND_VIO18	GND	GND for VIO18
J9	GND_VRF18	GND	GND for VRF18
J10	GND_VRF18	GND	GND for VRF18
J12	GND_VPA	GND	GND for VPA
J13	VPA	O	VPA switching output
J14	VBAT_VPA	PWR	VBAT for VPA
K1	BATON	I	Battery thermal detection input
K2	GND_VREF	GND	GND for reference
K3	USB_DLN	I	USB download key
K5	32K_IN	I	RTC 32K input used for fuel gauge operation
K6	GND_LDO	GND	GND for LDO
K7	GND_SPK2	GND	GND for speaker channel 2
K8	GND_LDO	GND	GND for LDO
K9	BST_GDRV	O	Boost controller gate drvie output
K10	GND_ISINK	GND	GND for ISINK
K12	GND_VPA	GND	GND for VPA
K13	VPA	O	VPA switching output
K14	VBAT_VPA	PWR	VBAT for VPA
L1	VDRV	O	Charger current drive output
L2	RESETB	O	Reset output
L3	USB_DLP	I	USB download key
L12	GND_DRV	GND	GND for flashligh and keypad LDO drivers
L13	FLASH	O	Flashlight open drain output
L14	KPLED	O	Keypad LED open drain output
M2	PCH_DET	O	Charging indicator current sink output
M3	PWRBB	I	Power on RTC domain latch signal
M4	PMU_TESTMODE	I	Test mode input (normal function should tie to GND)
M5	BYPASS	O	SPK common mode voltage bypass
M6	GND_LDO	GND	GND for LDO
M7	GND_SPK2	GND	GND for speaker channel 2
M8	GND_SPK1	GND	GND for speaker channel 1
M9	GND_SPK1	GND	GND for speaker channel 1
M10	ISINK4	O	Current sink channel 4 output
M11	GND_ISINK	GND	GND for ISINK
M12	GND_DRV	GND	GND for flashligh and keypad LDO drivers
M13	ISINK0	O	Current sink channel 0 output

Ball	Symbol	I/O	Description
N1	VCDT	I	Ratioed charger input voltage
N2	PWRKEY	I	Power key
N3	AUD1_P	I	Audio channel 1 differential input (positive)
N4	AUD1_N	I	Audio channel 1 differential input (negative)
N5	VBI_N	I	Voice differential input (negative)
N6	ASW_OUT	O	Analog switch output
N7	ASW_IN1	I	Analog switch input 1
N8	ASW_IN2	I	Analog switch input 2
N9	VBAT_MISC	PWR	VBAT for buck, driver and speaker controller
N11	ISINK5	O	Current sink channel 5 output
N12	ISINK3	O	Current sink channel 4 output
N13	ISINK2	O	Current sink channel 3 output
N14	ISINK1	O	Current sink channel 1 output
P1	BGA_NC-P1	I/O	NC
P2	AUD2_P	I	Audio channel 2 differential input (positive)
P3	AUD2_N	I	Audio channel 2 differential input (negative)
P5	VBI_P	I	Voice differential input (positive)
P7	VBAT_SPK2	PWR	VBAT for speaker channel 2
P8	VBAT_SPK1	PWR	VBAT for speaker channel 1
P10	SPK2_P	O	Speaker channel 2 differential output (positive)
P11	SPK2_N	O	Speaker channel 2 differential output (negative)
P12	SPK1_N	O	Speaker channel 1 differential output (negative)
P13	SPK1_P	O	Speaker channel 1 differential output (positive)
P14	BGA_NC-P14	I/O	NC

Stresses beyond those listed under Table 3 may cause permanent damage to the device. These numbers are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

Table 3: Absolute maximum ratings

Parameter	Conditions	Min.	Typical	Max.	Unit
Free-air temperature range		-40		85	°C
Storage temperature range		-65		150	°C
Battery input voltage range				4.3	V
ESD robustness	HBM	2,000			V
Charger input withstand				10	V

Parameter	Conditions	Min.	Typical	Max.	Unit
Thermal resistance from junction to ambient	In free air		39.8[1]		°C/W

Note: The device is mounted on a 4-metal-layer PCB and modeled per JEDEC51-9 condition.

Table 4: Operation condition

Parameter	Conditions	Min.	Typical	Max.	Unit
Operating temperature range		-25		85	°C

VBAT = 3.4 ~ 4.2V, minimum loads applied on all outputs, unless otherwise noted.
Typical values are at T_A = 25°C.

Table 5: General electrical specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Switch-off mode: supply current					
VBAT < 2.4 V	RTC LDO OFF		85		µA
2.4 V < VBAT < 3.2 V			35		µA
3.2 V < VBAT			60		µA
Operation ground current					
Standby	Low-power mode		300		µA
Under voltage (UV)					
Under voltage falling threshold 1	UV_SEL[1:0] = 00	2.8	2.9	3.0	V
Under voltage falling threshold 2	UV_SEL[1:0] = 01		2.75		V
Under voltage falling threshold 3	UV_SEL[1:0] = 10		2.6		V
Under voltage falling threshold 4	UV_SEL[1:0] = 11		2.5		V
Under voltage rising threshold	UV_SEL[1:0] = xx	3.1	3.2	3.3	V
Reset generator					
Output high		V_{IO}-0.4			V
Output low				0.2	V
Output current (Ioh)	Vo > VIO-0.4V		1		mA
Delay Time from switched-on to RESETB release		100	200	400	ms
Interrupt					
Output high		V_{IO}-0.4			V
Output low				0.2	V
Power key input					
High voltage		0.7*VBAT			V
Low voltage				0.3*VBAT	V
De-bounce time		25	50	200	
Control input voltage					
PWRBB input high		2.1			V
PWRBB input low				0.54	V
Other control input high (SRCLKEN, PA_SEL)		2.0			V
Other control input low (SRCLKEN, PA_SEL)				0.5	V
Thermal shut-down					
PMIC shut-down threshold			150		degree
SW high power latch threshold			125		degree
Interrupt threshold			110		degree

Parameter	Conditions	Min.	Typical	Max.	Unit
LDO enable response time			250		µs

Table 6: Regulator specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Boost controller					
Efficiency	Vin = 3.8V, 20mA, Vout = 35V		80		%
Switch on max. duty cycle			93		%
Regulated feedback voltage (int.)		0.28	0.3	0.32	V
Turn-on rise time				1	ms
OVP on threshold		1.1	1.2	1.3	V
OVP off threshold			1		V
Buck - VCORE					
Output voltage			1.1		V
Output current			1,000		mA
Turn-on overshoot				10	%
Load regulation		-10		10	%
Buck - VPROC					
Output voltage			1.25		V
Output current			1,500		mA
Turn-on overshoot				10	%
Load regulation		-6		6	%
Buck - VIO18					
Output voltage			1.8		V
Output current			1,000		mA
Turn-on overshoot				10	%
Buck - VRF18					
Output voltage			1.825		V
Output current			250		mA
Turn-on overshoot				10	%

Parameter	Conditions	Min.	Typical	Max.	Unit
Buck - VPA					
Output voltage		0.9		3.4	V
Output current	VOUT=3.4V		800		mA
Turn-on overshoot				10	%
ALDO - VRF28					
Output voltage		2.7	2.85	3	V
Output current			200		mA
Output noise	Freq = 10 Hz to 80 kHz Iout = 0.01Imax ~ full load		90		uVrms
PSRR	100 Hz < freq < 3 kHz Iout = 0.01Imax/0.5Imax		65		dB
	3 kHz < freq < 30 kHz Iout = 0.01Imax/0.5Imax		45		
Turn-on rise time	No load			240	us
ALDO - VTCXO					
Output voltage		2.7	2.8	2.9	V
Output current			40		mA
Output noise	Freq = 10 Hz to 80 kHz Iout = 0.01Imax ~ full load		90		uVrms
PSRR	100 Hz < freq < 3 kHz Iout = 0.01Imax/0.5Imax		65		dB
	3 kHz < freq < 30 kHz Iout = 0.01Imax/0.5Imax		45		
Turn-on rise time	No load			240	us
ALDO - VA1					
Output voltage		2.35	2.5	2.65	V
Output current			100		mA
Output noise	Freq = 10 Hz to 80 kHz Iout = 0.01Imax ~ full load		90		uVrms
PSRR	100 Hz < freq < 3 kHz Iout = 0.01Imax/0.5Imax		65		dB
	3 kHz < freq < 30 kHz Iout = 0.01Imax/0.5Imax		45		
Turn-on rise time	No load			360	us
ALDO - VA2					
Output voltage		2.35	2.5	2.65	V
Output current			100		mA
Output Noise	Freq = 10 Hz to 80 kHz Iout = 0.01Imax ~ full load		90		uVrms
PSRR	100 Hz < freq < 3 kHz Iout = 0.01Imax/0.5Imax		65		dB
	3 kHz < freq < 30 kHz Iout = 0.01Imax/0.5Imax		45		

Parameter	Conditions	Min.	Typical	Max.	Unit
Turn-on rise time	No load			360	us
ALDO - VCAMA					
Output voltage	VCAMA_SEL = 00	1.4	1.5	1.6	V
	VCAMA _SEL = 01	1.7	1.8	1.9	V
	VCAMA _SEL = 10	2.35	2.5	2.65	V
	VCAMA _SEL = 11	2.65	2.8	2.95	V
Output current			200		mA
Output noise	Freq = 10 Hz to 80 kHz Iout = 0.01Imax ~ full load		40		uVrms
PSRR	100 Hz < freq < 3 kHz Iout = 0.01Imax/0.5Imax		65		dB
	3 kHz < freq < 30 kHz Iout = 0.01Imax/0.5Imax		45		
Turn-on rise time	No load			1,000	us
Load transient response	IOUT = 1mA to full Load (15mA/usec)			40	mV
DLDO - VM12_1					
Output voltage		1.1	1.2	1.3	V
Output current			300		mA
PSRR	Freq = 217 Hz Iout = 0.01Imax/0.5Imax		40		dB
Turn-on rise time	No load			360	us
DLDO - VM12_2					
Output voltage		1.1	1.2	1.3	V
Output current			300		mA
PSRR	Freq = 217 Hz Iout = 0.01Imax/0.5Imax		40		dB
Turn-on rise time	No load			360	us
DLDO - VM12_INT					
Output voltage		1.1	1.2	1.3	V
Output current			360		mA
PSRR	Freq = 217 Hz Iout = 0.01Imax/0.5Imax		40		dB
Turn-on rise Time	No load			360	us
DLDO - VIO28					
Output voltage		2.65	2.8	2.95	V
Output current			100		mA
PSRR	Freq = 217 Hz Iout = 0.01Imax/0.5Imax		40		dB
Turn-on rise time	No load			360	us
DLDO - USB					
Output voltage		3.1	3.3	3.5	V
Output current			100		mA

Parameter	Conditions	Min.	Typical	Max.	Unit
PSRR	Freq = 217 Hz Iout = 0.01Imax/0.5Imax		40		dB
Turn-on rise time	No load			360	us
DLDO - SIM1					
Output voltage	VSIM1_SEL = 0	1.7	1.8	1.9	V
	VSIM1_SEL = 1	2.85	3.0	3.15	V
Output current			100		mA
PSRR	Freq = 217 Hz Iout = 0.01Imax/0.5Imax		40		dB
Turn-on rise time	No load			360	us
DLDO - SIM2					
Output voltage	VSIM2_SEL = 000	1.2	1.3	1.4	V
	VSIM2_SEL = 001	1.4	1.5	1.6	V
	VSIM2_SEL = 010	1.7	1.8	1.9	V
	VSIM2_SEL = 011	2.35	2.5	2.65	V
	VSIM2_SEL = 100	2.65	2.8	2.95	V
	VSIM2_SEL = 101	2.85	3.0	3.15	V
	VSIM2_SEL = 110	3.1	3.3	3.5	V
Output current			100		mA
PSRR	Freq = 217 Hz Iout = 0.01Imax/0.5Imax		40		dB
Turn-on rise time	No load			360	us
DLDO - VCAMD					
Output voltage	VCAMD_SEL = 000	1.2	1.3	1.4	V
	VCAMD_SEL = 001	1.4	1.5	1.6	V
	VCAMD_SEL = 010	1.7	1.8	1.9	V
	VCAMD_SEL = 011	2.35	2.5	2.65	V
	VCAMD_SEL = 100	2.65	2.8	2.95	V
	VCAMD_SEL = 101	2.85	3.0	3.15	V
	VCAMD_SEL = 110	3.1	3.3	3.5	V
	VCAMD_SEL = 1111	1.1	1.2	1.3	
Output current			300		mA
PSRR	Freq = 217 Hz Iout = 0.01Imax/0.5Imax		40		dB
Turn-on rise time	No load			360	us
DLDO - VCAM_IO					
Output voltage	VCAM_IO_SEL = 000	1.2	1.3	1.4	V
	VCAM_IO_SEL = 001	1.4	1.5	1.6	V
	VCAM_IO_SEL = 010	1.7	1.8	1.9	V
	VCAM_IO_SEL = 011	2.35	2.5	2.65	V
	VCAM_IO_SEL = 100	2.65	2.8	2.95	V
	VCAM_IO_SEL = 101	2.85	3.0	3.15	V

Parameter	Conditions	Min.	Typical	Max.	Unit
	VCAM_IO_SEL = 110	3.1	3.3	3.5	V
Output current			100		mA
PSRR	Freq = 217 Hz Iout = 0.01Imax/0.5Imax		40		dB
Turn-on rise time	No load			360	us
DLDO - VCAM_AF					
Output voltage	VCAM_AF_SEL = 000	1.2	1.3	1.4	V
	VCAM_AF_SEL = 001	1.4	1.5	1.6	V
	VCAM_AF_SEL = 010	1.7	1.8	1.9	V
	VCAM_AF_SEL = 011	2.35	2.5	2.65	V
	VCAM_AF_SEL = 100	2.65	2.8	2.95	V
	VCAM_AF_SEL = 101	2.85	3.0	3.15	V
	VCAM_AF_SEL = 110	3.1	3.3	3.5	V
Output current			200		mA
PSRR	Freq = 217 Hz Iout = 0.01Imax/0.5Imax		40		dB
Turn-on rise time	No load			360	us
DLDO - VMC					
Output voltage	VMC_SEL = 000	1.2	1.3	1.4	V
	VMC_SEL = 001	1.4	1.5	1.6	V
	VMC_SEL = 010	1.7	1.8	1.9	V
	VMC_SEL = 011	2.35	2.5	2.65	V
	VMC_SEL = 100	2.65	2.8	2.95	V
	VMC_SEL = 101	2.85	3.0	3.15	V
	VMC_SEL = 110	3.1	3.3	3.5	V
Output current			200		mA
PSRR	Freq = 217 Hz Iout = 0.01Imax/0.5Imax		40		dB
Turn-on rise time	No load			40	us
DLDO - VMCH					
Output voltage	VMCH_SEL = 000	1.2	1.3	1.4	V
	VMCH_SEL = 001	1.4	1.5	1.6	V
	VMCH_SEL = 010	1.7	1.8	1.9	V
	VMCH_SEL = 011	2.35	2.5	2.65	V
	VMCH_SEL = 100	2.65	2.8	2.95	V
	VMCH_SEL = 101	2.85	3.0	3.15	V
	VMCH_SEL = 110	3.1	3.3	3.5	V
Output current			400		mA
PSRR	Freq = 217 Hz Iout = 0.01Imax/0.5Imax		40		dB
Turn-on rise time	No load			40	us
DLDO - VGP1					

Parameter	Conditions	Min.	Typical	Max.	Unit
Output voltage	VGP1_SEL = 000	1.2	1.3	1.4	V
	VGP1_SEL = 001	1.4	1.5	1.6	V
	VGP1_SEL = 010	1.7	1.8	1.9	V
	VGP1_SEL = 011	2.35	2.5	2.65	V
	VGP1_SEL = 100	2.65	2.8	2.95	V
	VGP1_SEL = 101	2.85	3.0	3.15	V
	VGP1_SEL = 110	3.1	3.3	3.5	V
Output current			200		mA
PSRR	Freq = 217 Hz Iout = 0.01Imax/0.5Imax		40		dB
Turn-on rise time	No load			360	us
DLDO - VGP2					
Output voltage	VGP2_SEL = 000	1.2	1.3	1.4	V
	VGP2_SEL = 001	1.4	1.5	1.6	V
	VGP2_SEL = 010	1.7	1.8	1.9	V
	VGP2_SEL = 011	2.35	2.5	2.65	V
	VGP2_SEL = 100	2.65	2.8	2.95	V
	VGP2_SEL = 101	2.85	3.0	3.15	V
	VGP2_SEL = 110	3.1	3.3	3.5	V
Output current			100		mA
PSRR	Freq = 217 Hz Iout = 0.01Imax/0.5Imax		40		dB
Turn-on rise time	No load			360	us
DLDO - VIBR					
Output voltage	VIBR_SEL = 000	1.2	1.3	1.4	V
	VIBR_SEL = 001	1.4	1.5	1.6	V
	VIBR_SEL = 010	1.7	1.8	1.9	V
	VIBR_SEL = 011	2.35	2.5	2.65	V
	VIBR_SEL = 100	2.65	2.8	2.95	V
	VIBR_SEL = 101	2.85	3.0	3.15	V
	VIBR_SEL = 110	3.1	3.3	3.5	V
Output current			100		mA
PSRR	Freq = 217 Hz Iout = 0.01Imax/0.5Imax		40		dB
Turn-on rise time	No load			360	us

Table 7: Class AB/D audio amplifier specifications

Class AB parameter	Conditions	Min.	Typical	Max.	Unit

Class AB parameter	Conditions	Min.	Typical	Max.	Unit
RMS power	8Ω load, VBAT = 4.2 V THD + N = 1%		850		mW
	8Ω load, VBAT = 3.7 V THD + N = 1%		700		mW
	8Ω load, VBAT = 3.4 V THD + N = 1%		600		mW
THD+N	1 kHz, Po = 0.5Wrms, 4.2V		0.05	0.2	%
PSRR	217 Hz, Vin = 200mVpk-pk Input AC to ground	75	85		dB
	1 kHz, Vin = 200mVpk-pk Input AC to ground	75	85		dB
	4 kHz, Vin = 200mVpk-pk Input AC to ground	75	85		dB
	20 kHz, Vin = 200mVpk-pk Input AC to ground		50		dB
Noise level	VBAT = 3.3V 0dB gain 8Ω, A-weighted		25	70	μV
	VBAT = 4.2V 0dB Gain 8Ω, A-weighted		25	70	uV
Gain adjustment		3		21	dB
Gain adjustment steps			3		dB
Quiescent current	No load		3	6	mA
CMRR	VBAT=3.4/3.8/4.2V f=1kHz, Vin=200mVpk-pk	49	60		Ω

Class D parameter	Conditions	Min.	Typical	Max.	Unit
RMS power	8Ω load, VBAT = 4.2 V THD + N = 1%		900		mW
	8Ω load, VBAT = 3.7 V THD + N = 1%		700		mW
	8Ω load, VBAT = 3.4V THD + N = 1%		600		mW
THD+N	1 kHz, Po = 0.5Wrms, 4.2V			0.2	%
PSRR	217 Hz, Vin = 200mVpk-pk Input AC to ground	65	75		dB
	1 kHz, Vin = 200mVpk-pk Input AC to ground	65	75		dB
	4 kHz, Vin = 200mVpk-pk Input AC to ground	65	75		dB
	20 kHz, Vin = 200mVpk-pk Input AC to ground		50		dB
Noise level	VBAT = 3.3V 0dB gain 8Ω, A-weighted		25	70	μV
	VBAT = 4.2V 0dB gain		25	70	uV

Class D parameter	Conditions	Min.	Typical	Max.	Unit
	8Ω, A-weighted				
Efficiency	VBAT = 4.2V 0.8W, 8Ω with 68uH, 1 kHz	80	90		%
Gain adjustment		Mute		21	dB
Gain adjustment steps			3		dB
Quiescent current	No load		4	6	mA
CMRR	VBAT = 3.4/3.8/4.2V f=1 kHz, Vin = 200mVpk-pk	49	60		Ω

Table 8: Charger specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
CHRIN voltage		4.3	5	7	V
Operation range VCGRIN		3.2	5	8	V
OTG detection		0.8	2.4	4	V
VCDT CHRIN detection threshold	VCDT_VTHL[3:0] = 0000 ~ 1111	4.2		10.5	V
HV adaptive current @ pre_charge	VCDT switch threshold (200mA => 70mA)		6		V
Pre-charging indicator	Vchg = 3.3/5V 4.5mA VISINK drop			1000	mV
VBAT CC		3.15	3.3	3.45	V
VBAT CV		4.15	4.2	4.25	V
VBAT OV		4.25	4.3	4.35	V
CC mode charging current	CS_VTH = 1111		$14/R_{sense}$		mA
	CS_VTH = 1110		$40/R_{sense}$		mA
	CS_VTH = 1101		$80/R_{sense}$		mA
	CS_VTH = 1100		$90/R_{sense}$		mA
	CS_VTH = 1011		$110/R_{sense}$		mA
	CS_VTH = 1010		$130/R_{sense}$		mA
	CS_VTH = 1001		$140/R_{sense}$		mA
	CS_VTH = 1000		$160/R_{sense}$		mA
	CS_VTH = 0111		$180/R_{sense}$		mA
	CS_VTH = 0110		$200/R_{sense}$		mA
	CS_VTH = 0101		$220/R_{sense}$		mA
	CS_VTH = 0100		$240/R_{sense}$		mA
	CS_VTH = 0011		$260/R_{sense}$		mA
	CS_VTH = 0010		$280/R_{sense}$		mA
	CS_VTH = 0001		$300/R_{sense}$		mA

Parameter	Conditions	Min.	Typical	Max.	Unit
	CS_VTH = 0000		320/R_{sense}		mA
UVLO	VTHH		3.2		V
	VTHL		2.9		V
DDLO	VTHH		2.7		V
	VTHL		2.5		V

Table 9: Driver specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Flash dropout voltage	VFlash @ ISINK = 450mA			0.5	V
Flash soft start time	VFlash @ ISINK = 300mA			1	ms
KPLED dropout voltage	KPLED @ ISINK = 150mA			0.5	V
KPLED soft start time	KPLED @ ISINK = 150mA			1	ms
ISINK current matching	VISINK = 0.3 ~ 2.5V 4/24mA, 5 LEDs	-5		5	%
ISINK LED sink current	ISINK_SEL = 000		4		mA
	ISINK_SEL = 001		8		
	ISINK_SEL = 010		12		
	ISINK_SEL = 011		16		
	ISINK_SEL = 100		20		
	ISINK_SEL = 101		24		
ISINK dropout voltage	4 ~ 20mA VISINK drop		150	250	mV
ISINK rise/fall time	VISINK > 0.3V			3.33	uS

Table 10: Analog switch specifications

Parameter	Conditions	Min.	Typical	Max.	Unit
Analog switch turn-on resistance	VBAT = 3.3/4.2V			3	Ω
Analog switch turn-on THD	VBAT = 3.4/4.2V 1k ~ 8 kHz, 200mVpp 10kΩ			70	dB

Parameter	Conditions	Min.	Typical	Max.	Unit
BC11 Charging Port	Standard down-string port	35	70	94	mA

Parameter	Conditions	Min.	Typical	Max.	Unit
Detection	Standard charging down-string port	35	70	94	mA
	DP, DM short	140	200	260	mA
	DP, DM floating	140	200	260	mA
BC11 Characteristics	IPU_DP, IPU_DM		9.6		uA
	IPD_DP, IPD_DM		96		uA
	VSRC on DP, DM		630		mV
	Current pulse value under 2.2V		70		mA
	Current pulse periode under 2.2V		550		ms
	OSC1M, timer		5		min
	RTC, timer		35		min
	BC1.1 flow on threshold		2.2		V

Parameter	Conditions	Min.	Typical	Max.	Unit
USBDL	Duration		8.0		s
	Current		550		mA

Parameter	Conditions	Min.	Typical	Max.	Unit
FG current characteristics	Output resolution		16		Bit
	Conversion time		1/2^15		s
	Over-sampling ratio	2^11		2^13	
	Auto-calibration time	0.25		4.96	s
ADC characteristics	Input voltage range	-50		50	mV
	Supply		2.5		V
	Current		60		uA
	Gain error	-2		2	%
	Accuracy		0.03		%
	Noise		5		uV

MT6329 is a fully integrated PMIC target for smart phone power provider. See Figure 2 the block diagram for the whole picture of MT6329 PMIC.

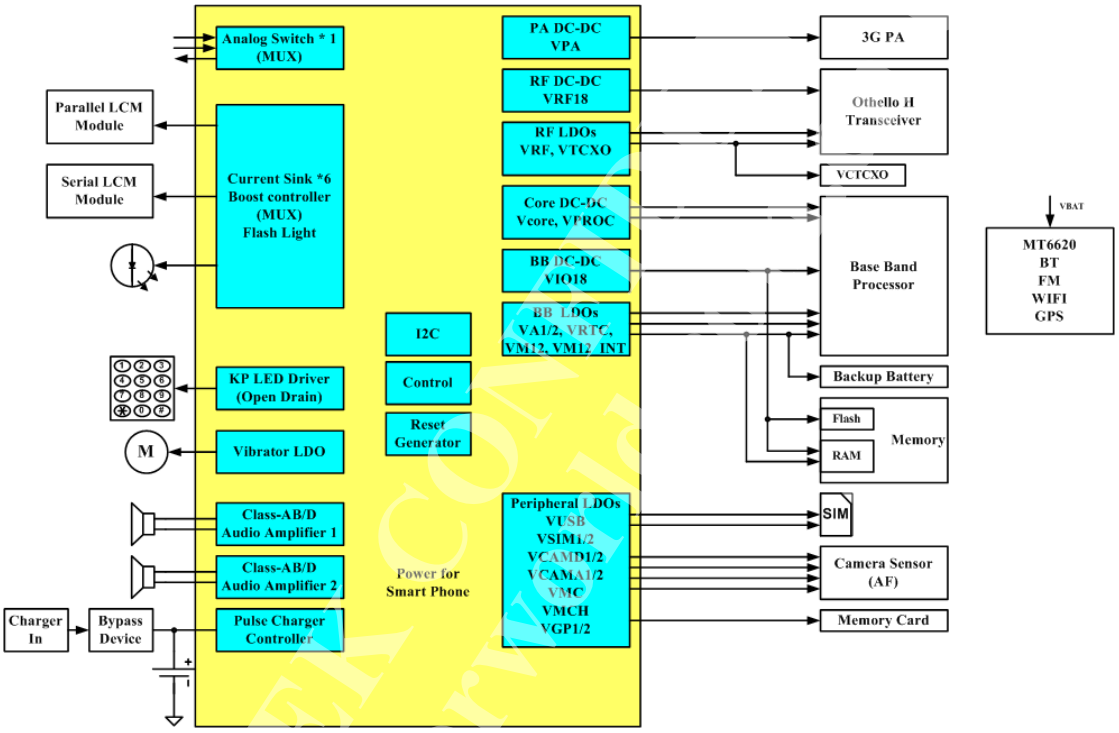


Figure 2: MT6329 block diagram

MT6329 manages the power supply of the whole chip, such as the baseband, processor, memory, SIM cards, camera, vibrator, etc. MT6329 includes the following analog functions for the use on smart phone platforms.

- LDO and BUCK: Provide regulated lower output voltage level from Li-Ion battery
- Keypad/Flash LED driver (KPLED/FLASHLED) and current sink (ISINK) driver: Sink current for keypad LED and LCM module
- Controller: Generates power-on/off sequence, system reset and exceptional handling function
- Charger controller: Controls/Protects battery charging procedure
- Class-AB/D audio amplifier: Supports high-power/quality audio amplifier
- Fuel gauge: Supports accurate battery capacity monitor

More detailed descriptions of each sub-block are explained in the following sections.

PMIC handles the powe-on and -off of the handset. If the battery voltage is neither in the UVLO state (VBAT ≥ 3.4V) nor in the thermal condition, there are three methods to power on the handset system: 1) Pulling PWRKEY low (the user pushes PWRKEY), 2) Pulling PWRBB high (baseband BB_WakeUp) and 3) Valid charger plug-in.

According to different battery voltage (VBAT) and phone state, control signals and regulators will have different responses.

Power on/off sequence

The power-on/off sequence controlled by the “control” and “reset generator” is shown in the figure below.

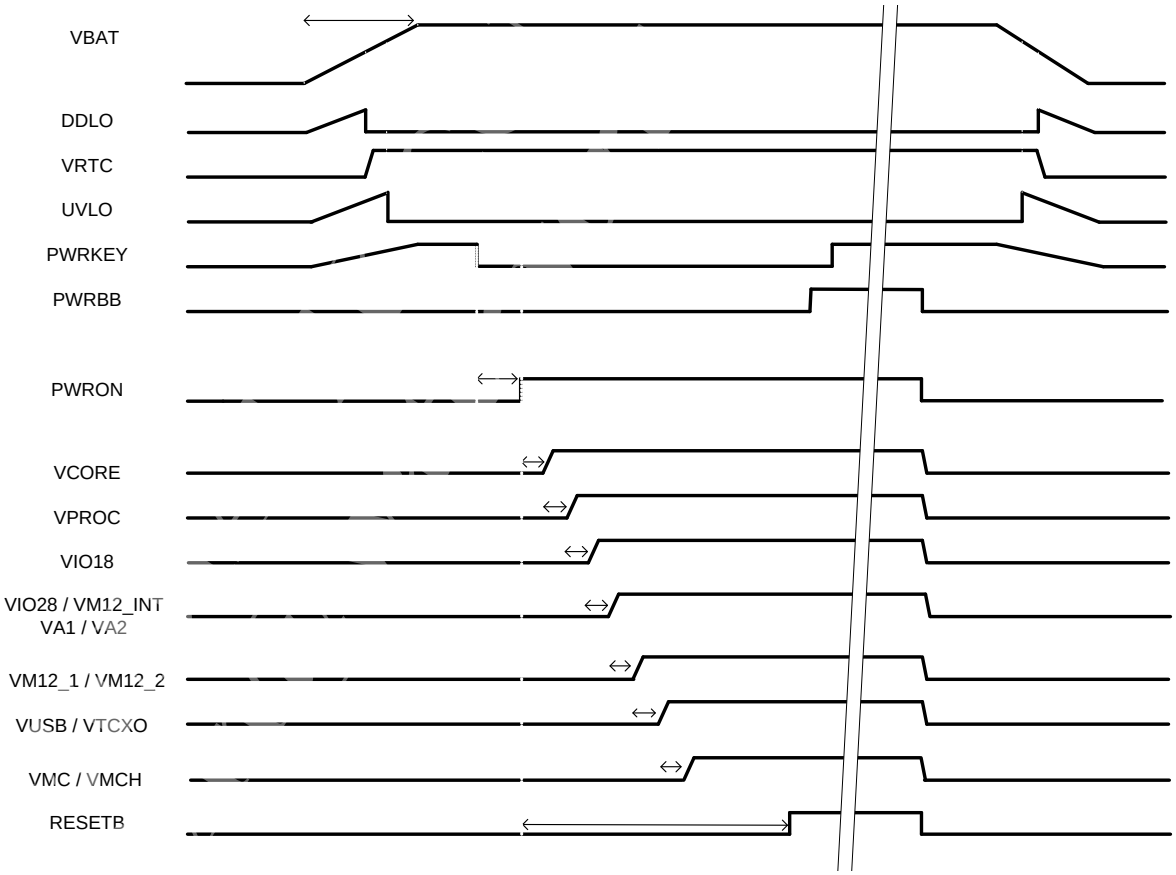


Figure 3: Power-on/off control sequence by pressing PWRKEY

Note that the figure above only shows one power-on/off. MT6329 handles the powe-on and -off of the handset. The following three different ways methods switch on the handset (when VBAT ≥ 3.4V):

1. Pushing PWRKEY (pulling the PWRKEY pin to low level)
   Pulling PWRKEY low is typical method to turn on the handset. The VCORE and VPROC buck converters will be turned on first then VIO18 and VIO28 LDOs are turned on sequentially. The supplies for the baseband are ready, and the system reset ends at the moment when all the default-on regulators are fully turned on to ensure correct timing and function. After that, the baseband sends the PWRBB signal back to PMIC for acknowledgement. To successfully power on the handset, PWRKEY should be kept low until PMIC receives PWRBB from the baseband.

2. RTC module generates PWRBB to wake up the system
   If the RTC module is scheduled to wake up the handset at some time, the PWRBB signal will be directly sent to PMIC. In this case, PWRBB becomes high at specific moment and allows PMIC power-on as the sequence described above. This is called the RTC alarm.

3. Valid charger plug-in (CHRIN voltage within valid range)
   The charger plug-in will also turn on the handset if the charger is valid (no OVP takes place). However, if the battery voltage is too low to power on the handset (UVLO state), the system will not be turned on by any of the three methods. In this case, the charger will charge the battery first, and the handset will be powered on automatically as long as the battery voltage is high enough.

Under-voltage lockout (UVLO)

The UVLO state in PMIC prevents start-up if the initial voltage of the main battery is below the 3.2V threshold. It ensures that the handset is powered on with the battery in good condition. The UVLO function is performed by a hysteretic comparator which ensures smooth power-on sequence. In addition, when the battery voltage is getting lower, it will enter the UVLO stat,e and PMIC will be turned off by itself, except for VRTC LDO, to prevent further discharging. Once PMIC enters the UVLO state, it will draw low quiescent current. RTC LDO will still be working until DDLO disables it.

Deep discharge lockout (DDLO)

PMIC will enter the deep discharge lockout (DDLO) state when the battery voltage drops below 2.5V. In this state, VRTC LDO will be shut down. Otherwise, it will draw very low quiescent current to prevent further discharging or even damage to the cells.

Reset

PMIC contains a reset control circuit which takes effect at both power-up and power-down. The RESETB pin is held low in the beginning of power-up and returns to high after the pre-determined delay time. The delay time is controlled by a large counter, which uses the clock from the internal ring-oscillator. At power-off, the RESETB pin will return to low immediately without any delay.

Over-temperature protection

If the die temperature of PMIC exceeds 150°C, PMIC will automatically disable all LDOs except for VRTC. Once the over-temperature state is resolved, a new power-on sequence will be required to enable the LDOs.

The charger controller senses the charger input voltage from either a standard AC-DC adaptor or an USB charger. When the charger input voltage is within a pre-determined range, the charging process will be activated. This detector resists higher input voltages than other parts of PMIC.

Charger block diagram

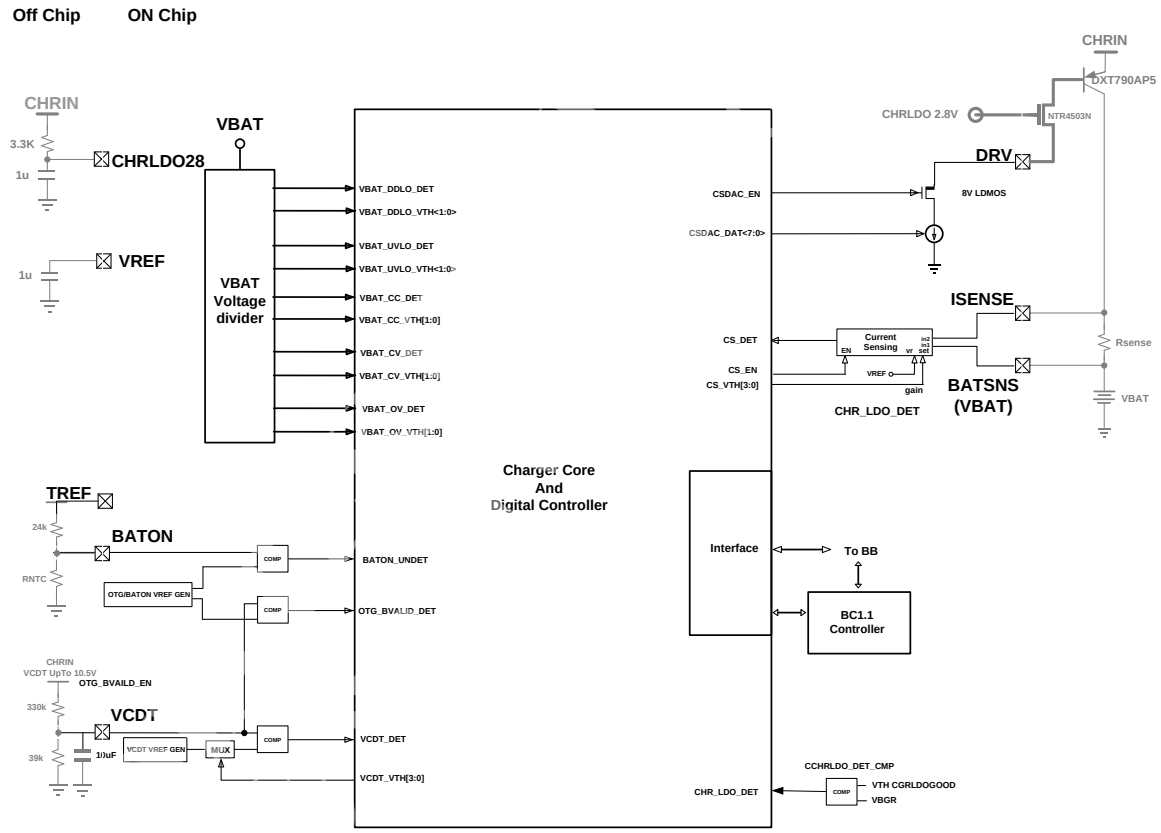


Figure 4: PCHR block diagram

Whenever an invalid charging source is detected (> 7.0V), the charger detector will stop the charging process immediately to avoid burning out the chip or even the phone. Furthermore, if the charger-in

level is not high enough (< 4.3V), the charger will also be disabled to avoid improper charging behavior.

When the charger is active, the charger controller will manage the charging phase according to the battery status. During the charging period, the battery voltage is constantly monitored. The battery charger supports pre-charge mode (VBAT < 3.2V, PMIC power-off state), CC mode (constant current mode or fast charging mode at the range of 3.2V < VBAT < 4.2V) and CV mode (constant voltage mode) to optimize the charging procedure for Li-ion battery. See the figure below for the charging states diagram.

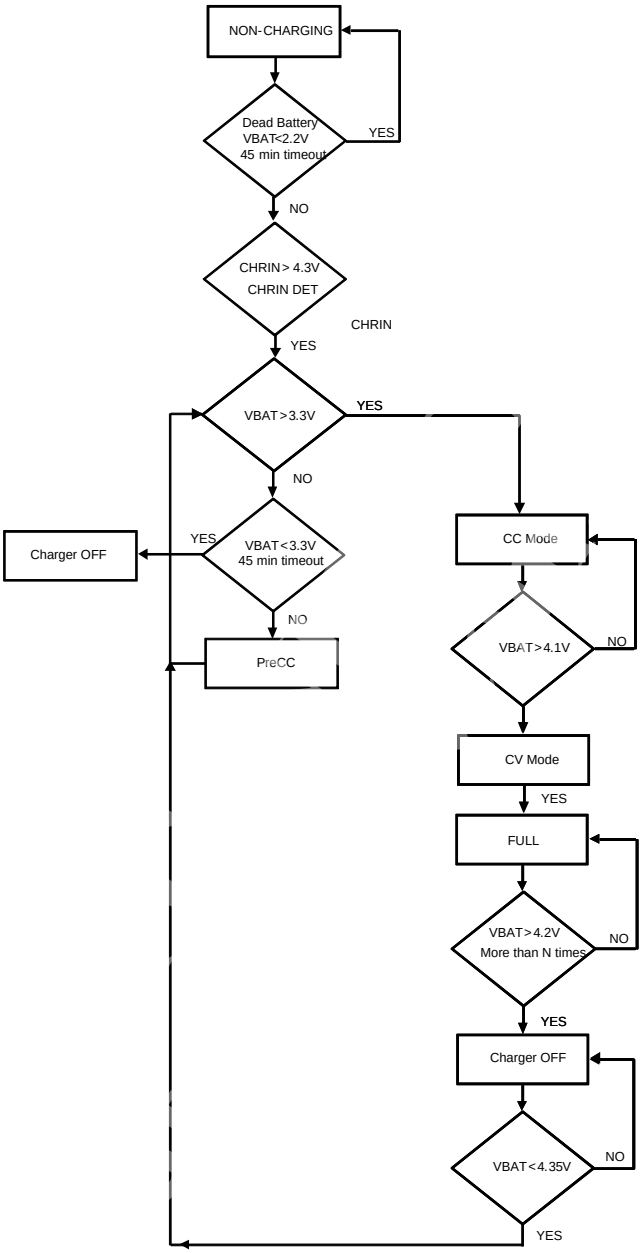


Figure 5: Charging states diagram

Pre-charge mode

When the battery voltage is in the UVLO state, the charger will operate in the pre-charge mode. There are two steps in this mode. While the battery voltage is deeply discharged below 2.2V, PRECC0 trickle charging current is applied to the battery.

The PRECC1 trickle charging current is about 56mA continuous current when VBAT is under 2.2V.

When the battery voltage exceeds 2.2V, i.e. the PRECC2 stage, the closed-loop pre-charge will be enabled. The voltage drop across the external RSENSE is kept around 40mV (AC charger) or 14mV (USB host). The closed-loop pre-charge current can be calculated:

$$I_{PRECC2,\ AC\ adapter} = \frac{V_{SENSE}}{Rsense} = \frac{40mV}{Rsense}$$

$$I_{PRECC2,\ USB\ HOST} = \frac{V_{SENSE}}{Rsense} = \frac{14mV}{Rsense}$$

Constant current mode

As the battery is charged up and over 3.3V, it can switch to the CC mode. (CHR_EN should be high) In the CC mode, several charging currents can be set by programming registers or the external RSENSE resistor. The charging current can be determined by CS_VTH/RSENSE, where CS_VTH is programmed by registers. For example, if RSENSE is selected as 0.2ohm, the CC mode charging current can be set from 70 to 800mA. It can accommodate the battery charger to various charger inputs with different current capability.

Constant-voltage mode and over-voltage protection (OV)

While the battery voltage reaches about 4.2V, a constant current with much shorter period is used for charging. It allows more often full battery detection in non-charging period. This is called the full-voltage charging mode or constant-voltage charging mode in correspondence to a linear charger. While the battery voltage actually reaches 4.2V, more than the pre-setting times within the limited charging cycles, the end-of-charging process starts. It may prolong the charging and detecting period for acquiring optimized full charging volume. The end of charging process is fully controlled by the baseband and can be easily optimized for different battery packs. Once the battery voltage exceeds 4.35V, a hardware OV protection should be activated and turn off the charger immediately.

MT6255 also support dead-battery condition from China standard (BC1.1). These specifications protect dead-battery charging by timer and trickle current. Once the battery voltage is below 2.2V, a period (TUNIT) of trickle current (IUNIT) will be applied to the battery.

If the battery voltage is still below 2.2V after applying the trickle current, the charger will be disabled. On the other hand, once if the battery voltage rises up to above 2.2V, the charger will enter the PRECC1 stage, and the charging current will be 70mA or 200mA depending on the type of the charging port.

Under the condition of battery voltage from 2.2V to 3.3V, the charger will charge the battery with the PRECC1 current.

A dedicated 5 mins. (T1) timer will be timed out and disable the charger if the battery voltage is always below 2.7V under charging. Another 35 mins. (T2) timer will also be timed out and disable the charger if the battery voltage is always kept between 2.7V and 3.3V under charging.

The trickle current (IUNIT) and two dedicated timers protect the charging action if the battery is dead.

There are 5 buck converters in MT6329 to efficiently generate regulated power for processor, digital core, 3G power amplifier, memory IO and RF circuit. The block diagram is shown in Figure 10. The buck converters operate with typically 2 MHz fixed frequency pulse width modulation (PWM) mode at moderate to heavy load currents. At light load currents, the converter automatically enters pulse frequency modulation (PFM) mode to save power and improve light load efficiency. It also has a force-PWM mode option to allow the converter to remain in the PWM mode regardless of the load current, so that the noise spectrum of the converter can be minimized for certain highly-noise-sensitive handset applications. The buck converters also have an internal over-current protection (OCP) circuit to limit the maximum high-side power FET current in over-load conditions. It has an internal soft start circuit to control the ramp-up rate of the output voltage during start-up.

Table 10: Buck converter brief specifications

BUCK name	Vout (Volt)	Imax (mA)	Application
VCORE	0.75 ~ 1.3 (25mV/step)	1,000	Digital CORE
VPROC/Vcore2	0.75 ~ 1.3 (25mV/step)	1,500	Processor
VIO18	1.8	1,000	IO
VRF_1V8	1.825	250	RF chip
V3GPA	0.9 ~ 3.4 (0.1V/step)	800	3G power amplifier

1. Processor power, VPROC
   VPROC is a high-current buck converter to provide a highly-efficient power supply for the handset processor. Powering from a Li-ion battery, VPROC steps down the input voltage from 3.4 ~ 4.3V to the typical output voltage of 1.2V with a maximum load current capability of 1.2A. The output voltage can be adjusted between 0.7V and 1.3V. In order to optimize the overall system efficiency for the processor, VPROC features a Dynamic Voltage Frequency Scaling (DVFS) function which allows it to dynamically adjust its output voltage between 0.9V and 1.2V under different voltage supply demands from the processor. For more details, refer to the “Dynamic Voltage Frequency Scaling (DVFS)” section.

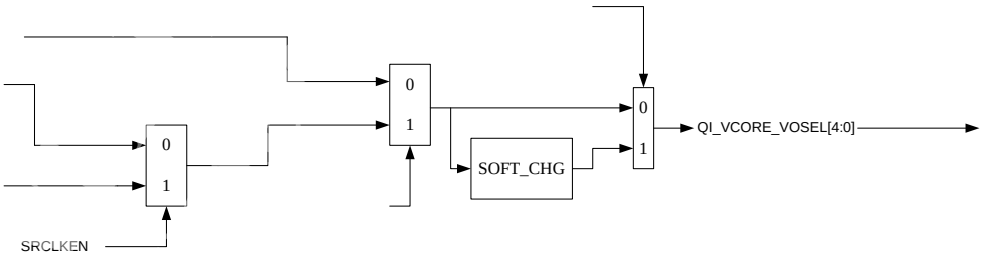
2. Digital CORE power, VCORE
   VCORE is a high-current buck converter to provide a highly-efficient power supply for the handset digital core. Powering from a Li-ion battery, VCORE steps down the input voltage from 3.4 ~ 4.3V to the typical output voltage of 1.1V with a maximum load current capability of 1.0A. The output voltage can be adjusted between 0.7V and 1.3V. In order to optimize the overall system efficiency for digital core, VCORE features a Dynamic Voltage Frequency Scaling (DVFS) function which allows it to dynamically adjust its output voltage between 0.9V and 1.1V under different voltage supply demands from the digital core circuit. For more details, refer to the “Dynamic Voltage Frequency Scaling (DVFS)” section.

3. IO & memory power, VIO18
   VIO18 is a high-current buck converter to provide a highly-efficient power supply for the handset I/O power. Powering from a Li-ion battery, VIO18 steps down the input voltage from 3.4 ~ 4.3V to the typical output voltage of 1.8V with a maximum load current capability of 1.0A.

4. 3G PA power, VPA

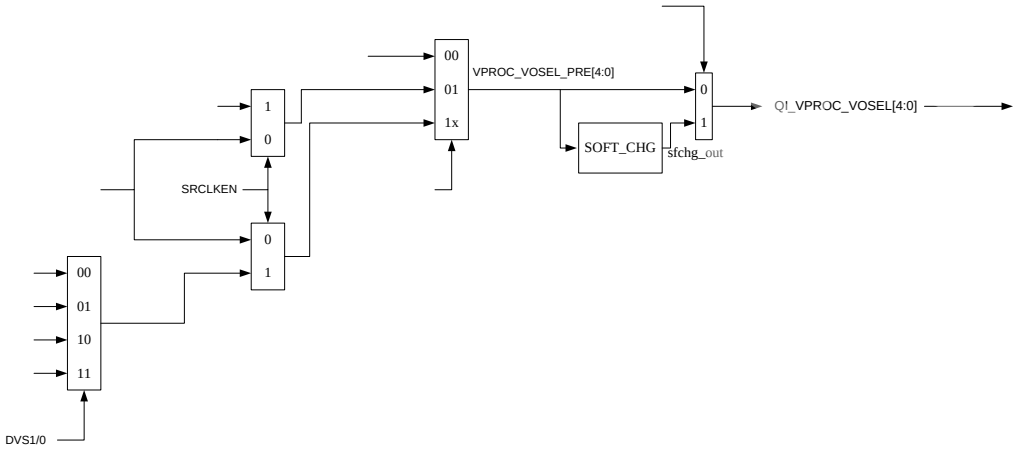
5. RF power, VRF18
   VRF18 is a buck converter to provide a highly-efficient power supply for the handset RF power. Powering from a Li-ion battery, VRF18 steps down the input voltage from 3.4 ~ 4.3V to the typical output voltage of 1.825V with a maximum load current capability of 0.25A.

VCORE1, VPROC and VM12_INT have DVFS control respectively. There are two DVS modes: 1) One-shot mode: If DVFS is issued, the voltage will directly jump to the target one. 2) Soft-change mode: If DVFS is issued, the voltage will be switched step by step. See the figure below for the VCORE DVFS voltage control logic:



There are two control modes:
1. Direct control by register (when @RG_VCORE_CTRL = 0)
2. Auto switch between normal operation mode and sleep mode voltage (when @RG_VCORE_CTRL = 1)

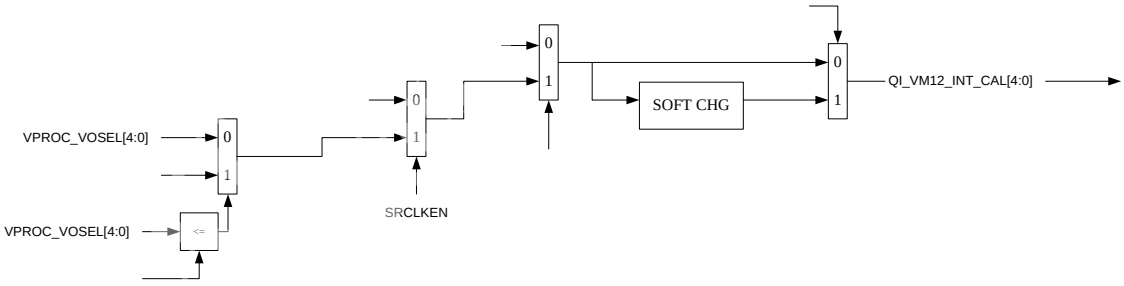
See the figure below for the VPROC DVFS voltage control logic:



There are three control modes:

1. Direct control by register (when @RG_VPROC_CTRL[1:0] = 00)
2. Auto switch between normal operation mode and sleep mode voltage (when @RG_VPROC_CTRL[1:0] = 01)
3. Voltage control by dedicated pins DVS1 and DVS0. There are 4 dedicated registers for 4 DVS1,0 combinations. This mode enables fast voltage change to achieve better power and performance. In addition, auto switch between normal operation and sleep mode voltage is still supported in the mode. (when @RG_VPROC_CTRL[1:0] = 1x)

See the figure below for the VM12_INT DVFS voltage control logic:



There are two control modes:

1. Direct control by register (when @RG_VM12_INT_CTRL_SEL = 0)
2. Auto switch between normal operation mode and sleep mode voltage (when @ RG_VM12_INT_CTRL_SEL = 1). Note that due to VM12_INT is for CPU internal SRAM power which needs to track the VPROC voltage, the hardware auto tracking logic is implemented in this mode. However, it has lower bound during operation to achieve normally access, there is hardware auto low-voltage limit for this control logic.

MT6329 integrates 21 LDOs optimized for their given functions by balancing quiescent current, dropout voltage, line/load regulation, ripple rejection and output noise.

A low-dropout regulator (LDO) is capable of maintaining its specified output voltage over a wide range of load current and input voltage, down to a very small difference between input and output voltages.

There are several features in the design of LDO, including discharge control, soft start and current limit. Before LDO is enabled, the output pin of LDO should be discharged first to avoid voltage accumulation on the capacitance. Soft-start limits inrush current and controls output-voltage rise time during power-up. Current limit is the current protection to limit LDO's output current and power dissipation.

There are three types of LDOs in the MT6329 PMIC. The analog LDO is optimized for low-frequency ripple rejection in order to reject the ripple coming from the burst of RF power amplifier. The digital IO LDO is a linear regulator optimized for very low quiescent current. The single-step RTC LDO is a linear regulator that can charge up a capacitor-type backup coin cell, which also supplies the RTC module even at the absence of the main battery. The single-step LDO features the reverse current protection and is optimized for ultra-low quiescent current while sustaining the RTC function as long as possible.

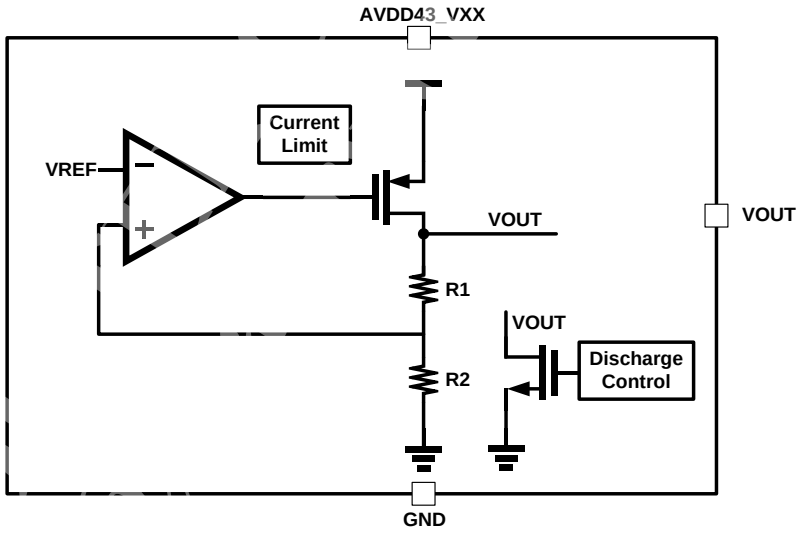


Figure 6: LDO block diagram

Table 11: LDO types and brief specifications

Type	LDO name	Vout (Volt)	Imax (mA)	Application
ALDO	VRF/VRF28	2.85	200	RF chip
ALDO	VTCXO	2.8	40	13/26 MHz reference clock

Type	LDO name	Vout (Volt)	Imax (mA)	Application
ALDO	VA1	1.8/2.0/2.1/2.5	100	Analog baseband
ALDO	VA2	2.5/2.8	100	Analog baseband
ALDO	VCAMA	1.5/1.8/2.5/2.8	200	Analog power for camera module
DLDO	VM12_1	1.2	300	DRAM
DLDO	VM12_2	1.2/1.1/1.0/0.9	300	DRAM or AST3001
DLDO	VM12_INT	1.2	360	SRAM
DLDO	VIO28	2.8	100	Digital IO
DLDO	VSIM1	1.8/3.0	100	1st SIM card
DLDO	VSIM2	1.3/1.5/1.8/2.5 2.8/3.0/3.3	100	2nd SIM card
DLDO	VUSB	3.3	100	USB
DLDO	VCAMD	1.3/1.5/1.8/2.5 2.8/3.0/3.3	300	Digital power for camera module
DLDO	VCAM_IO	1.3/1.5/1.8/2.5 2.8/3.0/3.3	100	IO power for camera module
DLDO	VCAM_AF	1.3/1.5/1.8/2.5 2.8/3.0/3.3	200	Auto-focus power for camera module
DLDO	VMC	1.3/1.5/1.8/2.5 2.8/3.0/3.3	200	Memory card
DLDO	VMCH	1.3/1.5/1.8/2.5 2.8/3.0/3.3	400	SD3.0 memory card
DLDO	VGP1	1.3/1.5/1.8/2.5 2.8/3.0/3.3	100	1st general-purpose LDO
DLDO	VGP2	1.3/1.5/1.8/2.5 2.8/3.0/3.3	100	2nd general-purpose LDO
DLDO	VIBR	1.3/1.5/1.8/2.5 2.8/3.0/3.3	200	Vibrator
RTCLDO	VRTC	1.8/2.0/2.1/2.8	2	Real-time clock

1. Digital IO LDO (VIO28)
   The digital IO LDO is a regulator that sources 100 mA (max.) with fixed 2.8V output voltage. The LDO supplies the BB circuitry in the handset and is optimized for a very low quiescent current. The VIO28 LDO is powered on as soon as the system enters the switched-on/stand-by mode. Besides, the output voltage/current will fold-back as over-current/hard-short occurs.

2. Digital camera LDO (VCAMD)
   The digital camera LDO is a regulator that sources 300 mA (max.) with programmable output voltage. The LDO supplies the camera circuitry in the handset and is optimized for a low-quiescent current. VCAMD LDO can be enabled through the I2C interface. Besides, the folded-back OC protection is also available.

3. Digital camera auto focus LDO (VCAM_AF)
   The digital camera auto focus LDO is a regulator that sources 200 mA (max.) with programmable output voltage. The LDO supplies the camera auto focus circuitry in the handset and is optimized

for a low-quiescent current. VCAM_AF LDO can be enabled through the I2C interface. Besides, the folded-back OC protection is also available.

4. Digital camera IO power LDO (VCAM_IO)
   The digital camera IO power LDO is a regulator that sources 100 mA (max.) with programmable output voltage. The LDO supplies the camera IO circuitry in the handset and is optimized for a low-quiescent current. VCAM_IO LDO can be enabled through the I2C interface. Besides, the folded-back OC protection is also available.

5. Vibrator power LDO (VIBR)
   The vibrator power LDO is a regulator that sources 200 mA (max.) with programmable output voltage. The LDO supplies the vibrator circuitry in the handset and is optimized for a low-quiescent current. VIBR LDO can be enabled through the I2C interface. Besides, the folded-back OC protection is also available.

6. Memory card power LDO (VMC)
   The memory card power LDO is a regulator that sources 200 mA (max.) with programmable output voltage. The LDO supplies the memory card circuitry in the handset and is optimized for a low-quiescent current. VMC LDO can be enabled through the I2C interface. Besides, the folded-back OC protection is also available.

7. SD3.0 memory card power LDO (VMCH)
   The SD3.0 memory card power LDO is a regulator that sources 400 mA (max.) with programmable output voltage. The LDO supplies the SD3.0 memory card circuitry in the handset and is optimized for a low-quiescent current. VMCH LDO can be enabled through the I2C interface. Besides, the folded-back OC protection is also available.

8. SIM LDO (VSIM1)
   The SIM LDO is a regulator that sources 100 mA (max.) with 1.8 V or 3.0 V output voltages based on the supply specs of subscriber identity module (SIM) card. The VSIM1 LDO supplies the SIMs in the handset and is controlled independently of the other LDOs. Besides, the folded-back OC protection is also available.

9. 2nd SIM LDO (VSIM2)
   The SIM LDO is a regulator that sources 100 mA (max.) with programmable output voltages based on the supply specs of subscriber identity module (SIM) card. The VSIM2 LDO supplies the second SIM card in the handset and is controlled independently of the other LDOs. Besides, the folded-back OC protection is also available.

10. Memory 1.2V LDO (VM12_1)
    The memory 1.2V LDO is a regulator that sources 300 mA (max.) with fixed 1.2V output voltage. The LDO supplies 1.2V to memory circuitry in the handset and is optimized for a low-quiescent current. The VM12_1 LDO can be enabled through the I2C interface. Besides, the folded-back OC protection is also available.

11. Reserve 1.2V power LDO (VM12_2)
    The reserved 1.2V power LDO is a regulator that sources 300 mA (max.) with programmable output voltage. The LDO supplies the reserved 1.2V power for AST3001 core circuitry in the handset and is optimized for a low-quiescent current. VM12_2 LDO can be enabled through the I2C interface. Besides, the folded-back OC protection is also available.

12. SRAM 1.2V power LDO (VM12_INT)
    The SRAM 1.2V power LDO is a regulator that sources 360 mA (max.) with programmable output voltage. The LDO supplies the SRAM circuitry in the handset and is optimized for a low-quiescent current. VM12_INT LDO can be enabled through the I2C interface. Besides, the folded-back OC protection is also available.

13. Analog camera LDO (VCAMA)
    The analog camera LDO is a regulator that sources 200 mA (max.) with programmable 1.5/1.8/2.5/2.8V output voltage. The LDO supplies the camera circuitry in the handset and is optimized for a very low frequency ripple rejection in order to reject the ripple coming from the burst of RF power amplifier at 217 Hz. VCAMA LDO can be enabled through the I2C interface. Besides, the folded-back OC protection is also available.

14. Analog LDO (VA1)
    The analog LDO is a regulator that sources 200 mA (max.) with fixed 2.5V output voltage. The LDO supplies the analog sections of the BB chipsets and is optimized for low-frequency ripple rejection in order to reject the ripple coming from the burst of RF power amplifier at 217 Hz. VA LDO is powered on as soon as the system enters the switched-on/stand-by mode. Besides, the output voltage/current will fold-back as over-current/hard-short occurs.

15. Analog LDO (VA2)
    The analog LDO2 is a regulator that sources 100 mA (max.) with fixed 2.5V output voltage. The LDO supplies the analog sections of the BB chipsets and is optimized for low-frequency ripple rejection in order to reject the ripple coming from the burst of RF power amplifier at 217 Hz. VA2 LDO is powered on as soon as the system enters the switched-on/stand-by mode. Besides, the output voltage/current will fold-back as over-current/hard-short occurs.

16. TCXO LDO (VTCXO)
    TCXO LDO is a regulator that sources 40 mA (max.) with a 2.8V output voltage. The LDO supplies the temperature compensated crystal oscillator, which needs its own ultra-low noise supply and very good ripple rejection ratio.

17. RF LDO (VRF)
    The analog LDO is a regulator that sources 200 mA (max.) with fixed 2.85V output voltage. The LDO supplies the RF circuitry in the handset and is optimized for low-frequency ripple rejection in order to reject the ripple coming from the burst of RF power amplifier at 217 Hz.

18. General-purpose LDO (VGP1)
    The general-purpose LDO is a regulator that sources 100 mA (max.) with programmable output voltage. The LDO supplies the camera circuitry in the handset and is optimized for a very low quiescent current. VGP LDO can be enabled through the I2C interface. Besides, the folded-back OC protection is also available.

19. General-purpose LDO2 (VGP2)
    The general-purpose LDO2 is a regulator that sources 100 mA (max.) with programmable output voltage. The LDO supplies the camera circuitry in the handset and is optimized for a very low quiescent current. VGP2 LDO can be enabled through the I2C interface. Besides, the folded-back OC protection is also available.

20. USB LDO (VUSB)
    The digital IO LDO is a regulator that sources 100 mA (max.) with fixed 3.3V output voltage. The LDO supplies the BB circuitry in the handset and is optimized for a very low quiescent current. VIO LDO is powered on as soon as the system enters the switched-on/stand-by mode. Besides, the output voltage/current will fold-back as over-current/hard-short occurs.

21. RTC LDO (VRTC)
    PMIC features a 2-step RTC that keeps RTC alive for a long time after the battery has been removed. The first LDO charges a backup battery on the BAT_BACKUP pin to ~ 2.8V. In addition, when the battery is removed, the first stage prevents the backup battery from leaking back to VBAT. The second LDO regulates the 2.8V supply to a 1.5V/1.2V optional RTC voltage. The RTC voltage can be set by the VCORE_SEL pin while BB is alive. The setting is retained while BB is powered down. When the backup battery is fully charged, the high backup battery voltage, low reverse current leakage and the low second LDO operating current sustain the RTC block for even tens of hours with the absence of the main battery.

22. Reference voltage output (VREF)
    The reference voltage output is a low-noise, high-PSRR and high-precision reference with a guaranteed accuracy of 1.5% over temperature. The output is used as the system's reference for MT6329 internally. For accurate regulator and charger output voltage, DO NOT load the reference voltage. Bypass it to GND with a minimum 100nF external capacitor.

MT6329 supports backlight LED drivers both in parallel and in series configurations by pin sharing ISINK and boost controller circuits. Besides, it provides the drivers for keypad LED and Flash light LED. The following two figures depict two major applications for backlight LEDs and other drivers.

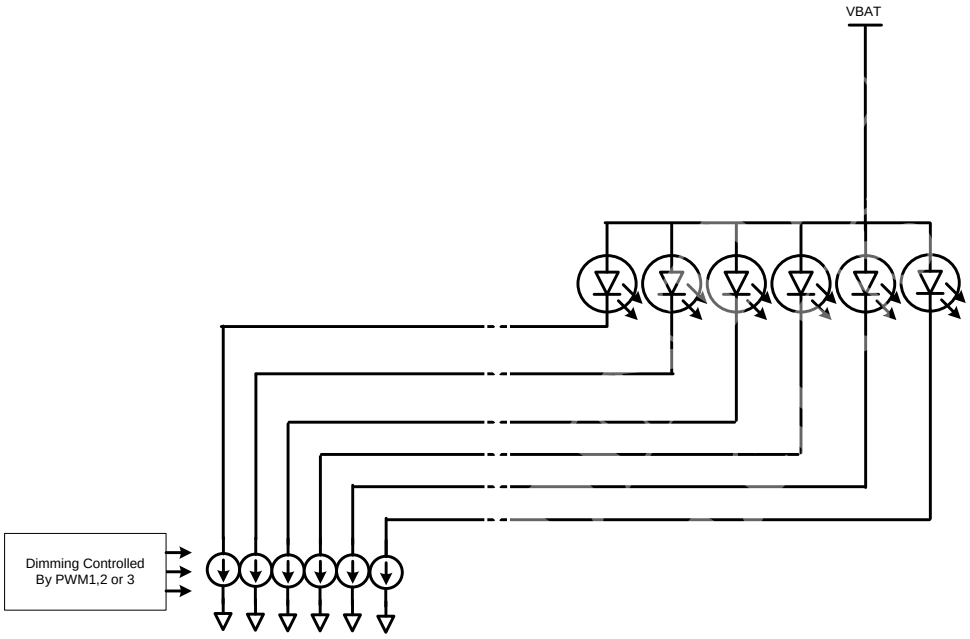


Figure 7: Configuration for parallel BL LED drivers

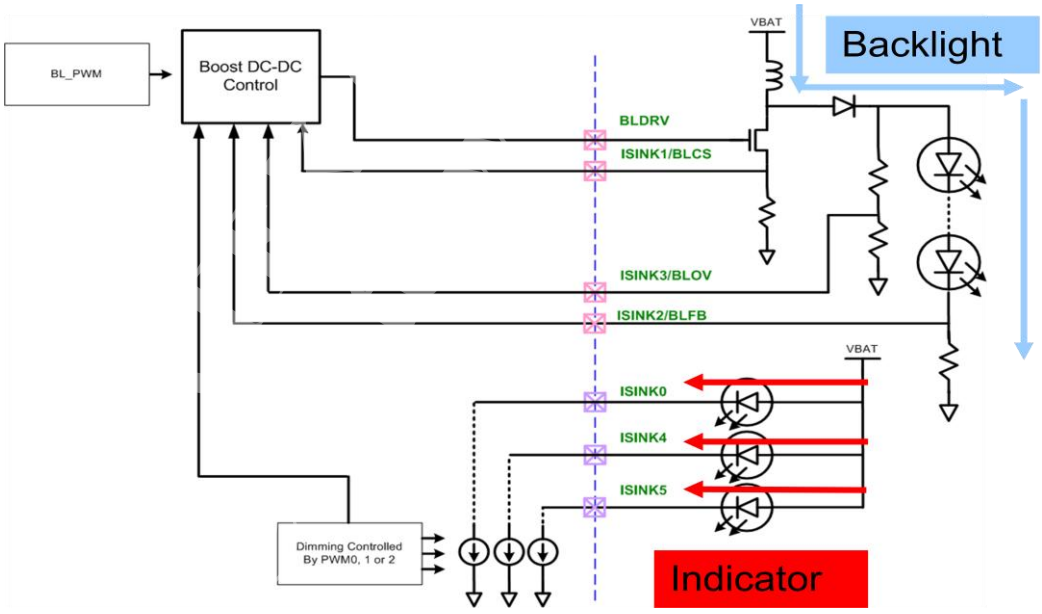


Figure 8: Configuration for serial BL LED drivers

For parallel configuration, MT6329 supports up to 6 LEDs in parallel with 6-step programmable current in each channel. The B.L. LEDs are supplied by the battery voltage. The LED current are

controlled by the current sinks in MT6329. The brightness of the B.L. LEDs can be controlled by tuning the current for current sinks or switching on/off the current sinks through dimming control. The dimming frequency and duty can be programmed by registers through the I2C interface. For more details, refer to the “Dimming Control” section.

For series configuration, MT6329 internal boost controller supports 20mA for up to 10 LEDs in series. External ballast resistor is necessary and serially connected between the LED string and ground. The voltage across the external ballast resistor is used to feedback the BL LED current information to the boost controller of MT6329. The BL LED current is regulated by the negative feedback loop formed in the boost controller. In addition, the brightness of the B.L. LEDs can be controlled by changing the external ballast resistors, tuning the feedback voltage (analog dimming) or switching on/off the boost controller through dimming control (digital dimming). The analog/digital dimming selection, dimming frequency and duty can be programmed by registers through the I2C interface. For more details on digital dimming, refer to the “Dimming Control” section.

The flash light LED driver is a low Ron switch which allows up to 500mA current. The brightness of the flash light LED can be controlled by changing the external series ballast resistor.

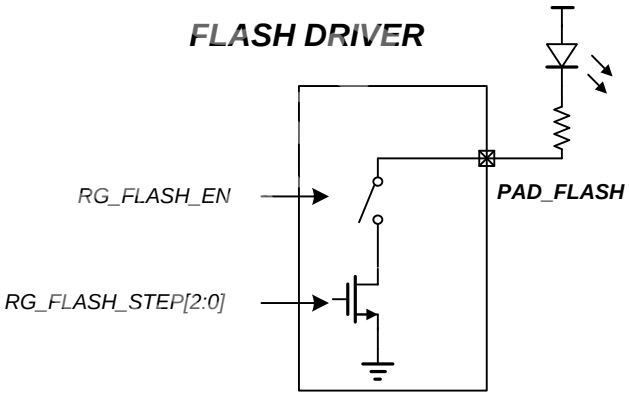


Figure 9: Configuration for flash light LED driver

The keypad LED driver is a low Ron switch which allows up to 150mA current. The brightness of the keypad LED can be controlled by changing the external series ballast resistor.

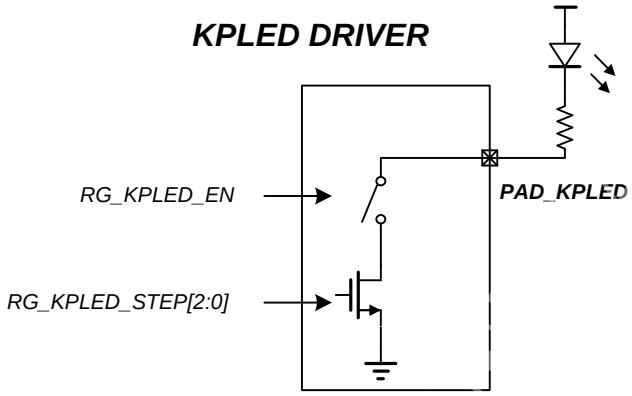


Figure 10: Configuration for KP LED driver

The intensity of the backlight WLED, flash light LED, keypad LED and vibrator can be adjusted by dimming control. Although they can be controlled separately, the concepts are the same. It can be controlled by programming some internal registers to change the on/offF pulse duty cycle and frequency.

For all drivers, the output duty cycle is adjusted by selecting the corresponding driver's PWM_DUTY value according to the following relationship:

(VIBR/KP/FLASH/BL) PWM duty cycle = (PWM_DUTY + 1) high's , and 32 - (PWM_DUTY +1) low's

, where PWM_DUTY ranges from 0 to 31.

For all drivers, the output frequency is changed by adjusting the corresponding driver's PWM_DIV value according to the following relationship:

(VIBR/KP/FLASH/BL) PWM frequency = 1.4M/25/(PWM_DIV + 1)/32

, where PWM_DIV ranges from 0 to15.

For FLASH/BL, the output frequency is changed by adjusting PWM_DIV and BYPASS. The output frequency is governed by:

When bypass = 0,

(FLASH/BL) PWM frequency = 1.4M/25/(PWM_DIV + 1)/32

When bypass = 1,

(FLASH/BL) PWM frequency = 1.4M/(PWM_DIV + 1)/32

, where PWM_DIV ranges from 0 to 15.

The features of each driver are listed in the table below. All drivers can be enabled, and their duty and frequency can be adjusted. For FLASH and BL, the fixed divisor, 25, can be bypassed.

VIBR	○	○	○	
KP	○	○	○	
FLASH	○	○	○	○
BL	○	○	○	○

MT6239 has a built-in 2-to-1 analog switch with less than 3 ohm turn-on resistance supporting both microphone input and video line-out operation. THD is up to 70dB for microphone and good PSRR which is around 75dB across the voice band. The low turn-on resistance ensures linearity of the video playback.

MT6329 has built-in dual channel high efficiency class AB/D audio power amplifier capable of delivering 1 watt of power to an 8 ohm (each channel, stereo) BTL load and up to 2 watts onto parallel equivalent 4-ohm load (mono in two channels) from a 4.2V battery supply. The THD performance is 74/76dB for class-D/AB mode respectively. The input must be AC-coupled. Over-current protection is integrated. MT6329 also has built-in receiver bypass function for 2-in-1 loudspeaker. This built–in receiver bypass supports multi-purpose loudspeaker without any extra BOM cost. The output power can reach 97mW onto 8 ohm speaker load. The block diagram is shown in **Error! Reference source not found.**.

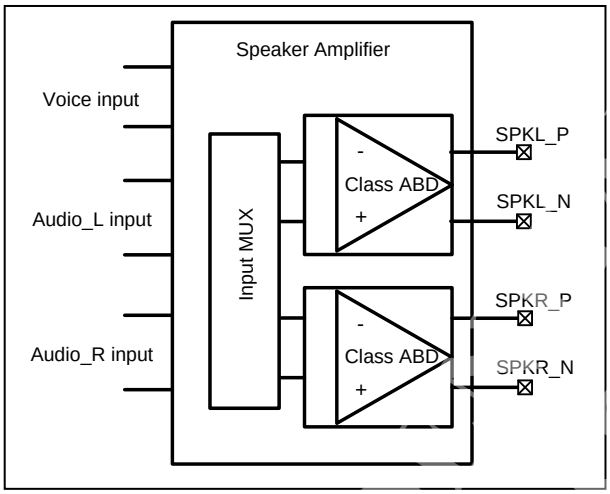


Figure 11: Block diagram of class-AB/D

The fuel gauging system includes a dedicated ADC for Li-Ion battery current measurement and utilizes the measurement ADC (AUXADC) for battery voltage and temperature measurement. The battery state-of-charge (SOC) estimation is performed by the software using the three measuring methods and the accumulated current measurement. The application diagram of the fuel gauging system is shown in the figure below, where an external resistor is used to converter the current drawn from the battery into a voltage which is then measured by FG ADC. The value of the external resistor must be chosen so that the maximum current during charging or discharging will not cause ADC to exceed its input voltage range.

The principle of operation of the fuel gauge relies on a combination of Coulomb counting and light load battery voltage measurement. Coulomb counting provides an estimate of the charge that has been withdrawn or delivered to the battery, while battery voltage measurement proves a good estimate of the battery SOC under low-load conditions. The battery voltage measurement compensates for error accumulation during the current integration inherent in Coulomb counting. The hardware also includes necessary modes to allow for simultaneous current and voltage measurement which can be utilized to estimate the battery impedance.

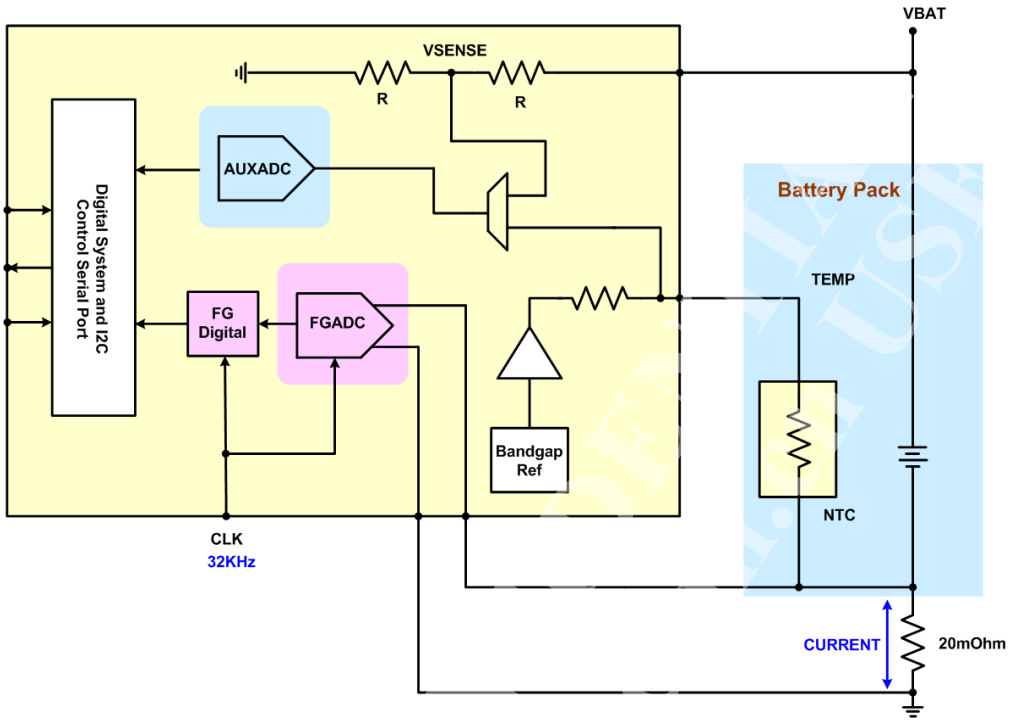
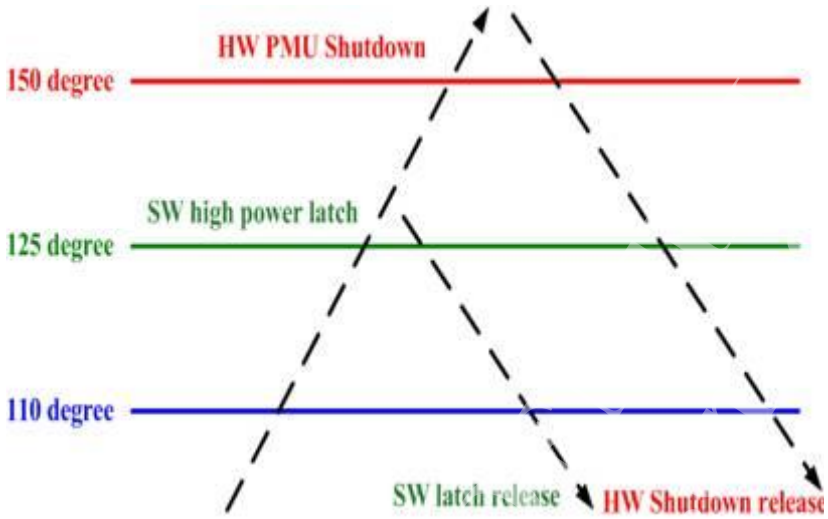


Figure 12: Fuel gauge block diagram and external connection

There are 7 groups of interrupts for MT6329 to inform BB IC:

1. Key pressed and released interrupt
   - PWRKEY: Interrupt is issued when PWRKEY is pressed (and released, set by the register). After receiving the interrupt, the software will read the PWRKEY_DEB status to see if it is pressed or released.
   - HOMEKEY: Interrupt is issued when HOMEKEY is pressed (and released, set by the register). After receiving the interrupt, the software will read the HOMEKEY_DEB status to see if it is pressed or released.

2. Thermal interrupt
   MT6329 issues THR_H interrupt for the software high power latch if PMIC die temperature is over 125c and issues THR_L for software latch release if PMIC die temperature goes from 125c back to under 110c.



3. Charger related interrupt
   There are several interrupts supported for charger control:
   CHRDET
   OV
   WATCHDOG
   OTG_BVALID
   VBATON_UNDET

4. Battery voltage/current H/L interrupt
   There are two groups of VBAT detection interrupt.
   1) VBAT detected by AUXADC
      If VBAT is higher than the threshold specified by an register setting, the HIGHBATTERY interrupt will be issued. If VBAT is lower than the threshold specified by another register setting, the LOWBATTERY interrupt will be issued.

   2) VBAT detected by fuel gauge
      If VBAT is higher than the threshold specified by an register setting, the VBAT_H interrupt will be issued. If VBAT is lower than the threshold specified by another register setting, the VBAT_L interrupt will be issued.

5. Speaker OC interrupt
   MT6329 supports speaker OC interrupt generation which uses PWM detection method.

6. BUCK OC interrupt
   MT6329 supports VPA and VRF18 OC interrupt generation which uses PWM detection method.

7. LDO OC interrupt
   MT6329 supports LDO OC interrupt generation. It will be issued if any one of the LDOs has OC condition.

MT6329 interrupt tables:

STRUP	PWRKEY_DEB_INT_FLAG	RG_PWRKEY_INT_EN	bank0, 0x16, bit 1	RG_PWRKEY_INT_STATUS	bank0, 0x19, bit1	
STRUP	HOMEKEY_DEB_INT_FLAG	RG_HOMEKEY_INT_EN	bank0, 0x18, bit 5	RG_HOMEKEY_INT_STATUS	bank0, 0x1B, bit5	
STRUP	THR_H_INT_FLAG	RG_THR_H_INT_EN	bank0, 0x16, bit 3	RG_THR_H_INT_STATUS	bank0, 0x19, bit3	edge(rising)
STRUP	THR_L_INT_FLAG	RG_THR_L_INT_EN	bank0, 0x16, bit 2	RG_THR_L_INT_STATUS	bank0, 0x19, bit2	edge(falling)
Charger	CHRDET_INT_FLAG	RG_CHRDET_INT_EN	bank0, 0x16, bit 6	RG_CHRDET_INT_STATUS	bank0, 0x19, bit6	edge(rising & falling)
Charger	OV_INT_FLAG	RG_OV_INT_EN	bank0, 0x16, bit 7	RG_OV_INT_STATUS	bank0, 0x19, bit7	
Charger	WATCHDOG_INT_FLAG	RG_WATCHDOG_INT_EN	bank0, 0x16, bit 0	RG_WATCHDOG_INT_STATUS	bank0, 0x19, bit0	level
Charger	OTG_BVALID	RG_BVALID_DET_INT_EN	bank0, 0x16, bit 5	RG_BVALID_DET_INT_STATUS	bank0, 0x19, bit5	level
Charger	VBATON_UNDET	RG_VBATON_UNDET_INT_EN	bank0, 0x16, bit 4	RG_VBATON_UNDET_INT_STATUS	bank0, 0x19, bit4	level
Auxadc	HIGHBATTERY_INT_FLAG	RG_HIGH_BAT_INT_EN	bank0, 0x17, bit 5	RG_HIGH_BAT_INT_STATUS	bank0, 0x1A, bit5	level
Auxadc	LOWBATTERY_INT_FLAG	RG_LOW_BAT_INT_EN	bank0, 0x17, bit 4	RG_LOW_BAT_INT_STATUS	bank0, 0x1A, bit4	level
FGADC	VBAT_H_INT_FLAG	RG_FG_BAT_H_INT_EN	bank0, 0x17, bit 7	RG_FG_BAT_H_INT_STATUS	bank0, 0x1A, bit7	level
FGADC	VBAT_L_INT_FLAG	RG_FG_BAT_L_INT_EN	bank0, 0x17, bit 6	RG_FG_BAT_L_INT_STATUS	bank0, 0x1A, bit6	level
Speaker	SPKR_D_OC_FLAG	RG_SPKR_D_OC_INT_EN	bank0, 0x17, bit 3	RG_SPKR_D_OC_INT_STATUS	bank0, 0x1A, bit3	level
Speaker	SPKL_D_OC_FLAG	RG_SPKL_D_OC_INT_EN	bank0, 0x17, bit 2	RG_SPKL_D_OC_INT_STATUS	bank0, 0x1A, bit2	level
Speaker	SPKR_AB_OC_FLAG	RG_SPKR_AB_OC_INT_EN	bank0, 0x17, bit 1	RG_SPKR_AB_OC_INT_STATUS	bank0, 0x1A, bit1	level
Speaker	SPKL_AB_OC_FLAG	RG_SPKL_AB_OC_INT_EN	bank0, 0x17, bit 0	RG_SPKL_AB_OC_INT_STATUS	bank0, 0x1A, bit0	level
Regulator	VRF18_OC_FLAG	RG_VRF18_OC_INT_EN	bank0, 0x18, bit 4	RG_VRF18_OC_INT_STATUS	bank0, 0x1B, bit4	level
Regulator	VPA_OC_FLAG	RG_VPA_OC_INT_EN	bank0, 0x18, bit 3	RG_VPA_OC_INT_STATUS	bank0, 0x1B, bit3	level
Regulator	LDO_OC_FLAG	RG_LDO_OC_INT_EN	bank0, 0x18, bit 2	RG_LDO_OC_INT_STATUS	bank0, 0x1B, bit2	level

PWRKEY_DEB_INT_FLAG	1	50ms (in STRUP)	Write 1 Clear
HOMEKEY_DEB_INT_FLAG	0	50ms (in STRUP)	Write 1 Clear
THR_H_INT_FLAG	0	40ms (in STRUP)	Write 1 Clear
THR_L_INT_FLAG	0	40ms (in STRUP)	Write 1 Clear
CHRDET_INT_FLAG	1	50ms (in STRUP)	Read Clear
OV_INT_FLAG	1	4us (in PCHR_DIG)	
WATCHDOG_INT_FLAG	1	No	Write 1 Clear
OTG_BVALID	1	0/100/200/400us (in INT_CTRL)	Write 1 Clear
VBATON_UNDET	1	4us (in PCHR_DIG)	Write 1 Clear
HIGHBATTERY_INT_FLAG	0	V (in AUXADC)	Write 1 Clear
LOWBATTERY_INT_FLAG	0	V (in AUXADC)	Write 1 Clear
VBAT_H_INT_FLAG	0	V (in FGADC)	Write 1 Clear
VBAT_L_INT_FLAG	0	V (in FGADC)	Write 1 Clear
SPKR_D_OC_FLAG	0	V (in SPK)	Write 1 Clear
SPKL_D_OC_FLAG	0	V (in SPK)	Write 1 Clear
SPKR_AB_OC_FLAG	0	V (in SPK)	Write 1 Clear
SPKL_AB_OC_FLAG	0	V (in SPK)	Write 1 Clear
VRF18_OC_FLAG	0	PMW deb (in INT_CTRL)	Write 1 Clear
VPA_OC_FLAG	0	PMW deb (in INT_CTRL)	Write 1 Clear
LDO_OC_FLAG	1	100/200/400/800us (in INT_CTRL)	Write 1 Clear

Watchdog is used to monitor whether the baseband is still awake while charging. The user can set up the time-out threshold by TIMEOUT_GEAR. They are 4s, 8s, 16s, and 32s respectively. The figure below is the state diagram of watchdog. Watchdog timer starts to count when the charger enabling register is set. If the software does not write the specific register within designated time, the watchdog will time out and issue interrupts. It means that the watchdog is also one type of interrupt source in addition to those described in 4.3.10.1. The software can select a proper time-out value by setting up the time-out gear register. Like most of the interrupt mechanism mentioned above, the watchdog interrupt is write-clear.

PMIC can start to charge only when the charger is detected, charger enabling register is set, and watchdog is not timed-out. If one of the three conditions is false, the charging will be prohibited.

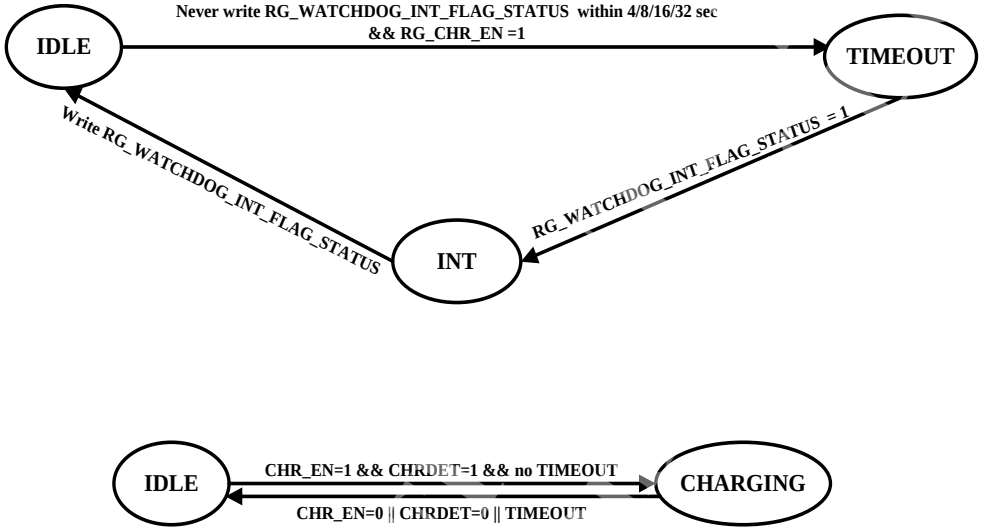


Figure 13: Watchdog

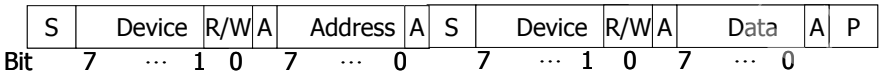
PMIC uses a 2-wire interface consisting of a clock and data signals (SCL and SDA) to connect to BB. This bi-directional serial bus interface allows BB to write commands to and read status from PMIC. The SCL signal is driven by the master, whereas the SDA signal is bidirectional and can be driven by either the master or slave.

I2C write cycle:

	S	Device				R/W	A	Address				A	Data				A	P
Bit		7	…	1		0		7	…		0		7	…		0		

"S" is the start bit as defined in I2C spec. "Device" is the device ID, and our device ID is "1100000". R/W is read/write flag of the following byte. 1 means read, and 0 means write. "A" is the acknowledgement bit. "P" is the stop bit. The number below the blue bar is the bit order. The device has 7 bits from 7 to 1, and bit 0 is R/W. The "Address" and "Data" both have 8 bits. After the write sequence, the data in "Data" will be written to address "Address".

I2C read cycle:



The write sequence has 3 byte of data, but the read sequence has 4 bytes. In the read sequence, the device and R/W are sent twice, and R/W is 0 (write) at the first time and 1 (read) at the second time. There are also two start bits. The second start bit means the device will be sent again, and the read/write mode can be switched. The address is sent from the host, and the data will be given from the device.

There are two register banks: bank 0 and bank 1

Bank 0

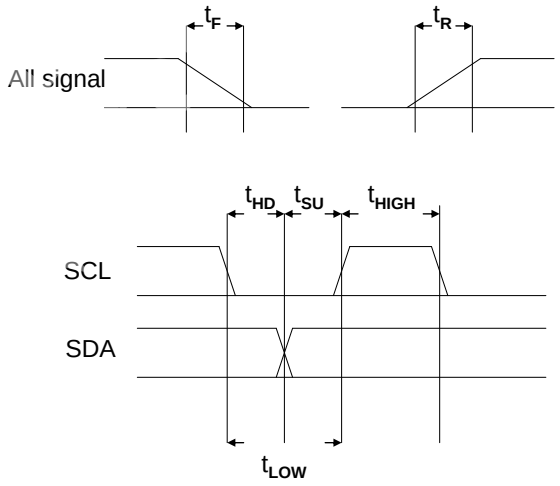
Device address[7:1] = 0110000

Includes top, startup, interrupt, pulse charger, Buck, analog LDO, digital LDO and AUXADC related control settings.

Bank 1

Device address[7:1] = 0110001

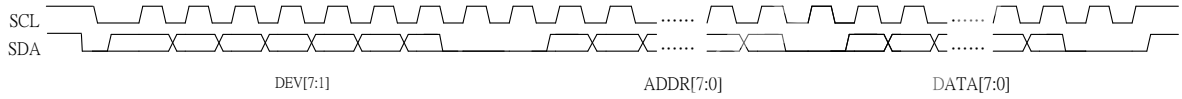
Includes test, driver, boost, speaker, analog switch, fuel gauge, OTP and I2C related control settings.



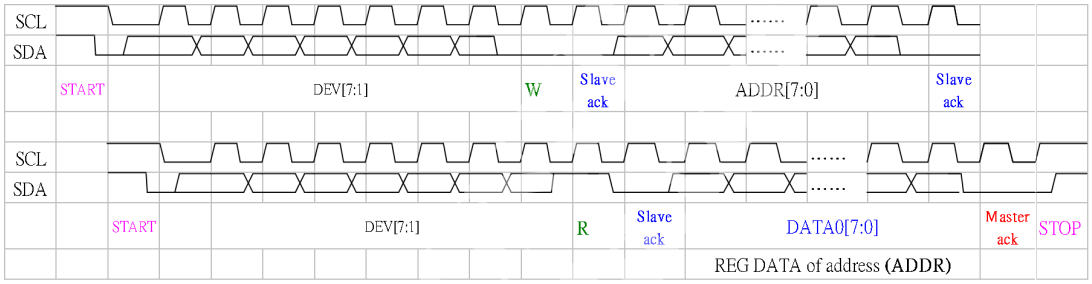
Constraint	Min.	Max.	Description
t_F	25ns	100ns	Fall time
t_R	25ns	100ns	Rise time
t_{HD}	100ns	-	Hold time of SDA to SCL

Constraint	Min.	Max.	Description
t_{SU}	100ns	-	Setup time of SDA to SCL
t_{HIGH}	100ns	-	Period when SCL is high
t_{LOW}	100ns	-	Period when SCL is low

(1) MTK's register write protocol



(2) MTK's register read protocol



SCL and SDA can be pulled high optionally by I2C_PULL_HIGH_B. If the master in baseband forces to send 1 through SCL and SDA to slave, the slave can set I2C_PULL_HIGH_B to 1 (not pull high internally) to save power. If the master only pulls SCL and SDA high internally, I2C_PULL_HIGH_B must be set to 0 to meet the I2C protocol.

Address	Name	Width	Register Function
21	CHR_CON0	8	**Charger Control Register 0** Set this register for PMIC Charger circuit configuration controls.
22	CHR_CON1	8	**Charger Control Register 1**
23	CHR_CON2	8	**Charger Control Register 2** Set this register for PMIC Charger circuit configuration controls.
24	CHR_CON3	8	**Charger Control Register 3**
25	CHR_CON4	8	**Charger Control Register 4**

			Set this register for PMIC Charger circuit configuration controls.
27	CHR_CON6	8	**Charger Control Register 6** Set this register for PMIC Charger circuit configuration controls.
28	CHR_CON7	8	**Charger Control Register 7**
2B	CHR_CONA	8	**Charger Control Register 10** Set this register for PMIC Charger circuit configuration controls.
2E	CHR_COND	8	**Charger Control Register 13**
30	CHR_CONF	8	**Charger Control Register 15**
44	VPROC_CON5	8	**VPROC Control Register 5**
45	VPROC_CON6	8	**VPROC Control Register 6**
47	VPROC_CON8	8	**VPROC Control Register 8**
48	VPROC_CON9	8	**VPROC Control Register 9**
49	VPROC_CONA	8	**VPROC Control Register A**
4A	VPROC_CONB	8	**VPROC Control Register B**
4B	VPROC_CONC	8	**VPROC Control Register C**
57	VCORE_CON5	8	**VCORE Control Register 5**
59	VCORE_CON7	8	**VCORE Control Register 7**
60	VRF18_CON3	8	**VRF18 Control Register 3**
73	VPA_CON3	8	**VPA Control Register 3**
75	VPA_CON5	8	**VPA Control Register 5**
76	VPA_CON6	8	**VPA Control Register 6**
77	VPA_CON7	8	**VPA Control Register 7**
78	VPA_CON8	8	**VPA Control Register 8**
79	VPA_CON9	8	**VPA Control Register 9**
7A	VPA_CONA	8	**VPA Control Register A**
7B	VPA_CONB	8	**VPA Control Register B**
7C	VPA_CONC	8	**VPA Control Register C**
7D	VPA_COND	8	**VPA Control Register D**
7E	VPA_CONE	8	**VPA Control Register E**
7F	VPA_CONF	8	**VPA Control Register F**
83	DIGLDO_CON1	8	**Digital LDO Control Register 1**
87	DIGLDO_CON5	8	**Digital LDO Control Register 5**
95	DIGLDO_CON13	8	**Digital LDO Control Register 13**
98	DIGLDO_CON16	8	**Digital LDO Control Register 16**
9E	DIGLDO_CON1C	8	**Digital LDO Control Register 1C**
A1	DIGLDO_CON1F	8	**Digital LDO Control Register 1F**
A4	DIGLDO_CON22	8	**Digital LDO Control Register 22**
A7	DIGLDO_CON25	8	**Digital LDO Control Register 25**
AB	DIGLDO_CON29	8	**Digital LDO Control Register 29**
AF	DIGLDO_CON2D	8	**Digital LDO Control Register 2D**
B2	DIGLDO_CON30	8	**Digital LDO Control Register 30**
B5	DIGLDO_CON33	8	**Digital LDO Control Register 33**
B7	DIGLDO_CON35	8	**Digital LDO Control Register 35**
B8	DIGLDO_CON36	8	**Digital LDO Control Register 36**
BA	DIGLDO_RSV	8	**Reserved register**

BE	ANALDO_CON1	8	Analog LDO Control Register 1
C1	ANALDO_CON4	8	Analog LDO Control Register 4
C8	ANALDO_CONB	8	Analog LDO Control Register B
CB	ANALDO_CONE	8	Analog LDO Control Register E
D0	ANALDO_CON13	8	Analog LDO Control Register 13
DA	AUXADC_CON0	8	AUXADC Control Register 0
DB	AUXADC_CON1	8	AUXADC Control Register 1
DC	AUXADC_CON2	8	AUXADC Control Register 2
DD	AUXADC_CON3	8	AUXADC Control Register 3
DE	AUXADC_CON4	8	AUXADC Control Register 4
DF	AUXADC_CON5	8	AUXADC Control Register 5
E0	AUXADC_CON6	8	AUXADC Control Register 6
E1	AUXADC_CON7	8	AUXADC Control Register 7
E2	AUXADC_CON8	8	AUXADC Control Register 8
E3	AUXADC_CON9	8	AUXADC Control Register 9
E6	AUXADC_CON12	8	AUXADC Control Register 12
E7	AUXADC_CON13	8	AUXADC Control Register 13
E8	AUXADC_CON14	8	AUXADC Control Register 14

Bit	7	6	5	4	3	2	1	0
Name								
Type	RO		RO	RW	RW		RO	RW
Reset	0		0	0	0		0	1

Bit(s)	Mnemonic	Name	Description
7		VCDT_HV_DET	**Charger-in high voltage detection (with de-bounce).** 0: charge-in voltage < VCDT_HV_VTH 1: charge-in voltage > VCDT_HV_VTH
5		CHRDET	**Charger-in detect.**
4		CHR_EN	**Charger enable setting, which would gated CSDAC_EN & PCHR_AUTO & charger watch-dog timer**
3		CSDAC_EN	**CS DAC enable.**
1		CHR_LDO_DET	**Charger LDO Detect. If not detect, PCHR won't work**
0		VCDT_HV_EN	**Charger-in high voltage detection comparator enable.** 0: disable. Only compare LV threshold 1: enable. Compare both LV and HV threshold

Bit	7	6	5	4	3	2	1	0
Name								

Type	RW							
Reset	1	1	1	1				

Bit(s)	Mnemonic	Name	Description
7:4		VCDT_HV_VTH	**Charger-in high voltage detection vth.** 0000~1000: 4.2V~4.6V with 50mV/step 1001~1100: 6V~7.5V with 500mV/step 1101~1111: 8.5V~10.5V with 1000mV/step

Bit	7	6	5	4	3	2	1	0
Name								
Type	RO	RO	RO		RW		RW	
Reset	0	0	0		0		0	

Bit(s)	Mnemonic	Name	Description
7		VBAT_CC_DET	**VBAT voltage detection for CC.** 0: VBAT voltage < VBAT_CC_VTH 1: VBAT voltage > VBAT_CC_VTH
6		VBAT_CV_DET	**VBAT voltage detection for CV.** 0: VBAT voltage < VBAT_CV_VTH 1: VBAT voltage > VBAT_CV_VTH
5		CS_DET	**Current sense voltage detection.** 0: CS voltage < CS_VTH 1: CS voltage > CS_VTH
3		CS_EN	**Current sense voltage detection comparator enable.**
1		VBAT_CV_EN	**Battery CV detection enable (0: disable, 1: enable)**

Bit	7	6	5	4	3	2	1	0
Name								
Type				RW				
Reset				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		VBAT_CV_VTH	**Battery CV dection threshold trimming option, default 4.2V** this register is used for FT CV threshold trimming and not for customer's fine tuning (pchr_dig should invert MSB bit. otherwise, BC1.1 2.2V threshold would be wrong) 10000~11111: 4.0000V~4.1875V with 12.5mV/step 00000~00111: 4.2000V~4.2875V with 12.5mV/step 01000~01110: 4.2000V~4.2750V with 12.5mV/step 01111: 2.2V (used in BC1.1 application)

Bit	7	6	5	4	3	2	1	0
Name								
Type					RW			
Reset					1	1	1	1

Bit(s)	Mnemonic	Name	Description
3:0		CS_VTH	**Current sense voltage detection threshold @ Rcs=0.2ohm** 1111: 70mA 1110: 200mA 1101: 400mA 1100: 450mA 1011: 550mA 1010: 650mA 1001: 700mA 1000: 800mA 0111: 900mA 0110: 1000mA 0101: 1100mA 0100: 1200mA 0011: 1300mA 0010: 1400mA 0001: 1500mA 0000: 1600mA

Bit	7	6	5	4	3	2	1	0
Name								
Type		RO	RW			RW		RW
Reset		0	0			1	1	1

Bit(s)	Mnemonic	Name	Description
6		VBAT_OV_DET	**VBAT_OV voltage detection.** 0: VBAT voltage < VBAT_OV_VTH 1: VBAT voltage > VBAT_OV_VTH
5		VBAT_OV_DEG	**VBAT OV voltage detection deglitch enable.** 0: no debounce 1: debounce one cycle (1us)
2:1		VBAT_OV_VTH	**VBAT OV voltage detection threshold** 00: 4.300V 01: 4.350V 10: 4.375V 11: 4.115V
0		VBAT_OV_EN	**VBAT OV over-voltage detection comparator enable.**

Bit	7	6	5	4	3	2	1	0

Name								
Type	RO					RW	RW	
Reset	0					0	1	

Bit(s)	Mnemonic	Name	Description
7		BATON_UNDET	**BATON_UNDET voltage detection. BATON_UNDET always is 0 during DDLO/UVLO** 0 Battery is OK 1 Battery is Fail
2		BATON_HT_EN	**Battery-On HW high temperature detection (1: enable, 0: disable)**
1		BATON_EN	**BATON_UNDET detection enable.** 0 BATON_UNDET always = 0 1 Compare enable

Bit	7	6	5	4	3	2	1	0
Name								
Type		RO	RW					
Reset		0	1					

Bit(s)	Mnemonic	Name	Description
6		OTG_BVALID	**Indicates if the session for B-peripheral is valid (0.8V<Vth<4V). Here VBUS is connected to CHRIN.** 0: Vbus < 0.8V 1: Vbus > 4V
5		OTG_BVALID_EN	**BVALID detect enable.**

Bit	7	6	5	4	3	2	1	0
Name								
Type				RW	RW			
Reset				1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4		CHRWDT_EN	**Enable setting for charger watch-dog timer** 0: disable 1: enable if (CHR_EN(@CHR_CON0) == 1) Note1: UVLO don't care this bit and will timeout after 3000s Note2: PCHR_TESTMODE can force to control watch-dog enable by using this bit
3:0		CHRWDT_TD	**Time constant setting for charger watch-dog timer** b0000: 4 sec

Bit(s)	Mnemonic	Name	Description
			b0001: 8 sec b0010: 16 sec b0011: 32 sec b0100: 128 sec b0101: 256 sec b0110: 512 sec b0111: 1024 sec b1xxx: 3000 sec

Bit	7	6	5	4	3	2	1	0
Name								
Type						RO	RW	RW
Reset						0	0	0

Bit(s)	Mnemonic	Name	Description
2		CHRWDT_OUT	**Time-out flag for charger watch-dog timer** Read: 0: no time-out status 1: has time-out status Write: 1: clear time-out status flag to 0
1		CHRWDT_FLAG_WR	**Time-out flag for charger watch-dog timer** Read: 0: no time-out status 1: has time-out status Write: 1: clear time-out status flag to 0
0		CHRWDT_INT_EN	**Interrupt enable setting for charger watch-dog timer.**

Bit	7	6	5	4	3	2	1	0
Name								
Type				RW				
Reset				1	0	1	0	0

Bit(s)	Mnemonic	Name	Description
4:0		RG_VPROC_VOSEL	**Vout selection** (25mV/step) 00000: 0.700V 00001: 0.725V 00010: 0.750V 00011: 0.775V 00100: 0.800V 00101: 0.825V 00110: 0.850V 00111: 0.875V 01000: 0.900V 01001: 0.925V

Bit(s)	Mnemonic	Name	Description
			01010: 0.950V 01011: 0.975V 01100: 1.000V 01101: 1.025V 01110: 1.050V 01111: 1.075V 10000: 1.100V 10001: 1.125V 10010: 1.150V 10011: 1.175V 10100: 1.200V 10101: 1.225V 10110: 1.250V 10111: 1.275V 11000: 1.300V 11001~11111: 1.300V

Bit	7	6	5	4	3	2	1	0
Name								
Type				RW				
Reset				1	0	1	0	0

Bit(s)	Mnemonic	Name	Description
4:0		VPROC_VOSEL_SRCLKEN0	**VPROC voltage setting for SRCLKEN=0** The setting is the same as RG_VPROC_VOSEL

Bit	7	6	5	4	3	2	1	0
Name								
Type				RW				
Reset				1	0	1	0	0

Bit(s)	Mnemonic	Name	Description
4:0		VPROC_VOSEL_DVS00	**VPROC voltage setting for DVS=00** The setting is the same as RG_VPROC_VOSEL

Bit	7	6	5	4	3	2	1	0
Name								
Type				RW				
Reset				1	0	1	0	0

Bit(s)	Mnemonic	Name	Description

Bit(s)	Mnemonic	Name	Description
4:0		VPROC_VOSEL_DVS01	**VPROC voltage setting for DVS=01** The setting is the same as RG_VPROC_VOSEL

Bit	7	6	5	4	3	2	1	0
Name								
Type				RW				
Reset				1	0	1	0	0

Bit(s)	Mnemonic	Name	Description
4:0		VPROC_VOSEL_DVS10	**VPROC voltage setting for DVS=10** The setting is the same as RG_VPROC_VOSEL

Bit	7	6	5	4	3	2	1	0
Name								
Type				RW				
Reset				1	0	1	0	0

Bit(s)	Mnemonic	Name	Description
4:0		VPROC_VOSEL_DVS11	**VPROC voltage setting for DVS=11** The setting is the same as RG_VPROC_VOSEL

Bit	7	6	5	4	3	2	1	0
Name								
Type							RW	
Reset							0	0

Bit(s)	Mnemonic	Name	Description
1:0		RG_VPROC_CTRL	**VPROC control** 00: by SW RG_VPROC_VOSEL 01: Only by SRCLKEN 1x: Control by SRCLKEN and DVS1/0

Bit	7	6	5	4	3	2	1	0

Name								
Type				RW				
Reset				1	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		RG_VCORE_VOSEL	**Vout selection** (25mV/step) 5'b00000: 0.700V 5'b00001: 0.725V 5'b00010: 0.750V 5'b00011: 0.775V 5'b00100: 0.800V 5'b00101: 0.825V 5'b00110: 0.850V 5'b00111: 0.875V 5'b01000: 0.900V 5'b01001: 0.925V 5'b01010: 0.950V 5'b01011: 0.975V 5'b01100: 1.000V 5'b01101: 1.025V 5'b01110: 1.050V 5'b01111: 1.075V 5'b10000: 1.100V 5'b10001: 1.125V 5'b10010: 1.150V 5'b10011: 1.175V 5'b10100: 1.200V 5'b10101: 1.225V 5'b10110: 1.250V 5'b10111: 1.275V 5'b11000: 1.300V 5'b11001: 1.300V 5'b11010: 1.300V 5'b11011: 1.300V 5'b11100: 1.300V 5'b11101: 1.300V 5'b11110: 1.300V 5'b11111: 1.300V

Bit	7	6	5	4	3	2	1	0
Name								
Type								RW
Reset								0

Bit(s)	Mnemonic	Name	Description
0		RG_VCORE_CTRL	**VCORE control** 0: by SW RG_VCORE_VOSEL 1: by SRCLKEN

Bit	7	6	5	4	3	2	1	0
Name								
Type								RW
Reset								0

Bit(s)	Mnemonic	Name	Description
0		RG_VRF18_EN	**VRF18 enable** 1'b1: enable 1'b0: disable

Bit	7	6	5	4	3	2	1	0
Name								
Type								RW
Reset								0

Bit(s)	Mnemonic	Name	Description
0		RG_VPA_EN	**VPA enable signal** 0: disable 1: enable

Bit	7	6	5	4	3	2	1	0
Name								
Type				RW				
Reset				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		RG_VPA_VOSEL	**Vout selection** 00000: 0.9V ~ 11001: 3.4V (100mV/step) 5'b00000: 0.9V 5'b00001: 1.0V 5'b00010: 1.1V 5'b00011: 1.2V 5'b00100: 1.3V 5'b00101: 1.4V 5'b00110: 1.5V 5'b00111: 1.6V 5'b01000: 1.7V 5'b01001: 1.8V 5'b01010: 1.9V 5'b01011: 2.0V 5'b01100: 2.1V 5'b01101: 2.2V 5'b01110: 2.3V 5'b01111: 2.4V 5'b10000: 2.5V

Bit(s)	Mnemonic	Name	Description
			5'b10001: 2.6V 5'b10010: 2.7V 5'b10011: 2.8V 5'b10100: 2.9V 5'b10101: 3.0V 5'b10110: 3.1V 5'b10111: 3.2V 5'b11000: 3.3V 5'b11001: 3.4V 5'b11010~5'b11111: 3.4V

Bit	7	6	5	4	3	2	1	0
Name								
Type				RW				
Reset				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		RG_PASEL_SET0	**VPA voltage control with PASEL=000** same as RG_VPA_VOSEL

Bit	7	6	5	4	3	2	1	0
Name								
Type				RW				
Reset				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		RG_PASEL_SET1	**VPA voltage control with PASEL=001** same as RG_VPA_VOSEL

Bit	7	6	5	4	3	2	1	0
Name								
Type				RW				
Reset				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		RG_PASEL_SET2	**VPA voltage control with PASEL=010** same as RG_VPA_VOSEL

Bit	7	6	5	4	3	2	1	0
Name								
Type				RW				
Reset				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		RG_PASEL_SET3	**VPA voltage control with PASEL=011** same as RG_VPA_VOSEL

Bit	7	6	5	4	3	2	1	0
Name								
Type				RW				
Reset				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		RG_PASEL_SET4	**VPA voltage control with PASEL=100** same as RG_VPA_VOSEL

Bit	7	6	5	4	3	2	1	0
Name								
Type				RW				
Reset				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		RG_PASEL_SET5	**VPA voltage control with PASEL=101** same as RG_VPA_VOSEL

Bit	7	6	5	4	3	2	1	0
Name								
Type				RW				
Reset				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		RG_PASEL_SET6	**VPA voltage control with PASEL=110** same as RG_VPA_VOSEL

Bit	7	6	5	4	3	2	1	0
Name								
Type				RW				
Reset				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		RG_PASEL_SET7	**VPA voltage control with PASEL=111** same as RG_VPA_VOSEL

Bit	7	6	5	4	3	2	1	0
Name								
Type	RW			RW				RW
Reset	0	0	0	0				0

Bit(s)	Mnemonic	Name	Description
7:5		RG_VPA_RSV	**reserved**
4		RG_VPA_VO_UP50MV	**Vout shift selection** 0: no shift 1: shift up by 50mV
0		RG_VPA_CTRL	**VPA control** 0: by SW RG_VPA_CAL 1: by PASEL2/1/0

Bit	7	6	5	4	3	2	1	0
Name								
Type				RO				
Reset				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		QI_VPA_VOSEL	

Bit	7	6	5	4	3	2	1	0
Name								
Type	RO							RW
Reset	0							1

Bit(s)	Mnemonic	Name	Description	
7		QI_VM12_1_EN	**LDO enable/disable status**	
0		VM12_1_EN	**VM12 enable** 1'b1: 1'b0: disable	enable

Bit	7	6	5	4	3	2	1	0
Name								
Type								RW
Reset								1

Bit(s)	Mnemonic	Name	Description	
0		VM12_2_EN	**VM12_2 enable** 1'b1: 1'b0: disable	enable

Bit	7	6	5	4	3	2	1	0
Name								
Type				RW				RW
Reset				1				0

Bit(s)	Mnemonic	Name	Description	
4		RG_VSIM_VOSEL	**output selection signal** (1'b0:1.8V) 1'b0: 1'b1: 3.0V	1.8V
0		RG_VSIM_EN	**Enable** 1'b1: 1'b0: disable	enable

Bit	7	6	5	4	3	2	1	0
Name								
Type		RW						RW
Reset		1	0	1				0

Bit(s)	Mnemonic	Name	Description
6:4		RG_VSIM2_VOSEL	**output selection signal** (3'b010:1.8V) 3'b000: 1.3V 3'b001: 1.5V 3'b010: 1.8V 3'b011: 2.5V 3'b100: 2.8V 3'b101: 3.0V 3'b110: 3.3V 3'b111: 3.3V
0		RG_VSIM2_EN	**Enable** (1'b1: enable; 1'b0: disable) 1'b1: enable 1'b0: disable

Bit	7	6	5	4	3	2	1	0
Name								
Type		RW						RW
Reset		0	0	1				0

Bit(s)	Mnemonic	Name	Description
6:4		RG_VCAMD_VOSEL	**output selection signal** (3'b000:1.3V) 3'b000: 1.3V 3'b001: 1.5V 3'b010: 1.8V 3'b011: 2.5V 3'b100: 2.8V 3'b101: 3.0V 3'b110: 3.3V 3'b111: 1.2V
0		RG_VCAMD_EN	**Enable** 1'b1: enable 1'b0: disable

Bit	7	6	5	4	3	2	1	0
Name								
Type		RW						RW
Reset		0	1	0				0

Bit(s)	Mnemonic	Name	Description
6:4		RG_VCAM_IO_VOSEL	**output selection signal** (3'b010:1.8V) 3'b000: 1.3V 3'b001: 1.5V

Bit(s)	Mnemonic	Name	Description
			3'b010: 1.8V 3'b011: 2.5V 3'b100: 2.8V 3'b101: 3.0V 3'b110: 3.3V 3'b111: 3.3V
0		RG_VCAM_IO_EN	**Enable** 1'b1: enable 1'b0: disable

Bit	7	6	5	4	3	2	1	0
Name								
Type		RW						RW
Reset		1	0	0				0

Bit(s)	Mnemonic	Name	Description
6:4		RG_VCAM_AF_VOSEL	**output selection signal** (3'b100:2.8V) 3'b000: 1.3V 3'b001: 1.5V 3'b010: 1.8V 3'b011: 2.5V 3'b100: 2.8V 3'b101: 3.0V 3'b110: 3.3V 3'b111: 3.3V
0		RG_VCAM_AF_EN	**Enable** 1'b1: enable 1'b0: disable

Bit	7	6	5	4	3	2	1	0
Name								
Type		RW						RW
Reset		1	1	1				1

Bit(s)	Mnemonic	Name	Description
6:4		RG_VMC_VOSEL	**output selection signal** (3'b100:2.8V) 3'b000: 1.3V 3'b001: 1.5V 3'b010: 1.8V 3'b011: 2.5V 3'b100: 2.8V 3'b101: 3.0V 3'b110: 3.3V

Bit(s)	Mnemonic	Name	Description
			3'b111: 3.3V
0		RG_VMC_EN	**VMC0 enable** 1'b1: enable 1'b0: disable

Bit	7	6	5	4	3	2	1	0
Name								
Type		RW						RW
Reset		1	1	1				1

Bit(s)	Mnemonic	Name	Description
6:4		RG_VMCH_VOSEL	**output selection signal** (3'b100:2.8V) 3'b000: 1.3V 3'b001: 1.5V 3'b010: 1.8V 3'b011: 2.5V 3'b100: 2.8V 3'b101: 3.0V 3'b110: 3.3V 3'b111: 3.3V
0		RG_VMCH_EN	**VMC1 enable** 1'b1: enable 1'b0: disable

Bit	7	6	5	4	3	2	1	0
Name								
Type		RW						RW
Reset		1	0	0				0

Bit(s)	Mnemonic	Name	Description
6:4		RG_VGP_VOSEL	**output selection signal** (3'b100:2.8V) 3'b000: 1.3V 3'b001: 1.5V 3'b010: 1.8V 3'b011: 2.5V 3'b100: 2.8V 3'b101: 3.0V 3'b110: 3.3V 3'b111: 3.3V
0		RG_VGP_EN	**Enable** 1'b1: enable 1'b0: disable

Bit	7	6	5	4	3	2	1	0
Name								
Type		RW						RW
Reset		1	0	0				0

Bit(s)	Mnemonic	Name	Description
6:4		RG_VGP2_VOSEL	**output selection signal** (3'b100:2.8V) 3'b000: 1.3V 3'b001: 1.5V 3'b010: 1.8V 3'b011: 2.5V 3'b100: 2.8V 3'b101: 3.0V 3'b110: 3.3V 3'b111: 3.3V
0		RG_VGP2_EN	**Enable** 1'b1: enable 1'b0: disable

Bit	7	6	5	4	3	2	1	0
Name								
Type		RW						RW
Reset		1	1	0				0

Bit(s)	Mnemonic	Name	Description
6:4		RG_VIBR_VOSEL	**output selection signal** (3'b110:3.3V) 3'b000: 1.3V 3'b001: 1.5V 3'b010: 1.8V 3'b011: 2.5V 3'b100: 2.8V 3'b101: 3.0V 3'b110: 3.3V 3'b111: 3.3V
0		RG_VIBR_EN	**Enable** 1'b1: enable 1'b0: disable

Bit	7	6	5	4	3	2	1	0
Name								
Type		RO	RO	RO	RO	RO	RO	RO
Reset		0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
6		RO_QI_VUSB_OC_STATUS	**over current status** 1'b1: over current occur 1'b0: no over current occur
5		RO_QI_VSIM2_OC_STATUS	**over current status** 1'b1: over current occur 1'b0: no over current occur
4		RO_QI_VSIM_OC_STATUS	**over current status** 1'b1: over current occur 1'b0: no over current occur
3		RO_QI_VIO28_OC_STATUS	**over current status** 1'b1: over current occur 1'b0: no over current occur
2		RO_QI_VM12_INT_OC_STATUS	**over current status** 1'b1: over current occur 1'b0: no over current occur
1		RO_QI_VM12_2_OC_STATUS	**over current status** 1'b1: over current occur 1'b0: no over current occur
0		RO_QI_VM12_1_OC_STATUS	**over current status** 1'b1: over current occur 1'b0: no over current occur

Bit	7	6	5	4	3	2	1	0
Name								
Type	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7		RO_QI_VIBR_OC_STATUS	**over current status** 1'b1: over current occur 1'b0: no over current occur
6		RO_QI_VGP2_OC_STATUS	**over current status** 1'b1: over current occur 1'b0: no over current occur
5		RO_QI_VGP_OC_STATUS	**over current status** 1'b1: over current occur

Bit(s)	Mnemonic	Name	Description
			1'b0: no over current occur
4		RO_QI_VMCH_OC_STATUS	**over current status** 1'b1: over current occur 1'b0: no over current occur
3		RO_QI_VMC_OC_STATUS	**over current status** 1'b1: over current occur 1'b0: no over current occur
2		RO_QI_VCAM_AF_OC_STATUS	**over current status** 1'b1: over current occur 1'b0: no over current occur
1		RO_QI_VCAM_IO_OC_STATUS	**over current status** 1'b1: over current occur 1'b0: no over current occur
0		RO_QI_VCAMD_OC_STATUS	**over current status** 1'b1: over current occur 1'b0: no over current occur

Bit	7	6	5	4	3	2	1	0
Name								
Type					RW			
Reset					0	0		

Bit(s)	Mnemonic	Name	Description
3:2		RG_VM12_2_VOSEL	**VM12_2 output voltage select** 2'b00: 1.2V 2'b01: 1.1V 2'b10: 1.0V 2'b11: 0.9V

Bit	7	6	5	4	3	2	1	0
Name								
Type							RW	RW
Reset							0	0

Bit(s)	Mnemonic	Name	Description
1		VRF_ON_CTRL	**VRF enable control** 0: SW control by RG_VRF_EN 1: SRCLKEN
0		RG_VRF_EN	**VRF enable**

Bit	7	6	5	4	3	2	1	0

Name								
Type	RO							RW
Reset	0							1

Bit(s)	Mnemonic	Name	Description	
7		QI_VTCXO_EN	**VTCXO enable status** 1'b1: 1'b0: disable	enable
0		RG_VTCXO_EN	**VTCXO enable** 1'b1: 1'b0: disable	enable

Bit	7	6	5	4	3	2	1	0
Name								
Type								RW
Reset								1

Bit(s)	Mnemonic	Name	Description	
0		RG_VA2_EN	**VA2 enable** 1'b1: 1'b0: disable	enable

Bit	7	6	5	4	3	2	1	0
Name								
Type			RW					RW
Reset			1	1				0

Bit(s)	Mnemonic	Name	Description	
5:4		RG_VCAMA_VOSEL	**output voltage select** 2'b00: 2'b01: 2b'10: 2b'11: 2.8V	1.5V 1.8V 2.5V
0		RG_VCAMA_EN	**Enable** 1'b1: 1'b0: disable	enable

Bit	7	6	5	4	3	2	1	0
Name								
Type				RO	RO	RO	RO	RO
Reset				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4		RO_QI_VCAMA_OC_STATUS	**over current status** 1'b1: over current occur 1'b0: no over current occur
3		RO_QI_VA2_OC_STATUS	**over current status** 1'b1: over current occur 1'b0: no over current occur
2		RO_QI_VA1_OC_STATUS	**over current status** 1'b1: over current occur 1'b0: no over current occur
1		RO_QI_VTCXO_OC_STATUS	**over current status** 1'b1: over current occur 1'b0: no over current occur
0		RO_QI_VRF_OC_STATUS	**over current status** 1'b1: over current occur 1'b0: no over current occur

Bit	7	6	5	4	3	2	1	0
Name								
Type	RO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		RG_ADC_OUT_C0_7_0	**AUXADC channel 0 output data**

Bit	7	6	5	4	3	2	1	0
Name								
Type	RO						RO	
Reset	0						0	0

Bit(s)	Mnemonic	Name	Description
7		RG_ADC_RDY_C0	**AUXADC channel 0 output data ready** 0: AUXADC data proceeding

Bit(s)	Mnemonic	Name	Description
			1: AUXADC data ready
1:0		RG_ADC_OUT_C0_9_8	**AUXADC channel 0 output data**

Bit	7	6	5	4	3	2	1	0
Name								
Type	RO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		RG_ADC_OUT_C1_7_0	**AUXADC channel 1 output data**

Bit	7	6	5	4	3	2	1	0
Name								
Type	RO						RO	
Reset	0						0	0

Bit(s)	Mnemonic	Name	Description
			AUXADC channel 1 output data ready
7		RG_ADC_RDY_C1	0: AUXADC data proceeding 1: AUXADC data ready
1:0		RG_ADC_OUT_C1_9_8	**AUXADC channel 1 output data**

Bit	7	6	5	4	3	2	1	0
Name								
Type	RO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		RG_ADC_OUT_C2_7_0	**AUXADC channel 2 output data**

Bit	7	6	5	4	3	2	1	0
Name								
Type	RO						RO	
Reset	0						0	0

Bit(s)	Mnemonic	Name	Description
7		RG_ADC_RDY_C2	**AUXADC channel 2 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
1:0		RG_ADC_OUT_C2_9_8	**AUXADC channel 2 output data**

Bit	7	6	5	4	3	2	1	0
Name								
Type	RO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		RG_ADC_OUT_C3_7_0	**AUXADC channel 3 output data**

Bit	7	6	5	4	3	2	1	0
Name								
Type	RO						RO	
Reset	0						0	0

Bit(s)	Mnemonic	Name	Description
7		RG_ADC_RDY_C3	**AUXADC channel 3 output data ready** 0: AUXADC data proceeding 1: AUXADC data ready
1:0		RG_ADC_OUT_C3_9_8	**AUXADC channel 3 output data**

Bit	7	6	5	4	3	2	1	0
Name								
Type	RO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		RG_ADC_OUT_WAKEUP_7_0	**AUXADC wakeup output data**

Bit	7	6	5	4	3	2	1	0
Name								
Type	RO						RO	
Reset	0						0	0

Bit(s)	Mnemonic	Name	Description
7		RG_ADC_RDY_WAKEUP	**AUXADC wakeup output data ready** 0: AUXADC wakeup data not ready 1: AUXADC wakeup data ready
1:0		RG_ADC_OUT_WAKEUP_9_8	**AUXADC wakeup output data**

Bit	7	6	5	4	3	2	1	0
Name								
Type	RO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		RG_ADC_OUT_TRIM_7_0	**AUXADC trimming output data**

Bit	7	6	5	4	3	2	1	0
Name								
Type	RO						RO	

Reset	0						0	0

Bit(s)	Mnemonic	Name	Description
7		RG_ADC_RDY_TRIM	**AUXADC trimming output data ready** 0: AUXADC trimming data proceeding 1: AUXADC trimming data ready
1:0		RG_ADC_OUT_TRIM_9_8	**AUXADC trimming output data**

Bit	7	6	5	4	3	2	1	0
Name								
Type	RW							RW
Reset	0	0	0	0				0

Bit(s)	Mnemonic	Name	Description
7:4		RG_AUXADC_CHSEL	**AUXADC channel selection** 4'h0: VBAT 4'h1: VISENSE 4'h2: VCHARGER 4'h3: TBAT 4'h4~4'h15: Reserved
0		RG_AUXADC_START	**AUXADC start trigger, write 1 trigger, auto clear to 0** 0: AUXADC not start trigger 1: AUXADC start trigger

Address	Name	Width	Register Function
22	FLASH_CON0	8	**FLASH Control Register 0**
23	FLASH_CON1	8	**FLASH Control Register 1**
24	FLASH_CON2	8	**FLASH Control Register 2**
26	FLASH_CON4	8	**FLASH Control Register 4**
27	KPLED_CON0	8	**KPLED Control Register 0**
28	KPLED_CON1	8	**KPLED Control Register 1**
29	KPLED_CON2	8	**KPLED Control Register 2**
2A	KPLED_CON3	8	**KPLED Control Register 3**
2B	KPLED_CON4	8	**KPLED Control Register 4**

2C	ISINKS_CON0	8	ISINKS Control Register 0
2D	ISINKS_CON1	8	ISINKS Control Register 1
2E	ISINKS_CON2	8	ISINKS Control Register 2
2F	ISINKS_CON3	8	ISINKS Control Register 3
30	ISINKS_CON4	8	ISINKS Control Register 4
31	ISINKS_CON5	8	ISINKS Control Register 5
32	ISINKS_CON6	8	ISINKS Control Register 6
33	ISINKS_CON7	8	ISINKS Control Register 7
34	ISINKS_CON8	8	ISINKS Control Register 8
35	ISINKS_CON9	8	ISINKS Control Register 9
36	ISINKS_CON10	8	ISINKS Control Register 10
37	ISINKS_CON11	8	ISINKS Control Register 11
38	ISINKS_CON12	8	ISINKS Control Register 12
39	ISINKS_CON13	8	ISINKS Control Register 13
3F	BOOST_CON0	8	BOOST Control Register 0
40	BOOST_CON1	8	BOOST Control Register 1
46	SPK_CON0	8	Speaker Control Register 0
47	SPK_CON1	8	Speaker Control Register 1
4C	SPK_CON6	8	Speaker Control Register 6
4D	SPK_CON7	8	Speaker Control Register 7
5A	SPK_CON20	8	Speaker Control Register 20
5F	ASW_CON0	8	ASW Control Register 0
6B	FGADC_CON2	8	FGADC Control Register 2
6C	FGADC_CON3	8	FGADC Control Register 3
6D	FGADC_CON4	8	FGADC Control Register 4
6E	FGADC_CON5	8	FGADC Control Register 5
6F	FGADC_CON6	8	FGADC Control Register 6
70	FGADC_CON7	8	FGADC Control Register 7
71	FGADC_CON8	8	FGADC Control Register 8
72	FGADC_CON9	8	FGADC Control Register 9
73	FGADC_CON10	8	FGADC Control Register 10
78	FGADC_CON15	8	FGADC Control Register 15
79	FGADC_CON16	8	FGADC Control Register 16

Bit	7	6	5	4	3	2	1	0
Name								
Type				RW				
Reset				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		FLASH_DIM_DUTY	**Flash ON-duty of dimming control** 0: 1/32

Bit(s)	Mnemonic	Name	Description
			1: 2/32 2: 3/32 N: N+1/32 31: 32/32

Bit	7	6	5	4	3	2	1	0
Name								
Type							RW	RW
Reset							0	0

Bit(s)	Mnemonic	Name	Description
1		FLASH_THER_SHDN_EN	**Flash thermal shut down enable** 0: Disable 1: Enable
0		FLASH_EN	**Turn on Flash driver** 0: Disable 1: Enable

Bit	7	6	5	4	3	2	1	0
Name								
Type	RW							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		FLASH_DIM_DIV	**Flash dimming frequency division** 0: /1 1: /2 2: /3 N: /N+1 255: 256

Bit	7	6	5	4	3	2	1	0
Name								
Type	RW		RW					RW
Reset	0		0	0				0

Bit(s)	Mnemonic	Name	Description
7		FLASH_SFSTREN	**Flash soft-start enable** 0: Disable

Bit(s)	Mnemonic	Name	Description
			1: Enable
5:4		FLASH_SFSTR	**Flash soft-start time** 00: 30.52us 01: 61.04us 10: 91.55us 11: 122.07us
0		FLASH_MODE	**Flash enable mode select** 0: PWM mode 1: Register mode (FLASH_EN)

Bit	7	6	5	4	3	2	1	0
Name								
Type				RW				
Reset				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		KPLED_DIM_DUTY	**Kpled ON-duty of dimming control** 0: 1/32 1: 2/32 2: 3/32 N: N+1/32 31: 32/32

Bit	7	6	5	4	3	2	1	0
Name								
Type							RW	RW
Reset							0	0

Bit(s)	Mnemonic	Name	Description
1		KPLED_THER_SHDN_EN	**Kpled thermal shut down enable** 0: Disable 1: Enable
0		KPLED_EN	**Turn on kpled** 0: Disable 1: Enable

Bit	7	6	5	4	3	2	1	0
Name								
Type	RW							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		KPLED_DIM_DIV	**Kpled dimming frequency division** 0: /1 1: /2 2: /3 N: /N+1 255: 256

Bit	7	6	5	4	3	2	1	0
Name								
Type						RW		
Reset						0	0	0

Bit(s)	Mnemonic	Name	Description
2:0		KPLED_SEL	**Kpled driving step select**

Bit	7	6	5	4	3	2	1	0
Name								
Type	RW		RW					RW
Reset	0		0	0				0

Bit(s)	Mnemonic	Name	Description
7		KPLED_SFSTREN	**Kpled soft-start enable** 0: Disable 1: Enable
5:4		KPLED_SFSTR	**Kpled soft-start time** 00: 30.52us 01: 61.04us 10: 91.55us 11: 122.07us
0		KPLED_MODE	**Kpled enable mode select** 0: PWM mode 1: Register mode (KPLED_EN)

Bit	7	6	5	4	3	2	1	0
Name								
Type					RW			
Reset					0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0		ISINK_DIM0_DUTY	**ISINK ON-duty of dimming0 control** 0: 1/16 1: 2/16 2: 3/16 N: N+1/16 15: 16/16

Bit	7	6	5	4	3	2	1	0
Name								
Type				RW				
Reset				0	1	0	1	1

Bit(s)	Mnemonic	Name	Description
4:0		ISINK_DIM0_FSEL	**ISINK dimming0 frequency selection** 0: 31.25KHz 1: 29.762KHz 2: 28.409KHz 3: 27.174KHz 4: 26.042KHz 5: 25KHz 6: 24.038KHz 7: 23.148KHz 8: 22.321KHz 9: 21.552KHz 10: 20.833KHz 11: 20.161KHz 12: 19.531KHz 13: 1KHz 14: 901Hz 15: 800Hz 16: 700Hz 17: 600Hz 18: 500Hz 19: 400Hz 20: 300Hz 21: 200Hz 22: 100Hz Others: Reserved

Bit	7	6	5	4	3	2	1	0
Name								
Type				RW				
Reset				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		ISINK_DIM1_DUTY	**ISINK ON-duty of dimming1 control** 0: 1/32 1: 2/32 2: 3/32 N: N+1/32 31: 32/32

Bit	7	6	5	4	3	2	1	0
Name								
Type				RW				
Reset				0	1	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		ISINK_DIM1_FSEL	**ISINK dimming1 frequency selection** ISINK_DIM1_CKSEL[1: 0]=00/01/10/11 0: 1008Hz/504Hz/252Hz/126Hz 1: 893Hz/446Hz/223Hz/112Hz 2: 801Hz/400Hz/200Hz/100Hz 3: 694Hz/347Hz/174Hz/87Hz 4: 601Hz/300Hz/150Hz/75Hz 5: 496Hz/248Hz/124Hz/62Hz 6: 401Hz/200Hz/100Hz/50Hz 7: 300Hz/150Hz/75Hz/37.5Hz 8: 200Hz/100Hz/50Hz/25Hz 9: 100Hz/50Hz/25Hz/12.5Hz 10: 90Hz/45Hz/22.5Hz/11.3Hz 11: 80Hz/40Hz/20Hz/10Hz 12: 70Hz/35Hz/17.5Hz/8.75Hz 13: 60Hz/30Hz/15Hz/7.5Hz 14: 50Hz/25Hz/12.5Hz/6.25Hz 15: 40Hz/20Hz/10Hz/5Hz 16: 30Hz/15Hz/7.5Hz/3.75Hz 17: 20Hz/10Hz/5Hz/2.5Hz 18: 10Hz/5Hz/2.5Hz/1.25Hz 19: 9Hz/4.5Hz/2.25Hz/1.125Hz 20: 8Hz/4Hz/2Hz/1Hz 21: 7Hz/3.5Hz/1.75Hz/0.875Hz 22: 6Hz/3Hz/1.5Hz/0.75Hz 23: 5Hz/2.5Hz/1.25Hz/0.625Hz 24: 4Hz/2Hz/1Hz/0.5Hz 25: 3Hz/1.5Hz/0.75Hz/0.375Hz 26: 2Hz/1Hz/0.5Hz/0.25Hz 27: 1.5Hz/0.75Hz/0.375Hz/0.188Hz 28: 1Hz/0.5Hz/0.25Hz/0.125Hz 29: 0.8Hz/0.4Hz/0.2Hz/0.1Hz 30: 0.6Hz/0.3Hz/0.15Hz/0.075Hz 31: 0.5Hz/0.25Hz/0.125Hz/0.0625Hz

Bit	7	6	5	4	3	2	1	0
Name								
Type				RW				
Reset				0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		ISINK_DIM2_DUTY	**ISINK ON-duty of dimming2 control** 0: 1/32 1: 2/32 2: 3/32 N: N+1/32

Bit(s)	Mnemonic	Name	Description
			31: 32/32

Bit	7	6	5	4	3	2	1	0
Name								
Type				RW				
Reset				0	1	0	0	0

Bit(s)	Mnemonic	Name	Description
4:0		ISINK_DIM2_FSEL	**ISINK dimming2 frequency selection** ISINK_DIM2_CKSEL[1:0]=00/01/10/11 0: 1008Hz/504Hz/252Hz/126Hz 1: 893Hz/446Hz/223Hz/112Hz 2: 801Hz/400Hz/200Hz/100Hz 3: 694Hz/347Hz/174Hz/87Hz 4: 601Hz/300Hz/150Hz/75Hz 5: 496Hz/248Hz/124Hz/62Hz 6: 401Hz/200Hz/100Hz/50Hz 7: 300Hz/150Hz/75Hz/37.5Hz 8: 200Hz/100Hz/50Hz/25Hz 9: 100Hz/50Hz/25Hz/12.5Hz 10: 90Hz/45Hz/22.5Hz/11.3Hz 11: 80Hz/40Hz/20Hz/10Hz 12: 70Hz/35Hz/17.5Hz/8.75Hz 13: 60Hz/30Hz/15Hz/7.5Hz 14: 50Hz/25Hz/12.5Hz/6.25Hz 15: 40Hz/20Hz/10Hz/5Hz 16: 30Hz/15Hz/7.5Hz/3.75Hz 17: 20Hz/10Hz/5Hz/2.5Hz 18: 10Hz/5Hz/2.5Hz/1.25Hz 19: 9Hz/4.5Hz/2.25Hz/1.125Hz 20: 8Hz/4Hz/2Hz/1Hz 21: 7Hz/3.5Hz/1.75Hz/0.875Hz 22: 6Hz/3Hz/1.5Hz/0.75Hz 23: 5Hz/2.5Hz/1.25Hz/0.625Hz 24: 4Hz/2Hz/1Hz/0.5Hz 25: 3Hz/1.5Hz/0.75Hz/0.375Hz 26: 2Hz/1Hz/0.5Hz/0.25Hz 27: 1.5Hz/0.75Hz/0.375Hz/0.188Hz 28: 1Hz/0.5Hz/0.25Hz/0.125Hz 29: 0.8Hz/0.4Hz/0.2Hz/0.1Hz 30: 0.6Hz/0.3Hz/0.15Hz/0.075Hz 31: 0.5Hz/0.25Hz/0.125Hz/0.0625Hz

Bit	7	6	5	4	3	2	1	0
Name								
Type			RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5		ISINKS_CH5_EN	**Turn on ISINK Channel 5**

Bit(s)	Mnemonic	Name	Description
4		ISINKS_CH4_EN	**Turn on ISINK Channel 4**
3		ISINKS_CH3_EN	**Turn on ISINK Channel 3**
2		ISINKS_CH2_EN	**Turn on ISINK Channel 2**
1		ISINKS_CH1_EN	**Turn on ISINK Channel 1**
0		ISINKS_CH0_EN	**Turn on ISINK Channel 0**

Bit	7	6	5	4	3	2	1	0
Name								
Type			RW	RW	RW	RW	RW	RW
Reset			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description	
5		ISINKS_CH5_CABC_EN	**ISINK Channel 5 CABC enable** 0: 1: Enable	Disable
4		ISINKS_CH4_CABC_EN	**ISINK Channel 4 CABC enable** 0: 1: Enable	Disable
3		ISINKS_CH3_CABC_EN	**ISINK Channel 3 CABC enable** 0: 1: Enable	Disable
2		ISINKS_CH2_CABC_EN	**ISINK Channel 2 CABC enable** 0: 1: Enable	Disable
1		ISINKS_CH1_CABC_EN	**ISINK Channel 1 CABC enable** 0: 1: Enable	Disable
0		ISINKS_CH0_CABC_EN	**ISINK Channel 0 CABC enable** 0: 1: Enable	Disable

Bit	7	6	5	4	3	2	1	0
Name								
Type		RW					RW	
Reset		0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
6:4		ISINKS_CH0_STEP	**Coarse 6 step current level for ISINK CH0**

Bit(s)	Mnemonic	Name	Description
			000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA
1:0		ISINKS_CH0_MODE	**ISINK Channel 0 enable mode select** 00: PWM0 mode 01: PWM1 mode 10: PWM2 mode 11: Register mode (ISINKS_CH0_EN)

Bit	7	6	5	4	3	2	1	0
Name								
Type		RW					RW	
Reset		0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
			Coarse 6 step current level for ISINK CH1 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA
6:4		ISINKS_CH1_STEP	
1:0		ISINKS_CH1_MODE	**ISINK Channel 1 enable mode select** 00: PWM0 mode 01: PWM1 mode 10: PWM2 mode 11: Register mode (ISINKS_CH1_EN)

Bit	7	6	5	4	3	2	1	0
Name								
Type		RW					RW	
Reset		0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
			Coarse 6 step current level for ISINK CH2 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA
6:4		ISINKS_CH2_STEP	

Bit(s)	Mnemonic	Name	Description
1:0		ISINKS_CH2_MODE	**ISINK Channel 2 enable mode select** 00: PWM0 mode 01: PWM1 mode 10: PWM2 mode 11: Register mode (ISINKS_CH2_EN)

Bit	7	6	5	4	3	2	1	0
Name								
Type		RW					RW	
Reset		0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
6:4		ISINKS_CH3_STEP	**Coarse 6 step current level for ISINK CH3** 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA
1:0		ISINKS_CH3_MODE	**ISINK Channel 3 enable mode select** 00: PWM0 mode 01: PWM1 mode 10: PWM2 mode 11: Register mode (ISINKS_CH3_EN)

Bit	7	6	5	4	3	2	1	0
Name								
Type		RW					RW	
Reset		0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
6:4		ISINKS_CH4_STEP	**Coarse 6 step current level for ISINK CH4** 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA
1:0		ISINKS_CH4_MODE	**ISINK Channel 4 enable mode select** 00: PWM0 mode 01: PWM1 mode 10: PWM2 mode 11: Register mode (ISINKS_CH4_EN)

Bit	7	6	5	4	3	2	1	0
Name								
Type		RW					RW	
Reset		0	0	0			0	0

Bit(s)	Mnemonic	Name	Description
6:4		ISINKS_CH5_STEP	**Coarse 6 step current level for ISINK CH5** 000: 4mA 001: 8mA 010: 12mA 011: 16mA 100: 20mA 101: 24mA 110: 24mA 111: 24mA
1:0		ISINKS_CH5_MODE	**ISINK Channel 5 enable mode select** 00: PWM0 mode 01: PWM1 mode 10: PWM2 mode 11: Register mode (ISINKS_CH5_EN)

Bit	7	6	5	4	3	2	1	0
Name								
Type	RW		RW			RW		RW
Reset	0		0	0		0		0

Bit(s)	Mnemonic	Name	Description
7		BOOST_ISINK_HW_SEL	**select BOOST mode or ISINK** 0: ISINK mode 1: BOOST mode
5:4		BOOST_MODE	**Boost mode** 00: PWM0 mode 01: PWM1 mode 10: PWM2 mode 11: Register mode (BOOST_EN)
2		BOOST_CABC_EN	**CABC mode enable. PWM is from BL_PWM.** 0: Disable 1: Enable
0		BOOST_EN	**Boost backlight enable signal** 0: Disable 1: Enable

Bit	7	6	5	4	3	2	1	0

Name								
Type	RW				RW			
Reset	0	0			0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:6		BOOST_SR_NMOS	**Slew-Rate control (NMOS)** 00: driving x2 01: driving x1 10: driving x4 11: driving x3
3:0		BOOST_VRSEL	**select regulated voltage or current** 4'b0000: ILED=25mV*1/R 4'b0001: ILED=25mV*2/R 4'b0010: ILED=25mV*3/R 4'b0011: ILED=25mV*4/R 4'b0100: ILED=25mV*5/R 4'b0101: ILED=25mV*6/R 4'b0110: ILED=25mV*7/R 4'b0111: ILED=25mV*8/R 4'b1000: ILED=25mV*9/R 4'b1001: ILED=25mV*10/R 4'b1010: ILED=25mV*11/R 4'b1011: ILED=25mV*12/R 4'b1100: ILED=25mV*13/R 4'b1101: ILED=25mV*14/R 4'b1110: ILED=25mV*15/R 4'b1111: ILED=25mV*16/R

Bit	7	6	5	4	3	2	1	0
Name								
Type		RW				RW		RW
Reset		0				0		0

Bit(s)	Mnemonic	Name	Description
6		SPK_THER_SHDN_L_EN	**Speaker L-ch thermal shut down enable** 0: Disable 1: Enable
2		SPKMODE_L	**speaker L-ch driver mode select** 0: class D mode 1: class AB mode
0		SPK_EN_L	**speaker amp. L-ch enable** 0: disable 1: enable

Bit	7	6	5	4	3	2	1	0

Name								
Type						RW		
Reset						0	1	1

Bit(s)	Mnemonic	Name	Description
2:0		SPK_VOL_L	**speaker L-ch volume control** 000: 3dB 001: 6dB 010: 9dB 011: 12dB 100: 15dB 101: 18dB 110: 21dB 111: mute

Bit	7	6	5	4	3	2	1	0
Name								
Type		RW				RW		RW
Reset		0				0		0

Bit(s)	Mnemonic	Name	Description
6		SPK_THER_SHDN_R_EN	**Speaker R-ch thermal shut down enable** 0: Disable 1: Enable
2		SPKMODE_R	**speaker R-ch driver mode select** 0: class D mode 1: class AB mode
0		SPK_EN_R	**speaker amp. R-ch enable** 0: disable 1: enable

Bit	7	6	5	4	3	2	1	0
Name								
Type						RW		
Reset						0	1	1

Bit(s)	Mnemonic	Name	Description
2:0		SPK_VOL_R	**speaker R-ch volume control** 000: 3dB 001: 6dB 010: 9dB 011: 12dB 100: 15dB 101: 18dB

Bit(s)	Mnemonic	Name	Description
			110: 111: mute 21dB

Bit	7	6	5	4	3	2	1	0
Name								
Type			RW	RW				
Reset			0	0				

Bit(s)	Mnemonic	Name	Description
5		SPKMODE_L_SW	**speaker L-ch driver mode select** 0: class D mode 1: class AB mode
4		SPKMODE_R_SW	**speaker R-ch driver mode select** 0: class D mode 1: class AB mode

Bit	7	6	5	4	3	2	1	0
Name								
Type								RW
Reset								0

Bit(s)	Mnemonic	Name	Description
0		RG_ANA_SW_SEL	**Analog SW channel selection** 0: Channel 2 1: Channel 1

Bit	7	6	5	4	3	2	1	0
Name								
Type					RO			
Reset					0	0	0	0

Bit(s)	Mnemonic	Name	Description
3:0		FG_CAR_35_32	**Current charge value[35:32]**

Bit	7	6	5	4	3	2	1	0
Name								
Type	RO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		FG_CAR_31_24	**Current charge value[31:24]**

Bit	7	6	5	4	3	2	1	0
Name								
Type	RO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		FG_CAR_23_16	**Current charge value[23:16]**

Bit	7	6	5	4	3	2	1	0
Name								
Type	RO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		FG_CAR_15_08	**Current charge value[15:8]**

Bit	7	6	5	4	3	2	1	0
Name								
Type	RO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		FG_CAR_07_00	**Current charge value[7:0]**

Bit	7	6	5	4	3	2	1	0
Name								
Type			RO					
Reset			0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
5:0		FG_NTER_29_24	**Current charge time value[29:24]**

Bit	7	6	5	4	3	2	1	0
Name								
Type	RO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		FG_NTER_23_16	**Current charge time value[23:16]**

Bit	7	6	5	4	3	2	1	0
Name								
Type	RO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		FG_NTER_15_08	**Current charge time value[15:8]**

Bit	7	6	5	4	3	2	1	0
Name								
Type	RO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		FG_NTER_07_00	**Current charge time value[7:0]**

Bit	7	6	5	4	3	2	1	0
Name								
Type	RO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		FG_CURRENT_OUT_15_08	**Current output charge of first stage[15:8]**

Bit	7	6	5	4	3	2	1	0
Name								
Type	RO							
Reset	0	0	0	0	0	0	0	0

Bit(s)	Mnemonic	Name	Description
7:0		FG_CURRENT_OUT_07_00	**Current output charge of first stage[7:0]**

The following schematic illustrates a typical application for PMIC to connect with the MT6575 baseband chips.

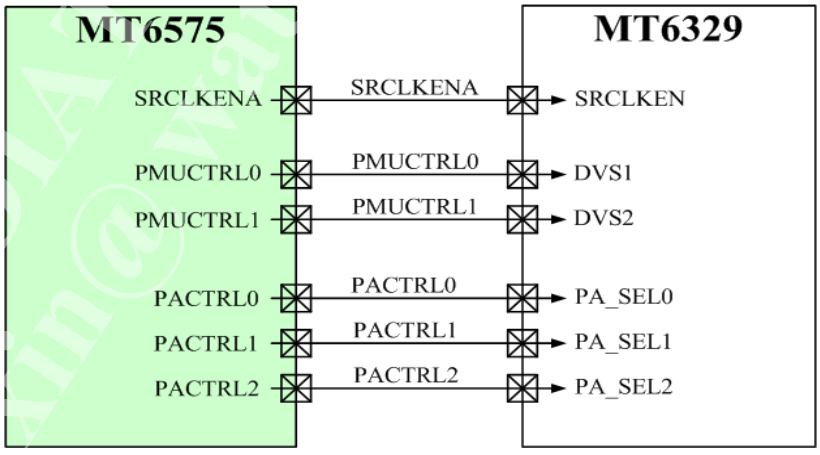


Figure 14: Connection to BB

The following schematic illustrates the hardware external shut-down function for MT6329 to power down when the main chip software crashes.

- Short press PWRKEY or HOMEKEY
  - INT-> EINT -> software control
  - Power-down, sleep mode or the other functions
- Long press shut-down
  - Force power-off of PMU
  - 5/8/11/14s with 50% accuracy
  - External reset function with source from:
    - PWRKEY and HOMEKEY both pressed for long period of time
    - PWERKEY pressed for long period of time
    - HOMEKEY pressed for long period of time
      - Software disables watchdog counter

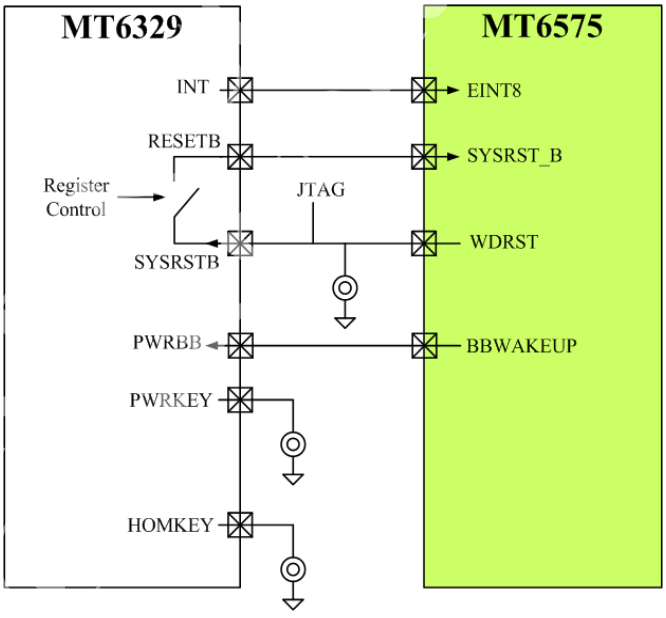


Figure 15: Hardware external shut-down function

The figure below shows MT6329 VRF18 buck converter that implements the LDO mode.

- VRF18 provides the LDO mode for lower-cost requirements.

  - VRF18 (Buck/LDO: 250/250mA)
- Buck mode: VRF18_FB connects to the output capacitor.
- LDO mode: VRF18_FB connects to VBAT.

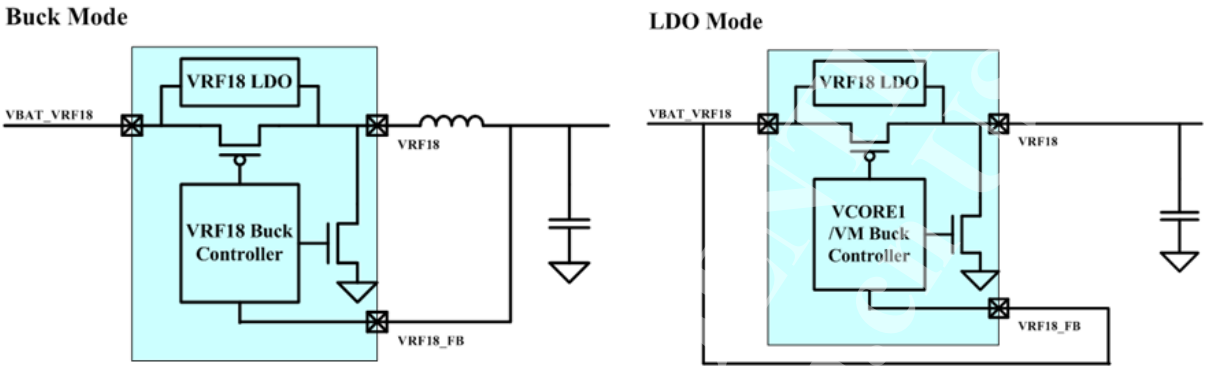


Figure 16: DC/DC and LDO mode HW setting application note

The figure below shows MT6329 VPA and VRF18 buck converter un-use configuration.

- For VPA not use configuration
  - VBAT_PA connect to VBAT; GND_PA connect to GND
  - VPA & VPA_FB: floating
  - RG_VPA_EN=0 & RG_VPA_NDIS_EN=1
- For VRF18 not use configuration
  - VBAT_RF18 connect to VBAT; GND_RF18 connect to GND
  - VRF18 & VRF18_FB: floating
  - RG_VRF18_EN=0 & RG_VRF18_NDIS=1

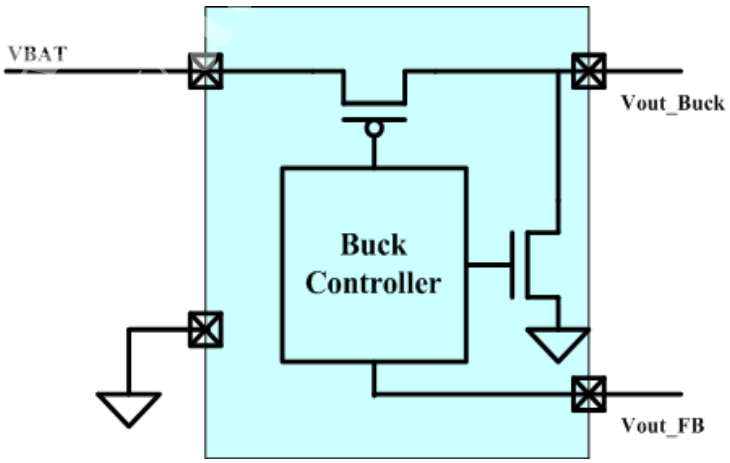
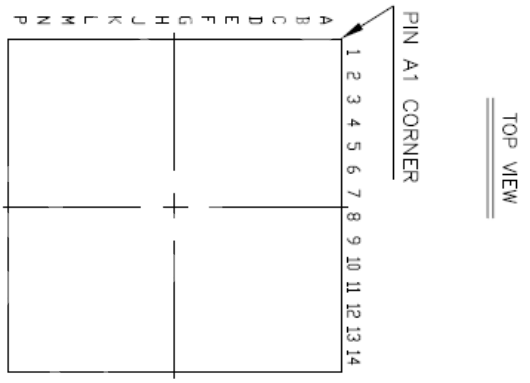
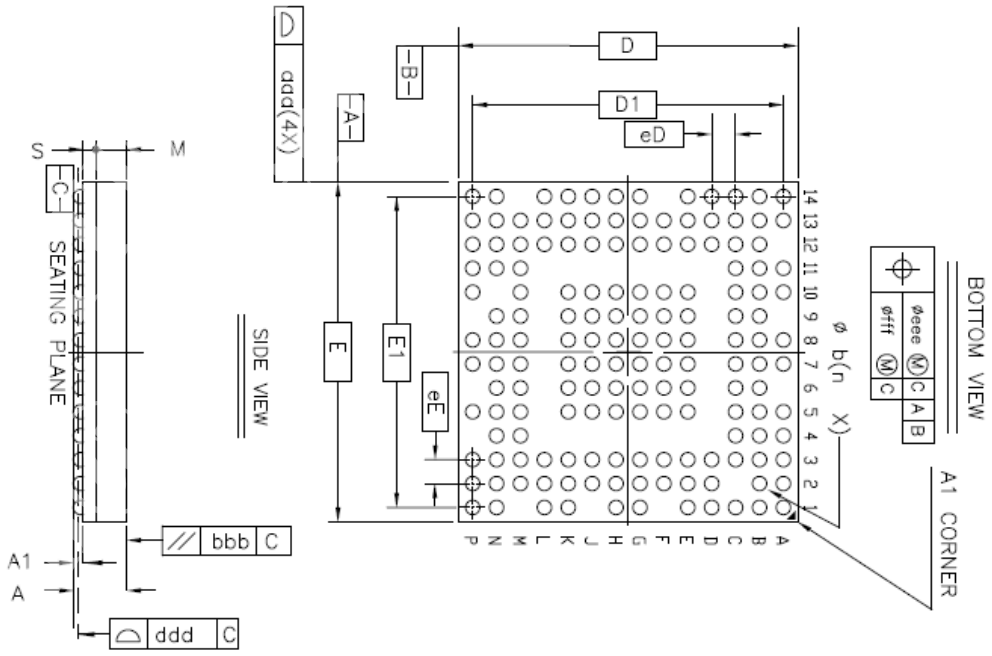


Figure 17: DC/DC un-useconfiguration

Package :		Symbol	Common Dimensions
Body Size:	X	E	7.100
	Y	D	7.100
Ball Pitch :	X	eE	0.500
	Y	eD	0.500
Total Thickness :		A	1.200 MAX.
Mold Thickness :		M	0.650 Ref.
Substrate Thickness :		S	0.260 Ref.
Ball Diameter :			0.300
Stand Off :		A1	0.160 ~ 0.260
Ball Width :		b	0.250 ~ 0.350
Package Edge Tolerance :		aaa	0.100
Mold Flatness :		bbb	0.100
Coplanarity:		ddd	0.080
Ball Offset (Package) :		eee	0.150
Ball Offset (Ball) :		fff	0.050
Ball Count :		n	155
Edge Ball Center to Center :	X	E1	6.500
	Y	D1	6.500





N/A