MT6628T Data Sheet

Version: 1.2
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Document Revision History

Revision	Date	Author	Description
1.0	2012/05/10	Lingbin Guo	First release
1.1	2012/06/05	Lingbin Guo	Update WiFi standard name
1.2	2012/08/13	Lingbin Guo	1. add power-domain 2. update PMU information 3. update RF measurement 4. add ordering guide 5. fix Figure 12 (SPDT -> Balun + BPF)

Table of Contents

1 System Overview

1.1 General Description

MT6628T is a 3-in-1 wireless communication device which includes

- WLAN
- Bluetooth
- FM Receiver

With four advanced radio technologies integrated into one single chip, MT6628T provides the best and most convenient connectivity solution among the industry. MT6628T implements advanced and sophisticated Radio Coexistence algorithms and hardware mechanisms. It also supports single 2.4 GHz antenna sharing between Bluetooth and WLAN. The enhanced overall quality is achieved for simultaneous voice, data, and audio/video transmission on mobile phones and Media Tablets. The small footprint of WLCSP package with low-power consumption greatly reduces PCB layout resource. The software package “Symphony” enables all advanced wireless features on Android OS.

1.2 Features

- Embedded single core 32-bit RISC CPU for better system level management between sub-systems
- Supports single antenna for Bluetooth and WLAN
- Self calibration
- Single crystal for BT and WLAN
- Integrated switching regulator enables direct connection to battery
- Best-in-class current consumption performance
- OS support: Android and Windows Mobile
- Intelligent BT/WLAN coexistence scheme that goes beyond PTA signaling (for example, transmit window and duration that take into account of protocol exchange sequence, frequency, etc.)
- Single antenna support for WLAN/Bluetooth
- WLCSP (3.99x4.45mm^2) package

WLAN

- Single-band (2.4GHz) single stream 802.11 b/g/n MAC/BB/RF
- 802.11 d/h/k compliant
- Security: WFA WPA/WPA2 personal, WPS2.0, WAPI (Hardware)
- QoS: WFA WMM, WMM PS
- Supports 802.11n optional features: STBC, A-MPDU, Blk-Ack, RIFS, MCS Feedback, 20/40MHz coexistence (PCO), unscheduled PSMP
- Supports 802.11w Protected Managed Frames
- Supports WiFi Direct (WFA P-2-P standard) and Wi-Fi Miracast (Wi-Fi Display)
- Supports HotSpot 2.0 Passpoint

- Interface: SDIO 2.0 (4-bit & 1-bit, up to 50MHz), SPI (48Mbps)
- Integrated PA with max 21dBm output power
- Typical -77.5 dBm 2.4GHz receiver sensitivity at 11g 54Mbps mode
- Per packet TX power control

Bluetooth

- Bluetooth specification v2.1+EDR
- Bluetooth specification 3.0+HS compliance
- Bluetooth v4.0 Low Energy (LE)
- Integrated PA with 10dBm (class 1) transmit power and Balun
- Rx sensitivity: GFSK -95dBm, DQPSK -94dBm, 8-DPSK -88dBm
- HCI over high speed (4Mbps) UART(H4), and SDIO 2.0
- Best-in-class BT/Wi-Fi coexistence performance
- Up to 4 piconets simultaneously with background inquiry/page scan
- Supports Scatternet
- Packet loss concealment (PLC) function for better voice quality
- Low-power scan function to reduce the power consumption in scan modes

FM

- 76-108MHz with 50kHz step
- Supports RDS/RBDS
- Digital stereo modulator/demodulator
- Digital audio interface (I2S)
- Fast seek time 30ms/channel
- Stereo noise reduction
- Audio sensitivity 2dBμVemf ((S+N)/N=26dB)
- Audio S/N 60dB
- Anti-jamming
- Integrated short antenna

1.3 Applications

- Smart phone applications
- Media Tablet applications
- Mobile Internet Device (MID) applications
- Portable Navigation Device (PND) applications
- Portable Media Player (PMP) applications
- Portable gaming devices

1.4 Block Diagram

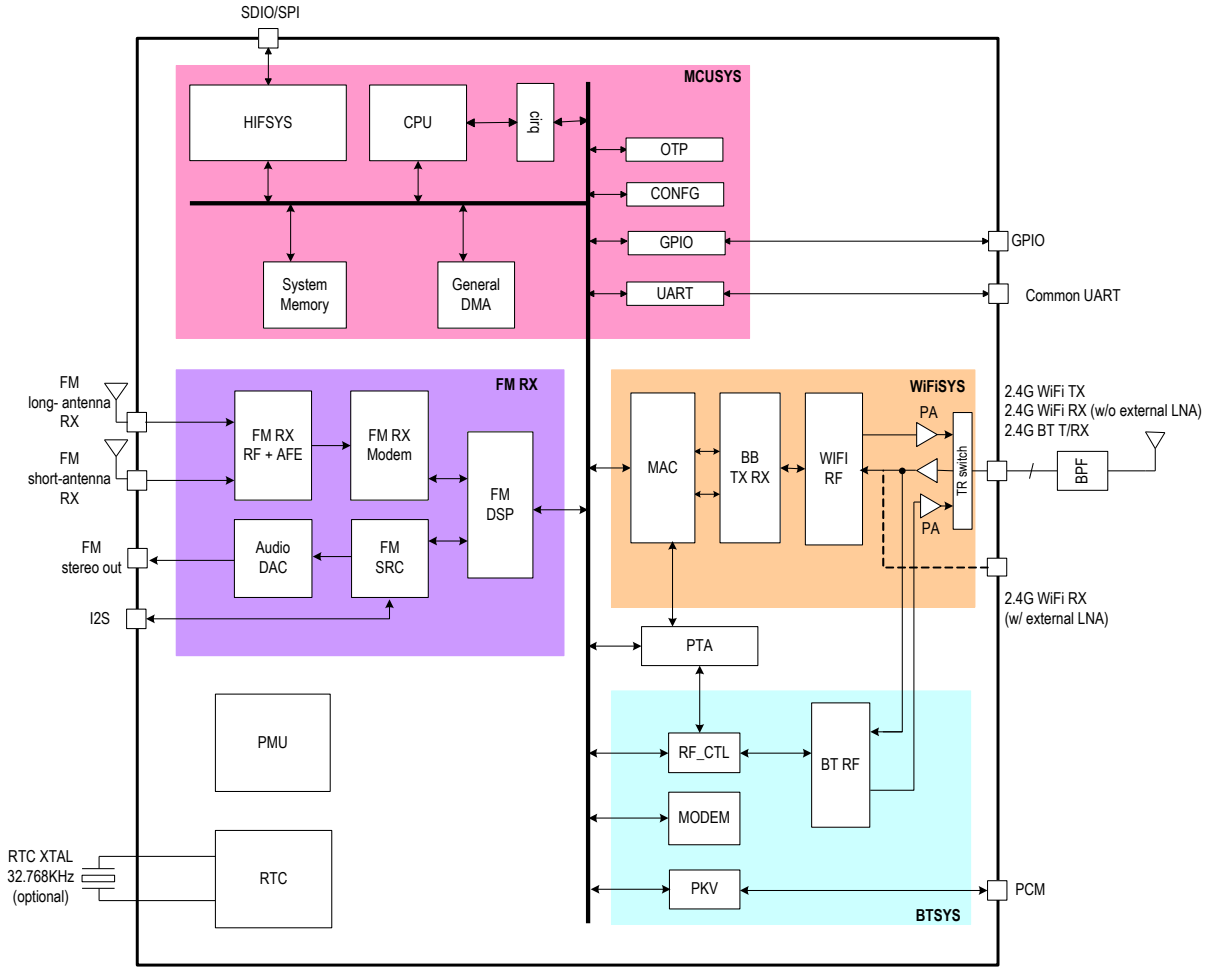

Figure 1. MT6628T block diagram

2 Product Description

2.1 Pin Description

There are total 88 pins in WLCSP package.

Symbol	WLCSP bump	Power domain	Description	PU/PD	I/O
			Power ground pin		
DVDD	G5		1.2V core power	NA	VDD
DVDD	E6		1.2V core power	NA	VDD
DVDD	C9		1.2V core power	NA	VDD
DVSS	G6		Ground	NA	VSS
DVSS	F7		Ground	NA	VSS
DVSS1	C10		Ground	NA	VSS
DVDDIO	C8		I/O power	NA	VDD
DVDDIO_SDIO	H4		SDIO I/O power	NA	VDD
			PMU		
PMU_EN	G3		PMU enable	NA	I
PMU_DSB	H3		Disable PMU deep sleep mode	NA	I
VREF	L1		Reference bandgap voltage	NA	Analog/O
AVDD55_MISC	L2		VBAT for internal circuit	NA	VDD
AVSS55_MISC	K1		MISC ground	NA	VSS
AVDD25_V2P5	G2		Internal 2.5V power	NA	VDD
AVDD25_V2P5NA	J3		Internal 2.5V power	NA	VDD
LXBK	L3		Switching node of buck	NA	O
AVDD55_SMPS	K3		Battery voltage	NA	VDD
AVSS55_SMPS	J4		Switching regulator ground	NA	VSS
AVDD17_CLDO_IN	J2		1.7V CLDO input	NA	VDD
AVDD28_TLDO_SW	H1		Power source for TCXO	NA	O
CLDO	K2		1.2V core power LDO output	NA	O
AVDD28_TLDO	J1		2.85V TCXO LDO output	NA	O
WFLDO	L4		3.3V WiFi LDO output	NA	O

Symbol	WLCSP bump	Power domain	Description	PU/PD	I/O
AUX_REF	H2		ADC top reference voltage input	NA	I
AVDD28_PLL	L5		2.8V PLL power	NA	VDD
AVSS28_PLL	K5		2.8V PLL ground	NA	VSS
			RTC		
RTCCLK	F10	VCCRTC	RTC 32kHz clock input	NA	Analog/I
RTCCLK_O	E10	VCCRTC	RTC 32kHz clock output	NA	Analog/O
VCCRTC	G9		RTC power	NA	VDD
AVSSRTC	G7		RTC ground	NA	VSS
			Analog		
NC	A6		Reserved	NA	NA
NC	B6		Reserved	NA	NA
NC	C6		Reserved	NA	NA
NC	A7		Reserved	NA	NA
NC	C7		Reserved	NA	NA
SANT_P	J10		Short antenna FM RF input	NA	RF/I
SALNA_IN_N_VSS	H10		Short antenna FM RF input	NA	RF/I
LNA_IN_N_VSS	K10		Long antenna FM RF input	NA	RF/I
LANT_P	L10		Long antenna FM RF input	NA	RF/I
AUROUT	K8		FM audio output	NA	Analog/O
AULOUT	L8		FM audio output	NA	Analog/O
AVDD28_FM	H9		FM power	NA	VDD
AVSS28_FM	J8		Ground	NA	VSS
AVSS28_FM	J9		Ground	NA	VSS
RF_IOP_WBT	A1		WiFi/BT RF port	NA	RF I/O
RF_ION_WBT	B1		WiFi/BT RF port	NA	RF I/O
LNA_IN_EXT	D1		External LNA input	NA	RF/I
AVDD33_TX_WBT	A3		WiFi/BT power	NA	VDD
AVDD16_TRX_WBT	D2		WiFi/BT power	NA	VDD
AVDD16_SX_WBT	D4		WiFi/BT power	NA	VDD
AVDD16_LF_WBT	E1		WiFi/BT power	NA	VDD
AVSS33_PA	A2		Ground	NA	VSS
AVSS33_PA	B2		Ground	NA	VSS

Symbol	WLCSP bump	Power domain	Description	PU/PD	I/O
AVSS16_WBT	B3		Ground	NA	VSS
AVSS16_WBT	C2		Ground	NA	VSS
AVSS16_LF_WBT	E2		Ground	NA	VSS
VCO_MON_WBT	C3		WiFi/BT RF monitor pin	NA	Analog/O
OSC_IN	A4		XTAL input	NA	Analog/I
AVDD28_OSC	A5		XTAL power	NA	VDD
AVSS28_OSC	B5		Ground	NA	VSS
FSOURCE_WR	G8		eFuse power pin	NA	VDD
		Digital			
XTEST	B8	DVDDIO	Test mode enable	PU	I
SYSRST_B	L7	DVDDIO	External system reset active low	PU	I
ANTSEL2	F3	Internal LDO 2.8V	ANTSEL_2: Antenna select no.2	PD/SW	O
			GPIO24: GPIO24 in/out		I/O
			Strap pin		I
ANTSEL1	F4	Internal LDO 2.8V	ANTSEL_1: Antenna select no.1	PD/SW	O
			GPIO23: GPIO23 in/out		I/O
			Strap pin		I
ANTSEL0	F2	Internal LDO 2.8V	ANTSEL_0: Antenna select no.0	PD/SW	O
			GPIO22: GPIO22 in/out		I/O
RF_I_CAL	F1	DVDDIO	EXT_INT_N: External interrupt input from Host	PU/SW	I
			AUXADC_IN: Analog pin		I
			RF_I_CAL: Analog pin		I
			GPIO21: GPIO21 in/out		I/O
OSC_EN	G4	Internal LDO 2.8V	OSC_EN: OSC enable in clock daisy chain	NA/SW	O
			GPIO20: GPIO20 in/out		I/O
SDIO_CLK	H7	DVDDIO_SDIO	SDIO_CLK: SDIO interface	NA/SW	I

Symbol	WLCSP bump	Power domain	Description	PU/PD	I/O
			HIF_SPI_CLK: SPI serial clock		I
			GPIO19: GPIO19 in/out		I/O
SDIO_CMD	J7	DVDDIO_SDIO	SD_CMD: SDIO interface	NA/SW	I/O
			HIF_SPI_CS: SPI chip select		I
			GPIO18: GPIO18 in/out		I/O
SDIO_DAT3	J6	DVDDIO_SDIO	SDIO_DAT3: SDIO interface	NA/SW	I/O
			HIF_SPI_DOUT: SPI data output		O
			GPIO17: GPIO17 in/out		I/O
SDIO_DAT2	H5	DVDDIO_SDIO	SDIO_DAT2: SDIO interface	NA/SW	I/O
			HIF_SPI_DIN: SPI data input		I
			GPIO16: GPIO16 in/out		I/O
SDIO_DAT1	J5	DVDDIO_SDIO	SDIO_DAT1: SDIO interface	NA/SW	I/O
			HIF_SPI_MODE_SEL: SPI mode select		I
			GPIO15: GPIO15 in/out		I/O
SDIO_DAT0	H6	DVDDIO_SDIO	SDIO_DAT0: SDIO interface	NA/SW	I/O
			HIF_SPI_INT_B: SPI interrupt		O
			GPIO14: GPIO14 in/out		I/O
UART_RXD	F9	DVDDIO	UART_RXD: UART RX data	PU/SW	I
			GPIO13: GPIO13 in/out		I/O
UART_TXD	E8	DVDDIO	UART_TXD: UART TX data	PU/SW	O
			GPIO12: GPIO12 in/out		I/O
UART_RTS	D9	DVDDIO	UART_RTS: UART flow control	PU/SW	

Symbol	WLCSP bump	Power domain	Description	PU/PD	I/O
			GPIO11: GPIO11 in/out		I/O
			Strap pin		I
UART_CTS	E9	DVDDIO	UART_CTS: UART flow control	PU/SW	
			GPIO10: GPIO10 in/out		I/O
PCM_CLK	A10	DVDDIO	PCM_CLK: PCM interface clock	PD/SW	I/O
			I2S_CLK: FM I2S interface clock		I/O
			DAI_CLK: digital audio interface clock		I
			GPIO9: GPIO9 in/out		I/O
PCM_SYNC	D10	DVDDIO	PCM_SYNC: PCM interface sync	PD/SW	I/O
			I2S_WS: FM I2S interface WS		I/O
			DAI_SYNC: digital audio interface sync		I
			GPIO8: GPIO8 in/out		I/O
PCM_OUT	B10	DVDDIO	PCM_OUT: PCM interface output data	PD/SW	O
			I2S_DATA_OUT: I2S interface output data		O
			DAI_TX: digital audio interface TX data		O
			GPIO7: GPIO7 in/out		I/O
PCM_IN	A9	DVDDIO	PCM_IN: PCM interface input data	PD/SW	I
			I2S_DATA_OUT: I2S interface output data		O
			DAI_RX: digital audio interface RX data		I
			GPIO6: GPIO6 in/out		I/O
GPIO5	B9	DVDDIO	GPIO5: GPIO5in/out	PD/SW	I/O
I2S_CLK	F8	DVDDIO	I2S_CLK: FM I2S interface clock	PD/SW	I/O
			PCM2CLK: PCM2 interface clock		I/O
			GPIO4: GPIO4 in/out		I/O
I2S_WS	E7	DVDDIO	I2S_WS: FM I2S word select	PD/SW	I/O

Symbol	WLCSP bump	Power domain	Description	PU/PD	I/O
			PCM2SYNC: PCM2 interface sync		I/O
			GPIO3: GPIO3 in/out		I/O
I2S_DATA_OUT	D7	DVDDIO	I2S_DATA_OUT: FM I2S data output	PD/SW	O
			PCM2OUT: PCM2 synchronous data output		O
			GPIO2: GPIO2 in/out		I/O
WIFI_INT_B	H8	DVDDIO	WIFI_INT_B: WLAN host interrupt	PU/SW	O
			GPIO1: GPIO1 in/out		I/O
BGF_INT_B	K7	DVDDIO	ALL_INT_B: All interrupt to host	PU/SW	O
			BGF_INT_B: BT & FM host interrupt		O
			GPIO0: GPIO0 in/out		I/O

Table 1. Pin descriptions

2.1.1 Strapping Table

ANTSEL1	Description
0	TCXO
1	Xtal

Table 2. Clock source selection

ANTSEL2	Description
0	SDIO
1	SPI

Table 3. WLAN host interface selection

UART_RTS	Description
0	UART
1	SDIO

Table 4. Common interface selection

2.2 Package Information

2.2.1 WLCSP Packaging

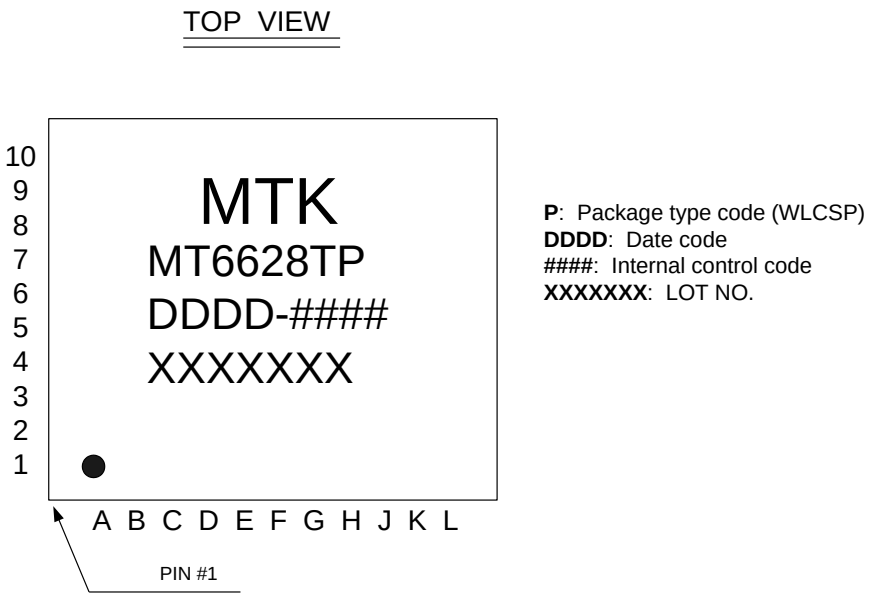

Figure 2. MT6628T WLCSP top marking

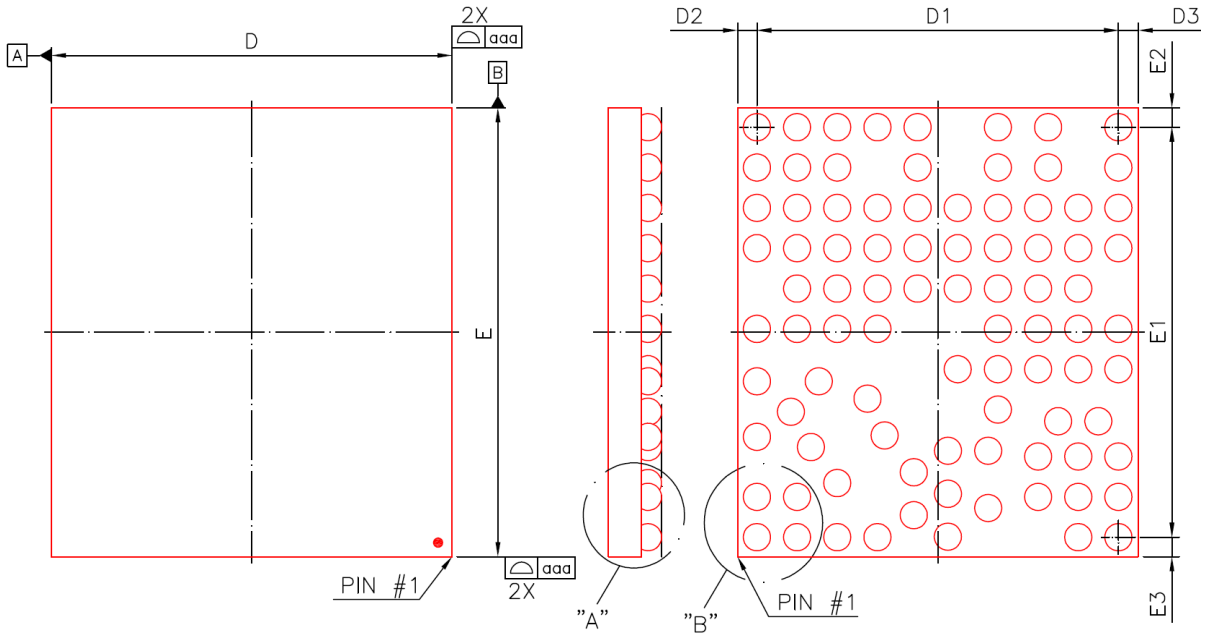

Figure 3. MT6628T WLCSP POD (a)

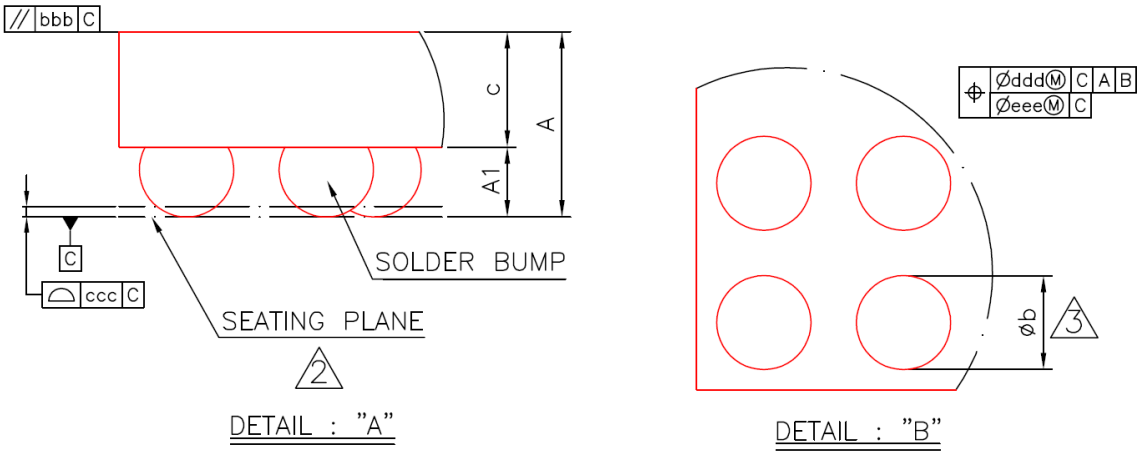

Figure 4. MT6628T WLCSP POD (b)

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.490	0.530	0.570	0.019	0.021	0.022
A1	0.170	0.200	0.230	0.007	0.008	0.009
c	0.305	0.330	0.355	0.012	0.013	0.014
D	3.936	3.991	4.016	0.155	0.157	0.158
E	4.397	4.452	4.477	0.173	0.175	0.176
D1	---	3.600	---	---	0.142	---
D2	---	0.193	---	---	0.008	---
D3	---	0.198	---	---	0.008	---
E1	---	4.066	---	---	0.160	---
E2	---	0.193	---	---	0.008	---
E3	---	0.193	---	---	0.008	---
b	0.240	0.270	0.300	0.009	0.011	0.012
aaa	+0.025 −0.055			+0.001 −0.002		
bbb	0.10			0.004		
ccc	0.03			0.001		
ddd	0.15			0.006		
eee	0.05			0.002		

Figure 5. MT6628T WLCSP POD (c)

Bump coordinates:

TOP VIEW

BUMP	LOCATION X(mm)	LOCATION Y(mm)	BUMP	LOCATION X(mm)	LOCATION Y(mm)
A1	−1.802	2.033	A6	0.099	2.028
B1	−1.802	1.633	B6	0.100	1.603
D1	−1.802	1.038	C6	0.100	1.176
E1	−1.802	0.488	E6	0.198	0.367
F1	−1.802	−0.033	G6	0.198	−0.433
H1	−1.802	−0.833	H6	0.198	−0.833
J1	−1.802	−1.233	J6	0.198	−1.233
K1	−1.802	−1.633	A7	0.500	1.745
L1	−1.802	−2.033	C7	0.500	1.176
A2	−1.402	2.033	D7	0.598	0.767
B2	−1.402	1.633	E7	0.598	0.367
C2	−1.264	1.140	F7	0.598	−0.033
D2	−1.464	0.789	G7	0.598	−0.433
E2	−1.186	0.488	H7	0.598	−0.833
F2	−1.402	−0.033	J7	0.598	−1.233
G2	−1.402	−0.433	K7	0.598	−1.633
H2	−1.402	−0.833	L7	0.598	−2.033
J2	−1.402	−1.233	B8	0.998	1.633
K2	−1.402	−1.633	C8	0.998	1.233
L2	−1.402	−2.033	E8	0.998	0.367
A3	−1.002	2.033	F8	0.998	−0.033
B3	−1.002	1.496	G8	0.998	−0.433
C3	−0.701	0.659	H8	0.998	−0.833
F3	−1.002	−0.033	J8	0.998	−1.233
G3	−1.002	−0.433	K8	1.098	−1.633
H3	−1.002	−0.833	L8	1.098	−2.033
J3	−1.002	−1.233	A9	1.398	2.033
K3	−1.002	−1.633	B9	1.398	1.633
L3	−1.002	−2.033	C9	1.398	1.233
A4	−0.602	2.033	D9	1.198	0.883
D4	−0.530	1.024	E9	1.398	0.367
F4	−0.602	−0.033	F9	1.398	−0.033
G4	−0.602	−0.433	G9	1.398	−0.433
H4	−0.602	−0.833	H9	1.398	−0.833
J4	−0.602	−1.233	J9	1.398	−1.233
L4	−0.602	−2.033	A10	1.798	2.033
A5	−0.240	1.815	B10	1.798	1.633
B5	−0.240	1.390	C10	1.798	1.233
G5	−0.202	−0.433	D10	1.598	0.883
H5	−0.202	−0.833	E10	1.798	0.367
J5	−0.202	−1.233	F10	1.798	−0.033
K5	−0.202	−1.633	H10	1.798	−0.833
L5	−0.202	−2.033	J10	1.798	−1.233
			K10	1.798	−1.633
			L10	1.798	−2.033

2.3 Ordering guide

Model	Temperature Range	Package	Shipping Medium
AD6546BCPZ	-20˚C to +85˚C	LFCSP-40	Tray
AD6546BCPZ-REEL			Tape & Reel

3 Electrical Characteristics

3.1 PMU Description

The power management unit (PMU) contains Under-Voltage Lockout (UVLO) circuit, Low Dropout Regulators (LDOs), LDO switch (TLDO_SW), buck converter and reference band-gap circuit.

The PMU integrates three LDOs and one buck converter. Those circuits are optimized for the given functions by balancing quiescent current, dropout voltage, line/load regulation, ripple rejection and output noise.

The input voltage of the buck converter ranges from 2.5V to 4.4V. Its output voltage is 1.7V and feeds into the input power of the RF circuit and input power of CLDO (core LDO) which has 1.2V output voltage for all digital circuits.

There is only one PA LDO for WLAN with output voltage of 3.3V. There is also one dedicated LDO which provides 2.85V output voltage for RF blocks, ANTSEL IO power and TCXO via TLDO switch (TLDO_SW).

3.1.1 Under-Voltage Lockout (UVLO)

The UVLO state in the PMU prevents startup if the initial voltage of the main battery is below 2.15V threshold. It ensures that MT6628T is powered on with the battery in good condition. The UVLO function is performed by a hysteretic comparator which ensures smooth power-on sequence. In addition, when the battery voltage is getting lower, it will enter the UVLO state, and the PMU will be turned off by itself to prevent further discharging.

3.1.2 WF_PA_LDO

WF_PA_LDO converts the battery input to a 3.3V supply for using WiFi RF PA circuits. It is optimized for high-performance and adequate quiescent current.

3.1.3 CLDO

One CLDO is integrated in the PMU to supply digital core. It converts voltage from1.7V input to 1.2V output which suits the digital circuits. The input is typically connected to the buck's output.

3.1.4 Buck Converter

The regulator is a DC-DC step-down converter (buck converter) to source 300mA (max.) with 2.0V to 1.7V programmable output voltage based on the software register setting. It supplies power for the RF

circuitry and CLDO. The buck converter is optimized for high-efficiency, low-EMI, and low quiescent current.

3.1.5 PMU Power Connection

Two power connection methods are suggested. One is for normal mode, and the other is for low-power mode. In the normal mode, the voltage source for RF and digital core LDO is from the DC-DC converter. The voltage source of PA and TCXO/XTAL LDOs is from VBAT directly. The 1.8V or 2.8V IO voltages are from the host side. The connection structure is shown in the figure below.

In the system sleep mode, PA LDO and TCXO/XTAL LDO are turned off. The voltage source of the digital core LDO is switched to IO voltage instead of the DC-DC converter, which is also turned off.

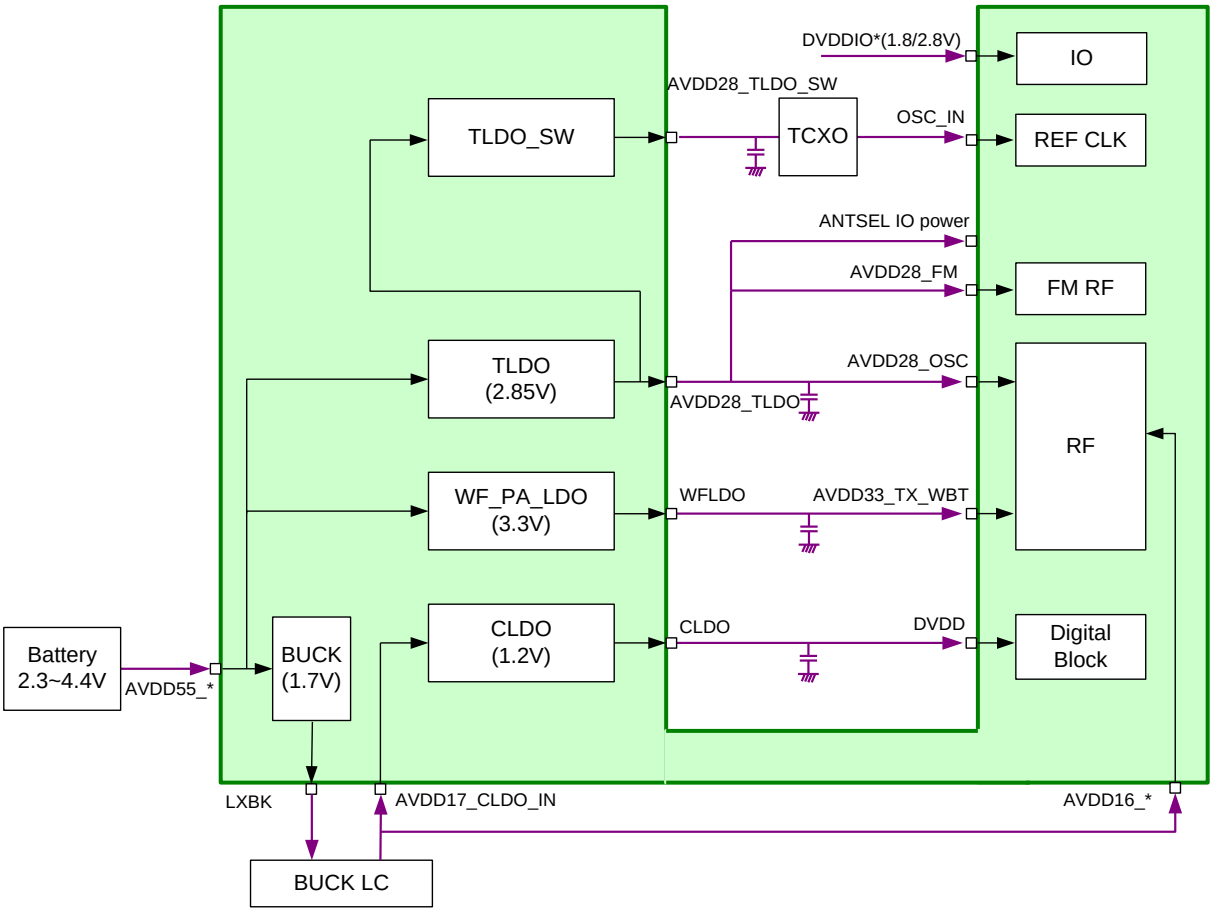

Figure 6. Normal mode power connection

Note that due to legacy naming, AVDD16_* is actually operated in 1.7V.

3.2 Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
DVDDIO	1.8V/2.8V digital IO power supply	-0.3 to 3.6	V
DVDDIO_SDIO	1.8V or 2.8V SDIO digital IO power supply	-0.3 to 3.6	V
DVDD	Digital 1.2V power supply	-0.3 to 1.32	V
VCCRTC	RTC power supply	-0.3 to 3.6	V
CLDO	Internal core LDO power supply	-0.3 to 3.6	V
TLDO WFLDO	Internal LDO power supply	-0.3 to 4.4	V
TLDO_SW	TLDO switch for TCXO	-0.3 to 3.6	V
AVDD28_* AVDD33_*	RF power supply	-0.3 to 3.6	V
AVDD16_*	RF power supply	-0.3 to 1.8	V
AVDD55_SMPS	BUCK power supply	-0.3 to 4.4	V
AVDD55_MISC	Power-on circuit supply	-0.3 to 4.4	V
T_{STG}	Storage temperature	-60 to +150	°C
T_A	Operating temperature	-40 to +85	°C

Table 5. Absolute maximum ratings

3.3 Recommended Operating Range

Symbol	Parameter	Min.	Typ.	Max.	Unit
DVDDIO DVDDIO_SDIO	2.8V digital power supply	2.0	2.8	3.3	V
	1.8V digital power supply	1.6	1.8	2.0	V
DVDD	Digital core power supply	1.08	1.2	1.32	V
VCCRTC	RTC power supply	2.52	2.8	3.08	V
		1.62	1.8	1.98	V
AVDD16_*	RF power supply	1.6	1.7	1.8	V
AVDD28_*	RF power supply	2.66	2.8	2.94	V
AVDD33_*	RF power supply	3.14	3.3	3.46	V
AVDD55_SMPS	BUCK power supply	2.5	3.8	4.4	V
AVDD55_MISC	Power-on circuit supply	2.3	3.8	4.4	V
T_j	Commercial junction operating temperature	0	25	115	°C
	Industry junction operating temperature	-40	25	125	°C
T_a	Operation temperature	-40	25	85	°C
T_{stg}	Storage temperature	-60	25	150	°C

Table 6. Recommended operating range

3.4 PMU Electrical Characteristics

3.4.1 PMU Characteristics

Parameter	Conditions	Min.	Typ.	Max.	Unit
PMU_EN = 0: Shut down current					
2.3V < VBAT < 4.3V	VBAT = 3.8V		20	25	µA
4.3V < VBAT	VBAT = 4.4V		25	35	µA
Under Voltage Lock-Out (UVLO)					
Under voltage rising threshold			2.25		V
Under voltage falling threshold			2.15		V
PMU_EN Voltage Level					
High voltage		1.4			V
Low voltage				1	V
Thermal Shutdown					
Threshold			150		°C
Hysteresis			40		°C
LDO Enable Response Time			250		µs

Parameter	Conditions	Min.	Typ.	Max.	Unit
SMPS Voltage					
Input voltage		2.5	3.8	4.4	V
Output voltage (OUT_BK)		1.6	1.7	1.8	V
Output current (Imax)				300	mA
Quiescent current			40		uA
Line regulation	@150mA		0.5		%
Load regulation				30	mV
PWM mode switching frequency			1.7		MHz
PWM mode ripple voltage	Static load		20		mV
Burst mode ripple voltage	Static load		40		mV
PFM/PWM mode switching condition	VBAT = 3.8V		50		mA
Efficiency (PWM)			84		%
Efficiency (PFM)			82		%
Digital Core Voltage					

Parameter	Conditions	Min.	Typ.	Max.	Unit
Input voltage		1.6	1.7	1.8	V
Output voltage (V_CLDO)		1.1	1.2	1.3	V
Output current (Imax)				200	mA
Quiescent current			15		uA
Drop-out voltage	0.5*Imax		250		mV
	1*Imax		350		mV
Start-up time				450	us
Line regulation				12	mV
Load regulation	1mA ~ Imax (full-load)			12	mV
External output capacitor			1		uF
WLAN PA Voltage					
Input voltage		2.3	3.8	4.4	V
Output voltage (VWIFI_PALDO)		2.3	3.3	3.465	V
Output current (Imax)				300	mA
Quiescent current			67		uA
Line regulation				33	mV
Load regulation	1mA ~ Imax (full-load)			33	mV
Output noise voltage	f = 10Hz to 80kHz		60		uVrms
PSRR	At 1kHz	60			dB
	At 30kHz	40			dB
Drop-out voltage	0.5*Imax		250		mV
	1*Imax		350		mV
Start-up time				320	us
External output capacitor			3.2(2.2+1)		uF
TLDO Voltage					
Input voltage		2.3	3.8	4.4	V
Output voltage (VTLDO)		2.71	2.85	2.99	V
Output current (Imax)				100	mA
Quiescent current			42		uA
Line regulation				1	%
Load regulation	1mA ~ Imax (full-load)			1	%
Output noise voltage	f = 10Hz to 80kHz		60		uVrms

Parameter	Conditions	Min.	Typ.	Max.	Unit
PSRR	At 1kHz	60			dB
	At 30kHz	40			dB
Drop-out voltage	0.5*Imax		250		mV
	1*Imax		350		mV
Start-up time				320	us
External output capacitor			1		uF
TLDO switch					
Input voltage			2.85		V
Output voltage (TLDO_SW)		2.66			V
Output current (Imax)				10	mA
External output capacitor			1		uF

Table 7. PMU characteristics

3.4.2 PMU Summary List

Item	LDO/Switcher	Voltage	Current	Description
1	DVDDIO18	1.6V/1.8V/2.0V	400mA	Digital 1.8V IO
2	SMPS	1.7V	300mA	Buck output
3	VCORE	1.2V	200mA	Digtial CORE
4	WFLDO	3.3V	300mA	WLAN PA LDO
5	TLDO	2.85V	100mA	TCXO LDO
6	TLDO_SW	2.8V	10mA	TCXO SW

Table 8. PMU summary list

Note: All the characteristic values are guaranteed at room temperature (25°C).

3.5 XOSC32

3.5.1 Block Description

The low-power 32-kHz crystal oscillator, XOSC32, is designed to work with an external piezoelectric 32.768 kHz crystal and a load composed of two functional capacitors, as shown in the figure below.

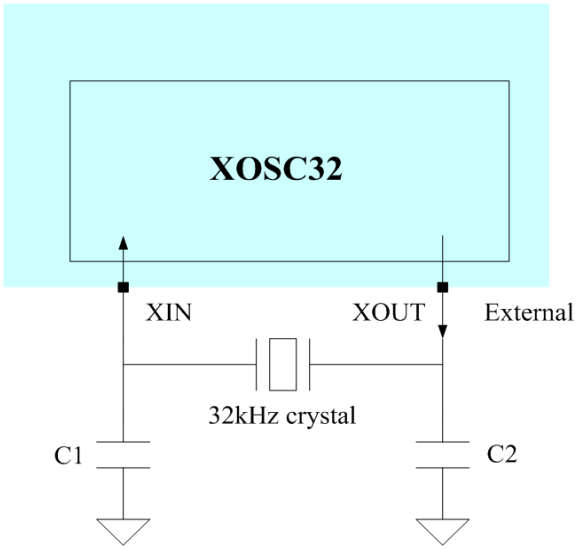

Figure 7. Block diagram of XOSC32

3.5.2 Functional Specifications of XOSC32

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCRTC	Analog power supply	1	2.8	3	V
Tosc	Start-up time			1	sec
Dcyc	Duty cycle		50		%
	Current consumption		5		μA

Table 9. Functional specifications of XOSC32

3.5.3 Recommendations for Crystal Parameters for XOSC32

Symbol	Parameter	Min.	Typ.	Max.	Unit
F	Frequency range		32768		Hz
GL	Drive level			5	uW
Δf/f	Frequency tolerance		+/- 20		ppm
ESR	Series resistance			50	KΩ
C0	Static capacitance			1.6	pF
CL[1]	Load capacitance	6		12.5	pF

Table 10. Recommended parameters of the 32 kHz crystal

[1] CL is the parallel combination of C1 and C2 in the block diagram.

3.6 DC Electrical Characteristics for 2.8 Volts Operation

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{IL}	Input low voltage	LVTTL	-0.28	0.6	V
V_{IH}	Input high voltage		2.0	3.08	V
V_{T-}	Schmitt trigger negative going threshold voltage	LVTTL	0.68	1.36	V
V_{T+}	Schmitt trigger positive going threshold voltage		1.36	1.7	V
V_{OL}	Output low voltage	$\|I_{OL}\|$ = 1.6~14mA	-0.28	0.4	V
V_{OH}	Output high voltage	$\|I_{OH}\|$ = 1.6~14mA	2.4	VDD28 + 0.28	V
R_{PU}	Input pull-up resistance	PU=high, PD=low	40	190	KΩ
R_{PD}	Input pull-down resistance	PU=low, PD=high	40	190	KΩ

Table 11. Pin descriptions

3.7 DC Electrical Characteristics for 1.8 Volts Operation

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{IL}	Input lower voltage	LVTTL	-0.18	0.4	V
V_{IH}	Input high voltage		1.5	1.98	V
V_{T-}	Schmitt trigger negative going threshold voltage	LVTTL	0.44	0.88	V
V_{T+}	Schmitt trigger Positive going threshold voltage		0.88	1.1	V
V_{OL}	Output low voltage	$\|I_{OL}\|$ = 1.6~14mA	-0.18	0.4	V
V_{OH}	Output high voltage	$\|I_{OH}\|$ = 1.6~14mA	1.4	VDD18 + 0.18	V
R_{PU}	Input pull-up resistance	PU=high, PD=low	40	190	KΩ
R_{PD}	Input pull-down resistance	PU=low, PD=high	40	190	KΩ

Table 12. Pin descriptions

ESD CAUTION

MT6628T is ESD (electrostatic discharge) sensitive device and may be damaged with ESD or spike voltage. Although MT6628T is with built-in ESD protection circuitry, please handle with care to avoid the permanent malfunction or the performance degradation.