7008CATI_0452_CSE4001_SUDHA | 30 marks | 60 minutes

Instructions

Read the instructions provided for every question properly before attempting the answer.

1. A | **10** marks per question | **1** display questions | **1** maximum answerable

Q1 (72278) Scan and/or Upload | **10** marks | Easy | K1. Remembering | CO1

1. A COVID-19 data collection centre wants to collect the samples faster and enhance the system to run 10 times faster and achieved speedup of 5 times. Compute the fraction that is enhanced. [5M]
2. For executing the pattern sequencing algorithm, two machines A and B are chosen with the same instruction set architecture. Machine A has CPI of 3.0 and clock cycle time of 30ns. Machine B has CPI of 5.0 and clock cycle time of 20ns. Identify the faster machine and compute how many times faster.[5M]

Rubrics

Q2 (72279) Scan and/or Upload | **10** marks | Easy | K1. Remembering | CO1

Discuss the necessity of cache coherence mechanism in shared memory models with the help of an example. Provide a solution for the cache coherence and draw the architecture for cache coherence model along with the explanation.

Rubrics

Q3 (72280) Scan and/or Upload | **10** marks | Easy | K1. Remembering | CO1

“The growth of multi-core architectures is not a necessity”-Provide your analysis on this statement with any two multi-core architectures.

Rubrics

2. B | **10** marks per question | **1** display questions | **1** maximum answerable

Q1 (72281) Scan and/or Upload | **10** marks | Medium | K1. Remembering | CO7

For the following question assume that the pipeline contains 5 stages: IF (Instruction Fetch), ID (Instruction Decode and register read), EX (Execute), MEM (memory), and WB (Write Back). Each stage except EX requires one clock cycle.

System contains 4 functional units for floating point (FP) operations for FP-load / store, FP-addition / subtraction, FP-multiplication and FP-division.
EX-stage for Load / Store operations contains 1 clock cycle (EX); for ADDD or SUBD operations contains 1 clock cycle (A or S); for MULTD operation contains 3 clock cycles (M1, M2, M3), and for DIVD operation contains 4 clock cycles (D1, D2, D3, D4).
To execute the following instructions,
***I1:* LD F5, 40(R4)**
***I2:* LD F1, 48(R4)**
***I3:* MULTD F0,F1,F3**
***I4:* SUBD F7,F5,F2**
***I5:* DIVD F9,F0,F5**
***I6:* ADDD F5,F7,F1**
***I7:* SD F7,60(R4)**

i. Identify and show the kind of dependencies present in the above instruction set. [2M]
ii. Discuss whether the above instructions can be parallelized [2M]
iii. Identify the hazards that will occur during implementation [3M]
iv. Give a solution for the above hazards and discuss whether all the hazards can be eliminated by that solution. Justify with the given instruction set.[3M]

Rubrics

Q2 (72282) Scan and/or Upload | **10** marks | Medium | K1. Remembering | CO7

For the following question assume that the pipeline contains 5 stages: IF (Instruction Fetch), ID (Instruction Decode and register read), EX (Execute), MEM (memory), and WB (Write Back). Each stage except EX requires one clock cycle.

System contains 4 functional units for floating point (FP) operations for FP-load / store, FP-addition / subtraction, FP-multiplication and FP-division.
EX-stage for Load / Store operations contains 1 clock cycle (EX); for ADDD or SUBD operations contains 1 clock cycle (A or S); for MULTD operation contains 3 clock cycles (M1, M2, M3), and for DIVD operation contains 4 clock cycles (D1, D2, D3, D4).
To execute the following instructions,
I1: **LD F7, 40(R6)**
I2: **LD F3, 48(R6)**
I3: **MULTD F2,F3,F5**
I4: **SUBD F9,F7,F4**
I5: **DIVD F11,F2,F7**
I6: **ADDD F7,F9,F3**
I7: **SD F9,60(R4)**

i. Identify and show the kind of dependencies present in the above instruction set. [2M]
ii. Discuss whether the above instructions can be parallelized [2M]
iii. Identify the hazards that will occur during implementation [3M]
iv. Give a solution for the above hazards and discuss whether all the hazards can be eliminated by that solution. Justify with the given instruction set.[3M]

Rubrics

Q3 (72283) Scan and/or Upload **10** marks Medium K1. Remembering CO7

For the following question assume that the pipeline contains 5 stages: IF (Instruction Fetch), ID (Instruction Decode and register read), EX (Execute), MEM (memory), and WB (Write Back). Each stage except EX requires one clock cycle.

System contains 4 functional units for floating point (FP) operations for FP-load / store, FP-addition / subtraction, FP-multiplication and FP-division.
EX-stage for Load / Store operations contains 1 clock cycle (EX); for ADDD or SUBD operations contains 1 clock cycle (A or S); for MULTD operation contains 3 clock cycles (M1, M2, M3), and for DIVD operation contains 4 clock cycles (D1, D2, D3, D4).
To execute the following instructions,
I1: **LD F8, 30(R5)**
I2: **LD F4, 38(R5)**
I3: **MULTD F3,F4,F6**
I4: **SUBD F10,F8,F5**
I5: **DIVD F12,F3,F8**
I6: **ADDD F8,F10,F4**
I7: **SD F10,50(R5)**

i. Identify and show the kind of dependencies present in the above instruction set. [2M]
ii. Discuss whether the above instructions can be parallelized [2M]
iii. Identify the hazards that will occur during implementation [3M]
iv. Give a solution for the above hazards and discuss whether all the hazards can be eliminated by that solution. Justify with the given instruction set.[3M]

Rubrics

3. C **10** marks per question **1** display questions **1** maximum answerable

Q1 (72284) Scan and/or Upload **10** marks Hard K1. Remembering CO3

Using shared memory programming model, write a program to generate the following series in the given range 1 to N.
Series: 1,6,3,8,5,10,7,12,9,14,….
Find sum of all numbers in the series once the series is generated
[Hint: check the relation between numbers]

Rubrics

Q2 (72285) Scan and/or Upload **10** marks Hard K1. Remembering CO3

Using shared memory programming model, write a program to generate the following series in the given range 1 to N.
Series: 1,5,4,9,9,15,16,23,25,33,….
Find sum of all numbers in the series once the series is generated
[Hint: check the relation between numbers]

Rubrics

Q3 (72286) Scan and/or Upload **10** marks Hard K1. Remembering CO3

Using shared memory programming model, write a program to generate the following series in the given range 1 to N.
Series: 1,2,3,6,5,10,7,14,9,18,….
Find sum of all numbers in the series once the series is generated
[Hint: check the relation between numbers]

Rubrics