

Overhead		Memory Accesses	Cycles	Notes	
Fetch		1	2		
Decode			1		
Branch			1		
Addressing Mode					
Direct Register			2		
Indirect Register		1	3		
Auto-increment		1	4		
Auto-decrement		1	4		
Indexed		2	7		
Indirect Addressing		1	1		
Branch to Single or Double Operand			1		
Write Mode					
Direct Register Write			2		
Indirect Write		1	1		
End			1		

Each Instruction deals with some overhead according to its type, the number of its operands and how it needs to access these operands.

Instruction	Overhead	Memory Accesses	Cycles	Memory Accesses + Invariant Overhead	Cycles + Invariant Overhead	Worst Case Memory Accesses	Worst Case Cycles	Average Memory Accesses	Average Cycles	Notes
R0V SRC, DST	Fetch, Decode, Branch, (Source Addressing Mode), (Destination Addressing Mode), Branch to Single or Double Operand, (Write Mode), End	0	2	1	8	8	26	4.875	19	
ADD SRC, DST	Fetch, Decode, Branch, (Source Addressing Mode), (Destination Addressing Mode), Branch to Single or Double Operand, (Write Mode), End	0	3	1	9	8	27	4.875	20	
ADC SRC, DST	Fetch, Decode, Branch, (Source Addressing Mode), (Destination Addressing Mode), Branch to Single or Double Operand, (Write Mode), End	0	3	1	9	8	27	4.875	20	
SUB SRC, DST	Fetch, Decode, Branch, (Source Addressing Mode), (Destination Addressing Mode), Branch to Single or Double Operand, (Write Mode), End	0	3	1	9	8	27	4.875	20	
SBC SRC, DST	Fetch, Decode, Branch, (Source Addressing Mode), (Destination Addressing Mode), Branch to Single or Double Operand, (Write Mode), End	0	3	1	9	8	27	4.875	20	
AND SRC, DST	Fetch, Decode, Branch, (Source Addressing Mode), (Destination Addressing Mode), Branch to Single or Double Operand, (Write Mode), End	0	3	1	9	8	27	4.875	20	
OR SRC, DST	Fetch, Decode, Branch, (Source Addressing Mode), (Destination Addressing Mode), Branch to Single or Double Operand, (Write Mode), End	0	3	1	9	8	27	4.875	20	
XOR SRC, DST	Fetch, Decode, Branch, (Source Addressing Mode), (Destination Addressing Mode), Branch to Single or Double Operand, (Write Mode), End	0	3	1	9	8	27	4.875	20	
CMP SRC, DST	Fetch, Decode, Branch, (Source Addressing Mode), (Destination Addressing Mode), Branch to Single or Double Operand, (Write Mode), End	0	3	1	9	8	27	4.875	20	
INC DST	Fetch, Decode, Branch, (Destination Addressing Mode), Branch to Single or Double Operand, (Write Mode), End	0	2	1	8	5	18	3.375	14.25	
DEC DST	Fetch, Decode, Branch, (Destination Addressing Mode), Branch to Single or Double Operand, (Write Mode), End	0	2	1	8	5	18	3.375	15.25	
CLR DST	Fetch, Decode, Branch, (Destination Addressing Mode), Branch to Single or Double Operand, (Write Mode), End	0	2	1	8	5	18	3.375	15.25	
INW DST	Fetch, Decode, Branch, (Destination Addressing Mode), Branch to Single or Double Operand, (Write Mode), End	0	2	1	8	5	18	3.375	15.25	
LIR DST	Fetch, Decode, Branch, (Destination Addressing Mode), Branch to Single or Double Operand, (Write Mode), End	0	2	1	8	5	18	3.375	15.25	
ROR DST	Fetch, Decode, Branch, (Destination Addressing Mode), Branch to Single or Double Operand, (Write Mode), End	0	2	1	8	5	18	3.375	15.25	
ASR DST	Fetch, Decode, Branch, (Destination Addressing Mode), Branch to Single or Double Operand, (Write Mode), End	0	2	1	8	5	18	3.375	15.25	
LRL DST	Fetch, Decode, Branch, (Destination Addressing Mode), Branch to Single or Double Operand, (Write Mode), End	0	2	1	8	5	18	3.375	15.25	
ROL DST	Fetch, Decode, Branch, (Destination Addressing Mode), Branch to Single or Double Operand, (Write Mode), End	0	2	1	8	5	18	3.375	15.25	
BR Offset	Fetch, Decode, Branch, End	0	6	1	11	1	11	1	11	Add + 3
BEQ Offset	Fetch, Decode, Branch, End	0	6	1	11	1	11	1	11	
BNE Offset	Fetch, Decode, Branch, End	0	6	1	11	1	11	1	11	
BLO Offset	Fetch, Decode, Branch, End	0	6	1	11	1	11	1	11	
BLS Offset	Fetch, Decode, Branch, End	0	6	1	11	1	11	1	11	
BHI Offset	Fetch, Decode, Branch, End	0	6	1	11	1	11	1	11	
BHS Offset	Fetch, Decode, Branch, End	0	6	1	11	1	11	1	11	
HALT	Fetch, Decode, Branch, End	0	1	1	5	1	5	1	5	
RESET	Fetch, Decode, Branch, End	0	2	1	7	1	7	1	7	
NOP	Fetch, Decode, Branch, End	0	1	1	6	1	6	1	6	
JSR Address	Fetch, Decode, Branch, End	2	10	3	15	3	15	3	15	
INTERRUPT	Fetch, Decode, Branch, End	2	10	3	15	3	15	3	15	
RTS	Fetch, Decode, Branch, End	1	4	2	9	2	9	2	9	
JMPT	Fetch, Decode, Branch, End	2	8	3	13	3	13	3	13	