PDP-11 Microprocessor - Team 01

Team Information

Name	Section	Bench Number
Ahmed Nasser	1	8
Ahmed Hesham Eid	1	9
Abdelrahman Ahmed Mohamed Farid	1	34
Youssef Walid	2	34

Workload Distribution

Name	SEC: BN:	Load
Ahmed Nasser	SEC: 1 BN: 8	Assembler PLA Integration
Ahmed Hesham Eid	SEC: 1 BN: 9	Assembler Control Word Decoder Integration
Abdelrahman Farid	SEC: 1 BN: 34	JK-FF MIU (memory interface unit) JSR and interrupt Integration
Youssef Walid	SEC: 2 BN: 34	Basic Components (D-FF, Counter, ALU, RAM, ROM, Tristate Buffer) Control Store Integration

Changes from Phase 1 design

None, we continued on the previous design as planned and everything went smoothly..