AN439
Application note

Snubberless™ and logic level TRIAC behavior at turn-off

Introduction

The use of TRIACs is limited by their switching behavior. Indeed, there is a risk of spurious triggering after conduction if the slope of the decreasing current is too high, and/or if the slope of the reapplied voltage is too high. The designer must then take some precautions: device over-rating, switching aid network (snubber), and junction temperature margin, and so on. This generally involves additional costs.

After a brief discussion of commutation when a TRIAC is turned off, this article will describe the behavior of the logic level and Snubberless TRIACs, which present high commutation capabilities.

Contents

1 TRIAC turn-off description

1.1 Definition

The TRIAC can be compared to two thyristors mounted in back-to-back and coupled with a control area which allows the triggering of this Alternating Current Switch with only one gate (see *Figure 1*).

Looking at the TRIAC silicon structure (see *Figure 2*), it can be noted that the conduction areas, corresponding to these two thyristors, narrowly overlap each other on the control area.

Figure 1. Simplified equivalent schematic of TRIAC circuit

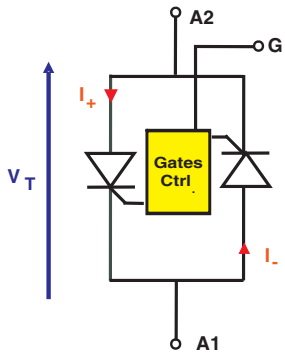
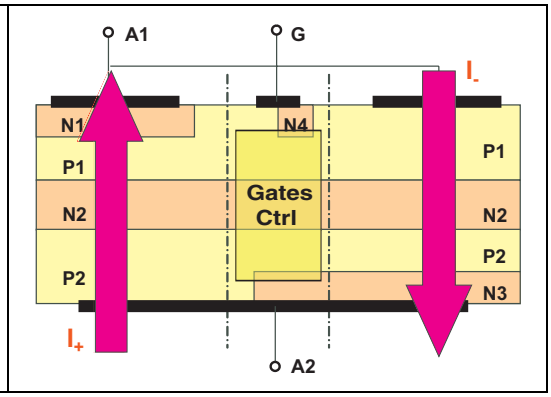


Figure 2. Example of TRIAC silicon structure

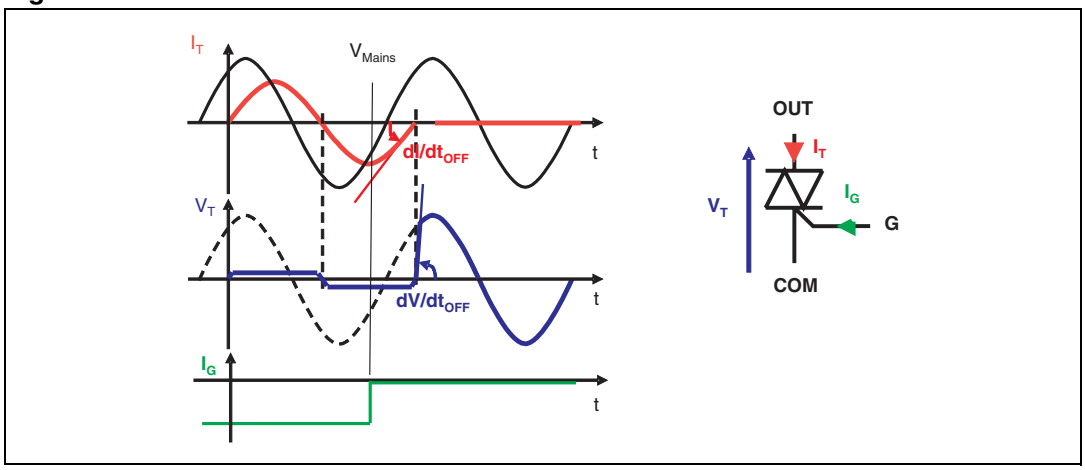


During the conduction time, a certain quantity of charge is injected into the structure. The biggest part of this charge disappears by recombination during the current decrease, while another part is extracted after the turn-off by the reverse recovery current. Nonetheless, an excess charge remains, particularly in the neighboring regions of the gate, which can induce the triggering of the other conduction area when the mains voltage is reapplied across the TRIAC. This is the problem of commutation.

For a given structure at a determined junction temperature, the turn-off behavior depends on:

1. **The quantity of charge which remains when the current drops to zero**. The quantity of the charge is linked to the value of the current which was circulating in the TRIAC approximately 100 µs, about two or three times the minority carriers' life time, before the turn-off. Thus, the parameter to consider is the slope of the decreasing current, called the turn-off dI/dt or dI/dt_{OFF} (see *Figure 3*)
2. **The slope of the reapplied voltage during turn-off**. This parameter is the commutation dV/dt, called the turn-off dV/dt or dV/dt_{OFF} (see *Figure 3*). A capacitive current, proportional to the dV/dt_{OFF}, flows into the structure, and therefore charges are injected and added to those coming from the previous conduction.

Figure 3. dI/dt and dV/dt at turn-off



1.2 (dI/dt)c versus (dV/dt)c characterization

To characterize the turn-off TRIAC behavior, we consider a circuit in which the slope of the decreasing current can be adjusted. In addition, the slope of the reapplied voltage can be controlled by using, a circuit of resistors and capacitors connected across the TRIAC. For a determined dV/dt_{OFF} ((dV/dt)c), we progressively increase the dI/dt_{OFF} until a certain level which induces the spontaneous triggering of the TRIAC. This is the critical dI/dt_{OFF}, called the (dI/dt)c in TRIAC datasheets. This is also the way to trace the curve of the TRIAC commutation behavior (see TRIAC datasheet curve “Relative variation of critical rate of decrease of main current (dI/dt)c versus reapplied (dV/dt)c”).

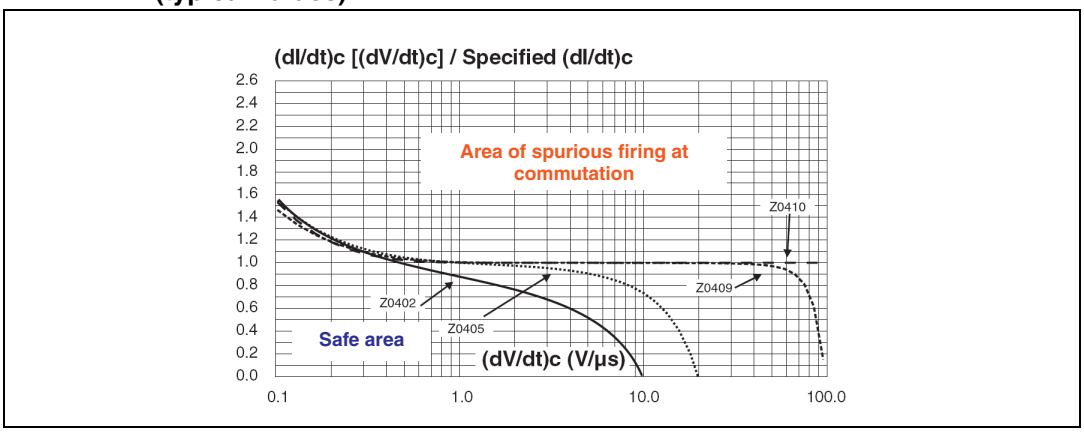
In TRIAC datasheets, the commutation behavior is specified in different way according to the TRIAC technologies. For standard TRIAC, a minimum (dV/dt)c is specified for a given (dI/dt)c. For logic level TRIACs, a minimum (dI/dt)c is specified for two given (dV/dt)c (0.1 V/µs and 10 V/µs). For Snubberless TRIACs, a minimum (dI/dt)c is specified without (dV/dt)c limitation.

Figure 4 represents the curve of the commutation behavior obtained with a standard 4 A TRIAC. This TRIAC is available with different sensitivities:

- Z0402: I_{GT} = 3 mA;
- Z0405: I_{GT} = 5 mA;
- Z0409: I_{GT} = 10 mA;
- Z0410: I_{GT} = 25 mA.

For lower sensitive gate TRIACs (Z0409 and Z0410), the (dI/dt)c is slightly modified according to the (dV/dt)c. For sensitive gate TRIACs (Z0402 and Z0405), this parameter noticeably decreases when the slope of the reapplied voltage increases.

Figure 4. Relative variation of (dI/dt)c versus (dV/dt)c for a 4 A standard TRIAC (typical values)



In practice, the current waveform, and thus the dI/dt_{OFF}, is imposed by the load. Generally we cannot change it.

So, in TRIAC applications, it is always necessary to know the dI/dt_{OFF} of the load to choose a TRIAC with a suitable (dI/dt)c. This is the most important parameter.

Suppose a circuit in which the dI/dt_{OFF} reaches 2 times the specified (dI/dt)c. The standard 4 A TRIACs, characterized by the curves in *Figure 4*, will be not suitable even if the dV/dt_{OFF} is equal to 0.1 V/µs.

1.3 Application requirements

1.3.1 TRIAC with resistive load

In this case, the TRIAC current and the mains voltage are in phase (see *Figure 5*). When the TRIAC switches off (i.e. when the current drops to zero), the mains voltage is equal to zero at this instant and will increase across the TRIAC according to the sinusoidal law:

Equation 1

$$V_{Mains} = V_{Max} \cdot \sin(\omega \cdot t)$$

For the European mains, i.e. V_{RMS} = 220 V at 50 Hz, the slope will be:

Equation 2

$$dV / dt_{OFF\,(V/\mu s)} = V_{RMS\,(V)} \cdot \sqrt{2} \cdot 2\pi \cdot f_{(Hz)} \cdot 10^{-6} \approx 0.1 \quad V/\mu s$$

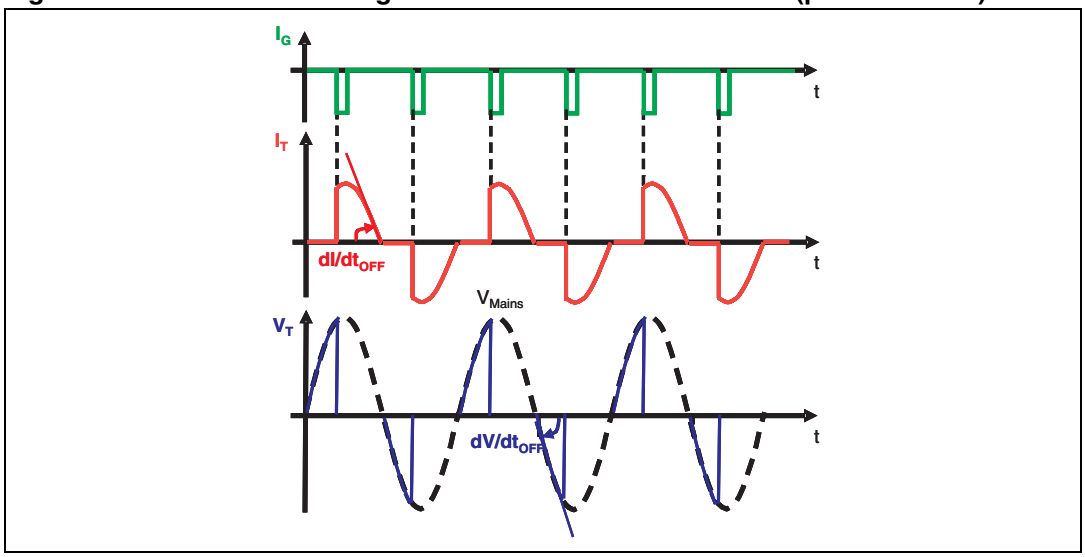
For 110 V, 60 Hz mains, the slope will be: $dV/dt_{OFF} \approx 0.06$ V/µs.

These relatively low dV/dt_{OFF} correspond to the left points on the curves in *Figure 4*. The dI/dt_{OFF} only depends on the load rms current and the mains frequency. For resistive loads, as for most other loads, we will have:

Equation 3

$$dI / dt_{OFF\,(A/ms)} = I_{RMS\,(A)} \cdot \sqrt{2} \cdot 2\pi \cdot f_{(Hz)} \cdot 10^{-3} \approx 0.5 \cdot I_{RMS\,(A)}$$

Figure 5. Current and voltage waveforms for resistive loads (phase control)

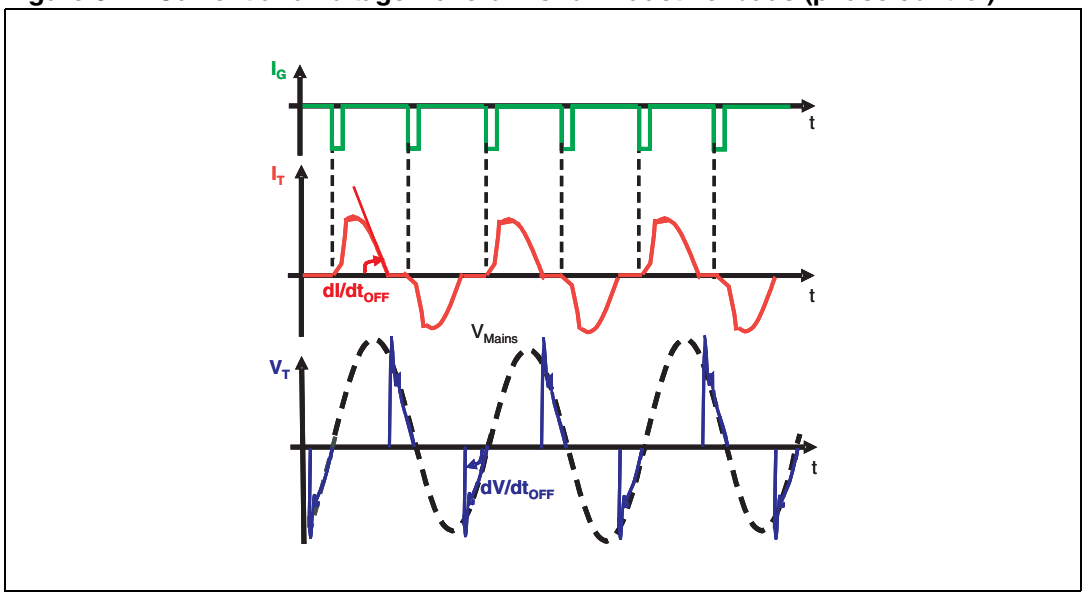


1.3.2 TRIAC with inductive load

An inductive load induces a phase lag between the TRIAC current and the mains voltage (see *Figure 6*).

When the current drops to zero, the TRIAC turns off and the voltage is abruptly applied across its terminals. To limit the speed of the reapplied voltage, a resistive / capacitive network mounted in parallel with the TRIAC is generally used (see *Figure 13*). This “snubber” is calculated to limit the dV/dt_{OFF} at a value for which the dI/dt_{OFF} is lower than the (dI/dt)c specified in the datasheet. The dI/dt_{OFF} is also determined in this case by the load impedance (Z) and the mains rms voltage. (see. AN437 for RC snubber circuit design)

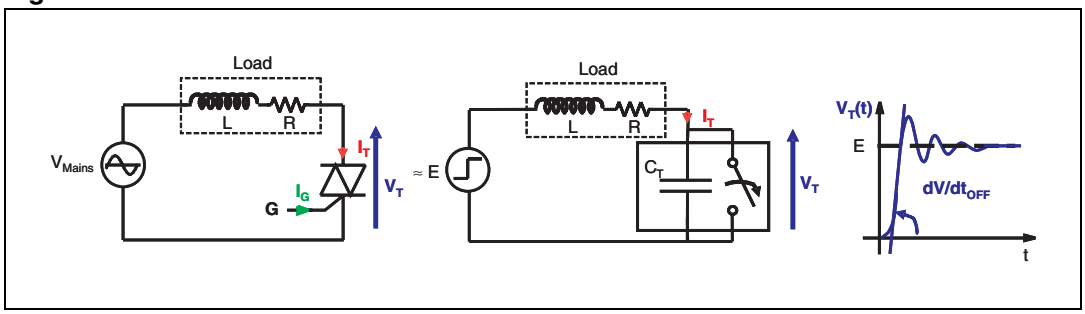
Figure 6. Current and voltage waveforms for inductive loads (phase control)



1.4 TRIAC without snubber network

Without snubber circuit, the dV/dt_{OFF} is limited by the capacitance between anode cathode junction of the TRIAC. When the current drops to zero, the TRIAC is considered as a switch which turns off. The dampened oscillating circuit is constituted by the loads, L and R, and the internal capacitance, C_T, of the TRIAC (see *Figure 7*). The final value E depends on the peak mains voltage and the phase difference (ϕ) between voltage and current.

Figure 7. TRIAC commutation on an inductive load without a snubber network



For a second order linear differential equation with a step function input, the voltage variation across the TRIAC ($V_T(t)$) is given by:

Equation 4

$$\frac{1}{\omega_0^2}\cdot\frac{d^2V_T(t)}{dt^2}+\frac{2.\xi}{\omega_0}\cdot\frac{dV_T(t)}{dt}+V_T(t)=E$$

With damping factor:

Equation 5

$$\xi=\frac{R_{(\Omega)}}{2}\cdot\sqrt{\frac{C_{T(F)}}{L_{(H)}}}$$

Undamped natural resonance:

Equation 6

$$\omega_{0(rad/s)}=\frac{1}{\sqrt{L_{(H)}\cdot C_{T(F)}}}$$

Final voltage value:

Equation 7

$$E=V_{RMS}\cdot\sqrt{2}\cdot\sin(\phi)$$

For example, the typical internal capacitances of 1 A, 12 A and 24 A TRIACs are respectively 12 pF, 90 pF and 180 pF (without direct voltage junction polarisation, worst case). Without snubber, and for most part of inductive loads, the damping factor (ξ) is generally lower than 1.

For an underdamped oscillating circuit ($0 \leq \xi \leq 1$), the voltage variation ($V_T(t)$) across the TRIAC is defined by:

Equation 8

$$V_T(t) = E - E \cdot \left(\cos(\omega_p \cdot t) + \frac{\xi \cdot \omega_0}{\omega_p} \cdot \sin(\omega_p \cdot t) \right) \cdot e^{-\xi \cdot \omega_0 \cdot t}$$

With damped natural resonance:

Equation 9

$$\omega_p = \omega_0 \cdot \sqrt{1 - \xi^2}$$

In the case of pure inductive load (R = 0, worst case), the circuit is undamped. The maximum reapplied dV/dt_{OFF} across the TRIAC is:

Equation 10

$$dV / dt_{OFF\,(V/\mu s)} = \frac{V_{RMS\,(V)} \cdot \sqrt{2}}{\sqrt{L_{(H)} \cdot C_{T(F)}}} .10^{-6} \quad \text{at} \quad t = \frac{\pi}{2.\omega_0}$$

Without snubber, according to the characteristics of inductive loads, the maximum dV/dt_{OFF} without snubber will be limited to about 60 V/µs for 100 – 220 V applications. Thus, it is not necessary to get the (dI/dt)c values for (dV/dt)c above 100 V/µs .

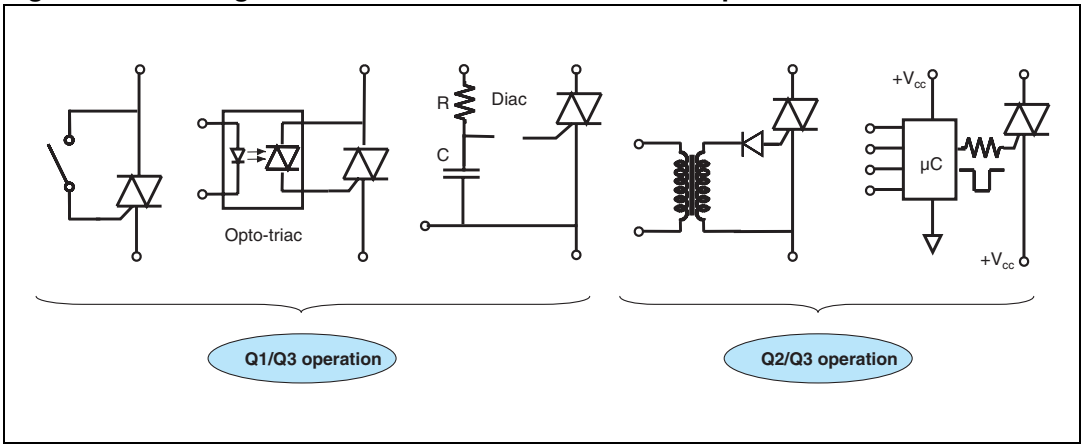
2 Logic level and Snubberless TRIACs

2.1 Operation in Q1-Q2-Q3 quadrants

To make significant progress in the TRIAC technology is to essentially improve the turn-off behaviour. In other words, the critical (dI/dt)c has to be improved.

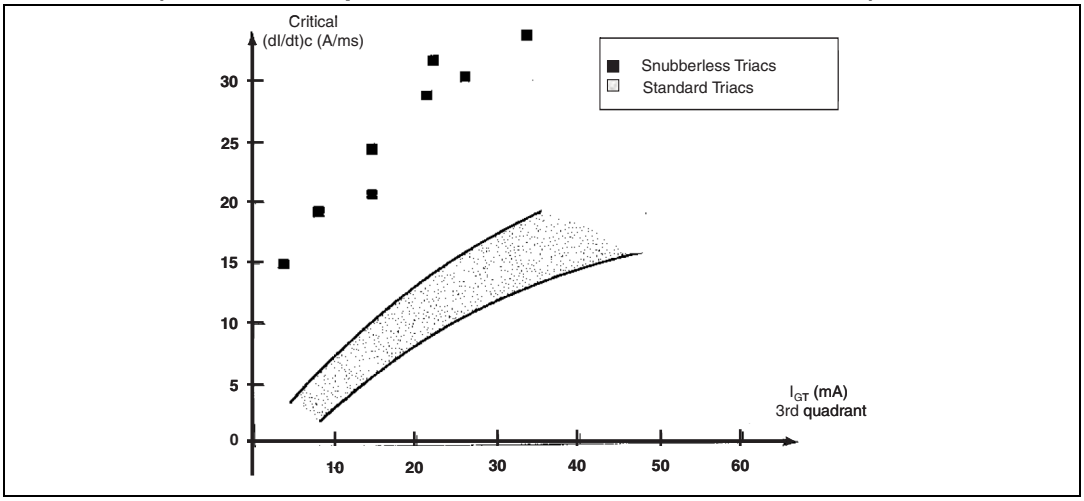
To reach this aim, a different structure has been developed. In this structure, the different active areas have been decoupled to separate the elementary thyristors and the gate area. This improvement provides the gate triggering in the fourth quadrant. In practice this modification does not lead to a problem because the gate drive circuits generally work in Q1/Q3 or Q2/Q3. (see *Figure 8*)

Figure 8. Basic gate drive circuits in Q1/Q3 or Q2/Q3 operations



For a given technology, the TRIACs commutation behaviour depends on the gate sensitivity. The correlation between the critical (dI/dt)c and the triggering gate current for 12 A TRIACs is represented in *Figure 9*. For a same current rating and gate sensitivity, Snubberless TRIACs present a (dI/dt)c at least 2 times higher than for standard TRIACs.

Figure 9. Correlation between commutation behavior and sensitivity (measurement performed on several lots of 12 A TRIACs)



Logic level TRIACs use the breakthrough of the Snubberless technology to improve the trade-off between sensitivity and commutation. Nevertheless, a snubber can still be necessary with these TRIACs.

2.2 Performances and specifications

2.2.1 Logic level TRIACs

In this category, sensitive TRIACs are defined by a maximum gate current (I_{GT}) of 5 mA for the TW type and 10 mA for the SW one.

In the datasheets of logic level TRIACs, a minimum (dI/dt)c is specified for the following cases:

- Resistive load with a (dV/dt)c of 0.1 V/µs.
- Inductive load with a (dV/dt)c of 10 V/µs.

For example, a 6 A logic level TRIAC is specified as follows:

Table 1. (dI/dt)c and (dV/dt)c specifications for a 6 A logic level TRIAC

Symbol	Test Conditions	Quadrant		BTA06 / BTB06		Unit
				TW	SW	
I_{GT} (1)	V_D = 12 V R_L = 30 Ω	I - II - III	MAX.	5	10	mA
V_{GT}		I - II - III	MAX.	1.3		V
(dI/dt)c (2)	(dV/dt)c = 0.1 V/µs T_j = 125 °C		MIN.	2.7	3.5	A/ms
	(dV/dt)c = 10 V/µs T_j = 125 °C			1.2	2.4	
	Without snubber T_j = 125 °C			-	-	

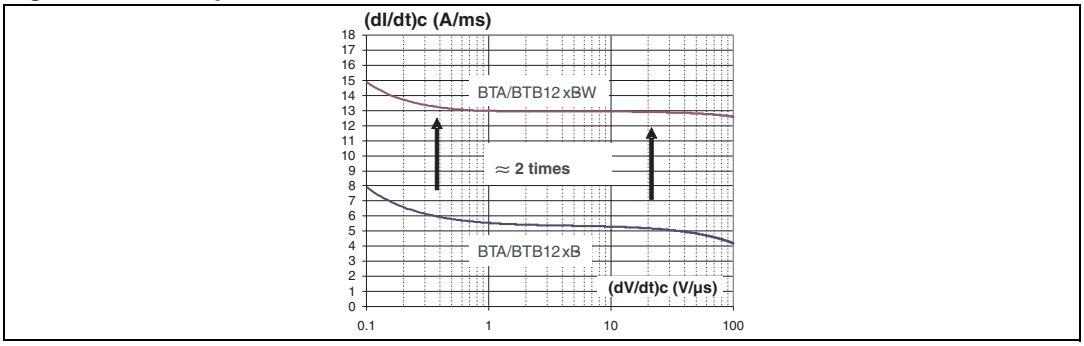
1. Minimum I_{GT} is guaranted at 5% of I_{GT} max
2. For both polarities of A2 referenced to A1

2.2.2 Snubberless TRIACs

This series covers the range of 6 to 25 A with gate currents of 35 mA (CW type) and 50 mA (BW type). This series has been specially designed so that the TRIACs turn-off without external snubber circuit.

For a same size and gate sensitivity, the (dI/dt)c improvement is at least equal to 2 between Snubberless and standard TRIACs (see *Figure 10*).

Figure 10. Comparison between standard and Snubberless 12 A TRIACs



Whatever the nature of the load, there is absolutely no risk of spurious turn-off triggering if the dI/dt_{OFF} is lower than the specified (dI/dt)c value. The specified (dI/dt)c for a Snubberless TRIAC is higher than the decreasing slope of its rms on-state current specified ($I_{T(RMS)}$).

Equation 11

$$dI/dt_{OFF\,(A/ms)} = I_{RMS\,(A)} \cdot \sqrt{2} \cdot 2\pi \cdot f_{(Hz)} \cdot 10^{-3} \approx 0.5 \cdot I_{RMS\,(A)}$$

$$dI/dt_{OFF\,(A/ms)} = 0.44 \cdot I_{RMS\,(A)} \quad \text{for 50 Hz}$$

$$dI/dt_{OFF\,(A/ms)} = 0.53 \cdot I_{RMS\,(A)} \quad \text{for 60 Hz}$$

For example, the slope of the decreasing current in a TRIAC conducting 6 A, 8 A, 10 A, 12 A, 16 A or 25 A when the current drops to zero is given in the *Table 2*.

Table 2 summarizes also the characteristics of the available BW and CW Snubberless TRIACs.

Table 2. (dI/dt)c specification for available BW and CW Snubberless TRIACs and slope of the different decreasing rms on-state currents ($I_{T(RMS)}$)

Type	$I_{T(RMS)}$ (A)	Voltage (V_{DRM} / V_{RRM}) (V)	Suffix	I_{GT} Max. (mA)	Static (dV/dt) Min. (V/µs)	(dI/dt)c Min. (1) (A/ms)	$I_{T(RMS)}$ x 0.5 (A/ms)
BTA / BTB	6	600	CW	35	400	3.5	3
			BW	50	1 000	5.3	
BTA / BTB	8	600 or 800	CW	35	400	4.5	4
			BW	50	1 000	7	
BTA / BTB	10	600 or 800	CW	35	500	5.5	5
			BW	50	1 000	9	
BTA / BTB	12	600 or 800	CW	35	500	6.5	6
			BW	50	1 000	12	
BTA / BTB	16	600 or 800	CW	35	500	8.5	8
			BW	50	1 000	14	

Table 2. (dI/dt)c specification for available BW and CW Snubberless TRIACs and slope of the different decreasing rms on-state currents ($I_{T(RMS)}$)

BTA / BTB	25	600 or 800	CW	35	500	13	12.5
			BW	50	1 000	22	

1. (dI/dt)c specified without snubber

2.3 Typical applications

2.3.1 Logic level TRIACs

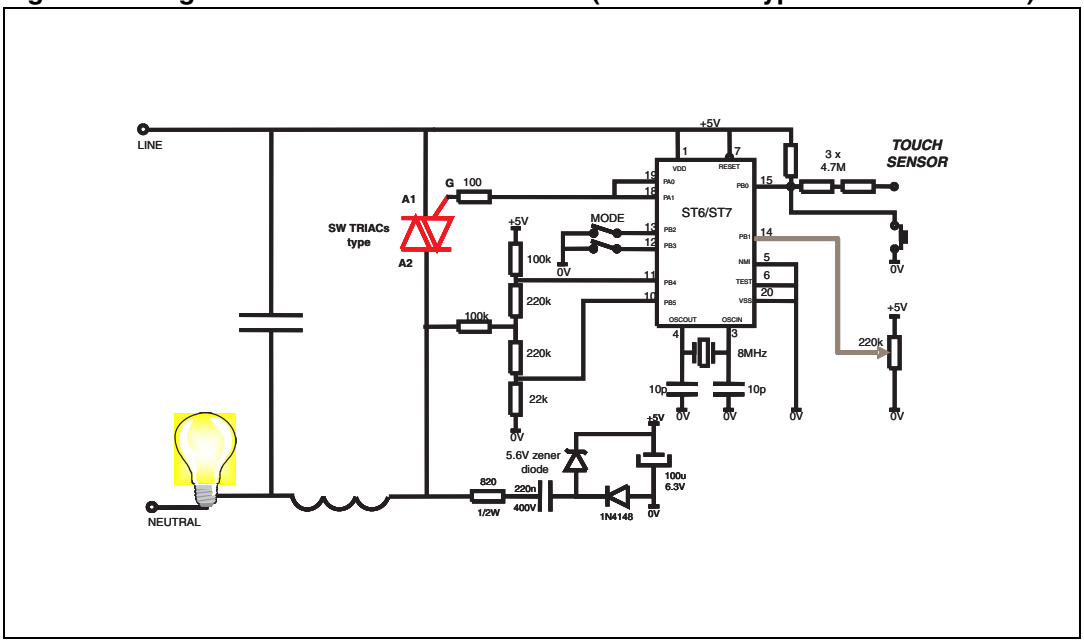
These TRIACs can be directly controlled by logic circuits and microcontrollers like the ST6 or ST7 series. Outputs of ST6/ST7 can sink currents up to 20 mA per I/O line, and therefore drive TW and SW.

These TRIACs are ideal interface for power components supplied by 110 V or 220 V, such as valves, heating resistances, and small motors.

The specification of the critical (dI/dt)c on both resistive and inductive loads offers:

- Knowledge of the security margin of the circuit in relation to the risk of the spurious triggering
- Optimization of the performance of the TRIAC used, which results in a cost reduction

Figure 11. Light dimmer circuit with ST6/ST7 (SW TRIACs type is recommended)



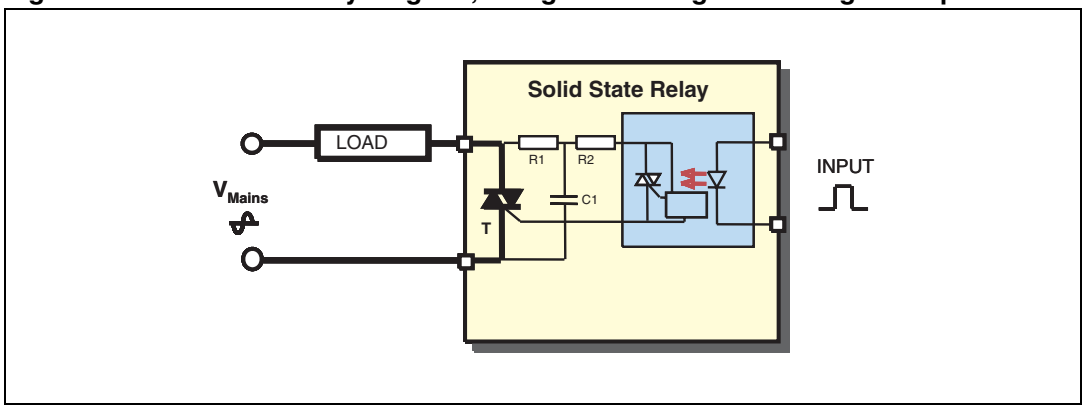
2.3.2 Snubberless TRIACs

The commutation of Snubberless TRIACs is specified without a (dV/dt)c limitation. The external snubber circuit can be suppressed for TRIAC turn-off and leads to a noticeable cost reduction. Nevertheless, a snubber circuit is sometimes used to eliminate spurious triggering due to fast line transients (see *Figure 13*).

Thanks to their significant improvement in the trade-off between gate sensitivity (I_{GT}) and critical (dI/dt)c value and also static dV/dt, Snubberless TRIACs are used in circuits which need high safety margin, such as:

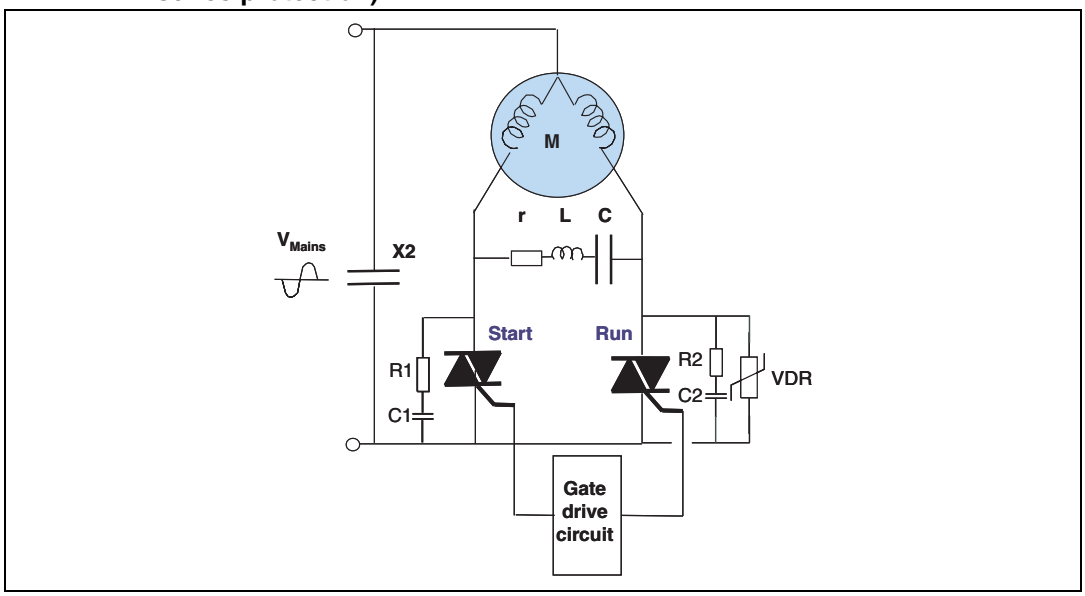
- Static relays in which the load is not well defined. With standard TRIACs, it is difficult to adapt the snubber to all possible cases. Snubberless TRIACs resolve this problem (see *Figure 12*).

Figure 12. Solid state relay diagram, using Zero Voltage Switching with opto-TRIAC



- Motor drive circuits. The circuit Figure 12 shows an asynchronous motor controlled in both direction by turning on each TRIAC alternately.

Figure 13. Motor control circuit using Snubberless TRIACs (Ls + r = network for series protection)



Note: Series impedance (r + L) is needed to protect the blocked TRIAC in case of unwanted triggering (when the other is already on). Only one clamping device (V_{DR}) provides overvoltage protection for both TRIACs (IEC 61000-4-5). Snubber networks (R1C1 and R2C2) eliminate spurious triggering due to fast line transients (IEC 61000-4-4).

The specified (dI/dt)c for a Snubberless TRIAC is higher than the decreasing slope of its specified rms on-state current ($I_{T(RMS)}$). This feature is important for several applications, including:

- Circuits in which the dI/dt_{OFF} is higher than the dI/dt_{OFF} calculated with the *Equation 3*. For universal motors, due to the impact of the brushes, the dI/dt_{OFF} is typically three times higher (see *Figure 14*). *Table 3* illustrates the component choice optimization by using Snubberless TRIACs. For example, a 8 A Snubberless TRIAC is sufficient to control a 110 V / 600 W motor instead of a 16 A standard TRIAC.

Figure 14. TRIAC turn-off behavior for universal motors

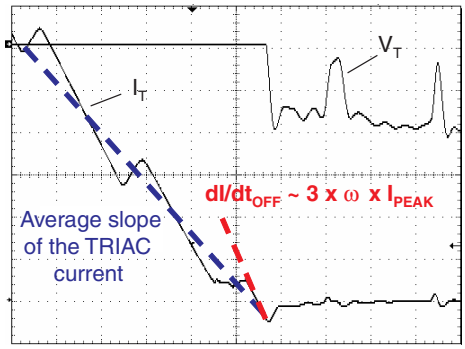


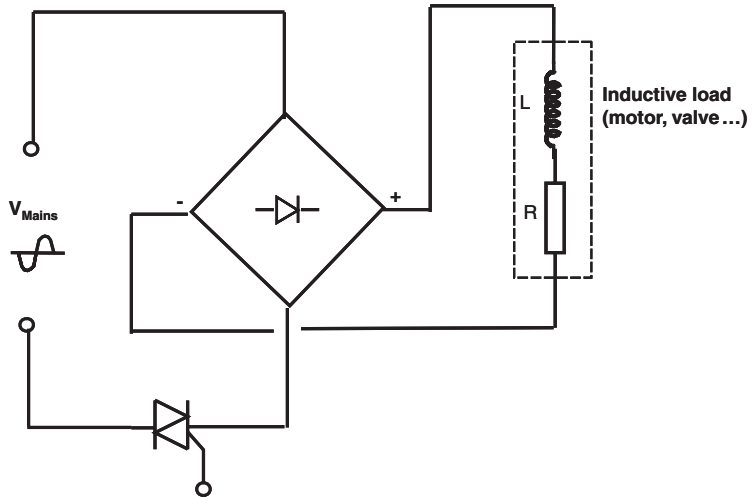
Table 3. TRIAC choice for universal motor control

Power	Mains voltage and frequency	Load current	$I_{T(RMS)}$	dI/dt_{OFF} Max. (1)	Standard TRIAC	Snubberless TRIAC
600 W	220 V / 50 Hz	3 A rms	6 A	3.5 A/ms	BTx10-600B	BTx06-600BW
	110 V / 60 Hz	6 A rms	10 A	7 A/ms	BTx16-600B (2)	BTx08-600BW
1200 W	220 V / 50 Hz	6 A rms	10 A	7 A/ms	BTx16-600B (2)	BTx08-600BW
	110 V / 60 Hz	12 A rms	16 A	15 A/ms	BTx40-600B / BTx41-600B	BTx24-600CW

1. Maximum dI/dt_{OFF}. This parameter depends on the type of motor and can be higher during start-up.
2. This type specified at 7 A/ms minimum can be too small. Certain applications could need 25 A standard TRIAC.

- Circuits which generate waveforms with a very high dI/dt_{OFF}, such as inductive load controlled by a diode bridge (see *Figure 15*). The current variation at turn-off is then only limited by the parasitic inductance of the line and the diodes bridge circuit.

Figure 15. Inductive load controlled by a diode bridge



3 Conclusion

Thanks to the logic level and Snubberless TRIACs, the designer can use devices with a commutation behavior which is compatible with all applications in the 50 or 60 Hz range. This includes phase control and static commutation for loads going from a few watts to several kilowatts.

These classes of TRIAC offer:

- An increase in the security margin of circuits, particularly where there is a risk of spurious triggering
- Reduction of costs by using logic level TRIACs, without the need of an interface between the TRIAC gate and the logic circuit, or using Snubberless TRIACs, which are specified without a resistive / capacitive network

4 Revision history

Table 4. Document revision history

Date	Revision	Changes
May-1992	1	Initial release.
19-Apr-2004	2	Stylesheet update. No content change.
07-Mar-2008	3	Reformatted to current standards. Complete rewrite for text and graphics. Part numbers updated for current products.