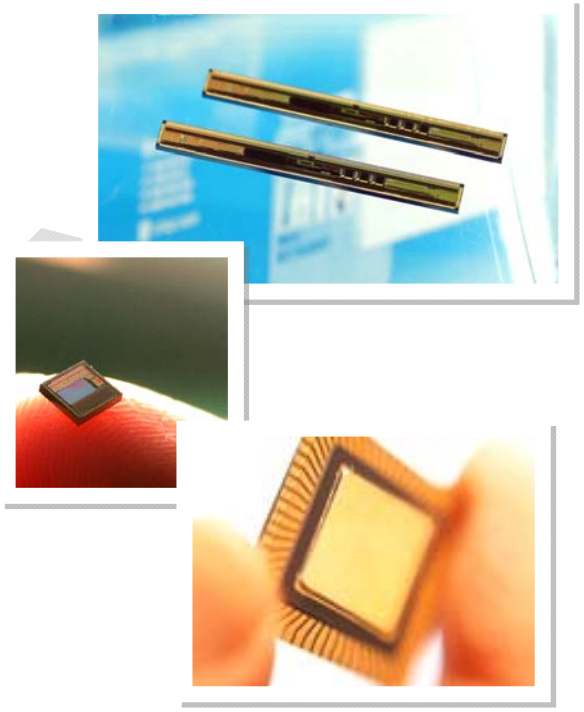
Raydium 瑞鼎科技股份有限公司
Raydium Semiconductor Corporation



RM68050 Data Sheet

Single Chip Driver with 262K color

for 240RGBx320 a-Si TFT LCD

Revision：0.1

Date：Sept 1, 2009

Revision History：

Revision	Description Of Change	Date
0.1	New creation	2009/09/01

Table of Content

1. General Description

The RM68050 is a single-chip liquid crystal controller driver LSI for a-Si TFT panel, comprising 172,800 bytes RAM for a maximum 240 RGB x 320 dots graphics display, source driver, gate driver and power supply circuit. For efficient data transfer, the RM68050 supports high-speed interface via 8-/9-/16-/18-bit ports as system interface to the microcomputer and high-speed RAM write function. As moving picture interface, the RM68050 supports RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, and DB17-0).

Also, the RM68050 incorporates step-up circuit and voltage follower circuit to generate TFT liquid crystal panel drive voltages.

The RM68050's power management functions such as 8-color display and power operation mode such as deep standby mode, standby mode and sleep mode make this LSI a perfect driver for the medium or small sized portable products with color display systems such as digital cellular phones or hand-held devices with outstanding battery consistency.

2. Features

- A single-chip controller driver incorporating a gate circuit and a power supply circuit for a maximum 240 RGB x 320 dots graphics display on amorphous TFT panel in 262k colors
- System interface
  1. High-speed interface via 8-, 9-, 16-, 18-bit parallel ports
  2. Clock synchronous serial interface
- Moving picture display interface
  1. 6-, 16-, 18-bit RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, DB17-0)
  2. VSYNC interface (System interface + VSYNC)
- High-speed RAM write function
- Window address function to specify a rectangular area writing data in the internal RAM
- Write data within a rectangular area in the internal RAM via moving picture interface
- Reduce data transfer repeat by specifying the area in the RAM to rewrite data
- Support displaying still picture data in RAM area while displaying moving pictures simultaneously

- Abundant color display and drawing functions
  1. Programmable γ-correction function for 262k-color display
  2. Partial display function
- Low power consumption architecture (allowing direct input of interface I/O power supply)
  1. Deep standby mode
  2. Standby mode
  3. Sleep mode
  4. 8-color display function
  5. Input power supply voltages: IOVCC = 1.65V~3.3V (interface I/O power supply)
     VCI = 2.5V~3.3V (liquid crystal analog circuit power supply)
- Incorporates a liquid crystal drive power supply circuit
  1. Source driver liquid crystal drive/VCOM power supply: DDVDH-GND = 4.5V ~ 6.0V
     VCL-GND = -2.0V ~ -3.0V
     VCI-VCL ≦ 6.0V
  2. Gate drive power supply: VGH-GND = 10.0V ~ 19.8V
     VGL-GND = -4.5V ~ -13.5V
     VGH-VGL ≦ 30.0V
  3. VCOM drive (VCOM power supply): VCOMH = (VCI+0.2)V ~ (DDVDH-0.2)V
     VCOML = (VCL+0.2) V ~ 0V
     VCOMH-VCOML amplitude = 6.0V (max.)
- Liquid crystal power supply startup sequencer
- TFT storage capacitance: Cst only (common VCOM formula)
- 172,800-byte internal RAM
- Internal 720-channel source driver and 320-channel gate driver
- Single-chip solution for COG module with the arrangement of gate circuits on both sides of the

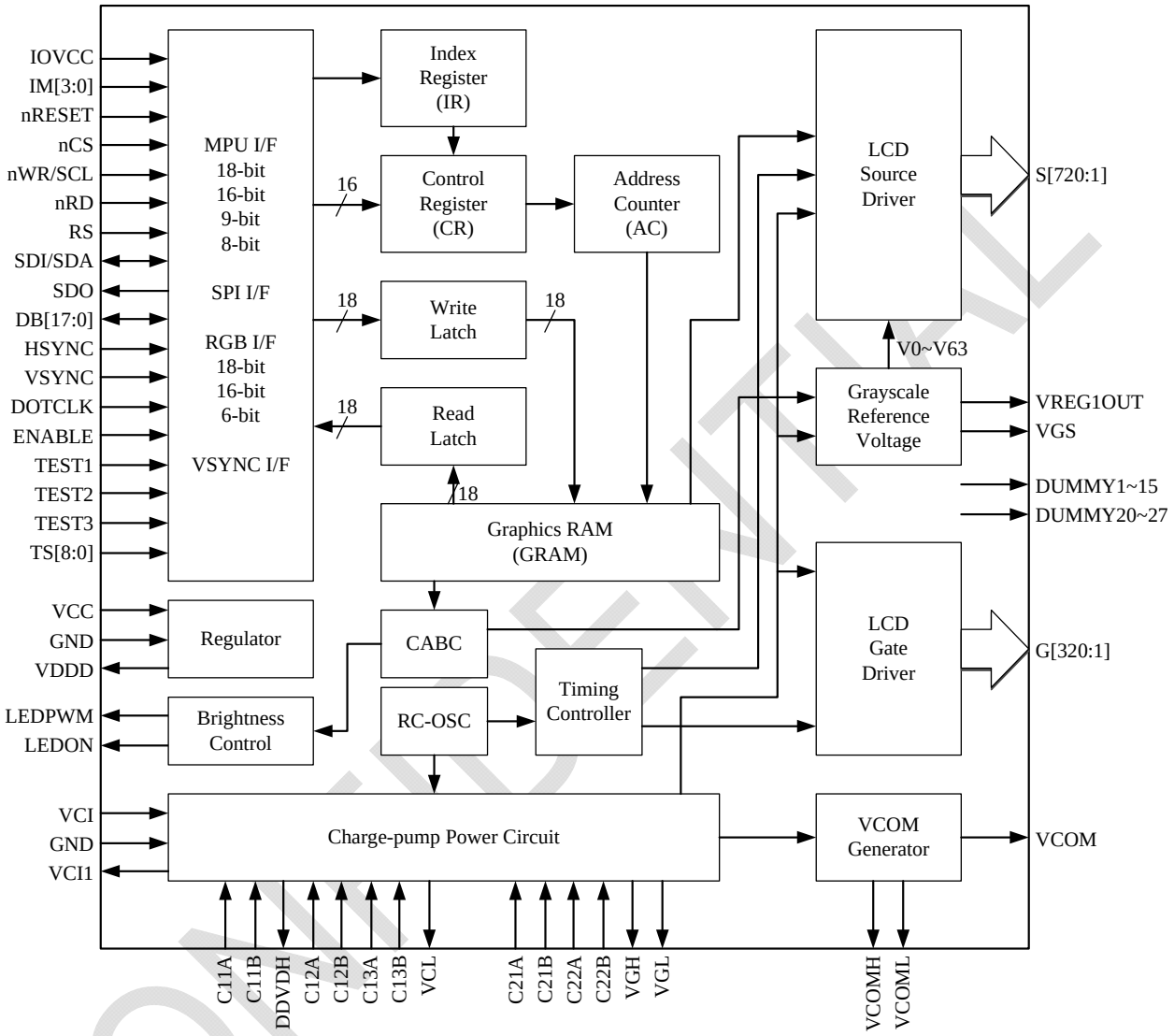
glass substrate

- Internal reference voltage: to generate VREG1OUT
- CABC (Content Adaptive Brightness Control)

Table 1 Power Supply Specifications

No.	Item		RM68050
1	TFT data lines		720 output
2	TFT gate lines		320 output
3	TFT display storage capacitance		Cst only (Common VCOM)
4	Liquid crystal drive output	S1~S720	V0~V63 grayscales
		G1~G320	VGH-VGL
		VCOM	Change VCOMH-VCOML amplitude with electronic volume Change VCOMH with either electronic volume or from VCOMR
5	Input voltage	IOVCC (interface voltage)	1.65V~3.30V Power supply to IM0/ID, IM1-3, nRESET, DB17-0, nRD, SDI, SDO, WR/SCL, RS, nCS, VSYNC, HSYNC, DOTCLK, ENABLE, FMARK. Connect to VCC and VCI on the FPC when the electrical potentials are the same.
		VCI (liquid crystal drive power supply voltage)	2.40V~3.30V Connect to IOVCC and VCC on the FPC when the electrical potentials are the same.
6	Liquid crystal drive voltages	DDVDH	4.5V ~ 6.0V
		VGH	10.0V ~ 19.8V
		VGL	-4.5V ~ -13.5V
		VGH-VGL	Max. 30.0V
		VCL	-1.9V ~ -3.3V
		VCI-VCL	Max. 6.0V
7	Internal step-up circuits	VLOUT1 (DDVDH)	VCI1x2
		VLOUT2 (VGH)	VCI1x4, x5, x6
		VLOUT3 (VGL)	VCI1x-3, -4, -5
		VCL	VCI1x-1

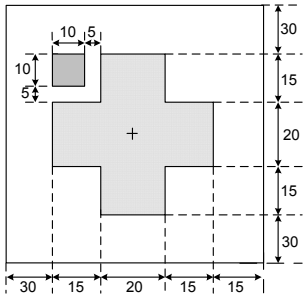
3. Block Diagram



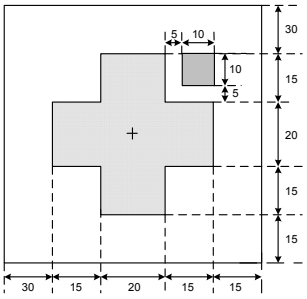
4. Pin Diagram

Alignment Marks

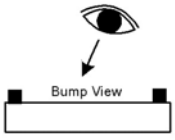
A1

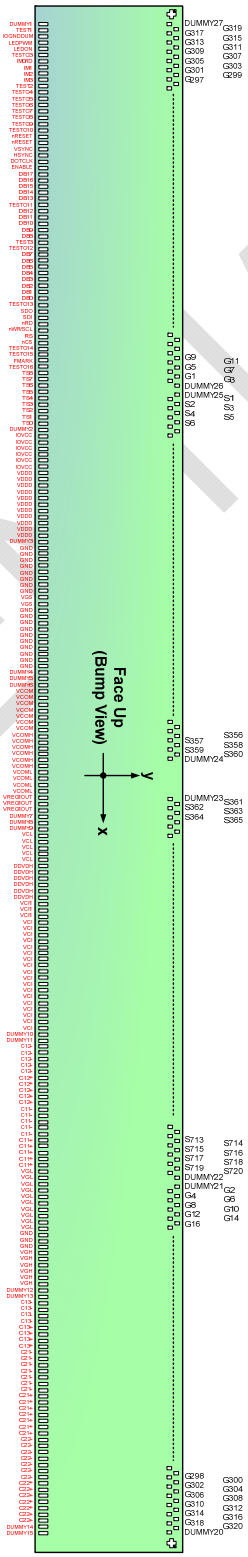


A2



Unit: um





- Chip size: 17.82 mm x 0.73 mm (Include sealing and scribe line)
- Chip thickness: 280 um (typ.)
- PAD coordinates: PAD center
- PAD coordinates origin: Chip center
- Au bump size

4.1.1 16um x 98um: Gate:G1~G320, Source:S1~S720

4.1.2 50um x 80um: Input Pads, Pad 1 ~ 243

- Au bump pitch: See PAD coordinates table
- Au bump height: 12um (typ.)
- Alignment mark

Alignment mark shape	X	Y
Type A	-8751.0	214.5
	8751.0	214.5

Pad Coordinate (Unit: um)

No	Name	X	Y	No	Name	X	Y	No	Name	X	Y	No	Name	X	Y
1	DUMMY1	-8610	-252	61	TS4	-4130	-252	121	VCOML	70	-252	181	C11+	4270	-252
2	TEST1	-8540	-252	62	TS3	-4060	-252	122	VCOML	140	-252	182	C11+	4340	-252
3	IOGNDDUM	-8470	-252	63	TS2	-3990	-252	123	VCOML	210	-252	183	C11+	4410	-252
4	LEDPWM	-8400	-252	64	TS1	-3920	-252	124	VCOML	280	-252	184	C11+	4480	-252
5	LEDON	-8330	-252	65	TS0	-3850	-252	125	VREG1OUT	350	-252	185	VGL	4550	-252
6	TESTO3	-8260	-252	66	DUMMY2	-3780	-252	126	VREG1OUT	420	-252	186	VGL	4620	-252
7	IM0/ID	-8190	-252	67	IOVCC	-3710	-252	127	VREG1OUT	490	-252	187	VGL	4690	-252
8	IM1	-8120	-252	68	IOVCC	-3640	-252	128	DUMMY7	560	-252	188	VGL	4760	-252
9	IM2	-8050	-252	69	IOVCC	-3570	-252	129	DUMMY8	630	-252	189	VGL	4830	-252
10	IM3	-7980	-252	70	IOVCC	-3500	-252	130	DUMMY9	700	-252	190	VGL	4900	-252
11	TEST2	-7910	-252	71	IOVCC	-3430	-252	131	VCL	770	-252	191	VGL	4970	-252
12	TESTO4	-7840	-252	72	IOVCC	-3360	-252	132	VCL	840	-252	192	VGL	5040	-252
13	TESTO5	-7770	-252	73	VDDD	-3290	-252	133	VCL	910	-252	193	VGL	5110	-252
14	TESTO6	-7700	-252	74	VDDD	-3220	-252	134	VCL	980	-252	194	VGL	5180	-252
15	TESTO7	-7630	-252	75	VDDD	-3150	-252	135	VCL	1050	-252	195	GND	5250	-252
16	TESTO8	-7560	-252	76	VDDD	-3080	-252	136	DDVDH	1120	-252	196	GND	5320	-252
17	TESTO9	-7490	-252	77	VDDD	-3010	-252	137	DDVDH	1190	-252	197	GND	5390	-252
18	TESTO10	-7420	-252	78	VDDD	-2940	-252	138	DDVDH	1260	-252	198	VGH	5460	-252
19	nRESET	-7350	-252	79	VDDD	-2870	-252	139	DDVDH	1330	-252	199	VGH	5530	-252
20	nRESET	-7280	-252	80	VDDD	-2800	-252	140	DDVDH	1400	-252	200	VGH	5600	-252
21	VSYNC	-7210	-252	81	VDDD	-2730	-252	141	DDVDH	1470	-252	201	VGH	5670	-252
22	HSYNC	-7140	-252	82	VDDD	-2660	-252	142	VCI1	1540	-252	202	VGH	5740	-252
23	DOTCLK	-7070	-252	83	VDDD	-2590	-252	143	VCI1	1610	-252	203	VGH	5810	-252
24	ENABLE	-7000	-252	84	DUMMY3	-2520	-252	144	VCI1	1680	-252	204	DUMMY12	5880	-252
25	DB17	-6905	-252	85	GND	-2450	-252	145	VCI	1750	-252	205	DUMMY13	5950	-252
26	DB16	-6825	-252	86	GND	-2380	-252	146	VCI	1820	-252	206	C13-	6020	-252
27	DB15	-6745	-252	87	GND	-2310	-252	147	VCI	1890	-252	207	C13-	6090	-252
28	DB14	-6665	-252	88	GND	-2240	-252	148	VCI	1960	-252	208	C13-	6160	-252
29	DB13	-6585	-252	89	GND	-2170	-252	149	VCI	2030	-252	209	C13-	6230	-252
30	TESTO11	-6495	-252	90	GND	-2100	-252	150	VCI	2100	-252	210	C13+	6300	-252
31	DB12	-6405	-252	91	GND	-2030	-252	151	VCI	2170	-252	211	C13+	6370	-252
32	DB11	-6325	-252	92	GND	-1960	-252	152	VCI	2240	-252	212	C13+	6440	-252
33	DB10	-6245	-252	93	VGS	-1890	-252	153	VCI	2310	-252	213	C13+	6510	-252
34	DB9	-6165	-252	94	VGS	-1820	-252	154	VCI	2380	-252	214	C21-	6580	-252
35	DB8	-6085	-252	95	GND	-1750	-252	155	VCI	2450	-252	215	C21-	6650	-252
36	TEST3	-5990	-252	96	GND	-1680	-252	156	VCI	2520	-252	216	C21-	6720	-252
37	TESTO12	-5920	-252	97	GND	-1610	-252	157	VCI	2590	-252	217	C21-	6790	-252
38	DB7	-5825	-252	98	GND	-1540	-252	158	VCI	2660	-252	218	C21-	6860	-252
39	DB6	-5745	-252	99	GND	-1470	-252	159	VCI	2730	-252	219	C21-	6930	-252
40	DB5	-5665	-252	100	GND	-1400	-252	160	VCI	2800	-252	220	C21-	7000	-252
41	DB4	-5585	-252	101	GND	-1330	-252	161	VCI	2870	-252	221	C21+	7070	-252
42	DB3	-5505	-252	102	GND	-1260	-252	162	VCI	2940	-252	222	C21+	7140	-252
43	DB2	-5425	-252	103	GND	-1190	-252	163	DUMMY10	3010	-252	223	C21+	7210	-252
44	DB1	-5345	-252	104	GND	-1120	-252	164	DUMMY11	3080	-252	224	C21+	7280	-252
45	DB0	-5265	-252	105	DUMMY4	-1050	-252	165	C12-	3150	-252	225	C21+	7350	-252
46	TESTO13	-5180	-252	106	DUMMY5	-980	-252	166	C12-	3220	-252	226	C21+	7420	-252
47	SDO	-5110	-252	107	DUMMY6	-910	-252	167	C12-	3290	-252	227	C21+	7490	-252
48	SDI	-5040	-252	108	VCOM	-840	-252	168	C12-	3360	-252	228	C22-	7560	-252
49	nRD	-4970	-252	109	VCOM	-770	-252	169	C12-	3430	-252	229	C22-	7630	-252
50	nWR/SCL	-4900	-252	110	VCOM	-700	-252	170	C12+	3500	-252	230	C22-	7700	-252
51	RS	-4830	-252	111	VCOM	-630	-252	171	C12+	3570	-252	231	C22-	7770	-252
52	nCS	-4760	-252	112	VCOM	-560	-252	172	C12+	3640	-252	232	C22-	7840	-252
53	TESTO14	-4690	-252	113	VCOM	-490	-252	173	C12+	3710	-252	233	C22-	7910	-252
54	TESTO15	-4620	-252	114	VCOM	-420	-252	174	C12+	3780	-252	234	C22-	7980	-252
55	FMARK	-4550	-252	115	VCOMH	-350	-252	175	C11-	3850	-252	235	C22+	8050	-252
56	TESTO16	-4480	-252	116	VCOMH	-280	-252	176	C11-	3920	-252	236	C22+	8120	-252
57	TS8	-4410	-252	117	VCOMH	-210	-252	177	C11-	3990	-252	237	C22+	8190	-252
58	TS7	-4340	-252	118	VCOMH	-140	-252	178	C11-	4060	-252	238	C22+	8260	-252
59	TS6	-4270	-252	119	VCOMH	-70	-252	179	C11-	4130	-252	239	C22+	8330	-252
60	TS5	-4200	-252	120	VCOMH	0	-252	180	C11+	4200	-252	240	C22+	8400	-252

No	Name	X	Y
241	C22+	8470	-252
242	DUMMY14	8540	-252
243	DUMMY15	8610	-252
244	DUMMY20	8659	148
245	G320	8643	265
246	G318	8627	148
247	G316	8611	265
248	G314	8595	148
249	G312	8579	265
250	G310	8563	148
251	G308	8547	265
252	G306	8531	148
253	G304	8515	265
254	G302	8499	148
255	G300	8483	265
256	G298	8467	148
257	G296	8451	265
258	G294	8435	148
259	G292	8419	265
260	G290	8403	148
261	G288	8387	265
262	G286	8371	148
263	G284	8355	265
264	G282	8339	148
265	G280	8323	265
266	G278	8307	148
267	G276	8291	265
268	G274	8275	148
269	G272	8259	265
270	G270	8243	148
271	G268	8227	265
272	G266	8211	148
273	G264	8195	265
274	G262	8179	148
275	G260	8163	265
276	G258	8147	148
277	G256	8131	265
278	G254	8115	148
279	G252	8099	265
280	G250	8083	148
281	G248	8067	265
282	G246	8051	148
283	G244	8035	265
284	G242	8019	148
285	G240	8003	265
286	G238	7987	148
287	G236	7971	265
288	G234	7955	148
289	G232	7939	265
290	G230	7923	148
291	G228	7907	265
292	G226	7891	148
293	G224	7875	265
294	G222	7859	148
295	G220	7843	265
296	G218	7827	148
297	G216	7811	265
298	G214	7795	148
299	G212	7779	265
300	G210	7763	148

No	Name	X	Y
301	G208	7747	265
302	G206	7731	148
303	G204	7715	265
304	G202	7699	148
305	G200	7683	265
306	G198	7667	148
307	G196	7651	265
308	G194	7635	148
309	G192	7619	265
310	G190	7603	148
311	G188	7587	265
312	G186	7571	148
313	G184	7555	265
314	G182	7539	148
315	G180	7523	265
316	G178	7507	148
317	G176	7491	265
318	G174	7475	148
319	G172	7459	265
320	G170	7443	148
321	G168	7427	265
322	G166	7411	148
323	G164	7395	265
324	G162	7379	148
325	G160	7363	265
326	G158	7347	148
327	G156	7331	265
328	G154	7315	148
329	G152	7299	265
330	G150	7283	148
331	G148	7267	265
332	G146	7251	148
333	G144	7235	265
334	G142	7219	148
335	G140	7203	265
336	G138	7187	148
337	G136	7171	265
338	G134	7155	148
339	G132	7139	265
340	G130	7123	148
341	G128	7107	265
342	G126	7091	148
343	G124	7075	265
344	G122	7059	148
345	G120	7043	265
346	G118	7027	148
347	G116	7011	265
348	G114	6995	148
349	G112	6979	265
350	G110	6963	148
351	G108	6947	265
352	G106	6931	148
353	G104	6915	265
354	G102	6899	148
355	G100	6883	265
356	G98	6867	148
357	G96	6851	265
358	G94	6835	148
359	G92	6819	265
360	G90	6803	148

No	Name	X	Y
361	G88	6787	265
362	G86	6771	148
363	G84	6755	265
364	G82	6739	148
365	G80	6723	265
366	G78	6707	148
367	G76	6691	265
368	G74	6675	148
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370	G70	6643	148
371	G68	6627	265
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374	G62	6579	148
375	G60	6563	265
376	G58	6547	148
377	G56	6531	265
378	G54	6515	148
379	G52	6499	265
380	G50	6483	148
381	G48	6467	265
382	G46	6451	148
383	G44	6435	265
384	G42	6419	148
385	G40	6403	265
386	G38	6387	148
387	G36	6371	265
388	G34	6355	148
389	G32	6339	265
390	G30	6323	148
391	G28	6307	265
392	G26	6291	148
393	G24	6275	265
394	G22	6259	148
395	G20	6243	265
396	G18	6227	148
397	G16	6211	265
398	G14	6195	148
399	G12	6179	265
400	G10	6163	148
401	G8	6147	265
402	G6	6131	148
403	G4	6115	265
404	G2	6099	148
405	DUMMY21	6083	265
406	DUMMY22	6047	265
407	S720	6031	148
408	S719	6015	265
409	S718	5999	148
410	S717	5983	265
411	S716	5967	148
412	S715	5951	265
413	S714	5935	148
414	S713	5919	265
415	S712	5903	148
416	S711	5887	265
417	S710	5871	148
418	S709	5855	265
419	S708	5839	148
420	S707	5823	265

No	Name	X	Y
421	S706	5807	148
422	S705	5791	265
423	S704	5775	148
424	S703	5759	265
425	S702	5743	148
426	S701	5727	265
427	S700	5711	148
428	S699	5695	265
429	S698	5679	148
430	S697	5663	265
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435	S692	5583	148
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438	S689	5535	265
439	S688	5519	148
440	S687	5503	265
441	S686	5487	148
442	S685	5471	265
443	S684	5455	148
444	S683	5439	265
445	S682	5423	148
446	S681	5407	265
447	S680	5391	148
448	S679	5375	265
449	S678	5359	148
450	S677	5343	265
451	S676	5327	148
452	S675	5311	265
453	S674	5295	148
454	S673	5279	265
455	S672	5263	148
456	S671	5247	265
457	S670	5231	148
458	S669	5215	265
459	S668	5199	148
460	S667	5183	265
461	S666	5167	148
462	S665	5151	265
463	S664	5135	148
464	S663	5119	265
465	S662	5103	148
466	S661	5087	265
467	S660	5071	148
468	S659	5055	265
469	S658	5039	148
470	S657	5023	265
471	S656	5007	148
472	S655	4991	265
473	S654	4975	148
474	S653	4959	265
475	S652	4943	148
476	S651	4927	265
477	S650	4911	148
478	S649	4895	265
479	S648	4879	148
480	S647	4863	265

No	Name	X	Y
481	S646	4847	148
482	S645	4831	265
483	S644	4815	148
484	S643	4799	265
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1168	G75	-6691	265
1169	G77	-6707	148
1170	G79	-6723	265
1171	G81	-6739	148
1172	G83	-6755	265
1173	G85	-6771	148
1174	G87	-6787	265
1175	G89	-6803	148
1176	G91	-6819	265
1177	G93	-6835	148
1178	G95	-6851	265
1179	G97	-6867	148
1180	G99	-6883	265
1181	G101	-6899	148
1182	G103	-6915	265
1183	G105	-6931	148
1184	G107	-6947	265
1185	G109	-6963	148
1186	G111	-6979	265
1187	G113	-6995	148
1188	G115	-7011	265
1189	G117	-7027	148
1190	G119	-7043	265
1191	G121	-7059	148
1192	G123	-7075	265
1193	G125	-7091	148
1194	G127	-7107	265
1195	G129	-7123	148
1196	G131	-7139	265
1197	G133	-7155	148
1198	G135	-7171	265
1199	G137	-7187	148
1200	G139	-7203	265

No	Name	X	Y
1201	G141	-7219	148
1202	G143	-7235	265
1203	G145	-7251	148
1204	G147	-7267	265
1205	G149	-7283	148
1206	G151	-7299	265
1207	G153	-7315	148
1208	G155	-7331	265
1209	G157	-7347	148
1210	G159	-7363	265
1211	G161	-7379	148
1212	G163	-7395	265
1213	G165	-7411	148
1214	G167	-7427	265
1215	G169	-7443	148
1216	G171	-7459	265
1217	G173	-7475	148
1218	G175	-7491	265
1219	G177	-7507	148
1220	G179	-7523	265
1221	G181	-7539	148
1222	G183	-7555	265
1223	G185	-7571	148
1224	G187	-7587	265
1225	G189	-7603	148
1226	G191	-7619	265
1227	G193	-7635	148
1228	G195	-7651	265
1229	G197	-7667	148
1230	G199	-7683	265
1231	G201	-7699	148
1232	G203	-7715	265
1233	G205	-7731	148
1234	G207	-7747	265
1235	G209	-7763	148
1236	G211	-7779	265
1237	G213	-7795	148
1238	G215	-7811	265
1239	G217	-7827	148
1240	G219	-7843	265
1241	G221	-7859	148
1242	G223	-7875	265
1243	G225	-7891	148
1244	G227	-7907	265
1245	G229	-7923	148
1246	G231	-7939	265
1247	G233	-7955	148
1248	G235	-7971	265
1249	G237	-7987	148
1250	G239	-8003	265
1251	G241	-8019	148
1252	G243	-8035	265
1253	G245	-8051	148
1254	G247	-8067	265
1255	G249	-8083	148
1256	G251	-8099	265
1257	G253	-8115	148
1258	G255	-8131	265
1259	G257	-8147	148
1260	G259	-8163	265

No	Name	X	Y
1261	G261	-8179	148
1262	G263	-8195	265
1263	G265	-8211	148
1264	G267	-8227	265
1265	G269	-8243	148
1266	G271	-8259	265
1267	G273	-8275	148
1268	G275	-8291	265
1269	G277	-8307	148
1270	G279	-8323	265
1271	G281	-8339	148
1272	G283	-8355	265
1273	G285	-8371	148
1274	G287	-8387	265
1275	G289	-8403	148
1276	G291	-8419	265
1277	G293	-8435	148
1278	G295	-8451	265
1279	G297	-8467	148
1280	G299	-8483	265
1281	G301	-8499	148
1282	G303	-8515	265
1283	G305	-8531	148
1284	G307	-8547	265
1285	G309	-8563	148
1286	G311	-8579	265
1287	G313	-8595	148
1288	G315	-8611	265
1289	G317	-8627	148
1290	G319	-8643	265
1291	DUMMY27	-8659	148

5. Pin Function

Table 2 Interface

<table>
<tr><th>Signal</th><th>I/O</th><th>Connect to</th><th>Function</th><th>When not in use</th></tr>
<tr><td>IM3-1,
IM0/ID</td><td>I</td><td>IOGND or
IOVCC</td><td>Select a mode to interface to an MPU. In serial interface operation, the IM0 pin is used to set the ID bit of device code.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0 /ID</th><th>Interface Mode</th><th>DB Pin</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80-system 16-bit interface</td><td>DB17-10, DB8-1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80-system 8-bit interface</td><td>DB17-10</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>(ID)</td><td>Clock synchronous serial interface</td><td>-</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>9-bit 3 wires Serial Peripheral Interface</td><td>SDA, SCL, nCS</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>8-bit 4 wires Serial Peripheral Interface</td><td>SDA, SCL, nCS, RS(D/CX)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80-system 18-bit interface</td><td>DB17-0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80-system 9-bit interface</td><td>DB17-9</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td>Setting disabled</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>Setting disabled</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>Setting disabled</td><td>-</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>Setting disabled</td><td>-</td></tr>
</table></td><td>-</td></tr>
<tr><td>nCS</td><td>I</td><td>MPU</td><td>Chip select signal. Amplitude: IOVCC-IOGND
Low: the RM68050 is selected and accessible
High: the RM68050 is not selected and not accessible.</td><td>IOGND</td></tr>
<tr><td>RS</td><td>I</td><td>MPU</td><td>Register select signal. Amplitude: IOVCC-IOGND
Low: select Index or status register
High: select control register
Fix to either IOVCC or DGND when not in use</td><td>IOVCC</td></tr>
<tr><td>nWR/SCL</td><td>I</td><td>MPU</td><td>Write strobe signal in 80-system bus interface operation and enables write operation when nWR is low. Synchronous clock signal (SCL) in serial interface operation.
Amplitude: IOVCC-IOGND</td><td>IOVCC</td></tr>
<tr><td>nRD</td><td>I</td><td>MPU</td><td>Read strobe signal in 80-system bus interface operation and enables read operation when nRD is low.</td><td>IOVCC</td></tr>
</table>

			Amplitude: IOVCC-IOGND	
SDI/SDA	I/O	MPU	Serial data input (SDI) pin in serial interface operation. The data is inputted and latched on the rising edge of the SCL signal. In the 8/9-bit SPI, this pis is a bi-directional data pin. Amplitude: IOVCC-IOGND	IOGND or IOVCC
SDO	I	MPU	Serial data output (SDO) pin in serial interface operation. The data is outputted on the falling edge of the SCL signal. Amplitude: IOVCC-IOGND	Open
DB0-DB17	I/O	MPU	18-bit parallel bi-directional data bus for 80-system interface operation. Amplitude: IOVCC-IOGND. 8-bit I/F: DB17-DB10 are used. 9-bit I/F: DB17-DB9 are used. 16-bit I/F: DB17-DB10 and DB8-DB1 are used. 18-bit I/F: DB17-DB0 are used. 18-bit parallel bi-directional data bus for RGB interface operation. Amplitude: IOVCC-IOGND. 6-bit I/F: DB17-DB12 are used. 16-bit I/F: DB17-DB13 and DB11-DB1 are used. 18-bit I/F: DB17-DB0 are used. Unused pins must be fixed to IOGND level.	IOGND or IOVCC
ENABLE	I	MPU	Data enable signal for RGB interface operation. Amplitude: IOVCC-IOGND. Low: accessible (select) High: Not accessible (Not select) The polarity of ENABLE signal can be inverted by setting the EPL bit.	IOGND or IOVCC
VSYNC	I	MPU	Frame synchronous signal for RGB interface operation.. Amplitude: IOVCC-IOGND. VSPL = “0”: Active low. VSPL = “1”: Active high.	IOGND or IOVCC
HSYNC	I	MPU	Line synchronous signal for RGB interface operation. Amplitude: IOVCC-IOGND. HSPL = “0”: Active low. HSPL = “1”: Active high.	IOGND or IOVCC
DOTCLK	I	MPU	Dot clock signal for RGB interface operation. The data input timing is on the rising edge of DOTCLK. Amplitude: IOVCC-IOGND. DPL = “0”: Input data on the rising edge of DOTCLK	IOGND or IOVCC

			DPL = “1”: Input data on the falling edge of DOTCLK	
FMARK	I	MPU	Frame head pulse signal, which is used when writing data to the internal RAM. (Amplitude: IOVCC-IOGND).	Open

Table 3 Reset, RC oscillation

Signal	I/O	Connect to	Function	When not in use
nRESET	I	MPU	Reset signal. Initializes the RM68050 when it is low. Make sure to execute a power-on reset when turning on power supply. Amplitude: IOVCC-IOGND.	IOGND or IOVCC

Table 4 Power supply

Signal	I/O	Connect to	Function	When not in use
GND	I	Power supply	GND for the analog side: GND = 0V.	-
VDDD	O	Stabilizing Capacitor	Internal logic regulator output, which is used as the power supply to internal logic. Connect a stabilizing capacitor.	-
IOVCC	I	Power supply	Power supply to the interface pins: IM[3:0], nRESET, nCS, WR, nRD, RS, DB17-0, VSYNC, HSYNC, DOTCLK, ENABLE, SCL, SDI, and SDO. IOVCC = 1.65V ~ 3.3V. VCC ≥ IOVCC. In case of COG, connect to VCC on the FPC if IOVCC=VCC, to prevent noise.	-

Table 5 Step-up circuit

Signal	I/O	Connect to	Function	When not in use
VCI	I	Power supply	Power supply to the liquid crystal power supply analog circuit. Connect to an external power supply of 2.5V ~ 3.3V.	-
VCI1	O	Stabilizing Capacitor	An internal reference voltage for the step-up circuit1.The amplitude between VCI and DGND is determined by the VC[2:0] bits. Make sure to set the VCI1 voltage so that the DDVDH, VGH and VGL voltages are set within the respective specification.	-
DDVDH	O	Stabilizing Capacitor	Power supply for the source driver liquid crystal drive unit and VCOM drive. DDVDH = 4.5V ~ 6.0V	-
VGH	O	Stabilizing Capacitor	Liquid crystal gate driver power supply.	-
VGL	O	Stabilizing Capacitor	Liquid crystal gate driver power supply.	-
VCL	O	Stabilizing Capacitor	VCOML drive power supply. Make sure to connect to stabilizing capacitor. VCL = 0.5V ~ -VCI	-
C11+, C11- C12+, C12-	I O	Step-up capacitor	Capacitor connection pins for the step-up circuit 1.	-
C13+, C13- C21+, C21- C22+, C22-	I O	Step-up capacitor	Capacitor connection pins for the step-up circuit 2.	-
VREG1 OUT	O	Stabilizing Capacitor	Output voltage generated from the reference voltage. The voltage level is set with the VRH bits. VREG1OUT is (1) a source driver grayscale reference voltage, (2)VcomH level reference voltage, and (3) Vcom amplitude reference voltage. Connect to a stabilizing capacitor. VREG1OUT = 3.0 ~ (DDVDH – 0.5)V.	Open

Table 6 LCD drive

Signal	I/O	Connect to	Function	When not in use
VCOM	O	TFT panel common electrode	Power supply to TFT panel's common electrode. VCOM alternates between VCOMH and VCOML. The alternating cycle is set by internal register.	Open
VCOMH	O	Stabilizing Capacitor	The High level of VCOM amplitude. Connect to a stabilizing capacitor.	Open
VCOML	O	Stabilizing Capacitor	The Low level of VCOM amplitude. Adjust the VCOML level with the VDV bits. Make sure to connect to stabilizing capacitor.	Open
VGS	I	GND or external resistor	Reference level for the grayscale voltage generating circuit. The VGS level can be changed by connecting to an external resistor.	-
S1~S720	O	LCD	Liquid crystal application voltages. To change the shift direction of segment signal output, set the SS bit as follows. When SS = 0, the data in the RAM address h00000 is outputted from S1. When SS = 1, the data in the RAM address h00000 is outputted from S720.	Open
G1~G320	O	LCD	Gate line output signals. VGH: gate line select level VGL: gate line non-select level	Open

Table 7 Brightness control

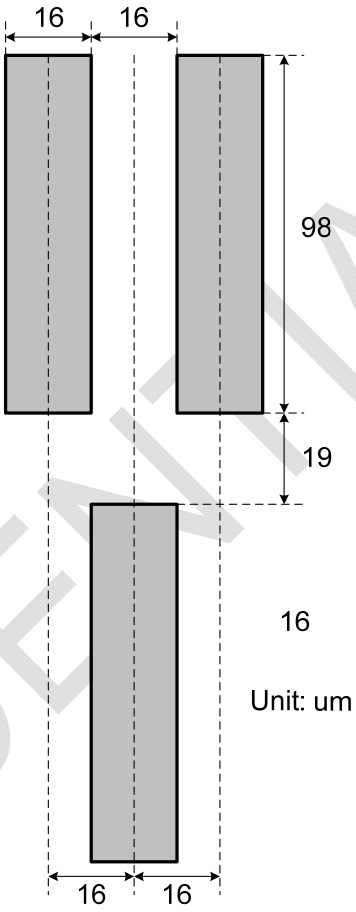
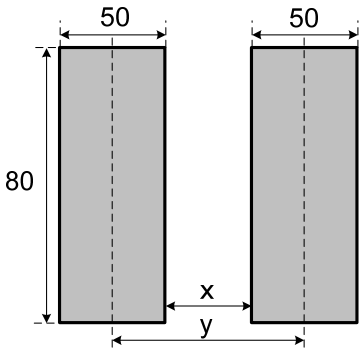
Signal	I/O	Connect to	Function	When not in use
LEDPWM	O	VCI	PWM signal output to control LED driver for LED brightness dimming	Open
LEDON	O	VCI	LED driver control pin to turn on/off the LED backlight	Open

Table 8 Others (test, dummy pins)

Signal	I/O	Connect to	Function	When not in use
DUMMY1-15 DUMMY20-27	-	-	Dummy pad. Leave these pins as open.	-
IOGNDDUM	O	GND	GND pin.	-

TESTO3-16	O	Open	Test pins. Leave them open.	Open
TEST1, 2, 3	I	Open	Test pins (internal pull low). Connect to GND or leave these pins as open.	IOGND
TS8-0	I	Open	Test pins (internal pull low). Leave them open.	Open

6. Bump Arrangement

Pad	Arrangement
S1 ~ S720 **G1 ~ G320** **DUMMY20 ~ 27** **(No. 244 ~ 1291)**	
I/O Pads **(No. 1 ~ 243)**	x=20,30,35 y=70,80,85 

7. Function Description

7.1 System Interface

The RM68050 supports 80-system high-speed interface via 8-, 9-, 16-, 18-bit parallel ports and a clock synchronous serial interface. The interface is selected by setting the IM3-0 pins.

The RM68050 has a 16-bit index register (IR), an 18-bit write-data register (WDR), and an 18-bit read-data register (RDR). The IR is the register to store index information about control register and internal GRAM. The WDR is the register to temporarily store data to be written to control register and internal GRAM. The RDR is the register to temporarily store the data read from the GRAM. The data from the MPU to be written to the internal GRAM is first written to the WDR and then automatically written to the internal GRAM in internal operation. The data is read via RDR from the internal GRAM. Therefore, invalid data is sent to the data bus when the RM68030 performs the first read operation from the internal GRAM. Valid data is read out when the RM68030 performs the second and subsequent read operation.

The instruction execution time except that of starting oscillation takes 0 clock cycle to allow writing instructions consecutively.

Table 9 Register Selection (80-system 8/9/16/18-bit Parallel Interface)

nWR	nRD	RS	Function
0	1	0	Write index to IR
1	0	0	Setting disabled
0	1	1	Write to control register or internal GRAM via WDR
1	0	1	Read from internal GRAM and register via RDR

Table 10 Register Selection (Clock synchronous serial interface)

Start byte		
R/W	RS	Function
0	0	Write index to IR
1	0	Setting disabled
0	1	Write to control register or internal GRAM via WDR
1	1	Read from internal GRAM and register via RDR

Table 11 IM Bit Settings and System Interface

IM3	IM2	IM1	IM0	System interface	DB pins	RAM write data	Instruction write transfer
0	0	0	0	Setting disabled	-	-	-
0	0	0	1	Setting disabled	-	-	-
0	0	1	0	80-system 16-bit interface	DB17-10, DB8-1	Single transfer (16 bits) 2 transfers (1st: 2 bits, 2nd: 16 bits) 2 transfers (1st: 16 bits, 2nd: 2 bits)	Single transfer (16 bits)
0	0	1	1	80-system 8-bit interface	DB17-10	2 transfers (1st: 8 bits, 2nd: 8 bits) 3 transfers (1st: 6 bits, 2nd: 6 bits, 3rd: 6 bits)	2 transfers (1st: 8 bits, 2nd: 8 bits)
0	1	0	*	Clock synchronous serial interface	(SDI, SDO)	2 transfers (1st: 8 bits, 2nd: 8 bits)	2 transfers (1st: 8 bits, 2nd: 8 bits)
0	1	1	0	9-bit 3-wire SPI	SDA, SCL, nCS	2 transfers (1st: 8 bits, 2nd: 8 bits) 3 transfers (1st: 6 bits, 2nd: 6 bits, 3rd: 6 bits)	Single transfer (8 bits)
0	1	1	1	8-bit 4-wire SPI	SDA, SCL, nCS, RS(D/CX)	2 transfers (1st: 8 bits, 2nd: 8 bits) 3 transfers (1st: 6 bits, 2nd: 6 bits, 3rd: 6 bits)	Single transfer (8 bits)
1	0	0	0	Setting disabled	-	-	-
1	0	0	1	Setting disabled	-	-	-
1	0	1	0	80-system 18-bit interface	DB17-0	Single transfer (18 bits)	Single transfer (16 bits)
1	0	1	1	80-system 9-bit interface	DB17-9	2 transfers (1st: 9 bits, 2nd: 9 bits)	2 transfers (1st: 8 bits, 2nd: 8 bits)
1	1	*	*	Setting disabled	-	-	-

7.2 External Display Interface (RGB, VSYNC interfaces)

The RM68050 supports RGB interface and VSYNC interface as the external interface to display moving picture. When the RGB interface is selected, the display operation is synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface operation, data (DB17-0) is written in synchronization with these signals when the polarity of enable signal (ENABLE) allows write operation in order to prevent flicker while updating display data.

In VSYNC interface operation, the display operation is synchronized with the internal clock except frame synchronization, which synchronizes the display operation with the VSYNC signal. The display data is written to the internal GRAM via system interface. When writing data via VSYNC interface, there are constraints in speed and method in writing data to the internal RAM. For details, see the “External Display interface” section.

The RM68050 allows switching interface by instruction according to the still and/or moving pictures display required. Via the RGB interface, the RM68050 writes all display data to the internal GRAM in order to transfer data only when updating the data and thereby reduce the data transfer and power consumption for moving picture display.

7.3 Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the index of the register to set a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As the RM68050 writes data to the internal GRAM, the address in the AC is automatically increased or decreased one step. The window address function enables writing data only within the rectangular area specified in the GRAM.

7.4 Graphics RAM (GRAM)

GRAM is graphics RAM, which can store bit-pattern data of 172,800 (240RGB x 320 x18/8) bytes with 18 bits per pixel.

7.5 Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates liquid crystal driving voltages according to the grayscale data in the γ-correction registers to enable 262k-color display. For details, see the γ-Correction Register section.

7.6 Timing Generator

The timing generator produces timing signals for the operations of internal circuits such as the internal GRAM, source driver, etc. The timing signals for display operations such as RAM read operation and the timing signals for internal operations such as RAM access from the MPU are generated separately in order to avoid mutual interference.

7.7 Oscillator (OSC)

The RM68050 generates the RC oscillation clock by internal RC oscillator circuit. The frame rate is adjusted by the register setting.

7.8 Liquid Crystal Driver Circuit

The liquid crystal driver circuit of the RM68050 consists of a 720-output source driver (S1 ~ S720) and a 320-output gate driver (G1~G320). The display pattern data is latched when 720 bits of data are inputted. The latched data control the source driver and output drive waveforms. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 720-bit source output from the source driver can be changed by setting the SS bit and the shift direction of gate output from the gate driver can be changed by setting the GS bit. The scan mode by the gate driver can be changed by setting the SM bit. Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for each LCD module.

7.9 Internal Logic Power Supply Regulator

The internal logic power supply regulator generates internal logic power supply VDD.

8. GRAM Address Map

Table 12 GRAM address and display position on the panel (SS = 0, BGR = 0)

GS=0		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	.....	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]			.....	WD[17:0]			WD[17:0]			WD[17:0]			WD[17:0]		
G1	G320	h00000			h00001			h00002			h00003			.....	h000EC			h000ED			h000EE			h000EF		
G2	G319	h00100			h00101			h00102			h00103			.....	h001EC			h001ED			h001EE			h001EF		
G3	G318	h00200			h00201			h00202			h00203			.....	h002EC			h002ED			h002EE			h002EF		
G4	G317	H00300			h00301			h00302			h00303			.....	h003EC			h003ED			h003EE			h003EF		
G5	G316	h00400			h00401			h00402			h00403			.....	h004EC			h004ED			h004EE			h004EF		
G6	G315	h00500			h00501			h00502			h00503			.....	h005EC			h005ED			h005EE			h005EF		
G7	G314	h00600			h00601			h00602			h00603			.....	h006EC			h006ED			h006EE			h006EF		
G8	G313	h00700			h00701			h00702			h00703			.....	h007EC			h007ED			h007EE			h007EF		
G9	G312	h00800			h00801			h00802			h00803			.....	h008EC			h008ED			h008EE			h008EF		
G10	G311	h00900			h00901			h00902			h00903			.....	h009EC			h009ED			h009EE			h009EF		
G11	G310	h00A00			h00A01			h00A02			h00A03			.....	h00AEC			h00AED			h00AEE			h00AEF		
G12	G309	h00B00			h00B01			h00B02			h00B03			.....	h00BEC			h00BED			h00BEE			h00BEF		
G13	G308	h00C00			h00C01			h00C02			h00C03			.....	h00CEC			h00CED			h00CEE			h00CEF		
G14	G307	h00D00			h00D01			h00D02			h00D03			.....	h00DEC			h00DED			h00DEE			h00DEF		
G15	G306	h00E00			h00E01			h00E02			h00E03			.....	h00EEC			h00EED			h00EEE			h00EEF		
G16	G305	h00F00			h00F01			h00F02			h00F03			.....	h00FEC			h00FED			h00FEE			h00FEF		
G17	G304	h01000			h01001			h01002			h01003			.....	h010EC			h010ED			h010EE			h010EF		
G18	G303	h01100			h01101			h01102			h01103			.....	h011EC			h011ED			h011EE			h011EF		
G19	G302	h01200			h01201			h01202			h01203			.....	h012EC			h012ED			h012EE			h012EF		
G20	G301	h01300			h01301			h01302			h01303			.....	h013EC			h013ED			h013EE			h013EF		
⋮	⋮	⋮			⋮			⋮			⋮			⋮	⋮			⋮			⋮			⋮		
G305	G16	h13000			h13001			h13002			h13003			.....	h130EC			h130ED			h130EE			h130EF		
G306	G15	h13100			h13101			h13102			h13103			.....	h131EC			h131ED			h131EE			h131EF		
G307	G14	h13200			h13201			h13202			h13203			.....	h132EC			h132ED			h132EE			h132EF		
G308	G13	h13300			h13301			h13302			h13303			.....	h133EC			h133ED			h133EE			h133EF		
G309	G12	h13400			h13401			h13402			h13403			.....	h134EC			h134ED			h134EE			h134EF		
G310	G11	h13500			h13501			h13502			h13503			.....	h135EC			h135ED			h135EE			h135EF		
G311	G10	h13600			h13601			h13602			h13603			.....	h136EC			h136ED			h136EE			h136EF		
G312	G9	h13700			h13701			h13702			h13703			.....	h137EC			h137ED			h137EE			h137EF		
G313	G8	h13800			h13801			h13802			h13803			.....	h138EC			h138ED			h138EE			h138EF		
G314	G7	h13900			h13901			h13902			h13903			.....	h139EC			h139ED			h139EE			h139EF		
G315	G6	h13A00			h13A01			h13A02			h13A03			.....	h13AEC			h13AED			h13AEE			h13AEF		
G316	G5	h13B00			h13B01			h13B02			h13B03			.....	h13BEC			h13BED			h13BEE			h13BEF		
G317	G4	h13C00			h13C01			h13C02			h13C03			.....	h13CEC			h13CED			h13CEE			h13CEF		
G318	G3	h13D00			h13D01			h13D02			h13D03			.....	h13DEC			h13DED			h13DEE			h13DEF		
G319	G2	h13E00			h13E01			h13E02			h13E03			.....	h13EEC			h13EED			h13EEE			h13EEF		
G320	G1	h13F00			h13F01			h13F02			h13F03			.....	h13FEC			h13FED			h13FEE			h13FEF		

Table 13 GRAM address and display position on the panel (SS = 1, BGR = 1)

GS=0		S720 S719 S718	S717 S716 S715	S714 S713 S712	S711 S710 S709	.....	S12 S11 S10	S9 S8 S7	S6 S5 S4	S3 S2 S1
GS=0	GS=1	WD[17:0]	WD[17:0]	WD[17:0]	WD[17:0]	.....	WD[17:0]	WD[17:0]	WD[17:0]	WD[17:0]
G1	G320	h00000	h00001	h00002	h00003	.....	h000EC	h000ED	h000EE	h000EF
G2	G319	h00100	h00101	h00102	h00103	.....	h001EC	h001ED	h001EE	h001EF
G3	G318	h00200	h00201	h00202	h00203	.....	h002EC	h002ED	h002EE	h002EF
G4	G317	H00300	h00301	h00302	h00303	.....	h003EC	h003ED	h003EE	h003EF
G5	G316	h00400	h00401	h00402	h00403	.....	h004EC	h004ED	h004EE	h004EF
G6	G315	h00500	h00501	h00502	h00503	.....	h005EC	h005ED	h005EE	h005EF
G7	G314	h00600	h00601	h00602	h00603	.....	h006EC	h006ED	h006EE	h006EF
G8	G313	h00700	h00701	h00702	h00703	.....	h007EC	h007ED	h007EE	h007EF
G9	G312	h00800	h00801	h00802	h00803	.....	h008EC	h008ED	h008EE	h008EF
G10	G311	h00900	h00901	h00902	h00903	.....	h009EC	h009ED	h009EE	h009EF
G11	G310	h00A00	h00A01	h00A02	h00A03	.....	h00AEC	h00AED	h00AEE	h00AEF
G12	G309	h00B00	h00B01	h00B02	h00B03	.....	h00BEC	h00BED	h00BEE	h00BEF
G13	G308	h00C00	h00C01	h00C02	h00C03	.....	h00CEC	h00CED	h00CEE	h00CEF
G14	G307	h00D00	h00D01	h00D02	h00D03	.....	h00DEC	h00DED	h00DEE	h00DEF
G15	G306	h00E00	h00E01	h00E02	h00E03	.....	h00EEC	h00EED	h00EEE	h00EEF
G16	G305	h00F00	h00F01	h00F02	h00F03	.....	h00FEC	h00FED	h00FEE	h00FEF
G17	G304	h01000	h01001	h01002	h01003	.....	h010EC	h010ED	h010EE	h010EF
G18	G303	h01100	h01101	h01102	h01103	.....	h011EC	h011ED	h011EE	h011EF
G19	G302	h01200	h01201	h01202	h01203	.....	h012EC	h012ED	h012EE	h012EF
G20	G301	h01300	h01301	h01302	h01303	.....	h013EC	h013ED	h013EE	h013EF
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
G305	G16	h13000	h13001	h13002	h13003	.....	h130EC	h130ED	h130EE	h130EF
G306	G15	h13100	h13101	h13102	h13103	.....	h131EC	h131ED	h131EE	h131EF
G307	G14	h13200	h13201	h13202	h13203	.....	h132EC	h132ED	h132EE	h132EF
G308	G13	h13300	h13301	h13302	h13303	.....	h133EC	h133ED	h133EE	h133EF
G309	G12	h13400	h13401	h13402	h13403	.....	h134EC	h134ED	h134EE	h134EF
G310	G11	h13500	h13501	h13502	h13503	.....	h135EC	h135ED	h135EE	h135EF
G311	G10	h13600	h13601	h13602	h13603	.....	h136EC	h136ED	h136EE	h136EF
G312	G9	h13700	h13701	h13702	h13703	.....	h137EC	h137ED	h137EE	h137EF
G313	G8	h13800	h13801	h13802	h13803	.....	h138EC	h138ED	h138EE	h138EF
G314	G7	h13900	h13901	h13902	h13903	.....	h139EC	h139ED	h139EE	h139EF
G315	G6	h13A00	h13A01	h13A02	h13A03	.....	h13AEC	h13AED	h13AEE	h13AEF
G316	G5	h13B00	h13B01	h13B02	h13B03	.....	h13BEC	h13BED	h13BEE	h13BEF
G317	G4	h13C00	h13C01	h13C02	h13C03	.....	h13CEC	h13CED	h13CEE	h13CEF
G318	G3	h13D00	h13D01	h13D02	h13D03	.....	h13DEC	h13DED	h13DEE	h13DEF
G319	G2	h13E00	h13E01	h13E02	h13E03	.....	h13EEC	h13EED	h13EEE	h13EEF
G320	G1	h13F00	h13F01	h13F02	h13F03	.....	h13FEC	h13FED	h13FEE	h13FEF

9. Instruction

9.1 Outline

The RM68050 adopts 18-bit bus architecture in order to interface to high-performance microcomputer in high speed. All the functional blocks of RM68050 starts to work after receiving the correct instruction from the external microprocessor by the 18-, 16-, 9-, 8-bit interface. The index register (IR) stores the register address to which the instructions and display data will be written. The register selection signal (RS), the read/write signals (nRD/nWR) and data bus D17-0 are used to read/write the instructions and data of RM68050. When accessing the RM68050's internal RAM, data is processed in units of 18 bits. The following are the categories of instruction in RM68050.

1. Specify the index of register
2. Display control
3. Power management control
4. Set internal GRAM address
5. Transfer data to and from the internal GRAM
6. γ -correction
7. Window address control
8. Panel display control
9. CABC control

The internal GRAM address is updated automatically as data is written to the internal GRAM, which, in combination with the window address function, contributes to minimizing data transfer and thereby lessens the loading on the microcomputer. The RM68050 writes instructions consecutively by executing the instruction within the cycle when it is written, meanwhile, there is no instruction execution time required.

9.2 Instruction Data Format

The data bus used to transfer 16 instruction bits (IB[15:0]) is different according to the interface format. Make sure to transfer the instruction bits according to the format of the selected interface. For more details, please refer to section of "System Interface".

The following are detail descriptions of instruction bits (IB15-0). Note that the instruction bits IB[15:0] in the following figures are transferred according to the format of the selected interface.

9.3 Index (IR)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the index R00h to RFFh of the control register or RAM control to be accessed using a binary number from “0000_0000” to “1111_1111”. The access to the register and instruction bits in it is prohibited unless the index is specified in the index register.

9.4 ID code (R00h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RO	1	1	0	0	1	0	0	1	1	0	0	1	0	0	1	0	1

9.5 Display control

9.5.1 Driver Output Control (R01h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SS: Sets the shift direction of output from the source driver.

When SS = “0”, the source driver output shift from S1 to S720.

When SS = “1”, the source driver output shift from S720 to S1.

The combination of SS and BGR settings determines the RGB assignment to the source driver pins S1 ~ S720.

When SS = “0” and BGR = “0”, RGB dots are assigned one to one from S1 to S720.

When SS = “1” and BGR = “1”, RGB dots are assigned one to one from S720 to S1.

When changing the SS bit, RAM data must be rewritten.

SM: Controls the scan mode in combination with GS setting. See “Scan mode setting”.

9.5.2 LCD Driving Wave Control (R02h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BC0: Selects the liquid crystal drive waveform VCOM..

BC0 = 0: frame inversion waveform is selected.

BC0 = 1: line inversion waveform is selected.

9.5.3 Entry Mode (R03h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	I//D1	I/D0	AM	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

AM: Sets either horizontal or vertical direction in updating the address counter automatically as the RM68050 writes data to the internal GRAM.
AM = “0”, sets the horizontal direction.
AM = “1”, sets the vertical direction.
When making a window address area, the data is written only within the area in the direction determined by I/D[1:0] and AM.

I/D[1:0]: Either increments or decrements the address counter automatically as the data is written to the GRAM. The I/D[0] bit sets either increment or decrement in horizontal direction (updates the address AD[7:0]). The I/D[1] bit sets either increment or decrement in vertical direction (updates the address AD[8:16]).

ORG: Moves the origin address according to the ID setting when a window address area is made. This function is enabled when writing data within the window address area using high-speed RAM write function. Also see Figure 3 and Figure 4.
ORG = 0: The origin address is not moved. In this case, specify the address to start write operation according to the GRAM address map within the window address area.
ORG = 1: The origin address “h00000” is moved according to the I/D[1:0] setting.

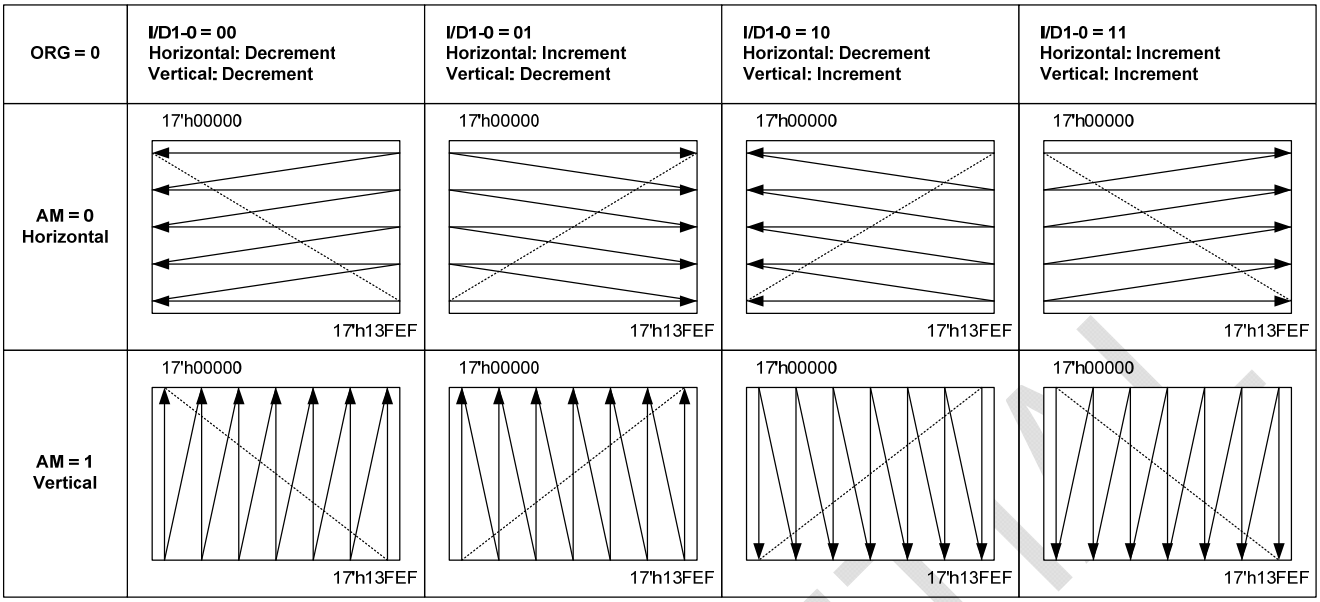


Figure 1 Automatic address update (ORG = 0, AM, ID)

Note: When writing data within the window address area with ORG = 0, any address within the window address area can be designated as the starting point of RAM write operation.

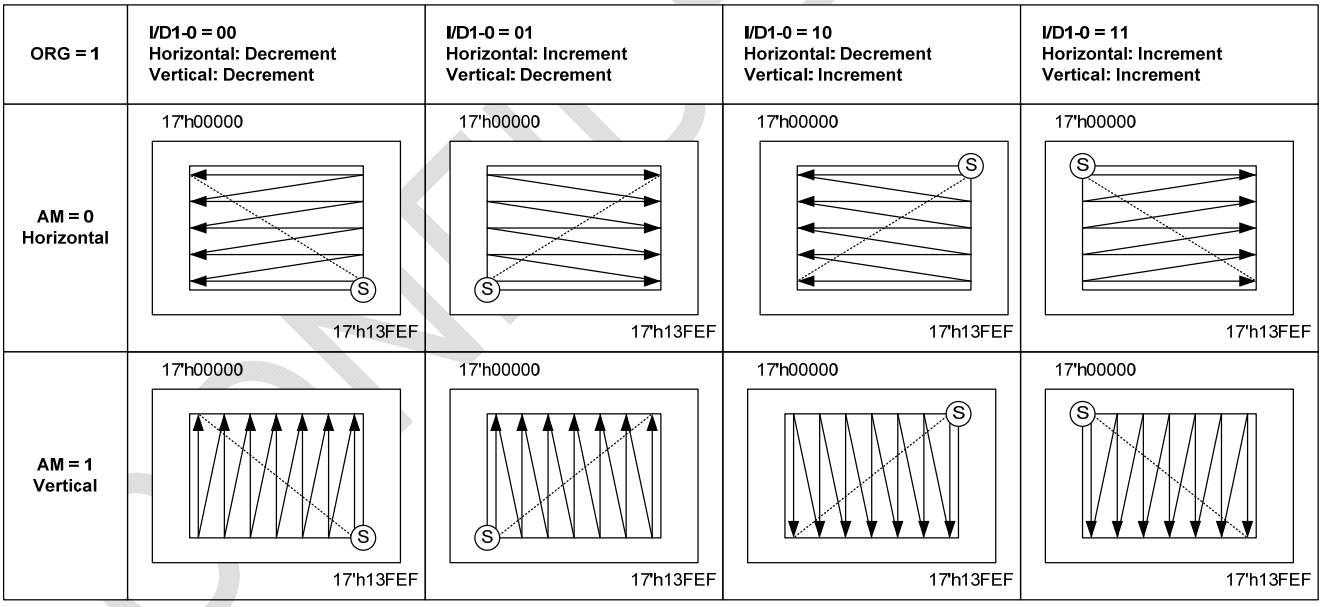


Figure 2 Automatic address update (ORG = 1, AM, ID)

Note: 1. When ORG = 1, make sure to set the address “h00000” in the RAM address set registers (R210h, R21h). Setting other addresses is inhibited. 2. When ORG = 1, the starting point of writing data within the window address area can be set at either corner of the window address area (“S” in circle in the above figure).

BGR: Reverse the order from RGB to BGR in writing 18-bit pixel data in the GRAM.

BGR = 0: Write data in the order of RGB to the GRAM.

BGR = 1: Reverse the order from RGB to BGR in writing data to the GRAM.

BGR = 0

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

BGR = 1

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
B5	B4	B3	B2	B1	B0	G5	G4	G3	G2	G1	G0	R5	R4	R3	R2	R1	R0

DFM: In combination with the TRI setting, sets the format to develop 16-/8-bit data to 18-bit data when using either 16-bit or 8-bit bus interface.

TRI: Selects the format to transfer data bits via 16-bit or 8-bit interface.

In 16-bit bus interface operation,

TRI = 0: 16-bit RAM data is transferred in one transfer.

TRI = 1: 18-bit RAM data is transferred in two transfers.

In 8-bit interface operation,

TRI = 0: 16-bit RAM data is transferred in two transfers.

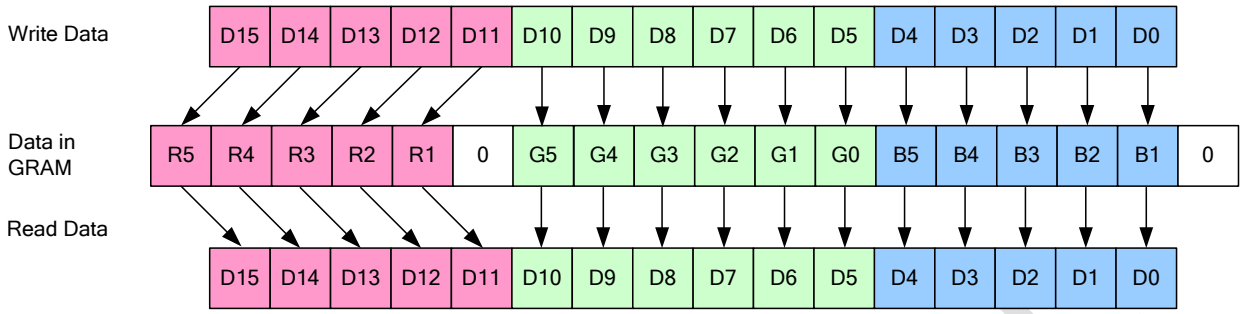
TRI = 1: 18-bit RAM data is transferred in three transfers.

9.5.4 16bits Data Format Selection (R05h)

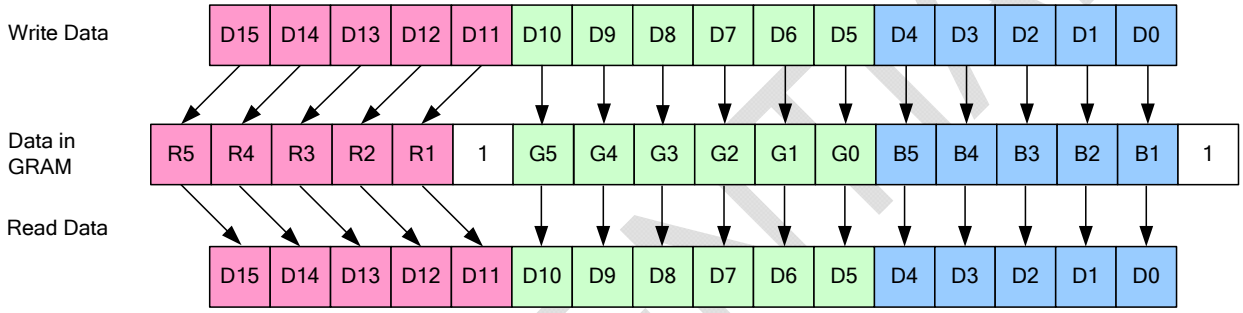
R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FPF1	FPF0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

FPF[1:0]: The extension method for transforming 16bits data format to 18bits data format.

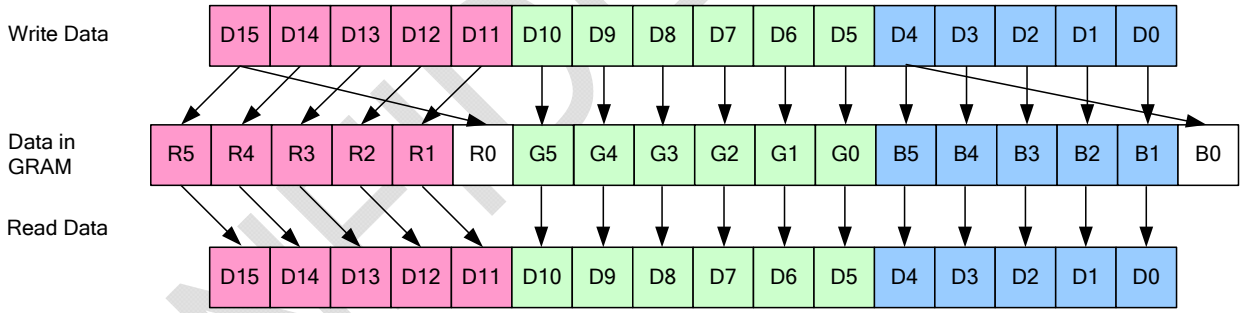
FPF[1:0]=00



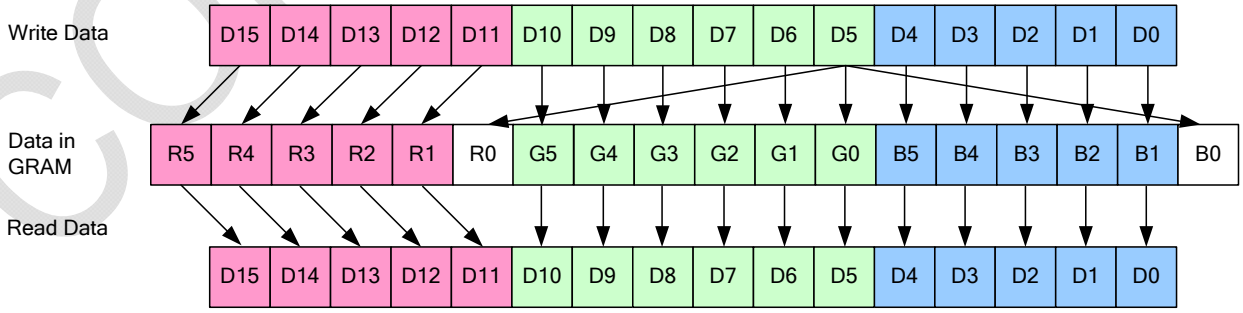
FPF[1:0]=01



FPF[1:0]=10



FPF[1:0]=11



9.5.5 Display Control 1 (R07h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	CL	0	D1	D0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

D[1:0]: A graphics display is turned on when writing D1 = “1”, and is turned off when writing D1 = “0”. When writing D1 = “0”, the graphics display data is retained in the internal GRAM and the RM68050 displays the data when writing D1 = “1”. When D1 = “0”, i.e. while no display is shown on the panel, all source outputs becomes the GND level to reduce charging/discharging current, which is generated within the LCD while driving liquid crystal with AC voltage.

When the display is turned off by setting D1-0 = 2’b01, the RM68050 continues internal display operation. When the display is turned off by setting D1-0 = 2’b00, the RM68050’s internal display operation is halted completely. In combination with the GON, DTE setting, the D[1:0] setting controls display ON/OFF.

D[1:0]	BASEE	Source, VCOM Output	Internal Operation
2’h0	*	GND	Halt
2’h1	*	GND	Operation
2’h2	*	Non-lit display	Operation
2’h3	0	Non-lit display	Operation
	1	Base-image display	Operation

Note:

1. The data write operation from the microcomputer is independent on the D[1:0] setting.
2. The D[1:0] setting is valid on both 1st and 2nd displays
3. The non-lit display level from the source output pins is determined by instruction (PTS).

CL: When CL = 1, the RM68050 displays in 8-colors with low power consumption.

CL	Display color
0	262,144
1	8

GON, DTE: The combination of GON and DTE settings set the output level form gate lines (G1 ~ G320).

GON	DTE	G1~G320 Gate Output
0	0	VGH
0	1	VGH
1	0	VGL
1	1	Normal display

BASEE: Base image display enable bit.

BASEE = 0: No base image is displayed. The RM68050 drives liquid crystal with non-lit display level or drives only partial image display areas.

BASEE = 1: A base image is displayed on the screen.

The D[1:0] setting has precedence over the BASEE setting.

PTDE[1:0]: PTDE[0] is the display enable bit of partial image 1. PTDE[1] is the display enable bit of partial image 2. When PTDE1/0 = 0, the partial image is turned off and only base image is displayed on the screen.

When PTDE1/0 = 1, the partial image is displayed on the screen. In this case, turn off the base image by setting BASEE = 0.

9.5.6 Display Control 2 (R08h)

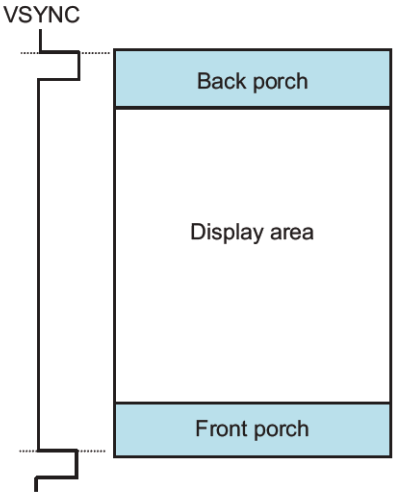
R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
Default		0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

FP [3:0] / BP [3:0]: Sets the number of lines for a front porch period / back porch period (a blank period following the end of display / (a blank period made before the beginning of display).

In external display interface operation, a back porch (BP) period starts on the falling edge of the VSYNC signal and the display operation starts after the back porch period. A blank period will start after a front porch (FP) period and it will continue until next VSYNC input is detected.

Internal clock operation mode	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP ≤ 16 lines
RGB interface operation	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP ≤ 16 lines
VSYNC interface operation	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP = 16 lines

FP[3:0] BP[3:0]	Front and Back Porch period (Line periods)
4'h0	Setting disabled
4'h1	Setting disabled
4'h2	2 lines
4'h3	3 lines
4'h4	4 lines
4'h5	5 lines
4'h6	6 lines
4'h7	7 lines
4'h8	8 lines
4'h9	9 lines
4'hA	10 lines
4'hB	11 lines
4'hC	12 lines
4'hD	13 lines
4'hE	14 lines
4'hF	Setting disabled



Note : The output timing to the LCD panel is delayed by two line periods from the synchronous signal (VSYNC) input timing.

9.5.7 Display Control 3 (R09h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC 2	ISC 1	ISC 0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

ISC [3:0]: Set the scan cycle when setting PTG[1:0]=”10” to selects interval scan. The scan cycle is defined by from 0 to 31 as table below. The polarity is inverted in the same timing every interval scan cycle.

ISC[3:0]	Scan cycle	Time for interval when (f_{FLM}) = 60Hz
4’h1	0 frames	-
4’h2	0 frames	-
4’h3	3 frames	50 ms
4’h4	5 frames	84 ms
4’h5	7 frames	117 ms
4’h6	9 frames	150 ms
4’h7	11 frames	184 ms
4’h8	13 frames	217 ms
4’h9	15 frames	251 ms
4’hA	19 frames	317 ms
4’hB	21 frames	351 ms
4’hC	23 frames	384 ms
4’hD	25 frames	418 ms
4’hE	27 frames	451 ms
4’hF	29 frames	484 ms

PTG[1:0]: Sets the scan mode in non-display area. The scan mode selected by PTG[1:0] bits is applied in the non-display area when the base image is turned off and the non-display area other than the first and second partial display areas.

PTG1	PTG0	Gate in non-display area	Source in non-display area	VCOM output
0	0	Normal scan	PTS[2:0] setting	VCOMH/VCOML
0	1	Setting disabled	-	-
1	0	Interval scan	PTS[2:0] setting	VCOMH/VCOML
1	1	Setting disabled	-	-

PTS[2:0]: Sets the source output level in non-display area drive period. When PTS[2] = 1, the operation of amplifiers which generates the grayscales other than V0 and V63 are halted and the step-up clock frequency becomes half the normal frequency in order to reduce power consumption.

PTS[1:0]	Source / VCOM output in non-display area	
	Frame with gate scan	Frame without gate scan
2’h0	White	V63 / VCOML
2’h1	Black	V0 / VCOML
2’h2	White	GND / GND
2’h3	White	Hi-Z / Hi-Z

9.5.8 Display Control 4 (R0Ah)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMI[2:0]: Sets the output interval of FMARK signal according to the display data rewrite cycle and data transfer rate.

FMARKOE: When FMARKOE = 1, the RM68050 starts outputting FMARK signal from the FMARK pin in the output interval set by FMI[2:0] bits.

FMI[2]	FMI[1]	FMI[0]	FMARK output interval
0	0	0	1 frame
0	0	1	2 frames
0	1	1	4 frames
1	0	1	6 frames
Other settings			Setting disabled

9.5.9 External Display Interface Control 1 (R0Ch)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	ENC2	ENC1	ENC0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM 0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RIM[1:0]: Sets the interface format in RGB interface.

RIM[1:0]	RGB interface operation	Display color
2'h0	18-bit RGB interface (1 transfer/pixel) via DB17-0	262,144
2'h1	16-bit RGB interface (1 transfer/pixel) via DB17-13 and DB 11-1	65,536
2'h2	6-bit RGB interface (3 transfers/pixel) via DB17-12	262,144
2'h3	Setting disabled	-

Note:

1. Instruction bits are set via system interface.
2. Transfer the RGB dot data one by one in synchronization with DOTCLK in 6-bit RGB interface operation.

DM[1:0]: Selects the interface for the display operation. The DM[1:0] setting allows switching between internal clock operation mode and external display interface operation mode. However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.

DM[1:0]	Display Interface
2'h0	Internal clock operations
2'h1	RGB interface
2'h2	VSYNC interface
2'h3	Setting disabled

RM: Selects the interface for RAM access operation. RAM access is possible only via the interface selected by the RM bit. Set RM = 1 when writing display data via RGB interface. When RM = 0, it is possible to write data via system interface while performing display operation via RGB interface.

RM	RAM Access Interface
0	System interface / VSYNC interface
1	RGB interface

ENC[2:0]: Sets the RAM write cycle via RGB interface.

ENC[2:0]	RAM Write Cycle (frame periods)
3'h0	1 frame
3'h1	2 frames
3'h2	3 frames
3'h3	4 frames
3'h4	5 frames
3'h5	6 frames
3'h6	7 frames
3'h7	8 frames

9.5.10 Frame Marker Position (R0Dh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FMP[8:0]: Sets the output position of frame cycle signal (frame marker). When FMP[8:0] = 9'h000, a high-active pulse FMARK is outputted at the start of back porch period for 1H period .

Make sure the setting restriction 9'h000 ≤ FMP ≤ BP+NL+FP.

FMP[8:0]	FMARK output position
9'h000	0
9'h001	1st line
9'h002	2nd line
…	…
9'h175	373rd line
9'h176	374th line
9'h177	375th line

9.5.11 External Display Interface Control 2 (R0Fh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DPL: Sets the signal polarity of DOTCLK pin.

DPL = 0: input data on the rising edge of DOTCLK

DPL = 1: input data on the falling edge of DOTCLK

EPL: Sets the signal polarity of ENABLE pin.

EPL = 0: writes data DB17-0 when ENABLE = “0” and disables data write operation when ENABLE = “1”.

EPL = 1: writes data DB17-0 when ENABLE = “1” and disables data write operation when ENABLE = “0”.

HSPL: Sets the signal polarity of HSYNC pin.

HSPL = 0: low active

HSPL = 1: high active

VSPL: Sets the signal polarity of VSYNC pin.

VSPL = 0: low active

VSPL = 1: high active

9.6 Power Control

9.6.1 Power Control 1 (R10h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	SAP	0	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	0	SLP	STB
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SLP: When SLP = 1, the RM68050 enters the sleep mode. In sleep mode, the internal display operation except RC oscillation is halted to reduce power consumption. In the sleep mode, the GRAM data and instructions cannot be updated except the following instruction, Exit sleep mode (SLP = “0”).

STB: When STB = 1, the RM68050 enters the standby mode and the display operation stops except the GRAM power supply to reduce the power consumption. In the standby mode, the GRAM data and instructions cannot be updated except the following instruction, Exit standby mode (STB = “0”).

AP[2:0]: Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit. The larger constant current enhances the drivability of the LCD, but it also increases the current consumption. Adjust the constant current taking the trade-off into account between the display quality and the current consumption. In no-display period, set AP[2:0] = 3’h0 to halt the operational amplifier circuits and the step-up circuits to reduce current consumption.

AP[2:0]	Gamma driver amplifiers	Source driver amplifiers
3’h0	Halt operation	Halt operation
3’h1	1.00	1.00
3’h2	1.00	0.75
3’h3	1.00	0.50
3’h4	0.75	1.00
3’h5	0.75	0.75
3’h6	0.75	0.50
3’h7	0.50	0.50

APE: Power supply enable bit.

Set APE = “1” to start the generation of power supply according to the power supply startup sequence.

SAP: Source Driver output control. SAP=0, Source driver is disabled. SAP=1, Source driver is enabled. When starting the charge-pump of LCD in the Power ON stage, make sure that SAP=0, and set the SAP=1, after starting up the LCD power supply circuit.

BT[2:0]: Sets the factor used in the step-up circuits. Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.

BT[2:0]	DDVDH	VCL	VGH	VGL
3’h0	VCI1 x 2	-VCI1	VCI1 x 6	-VCI1 x 5
3’h1				-VCI1 x 4
3’h2				-VCI1 x 3
3’h3			VCI1 x 5	-VCI1 x 5
3’h4				-VCI1 x 4
3’h5				-VCI1 x 3
3’h6			VCI1 x 4	-VCI1 x 4
3’h7				-VCI1 x 3

Notes:

1. Connect capacitors where required when using DDVDH, VGH, VGL and VCL voltages.
2. Set the following voltages within the respective ranges:

   DDVDH = 6.0V (max.)

9.6.2 Power Control 2 (R11h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
Default		0	0	0	0	0	1	1	1	0	1	1	1	0	0	0	0

DC0[2:0] / DC1[2:0]: Selects the operating frequency of the step-up circuit 1 / step-up circuit 2. The higher step-up operating frequency enhances the drivability of the step-up circuit and the quality of display but increases the current consumption. Adjust the frequency taking the trade-off between the display quality and the current consumption into account.

DC0[2:0]	Step-up circuit 1: step-up frequency (f_{DCDC1})
3’h0	fbclk
3’h1	fbclk / 2
3’h2	fbclk / 4
3’h3	fbclk / 8
3’h4	fbclk / 16
3’h5	fbclk / 32
3’h6	fbclk / 64
3’h7	Halt Step-up circuit 1

DC1[2:0]	Step-up circuit 2: step-up frequency (f_{DCDC2})
3’h0	fbclk / 4
3’h1	fbclk / 8
3’h2	fbclk / 16
3’h3	fbclk / 32
3’h4	fbclk / 64
3’h5	fbclk / 128
3’h6	fbclk / 256
3’h7	Halt Step-up circuit 2

Note: Make sure the DC0, DC1 setting restriction: $f_{DCDC1} \geq f_{DCDC2}$. “fbclk” is a clock for boost circuit.

9.6.3 Power Control 3 (R12h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	VCIRE	0	0	0	VRH3	VRH2	VRH1	VRH0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VCIRE: Select the external reference voltage VCI or internal reference voltage VCIR.

VCIRE = 0	External reference voltage VCI (**default**)
VCIRE =1	Internal reference voltage 2.5V

VRH[3:0]: Sets the factor to generate VREG1OUT from VCI.

	VCIRE=0	**VCIRE=1**
VRH[3:0]	**VREG1OUT Voltage**	**VREG1OUT Voltage**
4'h0	Halt	Halt
4'h1	VCI x 2.00	2.5V x 2.00 = 5.000V
4'h2	VCI x 2.05	2.5V x 2.05 = 5.125V
4'h3	VCI x 2.10	2.5V x 2.10 = 5.250V
4'h4	VCI x 2.20	2.5V x 2.20 = 5.500V
4'h5	VCI x 2.30	2.5V x 2.30 = 5.750V
4'h6	VCI x 2.40	2.5V x 2.40 = 6.000V
4'h7	VCI x 2.40	2.5V x 2.40 = 6.000V
4'h8	VCI x 1.60	2.5V x 1.60 = 4.000V
4'h9	VCI x 1.65	2.5V x 1.65 = 4.125V
4'hA	VCI x 1.70	2.5V x 1.70 = 4.250V
4'hB	VCI x 1.75	2.5V x 1.75 = 4.375V
4'hC	VCI x 1.80	2.5V x 1.80 = 4.500V
4'hD	VCI x 1.85	2.5V x 1.85 = 4.625V
4'hE	VCI x 1.90	2.5V x 1.90 = 4.750V
4'hF	VCI x 1.95	2.5V x 1.95 = 4.875V

Notes:

1. Make sure the VC and VRH setting restrictions: VREG1OUT ≦ (DDVDH-0.5)V.
2. When VCI<2.5V, internal reference voltage will be same as VCI.

9.6.4 Power Control 4 (R13h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	VDV4	VDV 3	VDV 2	VDV 1	VDV 0	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VDV[4:0]: Select the factor of VREG1OUT to set the amplitude of VCOM alternating voltage from 0.70 to 1.24 xVREG1OUT

VDV[4:0]	VCOM Amplitude	VDV[4:0]	VCOM Amplitude
5'h0	VREG1OUT x 0.70	5'h10	VREG1OUT x 0.94
5'h1	VREG1OUT x 0.72	5'h11	VREG1OUT x 0.96
5'h2	VREG1OUT x 0.74	5'h12	VREG1OUT x 0.98
5'h3	VREG1OUT x 0.76	5'h13	VREG1OUT x 1.00
5'h4	VREG1OUT x 0.78	5'h14	VREG1OUT x 1.02
5'h5	VREG1OUT x 0.80	5'h15	VREG1OUT x 1.04
5'h6	VREG1OUT x 0.82	5'h16	VREG1OUT x 1.06
5'h7	VREG1OUT x 0.84	5'h17	VREG1OUT x 1.08
5'h8	VREG1OUT x 0.86	5'h18	VREG1OUT x 1.10
5'h9	VREG1OUT x 0.88	5'h19	VREG1OUT x 1.12
5'hA	VREG1OUT x 0.90	5'h1A	VREG1OUT x 1.14
5'hB	VREG1OUT x 0.92	5'h1B	VREG1OUT x 1.16
5'hC	VREG1OUT x 0.94	5'h1C	VREG1OUT x 1.18
5'hD	VREG1OUT x 0.96	5'h1D	VREG1OUT x 1.20
5'hE	VREG1OUT x 0.98	5'h1E	VREG1OUT x 1.22
5'hF	VREG1OUT x 1.00	5'h1F	VREG1OUT x 1.24

9.7 RAM Access Instruction

9.7.1 RAM Address Set (Horizontal Address) (R20h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

9.7.2 RAM Address Set (Vertical Address) (R21h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AD[16:0]: A GRAM address set initially in the AC (Address Counter). The address in the AC is automatically updated according to the combination of AM, I/D[1:0] settings as the RM68050 writes data to the internal GRAM so that data can be written consecutively without resetting the address in the AC. The address is not automatically updated when reading data from the internal GRAM.

Note: In RGB interface operation (RM = "1"), the address AD16-0 is set in the address counter every frame on the falling edge of VSYNC.

AD[16:0]	GRAM Data Setting
17'h00000 ~ 17'h000EF	Bitmap data on the 1st line
17'h00100 ~ 17'h001EF	Bitmap data on the 2nd line
17'h00200 ~ 17'h002EF	Bitmap data on the 3rd line
17'h00300 ~ 17'h003EF	Bitmap data on the 4th line
17'h00400 ~ 17'h004EF	Bitmap data on the 5th line
..	..
17'h13C00 ~ 17'h13CEF	Bitmap data on the 317th line
17'h13D00 ~ 17'h13DEF	Bitmap data on the 318th line
17'h13E00 ~ 17'h13EEF	Bitmap data on the 319th line
17'h13F00 ~ 17'h13FEF	Bitmap data on the 320th line

9.7.3 Write Data to GRAM (R22h)

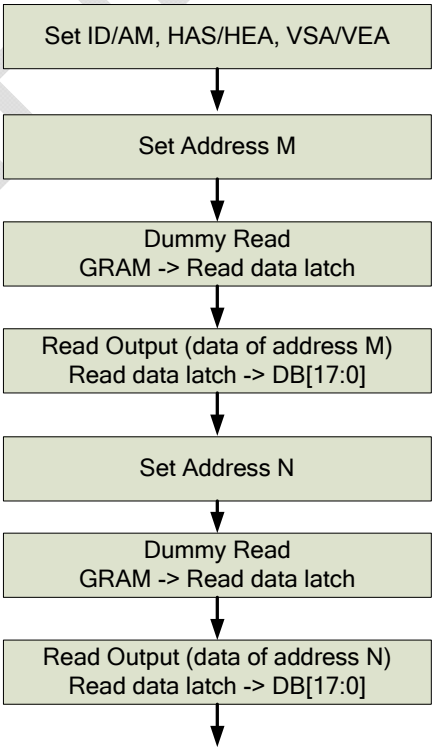
R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	RAM write data WD[17:0] is transferred via different data bus in different interface operation.															

This register is the GRAM access port. When update the display data through this register, the address counter (AC) is increased/decreased automatically.

9.7.4 Read Data from GRAM (R22h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	RAM read data RD[17:0] is transferred via different data bus in different interface operation.															

Read 18-bit data from GRAM through the read data register (RDR).



9.8 Power Control 7 (R29h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VCM [5:0]: Set internal VCOMH voltages.

VCM1[5:0]	VCOMH Voltage
6'h00	VREG1OUT x 0.685
6'h01	VREG1OUT x 0.690
6'h02	VREG1OUT x 0.695
6'h03	VREG1OUT x 0.700
6'h04	VREG1OUT x 0.705
6'h05	VREG1OUT x 0.710
6'h06	VREG1OUT x 0.715
6'h07	VREG1OUT x 0.720
6'h08	VREG1OUT x 0.725
6'h09	VREG1OUT x 0.730
6'h0A	VREG1OUT x 0.735
6'h0B	VREG1OUT x 0.740
6'h0C	VREG1OUT x 0.745
6'h0D	VREG1OUT x 0.750
6'h0E	VREG1OUT x 0.755
6'h0F	VREG1OUT x 0.760
6'h10	VREG1OUT x 0.765
6'h11	VREG1OUT x 0.770
6'h12	VREG1OUT x 0.775
6'h13	VREG1OUT x 0.780
6'h14	VREG1OUT x 0.785
6'h15	VREG1OUT x 0.790
6'h16	VREG1OUT x 0.795
6'h17	VREG1OUT x 0.800
6'h18	VREG1OUT x 0.805
6'h19	VREG1OUT x 0.810
6'h1A	VREG1OUT x 0.815
6'h1B	VREG1OUT x 0.820
6'h1C	VREG1OUT x 0.825
6'h1D	VREG1OUT x 0.830
6'h1E	VREG1OUT x 0.835
6'h1F	VREG1OUT x 0.840

VCM1[5:0]	VCOMH Voltage
6'h20	VREG1OUT x 0.845
6'h21	VREG1OUT x 0.850
6'h22	VREG1OUT x 0.855
6'h23	VREG1OUT x 0.860
6'h24	VREG1OUT x 0.865
6'h25	VREG1OUT x 0.870
6'h26	VREG1OUT x 0.875
6'h27	VREG1OUT x 0.880
6'h28	VREG1OUT x 0.885
6'h29	VREG1OUT x 0.890
6'h2A	VREG1OUT x 0.895
6'h2B	VREG1OUT x 0.900
6'h2C	VREG1OUT x 0.905
6'h2D	VREG1OUT x 0.910
6'h2E	VREG1OUT x 0.915
6'h2F	VREG1OUT x 0.920
6'h30	VREG1OUT x 0.925
6'h31	VREG1OUT x 0.930
6'h32	VREG1OUT x 0.935
6'h33	VREG1OUT x 0.940
6'h34	VREG1OUT x 0.945
6'h35	VREG1OUT x 0.950
6'h36	VREG1OUT x 0.955
6'h37	VREG1OUT x 0.960
6'h38	VREG1OUT x 0.965
6'h39	VREG1OUT x 0.970
6'h3A	VREG1OUT x 0.975
6'h3B	VREG1OUT x 0.980
6'h3C	VREG1OUT x 0.985
6'h3D	VREG1OUT x 0.990
6'h3E	VREG1OUT x 0.995
6'h3F	VREG1OUT x 1.000

9.9 Frame Rate and Color Control (R2Bh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	FRS2	FRS2	FRS1	FRS0
Default		0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

FRS[4:0] Set the frame rate when the internal resistor is used for oscillator circuit.

FRS[3:0]	Frame Rate	FRS[3:0]	Frame Rate
0000	30	1000	51
0001	31	1001	56
0010	33	1010	62
0011	35	1011	70 (default)
0100	38	1100	83
0101	40	1101	93
0110	43	1110	Setting Prohibited
0111	47	1111	Setting Prohibited

9.10 γ Control

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R30h	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
R31h	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
R32h	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP1[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
R35h	W	1	0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[1]	RP0[0]
R36h	W	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	VRP0[4]	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
R37h	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
R38h	W	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
R39h	W	1	0	0	0	0	0	KN5[2]	KN5[1]	KN1[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
R3Ch	W	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]
R3Dh	W	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	VRN0[4]	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]

KP5-0[2:0] / KN5-0[2:0] : γ Fine Adjustment Register for positive/negative polarity

PRP1-0[2:0] / PRN1-0[2:0] : γ Gradient Adjustment Register for positive/negative polarity

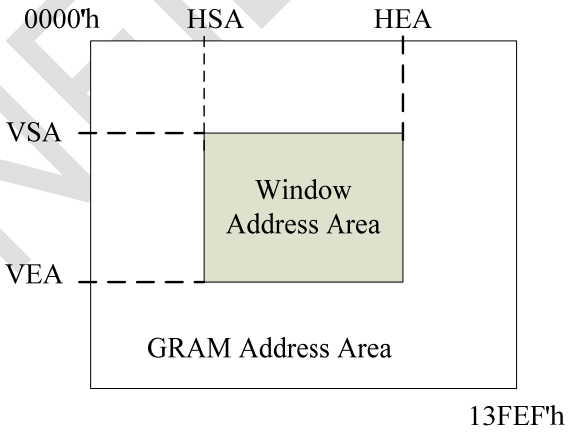
VRP1-0[4:0] / VRN1-0[4:0]: γ Amplitude Adjustment Register for positive/negative polarity

9.11 Window Address Write Control Instruction

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R50h	W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
R51h	W	1	0	0	0	0	0	0	0	0	HEA7	HSA6	HSA5	HEA4	HEA3	HEA2	HEA1	HEA0
R52h	W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
R53h	W	1	0	0	0	0	0	0	0	VEA8	VEA7	VSA6	VSA5	VEA4	VEA3	VEA2	VEA1	VEA0
R50h	Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R51h			0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R52h			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R53h			0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1

HSA[7:0], HEA[7:0]: HSA[7:0] and HEA[7:0] are the start and end addresses of the window address area in horizontal direction, respectively. HSA[7:0] and HEA[7:0] specify the horizontal range to write data. Set HSA[7:0] and HEA[7:0] before starting RAM write operation. In setting, make sure that 8'h00 ≤ HAS < HEA ≤ 8'hEF and 8'h01 ≤ HEA – HSA.

VSA[8:0], VEA[8:0]: VSA[8:0] and VEA[8:0] are the start and end addresses of the window address area in vertical direction, respectively. VSA[8:0] and VEA[8:0] specify the vertical range to write data. Set VSA[8:0] and VEA[8:0] before starting RAM write operation. In setting, make sure that 9'h000 ≤ VSA < VEA ≤ 9'h13F.



Note: The window address range must be within the GRAM address space.

9.12 Base Image Display Control Instruction

	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R60h	W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0

R61h	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
R6Ah	W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
R60h	Default		0	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0
R61h			0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1
R6Ah			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

REV: Enables the grayscale inversion of the image by setting REV = 1. This enables the RM68050 to display the same image from the same set of data whether the liquid crystal panel is normally black or white. The source output level during front, back porch periods and blank periods is determined by register setting (PTS).

REV	GRAM Data	Source Output Level in Display Area	
		Positive Polarity	Negative Polarity
0	18'h00000	V63	V0
	…	…	…
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	…	…	…
	18'h3FFFF	V63	V0

VLE: Vertical scroll display enable bit. When VLE = 1, the RM68050 starts displaying the base image from the line (of the physical display) determined by VL[8:0] bits. VL[8:0] sets the amount of scrolling, which is the number of lines to shift the start line of the display from the first line of the physical display. Note that the partial image display position is not affected by the base image scrolling.

The vertical scrolling is not available in external display interface operation. In this case, make sure to set VLE = "0".

VLE	Base Image
0	Fixed
1	Enable scrolling

NL[5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL[5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL[5:0]	Number of Lines	NL[5:0]	Number of Lines	NL[5:0]	Number of Lines
6'h00	8 (lines)	6'h0E	112	6'h1C	232
6'h01	16	6'h0F	120	6'h1D	240
6'h02	24	6'h10	128	6'h1E	248
6'h03	32	6'h11	136	6'h1F	256
6'h04	40	6'h12	144	6'h20	264
6'h05	48	6'h13	152	6'h21	272
6'h06	48	6'h14	160	6'h22	280
6'h07	56	6'h15	168	6'h23	288
6'h08	64	6'h16	176	6'h24	296
6'h09	72	6'h17	184	6'h25	304
6'h0A	80	6'h18	192	6'h26	312

6'h0B	88	6'h19	200	6'h27	320
6'h0C	96	6'h1A	216	Others	Setting inhibited
6'h0D	104	6'h1B	224		

SCN[5:0]: Specifies the gate line where the gate driver starts scan.

SCN[5:0]	Gate Line No (Scan start position)			
	SM=0		SM=1	
	GS=0	GS=1	GS=0	GS=1
6'h00	G1	G320	G1	G320
6'h01	G9	G312	G17	G304
6'h02	G17	G304	G33	G288
6'h03	G25	G296	G49	G272
6'h04	G33	G288	G65	G256
6'h05	G41	G280	G81	G240
6'h06	G49	G272	G97	G224
6'h07	G57	G264	G113	G208
6'h08	G65	G256	G129	G192
6'h09	G73	G248	G145	G176
6'h0A	G81	G240	G161	G160
6'h0B	G89	G232	G177	G144
6'h0C	G97	G224	G193	G128
6'h0D	G105	G216	G209	G112
6'h0E	G113	G208	G225	G96
6'h0F	G121	G200	G241	G80
6'h10	G129	G192	G257	G64
6'h11	G137	G184	G273	G48
6'h12	G145	G176	G289	G32
6'h13	G153	G168	G305	G16
6'h14	G161	G160	G2	G319
6'h15	G169	G152	G18	G303
6'h16	G177	G144	G34	G287
6'h17	G185	G136	G50	G271
6'h18	G193	G128	G66	G255
6'h19	G201	G120	G82	G239
6'h1A	G209	G112	G98	G223
6'h1B	G217	G104	G114	G207
6'h1C	G225	G96	G130	G191
6'h1D	G233	G88	G146	G175
6'h1E	G241	G80	G162	G159
6'h1F	G249	G72	G178	G143
6'h20	G257	G64	G194	G127
6'h21	G265	G56	G210	G111
6'h22	G273	G48	G226	G95
6'h23	G281	G40	G242	G79
6'h24	G289	G32	G258	G63
6'h25	G297	G24	G274	G47
6'h26	G305	G16	G290	G31
6'h27	G313	G8	G306	G15
6'h28~6'h3F	Setting disabled	Setting disabled	Setting disabled	Setting disabled

NDL: Sets the source output level in non-lit display area. NDL bit can keep the non-display area lit on.

NDL	Non-display area	
	Positive	Negative

0	V63	V0
1	V0	V63

VL[8:0]: Sets the amount of scrolling of the base image. The base image is scrolled in vertical direction and displayed from the line which is determined by VL[8:0]. Make sure VL[8:0] ≤ 320.

GS: Sets the direction of scan by the gate driver. Set GS bit in combination with SM and SS bits for the convenience of the display module configuration and the display direction.

9.13 SPI Read/Write Control (R66h, Write Only)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/WX
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

This register controls the read/write function when 3-wire or 4-wire SPI interface is used. If the read function needs to be active, R/WX has to be set to ‘1’. Otherwise, it is ‘0’.

R/WX	Function
0	Register write mode
1	Register readd mode

9.14 Partial Display Control Instruction

9.14.1 Partial Image 1: Display Position (R80h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTDP0[8]	PTDP0[7]	PTDP0[6]	PTDP0[5]	PTDP0[4]	PTDP0[3]	PTDP0[2]	PTDP0[1]	PTDP0[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

9.14.2 Partial Image 1: RAM Address (Start Line Address) (R81h), (End Line Address) (R82h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTSA0[8]	PTSA0[7]	PTSA0[6]	PTSA0[5]	PTSA0[4]	PTSA0[3]	PTSA0[2]	PTSA0[1]	PTSA0[0]
W	1	0	0	0	0	0	0	0	PTEA0[8]	PTEA0[7]	PTEA0[6]	PTEA0[5]	PTEA0[4]	PTEA0[3]	PTEA0[2]	PTEA0[1]	PTEA0[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

9.14.3 Partial Image 2: Display Position (R83h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTDP1[8]	PTDP1[7]	PTDP1[6]	PTDP1[5]	PTDP1[4]	PTDP1[3]	PTDP1[2]	PTDP1[1]	PTDP1[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

9.14.4 Partial Image 2: RAM Address (Start Line Address) (R84h), (End Line Address) (R85h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	PTSA1[8]	PTSA1[7]	PTSA1[6]	PTSA1[5]	PTSA1[4]	PTSA1[3]	PTSA1[2]	PTSA1[1]	PTSA1[0]
W	1	0	0	0	0	0	0	0	PTEA1[8]	PTEA1[7]	PTEA1[6]	PTEA1[5]	PTEA1[4]	PTEA1[3]	PTEA1[2]	PTEA1[1]	PTEA1[0]
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PTDP0[8:0]: Sets the display position of partial image 1.

PTDP1[8:0]: Sets the display position of partial image 2.

PTSA0[8:0] and PTEA0[8:0]: Sets the start line and end line addresses of the RAM area, respectively for the partial image 1. In setting, make sure that PTSA0 ≤ PTEA0.

PTSA1[8:0] and PTEA1[8:0]: Sets the start line and end line addresses of the RAM area, respectively for the partial image 2. In setting, make sure that PTSA1 ≤ PTEA1.

9.15 Panel Interface Control Instruction

9.15.1 Panel Interface Control 1 (R90h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	DIVI1	DIVI0	0	0	0	RTNI4	RTNI3	RTNI2	RTNI1	RTNI0
Default		0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

RTNI[4:0]: Sets 1H (line) period. This setting is enabled while the RM68050's display operation is synchronized with internal clock.

DIVI[1:0]: Sets the division ratio of the internal clock frequency.

Frame Frequency Calculation

$$Frame\ frequency = \frac{fosc}{Clocks\ per\ line \times division\ ratio \times (line + BP + FP)}\ [Hz]$$

fosc : RC oscillation frequency
Line : Number of lines to drive the LCD (NL bits)
Division ratio : DIVI
Clocks per line : RTNI

DIVI[1:0]	Division Ratio	Internal operation clock unit
2'h0	1/1	1 OSC
2'h1	1/2	2 OSC
2'h2	1/4	4 OSC
2'h3	1/8	8 OSC

RTNI[4:0]	Clocks per line
5'h00~5'h0F	Setting inhibited
5'h10	16 clocks
5'h11	17 clocks
5'h12	18 clocks
5'h13	19 clocks
5'h14	20 clocks

RTNI[4:0]	Clocks per line
5'h15	21 clocks
5'h16	22 clocks
5'h17	23 clocks
5'h18	24 clocks
5'h19	25 clocks
5'h1A	26 clocks

RTNI[4:0]	Clocks per line
5'h1B	27 clocks
5'h1C	28 clocks
5'h1D	29 clocks
5'h1E	30 clocks
5'h1F	31 clocks

9.15.2 Panel Interface Control 2 (R92h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	NOWI[2]	NOWI[1]	NOWI[0]	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0

NOWI[2:0]: Sets the non-overlap period of adjacent gate outputs. The setting is enabled in display operation synchronizing with the internal clock.

NOWI[2:0]	Non-overlap period
3'h0	Setting inhibited
3'h1	1 (internal clock)
3'h2	2
3'h3	3

NOWI[2:0]	Non-overlap period
3'h4	4
3'h5	5
3'h6	6
3'h7	Setting inhibited

Note: The internal clock is the frequency divided clock, which is set by DIVI[[1:0] bits.

9.15.3 Panel Interface Control 4 (R95h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

DIVE[1:0]: Sets the division ratio of DOTCLK when RM68050 display operation is synchronized with RGB interface signals.

DIVE[1:0]	Division Ratio	Internal operation clock unit (DOTCLK)			
		18-bit, 1 transfer RGB interface	DOTCLK = 5 MHz	8-bit, 3 transfer RGB interface	DOTCLK = 15 MHz
2'h0	Setting inhibited	Setting inhibited	-	Setting inhibited	-
2'h1	1/4	4 DOTCLKs	0.8 us	12 DOTCLKs	0.8 us
2'h2	1/8	8 DOTCLKs	1.6 us	24 DOTCLKs	1.6 us
2'h3	1/16	16 DOTCLKs	3.2 us	48 DOTCLKs	3.2 us

9.15.4 Panel Interface Control 5 (R97h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	NOWE[3]	NOWE[2]	NOWE[1]	NOWE[0]	0	0	0	0	0	0	0	0
Default		0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

NOWE[3:0]: Sets the non-overlap period of adjacent gate outputs. The setting is enabled in display operation via RGB interface.

NOWE[3:0]	Non-overlap period
4'h0	Setting inhibited
4'h1	1 (clocks)
4'h2	2
4'h3	3
4'h4	4
4'h5	5
4'h6	6
4'h7	7

NOWE[3:0]	Non-overlap period
4'h8	8
4'h9	9
4'hA	10
4'hB	11
4'hC	12
4'hD	13
4'hE	14
4'hF	15

Note: 1 clock = (Number of data transfers/pixel) x DIVE (division ratio) [DOTCLK].

9.16 OTP VCM Control

9.16.1 OTP VCM Programming Control 1 (RA1h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	OTP_PGM_EN	0	0	0	0	0	VCM_ OTP5	VCM_ OTP4	VCM_ OTP3	VCM_ OTP2	VCM_ OTP1	VCM_ OTP0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

OTP_PGM_EN: OTP programming enable. When program OTP, must set this bit.

OTP data can be programmed 3 times.

VCM_OTP[5:0]: OTP programming data for VCOMH voltage, the voltage refer to VCM[5:0] value.

9.16.2 OTP VCM Status and Enable (RA2h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	PGM_ CNT1	PGM_ CNT0	VCM_ D5	VCM _D4	VCM _D3	VCM _D2	VCM _D1	VCM _D0	0	0	0	0	0	0	0	VCM_ EN
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PGM_CNT[1:0]: OTP programmed record. These bits are read only.

OTP_PGM_CNT[1:0]	Description
2'h0	OTP clean
2'h1	OTP programmed 1 time
2'h2	OTP programmed 2 times
2'h3	OTP programmed 3 times

VCM_D[5:0]: OTP VCM data read value. These bits are read only.

VCM_EN: OTP VCM data enable.

VCM_EN=1: Set this bit to enable OTP VCM data to replace R29h VCM value.

VCM_EN=0: Default value, use R29h VCM value.

9.16.3 OTP VCM Programming ID Key (RA5h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	KEY 15	KEY 14	KEY 13	KEY 12	KEY 11	KEY 10	KEY 9	KEY 8	KEY 7	KEY 6	KEY 5	KEY 4	KEY 3	KEY 2	KEY 1	KEY 0
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

KEY[15:0]: OTP Programming ID key protection. Before writing OTP programming data RA1h, it must write RA5h with 0xAA55 value first to make OTP programming successfully. If RA5h is not written with 0xAA55, OTP programming will be fail. See OTP Programming flow.

9.17 CABC control

9.17.1 Write Display Brightness Value (RB1h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0

This command is used to adjust the brightness value of the display.

DBV[7:0]: control the brightness of manual setting or CABC in RM68050. The PWM output signal, LEDPWM, controls the LED driver IC to decide the display brightness

9.17.2 Read Display Brightness Value (RB2h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	0	0	0	0	0	0	0	0	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0

This command is used to return the brightness value of the display.

DBV[7:0] is reset when display is in sleep-in mode.

DBV[7:0] is ‘0’ when bit BCTRL of “Write CTRL Display (B3h)” command is ‘0’.

DBV[7:0] is manual set brightness specified with “Write CTRL Display (B3h)” command when BCTRL bit is ‘1’.

When bit BCTRL of “Write CTRL Display (B3h)” command is ‘1’ and C1/C0 bit of “Write Content Adaptive Brightness Control (B5h)” command are ‘0’, DBV[7:0] output is the brightness value specified with “Write Display Brightness (B1h)” command.

9.17.3 Write CTRL Display Value (RB3h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	BCTRL	0	DD	BL	0	0

This command is used to set the brightness control mechanism.

BCTRL: Brightness control block on/off. This bit is always used to switch brightness for display.

BCTRL	Description
0	Brightness Control Block OFF (DBV[7:0]=00H)
1	Brightness Control Block ON (DBV[7:0] is active)

DD: Display Dimming Control.

DD	Description
0	Display Dimming OFF
1	Display Dimming ON

BL: Backlight Control.

BL	Description
0	Backlight Control OFF
1	Backlight Control ON

Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 → 1 or 1→ 0.

When BL bit change from “On” to “Off”, backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected

9.17.4 Read CTRL Display Value (RB4h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	0	0	0	0	0	0	0	0	0	0	BCTRL	0	DD	BL	0	0

This command is used to read the status of the brightness control mechanism.

9.17.5 Write Content Adaptive Brightness Control Value (RB5h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C[1]	C[0]

This command is used to set parameters for image content based adaptive brightness control functionality. There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

C[1:0]	Description
2’h0	CABC OFF
2’h1	User Interface Image
2’h2	Still Picture
2’h3	Moving Image

9.17.6 Read Content Adaptive Brightness Control Value (RB6h)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C[1]	C[0]

This command is used to read the status for image content based adaptive brightness control functionality.

9.17.7 Write CABC Minimum Brightness (RBEh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	CMB[7]	CMB[6]	CMB[5]	CMB[4]	CMB[3]	CMB[2]	CMB[1]	CMB[0]

This command is used to set the minimum brightness value of the display for CABC function.

CMB[7:0]: CABC minimum brightness control, this parameter is used to avoid too much brightness reduction.

When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed. This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (BCTRL=0 of “Write CTRL Display (B3h)”), CABC minimum brightness setting is ignored.

In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.

9.17.8 Read CABC Minimum Brightness (RBFh)

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R	1	0	0	0	0	0	0	0	0	CMB[7]	CMB[6]	CMB[5]	CMB[4]	CMB[3]	CMB[2]	CMB[1]	CMB[0]

This command is used to read the minimum brightness value of the display for CABC function.

9.18 Deep standby control

R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSTB
Default		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DSTB: When DSTB = 1, the RM68050 enters the deep standby mode. In deep standby mode, the internal logic power supply is turned off to reduce power consumption. The GRAM data and instruction setting are not kept when the RM68050 enters the deep standby mode, and they would be reset automatically after exiting deep standby mode.

To exit deep standby mode, nCS pin needs to be toggled from low to high 6 times.

10. Instruction List

No.	Register Name	R/W	RS	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
IR	Index Register	W	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
00h	Driver Code Read	RO	1	1	0	0	1	0	0	1	1	0	0	1	0	0	1	0	1
01h	Driver Output Control 1	W	1	0	0	0	0	0	SM	0	SS	0	0	0	0	0	0	0	0
02h	LCD Driving Control	W	1	0	0	0	0	0	0	B/C	0	0	0	0	0	0	0	0	0
03h	Entry Mode	W	1	TRI	DFM	0	BGR	0	0	0	0	ORG	0	I//D1	I/D0	AM	0	0	0
05h	16 bits data format control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	FPF1	FPF0
07h	Display Control 1	W	1	0	0	PTDE1	PTDE0	0	0	0	BASEE	0	0	GON	DTE	CL	0	D1	D0
08h	Display Control 2	W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0
09h	Display Control 3	W	1	0	0	0	0	0	0	PTS1	PTS0	0	0	PTG1	PTG0	ISC3	ISC2	ISC1	ISC0
0Ah	Display Control 4	W	1	0	0	0	0	0	0	0	0	0	0	0	0	FMARKOE	FMI2	FMI1	FMI0
0Ch	RGB Display Interface Control 1	W	1	0	ENC2	ENC1	ENC0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM 0
0Dh	Frame Maker Position	W	1	0	0	0	0	0	0	0	FMP8	FMP7	FMP6	FMP5	FMP4	FMP3	FMP2	FMP1	FMP0
0Fh	RGB Display Interface Control 2	W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	0	EPL	DPL
10h	Power Control 1	W	1	0	0	0	SAP	0	BT2	BT1	BT0	APE	AP2	AP1	AP0	0	0	SLP	STB
11h	Power Control 2	W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0
12h	Power Control 3	W	1	0	0	0	0	0	0	0	0	VCIRE	0	0	0	VRH3	VRH2	VRH1	VRH0
13h	Power Control 4	W	1	0	0	0	VDV4	VDV 3	VDV 2	VDV 1	VDV 0	0	0	0	0	0	0	0	0
20h	Horizontal GRAM Address Set	W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
21h	Vertical GRAM Address Set	W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8
22h	Write Data to GRAM	RAM write data WD[17:0] / read data RD[17:0] is transferred via different data bus in different interface operation.																	

29h	Power Control 7	W	1	0	0	0	0	0	0	0	0	0	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
2Bh	Frame Rate and Color Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	FRS2	FRS2	FRS1	FRS0
30h	Gamma Control 1	W	1	0	0	0	0	0	KP1[2]	KP1[1]	KP1[0]	0	0	0	0	0	KP0[2]	KP0[1]	KP0[0]
31h	Gamma Control 2	W	1	0	0	0	0	0	KP3[2]	KP3[1]	KP3[0]	0	0	0	0	0	KP2[2]	KP2[1]	KP2[0]
32h	Gamma Control 3	W	1	0	0	0	0	0	KP5[2]	KP5[1]	KP1[0]	0	0	0	0	0	KP4[2]	KP4[1]	KP4[0]
35h	Gamma Control 4	W	1	0	0	0	0	0	RP1[2]	RP1[1]	RP1[0]	0	0	0	0	0	RP0[2]	RP0[1]	RP0[0]
36h	Gamma Control 5	W	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	VRP0[4]	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
37h	Gamma Control 6	W	1	0	0	0	0	0	KN1[2]	KN1[1]	KN1[0]	0	0	0	0	0	KN0[2]	KN0[1]	KN0[0]
38h	Gamma Control 7	W	1	0	0	0	0	0	KN3[2]	KN3[1]	KN3[0]	0	0	0	0	0	KN2[2]	KN2[1]	KN2[0]
39h	Gamma Control 8	W	1	0	0	0	0	0	KN5[2]	KN5[1]	KN1[0]	0	0	0	0	0	KN4[2]	KN4[1]	KN4[0]
3Ch	Gamma Control 9	W	1	0	0	0	0	0	RN1[2]	RN1[1]	RN1[0]	0	0	0	0	0	RN0[2]	RN0[1]	RN0[0]
3Dh	Gamma Control 10	W	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	VRN0[4]	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]
50h	Horizontal Address Start Position	W	1	0	0	0	0	0	0	0	0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
51h	Horizontal Address End Position	W	1	0	0	0	0	0	0	0	0	HEA7	HSA6	HSA5	HEA4	HEA3	HEA2	HEA1	HEA0
52h	Vertical Address Start Position	W	1	0	0	0	0	0	0	0	VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0
53h	Vertical Address End Position	W	1	0	0	0	0	0	0	0	VEA8	VEA7	VSA6	VSA5	VEA4	VEA3	VEA2	VEA1	VEA0
60h	Driver Output Control 2	W	1	GS	0	NL5	NL4	NL3	NL2	NL1	NL0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
61h	Base Image Display Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	NDL	VLE	REV
66h	SPI Read/Write Control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/WX
6Ah	Vertical Scroll Control	W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
80h	Partial Image 1 Display Position	W	1	0	0	0	0	0	0	0	PTDP0[8]	PTDP0[7]	PTDP0[6]	PTDP0[5]	PTDP0[4]	PTDP0[3]	PTDP0[2]	PTDP0[1]	PTDP0[0]
81h	Partial Image 1 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA0[8]	PTSA0[7]	PTSA0[6]	PTSA0[5]	PTSA0[4]	PTSA0[3]	PTSA0[2]	PTSA0[1]	PTSA0[0]
82h	Partial Image 1 Area (End Line)	W	1	0	0	0	0	0	0	0	PTEA0[8]	PTEA0[7]	PTEA0[6]	PTEA0[5]	PTEA0[4]	PTEA0[3]	PTEA0[2]	PTEA0[1]	PTEA0[0]
83h	Partial Image 2 Display Position	W	1	0	0	0	0	0	0	0	PTDP1[8]	PTDP1[7]	PTDP1[6]	PTDP1[5]	PTDP1[4]	PTDP1[3]	PTDP1[2]	PTDP1[1]	PTDP1[0]

84h	Partial Image 2 Area (Start Line)	W	1	0	0	0	0	0	0	0	PTSA1[8]	PTSA1[7]	PTSA1[6]	PTSA1[5]	PTSA1[4]	PTSA1[3]	PTSA1[2]	PTSA1[1]	PTSA1[0]
85h	Partial Image 2 Area (End Line	W	1	0	0	0	0	0	0	0	PTEA1[8]	PTEA1[7]	PTEA1[6]	PTEA1[5]	PTEA1[4]	PTEA1[3]	PTEA1[2]	PTEA1[1]	PTEA1[0]
90h	Panel Interface Control 1	W	1	0	0	0	0	0	0	DIVI1	DIVI0	0	0	0	RTNI4	RTNI3	RTNI2	RTNI1	RTNI0
92h	Panel Interface Control 2	W	1	0	0	0	0	0	NOWI[2]	NOWI[1]	NOWI[0]	0	0	0	0	0	0	0	0
95h	Panel Interface Control 4	W	1	0	0	0	0	0	0	DIVE1	DIVE0	0	0	0	0	0	0	0	0
97h	Panel Interface Control 5	W	1	0	0	0	0	NOWE[3]	NOWE[2]	NOWE[1]	NOWE[0]	0	0	0	0	0	0	0	0
A1h	OTP VCM Programming Control	W	1	0	0	0	0	OTP_PGM_EN	0	0	0	0	0	VCM_OTP5	VCM_OTP4	VCM_OTP3	VCM_OTP2	VCM_OTP1	VCM_OTP0
A2h	OTP VCM Status and Enable	W	1	PGM_CNT1	PGM_CNT0	VCM_D5	VCM_D4	VCM_D3	VCM_D2	VCM_D1	VCM_D0	0	0	0	0	0	0	0	VCM_EN
A5h	OTP Programming ID Key	W	1	KEY 15	KEY 14	KEY 13	KEY 12	KEY 11	KEY 10	KEY 9	KEY 8	KEY 7	KEY 6	KEY 5	KEY 4	KEY 3	KEY 2	KEY 1	KEY 0
B1h	Write Display Brightness	W	1	0	0	0	0	0	0	0	0	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0
B2h	Read Display Brightness	R	1	0	0	0	0	0	0	0	0	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0
B3h	Write CTRL Display value	W	1	0	0	0	0	0	0	0	0	0	0	BCTRL	0	DD	BL	0	0
B4h	Read CTRL Display value	R	1	0	0	0	0	0	0	0	0	0	0	BCTRL	0	DD	BL	0	0
B5h	Write Content Adaptive	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C[1]	C[0]
B6h	Brightness Control value	R	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C[1]	C[0]
BEh	Read Content Adaptive	W	1	0	0	0	0	0	0	0	0	CMB[7]	CMB[6]	CMB[5]	CMB[4]	CMB[3]	CMB[2]	CMB[1]	CMB[0]
BFh	Brightness Control value	R	1	0	0	0	0	0	0	0	0	CMB[7]	CMB[6]	CMB[5]	CMB[4]	CMB[3]	CMB[2]	CMB[1]	CMB[0]
E6h	Deep stand by mode control	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSTB

11. Interface and Data Format

The RM68050 supports system interface for making instruction and other settings, and external display interface for displaying a moving picture. The RM68050 can select the optimum interface for the display (moving or still picture) in order to transfer data efficiently.

As external display interface, the RM68050 supports RGB interface and VSYNC interface, which enables data rewrite operation without flicker effect of the moving picture on display.

In RGB interface operation, the display operation is executed in synchronization with synchronous signals VSYNC, HSYNC, and DOTCLK. In synchronization with these signals, the RM68050 writes display data according to data enable signal (ENABLE) via RGB data signal bus (DB17-0). The display data is stored in the RM68050's GRAM so that data is transferred only when rewriting the frames of moving picture and the data transfer required for moving picture display can be minimized. The window address function specifies the RAM area to write data for moving picture display, which enables displaying a moving picture and RAM data in other than the moving picture area simultaneously.

In VSYNC interface operation, the internal display operation is synchronized with the frame synchronization signal (VSYNC). The VSYNC interface enables a moving picture display via system interface by writing the data to the GRAM at faster than the minimum calculated speed in synchronization with the falling edge of VSYNC. In this case, there are restrictions in setting the frequency and the method to write data to the internal RAM.

The RM68050 operates in either one of the following four modes according to the state of the display. The operation mode is set in the external display interface control register (R0Ch). When switching from one mode to another, make sure to follow the relevant sequence in setting instruction bits.

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM)
Internal clock operation (displaying still pictures)	System interface (RM = 0)	Internal clock operation (DM1-0 = 00)
RGB interface (1) (displaying moving pictures)	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
RGB interface (2) (rewriting still pictures while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM1-0 = 01)
VSYNC interface (displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

Notes:

1. Instructions are set only via system interface.
2. The RGB and VSYNC interfaces cannot be used simultaneously.

12. System Interface

The following are the kinds of system interfaces available with the RM68050. The interface operation is selected by setting the IM3/2/1/0 pins. The system interface is used for instruction setting and RAM access.

IM3	IM2	IM1	IM0	Interfacing Mode with MPU	DB pins	Colors
0	0	0	0	Setting inhibited	-	-
0	0	0	1	Setting inhibited	-	-
0	0	1	0	80-system 16-bit interface	DB17-10, DB8-1	262,144
0	0	1	1	80-system 8-bit interface	DB17-10	262,144
0	1	0	ID	Clock synchronous serial interface	(SDI, SDO)	65,536
0	1	1	0	9-bit 3 wires Serial Peripheral Interface	SDA, SCL, nCS	262,144
0	1	1	1	8-bit 4 wires Serial Peripheral Interface	SDA, SCL, nCS, RS(D/CX)	262,144
1	0	0	*	Setting inhibited	-	-
1	0	1	0	80-system 18-bit interface	DB17-0	262,144
1	0	1	1	80-system 9-bit interface	DB17-9	262,144
1	1	*	*	Setting inhibited	-	-

12.1 80-system 18-bit Bus Interface

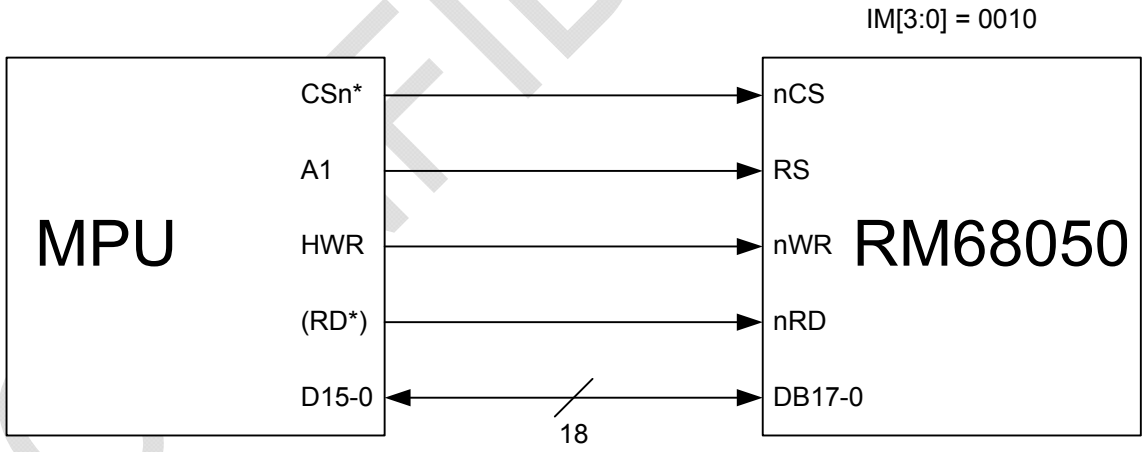


Figure 3 18-bit bus interface for 80-system

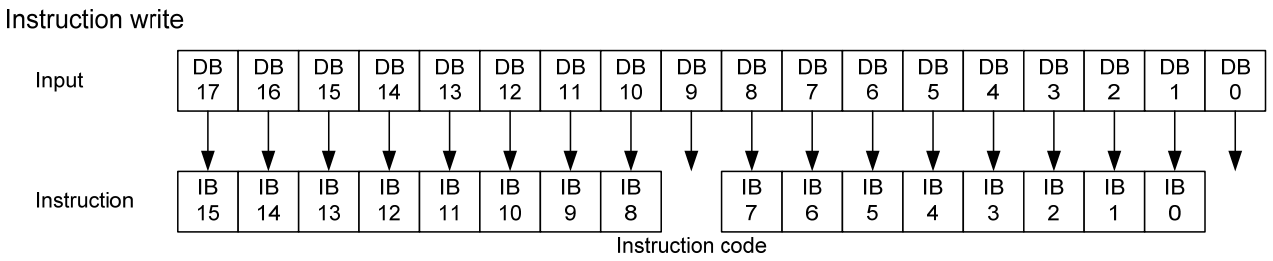


Figure 4 18-bit Interface Data Format (Instruction Write / Instruction Read)

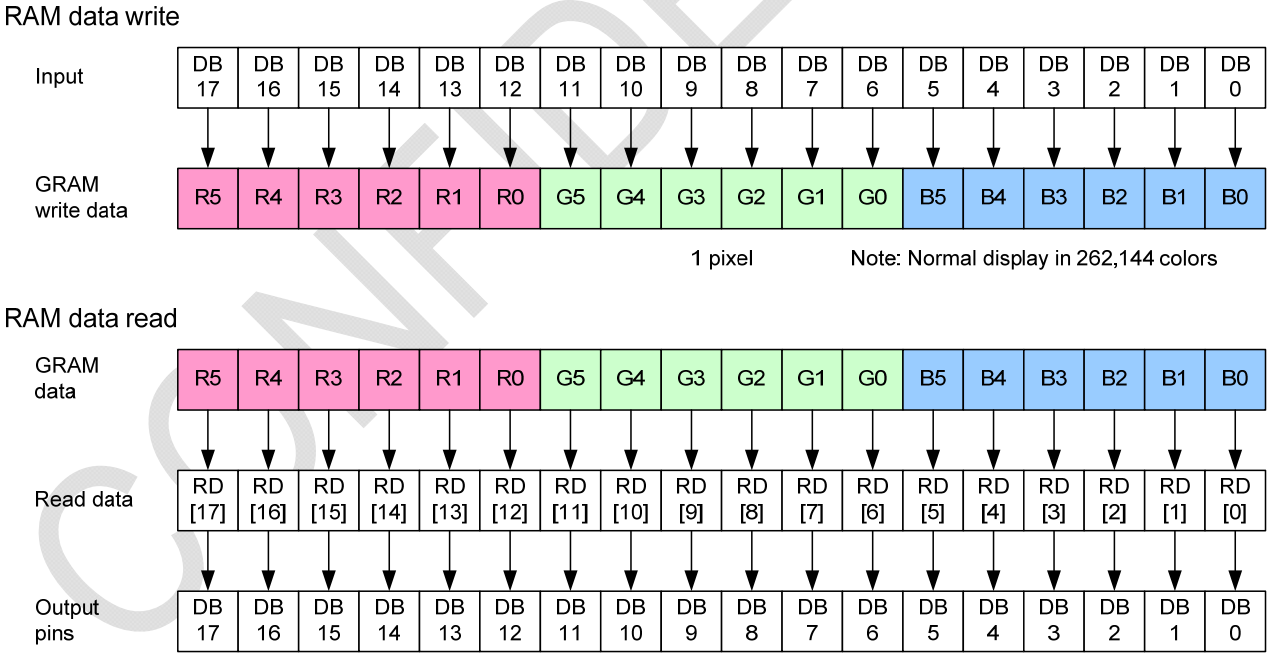


Figure 5 18-bit Interface Data Format (RAM Data Write / RAM Data Read)

12.2 80-system 16-bit Bus Interface

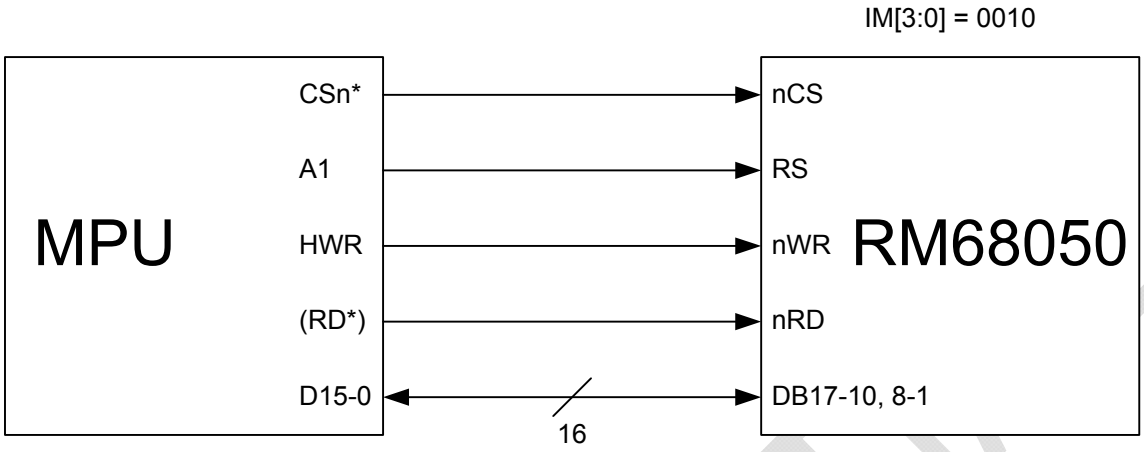


Figure 6 16-bit bus interface for 80-system

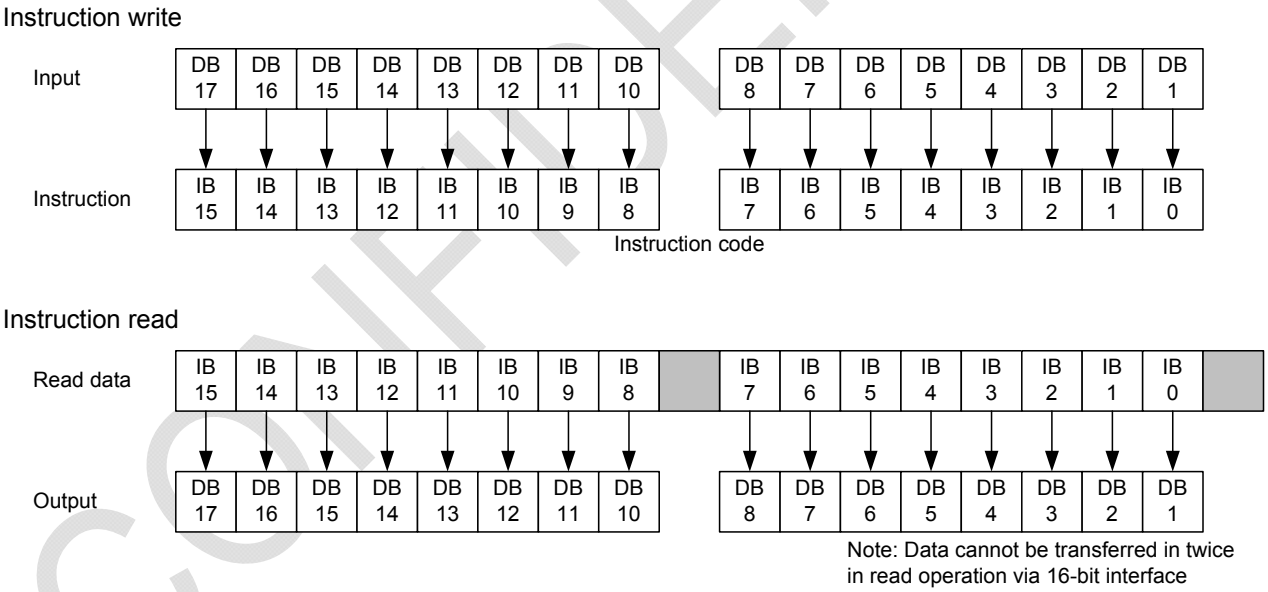
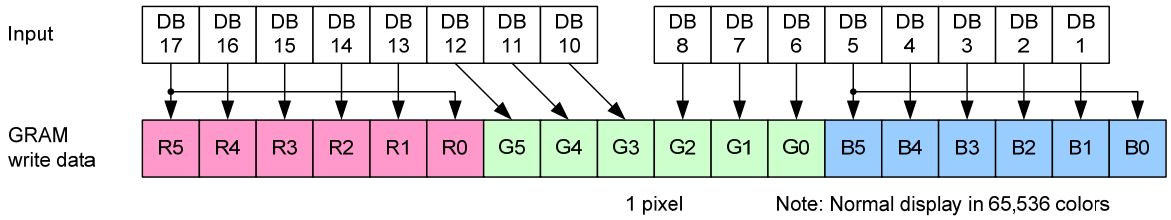
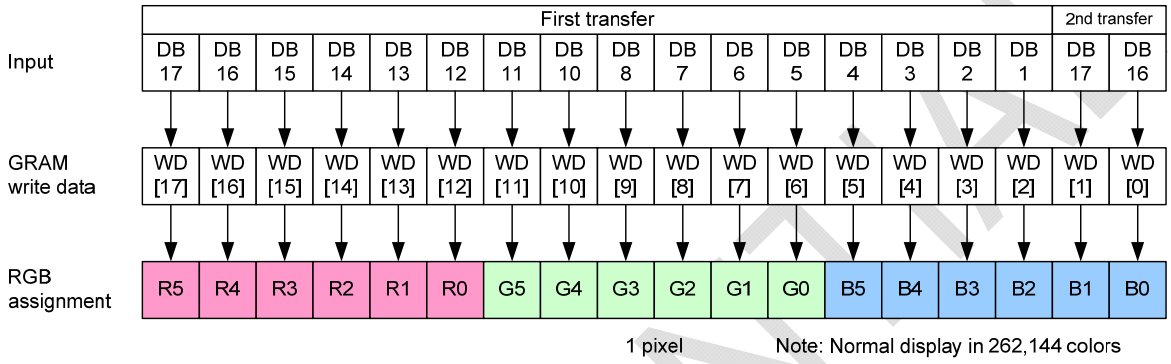


Figure 7 16-bit Interface Data Format (Instruction Write / Instruction Read)

RAM data write (single transfer mode: TRIREG = 0)



RAM data write (2 transfer mode: TRIREG = 1, DFM = 0)



RAM data write (2 transfer mode: TRIREG = 1, DFM = 1)

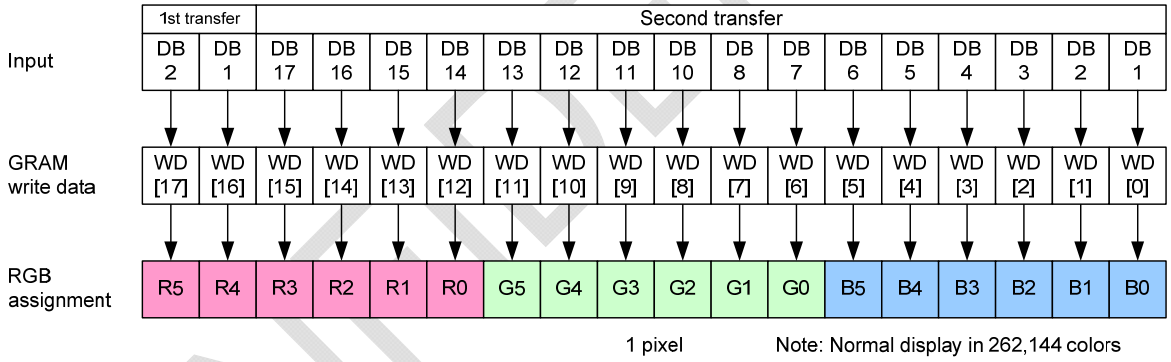


Figure 8 16-bit Interface Data Format (RAM data write)

RAM data read (single transfer: TRIREG = 0)

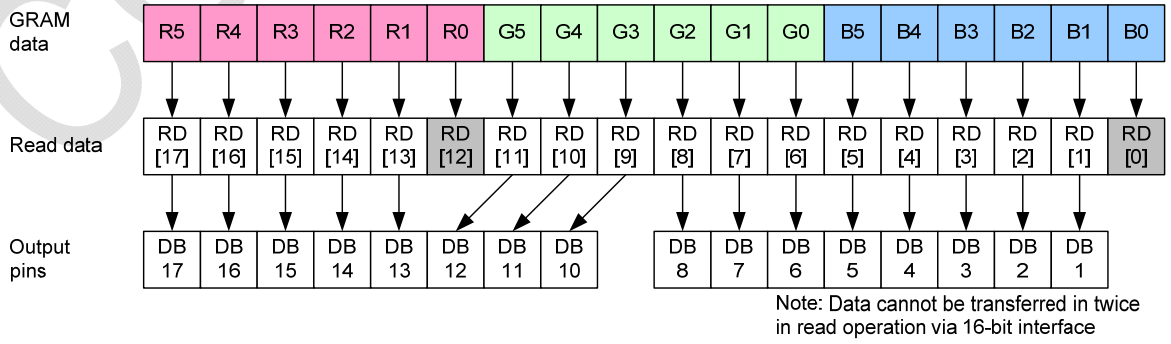


Figure 9 16-bit Interface Data Format (RAM data read)

12.3 80-system 9-bit Bus Interface

When transferring 16-bit instruction, it is divided into upper and lower 8 bits, and the upper 8 bits are transferred first (the LSB is not used). The RAM write data is also divided into upper and lower 9 bits, and the upper 9 bits are transferred first. The unused DB pins must be fixed at either IOVCC or IOGND level. When transferring the index register setting, make sure to write upper byte (8 bits).

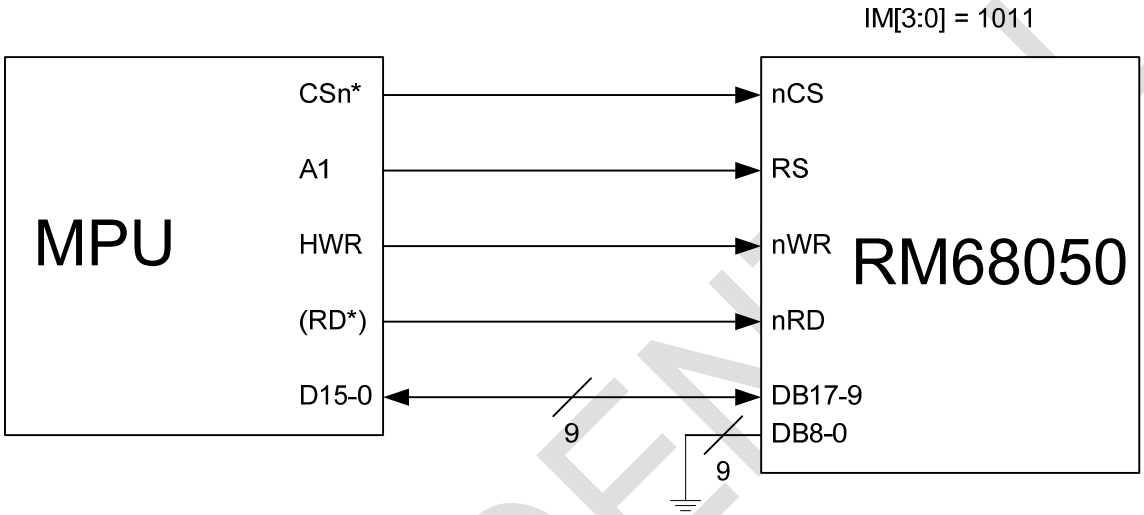


Figure 10 9-bit bus interface for 80-system

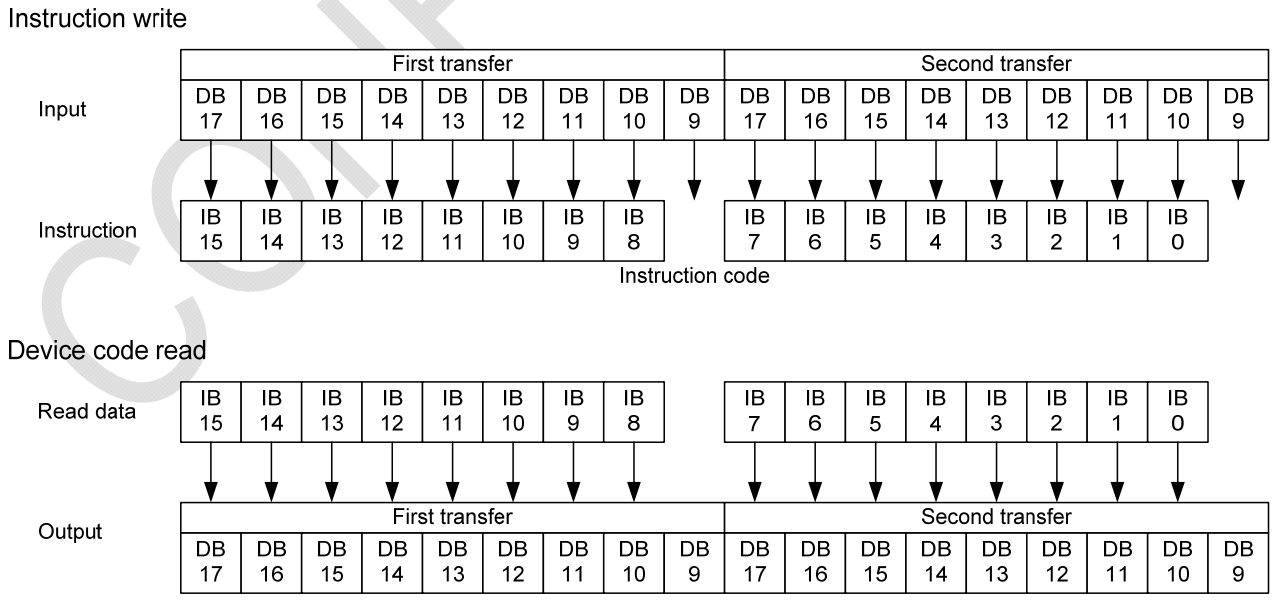


Figure 11 9-bit Interface Data Format (Instruction Write / Device Code Read)

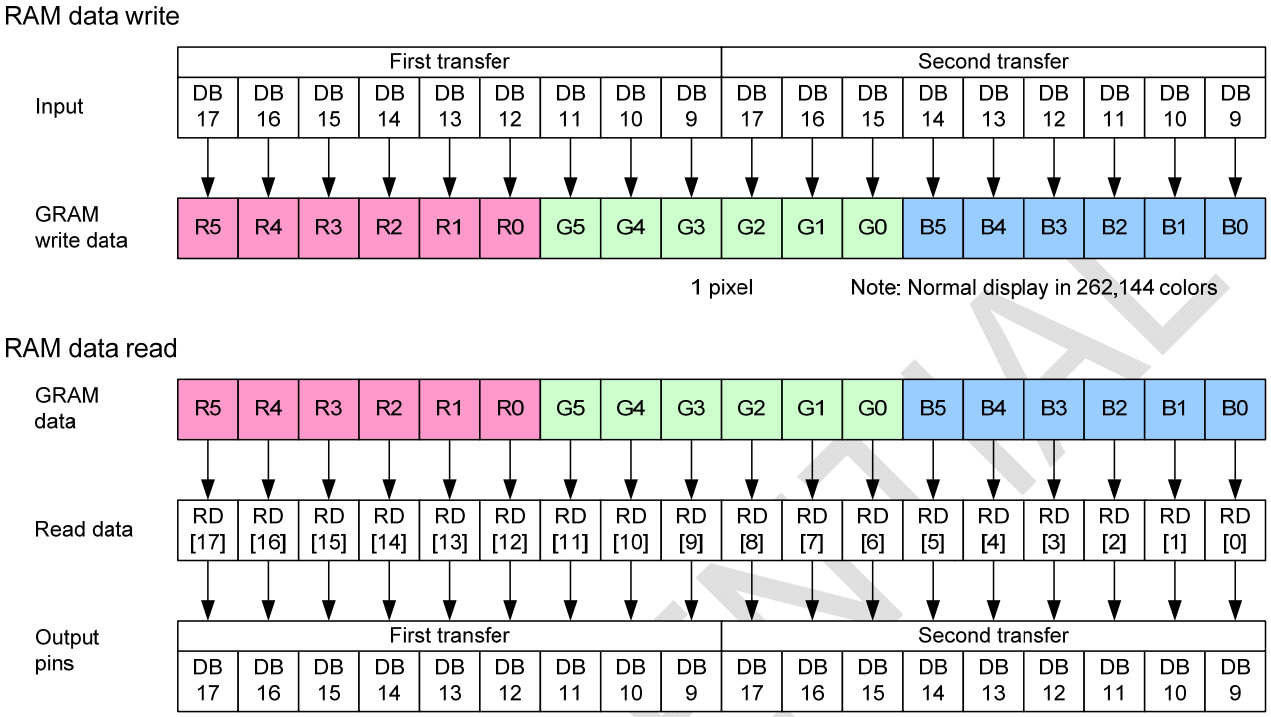


Figure 12 9-bit Interface Data Format (RAM Data Write / RAM Data Read)

12.4 80-system 8-bit Bus Interface

When transferring 16-bit instruction, it is divided into upper and lower 8 bits, and the upper 8 bits are transferred first. The RAM write data is also divided into upper and lower 8 bits, and the upper 8 bits are transferred first. The RAM write data is expanded into 18 bits internally as shown below. The unused DB pins must be fixed at either IOVCC or IOGND level. When transferring the index register setting, make sure to write upper byte (8 bits).

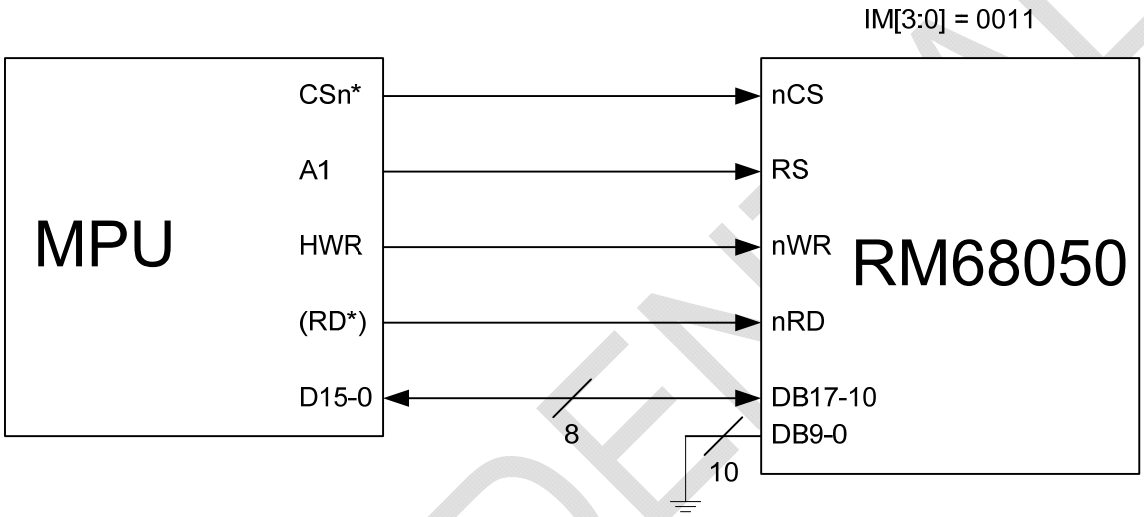


Figure 13 8-bit bus interface for 80-system

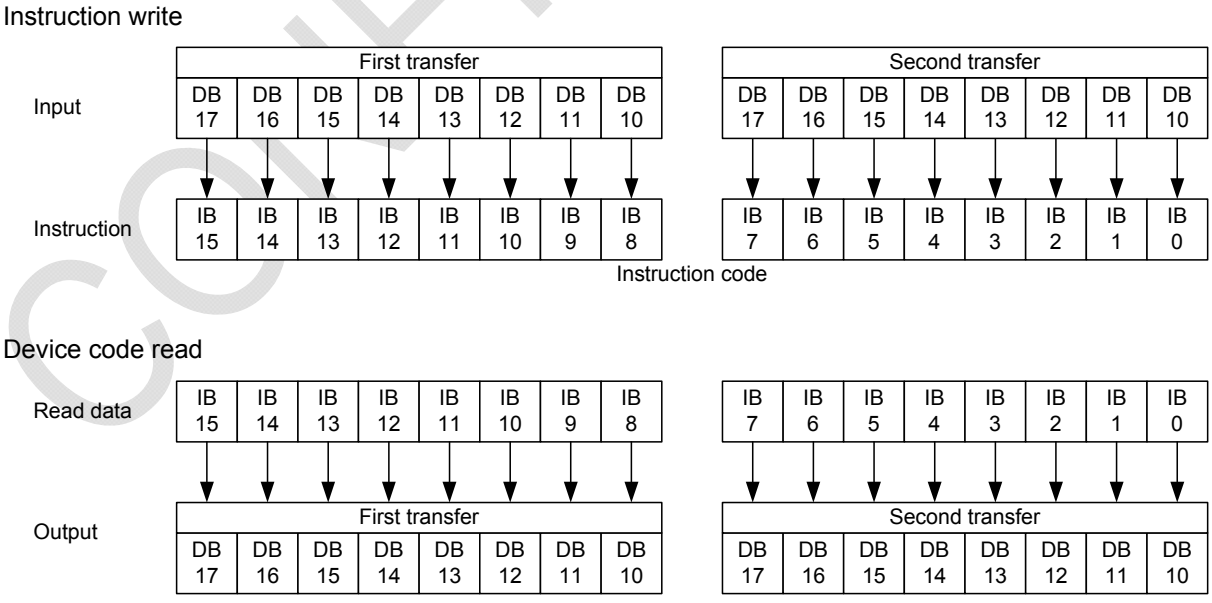
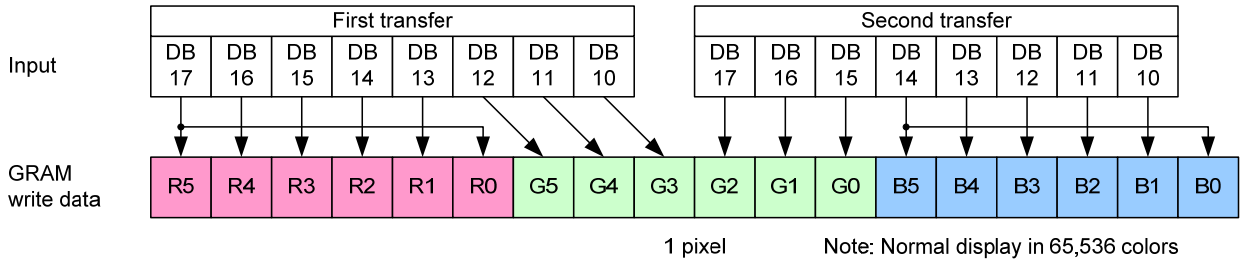
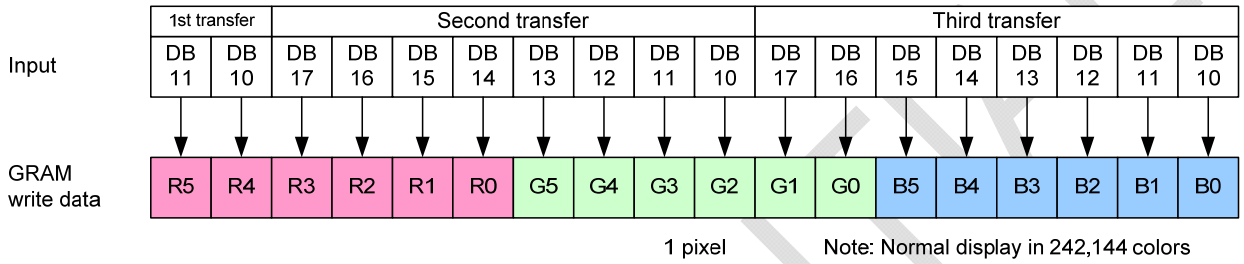


Figure 14 8-bit Interface Data Format (Instruction Write / Device Code Read)

RAM data write (2-transfer mode: TRIREG = 0)



RAM data write (3-transfer mode: TRIREG = 1, DFM = 0)



RAM data write (3-transfer mode: TRIREG = 1, DFM = 1)

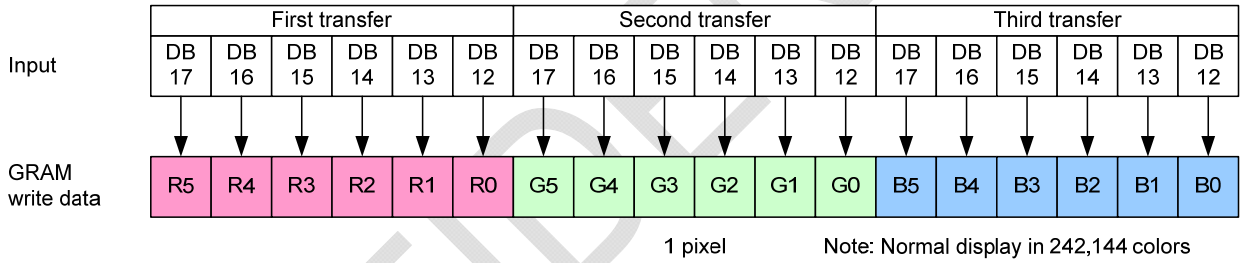
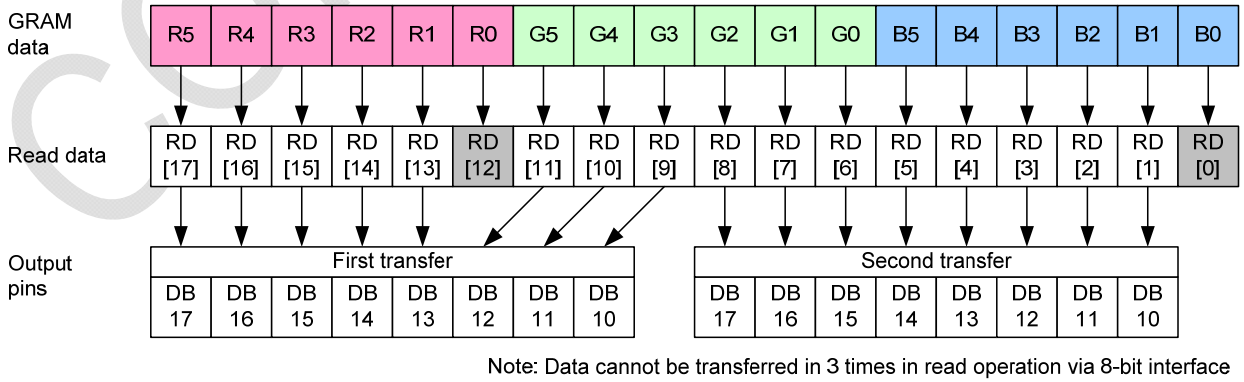


Figure 15 8-bit Interface Data Format (RAM Data Write)

RAM data read



Note: Data cannot be transferred in 3 times in read operation via 8-bit interface

Figure 16 8-bit Interface Data Format (RAM Data Read)

12.5 Serial Interface

The serial interface is selected by setting the IM3/2/1 pins to the IOGND/IOVCC/IOGND levels, respectively. The data is transferred via chip select line (nCS), serial transfer clock line (SCL), serial data input line (SDI), and serial data output line (SDO). In serial interface operation, the IM0/ID pin functions as the ID pin, and the DB17-0 pins, not used in this mode, must be fixed at either IOVCC or GND level.

The SPI interface operation enables from the falling edge of nCS and ends of data transfer on the rising edge of nCS. The start byte is transferred to start the SPI interface and the read/write operation and RS information are also included in the start byte. When the start byte is matched, the subsequent data is received by RM68050.

The seventh bit of start byte is RS bit. When RS = “0”, either index write operation or status read operation is executed. When RS = “1”, either register write operation or RAM read/write operation is executed. The eighth bit of the start byte is used to select either read or write operation (R/W bit). Data is written when the R/W bit is “0” and read back when the R/W bit is “1”.

After receiving the start byte, RM68050 starts to transfer or receive the data in unit of byte and the data transfer starts from the MSB bit. All the registers of the RM68050 are 16-bit format and receive the first and the second byte data as the upper and the lower eight bits of the 16-bit register respectively. In SPI mode, 5 bytes dummy read is necessary and the valid data starts from 6th byte of read back data.

Table 14 Start Byte Format

Transferred Bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note: The ID bit is determined by setting the IM0/ID pin.

Table 15 Functions of RS, R/W bits

RS	R/W	Function
0	0	Set index register
0	1	Read a status
1	0	Write instruction or RAM data
1	1	Read instruction or RAM data

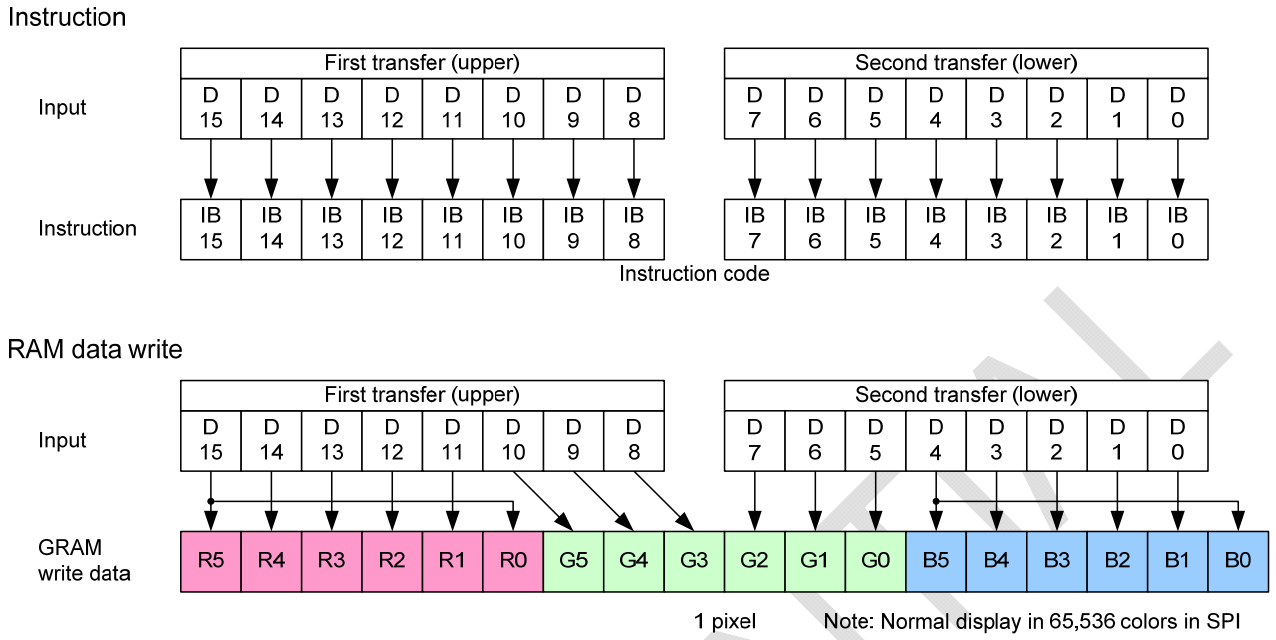
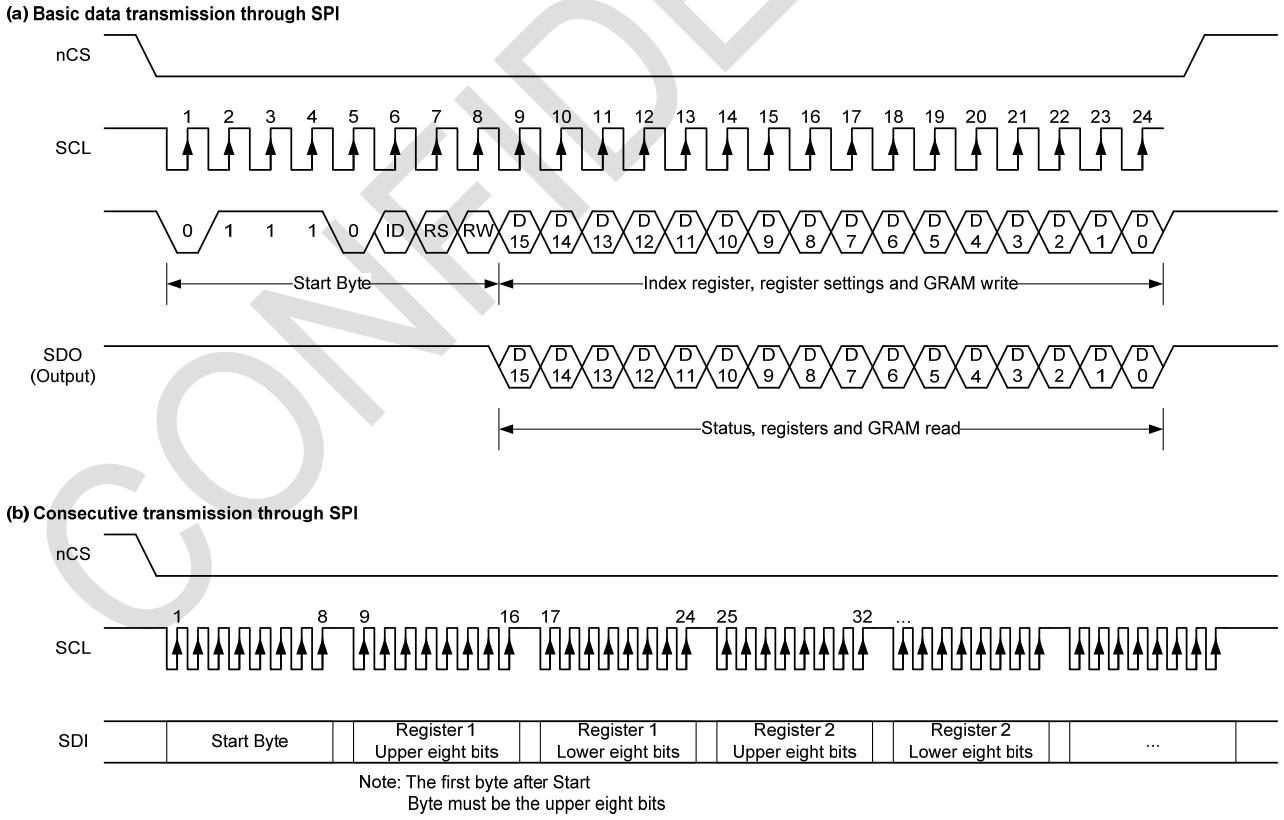
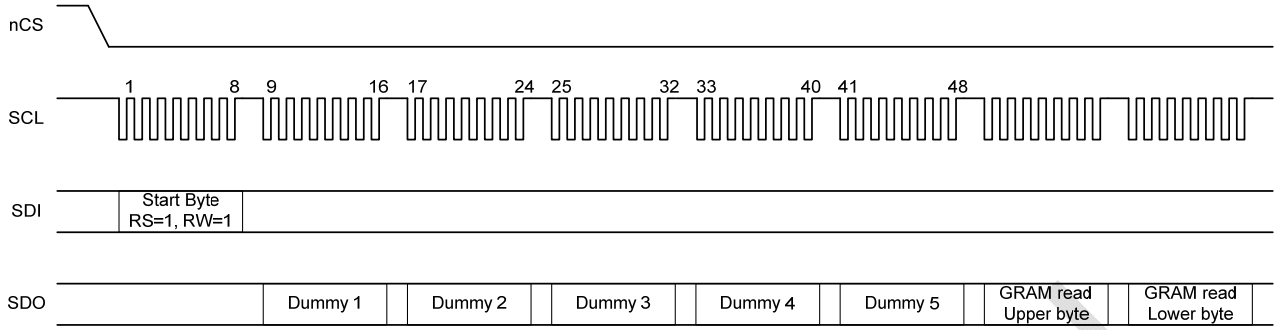


Figure 17 Serial Interface Data Format

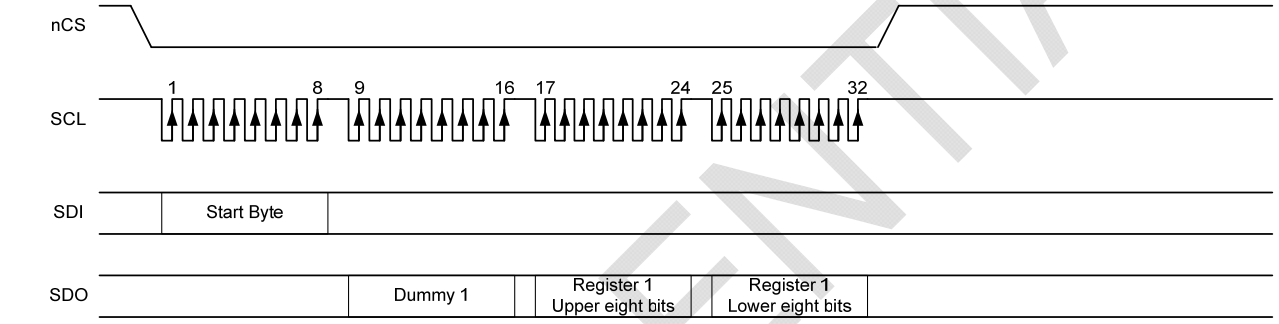


(c) GRAM data read transmission (TRI="0")



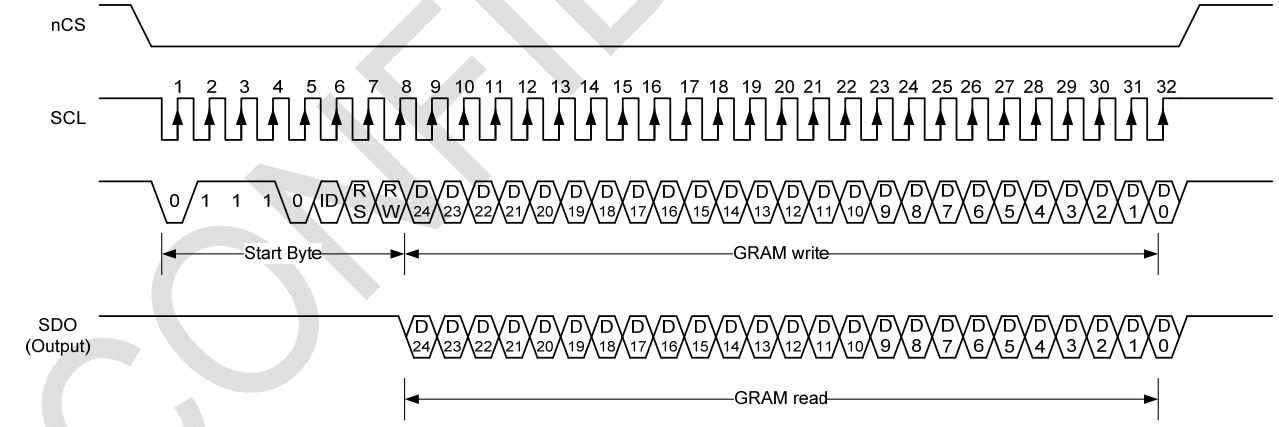
Note: Five bytes of dummy data are right after the Start Byte

(d) Status/register read transmission

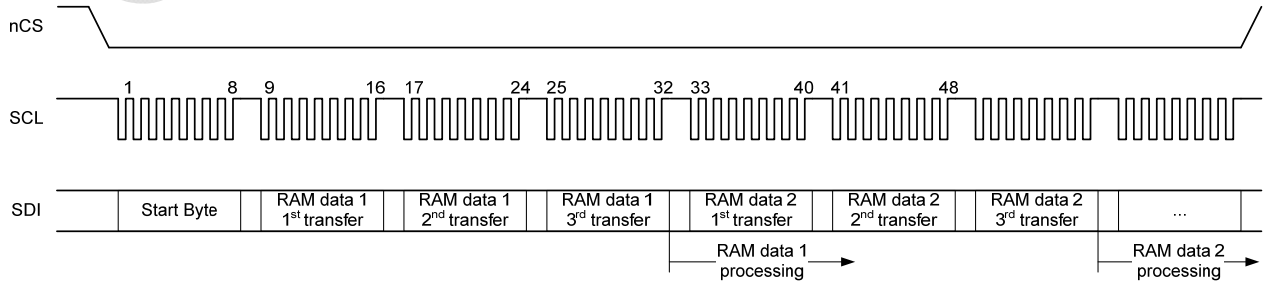


Note: One byte of dummy data is right after the Start Byte

(e) Basic RAMdata transmission through SPI (TRI="1")



(f) GRAM data write transmission through SPI (TRI="1")



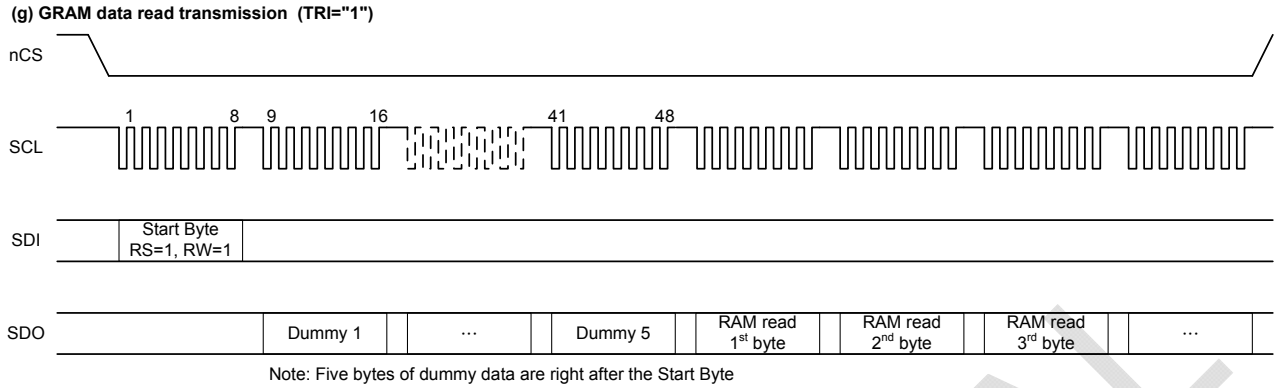


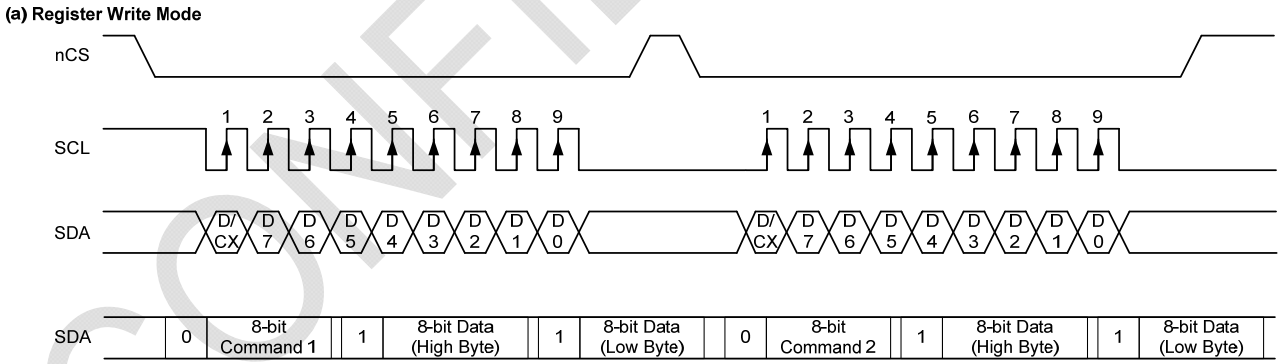
Figure 18 Data Transfer in Serial Interface

12.6 9-bit 3-wire Serial Interface

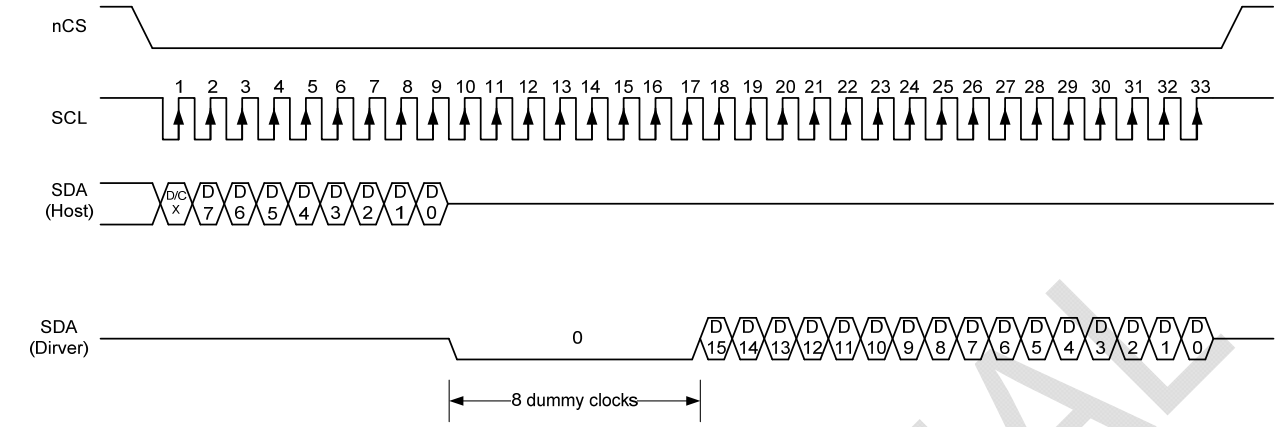
This SPI mode uses a 3-wire 9-bit serial interface. The chip-select nCS (active low) enables and disables the serial interface. SCL is the serial data clock and SDA is serial data.

Serial data must be input to SDA in the sequence D/CX, D7 to D0. The RM68050 catches the data at the rising edge of SCL signal. The first bit of serial data D/CX is data/command flag. D/CX = "1" indicates that D7 to D0 bits are display RAM data or command parameters. D/CX = "0" indicates that D7 to D0 bits are commands.

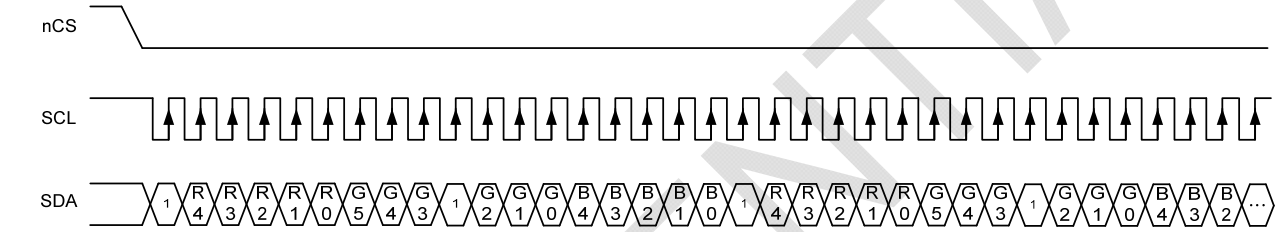
When users need to read back the register or GRAM data, the register R66h must be set to “1” first, and then write the register index to read back the register or GRAM data.



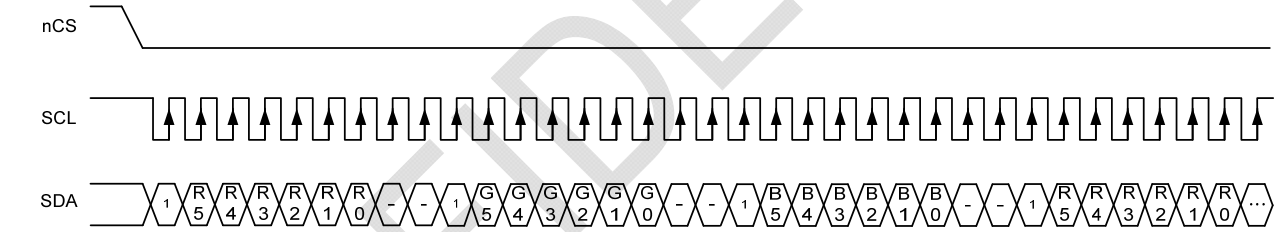
(b) Register Read Mode



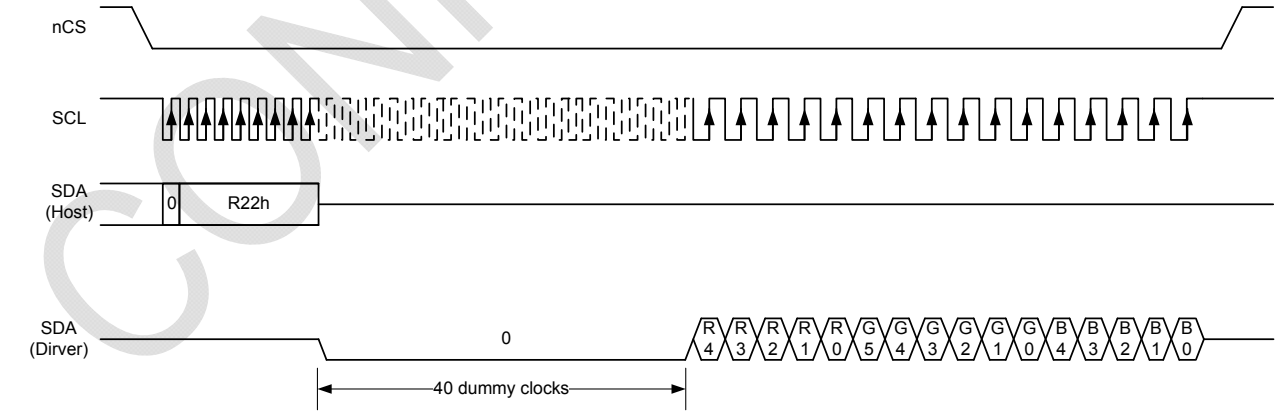
(c) GRAM Write Mode (TRI="0")



(d) GRAM Write Mode (TRI="1")



(e) GRAM Read Mode (TRI="0")



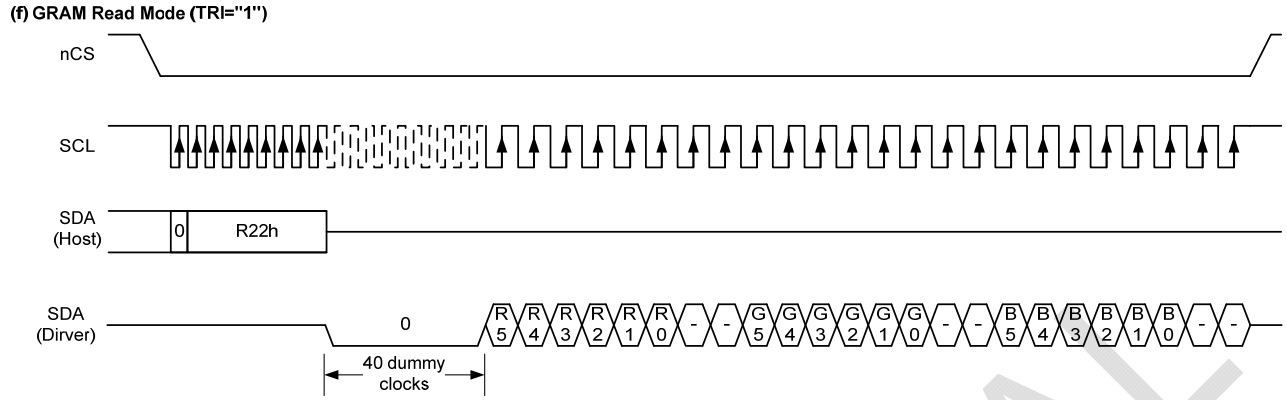
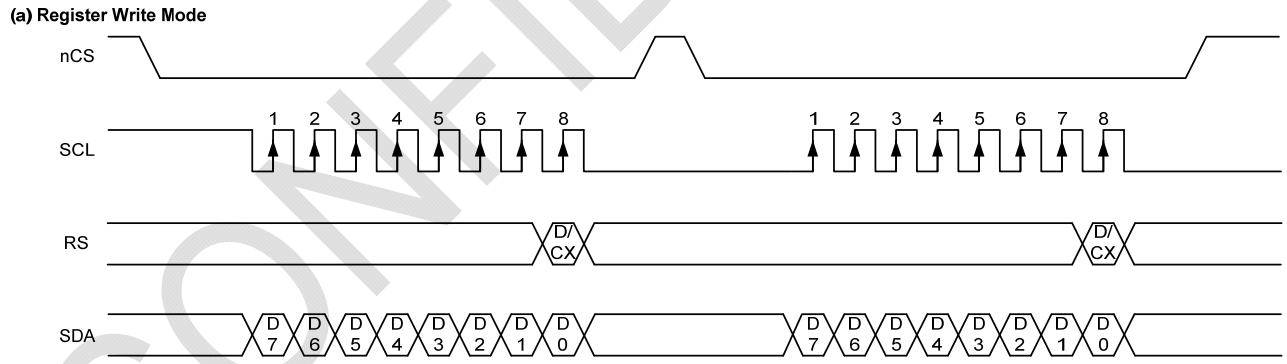


Figure 19 Data Transfer in 3-wire Serial Interface

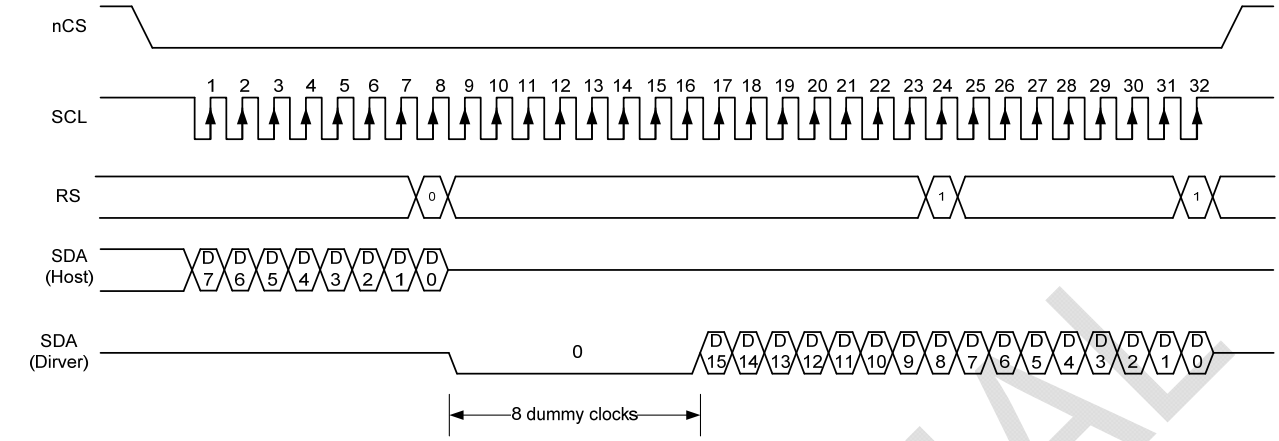
12.7 8-bit 4-wire Serial Interface

This SPI mode uses a 4-wire 9-bit serial interface. The chip-select nCS (active low) enables and disables the serial interface. D/CX (input through RS pin) is the command or data select signal, SCL is the serial data clock and SDA is serial data.

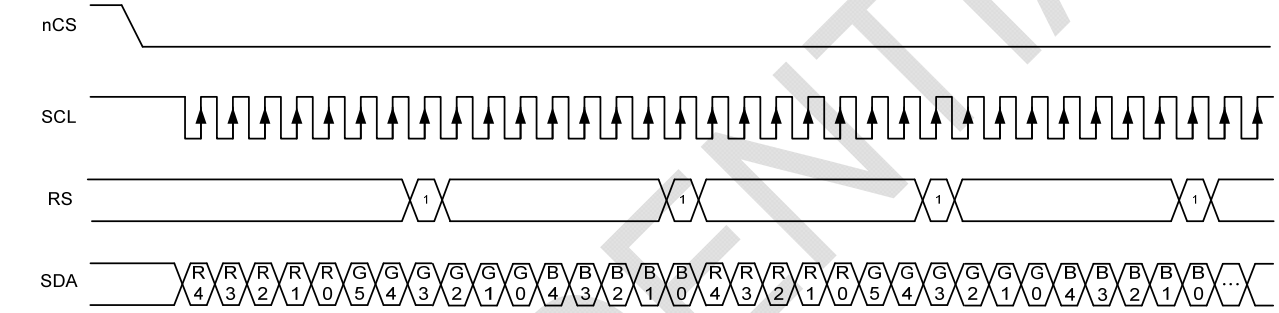
Serial data must be input to SDA in the sequence D7 to D0. The RM68050 catches the data at the rising edge of SCL signal. The D/CX signal indicates data/command. D/CX = "1" indicates that D7 to D0 bits are display RAM data or command parameters. D/CX = "0" indicates that D7 to D0 bits are commands.



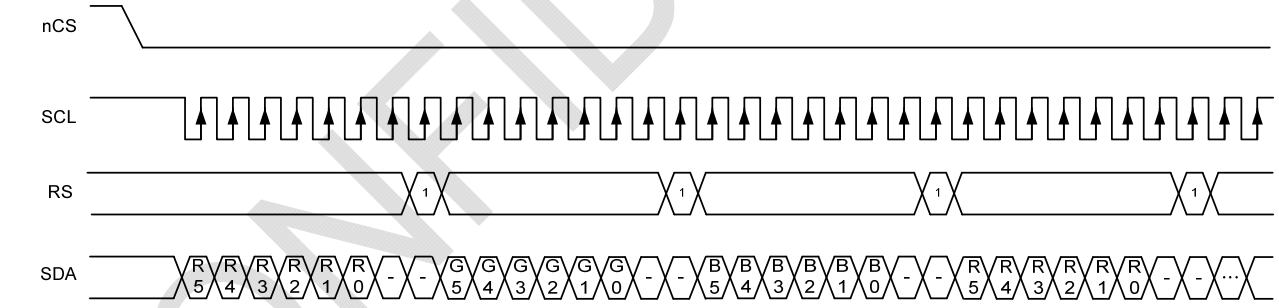
(b) Register Read Mode



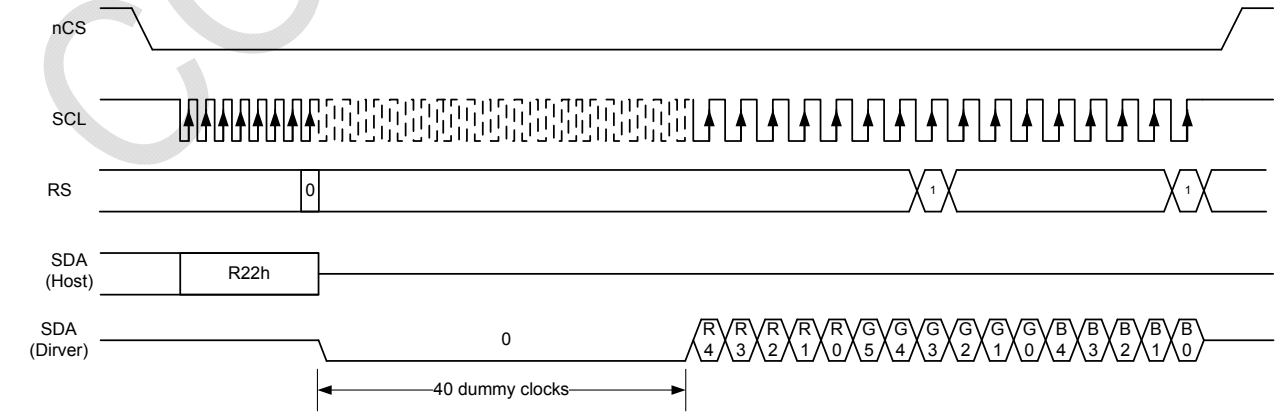
(c) GRAM Write Mode (TRI="0")



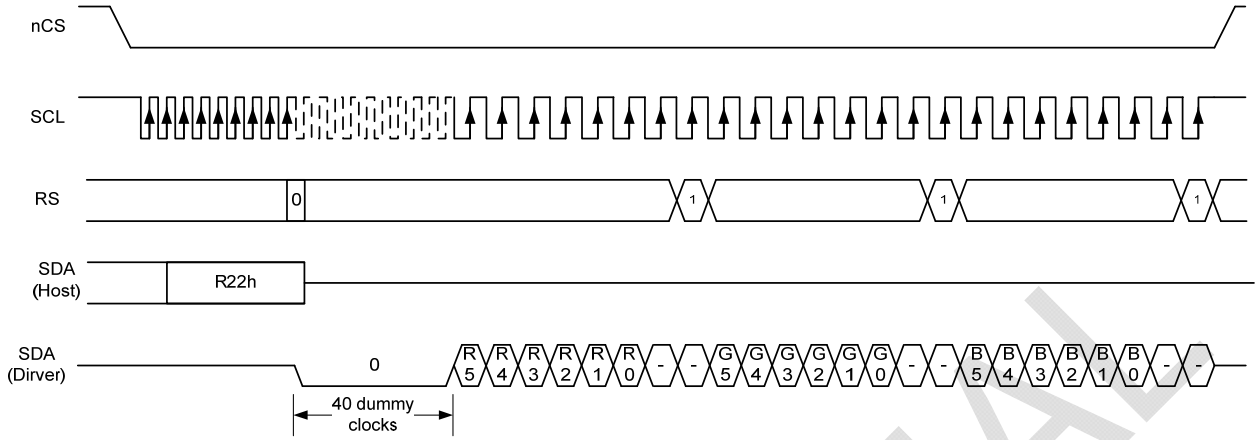
(d) GRAM Write Mode (TRI="1")



(e) GRAM Read Mode (TRI="0")



(f) GRAM Read Mode (TRI="1")



13. VSYNC Interface

RM68050 supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = “10” and RM = “0”.

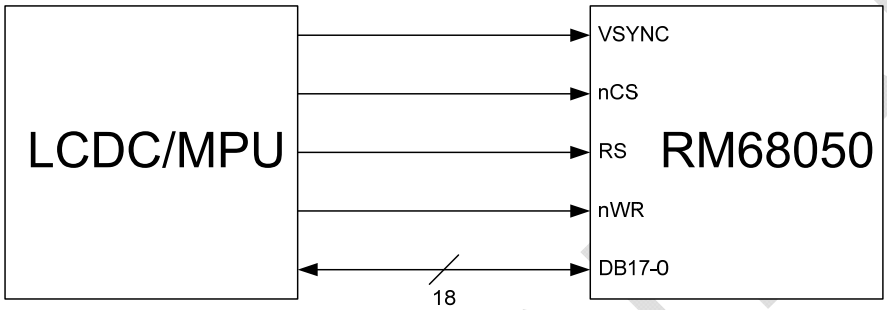


Figure 20 VSYNC Interface connection

In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.

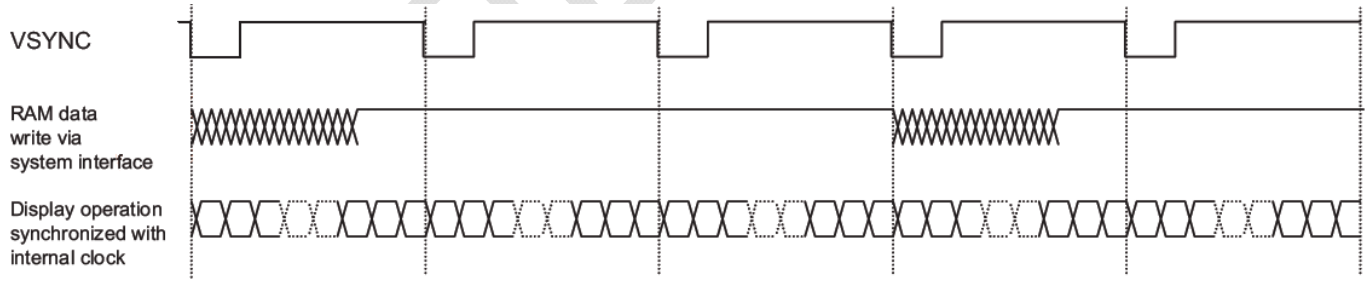


Figure 21 Moving Picture Data Transfers via VSYNC Interface

The VSYNC interface has the minimum for RAM data write speed and internal clock frequency, which must be more than the values calculated from the following formulas, respectively.

$$\text{Internal clock frequency (fosc) [Hz]}$$
$$= \text{FrameRate} \times (\text{DisplayLines(NL)} + \text{FrontPorch(FP)} + \text{BackPorch(BP)}) \times \text{ClocksPerLine(RTN)} \times \text{variance}$$

$$\text{RAM Write Speed(min.)[Hz]} > \frac{240 \times \text{DisplayLines(NL)}}{(\text{FrintPorch(FP)} + \text{BackPorch(BP)} + \text{DisplayLines(NL)} - \text{margins}) \times 16(\text{clocks}) \times \frac{1}{\text{fosc}}}$$

Note: When RAM write operation is not started right after the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of calculating minimum RAM writing speed and internal clock frequency in VSYNC interface operation is as follows.

[Example]

Panel Size	240 RGB x 320 lines (NL = 6'h27: 320 lines)
Total number of lines (NL)	320 lines
Black/front porch	14/2 lines (BP = 4'hE, FP = 4'h2)
Frame frequency	60 Hz

Internal clock frequency (fosc) [Hz]

= 60 Hz x (320 + 2 + 14) lines x 16 clocks x 1.1 / 0.9 = 394 kHz

When calculate the internal clock frequency, the oscillator variation is needed to be taken into consideration. In the above example, the calculated internal clock frequency with ±10% margin variation is considered and ensures to complete the display operation within one VSYNC cycle. The causes of frequency variation come from fabrication process of LSI, room temperature, external resistors and VCI voltage variation.

Minimum speed for RAM writing [Hz]

> 240 x 320 / {((14 + 320 - 2) lines x 16 clocks) x 1/394 kHz} = 5.7 MHz

The above theoretical value is calculated based on the premise that the RM68050 starts to write data into the internal GRAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line and the GRAM line address where data writing operation is performed. The GRAM write speed of 5.7MHz or more will guarantee the completion of GRAM write operation before the RM68050 starts to display the GRAM data on the screen and enable to rewrite the entire screen without flicker.

Notes:

1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into consideration.

2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.
3. When switching from the internal clock operation mode (DM[1:0] = “00”) to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.
4. The partial display and vertical scroll functions are not available in VSYNC interface mode and set the AM bit to “0” to transfer display data.

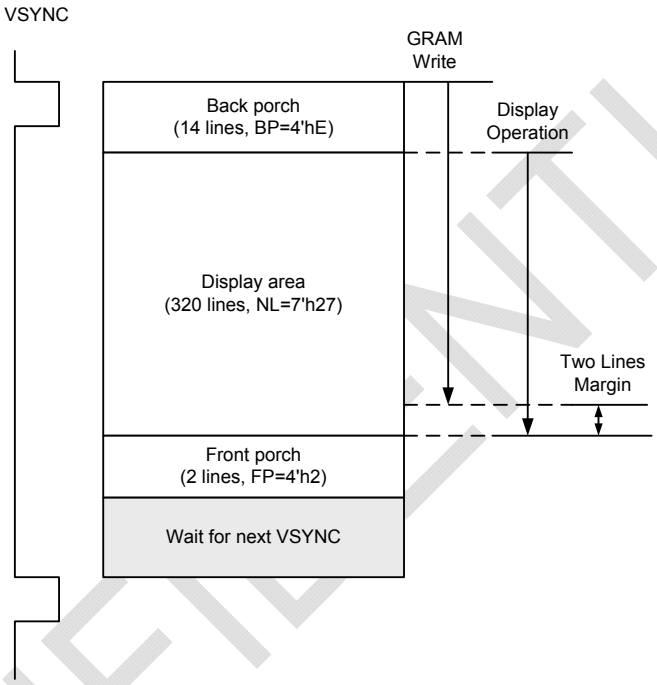


Figure 22 RAM Write Speed Margins

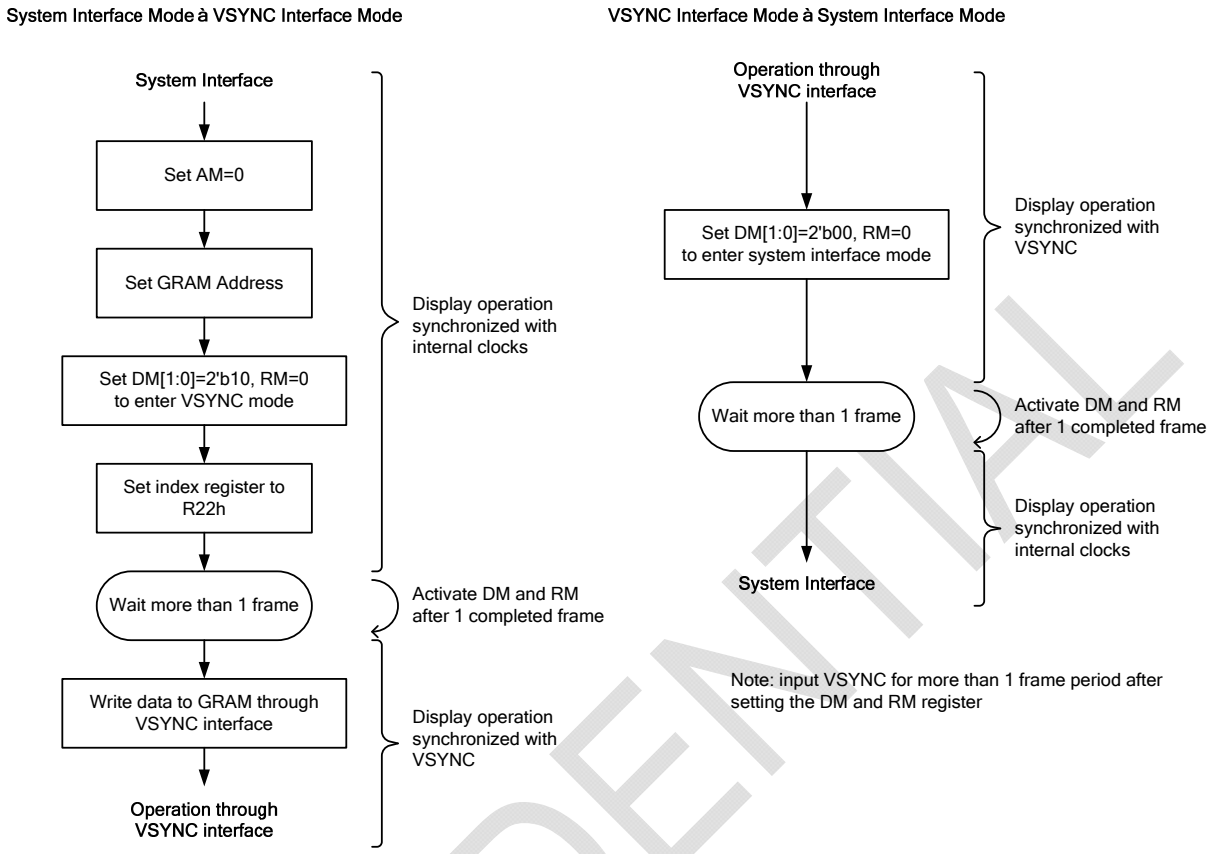


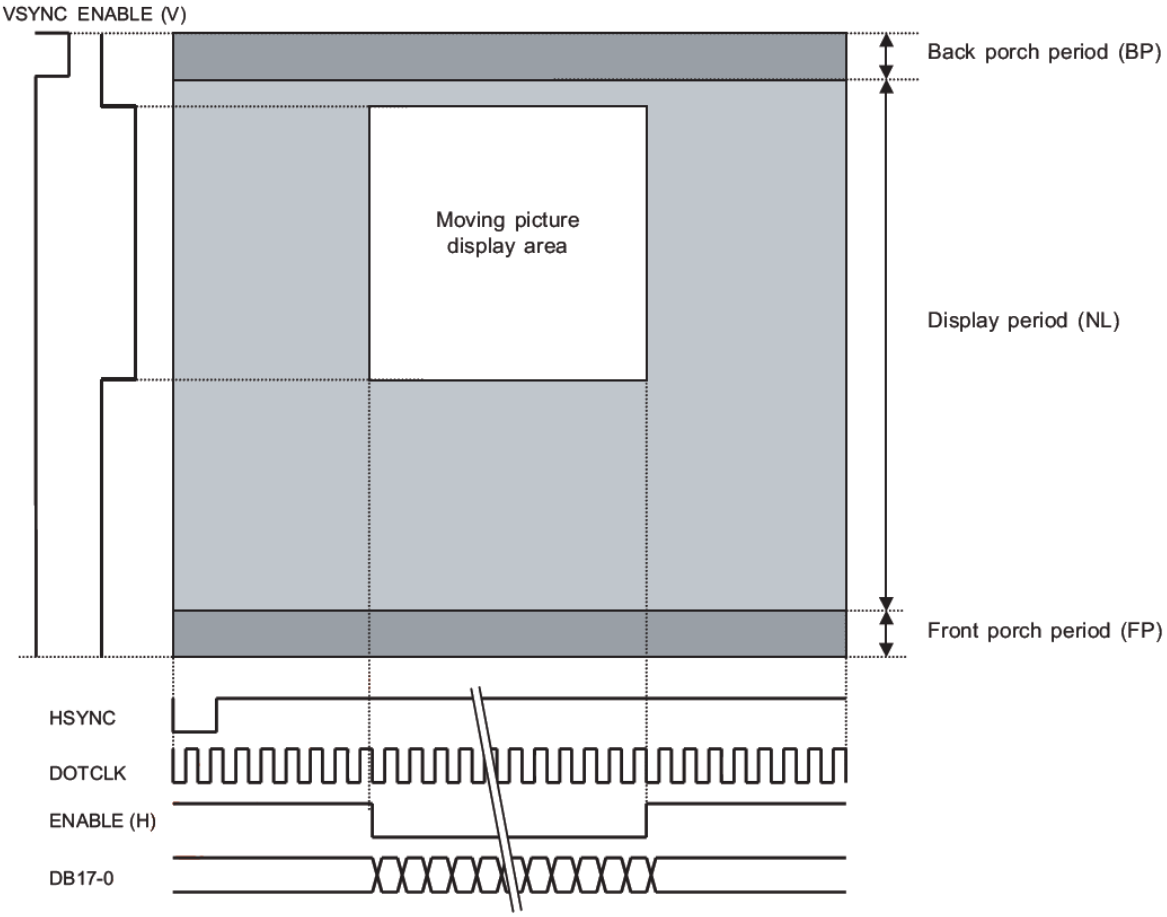
Figure 23 Sequences to Switch between VSYNC and Internal Clock Operation Modes

14. RGB Interface

The RM68050 supports the RGB interface. The interface format is set by RIM[1:0] bits. The internal RAM is accessible via RGB interface.

Table 16 RGB interface

RIM1	RIM0	RGB Interface	DB Pin
0	0	18-bit RGB interface	DB17-0
0	1	16-bit RGB interface	DB17-13, DB11-1
1	0	6-bit RGB interface	DB17-12
1	1	Setting inhibited	-



Notes: 1. The front porch period continues until next VSYNC input is detected.
2. Make sure to match the VSYNC, HSYNC, and DOTCLK frequencies to the resolution of liquid crystal panel.

Figure 24 Display Operation via RGB Interface

14.1 RGB Interface Timing

The timing relationship of signals in RGB interface operation is as follows.

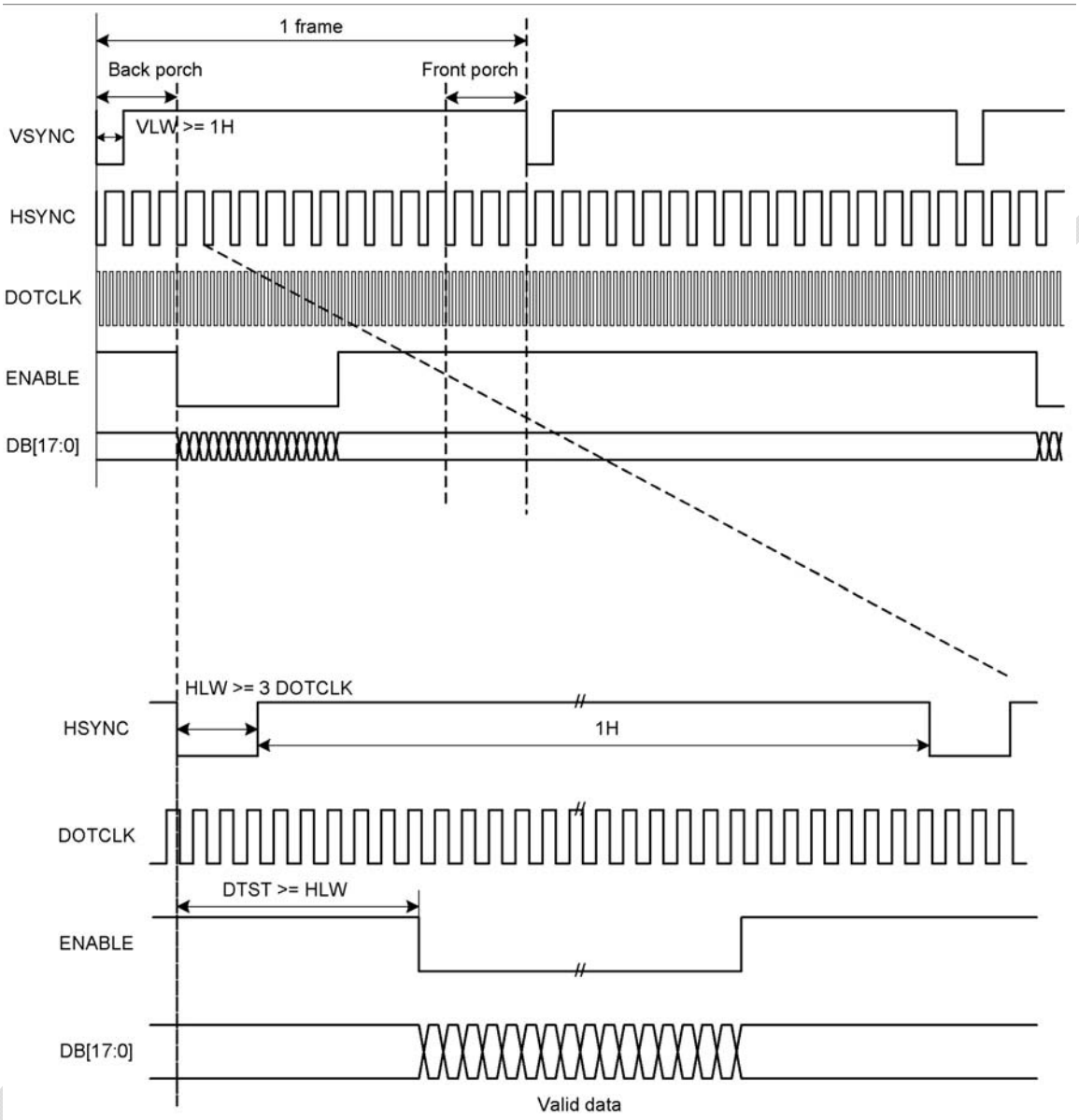


Figure 25 16-/18-bit RGB Interface Timing

Notes:

1. VLW: VSYNC Low period,
2. HLW: HSYNC Low period,
3. DTST: data transfer setup time

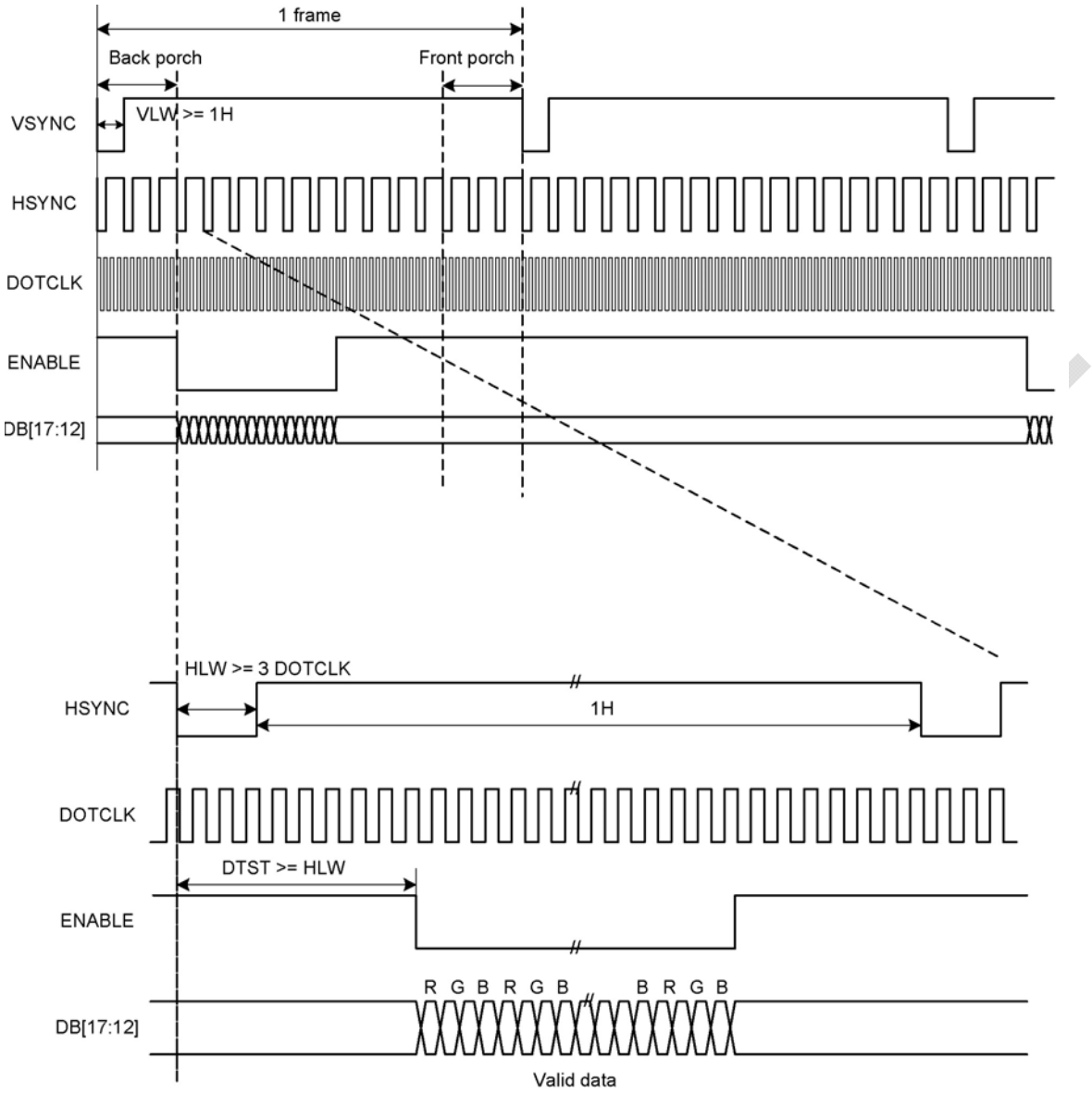


Figure 26 6-bit RGB Interface Timing

Notes:

1. VLW: VSYNC Low period,
2. HLW: HSYNC Low period,
3. DTST: data transfer setup time
4. In 6-bit RGB interface operation, set the VSYNC, HSYNC, ENABLE, DOTCLK cycles so that one pixel is transferred in units of three DOTCLKs via DB17-12.

14.2 Moving Pictures Mode

RM68050 has the RGB interface to display moving picture and incorporates GRAM to store display data, which has following advantages in displaying a moving picture.

• The window address function defined the update area of GRAM.

• Only the moving picture area of GRAM is updated.

• When display the moving picture in RGB interface mode, the DB[17:0] can be switched as system interface to update still picture area and registers, such as icons.

14.3 RAM access via system interface in RGB interface operation

RM68050 allows GRAM access via the system interface in RGB interface mode. In RGB interface mode, data are written to the internal GRAM in synchronization with DOTCLK and ENABLE signals. When write data to the internal GRAM by the system interface, set ENABLE to terminate the RGB interface and switch to the system interface to update the registers (RM = “0”) and the still picture of GRAM. When restart RAM access in RGB interface mode, wait one read/write cycle and then set RM = “1” and the index register to R22h to start accessing RAM via the RGB interface. If RAM accesses via two interfaces conflicts, there is no guarantee that data are written to the internal GRAM.

The following figure illustrates the operation of the RM68050 when displaying a moving picture via the RGB interface and rewriting the still picture RAM area via the system interface.

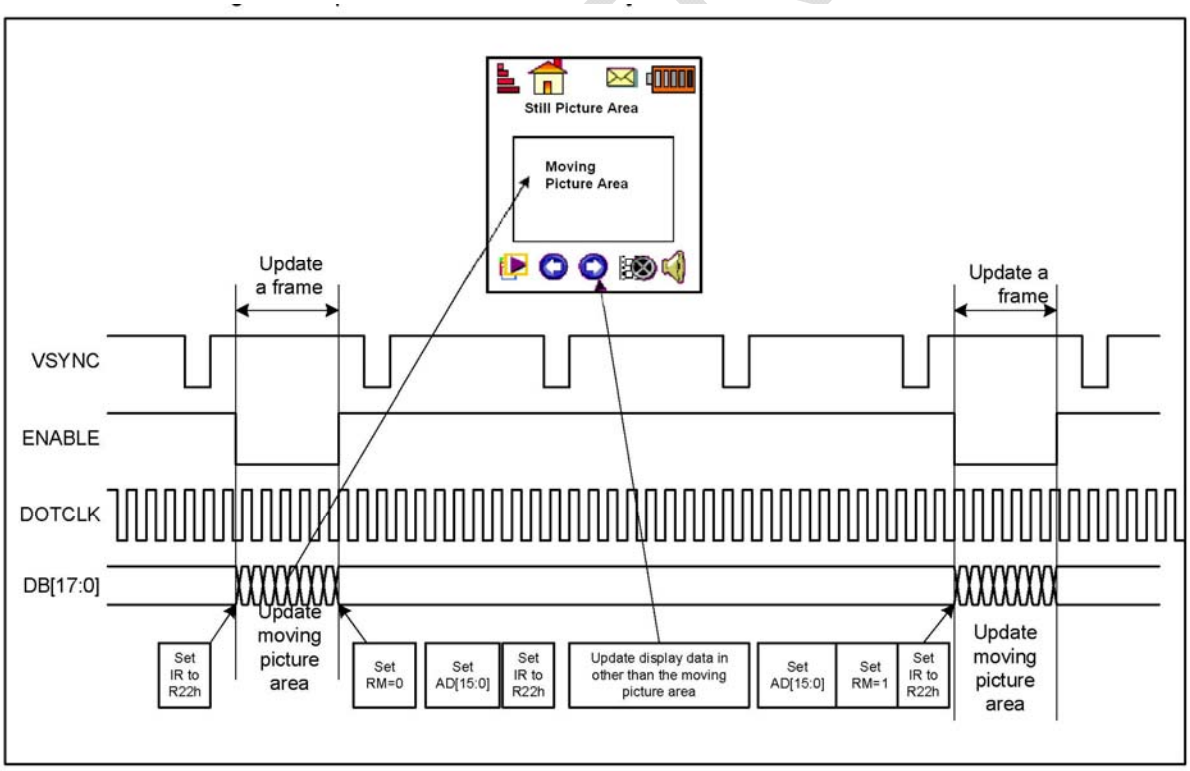


Figure 27 Updating the Still Picture Area while Displaying Moving Picture

14.4 6-bit RGB interface

The 6-bit RGB interface is selected by setting RIM[1:0] = 2'b10. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 6-bit port while data enable signal (ENABLE) allows RAM access via RGB interface. Unused pins DB11-0 (DB17-6) must be fixed at either IOVCC or IOGND level.

Instruction bits can be transferred only via system interface.

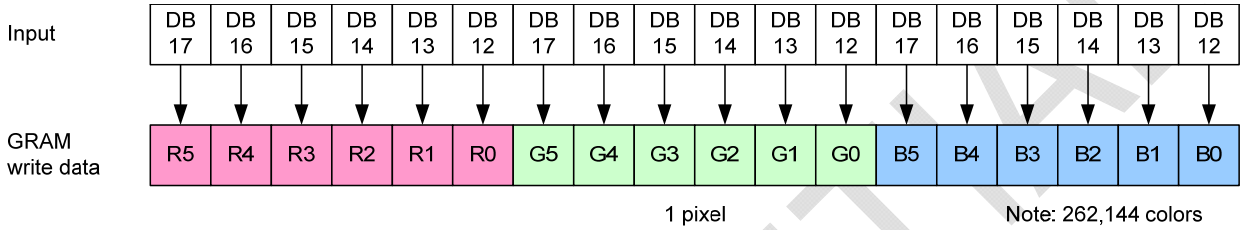


Figure 28 Example of 6-bit RGB Interface and Data Format

14.5 Data Transfer Synchronization in 6-bit Bus Interface Operation

The RM68050 has counters, which indicate the first, second, and third 6-bit transfer via 6-bit RBG interface. The counters are reset on the falling edge of VSYNC so that the data transfer will start from the first 6 bits of 18-bit RGB data from the next frame period. Accordingly, the data transfer via 6-bit interface can restart in correct order from the next frame period even if a mismatch occurs in transferring 6-bit data. This function can minimizes the effect from data transfer mismatch and help the display system return to normal display operation when data is transferred consecutively in moving picture operation.

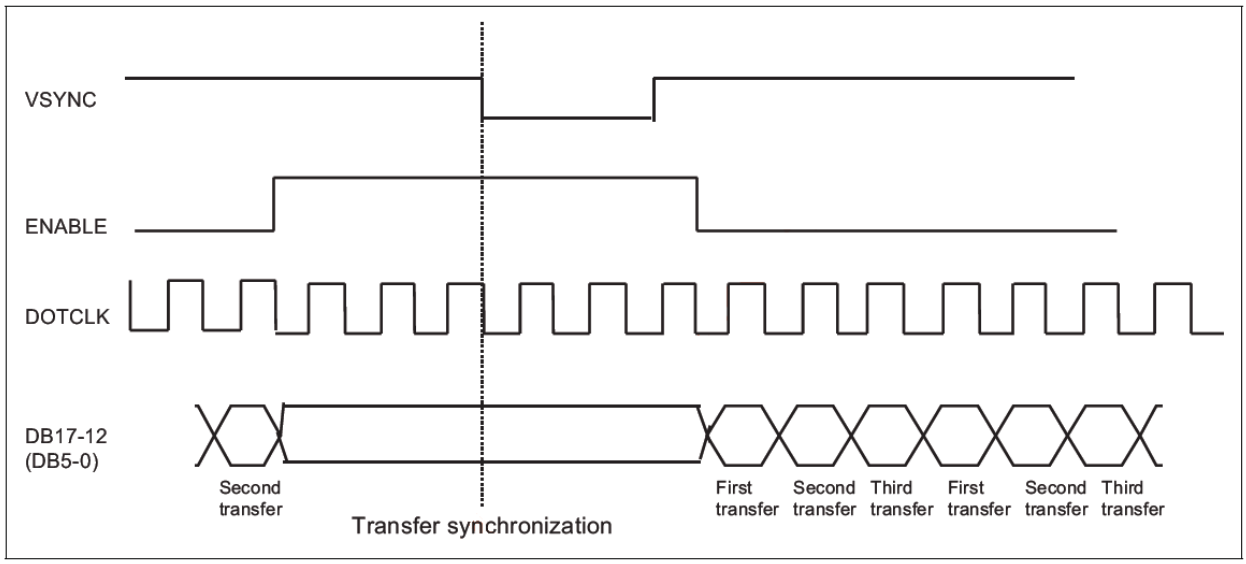


Figure 29 6-bit Transfer Synchronization

14.6 16-bit RGB interface

The 16-bit RGB interface is selected by setting RIM[1:0] = 2'b01. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 16-bit ports while data enable signal (ENABLE) allows RAM access via RGB interface.

Instruction bits can be transferred only via system interface.

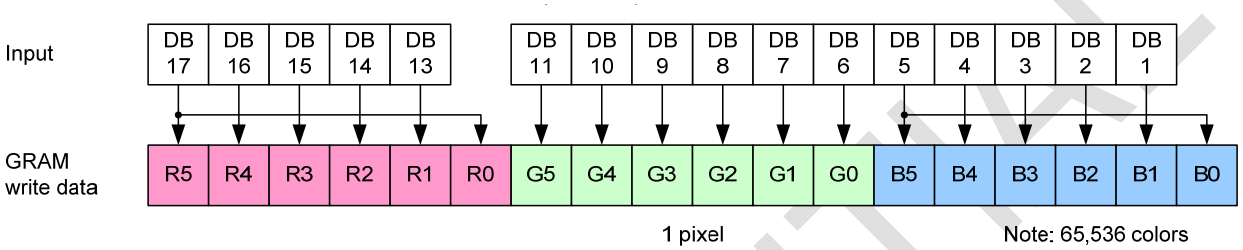


Figure 30 Example of 16-bit RGB Interface and Data Format

14.7 18-bit RGB interface

The 18-bit RGB interface is selected by setting RIM[1:0] = 2'b00. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. The display data is transferred to the internal RAM in synchronization with the display operation via 18-bit ports (DB17-0) while data enable signal (ENABLE) allows RAM access via RGB interface.

Instruction bits can be transferred only via system interface.

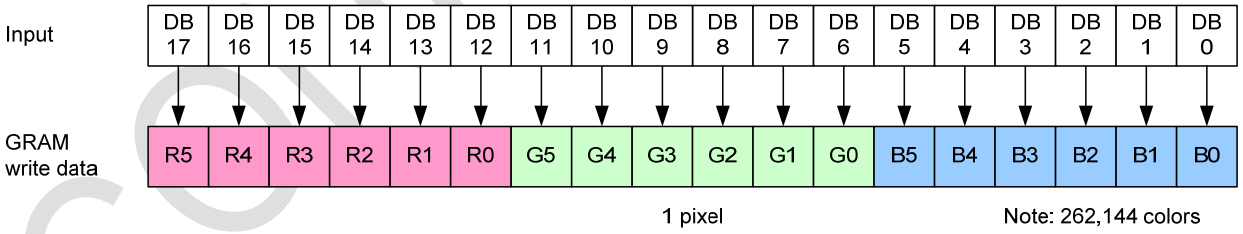


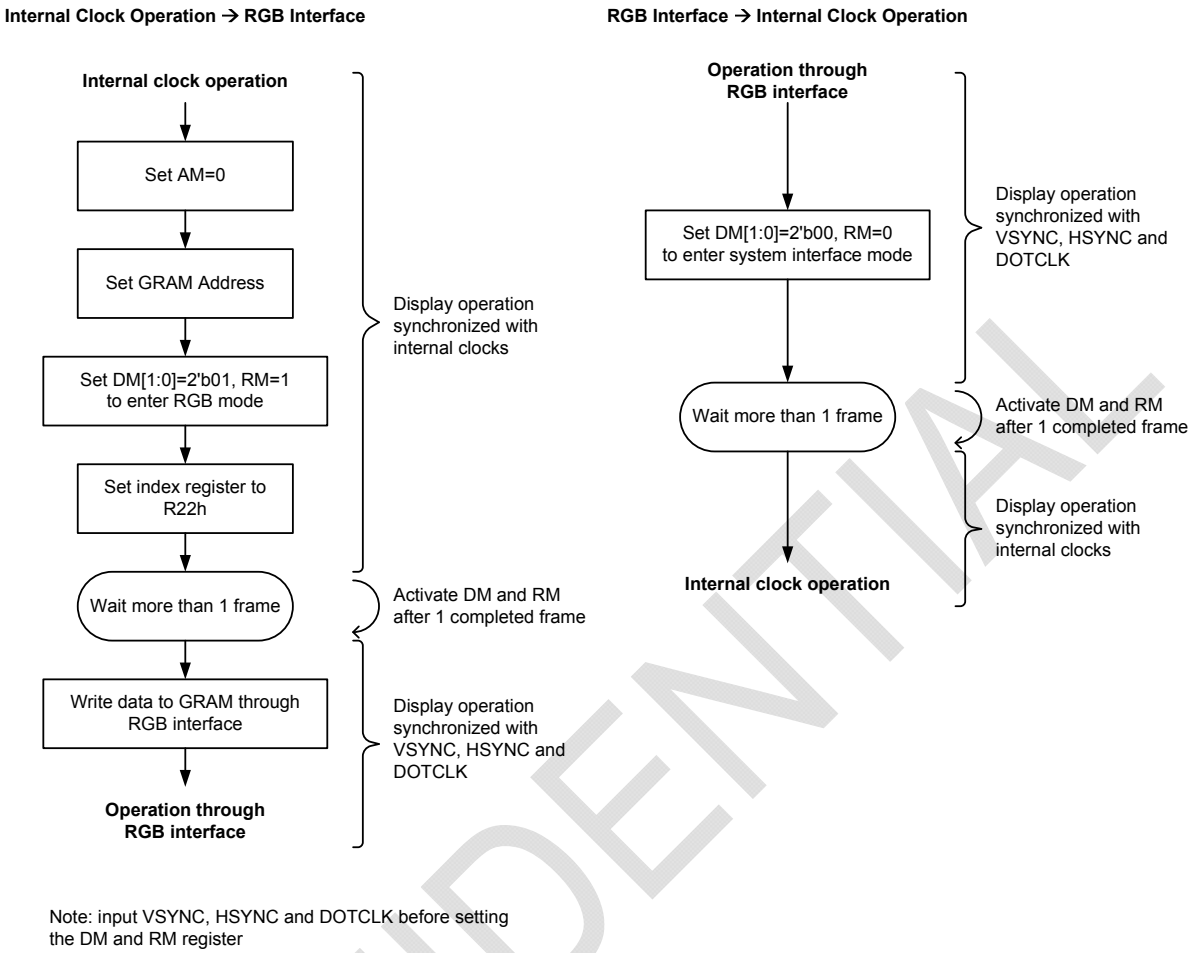
Figure 31 Example of 18-bit RGB Interface and Data Format

14.8 Notes to external display interface operation

1. The following functions are not available in external display interface operation.

Function	External Display Interface	Internal Display Operation
Partial display	Not available	Available
Scroll function	Not available	Available

2. The VSYNC, HSYNC, and DOTCLK signals must be supplied during display period.
3. The period set with the NOWE[1:0] bits (gate output non-overlap period) is not based on the internal clock but based on DOTCLK in RGB interface mode.
4. In 6-bit RGB interface mode, each of RGB dots is transferred in synchronization with a DOTCLK input. In other words, it takes 3 DOTCLK inputs to transfer one pixel. Be sure to complete data transfer in units of 3 DOTCLK inputs in 6-bit RGB interface mode.
5. In 6-bit RGB interface mode, data of one pixel, which consists of RGB dots, are transferred in units of 3 DOTCLK. Accordingly, set the cycle of each signal in 6-bit interface mode (VSYNC, HSYNC, ENABLE, DB[17:0]) to contain DOTCLK inputs of a multiple of 3 to complete data transfer in units of pixels.
6. When switching from the internal operation mode to the RGB Input Interface mode, or the other way around, follow the sequence below.
7. In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.
8. In RGB interface mode, a RAM address (AD[15:0]) is set in the address counter every frame on the falling edge of VSYNC.



Note: input VSYNC, HSYNC and DOTCLK before setting the DM and RM register

Figure 32 RGB and Internal Clock Operation Mode Switching Sequences

15. Partial Display Function

The RM68050 allows selectively driving two partial images on the screen at arbitrary positions set in the screen drive position registers.

The following example shows the setting for partial display function:

Partial image 1 display instruction		**Partial image 2 display instruction**		**Other instruction**	
PTDE0	1	PTDE1	1	BASEE	0
PTSA0[8:0]	9’h000	PTSA1[8:0]	9’h020	NL[5:0]	6’h27
PTEA0[8:0]	9’h00F	PTEA1[8:0]	9’h02F		
PTDP0[8:0]	9’h080	PTDP1[8:0]	9’h0C0		

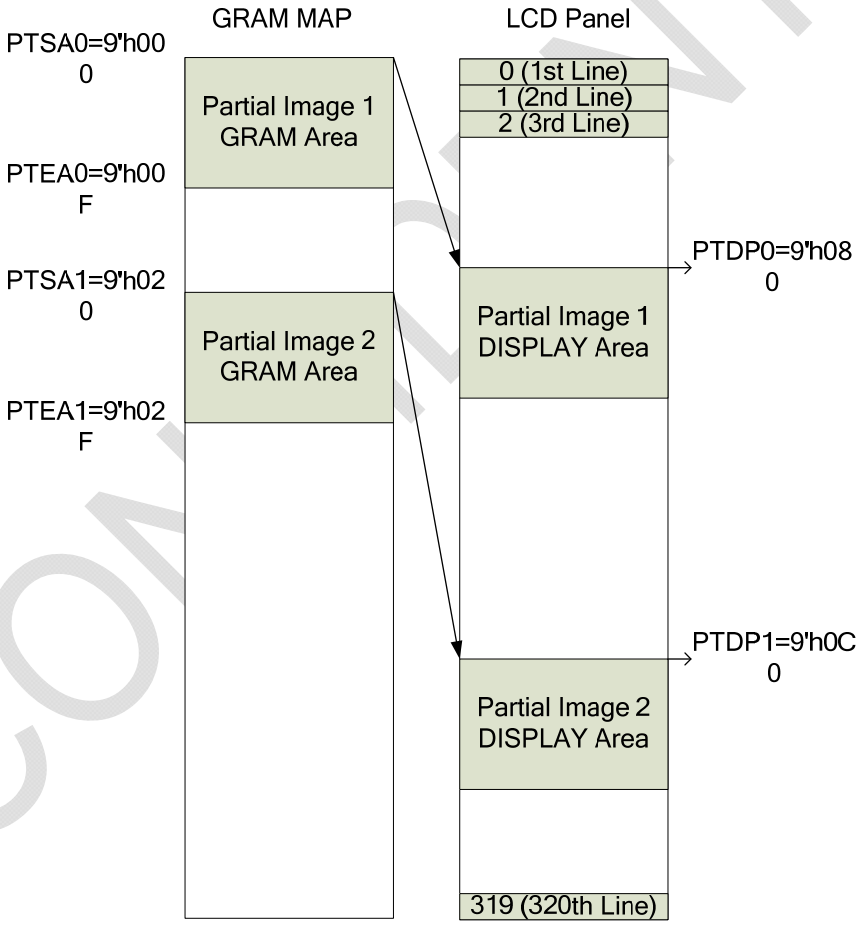


Figure 33 Partial Display example

16. Window Address Function

The window address function enables writing display data consecutively in a rectangular area (a window address area) made in the internal RAM. The window address area is made by setting the horizontal address register (start: HSA7-0, end: HEA 7-0 bits) and the vertical address register (start: VSA8-0, end: VEA8-0 bits). The AM and I/D bits set the transition direction of RAM address (increment or decrement, horizontal or vertical, respectively). Setting these bits enables the RM68050 to write data including image data consecutively without taking the data wrap position into account.

The window address area must be made within the GRAM address map area. Also, the AD16-0 bits (RAM address set register) must be set to an address within the window address area.

	Window address area setting range	**RAM address area setting range**
Horizontal direction	8'h00 ≤ HSA ≤ HEA ≤ 8'hEF	HSA ≤ AD[7:0] ≤ HEA
Vertical direction	9'h000 ≤ VSA ≤ VEA ≤ 9'h13F	VSA ≤ AD[16:8] ≤ VEA

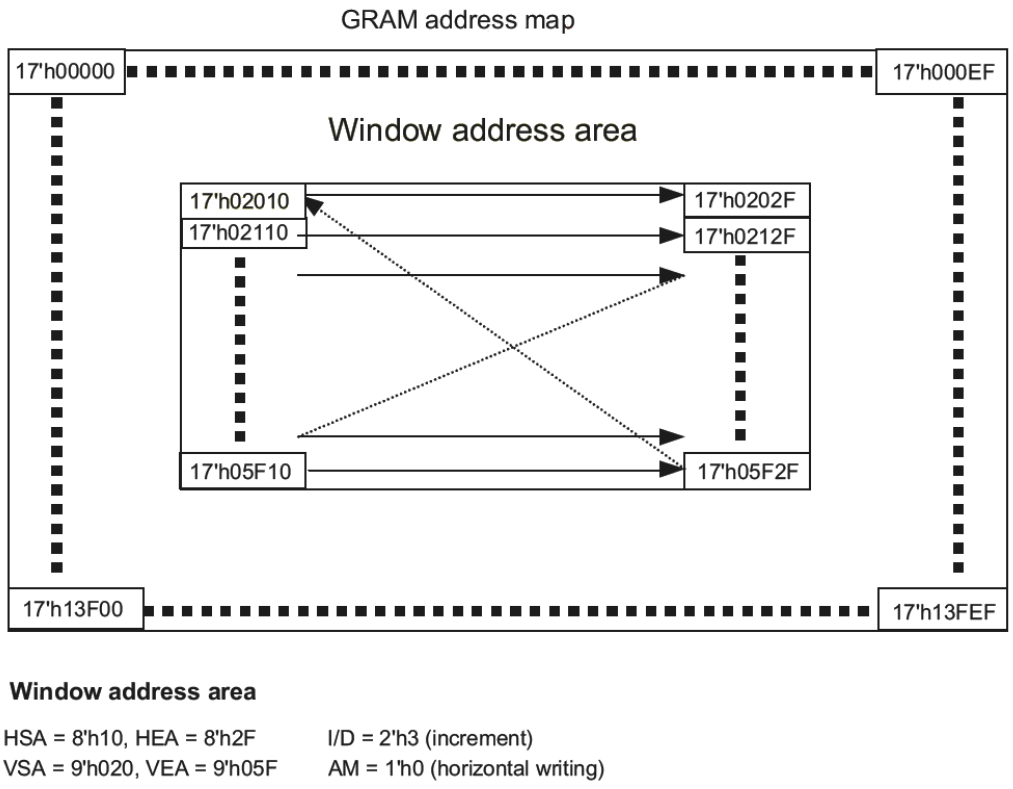
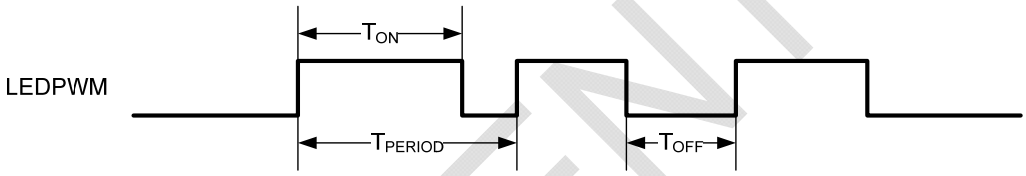


Figure 34 Automatic address update within a Window Address Area

17. CABC (Content Adaptive Brightness Control)

RM68050 provide a dynamic backlight control function as CABC (Content adaptive brightness control) to reduce the power consumption of the luminance source. RM68050 will refer the gray scale content of display image to output a PWM waveform to LED driver for backlight brightness control. Content adaptation means that the content of gray sale can be increased while simultaneously lowering brightness of the backlight to achieve the same perceived brightness. The adjusted gray level scale and thus the power consumption reduction depend on the content of the image.

RM68050 can calculate the backlight brightness level and send a PWM pulse to LED driver via LEDPWM pin for backlight brightness control purpose. The figure in the following is the basic timing diagram which is applied RM68050 to control LED driver.



18. γ Correction Function

The RM68050 supports γ-correction function to display in 262,144 colors simultaneously using gradient adjustment, amplitude-adjustment, and fine-adjustment registers. Each register consists of positive-polarity register and negative-polarity register to allow optimal gamma correction setting for the characteristics of the panel by enabling different settings for positive and negative polarities.

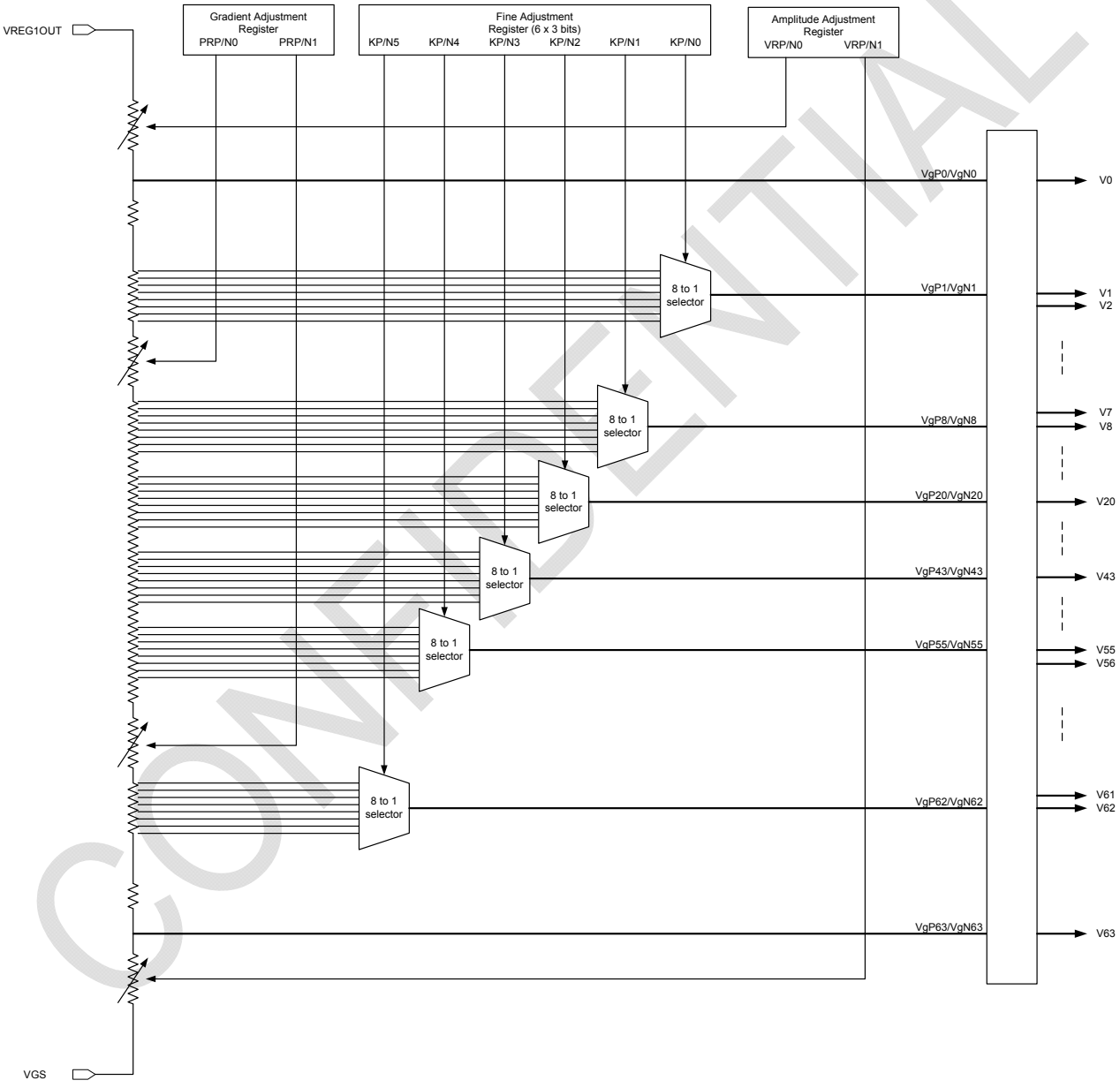


Figure 35 Structure of gamma correction function

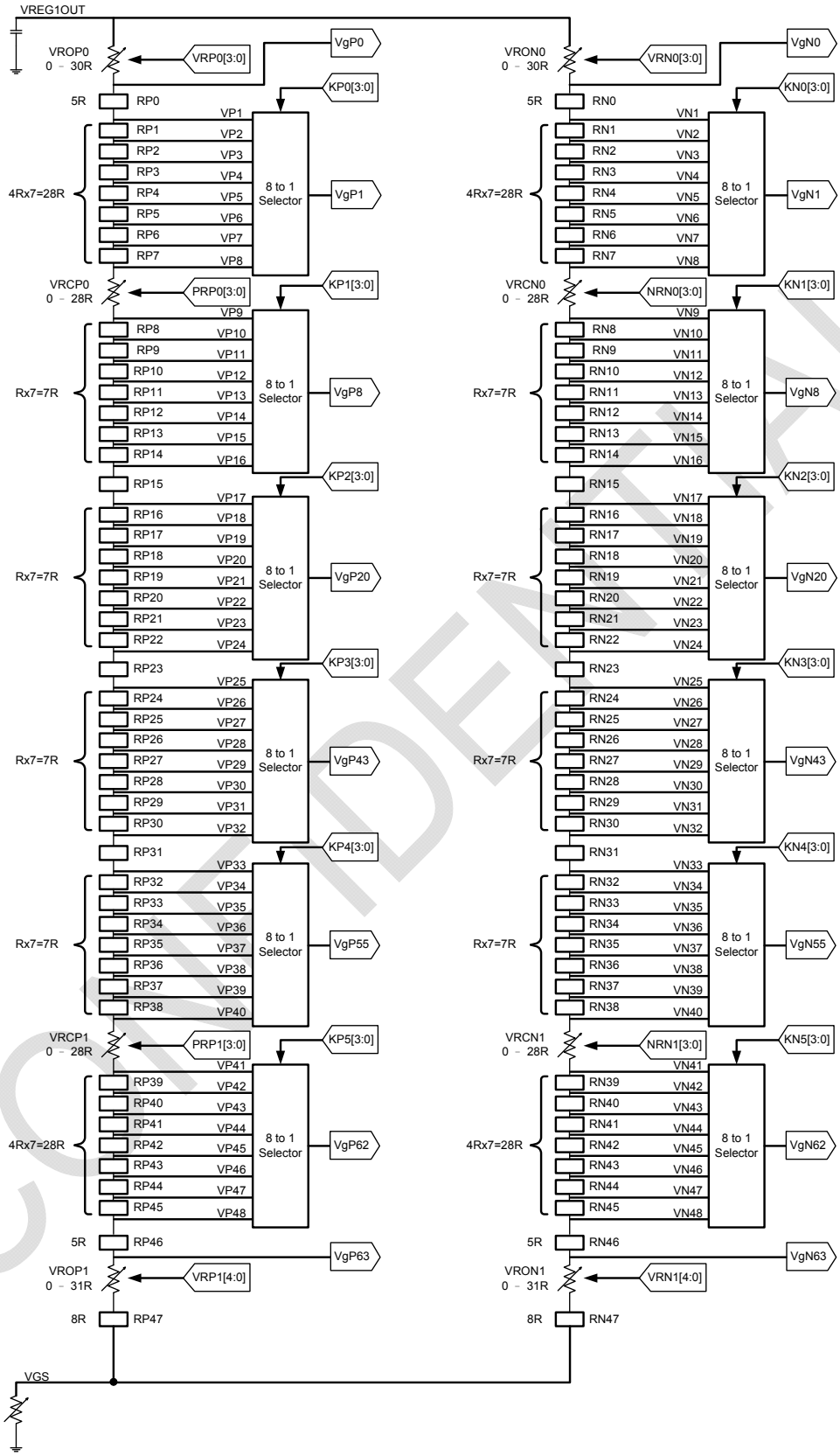


Figure 36 Grayscale Voltage Adjustment

1. Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale reference voltage level. To adjust the gradient, the resistance values of variable resistors in the middle of the ladder resistor are adjusted by registers PRP0[2:0]/PRN0[2:0], PRP1[2:0]/PRN1[2:0]. The registers consist of positive and negative polarity registers, allowing asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers, VRP0[3:0]/VRN0[3:0], VRP1[4:0]/VRN1[4:0], are used to adjust the amplitude of grayscale voltages. To adjust the amplitude, the resistance values of variable resistors at the top and bottom of the ladder resistor are adjusted. Same as the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

3. Fine adjustment registers

The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 8 levels for each register generated from the ladder resistor, in respective 8-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.

Register	Positive	Negative	Function
Gradient	PRP0 [2:0]	PRN1 [2:0]	Variable resistor VRCP0, VRCN0
	PRP1 [2:0]	PRN0 [2:0]	Variable resistor VRCP1, VRCN1
Amplitude	VRP0 [4:0]	VRN1 [4:0]	Variable resistor VROP0, VRON0
	VRP1 [4:0]	VRN0 [4:0]	Variable resistor VROP1, VRON1
Fine adjustment	KP0 [2:0]	KN5 [2:0]	8-to-1 selector (voltage level of V1)
	KP1 [2:0]	KN4 [2:0]	8-to-1 selector (voltage level of V8)
	KP2 [2:0]	KN3 [2:0]	8-to-1 selector (voltage level of V20)
	KP3 [2:0]	KN2 [2:0]	8-to-1 selector (voltage level of V43)
	KP4 [2:0]	KN1 [2:0]	8-to-1 selector (voltage level of V55)
	KP5 [2:0]	KN0 [2:0]	8-to-1 selector (voltage level of V62)

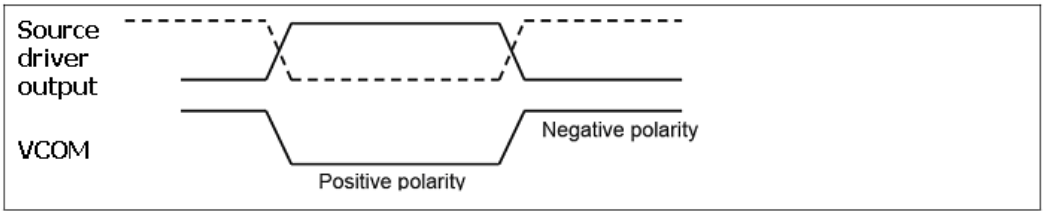


Figure 37 Source output waveform and VCOM polarity relationship

18.1 Ladder resistors and 8-to-1 selector Block configuration

The reference voltage generating block consists of two ladder resistor units including variable resistors and 8-to-1 selectors. Each 8-to-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the γ-correction registers. This unit has pins to connect a volume resistor externally to compensate differences in various characteristics of panels.

18.2 Variable resistors

RM68050 uses variable resistors for the following three purposes: gradient adjustment (VRCP(N)0/VRCP(N)1); amplitude adjustment (1) (VROP(N)0); and the amplitude adjustment (2) (VROP(N)1). The resistance values of these variable resistors are set by gradient adjustment registers and amplitude adjustment registers as follows.

Gradient adjustment	
PRP(N)0/1[2:0]	VRCP(N)0/1
3'h0	0R
3'h1	4R
3'h2	8R
3'h3	12R
3'h4	16R
3'h5	20R
3'h6	24R
3'h7	28R

Amplitude adjustment (1)	
VRP(N)0[3:0]	VROP(N)0
4'h0	0R
4'h1	2R
4'h2	4R
…	…
4'hD	26R
4'hE	28R
4'hF	30R

Amplitude adjustment (2)	
VRP(N)0[4:0]	VROP(N)0
5'h00	0R
5'h01	1R
5'h02	2R
…	…
5'h1D	29R
5'h1E	30R
5'h1F	31R

18.3 8-to-1 selectors

The 8-to-1 selector selects one of eight voltage levels generated from the ladder resistor unit according to the fine adjustment register and output the selected voltage level as a reference grayscale voltage (VgP(N)1~6). The table below shows the setting in the fine adjustment register and the selected voltage levels for respective reference grayscale voltages.

Fine Adjustment												
KP(N)[2:0]	VgP(N)1		VgP(N)8		VgP(N)20		VgP(N)43		VgP(N)55		VgP(N)62	
	voltage	resistor	voltage	resistor	voltage	resistor	voltage	resistor	voltage	resistor	voltage	resistor
3'h0	VP(N)1	0R	VP(N)9	0R	VP(N)17	0R	VP(N)25	0R	VP(N)33	0R	VP(N)41	0R
3'h1	VP(N)2	4R	VP(N)10	1R	VP(N)18	1R	VP(N)26	1R	VP(N)34	1R	VP(N)42	4R
3'h2	VP(N)3	8R	VP(N)11	2R	VP(N)19	2R	VP(N)27	2R	VP(N)35	2R	VP(N)43	8R
3'h3	VP(N)4	12R	VP(N)12	3R	VP(N)20	3R	VP(N)28	3R	VP(N)36	3R	VP(N)44	12R
3'h4	VP(N)5	16R	VP(N)13	4R	VP(N)21	4R	VP(N)29	4R	VP(N)37	4R	VP(N)45	16R
3'h5	VP(N)6	20R	VP(N)14	5R	VP(N)22	5R	VP(N)30	5R	VP(N)38	5R	VP(N)46	20R
3'h6	VP(N)7	24R	VP(N)15	6R	VP(N)23	6R	VP(N)31	6R	VP(N)39	6R	VP(N)47	24R
3'h7	VP(N)8	28R	VP(N)16	7R	VP(N)24	7R	VP(N)32	7R	VP(N)40	7R	VP(N)48	28R

19. Power-Supply Generating Circuit

19.1 Voltage Setting Pattern Diagram

The following are the diagrams of voltage generation in the RM68050 and the TFT display application voltage waveforms and electrical potential relationship.

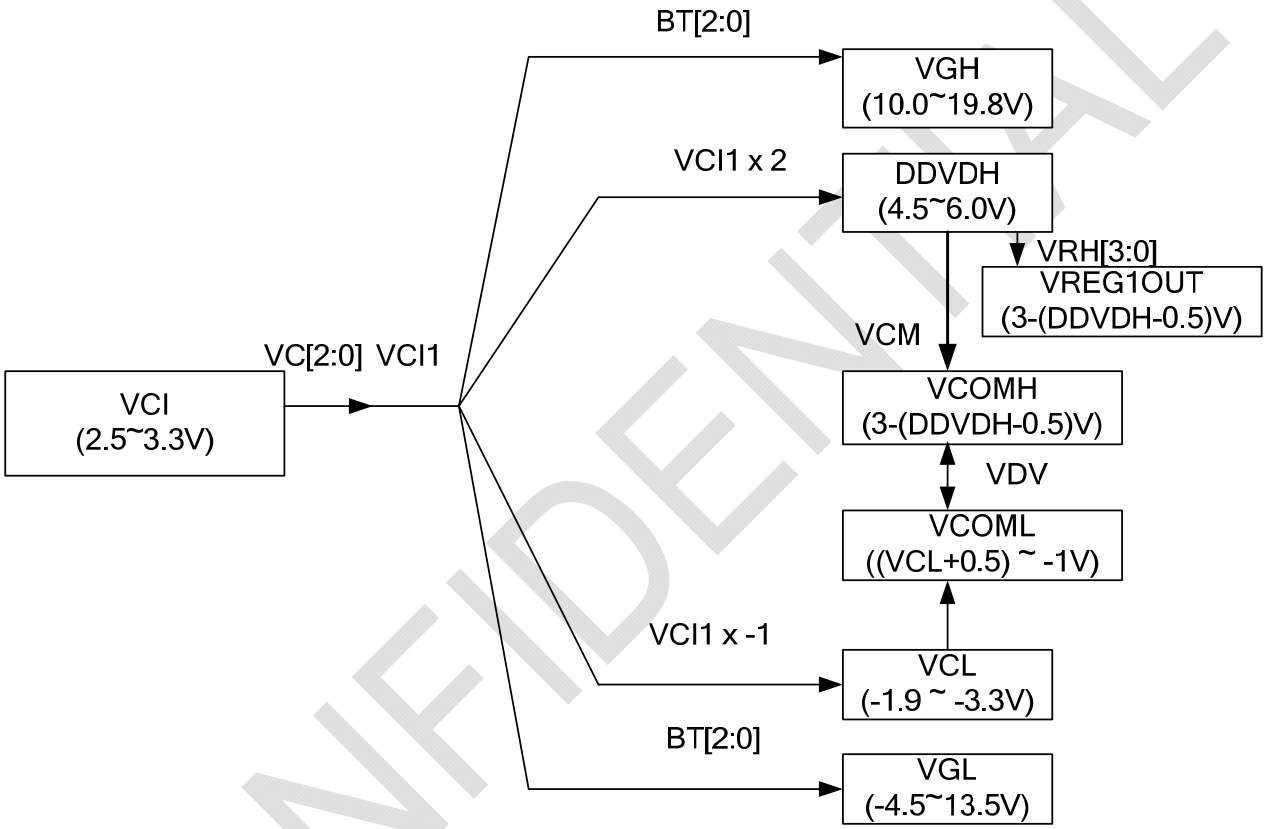


Figure 38 Diagram of voltage generation

Notes:

1. The DDVDH, VGH, VGL, and VCL output voltages will become lower than their theoretical levels (ideal voltages) due to current consumption at each output level. Make sure that output voltage level in operation maintains the following relationship: (DDVDH – VREG1OUT) ≥ 0.5V, (VCOML – VCL) > 0.5V. Also make sure VGH-VGL ≤ 28V, VCI-VCL ≤ 6V. When the alternating cycle of VCOM is high (e.g. polarity inverts every line cycle), current consumption will increase. In this case, check the voltage before use.
2. In operation, setting voltages within the respective voltage ranges are recommended.

19.2 Liquid crystal application voltage waveform and electrical potential

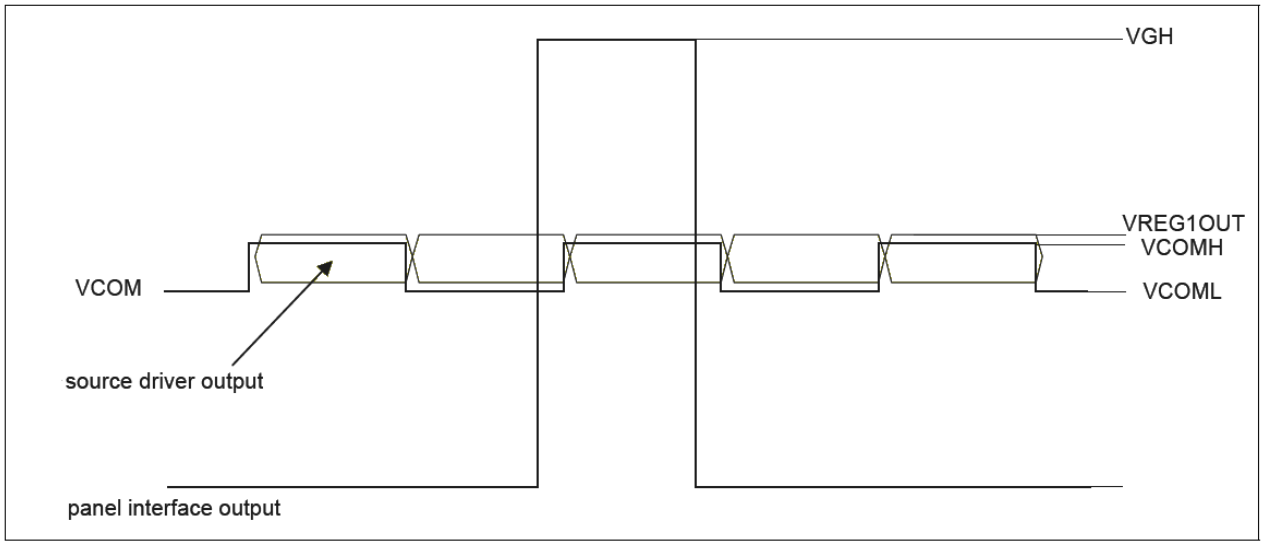


Figure 39 Voltage output to TFT LCD Panel

20. OTP control sequence

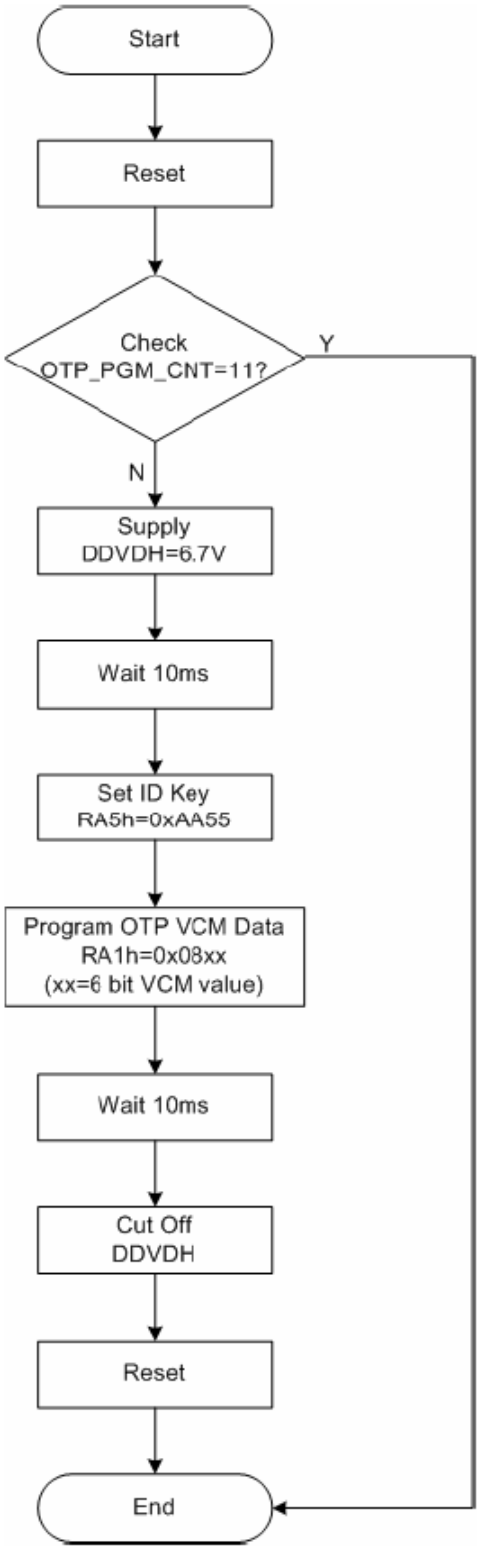
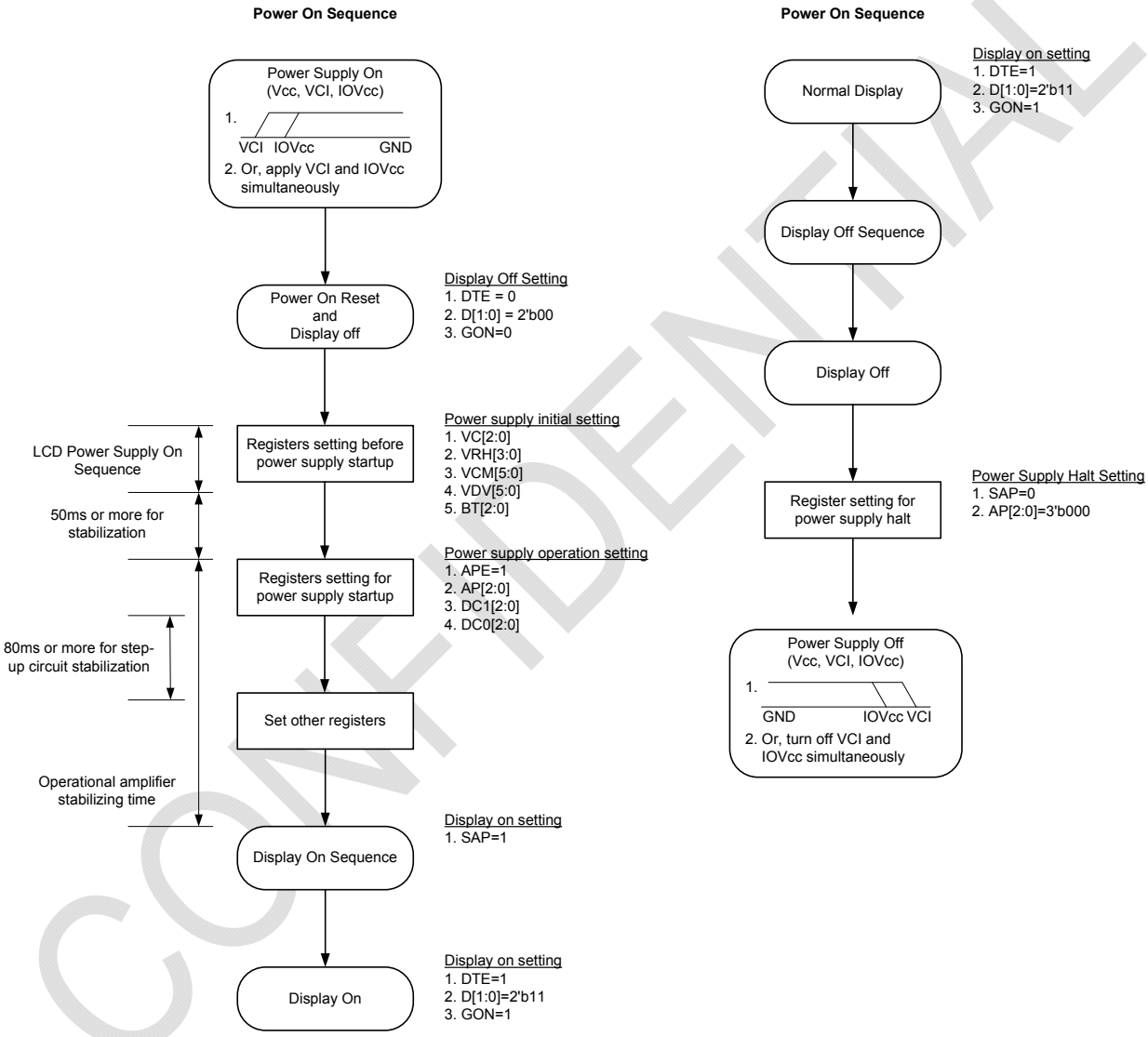


Figure 40 OTP control sequence diagram

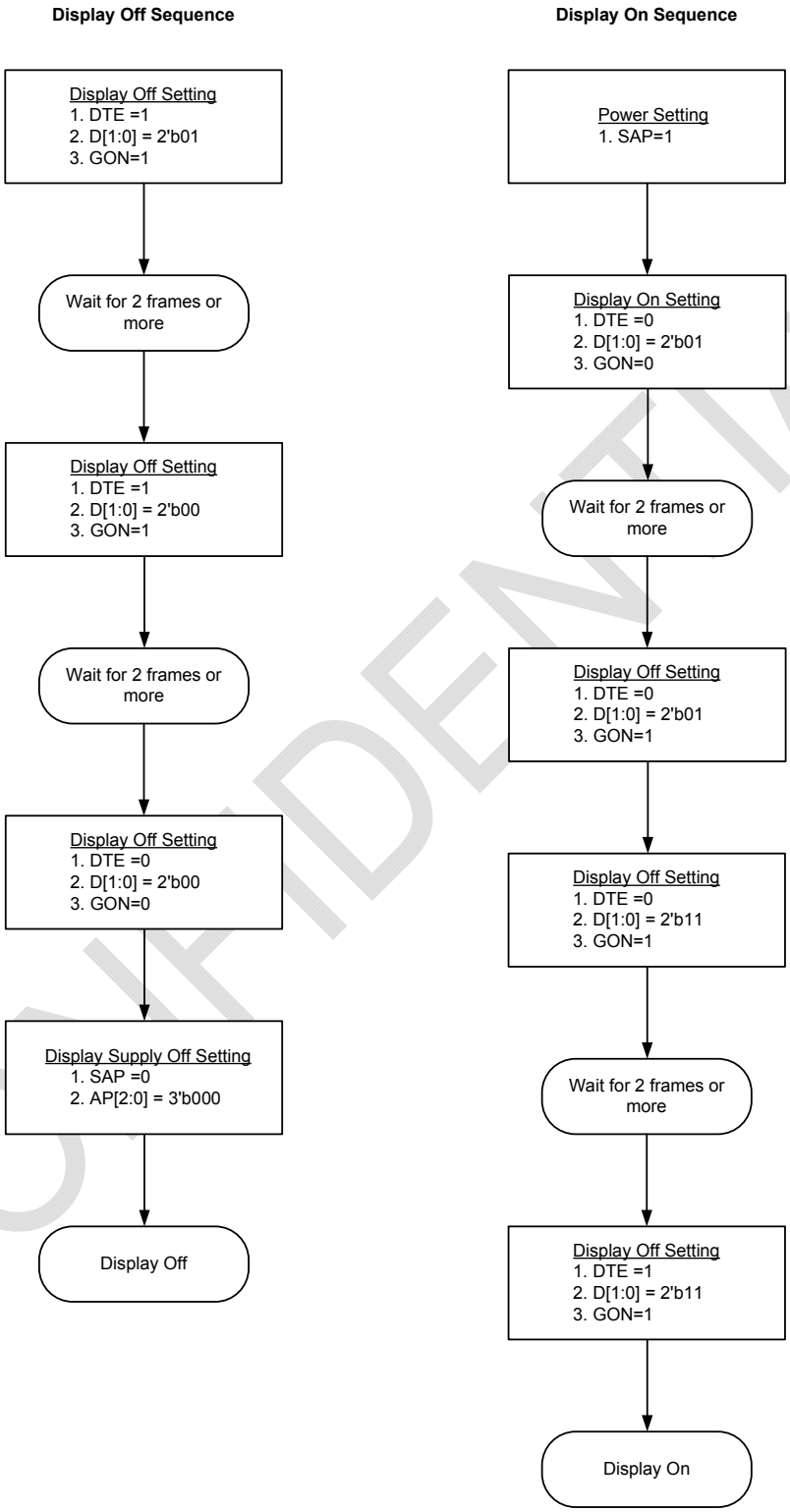
21. Power Supply Instruction Setting

The following are the sequences for setting power supply ON/OFF instructions. Set power supply ON/OFF instructions according to the following sequences in Display ON/OFF, Sleep set/exit sequences.

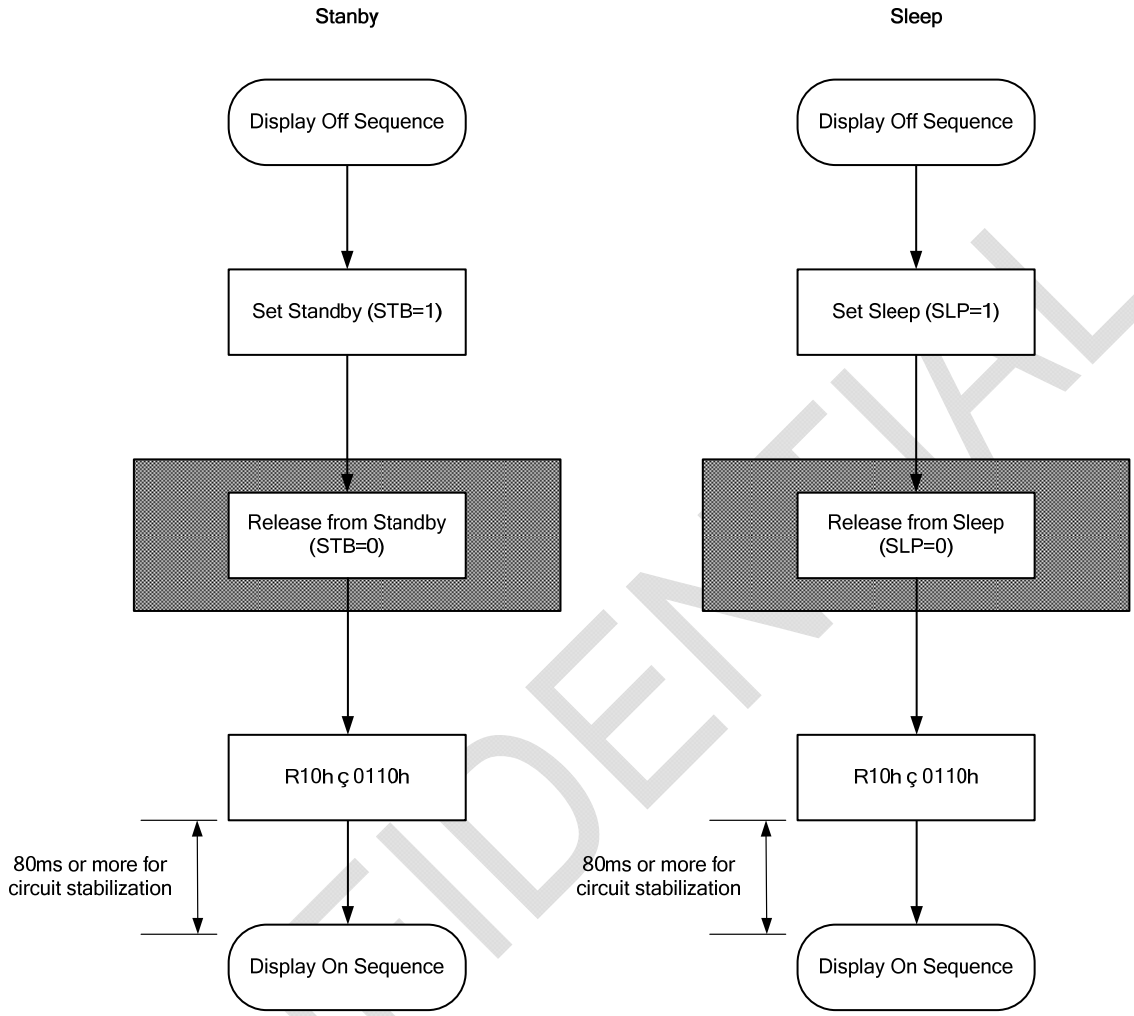
21.1 Power Supply Instruction Setting



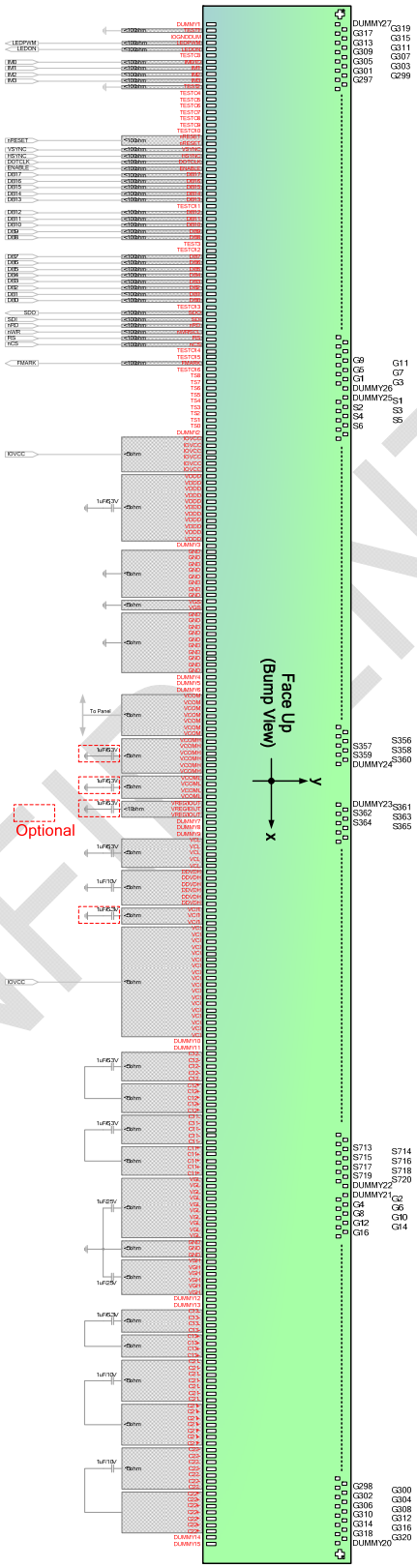
21.2 Display On / Off Instruction Setting



21.3 Sleep mode/Standby mode SET/EXIT sequence



22. Application Circuit



23. Absolute Maximum Ratings

Table 17

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	VCI, IOVCC	V	-0.3 ~ +4.6	1, 2
Power Supply Voltage 2	VCI – GND	V	-0.3 ~ +4.6	1, 3
Power Supply Voltage 3	DDVDH –GND	V	-0.3 ~ +6.0	1, 4
Power Supply Voltage 4	AGND – VCL	V	-0.3 ~ +4.6	1
Power Supply Voltage 5	DDVDH – VCL	V	-0.3 ~ +9.0	1, 5
Power Supply Voltage 6	VGH – GND	V	-0.3 ~ +18.5	1, 6
Power Supply Voltage 7	GND – VGL	V	-0.3 ~ +18.5	1
Input Voltage	Vt	V	-0.3 ~ IOVCC + 0.3	1
Operating Temperature	Topr	℃	-40 ~ +85	1, 7
Storage Temperature	Tstg	℃	-55 ~ +110	1, 7

Notes:

1. The absolute maximum rating is listed on table above. When RM68050 is used out of the absolute maximum ratings, the RM68050 may be permanently damaged. To use the RM68050 within the following electrical characteristics limit is strongly recommended for normal operation. If exposed to the condition not within the electrical characteristics, it may affect the reliability of the device.
2. Make sure VCI(high)≥DGND(low), IOVCC(high)≥DGND(low).
3. Make sure VCI(high)≥DGND(low).
4. Make sure DDVDH(high)≥AGND(low)
5. Make sure DDVDH(high) ≥VCL(low).
6. Make sure AGND(high)≥VGL(low)..

24. Electrical Characteristics

24.1 DC Electrical Characteristics

(VCC = 2.50V ~ 3.30V, IOVCC = 1.65V ~ 3.30V, Ta= -40℃~+85℃)

Item	Symbol	Unit	Test Condition	Min.	Typ	Max.
Input “High” level voltage	V_{IH}	V	IOVCC = 1.65V~3.30V	0.80 x IOVCC	-	IOVCC
Input “Low” level voltage	V_{IL}	V	IOVCC = 1.65V~3.30V	-0.3	-	0.2 x IOVCC
Output “High” level voltage 1 (DB0-17, FMARK)	V_{OH}	V	IOVCC = 1.65V~3.30V IOH = -0.1mA	0.80 x IOVCC	-	-
Output “Low” level voltage 1 (DB0-17, FMARK)	V_{OL}	V	IOVCC = 1.65V~3.30V IOL = 0.1mA	-	-	0.2 x IOVCC
Input/Output leak current	I_{LI}	uA	Vin = 0~IOVCC	-0.1	-	0.1
Current Consumption (IOVCC-IOGND)+(VCC-GND) Normal operation mode (262k-colors, display operation)	I_{OP1}	uA	fosc=512kHz (320line drive), IOVCC=VCC=2.80V, Ta=25℃, RAM data: 18’h000000	--	TBD	--
Current Consumption (IOVCC-IOGND)+(VCC-GND) Deep standby mode	I_{DST}	uA	IOVCC=VCC=2.80V, Ta=25℃	-	1	--
LCD Power Supply Current (VCI-GND) 262k-color display operation	Ici1	mA	IOVCC=VCC=2.80V, ddvdh=5.20V, VREG1OUT=4.8V, Frame Rate=70Hz, Ta=25, RAM data: 18’h000000, line-inversion	-	TBD	--
Output Voltage dispersion	ΔV_O	mV	-	-	TBD	-
Average output voltage variance	ΔV_Δ	mV	-	-	TBD	-

24.2 AC Timing Characteristics

24.2.180-System Bus Interface

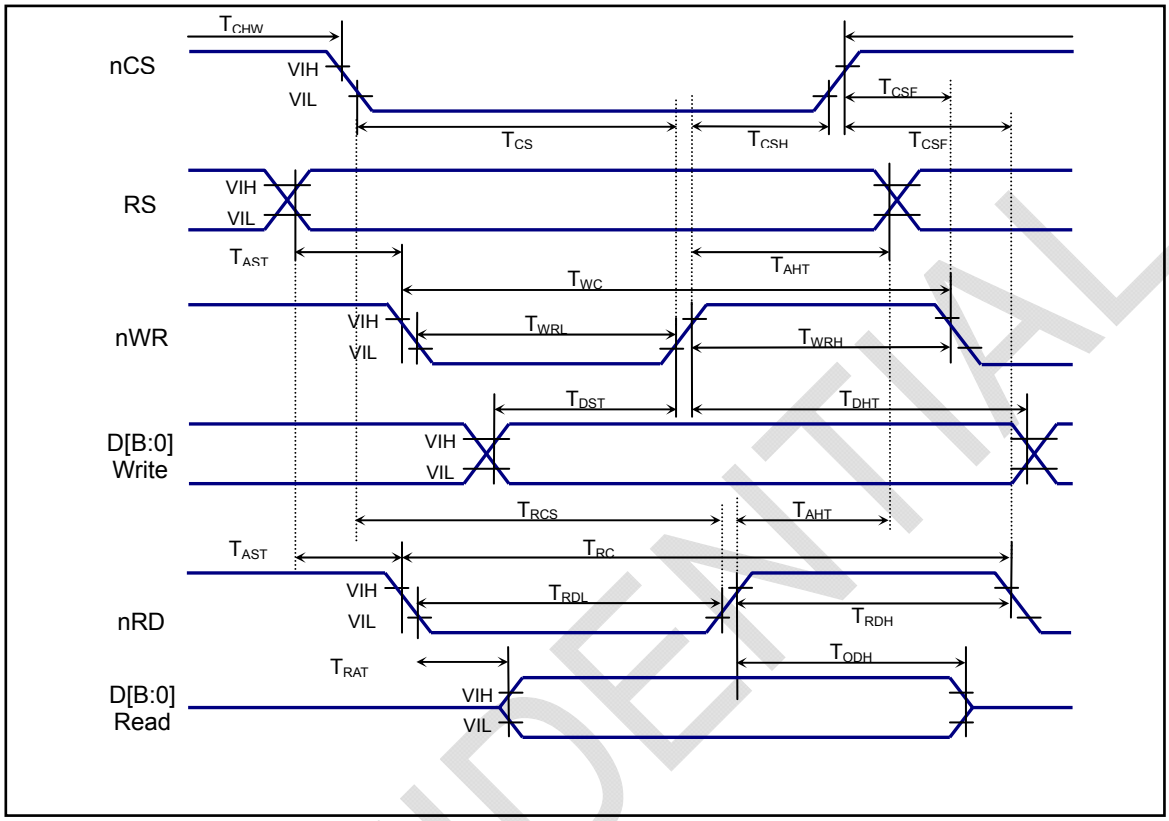


Figure 41 80-system Bus Interface

Normal Write Mode (IOVCC = 1.65~3.3V, VCC=2.4~3.3V)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
RS	T_{AST}	Address setup time	10		ns	-
	T_{AHT}	Address hold time (Write/Read)	5		ns	
nCS	T_{CHW}	Chip select “H” pulse width	0		ns	
	T_{CS}	Chip select setup time (Write)	10		ns	
	T_{RCS}	Chip select setup time (Read)	5		ns	
nWR	T_{WC}	Write cycle	100		ns	
	T_{WRH}	Control pulse “H” duration	50		ns	-
	T_{WRL}	Control pulse “L” duration	50		ns	
nRD (ID)	T_{RC}	Read cycle	300		ns	
	T_{RDH}	Control pulse “H” duration	150		ns	-
	T_{RDL}	Control pulse “L” duration	150		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	-
	T_{DHT}	Data hold time	15		ns	
	T_{RAT}	Read access time		100	ns	
	T_{ODH}	Output disable time	5		ns	

24.2.2 Clock Synchronous Serial Interface

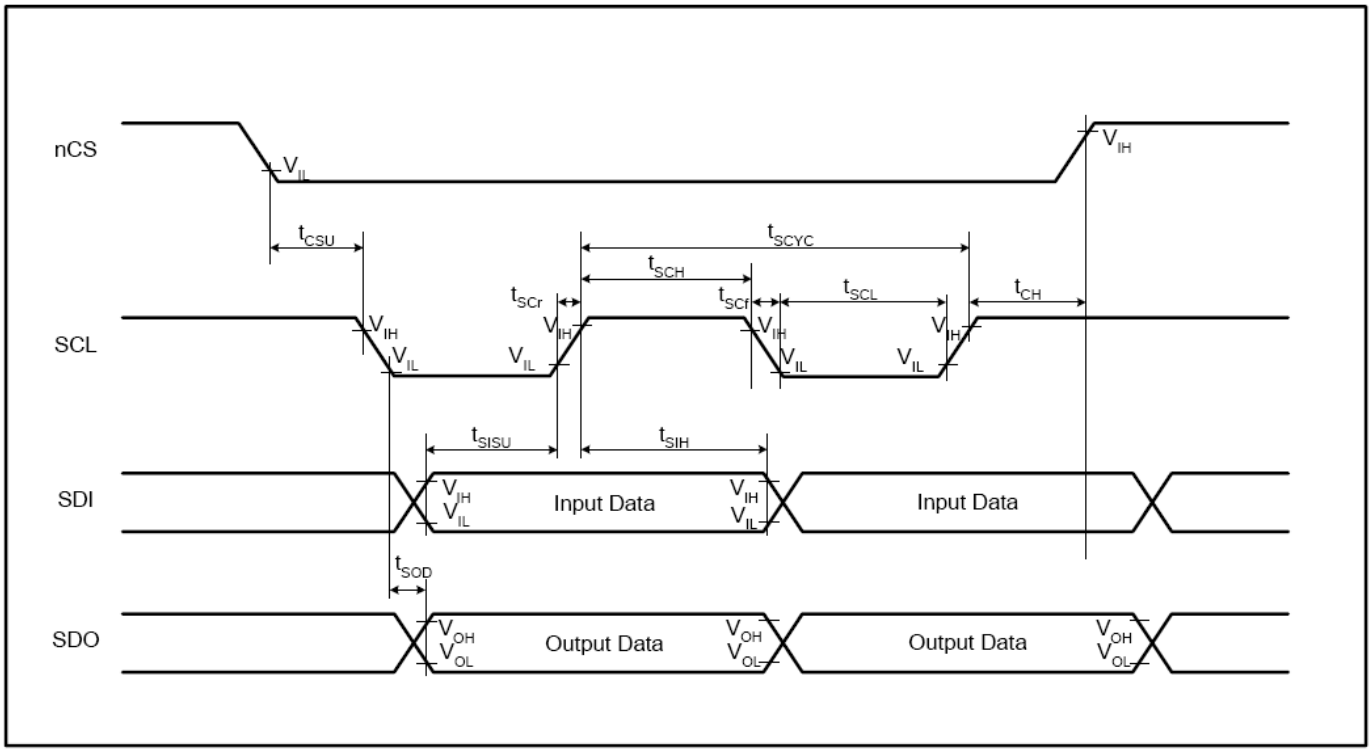


Figure 42 Clock Synchronous Serial Interface

IOVCC = 1.65~3.3V, VCC=2.4~3.3V

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
SCL	T_{SCYC}	Clock cycle (Write)	100		us	-
	T_{SCYC}	Clock cycle (Read)	200		us	
	T_{SCH}	Clock “H” pulse width (Write)	40		ns	
	T_{SCH}	Clock “H” pulse width (Read)	100		ns	
	T_{SCL}	Clock “L” pulse width (Write)	40		ns	
	T_{SCL}	Clock “L” pulse width (Read)	100		ns	
	T_{SCr}	Clock rise time		5	ns	
	T_{SCf}	Clock fall time		5	ns	
nCS	T_{CSU}	Chip select setup time	10		ns	
	T_{CH}	Chip select hold time	50		ns	-
	T_{WRL}	Control pulse “L” duration	15		ns	
SDI	T_{SISU}	Data input setup time	20		ns	-
	T_{SIH}	Data input hold time	20		ns	
SDO	T_{SOD}	Data output setup time		100	ns	-
	T_{SOH}	Data output hold time	5		ns	

24.2.3 RGB Interface

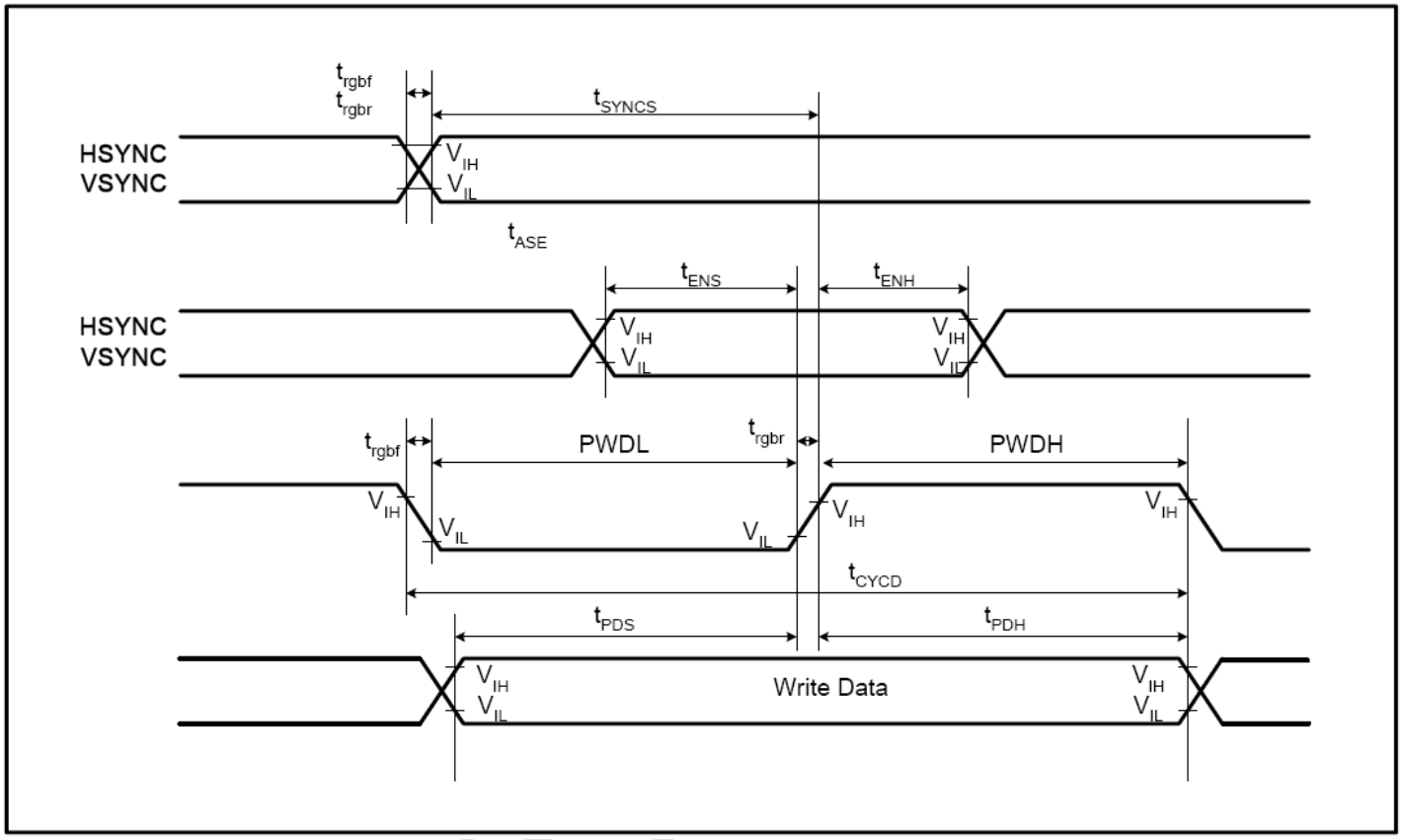


Figure 43 Timing chart for RGB Interface

18/16-bit Bus RGB Interface Mode (IOVCC = 1.65~3.3V, VCC=2.4~3.3V)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
VSYNC	T_{SYNCS}	VSYNC setup time	0		ns	-
	T_{rghr}	VSYNC rise time		25	ns	
	T_{rghf}	VSYNC fall time		25	ns	
HSYNC	T_{SYNCS}	HSYNC setup time	0		ns	-
	T_{rghr}	HSYNC rise time		25	ns	
	T_{rghf}	HSYNC fall time		25	ns	
ENABLE	T_{ENS}	ENABLE setup time	10		ns	-
	T_{ENH}	ENABLE hold time	10		ns	
DB[17:0]	T_{PDS}	Data input setup time	10		ns	-
	T_{PDH}	Data input hold time	40		ns	
DOTCLK	PWDH	DOTCLK “H” pulse width	40		ns	-
	PWDL	DOTCLK “L” pulse width	40		ns	
	T_{CYCD}	DOTCLK clock cycle	100			
	T_{rghr}	DOTCLK rise time		25	ns	
	T_{rghf}	DOTCLK fall time		25	ns	

6-bit Bus RGB Interface Mode (IOVCC = 1.65 ~ 3.3V, VCC=2.4~3.3V)

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
VSYNC	T_{SYNCS}	VSYNC setup time	0		ns	-
	T_{rghr}	VSYNC rise time		25	ns	
	T_{rghf}	VSYNC fall time		25	ns	

HSYNC	T_{SYNCS}	HSYNC setup time	0		ns	-
	T_{rghr}	HSYNC rise time		25	ns	
	T_{rghf}	HSYNC fall time		25	ns	
ENABLE	T_{ENS}	ENABLE setup time	10		ns	-
	T_{ENH}	ENABLE hold time	10		ns	
DB[17:0]	T_{PDS}	Data input setup time	10		ns	-
	T_{PDH}	Data input hold time	30		ns	
DOTCLK	PWDH	DOTCLK “H” pulse width	30		ns	-
	PWDL	DOTCLK “L” pulse width	30		ns	
	T_{CYCD}	DOTCLK clock cycle	80			
	T_{rghr}	DOTCLK rise time		25	ns	
	T_{rghf}	DOTCLK fall time		25	ns	

24.3 Reset Timing Characteristics

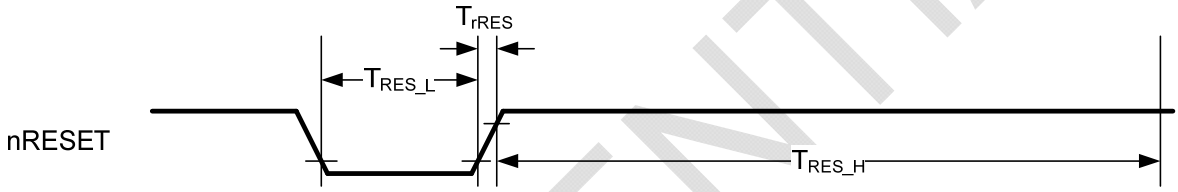


Figure 44 Reset Operation

Reset Timing Characteristics (VCC = 1.8 ~ 3.3 V, IOVCC = 1.65 ~ 3.3 V)

Item	Symbol	MIN	MAX	Unit	Description
Reset low-level width	T_{RES_L}	1		ns	-
Reset rise time	T_{rRES}		10	us	-
Reset high-level witdth	T_{RES_H}	50		ns	-