BeagleBone System Reference Manual

Revision 0.3
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Table of Contents

Figures

Tables

1.0 Introduction

This document is the high level design Specification for the BeagleBone board.

This document is a work in progress and will be updated frequently.

2.0 Change History

Table 1. Change History

Rev	Changes	Date	By
0.1	Original Release for review	August 22, 2011	GC
0.2	Updated added features	August 25, 2011	GC
0.2	Added more details	August 28, 2011	GC

3.0 BeagleBone Overview

The BeagleBone is designed specifically to address the Open Source Community, early adopters, and potential customers. It has been equipped with a minimum set of features to allow the user to experience the power of the processor and is not intended as a full development platform as many of the features and interfaces supplied by the processor are not accessible from the BeagleBone via onboard support of some interfaces.

By utilizing comprehensive expansion connectors, the BeagleBone is highly extensible to add many features and interfaces. A majority of the signals from the processor are exposed via the expansion headers and can be accessed there, but may require additional hardware in order to use them. This will be handled by the creation of various daughter cards. Due to the deep multiplexing of the pins, there are limits as to how many interfaces can coexist at any one time.

All of the design information will be freely available and can be used as the basis for a product or design. If the user decides to use the BeagleBone design in a product, they assume all responsibility for such use and are totally responsible for all aspects of its use.

4.0 BeagleBone Features and Specification

This section covers the specifications and features of the BeagleBone and provides a high level description of the major components and interfaces that make up the BeagleBone.

Table 2 provides a list of the BeagleBone's features.

Table 2. BeagleBone Features

	Feature	
Processor	720MHZ AM3359 15x15	
Memory	256MB DDR2 400MHZ (128MB Optional)	
PMIC TPS65217	Power Regulators	
	LiION Single cell battery charger (via expansion*)	
	20mA LED Backlight driver, 39V, PWM (via expansion*)	
	*(Additional components required)	
Debug Support	USB to Serial Adapter	miniUSB connector
	On Board JTAG via USB	4 USER LEDs
		Optional 20-pin CTI JTAG
Power	USB	5VDC External jack
PCB	3.4" x 2.1"	6 layers
Indicators	Power	
	4-User Controllable LEDs	
HS USB 2.0 Client Port	Access to the USB1 Client mode	
HS USB 2.0 Host Port	USB Type A Socket, 500mA LS/FS/HS	
Ethernet	10/100, RJ45	
SD/MMC Connector	microSD , 3.3V	
User Interface	1-Reset Button	
Overvoltage Protection	Shutdown @ 5.6V MAX	
Expansion Connectors	Power 5V, 3.3V , VDD_ADC 3.3V I/O on all signals McASP0, SPI1, I2C, GPIO(65), LCD, GPMC, MMC1, MMC2, 7 AIN(1.8V MAX), 4 Timers, PRI_MII0, 3 Serial Ports, CAN0, EHRPWM(0,2),XDMA Interrupt, Power button, Battery Charger, LED Backlight, Expansion Board ID (Up to 3 can be stacked)	

NOTE: DUE TO MULIPLEXING ON THE PROCESSOR, ALL OF THESE EXPANSION SIGNALS CANNOT BE AVAILABLE AT THE SAME TIME.

The following sections provide more detail on each feature and sections of the board,..

4.1 Board Component Locations

The figures below show the PRELIMINARY component locations on the PCB layout.

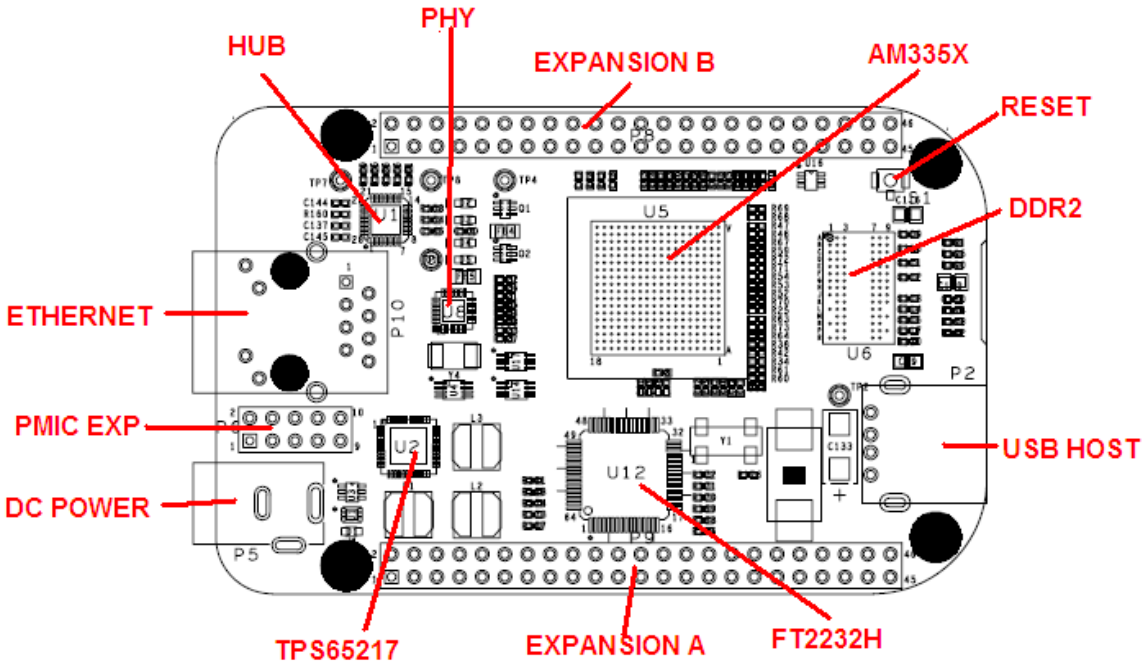

Figure 1. Top Side Components

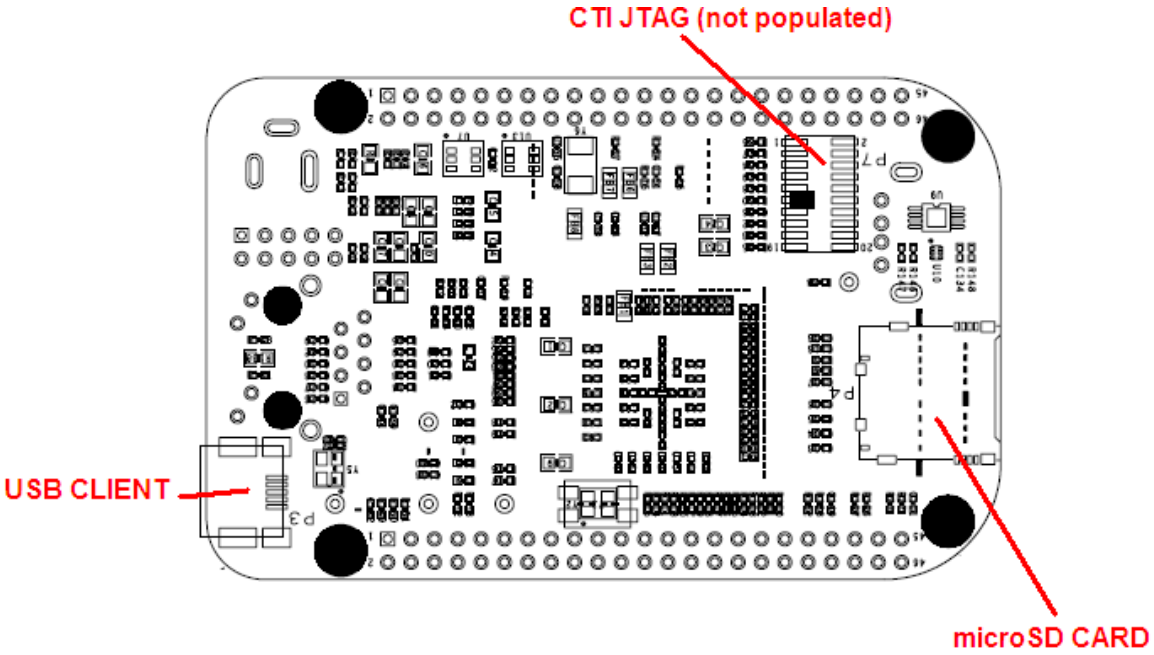

Figure 2. Bottom Side Components

Figure 3 shows a profile comparison between the BeagleBone and the other BeagleBoards.

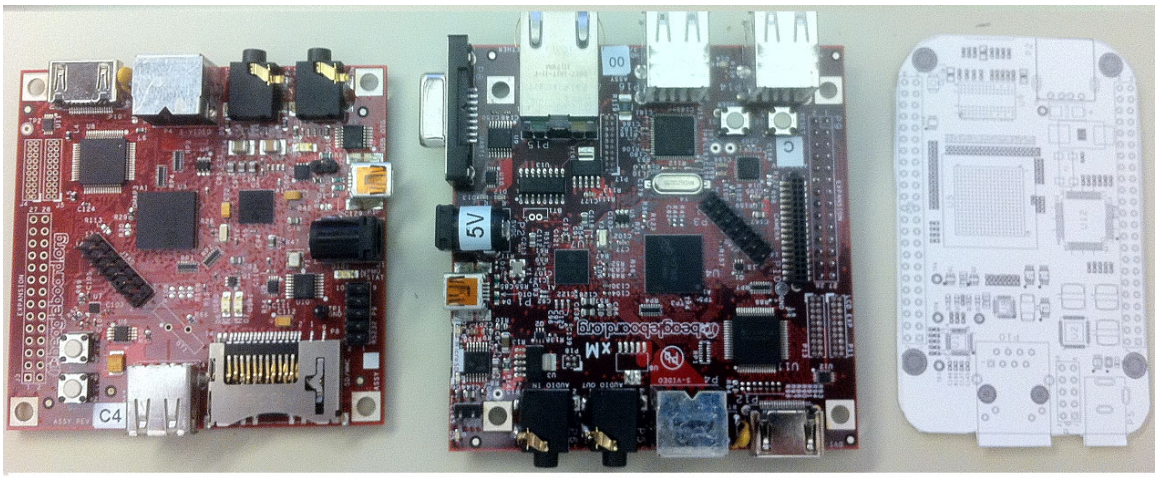

Figure 3. Profile Comparison

5.0 BeagleBone Design Specification

5.1 Processor

The board uses the AM3358 processor in the 15x15 package. Actual processor speed will be determined by the actual devices supplied. Initial units may have AM3359 due to availability of those parts in the 15x15 package.

5.2 Memory

One x16 bit DDR2 memory devices are used. The design supports 128MB or 256MB of memory. The standard configuration is 256MB and 400MHz. A 128MB version may be built later, but there are no definite plans for this.

A single 2KB EEPROM is provided on I2C0 that conforms to the same information as supplied on the EVM. This information includes board name, serial number, and revision information. The device does not have the same amount of unused space as provided on the EVM as it uses a smaller and less expensive device. Information will conform to the same standard as is found on the EVM.

5.3 Power Management

The TPS65127 power management device is used. This is the same device that is used by several key customers. SW support is already scheduled and is required by those customers. The board should have no issues powering up and running with no SW support required. The TPS65217 is based on an existing device and is a EEPROM change to create the desired operation with the AM3358 processor. RTP is scheduled for December 2011 and there should be no issues in obtaining sufficient parts to meet the schedule.

This part allows for a much simpler layout due to less power rails. It also provides a cost saving feature like an integrated USB and DC power switchover internal to the device.

Other features include:

- Integrated charger for a single cell LiION battery
- Integrated LED supply for an LCD backlight
- Ability to measure power consumption of the board via the processor

Access to the battery charger and backlight will require additional components to be added to the daughter card to take advantage of these features.

5.4 PC USB Interface

The board will have an onboard USB HUB that concentrates two USB ports used on the board to one to facilitate the use of a single USB connector and cable to the PC. Support via this HUB includes:

- USB to serial debug
- USB to JTAG
- USB processor port access

When connected to the PC each of these will show up as ports to the PC.

5.4.1 Serial Debug Port

Serial debug is provided via UART0 on the processor using a dual channel FT2232H USB to serial device from FTDI Serial signals include Tx, Rx, RTS, and CTS.

A single EEPROM is provided to allow for the programming of the vendor information so that when connected the board can be identified and the appropriate driver installed.

5.4.2 JTAG Port

The second port on the FT2232H will be used for the JATG port. Direct connection to the processor is made from the FT2232H.

5.4.3 USB1 Port

The HUB connects direct to the USB1 port on the processor.

5.5 MicroSD Connector

The board is equipped with a single microSD connector to act as the primary boot source for the board. A 2GB microSD card is supplied with each board.

5.6 USB Host Port

On the board a single USB Type A connector with full LS/FS/HS support. The port can provide power on/off control and up to 500mA of current at 5V. Under USB power, the board will not be able to supply the full 500mA, but should be sufficient to supply enough current for a lower power USB device.

You can use a wireless keyboard/mouse configuration or you can add a HUB for standard keyboard and mouse interfacing if required.

5.7 USB Client Port

Access to USB1 is provided via the onboard USB Hub. It will show up on a PC as a standard USB device..

5.8 Power Sources

The board can be powered from a USB port on a PC or from an optional 5VDC power supply. The power supply is not provided with the board.

5.9 Power Connector

Power can be supplied via a 2.1mm x 5.5mm center connector when connected to a positive power supply rated at 5VDC +/- .1V and 2A. This is the same power supply as currently used on BeagleBoards. Actual power requirements of the supply are TBD.

5.10 Reset Button

When pressed and released, causes a warm reset of the board.

5.11 Indicators

There are four green LEDs on the board that can be controlled by the user and one static LED.

- One power LED that indicates that power is applied.
- Four Green LEDs that can be controlled via the SW by setting GPIO ports.

5.12 CTI JTAG Header

An optional 20 pin CTI JTAG header can be provided on the board to facilitate the SW development and debugging of the board by using various JTAG emulators. In order to use the connector, series resistors must be removed to isolate the USB to JTAG feature. This header is not supplied standard on the board and the typical user will not be able to make the resistor changes. A spate SKU will be the better solution.

6.0 Expansion Interface

This section describes the expansion interface and the features and functions available from the expansion header.

6.1 Expansion Header

Two 46 pin dual row .1 x .1 female headers are supplied on the board for access to the expansion signals. Due to the number of pins, a low insertion force header will be chosen to facilitate the removal of the daughter boards. The header is numbered left to right. **Figure 4** below is the pinout and a picture of the header used.

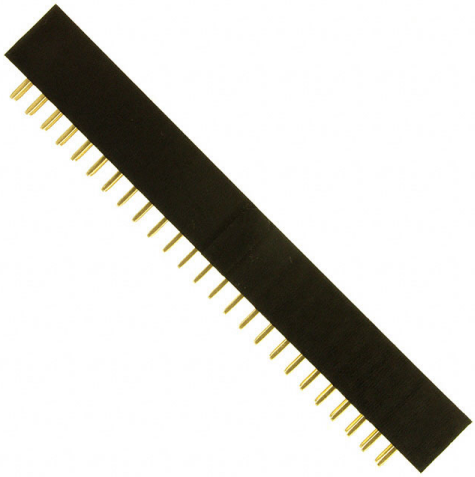

Figure 4. Expansion Connector

6.2 Daughter Boards

Each daughter board will have 2 60 pin male headers on the bottom of the board and a female socket on the top of the board to allow stacking. The connectors will be SMT connectors.

Up to three daughter boards can stacked onto the main board. Each daughterboard will have the same EEPROM as is found on the main board but will be at different addresses to allow for scanning for daughter boards, Based on the design of the daughter board, the address is automatically set based on the position the card is in the stack.

Standard daughter board size is 3.25” x 2.25”. The daughter board will have a notch in it to act as a key to insure proper orientation. The key is around the Ethernet connector on the main board.

Oversize boards, such as LCD panels, are allowed. The main board will extend out form under these boards and the keying notch must be provided.

6.3 Exposed Functions

This section covers functionality that is accessible from the expansion header.

NOTE: Not all functionality is available at the same time due to the extensive pin muxing of the signals on the processor.

6.3.1 LCD

A full 24 bit LCD panel can be supported. With the main board having backlight and touchscreen functionality, will simply and lower the cost of LCD daughter boards. Backlight power is limited to 25mA, so this may not be enough for larger panels.

If other functions are needed on an expansion board, such as NAND support, the full 24 bit display may not be able to be supported due to the pin muxing.

Signals supported are:

- DATA0-23,PCLK,HSYNC,VSYNC,ENABLE

6.3.2 GPMC

Access to the GPMC bus is provided. Depending on the configuration needed, this may result in the loss of the LCD interface.

Support for a 16 bit wide NAND is provided by the expansion board. This will limit the LCD display to 16Bits.

Signals supported are:

-

6.3.3 MMC

MMC1 signals are exposed on the expansion headers. Supported functions are:

- MMC1-D0-D7,CMD,CLK,CD

6.3.4 SPI

There are two SPI ports available on the expansion header.

- SPI0-DO,D1,CS,CLK
- SPI1-D0,D1,CLK,CS0,CS1

6.3.5 I2C

There are two I2c Ports on the expansion header, I2C1 and I2C2.

6.3.6 Serial Ports

There are five serial ports on the expansion headers. The supported ports are:

- **UART1**-TX,RX,RTS,CTS
- **UART2**-TX,RX,RTS,CTS
- **UART3**-TX,RX,RTS,CTS
- **UART4**-TX,RX,RTS,CTS
- **UART5**-TX,RX,CTS

6.3.7 A/D Converters

Seven 100K sample per second A to D converters are available on the expansion header.

NOTE: Maximum voltage is 1.8V. DO not exceed this voltage. Voltage dividers should be used for voltages higher than 1.8V.

6.3.8 GPIO

A maximum of 66 GPIO pins are accessible from the expansion header. All of these pins are 3.3V and can be configured as inputs or outputs. Any GPIO can be used as an interrupt and is limited to two interrupts per GPIO Bank for a maximum of eight pins as interrupts.

6.3.9 CAN Bus

There are two CAN bus interfaces available on the expansion header supporting CAN Version 2 parts A and B. The TX and RX digital signals are provided. The drivers and connectors will need to be provided on a daughter card for use.

6.3.10 TIMERS

There are four timer outputs on the expansion header.

6.3.11 PWM

There are up to eight PWM outputs on the expansion header.

- High Resolution Outputs- up to 6 single ended.
- ECAP PWM- 2 outputs

7.0 Detailed Board Design

This section describes the detailed design of the BeagleBone.

7.1 System Block Diagram

Figure 5 is the high level system block diagram of the board.

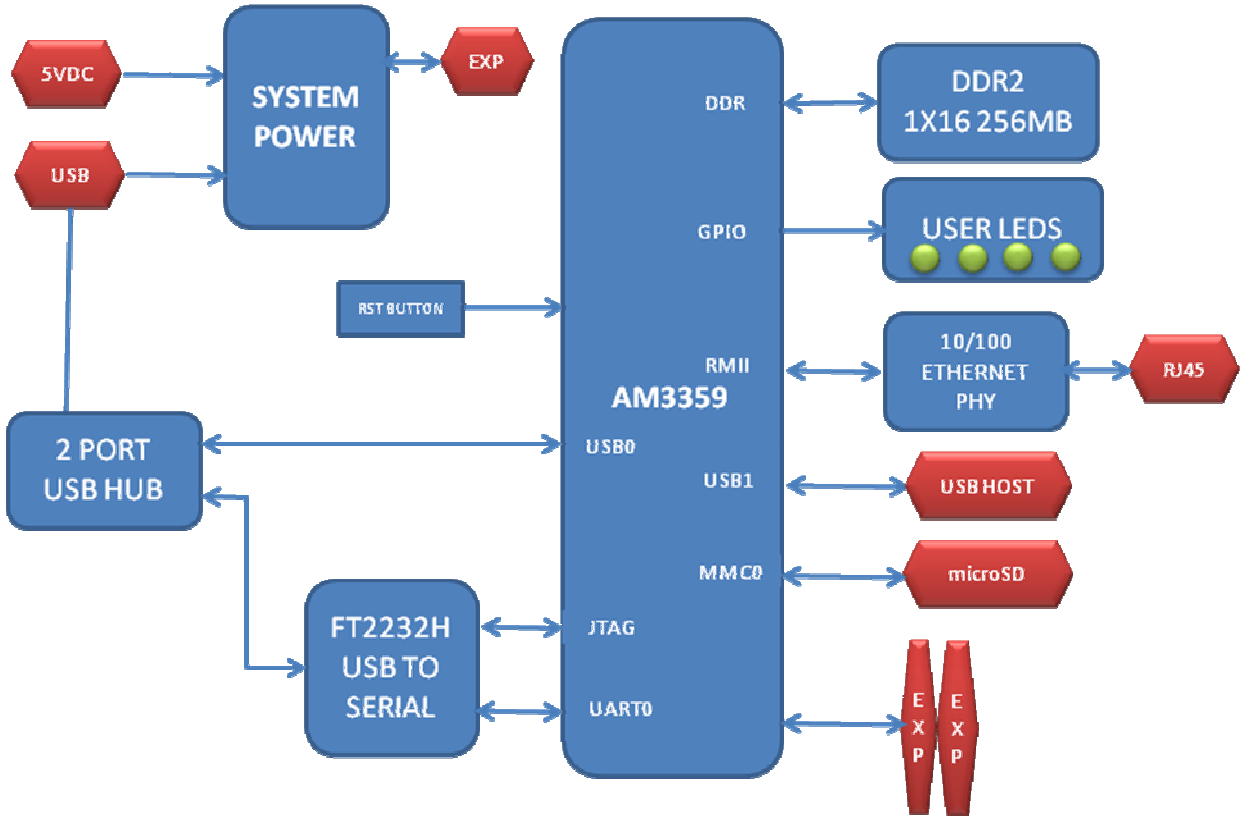

Figure 5. System Block Diagram

Each of these sections is discussed in more detail in the following sections.

7.2 Processor

The board is designed to use the AM335x processor in the 15 x 15 package. The exact version used is yet to be finalized as it depends on which device is available.

7.2.1 Processor Block Diagram

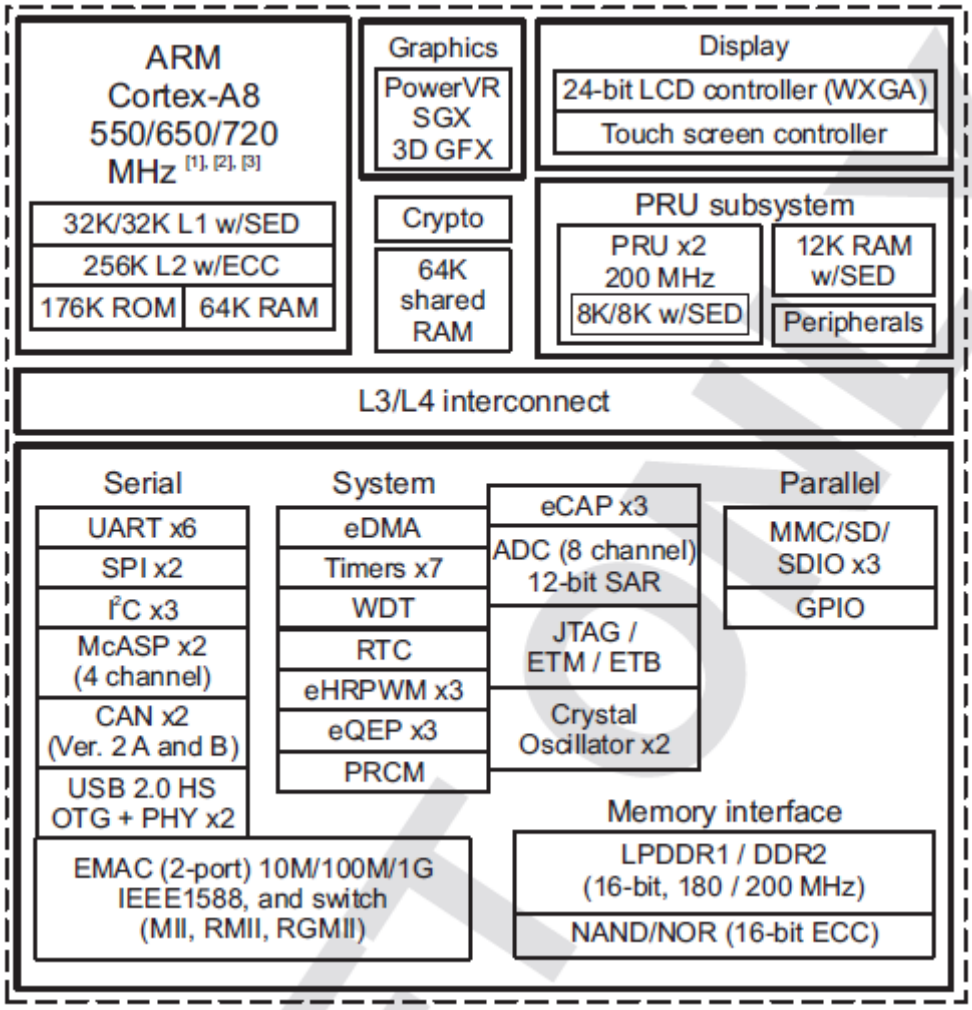

Figure 6. Processor Block Diagram

7.3 System Power

Figure 7 is a high level block diagram of the power section design.

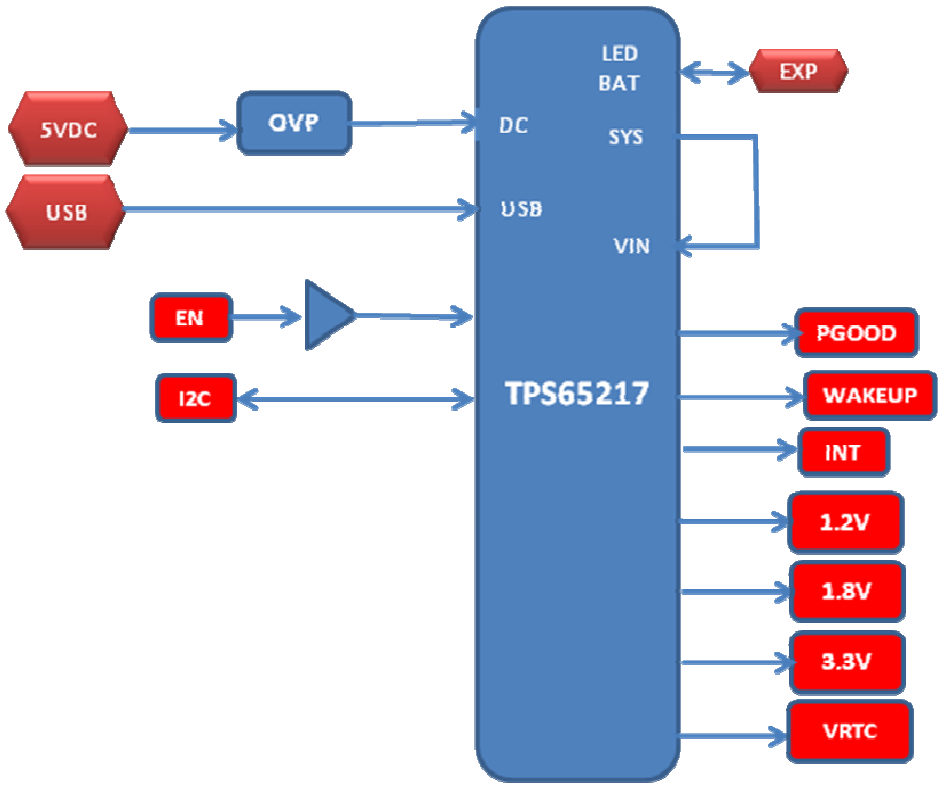

Figure 7. Power Subsection Block Diagram

7.3.1 5VDC Input

A 5VDC supply can be used to provide power to the board. The power supply current depends on how many and what type of daughter boards are connected to the board. For typical use a 5VDC +/1 .1V rated at 2A should be sufficient.

The connector used is a 2.1MM center positive x 5.5mm outer barrel. A NCP349 over voltage device is used to prevent the plugging in of 7 to 12 V power supplies by mistake. The NCP349 will shut down and the board will not power on. No visible indicator is provided to indicate that an over voltage condition exists. The board will not power up.

The 5VDC rail is connected to the expansion header. It is possible to power the board via the expansion headers from a daughter card. The 5VDC is also available for use by the daughter cards when the power is supplied by the 5VDC jack on the board.

7.3.2 USB Power

The board can also be powered from the USB port. A typical USB port is limited to 500mA max. When powering from the USB port, the 5VDC is not provided to the expansion header. So daughter cards that required that rail will not have that rail available for use.

7.3.1 Power Source Selection

The selection of either the 5VDC or the USB as the power source is handled internally to the TPS65217 via the I2C interface form the processor.

7.3.2 Power Sequencing

The power up process is made up of several stages and events. **Figure 8** is the events that make up the power up process of the system.

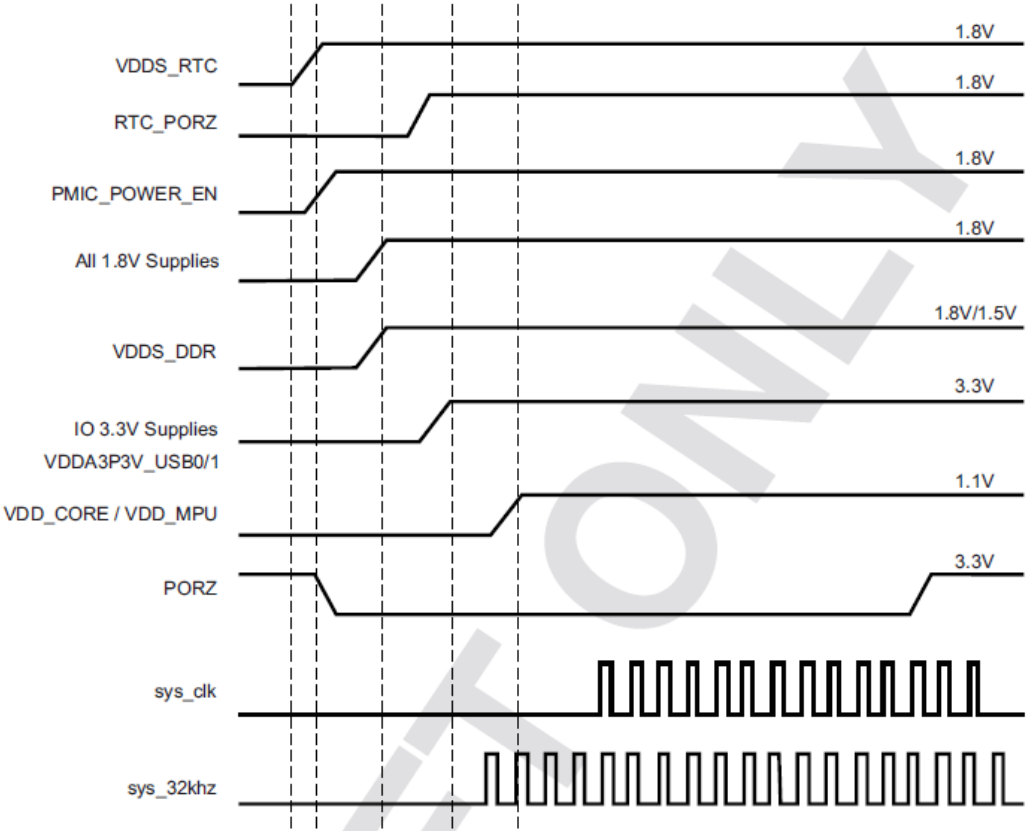

Figure 8. Power Sequencing

When voltage is applied, DC or USB, the TPS65217 connects the power to the SYS output pin which drives the switchers and LDOS in the TP65217.

At power up all switchers and LDOs are off except for the VRTC LDO (1.8V), provides power to the VRTC rail, and the VIO LDO (3.3V), which powers the I/O pins of the TPS65217. Once the RTC rail powers up, the RTC_PORZ pin of the processor can be release. **Figure 9** is the circuit that controls the RTZ_PORZ pin.

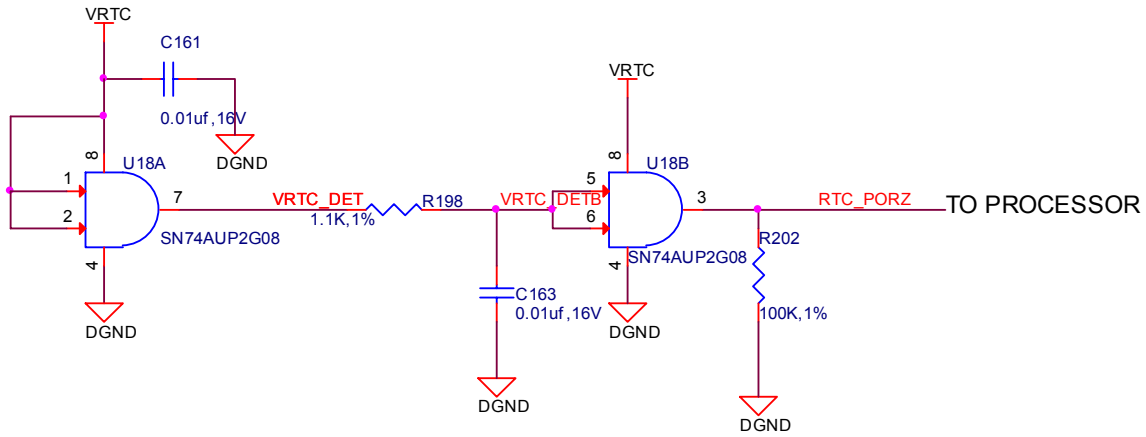

Figure 9. RTC_PORZ Control

Once the VRTC rail comes up the circuit delays the RTZ_PORZ which releases the RTC circuitry in the processor.

Once the RTC block reset is released, the processor starts the initialization process. After the RTC stabilizes, the processor launches the rest of the power up process by activating the PMIC_PWR_EN signal. Because this signal is powered by VRTC, 1.8V, it has to level shifted to match the VIO rail which is 3.3V. This starts the TPS65217 power up process.

A separate circuit holds the processor reset during this process. **Figure 10** shows that circuit.

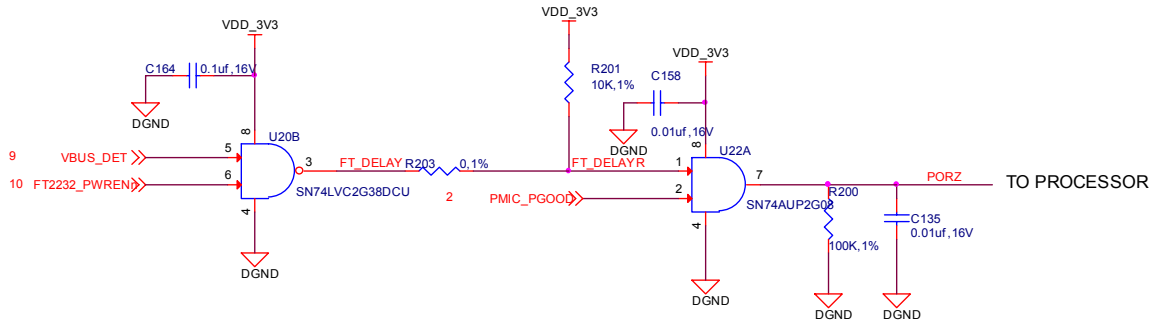

Figure 10. Processor Power On Reset

There are two signals that need to be HI in order for the reset to be released from the processor, PMIC_PGOOD and the FT_DELAY. PMIC_PWRGOOD goes active 200ms after all power rails have reached stability.

The FT_DELAYR signal is a lockout for the serial port supplied by the FT2232 USB to serial device. This allows time for the FT2232 to initialize and connect to the USB port on the host PC without missing any initial boot messages from the processor. If the DC power rail is active, the circuit is active. If not, then the PMIC_PWRGOOD signal controls the PORZ signal. In the event the USB DC is active, the FT2232_PWREN signal is high, which hold the reset on. After the FT2232 has initialized, the signal is released, allowing the reset signal to be taken HI, releasing the processor.

7.3.3 Power Indicator LED

The board has a single power indicator LED. It is controlled via the load switch LS1 on the TPS65217. The default mode of LS1 is on. When the TPS65217 has initialized and all switchers are on, the LS1 is activated turning on the LED. If the switchers are not initialized, for example if the processor does not enable the PWR_EN signal, the LED will not turn on. The power LED indicates that the TPS65217 is powered up.

Under software control, the power LED can be turned off to conserve power in a low powered mode. The SW could also pulse the LED if desired to indicate a low power mode.

7.4 Two port HUB

In order to provide access from a single USB port to the FT2232 and the processor USB port, a USB2412 Dual port USB 2.0 HUB is provided. This device connects to the host PC.

7.4.1 FT2232H Serial Adapter

The first port of the HUB is connected to the processor USB port 0.

7.4.2 Processor USB Port

The second port of the HUB connected to the FT2232 which handles the processor serial port and JTAG and is described in the next section.

7.5 FT2232H USB to Serial Adapter

The FT2232H from FTDI provides the conversion form the USB port to a JTAG and Serial port to the processor.

7.5.1 JTAG

Using a parallel I/O mode, the FT2232H can be used to access the JATG signals on the processor. At USB 2.0 speeds, the throughput is very good, and should provide connectivity to several popular debug environments including CCS.

7.5.2 Serial Port

Access to UART0 is provided by the FT2232H via the USB port. Signals available are TX, RX, RTS, and CTS.

7.6 256MB DDR2 Memory

The board comes standard with 256MB DDR SDRAM configured as a single 128M x 16 device. The design will also support a single 64M x 16 device for 128MB of memory. The design uses a single MT47H128M16RT-25E:C 400MHZ memory from Micron which comes in an 84-Ball 9.0mm x 12.5mm FBGA package. **Table 3** below is the addressing configuration of the device.

Table 3. DDR Addressing

Parameter	128 Meg x 16
Configuration	16 Meg x 16 x 8 banks
Refresh count	8K
Row address	A[13:0] (16K)
Bank address	BA[2:0] (8)
Column address	A[9:0] (1K)

Figure 11 is the functional block diagram of the DDR2 memory device.

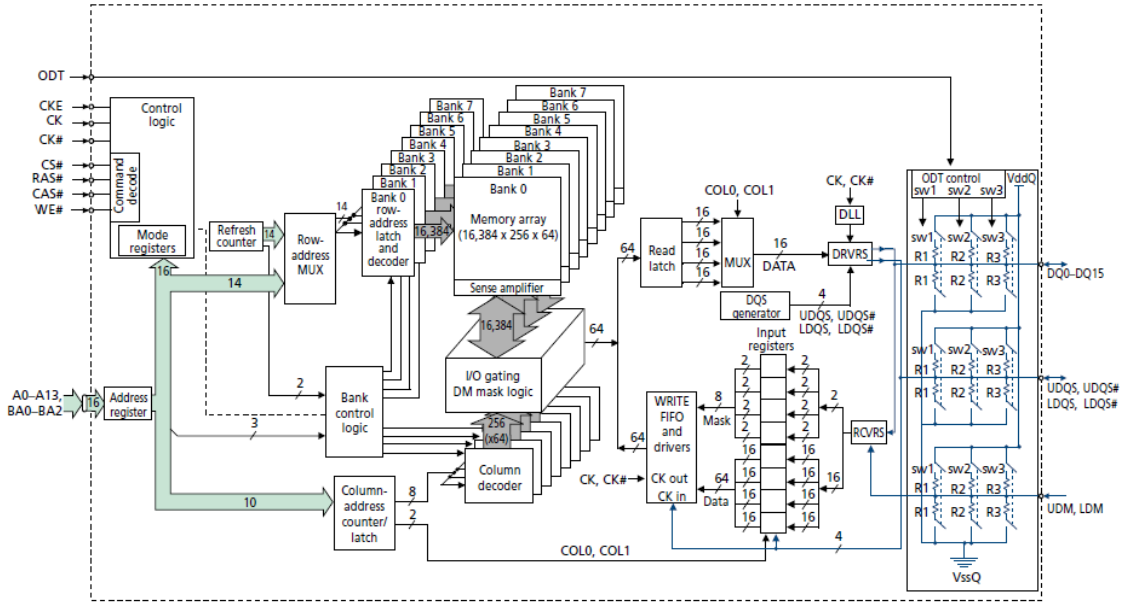

Figure 11. DDR Device Block Diagram

7.6.1 DDR 2 Design

Figure 12 below is the schematic of the DDR implementation. The memory is placed a as close to the processor as possible to minimize layout issues.

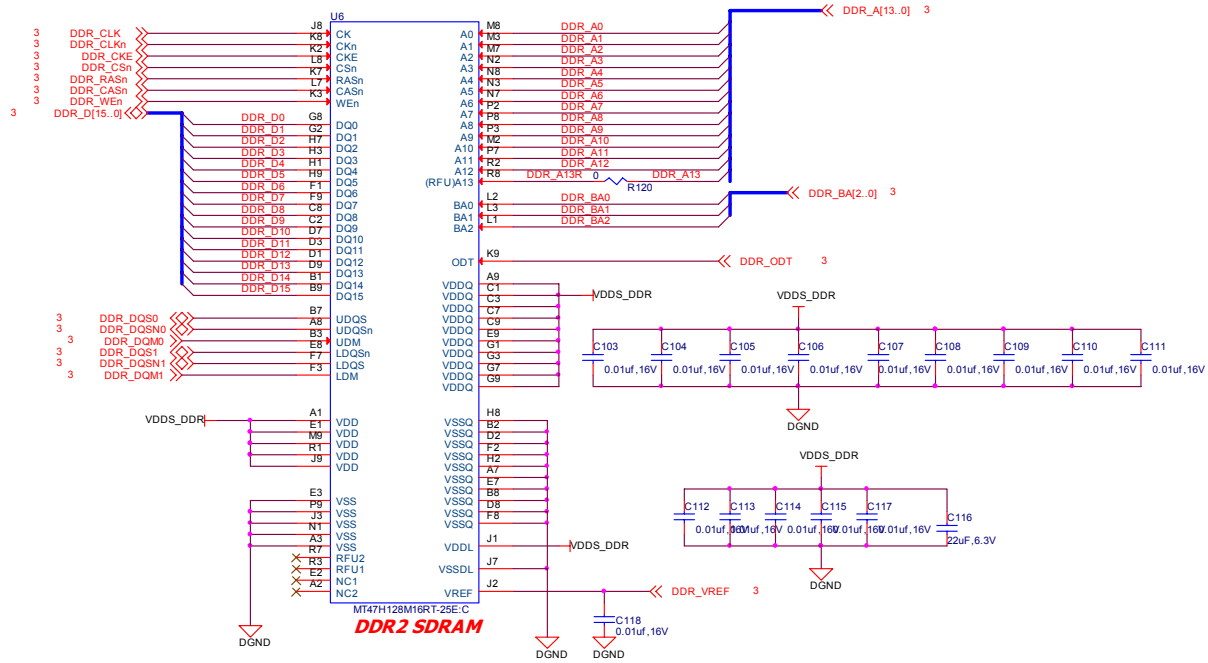

Figure 12. DDR Design

7.6.2 DDR2 Package

Figure 13 below is the dimensions of the DDR package.

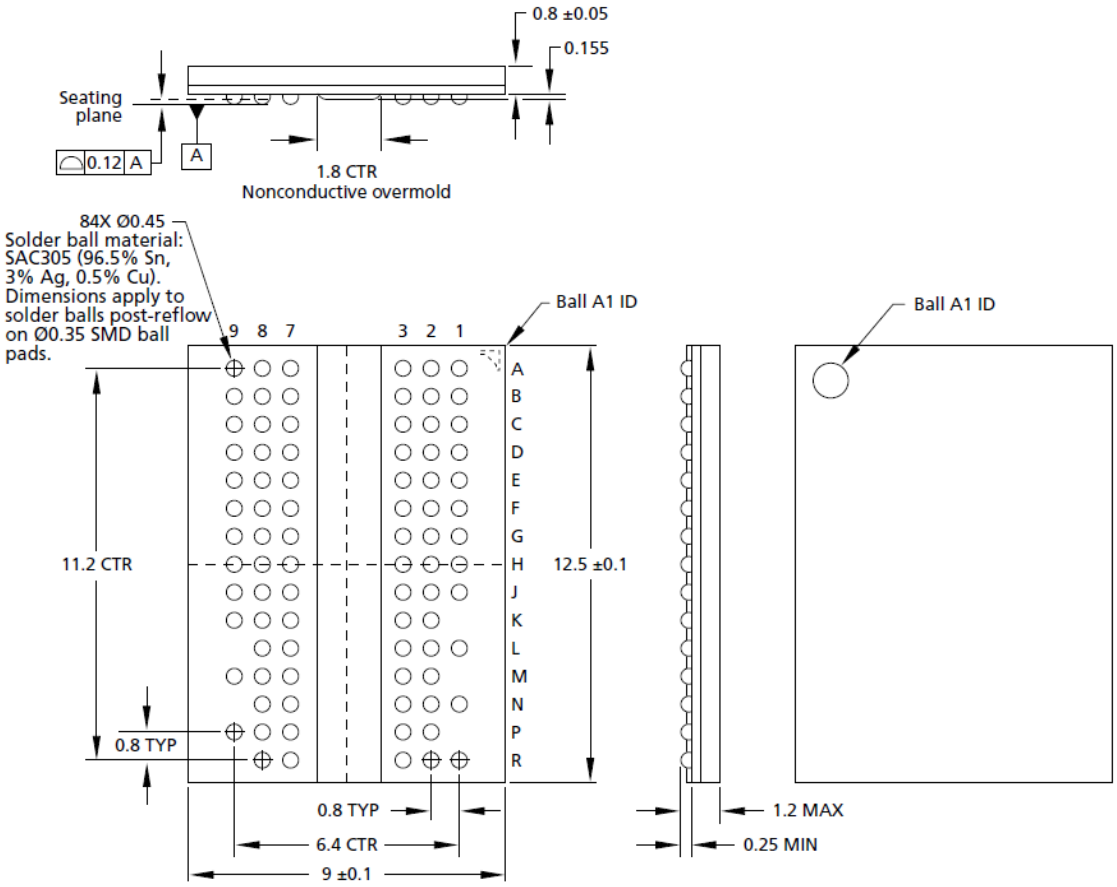

Figure 13. DDR2 84-Ball Package

7.7 User LEDs

Four user LEDS are provided via GPIO pins on the processor. **Figure 14** below shows the LED circuitry.

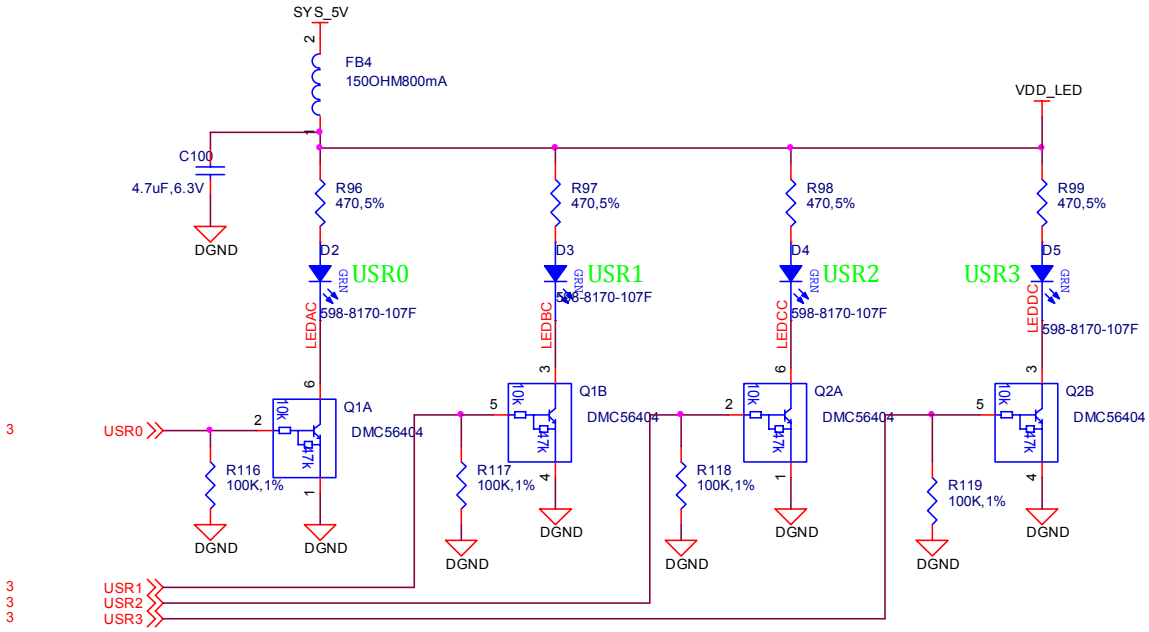

Figure 14. User LEDS

Q1 and Q2 provide level shifting from the processor to drive the LEDs that are connected the SYS_5V rail. FB4 provides noise immunity to the system by the LEDS which can be a source of noise back into the system rail. Each LED is controlled by setting the appropriate GPIO bit HI. At power up all LEDs are off. **Table 4** is the GPIO USER LED assignments.

Table 4. User LED Control

LED	GPIO
User 0	GPIO1_21
User 1	GPIO1_22
User 2	GPIO1_23
User 3	GPIO1_24

7.8 10/100 Ethernet

The 10/100 Ethernet uses a SMSC LAN8720A Ethernet PHY and interfaces to the processor using the RMII interface. Key features of this PHY include:

- Single chip PHY
- Variable I/O rail 1.6 to 3.3V
- HP Auto-MDIX support
- Small 4x4x0,85mm Package

7.8.1 Ethernet PHY Design

Figure 15 below is the design of the 10/100 PHY section of the board.

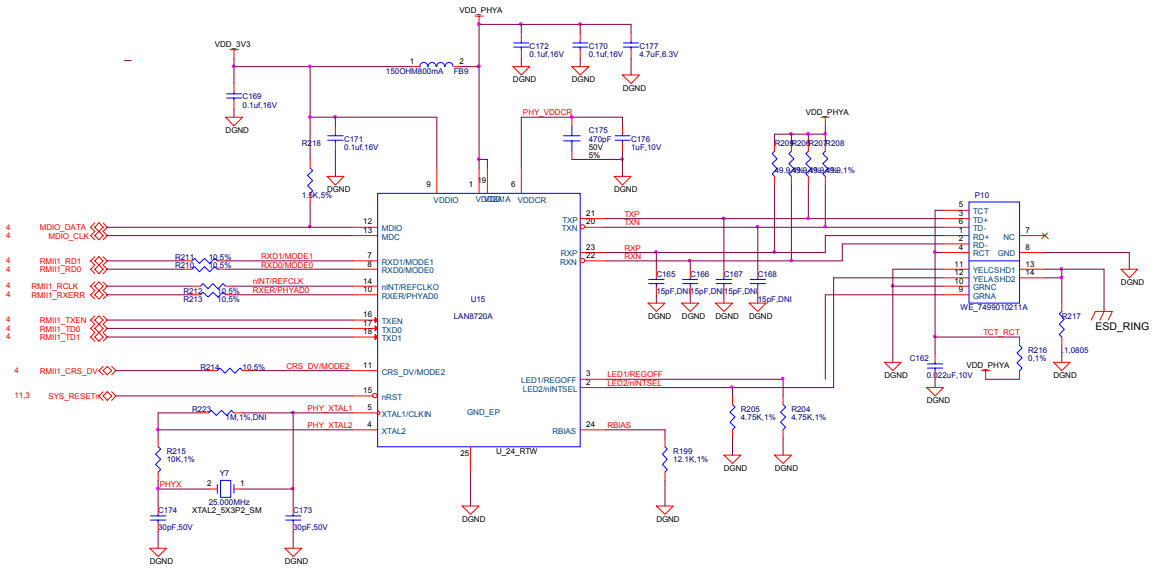

Figure 15. 10/100 Ethernet PHY Design

7.9 USB Host

A single USB Host port is provided on the board. It is driven by UAB port 1 of the processor. The port can deliver up to 500mA of current provided that much current is available from the power supply. In the scenario where the board is totally powered from the USB input, the power supplied will be much less and dependent on how much current is available after driving the board and any daughter cards that may be attached.

7.9.1 USB Host design

Figure 16 below is the USB Host design.

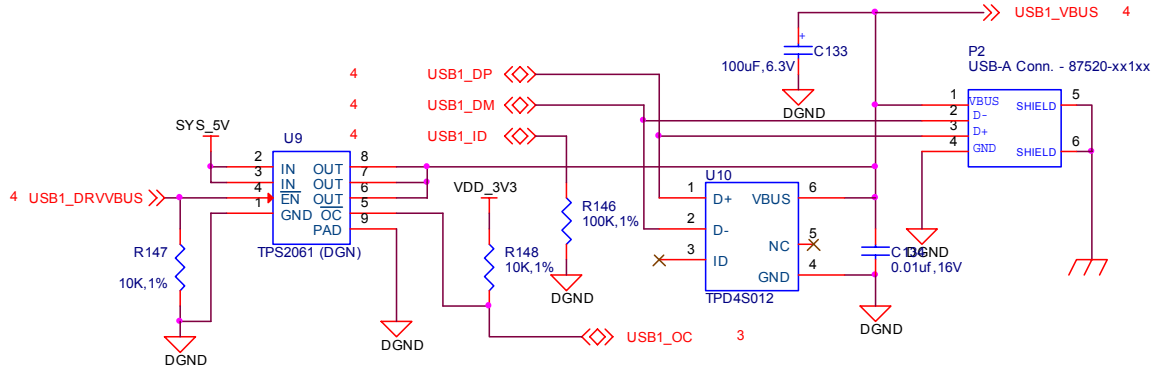

Figure 16. USB Host Design

The USB port on the processor is an OTG port. In order to force the host function needed, the ID pin is grounded.

U9 is the power switch that controls the 5VDC to the USB port. In the event of an over current condition, the switch will signal the processor of the event and the switch will shut down. **C133** provides extra current when devices are inserted into the connector. **U10** is an ESD protection device

7.10 SD Connector

The board is populated with a microSD small form factor SD slot. It will support High capacity cards. The voltage rail is 3.3V. A card detector output is provided from the connector to the CD/EMU4 signal. Figure 17 shows the connections to the microSD connector.

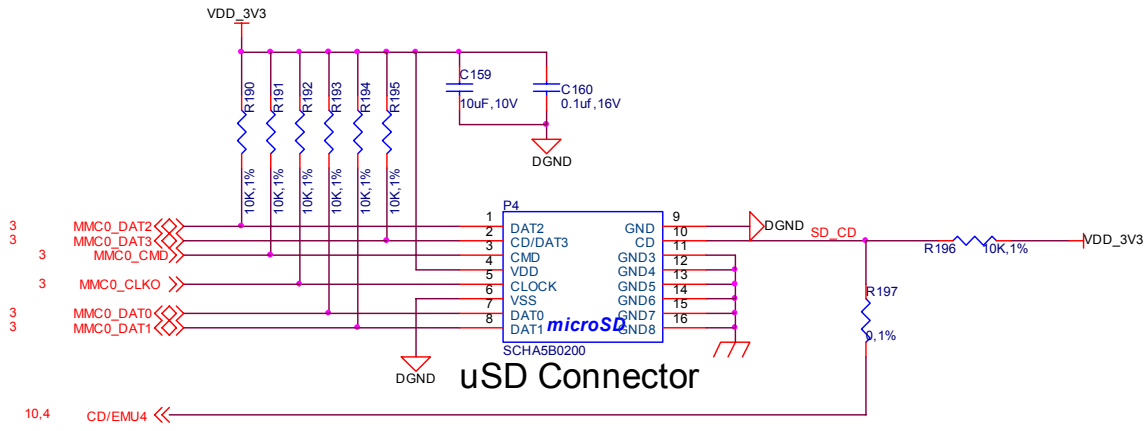

Figure 17. SD Connector Design

7.11 Expansion Headers

The expansion interface on the board is comprised of two 46 pin connectors. All signals on the expansion headers are 3.3V unless otherwise indicated.
NOTE: Do not connect 5V logic level signals to these pins or the board will be damaged.

7.11.1 Expansion Header A

Table 5 shows the default pinout of the A expansion header. Other signals can be connected to this connector based on setting the pin mux on the processor, but this is the default settings on power up.

Table 5. Expansion Header A Pinout

SIGNAL NAME	PIN	CONN		PIN	SIGNAL NAME
	GND	1	2	GND	
	VDD_5V	3	4	VDD_5V	
	SYS_VOLT	5	6	SYS_VOLT	
UART2_RXD	A17	7	8	C12	SPI1_CS0
SPI1_SCLK	A13	9	10	D12	SPI1_D1
SPI1_D0	B13	11	12	D13	EHRPWM0B
GPIO3_21	A14	13	14	V6	GPIO1_29
GPIO3_19	C13	15	16	U8	GPIO1_4
GPIO1_30	U9	17	18	R8	GPIO1_2
GPIO1_3	T8	19	20	U7	GPIO1_0
GPIO1_1	V7	21	22	V3	UART4_RTSN
GPIO2_1	V16	23	24	U4	UART3_RTSN
SPI1_CS1	C18	25	26	U2	UART5_RXD
UART4_CTSN	V2	27	28	T4	GPIO2_13
UART3_CTSN	U3	29	30	T2	GPIO2_11
UART5_TXD	U1	31	32	R4	GPIO2_9
GPIO_12	T3	33	34	R2	GPIO2_7
GPIO2_10	T1	35	36	R1	GPIO2_6
GPIO2_8	R3	37	38	AGND	
	VADC	39	40	B6	AIN0
AIN1	C7	41	42	B7	AIN2
AIN3	A7	43	44	C8	AIN4
AIN5	A5	45	46	A5	AIN6

NOTE: THE PINOUT IS SUBJECT TO CHANGE BASED ON THE FINAL LAYOUT ROUTING OF THE BOARD.

7.11.1.1 Connector A Signal Definitions

TBA

7.11.1.2 Connector A Signal Pin Mux Options

TBA

7.12 Expansion Header B

Table 6 shows the default pinout of the B expansion header. Other signals can be connected to this connector based on setting the pin mux on the processor, but this is the default settings on power up.

Table 6. Expansion Header B Pinout

SIGNAL NAME	PIN	CONN		PIN	SIGNAL NAME
	GND	1	2	GND	
	DC_3.3V	3	4	DC_3.3V	
SYS_RESETn	A10	5	6	D15	UART1_TXD
UART1_RXD	D16	7	8	B17	UART2_TXD
EHRPWM1A	U14	9	10	T14	EHRPWM1B
TIMER7	T7	11	12	T6	TIMER5
TIMER6	U6	13	14	R7	TIMER4
GPIO1_5	V8	15	16	R9	GPIO1_6
GPIO1_7	T9	17	18	U17	UART4_TXD
UART4_RXD	T17	19	20	V9	GPIO1_31
GPIO1_28		21	22	D14	CLKOUT2
GPIO2_22	U5	23	24	W5	GPIO2_24
GPIO2_25	R6	25	26	R5	GPIO2_23
EHRPWM2B	T10	27	28	U10	EHRPWM2A
GPIO0_27	U12	29	30	T11	GPIO0_26
GPIO1_13	R12	31	32	T12	GPIO1_12
GPIO1_15	U13	33	34	V13	GPIO1_14
UART5_CTSN	V4	35	36	T5	UART5_RTSN
I2C2_SCL	D17	37	38	D18	I2C2_SDA
PWR_BUT		39	40	B16	I2C1_SDA
I2C1_SCL	A16	41	42		BOARDID
	BOARDID	43	44		BOARDID
	GND	45	46	GND	

NOTE: THE PINOUT I S SUBJECT TO CHANGE BASED ON THE FINAL LAYOUT ROUTING OF THE BOARD.

7.12.1.1 Connector B Signal Definitions

TBA

7.12.1.2 Connector B Signal Pin Mux Options

TBA

7.13 PMIC Expansion Header

8.0 Expansion Board Support

The BeagleBone has the ability to accept up to three daughter boards stacked onto the expansion headers. This section describes the rule for doing this to insure proper operation with the board and proper interoperability with other daughter boards that are intended to co-exist on the board.

8.1 EEPROM

Each daughter board will have its own EEPROM containing information that will allow the SW to identify the board and to configure the expansion headers pins as needed.

8.1.1 I2C Bus

The BeagleBone and all daughter cards are equipped with a EEPROM that provides board information.

All of these are connected to I2C1. The EVM uses I2C0 to read the daughter board IDS. As we have no control over the daughter boards in the Beagle community, there was a feeling that it would be risky to extend I2C0 out the expansion connecter fearing that something could be tied to that bus that would interfere with the communication between the processor and the PMIC which uses I2C0.

8.1.2 EEPROM Address/Board ID

In order for each board to have a unique address, a board ID scheme is used that sets the address to be different depending on the order in which it is stacked onto the main board. Each daughter board has a top and bottom connector. The bottom pin is shifted one position to the right, each time removing a ground from one of the three address lines on the daughter board. This will result in a unique address of reach daughter board. **Figure 18** is representation of the concept.

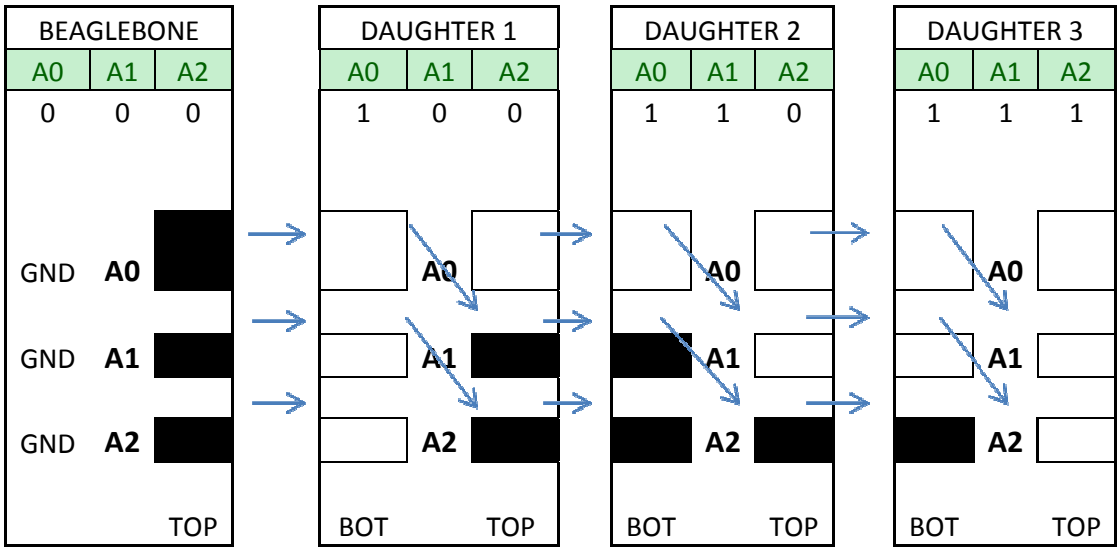

Figure 18. Board ID Address

8.1.3 EEPROM Address/Board ID

8.1.4 EEPROM Data Format

8.2 Connectors

A bottom side and top side connector is required on each daughter board to allow stacking of other boards. The bottom connector is a male header and the top side connector is a female header. All headers are Surface Mount connectors. The following sections describe how the connectors are to be implemented and used.

8.2.1 Bottom Side

The bottom side connector is a dual row 46 position male header. **Figure 19** is a picture of the connector.

Figure 19. Bottom Side Connector

It may be possible to buy a larger number of positions and cut the connector down. One example is a 100 position connector from Sullins (GRPB502VWQS-RC) which is a 100 pin header. This one connector when cut, will handle both edges of the board.

8.2.2 Top Side

8.2.3 Signal Pass Thru

8.2.4 Signal Stealing

8.3 Power Usage

8.4 Mechanical

8.4.1 Board Size

8.4.2 Mounting

8.4.3 Stacking

9.0 Mechanical Specification

Size: 3.5” x 2.1” (86.36mm x 53.34mm)
Max height: .187” (4.76mm)
PCB Layers: 6
PCB thickness: .062”
RoHS Compliant: Yes
Weight: TBW

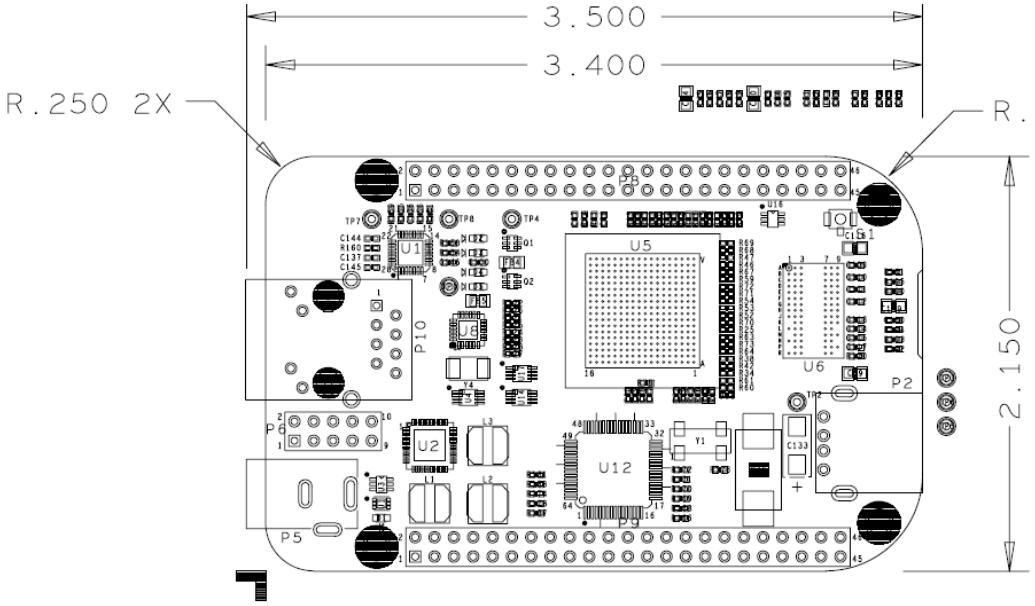

Figure 20. Preliminary Board Profile Top

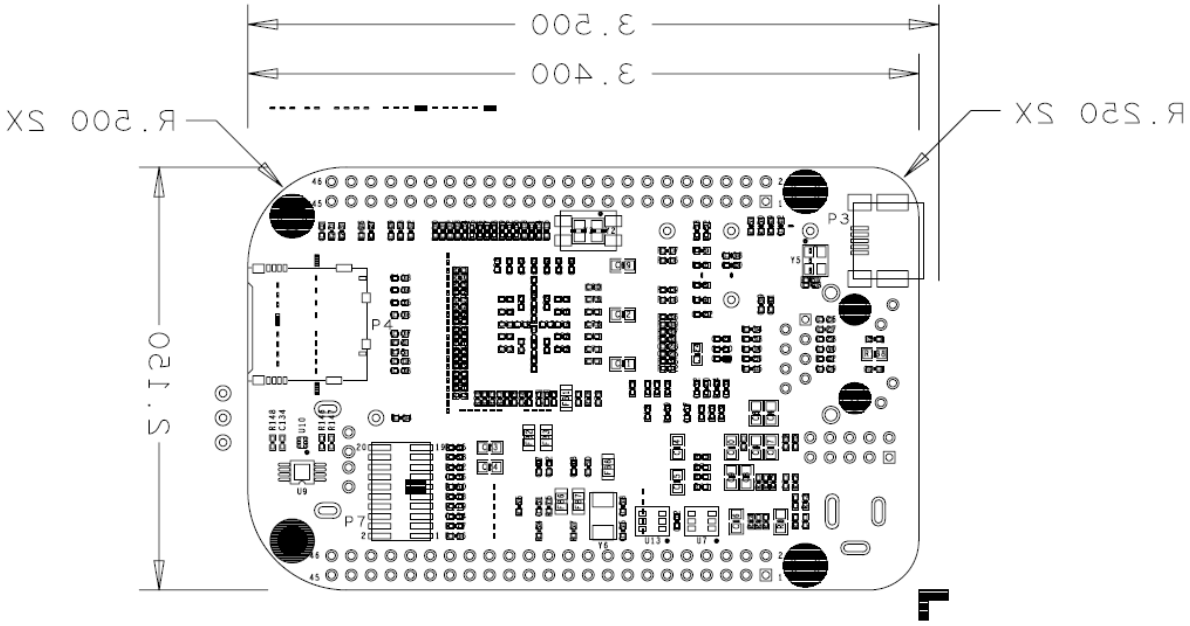

Figure 21. Preliminary Board Profile Bottom