REV	Description	DATE	BY
A	Initial relase.	9/10/11	GC
A1	1. [P2] Added jumper to connect PWR_EN pullup to VDD_VRTC as VDD_IO does not come up before PWR_EN. 2. [P2] Added jumper to connect I2C pullups to VDD_IO. 3. [P3] Made R189 DNI as USB cable insertion would cause Processor reset. 4. [P10] Made R163 as DNI as FT2232 was keeping Processor in reset. 5. [P8] Made C133 DNI due to current surge when activating USB1 power rail. 6. [P9] Made R152 4.75K. 7. [P8] Changed U9 to TPS2051 with active HI enable. 8. [P8] Changed R146 to 0 ohm.. 9. [P8] Changed R136 to DNI. 10. [P8] Changed R199 to DNI. 11. [P8] Changed R144 to DNI. 12. [P8] Change R143 to DNI. 12. [P8] Change R200 to installed.	10/1/11	GC

TEXAS INSTRUMENTS

PRELIMINARY documents contain information on a product under development and is issued for evaluation purposes only. Features characteristic data and other information are subject to change.

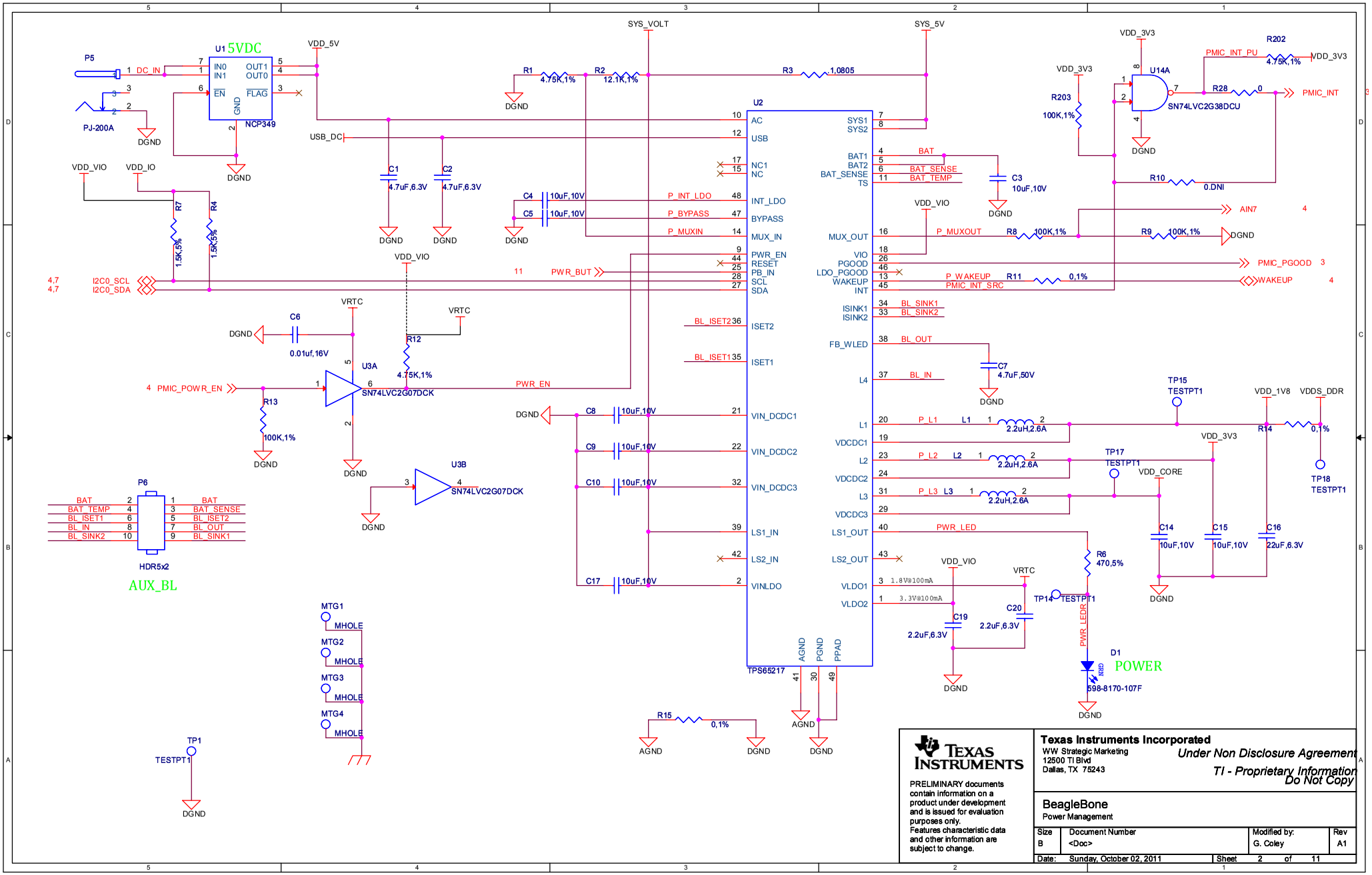
Texas Instruments Incorporated
WW Strategic Marketing
12500 TI Blvd
Dallas, TX 75243

Under Non Disclosure Agreement
TI - Proprietary Information
Do Not Copy

BeagleBone
Cover Page

Size	Document Number	Modified by:	Rev
B	<Doc>	G. Coley	A1

Date: Monday, October 03, 2011 | Sheet 1 of 11



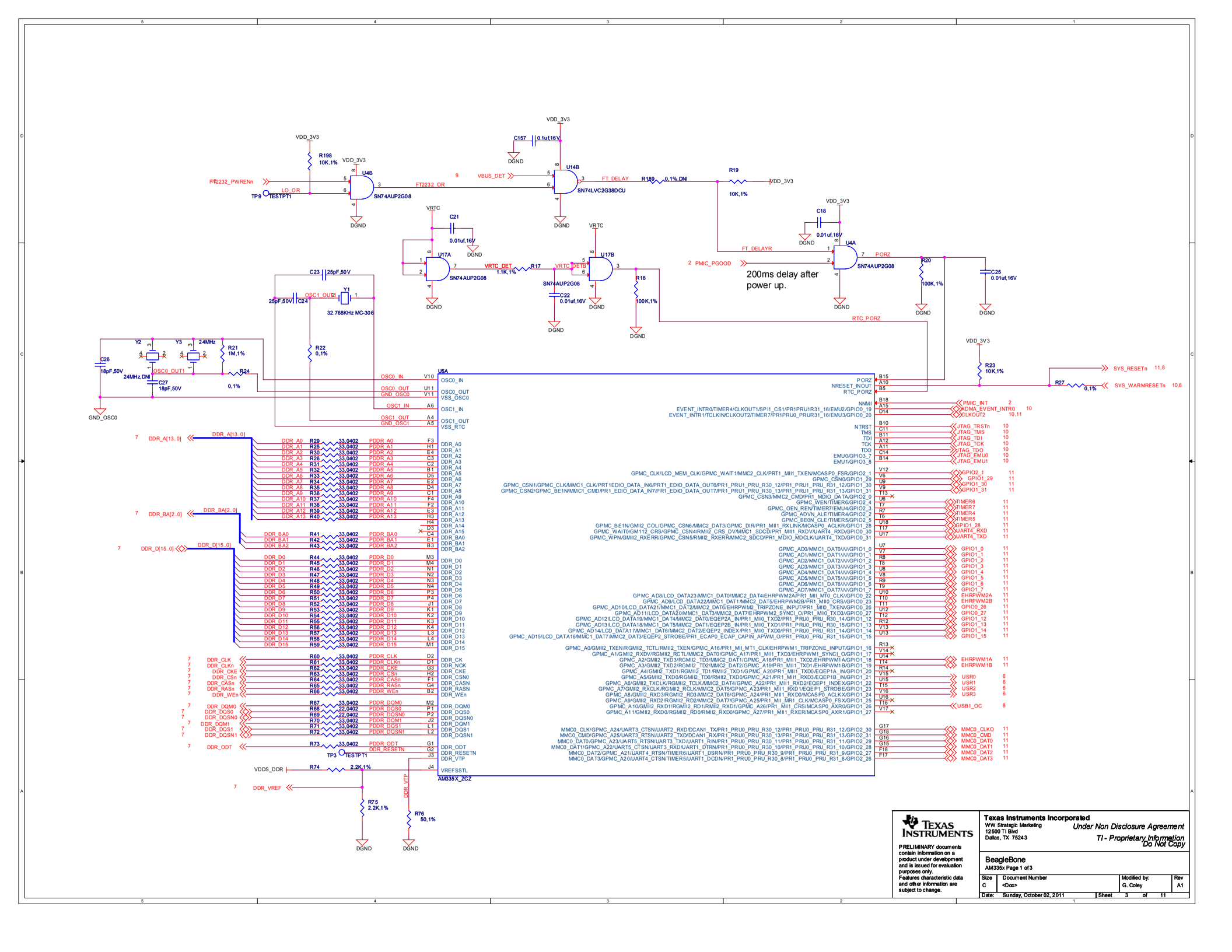
PRELIMINARY documents contain information on a product under development and is issued for evaluation purposes only. Features characteristic data and other information are subject to change.

Texas Instruments Incorporated
WW Strategic Marketing
12500 TI Blvd
Dallas, TX 75243

Under Non Disclosure Agreement
TI - Proprietary Information
Do Not Copy

BeagleBone
Power Management

Size	Document Number	Modified by:	Rev
B	<Doc>	G. Coley	A1
Date:	Sunday, October 02, 2011	Sheet 2 of 11	


VDD_3V3
R198
10K,1%
U4B
SN74AUP2G08
FT2232_PWRENn
LO_OR
TP9
TESTPT1
FT2232_OR
DGND
C157
0.1uf,16V
U14B
SN74LVC2G38DCU
VBUS_DET
FT_DELAY
R189
0.1%,DNI
R19
10K,1%
VRTC
C21
0.01uf,16V
U17A
SN74AUP2G08
VRTC_DET
1.1K,1%
R17
U17B
C22
0.01uf,16V
R18
100K,1%
C18
U4A
FT_DELAYR
PMIC_PGOOD
200ms delay after
power up.
PORZ
R20
100K,1%
C25
0.01uf,16V
RTC_PORZ
C23
25pF,50V
C24
OSC1_OUT2
Y1
32.768KHz MC-306
Y2
Y3
24MHz
R21
1M,1%
C26
18pF,50V
24MHz,DNI
C27
18pF,50V
OSC0_OUT1
R24
0,1%
R22
0,1%
GND_OSC0
U5A
OSC0_IN
OSC0_OUT
GND_OSC0
VSS_OSC0
OSC1_IN
OSC1_OUT
GND_OSC1
VSS_RTC
PORZ
NRESET_IN
OUT
RTC_PORZ
R23
10K,1%
R27
0,1%
SYS_RESETn
SYS_WARMRESETn
NMI
EVENT_INTR0/TIMER4/CLKOUT1/SPI1_CS1/PR1PRU1R31_16/EMU2/GPIO0_19
EVENT_INTR1/TCLKIN/CLKOUT2/TIMER7/PR1PRU0_PRUR31_16/EMU3/GPIO0_20
NTRST
TMS
TDI
TCK
TDO
EMU0/GPIO3_7
EMU1/GPIO3_8
JTAG_TRSTn
JTAG_TMS
JTAG_TDI
JTAG_TCK
JTAG_TDO
JTAG_EMU0
JTAG_EMU1
PMIC_INT
XDMA_EVENT_INTR0
CLKOUT2
GPMC_CLK/LCD_MEM_CLK/GPMC_WAIT1/MMC2_CLK/PRT1_MII1_TXEN/MCASP0_FSR/GPIO2_1
GPMC_CSN0/GPIO1_29
GPMC_CSN1/GPMC_CLK/MMC1_CLK/PRT1EDIO_DATA_IN6/PRT1_EDIO_DATA_OUT6/PR1_PRU1_PRU_R30_12/PR1_PRU1_PRU_R31_12/GPIO1_30
GPMC_CSN2/GPMC_BE1N/MMC1_CMD/PR1_EDIO_DATA_IN7/PR1_EDIO_DATA_OUT7/PR1_PRU1_PRU_R30_13/PR1_PRU1_PRU_R31_13/GPIO1_31
GPMC_CSN3/MMC2_CMD/PR1_MDIO_DATA/GPIO2_0
GPMC_WEN/TIMER6/GPIO2_4
GPMC_OEN_REN/TIMER7/EMU4/GPIO2_3
GPMC_ADVN_ALE/TIMER4/GPIO2_2
GPMC_BE0N_CLE/TIMER5/GPIO2_5
GPMC_BE1N/GMII2_COL/GPMC_CSN6/MMC2_DAT3/GPMC_DIR/PR1_MII1_RXLINK/MCASP0_ACLKR/GPIO1_28
GPMC_WAIT0/GMII2_CRS/GPMC_CSN4/RMII2_CRS_DV/MMC1_SDCD/PR1_MII1_RXDV/UART4_RXD/GPIO0_30
GPMC_WPN/GMII2_RXERR/GPMC_CSN5/RMII2_RXERR/MMC2_SDCD/PR1_MDIO_MDCLK/UART4_TXD/GPIO0_31
GPMC_AD0/MMC1_DAT0/////GPIO1_0
GPMC_AD1/MMC1_DAT1/////GPIO1_1
GPMC_AD2/MMC1_DAT2/////GPIO1_2
GPMC_AD3/MMC1_DAT3/////GPIO1_3
GPMC_AD4/MMC1_DAT4/////GPIO1_4
GPMC_AD5/MMC1_DAT5/////GPIO1_5
GPMC_AD6/MMC1_DAT6/////GPIO1_6
GPMC_AD7/MMC1_DAT7/////GPIO1_7
GPMC_AD8/LCD_DATA23/MMC1_DAT0/MMC2_DAT4/EHRPWM2APR1_MII_MT0_CLK/GPIO0_22
GPMC_AD9/LCD_DATA22/MMC1_DAT1/MMC2_DAT5/EHRPWM2B/PR1_MII0_CRS//GPIO0_23
GPMC_AD10/LCD_DATA21/MMC1_DAT2/MMC2_DAT6/EHRPWM2_TRIPZONE_INPUT/PR1_MII0_TXEN//GPIO0_26
GPMC_AD11/LCD_DATA20/MMC1_DAT3/MMC2_DAT7/EHRPWM2_SYNCI_O/PR1_MII0_TXD3/GPIO0_27
GPMC_AD12/LCD_DATA19/MMC1_DAT4/MMC2_DAT0/EQEP2A_IN/PR1_MII0_TXD2/PR1_PRU0_PRU_R30_14/GPIO1_12
GPMC_AD13/LCD_DATA18/MMC1_DAT5/MMC2_DAT1/EQEP2B_IN/PR1_MII0_TXD1/PR1_PRU0_PRU_R30_15/GPIO1_13
GPMC_AD14/LCD_DATA17/MMC1_DAT6/MMC2_DAT2/EQEP2_INDEX/PR1_MII0_TXD0/PR1_PRU0_PRU_R31_14/GPIO1_14
GPMC_AD15/LCD_DATA16/MMC1_DAT7/MMC2_DAT3/EQEP2_STROBE/PR1_ECAP0_ECAP_CAPIN_APWM_O/PR1_PRU0_PRU_R31_15/GPIO1_15
GPMC_A0/GMII2_TXEN/RGMII2_TCTL/RMII2_TXEN/GPMC_A16/PR1_MII_MT1_CLK/EHRPWM1_TRIPZONE_INPUT/GPIO1_16
GPMC_A1/GMII2_RXDV/RGMII2_RCTL/MMC2_DAT0/GPMC_A17/PR1_MII1_TXD3/EHRPWM1_SYNCI_O/GPIO1_17
GPMC_A2/GMII2_TXD3/RGMII2_TD3/MMC2_DAT1/GPMC_A18/PR1_MII1_TXD2/EHRPWM1A/GPIO1_18
GPMC_A3/GMII2_TXD2/RGMII2_TD2/MMC2_DAT2/GPMC_A19/PR1_MII1_TXD1/EHRPWM1B/GPIO1_19
GPMC_A4/GMII2_TXD1/RGMII2_TD1/RMII2_TXD1/GPMC_A20/PR1_MII1_TXD0/EQEP1A_IN/GPIO1_20
GPMC_A5/GMII2_TXD0/RGMII2_TD0/RMII2_TXD0/GPMC_A21/PR1_MII1_RXD3/EQEP1B_IN/GPIO1_21
GPMC_A6/GMII2_TXCLK/RGMII2_TCLK/MMC2_DAT4/GPMC_A22/PR1_MII1_RXD2/EQEP1_INDEX/GPIO1_22
GPMC_A7/GMII2_RXCLK/RGMII2_RCLK/MMC2_DAT5/GPMC_A23/PR1_MII1_RXD1/EQEP1_STROBE/GPIO1_23
GPMC_A8/GMII2_RXD3/RGMII2_RD3/MMC2_DAT6/GPMC_A24/PR1_MII1_RXD0/MCASP0_ACLKX/GPIO1_24
GPMC_A9/GMII2_RXD2/RGMII2_RD2/MMC2_DAT7/GPMC_A25/PR1_MII_MR1_CLK/MCASP0_FSX/GPIO1_25
GPMC_A10/GMII2_RXD1/RGMII2_RD1/RMII2_RXD1/GPMC_A26/PR1_MII1_CRS/MCASP0_AXR0/GPIO1_26
GPMC_A11/GMII2_RXD0/RGMII2_RD0/RMII2_RXD0/GPMC_A27/PR1_MII1_RXER/MCASP0_AXR1/GPIO1_27
USR0
USR1
USR2
USR3
USB1_OC
MMC0_CLK/GPMC_A24/UART3_CTSN/UART2_RXD/DCAN1_TX/PR1_PRU0_PRU_R30_12/PR1_PRU0_PRU_R31_12/GPIO2_30
MMC0_CMD/GPMC_A25/UART3_RTSN/UART2_TXD/DCAN1_RX/PR1_PRU0_PRU_R30_13/PR1_PRU0_PRU_R31_13/GPIO2_31
MMC0_DAT0/GPMC_A23/UART5_RTSN/UART3_TXD/UART1_RIN/PR1_PRU0_PRU_R30_11/PR1_PRU0_PRU_R31_11/GPIO2_29
MMC0_DAT1/GPMC_A22/UART5_CTSN/UART3_RXD/UART1_DTRN/PR1_PRU0_PRU_R30_10/PR1_PRU0_PRU_R31_10/GPIO2_28
MMC0_DAT2/GPMC_A21/UART4_RTSN/TIMER6/UART1_DSRN/PR1_PRU0_PRU_R30_9/PR1_PRU0_PRU_R31_9/GPIO2_27
MMC0_DAT3/GPMC_A20/UART4_CTSN/TIMER5/UART1_DCDN/PR1_PRU0_PRU_R30_8/PR1_PRU0_PRU_R31_8/GPIO2_26
MMC0_CLKO
MMC0_CMD
MMC0_DAT0
MMC0_DAT1
MMC0_DAT2
MMC0_DAT3
AM335X_ZCZ
DDR_A[13..0]
DDR_BA[2..0]
DDR_D[15..0]
DDR_CLK
DDR_CLKn
DDR_CKE
DDR_CSn
DDR_CASn
DDR_RASn
DDR_WEn
DDR_DQM0
DDR_DQS0
DDR_DQSN0
DDR_DQM1
DDR_DQS1
DDR_DQSN1
DDR_ODT
DDR_RESETN
DDR_VTP
TP3
TESTPT1
VDDS_DDR
R74
2.2K,1%
DDR_VREF
R75
2.2K,1%
R76
50,1%
DDR_VTP
PRELIMINARY documents contain information on a product under development and is issued for evaluation purposes only. Features characteristic data and other information are subject to change.
Texas Instruments Incorporated
WW Strategic Marketing
12500 TI Blvd
Dallas, TX 75243
Under Non Disclosure Agreement
TI - Proprietary Information
Do Not Copy
BeagleBone
AM335x Page 1 of 3
Size C
Document Number <Doc>
Modified by: G. Coley
Rev A1
Date: Sunday, October 02, 2011
Sheet 3 of 11

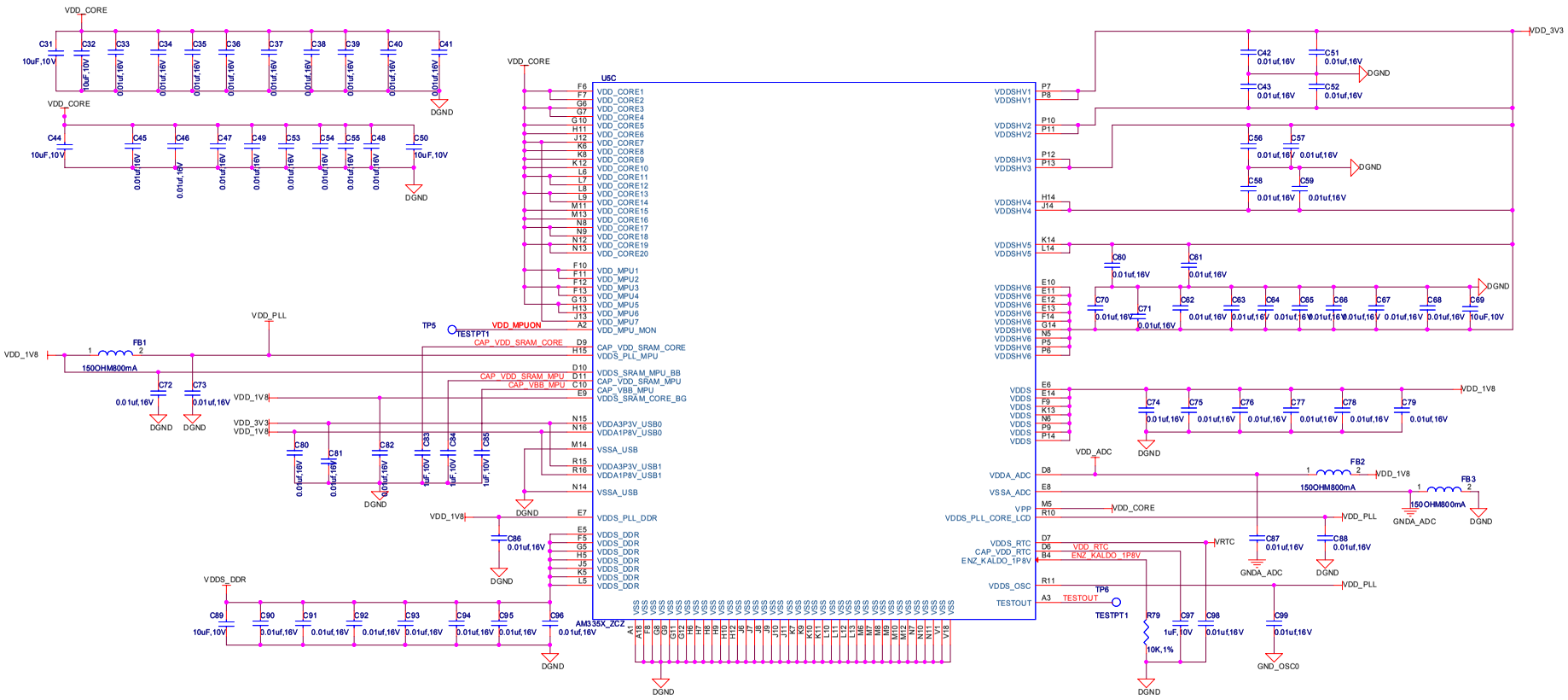
PRELIMINARY documents contain information on a product under development and is issued for evaluation purposes only. Features characteristic data and other information are subject to change.

Texas Instruments Incorporated
WW Strategic Marketing
12500 TI Blvd
Dallas, TX 75243

Under Non Disclosure Agreement
TI - Proprietary Information
Do Not Copy

BeagleBone
AM335x Page 2 of 3

Size	Document Number	Modified by:	Rev
C	<Doc>	G. Coley	A1
Date:	Sunday, October 02, 2011	Sheet 4 of 11	



TEXAS INSTRUMENTS

PRELIMINARY documents contain information on a product under development and is issued for evaluation purposes only. Features characteristic data and other information are subject to change.

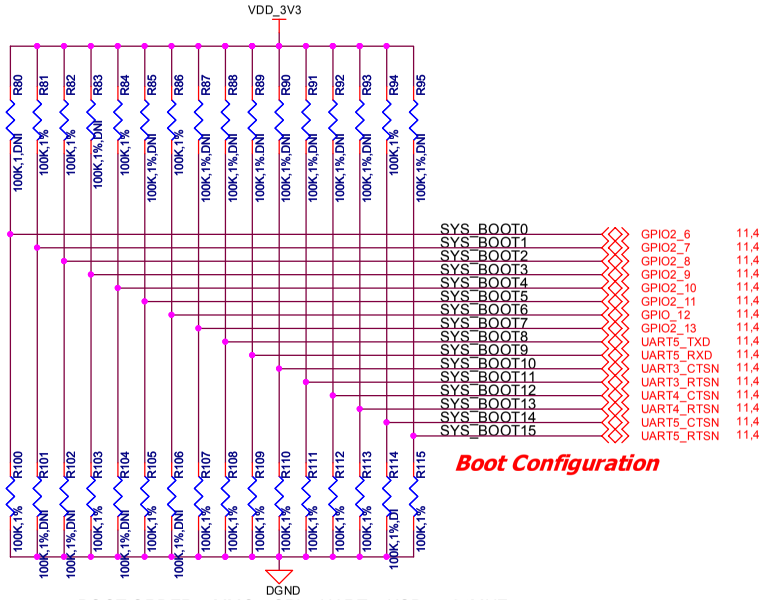
Texas Instruments Incorporated
WW Strategic Marketing
12500 TI Blvd
Dallas, TX 75243

Under Non Disclosure Agreement
TI - Proprietary Information
Do Not Copy

BeagleBone
AM335x Page 3 of 3

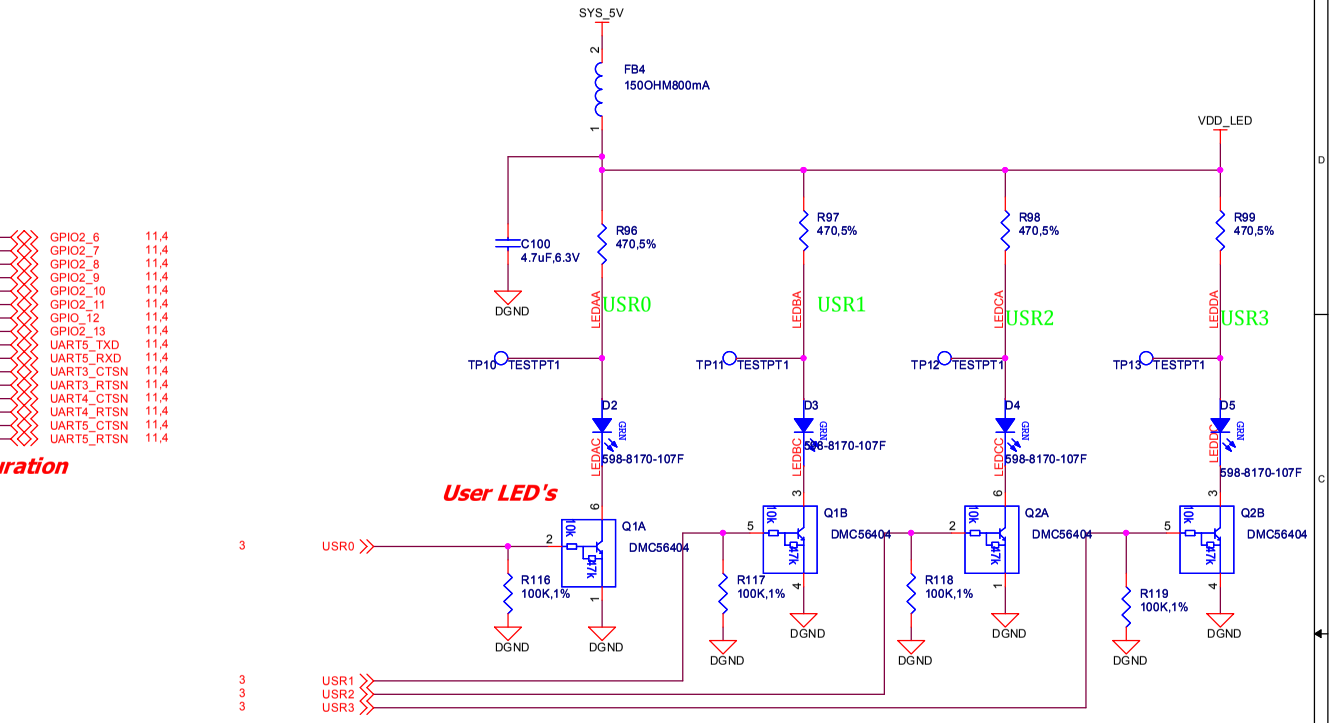
Size	Document Number	Modified by:	Rev
C	<Doc>	G. Coley	A1

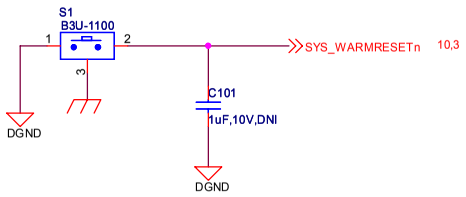
Date: Sunday, October 02, 2011 | Sheet 5 of 11



BOOT ORDER....MMC....SPI....UART....USB.....24MHZ

SYS_BOOT00=1
SYS_BOOT01=1
SYS_BOOT02= 1
SYS_BOOT03=0
SYS_BOOT04=1
SYS_BOOT05=0
SYS_BOOT06=0
SYS_BOOT07=0
SYS_BOOT08=0
SYS_BOOT09=0
SYS_BOOT10=0
SYS_BOOT11=0
SYS_BOOT12=0
SYS_BOOT13=0
SYS_BOOT14=1
SYS_BOOT15=0





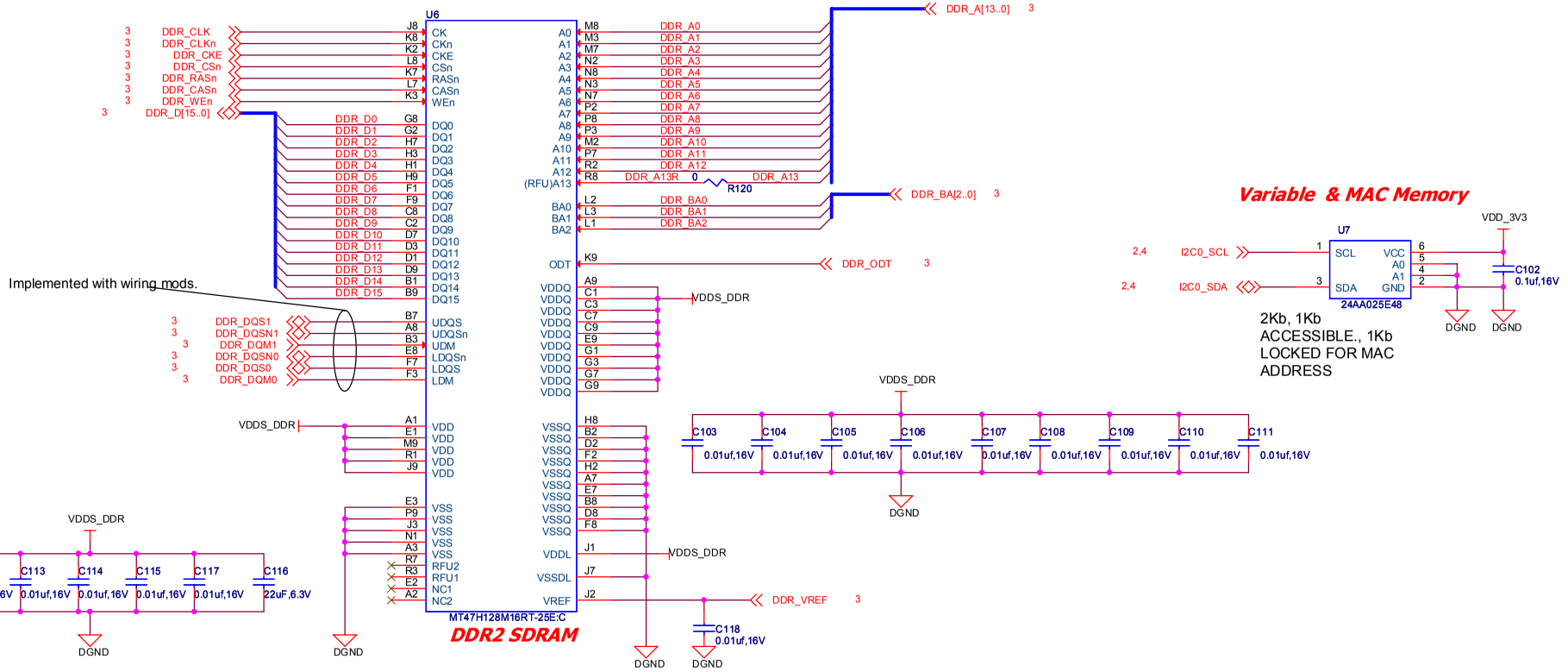
PRELIMINARY documents contain information on a product under development and is issued for evaluation purposes only. Features characteristic data and other information are subject to change.

Texas Instruments Incorporated
WW Strategic Marketing
12500 TI Blvd
Dallas, TX 75243

Under Non Disclosure Agreement
TI - Proprietary Information
Do Not Copy

BeagleBone
LEDs, Configuration, and Button

Size	Document Number	Modified by:	Rev
B	<Doc>	G. Coley	A1
Date:	Monday, October 03, 2011	Sheet 6 of 11	



PRELIMINARY documents contain information on a product under development and is issued for evaluation purposes only. Features characteristic data and other information are subject to change.

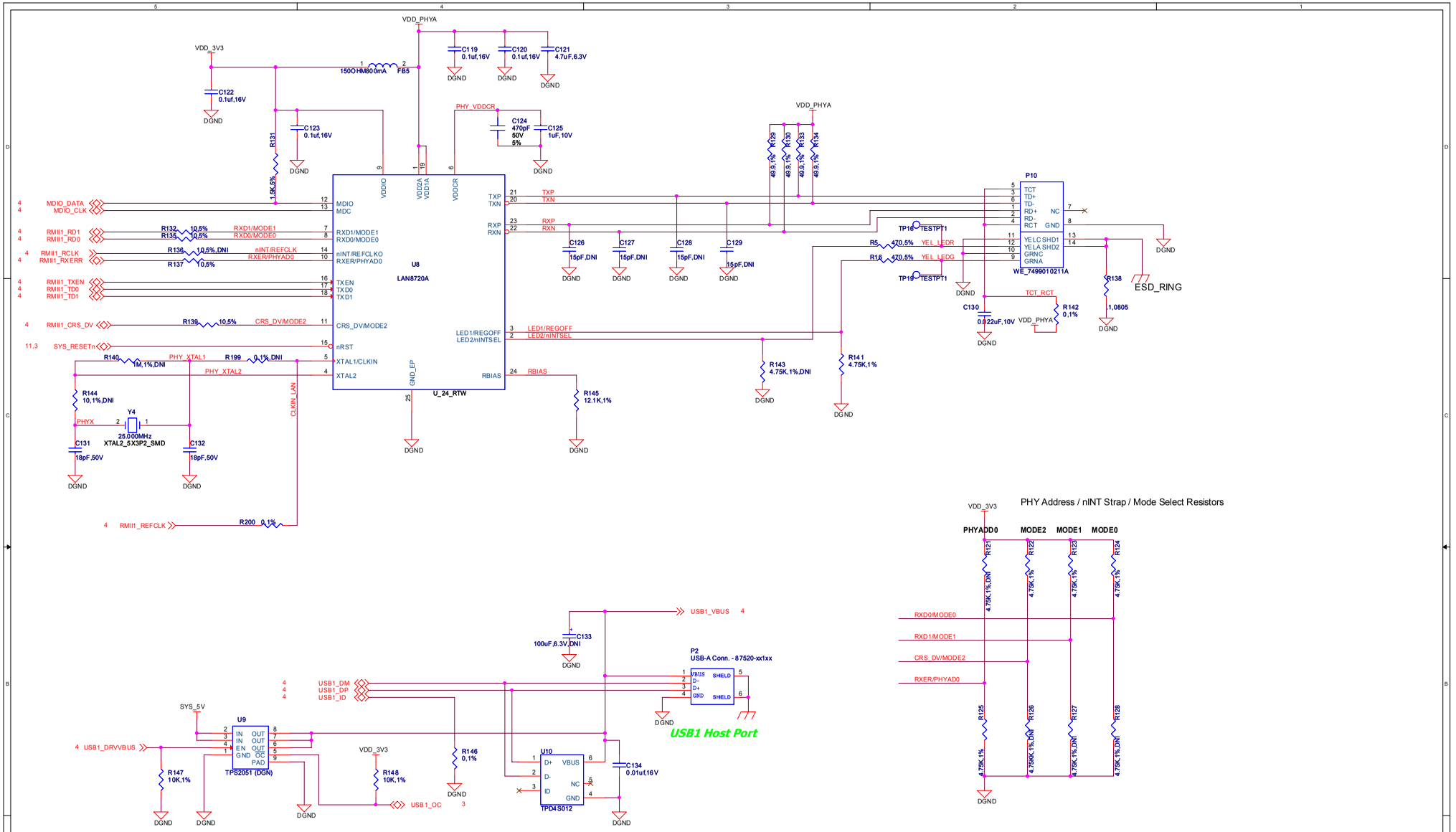
Texas Instruments Incorporated
WW Strategic Marketing
12500 TI Blvd
Dallas, TX 75243

Under Non Disclosure Agreement
TI - Proprietary Information
Do Not Copy

BeagleBone
DDR2 Mmeory and EEPROM

Size	Document Number	Modified by:	Rev
B	<Doc>	G. Coley	A1

Date: Monday, October 03, 2011 | Sheet 7 of 11



TEXAS INSTRUMENTS

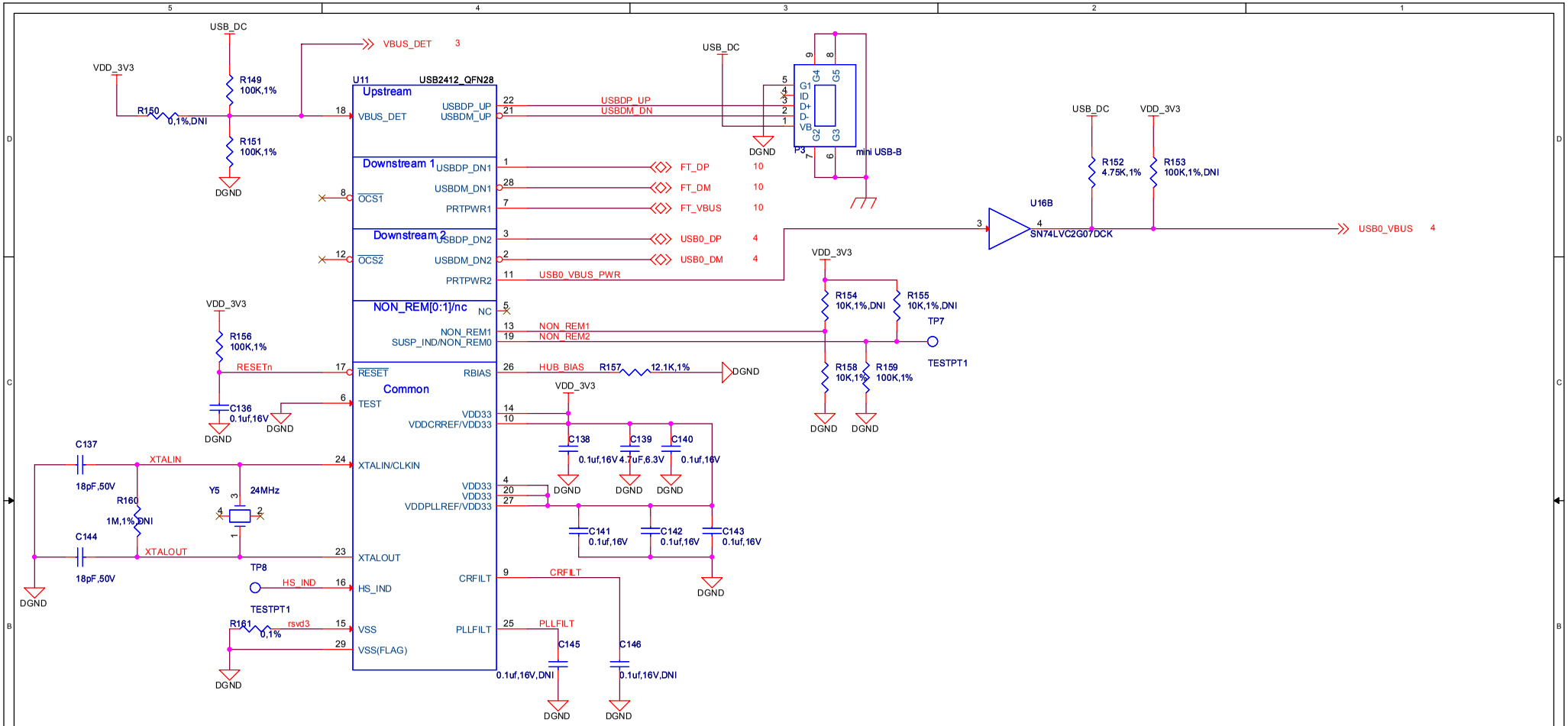
PRELIMINARY documents contain information on a product under development and is issued for evaluation purposes only. Features characteristic data and other information are subject to change.

Texas Instruments Incorporated
WW Strategic Marketing
12500 TI Blvd
Dallas, TX 75243

Under Non Disclosure Agreement
TI - Proprietary Information
Do Not Copy

BeagleBone
Subillo Ethernet and USB Host

Size	Document Number	Modified by:	Rev
C	<Doc>	G. Coley	A1
Date: Monday, October 03, 2011		Sheet 8 of 11	



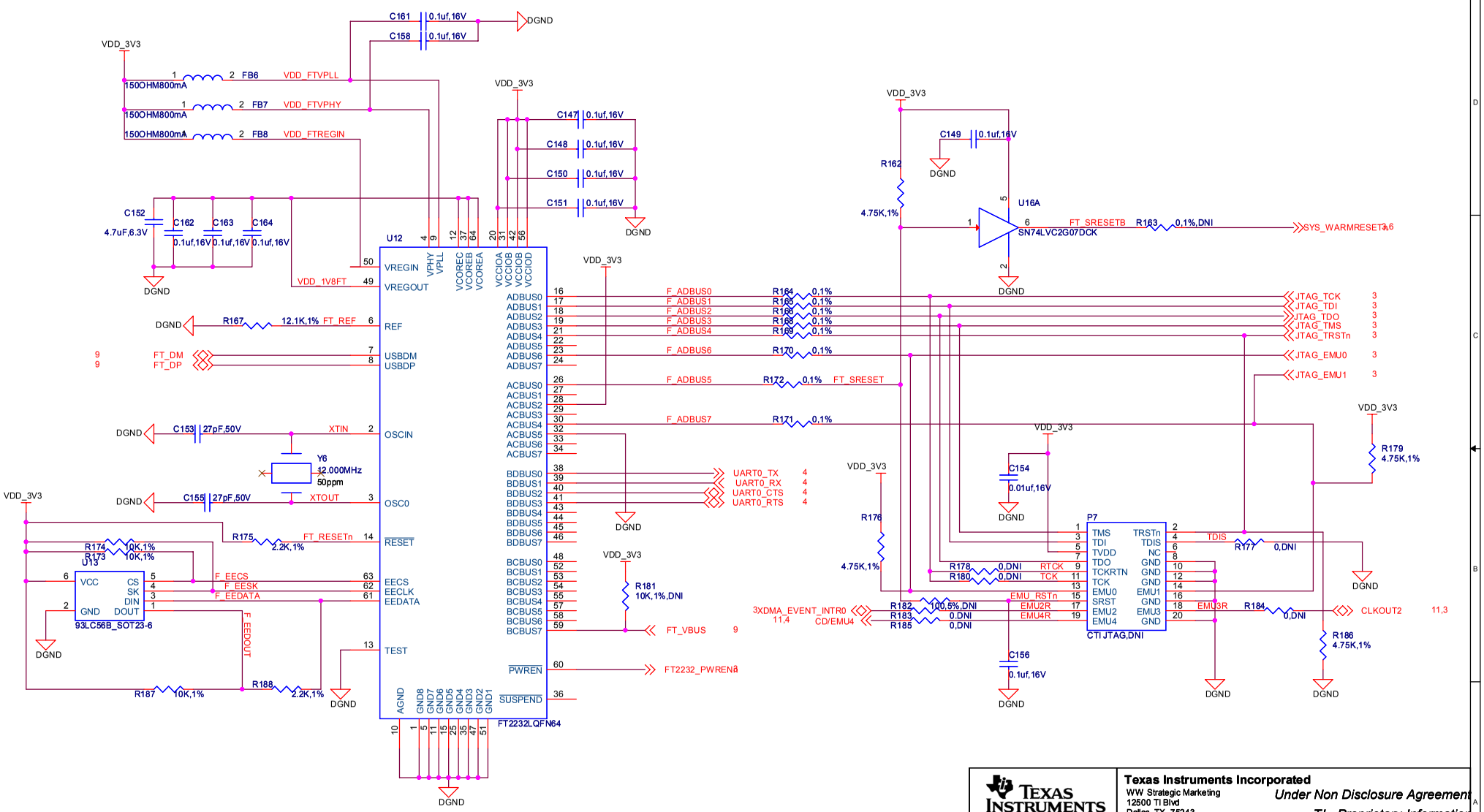
PRELIMINARY documents contain information on a product under development and is issued for evaluation purposes only. Features characteristic data and other information are subject to change.

Texas Instruments Incorporated
WW Strategic Marketing
12500 TI Blvd
Dallas, TX 75243

Under Non Disclosure Agreement
TI - Proprietary Information
Do Not Copy

BeagleBone
Serial, Debug, and SD

Size	Document Number	Modified by:	Rev
B	<Doc>	G. Coley	A1
Date:	Sunday, October 02, 2011	Sheet 9 of 11	



PRELIMINARY documents contain information on a product under development and is issued for evaluation purposes only. Features characteristic data and other information are subject to change.

Texas Instruments Incorporated
WW Strategic Marketing
12500 TI Blvd
Dallas, TX 75243

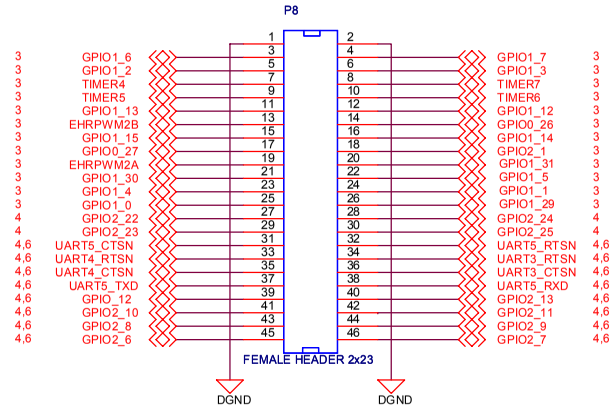
Under Non Disclosure Agreement
TI - Proprietary Information
Do Not Copy

BeagleBone
USB Serial Port and JTAG

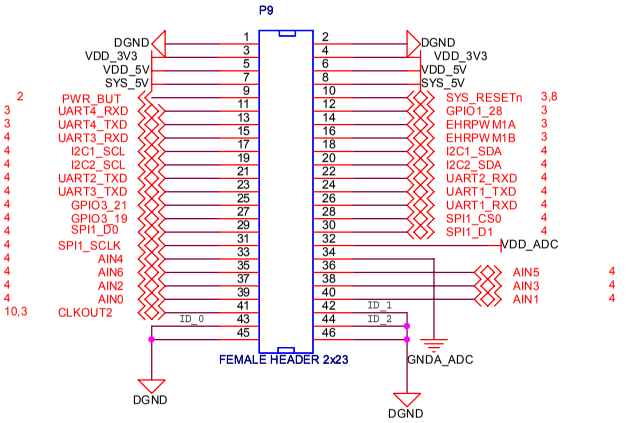
Size	Document Number	Modified by:	Rev
B	<Doc>	G. Coley	A1

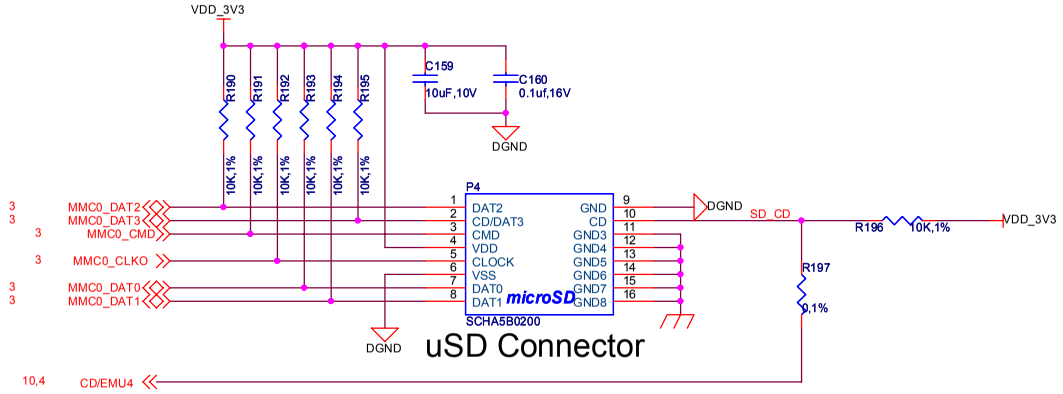
Date: Sunday, October 02, 2011 Sheet 10 of 10

CONN A



CONN B





TEXAS INSTRUMENTS

PRELIMINARY documents contain information on a product under development and is issued for evaluation purposes only. Features characteristic data and other information are subject to change.

Texas Instruments Incorporated
WW Strategic Marketing
12500 TI Blvd
Dallas, TX 75243

Under Non Disclosure Agreement
TI - Proprietary Information
Do Not Copy

BeagleBone
Expansion Connectors

Size	Document Number	Modified by:	Rev
B	<Doc>	G. Coley	A1

Date: Sunday, October 02, 2011 | Sheet 11 of 11