AM335x Applications Processor

1 AM335x Applications Processor

1.1 Features

- MPU Subsystem
  - 500 MHz[1], 600 MHz[2], or 720 MHz[3] ARM® Cortex™-A8 32-bit RISC microprocessor
  - NEON™ SIMD coprocessor
  - 32 KB of L1 Instruction cache with Single Error Detection (parity)
  - 32 KB of L1 Data cache with Single Error Detection (parity)
  - 256 KB of L2 cache with Error Correcting Code (ECC)
  - 176 KB of on-chip boot ROM
  - 64 KB of dedicated RAM
  - Emulation/Debug
    - JTAG.
    - Embedded Trace Module
    - Embedded Trace Buffer
  - Interrupt Controller (up to 128 interrupt requests)
- On-Chip Memory (Shared L3 RAM)
  - 64 KB of general purpose On-Chip Memory Controller (OCMC) RAM
  - Accessible to all Masters
  - Supports retention for fast wake-up
- External Memory Interfaces (EMIF)
  - mDDR/DDR2/DDR3 Controller:
    - mDDR: 200 MHz clock (400 MHz data rate)
    - DDR2: 266 MHz clock (532 MHz data rate)
    - DDR3: 303 MHz clock (606 MHz data rate)
    - 16-bit data bus
    - 1 GB of total addressable space
    - Supports one x16, two x8, or four x4 memory device configurations
    - Supports retention for fast wake-up
  - General Purpose Memory Controller (GPMC)
    - Flexible 8/16-bit asynchronous memory interface with up to 7 chip selects (NAND, NOR, Muxed-NOR, SRAM, etc.)[4]
    - Uses BCH code to support 4-bit, 8-bit, or 16-bit ECC
    - Uses Hamming code to support 1-bit ECC
  - Error Locator Module (ELM)
    - Used in conjunction with the GPMC to locate addresses of data errors from syndrome polynomials generated using a BCH algorithm
    - Supports 4-bit, 8-bit, and 16-bit per 512 byte block error location based on BCH algorithms
- Programmable Real-time Unit (PRU) Subsystem
  - Two PRUs
    - 32-bit Load/Store RISC processor capable of running at 200MHz
    - 8 KB instruction RAM with single error detection (parity)
    - 8 KB data RAM with single error detection (parity)
    - Single cycle 32-bit multiplier with 64-bit accumulator
    - Enhanced GPIO module[5] provides Shift In/Out support and parallel latch on external signal
  - 12 KB of shared RAM with Single Error Detection (parity)
  - Three 120 byte Register Banks accessible by each PRU
  - Interrupt controller module (INTC) for handling system input events
  - Local interconnect bus for connecting internal and external Masters to the resources inside the PRU subsystem
  - Peripherals inside the PRU subsystem[6][7]
    - One UART port with flow control pins, supports up to 12 Mbps
    - Two MII Ethernet Ports that support industrial Ethernet, such as EtherCAT®
    - One MDIO port
    - One enhanced Capture (eCAP) module
- Power Reset and Clock Management (PRCM) module
  - Controls the entry and exit of stand-by and deep-sleep modes

- Responsible for sleep sequencing, power domain switch-off sequencing, wake-up sequencing and power domain switch-on sequencing
- Clocks
  - Integrated 15-35 MHz high frequency oscillator used to generate a reference clock for various system and peripheral clocks[8]
  - Supports individual clock enable/disable control for subsystems and peripherals to facilitate reduced power consumption
  - 5 ADPLLs to generate system clocks (MPU Subsystem, DDR interface, USB & Peripherals [MMC/SD, UART, SPI, I2C, etc.], L3, L4, Ethernet, GFX [SGX530], LCD Pixel Clock)
- Power
  - 2 non-switchable power domains (Real Time Clock [RTC], Wake-up logic [WAKE-UP])
  - 3 switchable power domains (MPU subsystem [MPU], SGX530 [GFX], peripherals and infrastructure [PER])[9]
  - Implements SmartReflex™ Class 2B for core voltage scaling based on die temperature, process variation and performance (Adaptive Voltage Scaling [AVS])
  - Dynamic Voltage Frequency Scaling (DVFS)

- Real Time Clock (RTC)
  - Real-time date (day/month/year/day of week) and time (hours/minutes/seconds) information
  - Internal 32.768 KHz oscillator, RTC logic and 1.1 V internal LDO
  - Independent Power-on-Reset (RTC_PWRONRSTn) input[10]
  - Dedicated input pin (EXT_WAKEUP) for external wake events[10][11]
  - Programmable alarm can be used to generate internal interrupts to the PRCM (for wake up) or Cortex A8 (for event notification)
  - Programmable alarm can be used with external output (PMIC_POWER_EN) to enable the power management IC to restore non-RTC power domains[10]
- Peripherals[7]
  - Up to two USB 2.0 High Speed OTG Ports with integrated PHY[12]
  - Up to two Industrial gigabit Ethernet MACs (10/100/1000 Mbps)[12]
    - Integrated switch
    - Each MAC supports MII/RMII/RGMII and MDIO interfaces
    - Ethernet MACs and switch can operate independent of other functions
    - IEEE 1588 precision time protocol (PTP)
  - Up to two Controller–area Network (CAN) ports
    - Supports CAN version 2 parts A and B
  - Up to two Multi-channel Audio Serial Ports (McASP)
    - Transmit/Receive Clocks up to 50 MHz
    - Up to 4 serial data pins per McASP port with independent TX/RX clocks
    - Supports Time Division Multiplexing (TDM), Inter-IC Sound (I2S), and similar formats
    - Supports Digital Audio Interface Transmission (SPDIF, IEC60958-1, and AES-3 formats)
    - FIFO buffers for transmit and receive (256 bytes)
  - Up to six UARTs
    - All UARTs support IrDA, CIR and RTS, CTS flow control
    - UART1 supports full modem control
  - Up to two Master/Slave McSPI serial interfaces
    - Up to 2 chip selects
    - Up to 48 MHz
  - Up to three MMC/SD/SDIO ports
    - 1-bit, 4-bit and 8-bit MMC/SD/SDIO modes[13]
    - MMCSD0 has dedicated power rail for 1.8 V or 3.3 V operation
    - Up to 48 MHz data transfer rate
    - Supports card detect and write protect
    - Complies with MMC4.3 and SD/SDIO 2.0 specifications
  - Up to three I2C Master/Slave interfaces[14]
    - Standard mode (up to 100 KHz)
    - Fast mode (up to 400 KHz)
  - Up to four banks of General-purpose IO (GPIO)
    - 32 GPIOs per bank (multiplexed with other functional pins)
    - GPIOs can be used as interrupt inputs (up to 2 interrupt inputs per bank)
  - Up to three External DMA event inputs that can also be used as an interrupt inputs
  - Seven 32-bit general purpose timers
    - DMTIMER1 is a 1ms timer used for Operating System (OS) ticks
    - DMTIMER4 - DMTIMER7 are pinned out
  - One watchdog timer
  - SGX530 3D Graphics Engine
    - Tile based architecture delivering up to

20 MPloy/sec
- Universal Scalable Shader Engine is a multi-threaded engine incorporating Pixel and Vertex Shader functionality
- Advanced Shader Feature Set in excess of Microsoft VS3.0, PS3.0 and OGL2.0
- Industry standard API support of Direct3D Mobile, OGL-ES 1.1 and 2.0, OpenVG 1.0, and OpenMax
- Fine grained task switching, load balancing and power management
- Advanced geometry DMA driven operation for minimum CPU interaction
- Programmable high quality image anti-aliasing
- Fully virtualized memory addressing for OS operation in a unified memory architecture

– LCD Controller
- Up to 24-bits data output; 8-bits per pixel (RGB)
- Up to WXGA (1366x768) resolution
- Integrated LCD Interface Display Driver (LIDD) controller
- Integrated raster controller
- Integrated DMA engine to pull data from the external frame buffer without burdening the processor via interrupts or a firmware timer
- 512 word deep internal FIFO
- Supported Display types:
  – Character Displays - uses LCD Interface Display Driver (LIDD) controller to program these displays
  – Passive Matrix LCD Displays - uses LCD raster display controller to provide timing and data for constant graphics refresh to a passive display
  – Active Matrix LCD Displays - uses external Frame Buffer space and the internal DMA engine to drive streaming data to the panel. Maximum resolution is WXGA (1366x768) at 60 Hz Refresh Rate

– 12-bit Successive Approximation Register (SAR) ADC
- 100K samples per second
- Input can be selected from any of the 8 analog inputs multiplexed through an 8:1 analog switch
- Can be configured to operate as a 4-wire, 5-wire, or 8-wire resistive Touch Screen Controller (TSC) interface[15]

– Up to three 32-bit enhanced Capture Modules (eCAP)
- Configurable as 3 capture inputs or 3 auxiliary PWM outputs

– Up to three enhanced High Resolution PWM Modules (eHRPWM)
- Dedicated 16-bit time base counter with time and frequency controls
- Configurable as 6 Single Ended, 6 Dual Edge Symmetric, or 3 Dual Edge Asymmetric outputs

– Up to three 32-bit enhanced Quadrature Pulse Encoder (eQPE) modules

- Device Identification
  – Contains electrical fuse farm (FuseFarm) of which some bits are factory programmable
    - Production ID
    - Device part number (unique JTAG ID)
    - Device revision (readable by Host ARM)
- Debug Interface Support
  – JTAG/cJTAG for ARM (Cortex-A8 and PRCM), PRU debug
  – Embedded Trace Module (ETM) & Embedded Trace Buffer (ETB)
  – Supports device boundary scan
  – Supports IEEE1500
- DMA
  – On-chip Enhanced DMA controller (EDMA) has 3 Third Party Transfer Controllers (TPTC) and 1 Third Party Channel Controller (TPCC), which supports up to 64 programmable logical channels and 8 QDMA channels. EDMA is used for:
    - Transfers to/from on-chip memories
    - Transfers to/from external storage (EMIF, General Purpose Memory Controller, slave peripherals)
- Inter Processor Communication (IPC)
  – Integrates hardware based Mailbox for IPC and Spinlock for process synchronization between the Cortex A8, PRCM and each PRU
    - Mailbox registers that generate interrupts
      – 4 initiators (Cortex-A8, PRCM, PRU0, PRU1)[16] [17]
    - Spinlock has 128 Software assigned lock registers
- Security
  – Crypto hardware accelerators (AES, SHA, PKA, RNG)
- Boot Modes
  – Boot mode is selected via boot configuration pins latched on the rising edge of PWRONRSTn reset input pin
- Packages (see package descriptions):
  – 298-pin S-PBGA-N298 package (ZCE Suffix), .65mm Ball Pitch
  – 324-pin S-PBGA-N324 package (ZCZ Suffix), .80mm Ball Pitch

1.2 Applications

- **Gaming peripherals**
- **Home and Industrial automation**
- **Consumer medical appliances**
- **Printers**
- **Smart toll systems**
- **Connected vending machines**
- **Weighing scales**
- **Educational consoles**
- **Advanced toys**

1.3 Description

AM335x are broad market application processors with image, graphics processing, and peripherals.

The device supports high-level operating systems (OSs), such as:

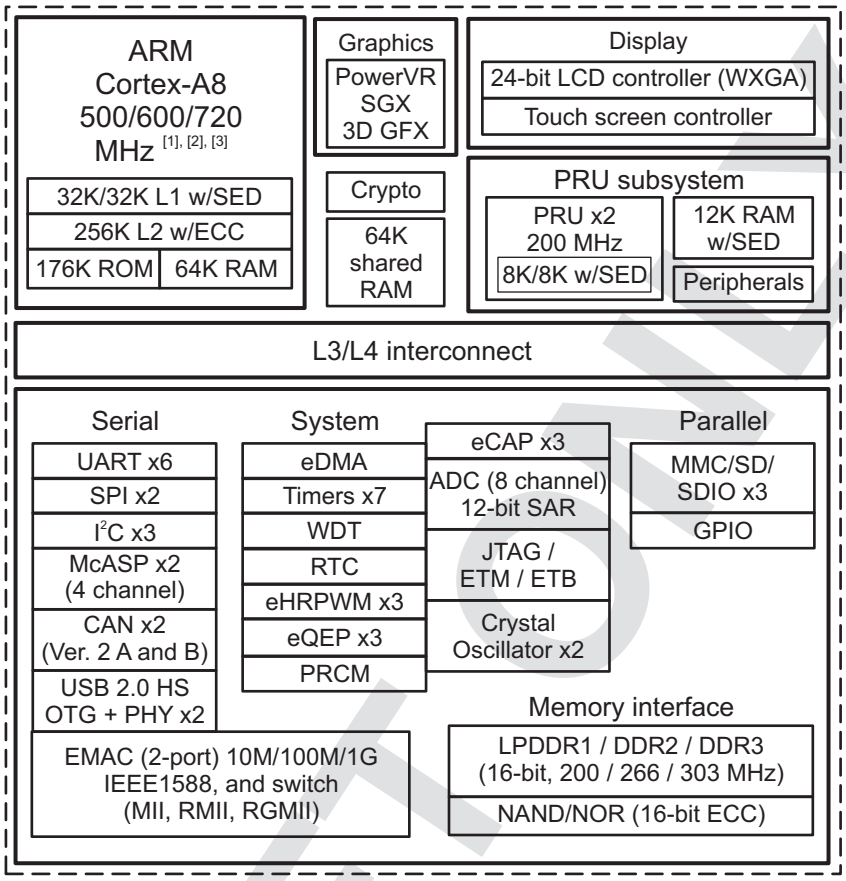
- Linux
- Windows CE
- Android

The AM335x Applications Processor contains these subsections:

- Microprocessor unit (MPU) subsystem based on the ARM Cortex-A8 microprocessor
- POWERVR® SGX Graphics Accelerator Subsystem for 3D graphics acceleration to support display and gaming effects.
- Programmable Real-time Unit (PRU) sub-system enables the user to create a variety of digital resources beyond native peripherals of the device. In addition, the PRU is separate from the ARM core. This allows independent operation and clocking to give the device greater flexibility in complex system solutions.
- High performance interconnects provide high-bandwidth data transfers for multiple initiators to the internal and external memory controllers and to on-chip peripherals. The device also offers a comprehensive clock-management scheme.
- The on-chip analog to digital converter (ADC) can be coupled with the LCD controller to provide an integrated touch screen solution. In addition, the ADC can be used in combination with the pulse width module to create a closed loop motor control solution.
- Real-time Clock (RTC) provides a clock reference on a separate power domain. This enables battery backed clock reference.

1.4 Functional Block Diagram

The functional block diagram of the AM335x Applications Processor is shown below.



[1] Nominal voltage condition (1.1v); available on ZCE and ZCZ packages.
[2] Overdrive voltage condition (1.2v); only available on ZCZ package.
[3] SR Turbo voltage condition (1.26v); only available on ZCZ package.

Figure 1-1. Functional Block Diagram for AM335x

1.5 Features Notes

1. Nominal voltage condition (1.1v); available on ZCE and ZCZ packages.
2. Overdrive voltage condition (1.2v); only available on ZCZ package.
3. SRTurbo voltage condition (1.26v); only available on ZCZ package .
4. Due to pin multiplexing all 7 CS pins may not be available.
5. Due to pin multiplexing these GPIO pins may not be available.
6. These peripherals are private to PRU subsystem and are not accessible for general purpose use.
7. All of the peripherals and peripheral functions listed may not be available concurrently.
8. The 15-35 MHz range will be refined to specific crystal frequencies supported by the boot-ROM.
9. The ZCZ package provides a dedicated power rail for MPU.
10. The RTC_PWRONRSTn input, EXT_WAKEUP input, and PMIC_POWER_EN output only supports 1.8v.
11. The EXT_WAKEUP output is only available on ZCZ package.
12. The ZCE package only supports one Ethernet port and one USB port.
13. 8-bit mode is only for MMC.
14. Standard LVCMOS buffers are used for I2C I/Os.

15. This function consumes some of the general purpose ADC inputs when configured as TSC. For example, only 4 general purpose ADC inputs are available when configured as a 4-wire TSC.
16. Inter Processor Communication between PRUs and PRCM is not supported.
17. PRCM does not have connectivity to L3/L4 targets. As a result IPC between Cortex A8 and PRCM is established through side band signaling.

2 Terminal Description

2.1 Pin Assignments

NOTE

The terms "ball", "pin", and "terminal are used interchangeably throughout the document. An attempt is made to use "ball" only when referring to the physical package.

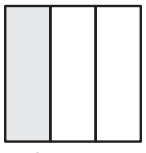
2.1.1 ZCE Package Pin Maps (Top View)

The pin maps below show the pin assignments on the ZCE package in three sections (left, middle, and right).

Table 2-1. ZCE Pin Map [Section Left - Top View]

	A	B	C	D	E	F
19	VSS	I2C0_SCL	UART1_TXD	UART1_RTSn	UART0_RXD	UART0_CTSn
18	SPI0_SCLK	SPI0_D0	I2C0_SDA	UART1_RXD	ECAP0_IN_PWM0_OUT	UART0_RTSn
17	SPI0_CS0	SPI0_D1	EXTINTn	XXXX	UART1_CTSn	UART0_TXD
16	WARMRSTn	SPI0_CS1	XXXX	XXXX	XXXX	VDDS
15	EMU0	XDMA_EVENT_INTR1	XDMA_EVENT_INTR0	XXXX	PWRONRSTn	XXXX
14	TDO	TCK	TMS	EMU1	XXXX	VDDSHV6
13	TRSTn	TDI	CAP_VBB_MPU	CAP_VDD_SRAM_MPU	VDDSHV6	VSS
12	AIN7	AIN5	VDDS_SRAM_MPU_BB	VDDS	VDDSHV6	VSS
11	AIN1	AIN3	XXXX	XXXX	VDDSHV6	VDD_CORE
10	AIN6	CAP_VDD_SRAM_CORE	VDDS_SRAM_CORE_BG	VSS	VSS	XXXX
9	VREFP	VREFN	XXXX	XXXX	VSS	VDD_CORE
8	AIN2	AIN0	AIN4	VSSA_ADC	VSS	VSS
7	RTC_KALDO_ENn	RTC_PWRONRSTn	PMIC_POWER_EN	VDDA_ADC	VSS	VSS
6	RTC_XTALIN	RESERVED	VDDS_RTC	CAP_VDD_RTC	XXXX	VSS
5	RTC_XTALOUT	EXT_WAKEUP	VDDS_PLL_DDR	XXXX	DDR_A4	XXXX
4	DDR_WEn	DDR_BA2	XXXX	XXXX	XXXX	DDR_A12
3	DDR_BA0	DDR_A3	DDR_A8	XXXX	DDR_A15	DDR_A0
2	DDR_A5	DDR_A9	DDR_CK	DDR_A7	DDR_A10	DDR_RASn
1	VSS	DDR_A6	DDR_CKn	DDR_A2	DDR_BA1	DDR_CASn

Pin map section location

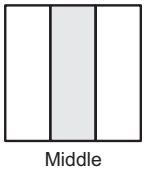


Left

Table 2-2. ZCE Pin Map [Section Middle - Top View]

	G	H	J	K	L	M
19	MMC0_CLK	MMC0_DAT3	MII1_COL	MII1_RX_ER	MII1_RX_DV	MII1_RX_CLK
18	MMC0_DAT0	MMC0_DAT2	MII1_CRS	RMII1_REF_CLK	MII1_TXD0	MII1_TXD1
17	MMC0_CMD	MMC0_DAT1	XXXX	MII1_TX_EN	XXXX	MII1_TXD3
16	USB0_DRVVBUS	VDDS_PLL_MPU	XXXX	VDD_CORE	XXXX	VDDS
15	VDDSHV4	VDDSHV4	VSS	VDD_CORE	VSS	VDDSHV5
14	XXXX	VDDSHV4	VSS	XXXX	VSS	VDDSHV5
13	XXXX	VDD_CORE	VDD_CORE	XXXX	VDD_CORE	VDD_CORE
12	VSS	VDD_CORE	VDD_CORE	VSS	VDD_CORE	VDD_CORE
11	VDD_CORE	VSS	VSS	VSS	VSS	VSS
10	XXXX	VSS	XXXX	XXXX	XXXX	VSS
9	VDD_CORE	VSS	VSS	VSS	VSS	VSS
8	VSS	VDD_CORE	VDD_CORE	VSS	VDD_CORE	VDD_CORE
7	XXXX	VDD_CORE	VDD_CORE	XXXX	VDD_CORE	VDD_CORE
6	XXXX	VDDS_DDR	VSS	XXXX	VSS	VDDS_DDR
5	VDDS_DDR	VDDS_DDR	VSS	VDDS_DDR	VSS	VDDS_DDR
4	DDR_A11	DDR_VREF	XXXX	VDDS_DDR	XXXX	DDR_D11
3	DDR_CKE	DDR_A14	XXXX	DDR_DQM1	XXXX	DDR_D10
2	DDR_RESETn	DDR_CSn0	DDR_A1	DDR_D8	DDR_DQSn1	DDR_D12
1	DDR_ODT	DDR_A13	DDR_VTP	DDR_D9	DDR_DQS1	DDR_D13

Pin map section location

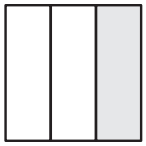


Middle

Table 2-3. ZCE Pin Map [Section Right - Top View]

	N	P	R	T	U	V	W
19	MII1_TX_CLK	MII1_RXD1	MDC	USB0_VBUS	USB0_DP	USB0_ID	VSS
18	MII1_TXD2	MII1_RXD0	VDDA3P3V_USB0	USB0_CE	USB0_DM	GPMC_BEn1	GPMC_WPn
17	MII1_RXD3	MDIO	VDDA1P8V_USB0	XXXX	GPMC_CSn3	GPMC_AD15	GPMC_AD14
16	MII1_RXD2	VSSA_USB	XXXX	XXXX	XXXX	GPMC_CLK	GPMC_AD9
15	VDDSHV5	XXXX	GPMC_WAIT0	XXXX	GPMC_CSn2	GPMC_AD8	GPMC_AD7
14	XXXX	VSS	XXXX	VDDS	GPMC_AD6	GPMC_CSn1	GPMC_AD5
13	XXXX	VSS	VDDSHV1	GPMC_AD13	GPMC_AD12	GPMC_AD4	GPMC_AD3
12	VSS	VSS	VDDSHV1	GPMC_AD10	GPMC_AD11	GPMC_AD2	XTALOUT
11	VDD_CORE	VDD_CORE	VDDSHV1	XXXX	XXXX	VSS_OSC	XTALIN
10	XXXX	XXXX	VSS	VSS	VDDS_OSC	GPMC_ADVn_ALE	GPMC_AD0
9	VDD_CORE	VDD_CORE	VDDSHV1	XXXX	XXXX	GPMC_AD1	GPMC_OEn_REn
8	VSS	VSS	VDDSHV1	VDDS_PLL_CORE_LCD	GPMC_WEn	GPMC_BEn0_CLE	GPMC_CSn0
7	XXXX	VSS	VDDSHV6	LCD_HSYNC	LCD_VSYNC	LCD_DATA15	LCD_AC_BIAS_EN
6	XXXX	VDDSHV6	XXXX	VDDS	LCD_DATA13	LCD_DATA12	LCD_DATA14
5	VDDS_DDR	XXXX	VPP	XXXX	LCD_DATA10	LCD_DATA11	LCD_PCLK
4	DDR_D0	DDR_D1	XXXX	XXXX	XXXX	LCD_DATA8	LCD_DATA9
3	DDR_DQM0	DDR_D4	DDR_D7	XXXX	LCD_DATA7	LCD_DATA6	LCD_DATA5
2	DDR_D14	DDR_D2	DDR_DQSn0	DDR_D6	LCD_DATA1	LCD_DATA3	LCD_DATA4
1	DDR_D15	DDR_D3	DDR_DQS0	DDR_D5	LCD_DATA0	LCD_DATA2	VSS

Pin map section location



Right

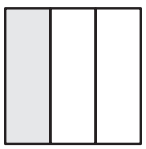
2.1.2 ZCZ Package Pin Maps (Top View)

The pin maps below show the pin assignments on the ZCZ package in three sections (left, middle, and right).

Table 2-4. ZCZ Pin Map [Section Left - Top View]

	A	B	C	D	E	F
18	VSS	EXTINTn	ECAP0_IN_PWM0_OUT	UART1_CTSn	UART0_CTSn	MMC0_DAT2
17	SPI0_SCLK	SPI0_D0	I2C0_SDA	UART1_RTSn	UART0_RTSn	MMC0_DAT3
16	SPI0_CS0	SPI0_D1	I2C0_SCL	UART1_RXD	UART0_TXD	USB0_DRVVBUS
15	XDMA_EVENT_INTR0	PWRONRSTn	SPI0_CS1	UART1_TXD	UART0_RXD	USB1_DRVVBUS
14	MCASP0_AHCLKX	EMU1	EMU0	XDMA_EVENT_INTR1	VDDS	VDDSHV6
13	MCASP0_ACLKX	MCASP0_FSX	MCASP0_FSR	MCASP0_AXR1	VDDSHV6	VDD_MPU
12	TCK	MCASP0_ACLKR	MCASP0_AHCLKR	MCASP0_AXR0	VDDSHV6	VDD_MPU
11	TDO	TDI	TMS	CAP_VDD_SRAM_MPU	VDDSHV6	VDD_MPU
10	WARMRSTn	TRSTn	CAP_VBB_MPU	VDDS_SRAM_MPU_BB	VDDSHV6	VDD_MPU
9	VREFN	VREFP	AIN7	CAP_VDD_SRAM_CORE	VDDS_SRAM_CORE_BG	VDDS
8	AIN6	AIN5	AIN4	VDDA_ADC	VSSA_ADC	VSS
7	AIN3	AIN2	AIN1	VDDS_RTC	VDDS_PLL_DDR	VDD_CORE
6	RTC_XTALIN	AIN0	PMIC_POWER_EN	CAP_VDD_RTC	VDDS	VDD_CORE
5	VSS_RTC	RTC_PWRONRSTn	EXT_WAKEUP	DDR_A6	VDDS_DDR	VDDS_DDR
4	RTC_XTALOUT	RTC_KALDO_ENn	DDR_BA0	DDR_A8	DDR_A2	DDR_A10
3	RESERVED	DDR_BA2	DDR_A3	DDR_A15	DDR_A12	DDR_A0
2	VDD_MPU_MON	DDR_WEn	DDR_A4	DDR_CK	DDR_A7	DDR_A11
1	VSS	DDR_A5	DDR_A9	DDR_CKn	DDR_BA1	DDR_CASn

Pin map section location

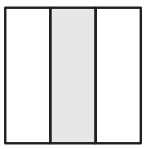


Left

Table 2-5. ZCZ Pin Map [Section Middle - Top View]

	G	H	J	K	L	M
18	MMC0_CMD	RMII1_REF_CLK	MII1_TXD3	MII1_TX_CLK	MII1_RX_CLK	MDC
17	MMC0_CLK	MII1_CRS	MII1_RX_DV	MII1_TXD0	MII1_RXD3	MDIO
16	MMC0_DAT0	MII1_COL	MII1_TX_EN	MII1_TXD1	MII1_RXD2	MII1_RXD0
15	MMC0_DAT1	VDDS_PLL_MPU	MII1_RX_ER	MII1_TXD2	MII1_RXD1	USB0_CE
14	VDDSHV6	VDDSHV4	VDDSHV4	VDDSHV5	VDDSHV5	VSSA_USB
13	VDD_MPU	VDD_MPU	VDD_MPU	VDDS	VSS	VDD_CORE
12	VSS	VSS	VDD_CORE	VDD_CORE	VSS	VSS
11	VSS	VDD_CORE	VSS	VSS	VSS	VDD_CORE
10	VDD_CORE	VSS	VSS	VSS	VSS	VSS
9	VSS	VSS	VSS	VSS	VDD_CORE	VSS
8	VSS	VSS	VSS	VDD_CORE	VDD_CORE	VSS
7	VDD_CORE	VSS	VSS	VSS	VDD_CORE	VSS
6	VDD_CORE	VSS	VSS	VDD_CORE	VDD_CORE	VSS
5	VDDS_DDR	VDDS_DDR	VDDS_DDR	VDDS_DDR	VDDS_DDR	VPP
4	DDR_RASn	DDR_A14	DDR_VREF	DDR_D12	DDR_D14	DDR_D1
3	DDR_CKE	DDR_A13	DDR_VTP	DDR_D11	DDR_D13	DDR_D0
2	DDR_RESETn	DDR_CSn0	DDR_DQM1	DDR_D10	DDR_DQSn1	DDR_DQM0
1	DDR_ODT	DDR_A1	DDR_D8	DDR_D9	DDR_DQS1	DDR_D15

Pin map section location

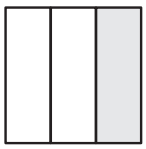


Middle

Table 2-6. ZCZ Pin Map [Section Right - Top View]

	N	P	R	T	U	V
18	USB0_DM	USB1_CE	USB1_DM	USB1_VBUS	GPMC_BEn1	VSS
17	USB0_DP	USB1_ID	USB1_DP	GPMC_WAIT0	GPMC_WPn	GPMC_A11
16	VDDA1P8V_USB0	USB0_ID	VDDA1P8V_USB1	GPMC_A10	GPMC_A9	GPMC_A8
15	VDDA3P3V_USB0	USB0_VBUS	VDDA3P3V_USB1	GPMC_A7	GPMC_A6	GPMC_A5
14	VSSA_USB	VDDS	GPMC_A4	GPMC_A3	GPMC_A2	GPMC_A1
13	VDD_CORE	VDDSHV3	GPMC_A0	GPMC_CSn3	GPMC_AD15	GPMC_AD14
12	VDD_CORE	VDDSHV3	GPMC_AD13	GPMC_AD12	GPMC_AD11	GPMC_CLK
11	VSS	VDDSHV2	VDDS_OSC	GPMC_AD10	XTALOUT	VSS_OSC
10	VSS	VDDSHV2	VDDS_PLL_CORE_LCD	GPMC_AD9	GPMC_AD8	XTALIN
9	VDD_CORE	VDDS	GPMC_AD6	GPMC_AD7	GPMC_CSn1	GPMC_CSn2
8	VDD_CORE	VDDSHV1	GPMC_AD2	GPMC_AD3	GPMC_AD4	GPMC_AD5
7	VSS	VDDSHV1	GPMC_ADVn_ALE	GPMC_OEn_REn	GPMC_AD0	GPMC_AD1
6	VDDS	VDDSHV6	LCD_AC_BIAS_EN	GPMC_BEn0_CLE	GPMC_WEn	GPMC_CSn0
5	VDDSHV6	VDDSHV6	LCD_HSYNC	LCD_DATA15	LCD_VSYNC	LCD_PCLK
4	DDR_D5	DDR_D7	LCD_DATA3	LCD_DATA7	LCD_DATA11	LCD_DATA14
3	DDR_D4	DDR_D6	LCD_DATA2	LCD_DATA6	LCD_DATA10	LCD_DATA13
2	DDR_D3	DDR_DQSn0	LCD_DATA1	LCD_DATA5	LCD_DATA9	LCD_DATA12
1	DDR_D2	DDR_DQS0	LCD_DATA0	LCD_DATA4	LCD_DATA8	VSS

Pin map section location



Right

2.2 Ball Characteristics

The table below identifies the terminal characteristics signals multiplexed on each terminal for the ZCZ and ZCE packages. The table column headers are explained below:

1. **BALL NUMBER:** Package ball number(s) associated with each signal(s).
2. **PIN NAME:** The name of the package pin or terminal.
   Note: The table does not take into account subsystem terminal multiplexing options.
3. **SIGNAL NAME**: The signal name for that pin in the mode being used.
4. **MODE:** Multiplexing mode number.
   (a) Mode 0 is the primary mode; this means that when mode 0 is set, the function mapped on the terminal corresponds to the name of the terminal. There is always a function mapped on the primary mode. Notice that primary mode is not necessarily the default mode.

   Note: The default mode is the mode at the release of the reset; also see the RESET REL. MODE column.
   (b) Modes 1 to 7 are possible modes for alternate functions. On each terminal, some modes are effectively used for alternate functions, while some modes are not used and do not correspond to a functional configuration.
5. **TYPE:** Signal direction
   - I = Input
   - O = Output
   - I/O = Input/Output
   - D = Open drain
   - DS = Differential
   - A = Analog
   - PWR = Power
   - GND = Ground

   Note: In the safe_mode, the buffer is configured in high-impedance.
6. **BALL RESET STATE:** The state of the terminal at the power-on reset.
   - 0: The buffer drives V_{OL} (pulldown/pullup resistor not activated)
     0(PD): The buffer drives V_{OL} with an active pulldown resistor.
   - 1: The buffer drives V_{OH} (pulldown/pullup resistor not activated)
     1(PU): The buffer drives V_{OH} with an active pullup resistor.
   - Z: High-impedance
   - L: High-impedance with an active pulldown resistor
   - H : High-impedance with an active pullup resistor
7. **BALL RESET REL. STATE:** The state of the terminal at the release of the System Control Module reset (PRCM CORE_RSTPWRON_RET reset signal).
   - 0: The buffer drives V_{OL} (pulldown/pullup resistor not activated)
     0(PD): The buffer drives V_{OL} with an active pulldown resistor.
   - 1: The buffer drives V_{OH} (pulldown/pullup resistor not activated)
     1(PU): The buffer drives V_{OH} with an active pullup resistor.
   - Z: High-impedance
   - L: High-impedance with an active pulldown resistor
   - H : High-impedance with an active pullup resistor
8. **RESET REL. MODE:** The mode is automatically configured at the release of the System Control Module reset (PRCM CORE_RSTPWRON_RET reset signal).
9. **POWER:** The voltage supply that powers the terminal's I/O buffers.
10. **HYS:** Indicates if the input buffer is with hysteresis.
11. **BUFFER STRENGTH:** Drive strength of the associated output buffer.
12. **PULLUP/DOWN TYPE:** Denotes the presence of an internal pullup or pulldown resistor. Pullup and

pulldown resistors can be enabled or disabled via software.

13. **I/O CELL:** IO cell information.

Note: Configuring two terminals to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration.

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
B8	B6	AIN0	AIN0	0	A (13)	Z	Z	0	VDDA_ADC / VDDA_ADC	NA	50	NA	Analog
A11	C7	AIN1	AIN1	0	A (12)	Z	Z	0	VDDA_ADC / VDDA_ADC	NA	50	NA	Analog
A8	B7	AIN2	AIN2	0	A (12)	Z	Z	0	VDDA_ADC / VDDA_ADC	NA	50	NA	Analog
B11	A7	AIN3	AIN3	0	A (11)	Z	Z	0	VDDA_ADC / VDDA_ADC	NA	50	NA	Analog
C8	C8	AIN4	AIN4	0	A (11)	Z	Z	0	VDDA_ADC / VDDA_ADC	NA	50	NA	Analog
B12	B8	AIN5	AIN5	0	A	Z	Z	0	VDDA_ADC / VDDA_ADC	NA	NA	NA	Analog
A10	A8	AIN6	AIN6	0	A	Z	Z	0	VDDA_ADC / VDDA_ADC	NA	NA	NA	Analog
A12	C9	AIN7	AIN7	0	A	Z	Z	0	VDDA_ADC / VDDA_ADC	NA	NA	NA	Analog
C13	C10	CAP_VBB_MPU	CAP_VBB_MPU	NA	A								
D6	D6	CAP_VDD_RTC	CAP_VDD_RTC	NA	A								
B10	D9	CAP_VDD_SRAM_CORE	CAP_VDD_SRAM_CORE	NA	A								
D13	D11	CAP_VDD_SRAM_MPU	CAP_VDD_SRAM_MPU	NA	A								
F3	F3	DDR_A0	ddr_a0	0	O	H	1	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
J2	H1	DDR_A1	ddr_a1	0	O	H	1	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
D1	E4	DDR_A2	ddr_a2	0	O	H	1	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
B3	C3	DDR_A3	ddr_a3	0	O	H	1	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
E5	C2	DDR_A4	ddr_a4	0	O	H	1	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
A2	B1	DDR_A5	ddr_a5	0	O	H	1	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
B1	D5	DDR_A6	ddr_a6	0	O	H	1	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
D2	E2	DDR_A7	ddr_a7	0	O	H	1	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
C3	D4	DDR_A8	ddr_a8	0	O	H	1	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
B2	C1	DDR_A9	ddr_a9	0	O	H	1	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
E2	F4	DDR_A10	ddr_a10	0	O	H	1	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
G4	F2	DDR_A11	ddr_a11	0	O	H	1	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
F4	E3	DDR_A12	ddr_a12	0	O	H	1	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
H1	H3	DDR_A13	ddr_a13	0	O	H	1	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
H3	H4	DDR_A14	ddr_a14	0	O	H	1	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
E3	D3	DDR_A15	ddr_a15	0	O	H	1	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
A3	C4	DDR_BA0	ddr_ba0	0	O	H	1	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
E1	E1	DDR_BA1	ddr_ba1	0	O	H	1	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
B4	B3	DDR_BA2	ddr_ba2	0	O	H	1	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
F1	F1	DDR_CASn	ddr_casn	0	O	H	1	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
C2	D2	DDR_CK	ddr_ck	0	O	L	0	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
G3	G3	DDR_CKE	ddr_cke	0	O	L	0	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
C1	D1	DDR_CKn	ddr_nck	0	O	H	1	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
H2	H2	DDR_CSn0	ddr_csn0	0	O	H	1	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
N4	M3	DDR_D0	ddr_d0	0	I/O	L	Z	0	VDDS_DDR / VDDS_DDR	Yes	8	PU/PD	LVCMOS/SSTL/ HSTL
P4	M4	DDR_D1	ddr_d1	0	I/O	L	Z	0	VDDS_DDR / VDDS_DDR	Yes	8	PU/PD	LVCMOS/SSTL/ HSTL
P2	N1	DDR_D2	ddr_d2	0	I/O	L	Z	0	VDDS_DDR / VDDS_DDR	Yes	8	PU/PD	LVCMOS/SSTL/ HSTL
P1	N2	DDR_D3	ddr_d3	0	I/O	L	Z	0	VDDS_DDR / VDDS_DDR	Yes	8	PU/PD	LVCMOS/SSTL/ HSTL
P3	N3	DDR_D4	ddr_d4	0	I/O	L	Z	0	VDDS_DDR / VDDS_DDR	Yes	8	PU/PD	LVCMOS/SSTL/ HSTL
T1	N4	DDR_D5	ddr_d5	0	I/O	L	Z	0	VDDS_DDR / VDDS_DDR	Yes	8	PU/PD	LVCMOS/SSTL/ HSTL
T2	P3	DDR_D6	ddr_d6	0	I/O	L	Z	0	VDDS_DDR / VDDS_DDR	Yes	8	PU/PD	LVCMOS/SSTL/ HSTL
R3	P4	DDR_D7	ddr_d7	0	I/O	L	Z	0	VDDS_DDR / VDDS_DDR	Yes	8	PU/PD	LVCMOS/SSTL/ HSTL
K2	J1	DDR_D8	ddr_d8	0	I/O	L	Z	0	VDDS_DDR / VDDS_DDR	Yes	8	PU/PD	LVCMOS/SSTL/ HSTL
K1	K1	DDR_D9	ddr_d9	0	I/O	L	Z	0	VDDS_DDR / VDDS_DDR	Yes	8	PU/PD	LVCMOS/SSTL/ HSTL
M3	K2	DDR_D10	ddr_d10	0	I/O	L	Z	0	VDDS_DDR / VDDS_DDR	Yes	8	PU/PD	LVCMOS/SSTL/ HSTL

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
M4	K3	DDR_D11	ddr_d11	0	I/O	L	Z	0	VDDS_DDR / VDDS_DDR	Yes	8	PU/PD	LVCMOS/SSTL/ HSTL
M2	K4	DDR_D12	ddr_d12	0	I/O	L	Z	0	VDDS_DDR / VDDS_DDR	Yes	8	PU/PD	LVCMOS/SSTL/ HSTL
M1	L3	DDR_D13	ddr_d13	0	I/O	L	Z	0	VDDS_DDR / VDDS_DDR	Yes	8	PU/PD	LVCMOS/SSTL/ HSTL
N2	L4	DDR_D14	ddr_d14	0	I/O	L	Z	0	VDDS_DDR / VDDS_DDR	Yes	8	PU/PD	LVCMOS/SSTL/ HSTL
N1	M1	DDR_D15	ddr_d15	0	I/O	L	Z	0	VDDS_DDR / VDDS_DDR	Yes	8	PU/PD	LVCMOS/SSTL/ HSTL
N3	M2	DDR_DQM0	ddr_dqm0	0	O	H	1	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
K3	J2	DDR_DQM1	ddr_dqm1	0	O	H	1	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
R1	P1	DDR_DQS0	ddr_dqs0	0	I/O	L	Z	0	VDDS_DDR / VDDS_DDR	Yes	8	PU/PD	LVCMOS/SSTL/ HSTL
L1	L1	DDR_DQS1	ddr_dqs1	0	I/O	L	Z	0	VDDS_DDR / VDDS_DDR	Yes	8	PU/PD	LVCMOS/SSTL/ HSTL
R2	P2	DDR_DQSn0	ddr_dqsn0	0	I/O	L	Z	0	VDDS_DDR / VDDS_DDR	Yes	8	PU/PD	LVCMOS/SSTL/ HSTL
L2	L2	DDR_DQSn1	ddr_dqsn1	0	I/O	L	Z	0	VDDS_DDR / VDDS_DDR	Yes	8	PU/PD	LVCMOS/SSTL/ HSTL
G1	G1	DDR_ODT	ddr_odt	0	O	L	0	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
F2	G4	DDR_RASn	ddr_rasn	0	O	H	1	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
G2	G2	DDR_RESETn	ddr_resetn	0	O	L	0	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
H4	J4	DDR_VREF	ddr_vref	0	AP (9)	NA	NA	NA	VDDS_DDR / VDDS_DDR	NA	NA	NA	Analog
J1	J3	DDR_VTP	ddr_vtp	0	I (10)	NA	NA	NA	VDDS_DDR / VDDS_DDR	NA	NA	NA	Analog
A4	B2	DDR_WEn	ddr_wen	0	O	H	1	0	VDDS_DDR / VDDS_DDR	NA	8	PU/PD	LVCMOS/SSTL/ HSTL
E18	C18	ECAP0_IN_PWM0_OUT	eCAP0_in_PWM0_out	0	I/O	Z	L	7	VDDSHV6 / VDDSHV6	Yes	4	PU/PD	LVCMOS
			uart3_txd	1	O								
			spi1_cs1	2	I/O								
			pr1_ecap0_ecap_capin_apwm_o	3	I/O								
			spi1_sclk	4	I/O								
			mmc0_sdwp	5	I								
			xdma_event_intr2	6	I								
			gpio0_7	7	I/O								
A15	C14	EMU0	EMU0	0	I/O	H	H	0	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			gpio3_7	7	I/O								

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
D14	B14	EMU1	EMU1	0	I/O	H	H	0	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			gpio3_8	7	I/O								
C17	B18	EXTINTn	nNMI	0	I	Z	H	0	VDDSHV6 / VDDSHV6	Yes	NA	PU/PD	LVCMOS
B5	C5	EXT_WAKEUP	EXT_WAKEUP	0	I	L	L	0	VDDS_RTC / VDDS_RTC	Yes	NA	NA	LVCMOS
NA	R13	GPMC_A0	gpmc_a0	0	O	L	L	7	NA / VDDSHV3	Yes	6	PU/PD	LVCMOS
			gmii2_txen	1	O								
			rgmii2_tctl	2	O								
			rmii2_txen	3	O								
			gpmc_a16	4	O								
			pr1_mii_mt1_clk	5	I								
			ehrpwm1_tripzone_input	6	I								
			gpio1_16	7	I/O								
NA	V14	GPMC_A1	gpmc_a1	0	O	L	L	7	NA / VDDSHV3	Yes	6	PU/PD	LVCMOS
			gmii2_rxdv	1	I								
			rgmii2_rctl	2	I								
			mmc2_dat0	3	I/O								
			gpmc_a17	4	O								
			pr1_mii1_txd3	5	O								
			ehrpwm0_synco	6	O								
			gpio1_17	7	I/O								
NA	U14	GPMC_A2	gpmc_a2	0	O	L	L	7	NA / VDDSHV3	Yes	6	PU/PD	LVCMOS
			gmii2_txd3	1	O								
			rgmii2_td3	2	O								
			mmc2_dat1	3	I/O								
			gpmc_a18	4	O								
			pr1_mii1_txd2	5	O								
			ehrpwm1A	6	O								
			gpio1_18	7	I/O								
NA	T14	GPMC_A3	gpmc_a3	0	O	L	L	7	NA / VDDSHV3	Yes	6	PU/PD	LVCMOS
			gmii2_txd2	1	O								
			rgmii2_td2	2	O								
			mmc2_dat2	3	I/O								
			gpmc_a19	4	O								
			pr1_mii1_txd1	5	O								
			ehrpwm1B	6	O								
			gpio1_19	7	I/O								

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
NA	R14	GPMC_A4	gpmc_a4	0	O	L	L	7	NA / VDDSHV3	Yes	6	PU/PD	LVCMOS
			gmii2_txd1	1	O								
			rgmii2_td1	2	O								
			rmii2_txd1	3	O								
			gpmc_a20	4	O								
			pr1_mii1_txd0	5	O								
			eQEP1A_in	6	I								
			gpio1_20	7	I/O								
NA	V15	GPMC_A5	gpmc_a5	0	O	L	L	7	NA / VDDSHV3	Yes	6	PU/PD	LVCMOS
			gmii2_txd0	1	O								
			rgmii2_td0	2	O								
			rmii2_txd0	3	O								
			gpmc_a21	4	O								
			pr1_mii1_rxd3	5	I								
			eQEP1B_in	6	I								
			gpio1_21	7	I/O								
NA	U15	GPMC_A6	gpmc_a6	0	O	L	L	7	NA / VDDSHV3	Yes	6	PU/PD	LVCMOS
			gmii2_txclk	1	I								
			rgmii2_tclk	2	O								
			mmc2_dat4	3	I/O								
			gpmc_a22	4	O								
			pr1_mii1_rxd2	5	I								
			eQEP1_index	6	I/O								
			gpio1_22	7	I/O								
NA	T15	GPMC_A7	gpmc_a7	0	O	L	L	7	NA / VDDSHV3	Yes	6	PU/PD	LVCMOS
			gmii2_rxclk	1	I								
			rgmii2_rclk	2	I								
			mmc2_dat5	3	I/O								
			gpmc_a23	4	O								
			pr1_mii1_rxd1	5	I								
			eQEP1_strobe	6	I/O								
			gpio1_23	7	I/O								

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
NA	V16	GPMC_A8	gpmc_a8	0	O	L	L	7	NA / VDDSHV3	Yes	6	PU/PD	LVCMOS
			gmii2_rxd3	1	I								
			rgmii2_rd3	2	I								
			mmc2_dat6	3	I/O								
			gpmc_a24	4	O								
			pr1_mii1_rxd0	5	I								
			mcasp0_aclkx	6	I/O								
			gpio1_24	7	I/O								
NA	U16	GPMC_A9	gpmc_a9	0	O	L	L	7	NA / VDDSHV3	Yes	6	PU/PD	LVCMOS
			gmii2_rxd2	1	I								
			rgmii2_rd2	2	I								
			mmc2_dat7	3	I/O								
			gpmc_a25	4	O								
			pr1_mii_mr1_clk	5	I								
			mcasp0_fsx	6	I/O								
			gpio1_25	7	I/O								
NA	T16	GPMC_A10	gpmc_a10	0	O	L	L	7	NA / VDDSHV3	Yes	6	PU/PD	LVCMOS
			gmii2_rxd1	1	I								
			rgmii2_rd1	2	I								
			rmii2_rxd1	3	I								
			gpmc_a26	4	O								
			pr1_mii1_rxdv	5	I								
			mcasp0_axr0	6	I/O								
			gpio1_26	7	I/O								
NA	V17	GPMC_A11	gpmc_a11	0	O	L	L	7	NA / VDDSHV3	Yes	6	PU/PD	LVCMOS
			gmii2_rxd0	1	I								
			rgmii2_rd0	2	I								
			rmii2_rxd0	3	I								
			gpmc_a27	4	O								
			pr1_mii1_rxer	5	I								
			mcasp0_axr1	6	I/O								
			gpio1_27	7	I/O								
W10	U7	GPMC_AD0	gpmc_ad0	0	I/O	L	L	7	VDDSHV1 / VDDSHV1	Yes	6	PU/PD	LVCMOS
			mmc1_dat0	1	I/O								
			gpio1_0	7	I/O								
V9	V7	GPMC_AD1	gpmc_ad1	0	I/O	L	L	7	VDDSHV1 / VDDSHV1	Yes	6	PU/PD	LVCMOS
			mmc1_dat1	1	I/O								
			gpio1_1	7	I/O								

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
V12	R8	GPMC_AD2	gpmc_ad2	0	I/O	L	L	7	VDDSHV1 / VDDSHV1	Yes	6	PU/PD	LVCMOS
			mmc1_dat2	1	I/O								
			gpio1_2	7	I/O								
W13	T8	GPMC_AD3	gpmc_ad3	0	I/O	L	L	7	VDDSHV1 / VDDSHV1	Yes	6	PU/PD	LVCMOS
			mmc1_dat3	1	I/O								
			gpio1_3	7	I/O								
V13	U8	GPMC_AD4	gpmc_ad4	0	I/O	L	L	7	VDDSHV1 / VDDSHV1	Yes	6	PU/PD	LVCMOS
			mmc1_dat4	1	I/O								
			gpio1_4	7	I/O								
W14	V8	GPMC_AD5	gpmc_ad5	0	I/O	L	L	7	VDDSHV1 / VDDSHV1	Yes	6	PU/PD	LVCMOS
			mmc1_dat5	1	I/O								
			gpio1_5	7	I/O								
U14	R9	GPMC_AD6	gpmc_ad6	0	I/O	L	L	7	VDDSHV1 / VDDSHV1	Yes	6	PU/PD	LVCMOS
			mmc1_dat6	1	I/O								
			gpio1_6	7	I/O								
W15	T9	GPMC_AD7	gpmc_ad7	0	I/O	L	L	7	VDDSHV1 / VDDSHV1	Yes	6	PU/PD	LVCMOS
			mmc1_dat7	1	I/O								
			gpio1_7	7	I/O								
V15	U10	GPMC_AD8	gpmc_ad8	0	I/O	L	L	7	VDDSHV1 / VDDSHV2	Yes	6	PU/PD	LVCMOS
			lcd_data23	1	O								
			mmc1_dat0	2	I/O								
			mmc2_dat4	3	I/O								
			ehrpwm2A	4	O								
			pr1_mii_mt0_clk	5	I								
			gpio0_22	7	I/O								
W16	T10	GPMC_AD9	gpmc_ad9	0	I/O	L	L	7	VDDSHV1 / VDDSHV2	Yes	6	PU/PD	LVCMOS
			lcd_data22	1	O								
			mmc1_dat1	2	I/O								
			mmc2_dat5	3	I/O								
			ehrpwm2B	4	O								
			pr1_mii0_col	5	I								
			gpio0_23	7	I/O								

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
T12	T11	GPMC_AD10	gpmc_ad10	0	I/O	L	L	7	VDDSHV1 / VDDSHV2	Yes	6	PU/PD	LVCMOS
			lcd_data21	1	O								
			mmc1_dat2	2	I/O								
			mmc2_dat6	3	I/O								
			ehrpwm2_tripzone_input	4	I								
			pr1_mii0_txen	5	O								
			gpio0_26	7	I/O								
U12	U12	GPMC_AD11	gpmc_ad11	0	I/O	L	L	7	VDDSHV1 / VDDSHV2	Yes	6	PU/PD	LVCMOS
			lcd_data20	1	O								
			mmc1_dat3	2	I/O								
			mmc2_dat7	3	I/O								
			ehrpwm0_synco	4	O								
			pr1_mii0_txd3	5	O								
			gpio0_27	7	I/O								
U13	T12	GPMC_AD12	gpmc_ad12	0	I/O	L	L	7	VDDSHV1 / VDDSHV2	Yes	6	PU/PD	LVCMOS
			lcd_data19	1	O								
			mmc1_dat4	2	I/O								
			mmc2_dat0	3	I/O								
			eQEP2A_in	4	I								
			pr1_mii0_txd2	5	O								
			pr1_pru0_pru_r30_14	6	O								
			gpio1_12	7	I/O								
T13	R12	GPMC_AD13	gpmc_ad13	0	I/O	L	L	7	VDDSHV1 / VDDSHV2	Yes	6	PU/PD	LVCMOS
			lcd_data18	1	O								
			mmc1_dat5	2	I/O								
			mmc2_dat1	3	I/O								
			eQEP2B_in	4	I								
			pr1_mii0_txd1	5	O								
			pr1_pru0_pru_r30_15	6	O								
			gpio1_13	7	I/O								
W17	V13	GPMC_AD14	gpmc_ad14	0	I/O	L	L	7	VDDSHV1 / VDDSHV2	Yes	6	PU/PD	LVCMOS
			lcd_data17	1	O								
			mmc1_dat6	2	I/O								
			mmc2_dat2	3	I/O								
			eQEP2_index	4	I/O								
			pr1_mii0_txd0	5	O								
			pr1_pru0_pru_r31_14	6	I								
			gpio1_14	7	I/O								

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
V17	U13	GPMC_AD15	gpmc_ad15	0	I/O	L	L	7	VDDSHV1 / VDDSHV2	Yes	6	PU/PD	LVCMOS
			lcd_data16	1	O								
			mmc1_dat7	2	I/O								
			mmc2_dat3	3	I/O								
			eQEP2_strobe	4	I/O								
			pr1_ecap0_ecap_capin_apwm_o	5	I/O								
			pr1_pru0_pru_r31_15	6	I								
			gpio1_15	7	I/O								
V10	R7	GPMC_ADVn_ALE	gpmc_advn_ale	0	O	H	H	7	VDDSHV1 / VDDSHV1	Yes	6	PU/PD	LVCMOS
			timer4	2	I/O								
			gpio2_2	7	I/O								
V8	T6	GPMC_BEn0_CLE	gpmc_be0n_cle	0	O	H	H	7	VDDSHV1 / VDDSHV1	Yes	6	PU/PD	LVCMOS
			timer5	2	I/O								
			gpio2_5	7	I/O								
V18	U18	GPMC_BEn1	gpmc_be1n	0	O	H	H	7	VDDSHV1 / VDDSHV3	Yes	6	PU/PD	LVCMOS
			gmii2_col	1	I								
			gpmc_csn6	2	O								
			mmc2_dat3	3	I/O								
			gpmc_dir	4	O								
			pr1_mii1_rxlink	5	I								
			mcasp0_aclkr	6	I/O								
			gpio1_28	7	I/O								
V16	V12	GPMC_CLK	gpmc_clk	0	I/O	L	L	7	VDDSHV1 / VDDSHV2	Yes	6	PU/PD	LVCMOS
			lcd_memory_clk	1	O								
			gpmc_wait1	2	I								
			mmc2_clk	3	I/O								
			pr1_mii1_crs	4	I								
			pr1_mdio_mdclk	5	O								
			mcasp0_fsr	6	I/O								
			gpio2_1	7	I/O								
W8	V6	GPMC_CSn0	gpmc_csn0	0	O	H	H	7	VDDSHV1 / VDDSHV1	Yes	6	PU/PD	LVCMOS
			gpio1_29	7	I/O								

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
V14	U9	GPMC_CSn1	gpmc_csn1	0	O	H	H	7	VDDSHV1 / VDDSHV1	Yes	6	PU/PD	LVCMOS
			gpmc_clk	1	I/O								
			mmc1_clk	2	I/O								
			pr1_edio_data_in6	3	I								
			pr1_edio_data_out6	4	O								
			pr1_pru1_pru_r30_12	5	O								
			pr1_pru1_pru_r31_12	6	I								
			gpio1_30	7	I/O								
U15	V9	GPMC_CSn2	gpmc_csn2	0	O	H	H	7	VDDSHV1 / VDDSHV1	Yes	6	PU/PD	LVCMOS
			gpmc_be1n	1	O								
			mmc1_cmd	2	I/O								
			pr1_edio_data_in7	3	I								
			pr1_edio_data_out7	4	O								
			pr1_pru1_pru_r30_13	5	O								
			pr1_pru1_pru_r31_13	6	I								
			gpio1_31	7	I/O								
U17	T13	GPMC_CSn3	gpmc_csn3	0	O	H	H	7	VDDSHV1 / VDDSHV2	Yes	6	PU/PD	LVCMOS
			mmc2_cmd	3	I/O								
			pr1_mii0_crs	4	I								
			pr1_mdio_data	5	I/O								
			EMU4	6	I/O								
			gpio2_0	7	I/O								
W9	T7	GPMC_OEn_REn	gpmc_oen_ren	0	O	H	H	7	VDDSHV1 / VDDSHV1	Yes	6	PU/PD	LVCMOS
			timer7	2	I/O								
			gpio2_3	7	I/O								
R15	T17	GPMC_WAIT0	gpmc_wait0	0	I	H	H	7	VDDSHV1 / VDDSHV3	Yes	6	PU/PD	LVCMOS
			gmii2_crs	1	I								
			gpmc_csn4	2	O								
			rmii2_crs_dv	3	I								
			mmc1_sdcd	4	I								
			pr1_mii1_col	5	I								
			uart4_rxd	6	I								
			gpio0_30	7	I/O								
U8	U6	GPMC_WEn	gpmc_wen	0	O	H	H	7	VDDSHV1 / VDDSHV1	Yes	6	PU/PD	LVCMOS
			timer6	2	I/O								
			gpio2_4	7	I/O								

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
W18	U17	GPMC_WPn	gpmc_wpn	0	O	H	H	7	VDDSHV1 / VDDSHV3	Yes	6	PU/PD	LVCMOS
			gmii2_rxerr	1	I								
			gpmc_csn5	2	O								
			rmii2_rxerr	3	I								
			mmc2_sdcd	4	I								
			pr1_mii1_txen	5	O								
			uart4_txd	6	O								
			gpio0_31	7	I/O								
C18	C17	I2C0_SDA	I2C0_SDA	0	I/OD	Z	H	7	VDDSHV6 / VDDSHV6	Yes	4	PU/PD	LVCMOS
			timer4	1	I/O								
			uart2_ctsn	2	I								
			eCAP2_in_PWM2_out	3	I/O								
			gpio3_5	7	I/O								
B19	C16	I2C0_SCL	I2C0_SCL	0	I/OD	Z	H	7	VDDSHV6 / VDDSHV6	Yes	4	PU/PD	LVCMOS
			timer7	1	I/O								
			uart2_rtsn	2	O								
			eCAP1_in_PWM1_out	3	I/O								
			gpio3_6	7	I/O								
W7	R6	LCD_AC_BIAS_EN	lcd_ac_bias_en	0	O	Z	L	7	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			gpmc_a11	1	O								
			pr1_mii1_crs	2	I								
			pr1_edio_data_in5	3	I								
			pr1_edio_data_out5	4	O								
			pr1_pru1_pru_r30_11	5	O								
			pr1_pru1_pru_r31_11	6	I								
			gpio2_25	7	I/O								
U1	R1	LCD_DATA0 (3)	lcd_data0	0	I/O	Z	Z	7	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			gpmc_a0	1	O								
			pr1_mii_mt0_clk	2	I								
			ehrpwm2A	3	O								
			pr1_pru1_pru_r30_0	5	O								
			pr1_pru1_pru_r31_0	6	I								
			gpio2_6	7	I/O								

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
U2	R2	LCD_DATA1 (3)	lcd_data1	0	I/O	Z	Z	7	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			gpmc_a1	1	O								
			pr1_mii0_txen	2	O								
			ehrpwm2B	3	O								
			pr1_pru1_pru_r30_1	5	O								
			pr1_pru1_pru_r31_1	6	I								
			gpio2_7	7	I/O								
V1	R3	LCD_DATA2 (3)	lcd_data2	0	I/O	Z	Z	7	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			gpmc_a2	1	O								
			pr1_mii0_txd3	2	O								
			ehrpwm2_tripzone_input	3	I								
			pr1_pru1_pru_r30_2	5	O								
			pr1_pru1_pru_r31_2	6	I								
			gpio2_8	7	I/O								
V2	R4	LCD_DATA3 (3)	lcd_data3	0	I/O	Z	Z	7	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			gpmc_a3	1	O								
			pr1_mii0_txd2	2	O								
			ehrpwm0_synco	3	O								
			pr1_pru1_pru_r30_3	5	O								
			pr1_pru1_pru_r31_3	6	I								
			gpio2_9	7	I/O								
W2	T1	LCD_DATA4 (3)	lcd_data4	0	I/O	Z	Z	7	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			gpmc_a4	1	O								
			pr1_mii0_txd1	2	O								
			eQEP2A_in	3	I								
			pr1_pru1_pru_r30_4	5	O								
			pr1_pru1_pru_r31_4	6	I								
			gpio2_10	7	I/O								
W3	T2	LCD_DATA5 (3)	lcd_data5	0	I/O	Z	Z	7	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			gpmc_a5	1	O								
			pr1_mii0_txd0	2	O								
			eQEP2B_in	3	I								
			pr1_pru1_pru_r30_5	5	O								
			pr1_pru1_pru_r31_5	6	I								
			gpio2_11	7	I/O								

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
V3	T3	LCD_DATA6 (3)	lcd_data6	0	I/O	Z	Z	7	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			gpmc_a6	1	O								
			pr1_edio_data_in6	2	I								
			eQEP2_index	3	I/O								
			pr1_edio_data_out6	4	O								
			pr1_pru1_pru_r30_6	5	O								
			pr1_pru1_pru_r31_6	6	I								
			gpio2_12	7	I/O								
U3	T4	LCD_DATA7 (3)	lcd_data7	0	I/O	Z	Z	7	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			gpmc_a7	1	O								
			pr1_edio_data_in7	2	I								
			eQEP2_strobe	3	I/O								
			pr1_edio_data_out7	4	O								
			pr1_pru1_pru_r30_7	5	O								
			pr1_pru1_pru_r31_7	6	I								
			gpio2_13	7	I/O								
V4	U1	LCD_DATA8 (3)	lcd_data8	0	I/O	Z	Z	7	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			gpmc_a12	1	O								
			ehrpwm1_tripzone_input	2	I								
			mcasp0_aclkx	3	I/O								
			uart5_txd	4	O								
			pr1_mii0_rxd3	5	I								
			uart2_ctsn	6	I								
			gpio2_14	7	I/O								
W4	U2	LCD_DATA9 (3)	lcd_data9	0	I/O	Z	Z	7	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			gpmc_a13	1	O								
			ehrpwm0_synco	2	O								
			mcasp0_fsx	3	I/O								
			uart5_rxd	4	I								
			pr1_mii0_rxd2	5	I								
			uart2_rtsn	6	O								
			gpio2_15	7	I/O								

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
U5	U3	LCD_DATA10 (3)	lcd_data10	0	I/O	Z	Z	7	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			gpmc_a14	1	O								
			ehrpwm1A	2	O								
			mcasp0_axr0	3	I/O								
			pr1_mii0_rxd1	5	I								
			uart3_ctsn	6	I								
			gpio2_16	7	I/O								
V5	U4	LCD_DATA11 (3)	lcd_data11	0	I/O	Z	Z	7	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			gpmc_a15	1	O								
			ehrpwm1B	2	O								
			mcasp0_ahclkr	3	I/O								
			mcasp0_axr2	4	I/O								
			pr1_mii0_rxd0	5	I								
			uart3_rtsn	6	O								
			gpio2_17	7	I/O								
V6	V2	LCD_DATA12 (3)	lcd_data12	0	I/O	Z	Z	7	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			gpmc_a16	1	O								
			eQEP1A_in	2	I								
			mcasp0_aclkr	3	I/O								
			mcasp0_axr2	4	I/O								
			pr1_mii0_rxlink	5	I								
			uart4_ctsn	6	I								
			gpio0_8	7	I/O								
U6	V3	LCD_DATA13 (3)	lcd_data13	0	I/O	Z	Z	7	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			gpmc_a17	1	O								
			eQEP1B_in	2	I								
			mcasp0_fsr	3	I/O								
			mcasp0_axr3	4	I/O								
			pr1_mii0_rxer	5	I								
			uart4_rtsn	6	O								
			gpio0_9	7	I/O								

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
W6	V4	LCD_DATA14 (3)	lcd_data14	0	I/O	Z	Z	7	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			gpmc_a18	1	O								
			eQEP1_index	2	I/O								
			mcasp0_axr1	3	I/O								
			uart5_rxd	4	I								
			pr1_mii_mr0_clk	5	I								
			uart5_ctsn	6	I								
			gpio0_10	7	I/O								
V7	T5	LCD_DATA15 (3)	lcd_data15	0	I/O	Z	Z	7	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			gpmc_a19	1	O								
			eQEP1_strobe	2	I/O								
			mcasp0_ahclkx	3	I/O								
			mcasp0_axr3	4	I/O								
			pr1_mii0_rxdv	5	I								
			uart5_rtsn	6	O								
			gpio0_11	7	I/O								
T7	R5	LCD_HSYNC	lcd_hsync	0	O	Z	L	7	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			gpmc_a9	1	O								
			pr1_edio_data_in3	3	I								
			pr1_edio_data_out3	4	O								
			pr1_pru1_pru_r30_9	5	O								
			pr1_pru1_pru_r31_9	6	I								
			gpio2_23	7	I/O								
W5	V5	LCD_PCLK	lcd_pclk	0	O	Z	L	7	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			gpmc_a10	1	O								
			pr1_mii0_crs	2	I								
			pr1_edio_data_in4	3	I								
			pr1_edio_data_out4	4	O								
			pr1_pru1_pru_r30_10	5	O								
			pr1_pru1_pru_r31_10	6	I								
			gpio2_24	7	I/O								
U7	U5	LCD_VSYNC	lcd_vsync	0	O	Z	L	7	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			gpmc_a8	1	O								
			pr1_edio_data_in2	3	I								
			pr1_edio_data_out2	4	O								
			pr1_pru1_pru_r30_8	5	O								
			pr1_pru1_pru_r31_8	6	I								
			gpio2_22	7	I/O								

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
NA	B13	MCASP0_FSX	mcasp0_fsx	0	I/O	L	L	7	NA / VDDSHV6	Yes	6	PU/PD	LVCMOS
			ehrpwm0B	1	O								
			spi1_d0	3	I/O								
			mmc1_sdcd	4	I								
			pr1_pru0_pru_r30_1	5	O								
			pr1_pru0_pru_r31_1	6	I								
			gpio3_15	7	I/O								
NA	B12	MCASP0_ACLKR	mcasp0_aclkr	0	I/O	L	L	7	NA / VDDSHV6	Yes	6	PU/PD	LVCMOS
			eQEP0A_in	1	I								
			mcasp0_axr2	2	I/O								
			mcasp1_aclkx	3	I/O								
			mmc0_sdwp	4	I								
			pr1_pru0_pru_r30_4	5	O								
			pr1_pru0_pru_r31_4	6	I								
			gpio3_18	7	I/O								
NA	C12	MCASP0_AHCLKR	mcasp0_ahclkr	0	I/O	L	L	7	NA / VDDSHV6	Yes	6	PU/PD	LVCMOS
			ehrpwm0_synci	1	I								
			mcasp0_axr2	2	I/O								
			spi1_cs0	3	I/O								
			eCAP2_in_PWM2_out	4	I/O								
			pr1_pru0_pru_r30_3	5	O								
			pr1_pru0_pru_r31_3	6	I								
			gpio3_17	7	I/O								
NA	A14	MCASP0_AHCLKX	mcasp0_ahclkx	0	I/O	L	L	7	NA / VDDSHV6	Yes	6	PU/PD	LVCMOS
			eQEP0_strobe	1	I/O								
			mcasp0_axr3	2	I/O								
			mcasp1_axr1	3	I/O								
			EMU4	4	I/O								
			pr1_pru0_pru_r30_7	5	O								
			pr1_pru0_pru_r31_7	6	I								
			gpio3_21	7	I/O								
NA	A13	MCASP0_ACLKX	mcasp0_aclkx	0	I/O	L	L	7	NA / VDDSHV6	Yes	6	PU/PD	LVCMOS
			ehrpwm0A	1	O								
			spi1_sclk	3	I/O								
			mmc0_sdcd	4	I								
			pr1_pru0_pru_r30_0	5	O								
			pr1_pru0_pru_r31_0	6	I								
			gpio3_14	7	I/O								

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
NA	C13	MCASP0_FSR	mcasp0_fsr	0	I/O	L	L	7	NA / VDDSHV6	Yes	6	PU/PD	LVCMOS
			eQEP0B_in	1	I								
			mcasp0_axr3	2	I/O								
			mcasp1_fsx	3	I/O								
			EMU2	4	I/O								
			pr1_pru0_pru_r30_5	5	O								
			pr1_pru0_pru_r31_5	6	I								
			gpio3_19	7	I/O								
NA	D12	MCASP0_AXR0	mcasp0_axr0	0	I/O	L	L	7	NA / VDDSHV6	Yes	6	PU/PD	LVCMOS
			ehrpwm0_tripzone_input	1	I								
			spi1_d1	3	I/O								
			mmc2_sdcd	4	I								
			pr1_pru0_pru_r30_2	5	O								
			pr1_pru0_pru_r31_2	6	I								
			gpio3_16	7	I/O								
NA	D13	MCASP0_AXR1	mcasp0_axr1	0	I/O	L	L	7	NA / VDDSHV6	Yes	6	PU/PD	LVCMOS
			eQEP0_index	1	I/O								
			mcasp1_axr0	3	I/O								
			EMU3	4	I/O								
			pr1_pru0_pru_r30_6	5	O								
			pr1_pru0_pru_r31_6	6	I								
			gpio3_20	7	I/O								
R19	M18	MDC	mdio_clk	0	O	H	H	7	VDDSHV5 / VDDSHV5	Yes	6	PU/PD	LVCMOS
			timer5	1	I/O								
			uart5_txd	2	O								
			uart3_rtsn	3	O								
			mmc0_sdwp	4	I								
			mmc1_clk	5	I/O								
			mmc2_clk	6	I/O								
			gpio0_1	7	I/O								
P17	M17	MDIO	mdio_data	0	I/O	H	H	7	VDDSHV5 / VDDSHV5	Yes	6	PU/PD	LVCMOS
			timer6	1	I/O								
			uart5_rxd	2	O								
			uart3_ctsn	3	I								
			mmc0_sdcd	4	I								
			mmc1_cmd	5	I/O								
			mmc2_cmd	6	I/O								
			gpio0_0	7	I/O								

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
L19	J17	MII1_RX_DV	gmii1_rxdv	0	I	L	L	7	VDDSHV5 / VDDSHV5	Yes	6	PU/PD	LVCMOS
			lcd_memory_clk	1	O								
			rgmii1_rctl	2	I								
			uart5_txd	3	O								
			mcasp1_aclkx	4	I/O								
			mmc2_dat0	5	I/O								
			mcasp0_aclkr	6	I/O								
			gpio3_4	7	I/O								
K17	J16	MII1_TX_EN	gmii1_txen	0	O	L	L	7	VDDSHV5 / VDDSHV5	Yes	6	PU/PD	LVCMOS
			rmii1_txen	1	O								
			rgmii1_tctl	2	O								
			timer4	3	I/O								
			mcasp1_axr0	4	I/O								
			eQEP0_index	5	I/O								
			mmc2_cmd	6	I/O								
			gpio3_3	7	I/O								
K19	J15	MII1_RX_ER	gmii1_rxerr	0	I	L	L	7	VDDSHV5 / VDDSHV5	Yes	6	PU/PD	LVCMOS
			rmii1_rxerr	1	I								
			spi1_d1	2	I/O								
			I2C1_SCL	3	I/OD								
			mcasp1_fsx	4	I/O								
			uart5_rtsn	5	O								
			uart2_txd	6	O								
			gpio3_2	7	I/O								
M19	L18	MII1_RX_CLK	gmii1_rxclk	0	I	L	L	7	VDDSHV5 / VDDSHV5	Yes	6	PU/PD	LVCMOS
			uart2_txd	1	O								
			rgmii1_rclk	2	I								
			mmc0_dat6	3	I/O								
			mmc1_dat1	4	I/O								
			uart1_dsrn	5	I								
			mcasp0_fsx	6	I/O								
			gpio3_10	7	I/O								

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
N19	K18	MII1_TX_CLK	gmii1_txclk	0	I	L	L	7	VDDSHV5 / VDDSHV5	Yes	6	PU/PD	LVCMOS
			uart2_rxd	1	I								
			rgmii1_tclk	2	O								
			mmc0_dat7	3	I/O								
			mmc1_dat0	4	I/O								
			uart1_dcdn	5	I								
			mcasp0_aclkx	6	I/O								
			gpio3_9	7	I/O								
J19	H16	MII1_COL	gmii1_col	0	I	L	L	7	VDDSHV5 / VDDSHV5	Yes	6	PU/PD	LVCMOS
			rmii2_refclk	1	I/O								
			spi1_sclk	2	I/O								
			uart5_rxd	3	I								
			mcasp1_axr2	4	I/O								
			mmc2_dat3	5	I/O								
			mcasp0_axr2	6	I/O								
			gpio3_0	7	I/O								
J18	H17	MII1_CRS	gmii1_crs	0	I	L	L	7	VDDSHV5 / VDDSHV5	Yes	6	PU/PD	LVCMOS
			rmii1_crs_dv	1	I								
			spi1_d0	2	I/O								
			I2C1_SDA	3	I/OD								
			mcasp1_aclkx	4	I/O								
			uart5_ctsn	5	I								
			uart2_rxd	6	I								
			gpio3_1	7	I/O								
P18	M16	MII1_RXD0	gmii1_rxd0	0	I	L	L	7	VDDSHV5 / VDDSHV5	Yes	6	PU/PD	LVCMOS
			rmii1_rxd0	1	I								
			rgmii1_rd0	2	I								
			mcasp1_ahclkx	3	I/O								
			mcasp1_ahclkr	4	I/O								
			mcasp1_aclkr	5	I/O								
			mcasp0_axr3	6	I/O								
			gpio2_21	7	I/O								

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
P19	L15	MII1_RXD1	gmii1_rxd1	0	I	L	L	7	VDDSHV5 / VDDSHV5	Yes	6	PU/PD	LVCMOS
			rmii1_rxd1	1	I								
			rgmii1_rd1	2	I								
			mcasp1_axr3	3	I/O								
			mcasp1_fsr	4	I/O								
			eQEP0_strobe	5	I/O								
			mmc2_clk	6	I/O								
			gpio2_20	7	I/O								
N16	L16	MII1_RXD2	gmii1_rxd2	0	I	L	L	7	VDDSHV5 / VDDSHV5	Yes	6	PU/PD	LVCMOS
			uart3_txd	1	O								
			rgmii1_rd2	2	I								
			mmc0_dat4	3	I/O								
			mmc1_dat3	4	I/O								
			uart1_rin	5	I								
			mcasp0_axr1	6	I/O								
			gpio2_19	7	I/O								
N17	L17	MII1_RXD3	gmii1_rxd3	0	I	L	L	7	VDDSHV5 / VDDSHV5	Yes	6	PU/PD	LVCMOS
			uart3_rxd	1	I								
			rgmii1_rd3	2	I								
			mmc0_dat5	3	I/O								
			mmc1_dat2	4	I/O								
			uart1_dtrn	5	O								
			mcasp0_axr0	6	I/O								
			gpio2_18	7	I/O								
L18	K17	MII1_TXD0	gmii1_txd0	0	O	L	L	7	VDDSHV5 / VDDSHV5	Yes	6	PU/PD	LVCMOS
			rmii1_txd0	1	O								
			rgmii1_td0	2	O								
			mcasp1_axr2	3	I/O								
			mcasp1_aclkr	4	I/O								
			eQEP0B_in	5	I								
			mmc1_clk	6	I/O								
			gpio0_28	7	I/O								

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
M18	K16	MII1_TXD1	gmii1_txd1	0	O	L	L	7	VDDSHV5 / VDDSHV5	Yes	6	PU/PD	LVCMOS
			rmii1_txd1	1	O								
			rgmii1_td1	2	O								
			mcasp1_fsr	3	I/O								
			mcasp1_axr1	4	I/O								
			eQEP0A_in	5	I								
			mmc1_cmd	6	I/O								
			gpio0_21	7	I/O								
N18	K15	MII1_TXD2	gmii1_txd2	0	O	L	L	7	VDDSHV5 / VDDSHV5	Yes	6	PU/PD	LVCMOS
			dcan0_rx	1	I								
			rgmii1_td2	2	O								
			uart4_txd	3	O								
			mcasp1_axr0	4	I/O								
			mmc2_dat2	5	I/O								
			mcasp0_ahclkx	6	I/O								
			gpio0_17	7	I/O								
M17	J18	MII1_TXD3	gmii1_txd3	0	O	L	L	7	VDDSHV5 / VDDSHV5	Yes	6	PU/PD	LVCMOS
			dcan0_tx	1	O								
			rgmii1_td3	2	O								
			uart4_rxd	3	I								
			mcasp1_fsx	4	I/O								
			mmc2_dat1	5	I/O								
			mcasp0_fsr	6	I/O								
			gpio0_16	7	I/O								
G17	G18	MMC0_CMD	mmc0_cmd	0	I/O	H	H	7	VDDSHV4 / VDDSHV4	Yes	6	PU/PD	LVCMOS
			gpmc_a25	1	O								
			uart3_rtsn	2	O								
			uart2_txd	3	O								
			dcan1_rx	4	I								
			pr1_pru0_pru_r30_13	5	O								
			pr1_pru0_pru_r31_13	6	I								
			gpio2_31	7	I/O								

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
G19	G17	MMC0_CLK	mmc0_clk	0	I/O	H	H	7	VDDSHV4 / VDDSHV4	Yes	6	PU/PD	LVCMOS
			gpmc_a24	1	O								
			uart3_ctsn	2	I								
			uart2_rxd	3	I								
			dcan1_tx	4	O								
			pr1_pru0_pru_r30_12	5	O								
			pr1_pru0_pru_r31_12	6	I								
			gpio2_30	7	I/O								
G18	G16	MMC0_DAT0	mmc0_dat0	0	I/O	H	H	7	VDDSHV4 / VDDSHV4	Yes	6	PU/PD	LVCMOS
			gpmc_a23	1	O								
			uart5_rtsn	2	O								
			uart3_txd	3	O								
			uart1_rin	4	I								
			pr1_pru0_pru_r30_11	5	O								
			pr1_pru0_pru_r31_11	6	I								
			gpio2_29	7	I/O								
H17	G15	MMC0_DAT1	mmc0_dat1	0	I/O	H	H	7	VDDSHV4 / VDDSHV4	Yes	6	PU/PD	LVCMOS
			gpmc_a22	1	O								
			uart5_ctsn	2	I								
			uart3_rxd	3	I								
			uart1_dtrn	4	O								
			pr1_pru0_pru_r30_10	5	O								
			pr1_pru0_pru_r31_10	6	I								
			gpio2_28	7	I/O								
H18	F18	MMC0_DAT2	mmc0_dat2	0	I/O	H	H	7	VDDSHV4 / VDDSHV4	Yes	6	PU/PD	LVCMOS
			gpmc_a21	1	O								
			uart4_rtsn	2	O								
			timer6	3	I/O								
			uart1_dsrn	4	I								
			pr1_pru0_pru_r30_9	5	O								
			pr1_pru0_pru_r31_9	6	I								
			gpio2_27	7	I/O								

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
H19	F17	MMC0_DAT3	mmc0_dat3	0	I/O	H	H	7	VDDSHV4 / VDDSHV4	Yes	6	PU/PD	LVCMOS
			gpmc_a20	1	O								
			uart4_ctsn	2	I								
			timer5	3	I/O								
			uart1_dcdn	4	I								
			pr1_pru0_pru_r30_8	5	O								
			pr1_pru0_pru_r31_8	6	I								
			gpio2_26	7	I/O								
C7	C6	PMIC_POWER_EN	PMIC_POWER_EN	0	O	H	1	0	VDDS_RTC / VDDS_RTC	NA	6	NA	LVCMOS
E15	B15	PWRONRSTn	porz	0	I	Z	Z	0	VDDSHV6 / VDDSHV6	Yes	NA	NA	LVCMOS
B6	A3	RESERVED	testout	0	O	NA	NA	NA	VDDSHV6 / VDDSHV6	NA	NA	NA	Analog
K18	H18	RMII1_REF_CLK	rmii1_refclk	0	I/O	L	L	7	VDDSHV5 / VDDSHV5	Yes	6	PU/PD	LVCMOS
			xdma_event_intr2	1	I								
			spi1_cs0	2	I/O								
			uart5_txd	3	O								
			mcasp1_axr3	4	I/O								
			mmc0_pow	5	O								
			mcasp1_ahclkx	6	I/O								
			gpio0_29	7	I/O								
A7	B4	RTC_KALDO_ENn	ENZ_KALDO_1P8V	0	I	Z	Z	0	VDDS_RTC / VDDS_RTC	NA	NA	NA	TBD
B7	B5	RTC_PWRONRSTn	RTC_porz	0	I	Z	Z	0	VDDS_RTC / VDDS_RTC	Yes	NA	NA	LVCMOS
A6	A6	RTC_XTALIN	OSC1_IN	0	I	Z	Z	0	VDDS_RTC / VDDS_RTC	Yes	NA	NA (2)	LVCMOS
A5	A4	RTC_XTALOUT	OSC1_OUT	0	O	Z (14)	Z	0	VDDS_RTC / VDDS_RTC	NA	TBD	NA	LVCMOS
A18	A17	SPI0_SCLK	spi0_sclk	0	I/O	Z	H	7	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			uart2_rxd	1	I								
			I2C2_SDA	2	I/OD								
			ehrpwm0A	3	O								
			pr1_uart0_cts_n	4	I								
			pr1_edio_sof	5	O								
			EMU2	6	I/O								
			gpio0_2	7	I/O								

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
A17	A16	SPI0_CS0	spi0_cs0	0	I/O	Z	H	7	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			mmc2_sdwp	1	I								
			I2C1_SCL	2	I/OD								
			ehrpwm0_synci	3	I								
			pr1_uart0_txd	4	O								
			pr1_edio_data_in1	5	I								
			pr1_edio_data_out1	6	O								
			gpio0_5	7	I/O								
B16	C15	SPI0_CS1	spi0_cs1	0	I/O	Z	H	7	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			uart3_rxd	1	I								
			eCAP1_in_PWM1_out	2	I/O								
			mmc0_pow	3	O								
			xdma_event_intr2	4	I								
			mmc0_sdcd	5	I								
			EMU4	6	I/O								
			gpio0_6	7	I/O								
B18	B17	SPI0_D0	spi0_d0	0	I/O	Z	H	7	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			uart2_txd	1	O								
			I2C2_SCL	2	I/OD								
			ehrpwm0B	3	O								
			pr1_uart0_rts_n	4	O								
			pr1_edio_latch_in	5	I								
			EMU3	6	I/O								
			gpio0_3	7	I/O								
B17	B16	SPI0_D1	spi0_d1	0	I/O	Z	H	7	VDDSHV6 / VDDSHV6	Yes	6	PU/PD	LVCMOS
			mmc1_sdwp	1	I								
			I2C1_SDA	2	I/OD								
			ehrpwm0_tripzone_input	3	I								
			pr1_uart0_rxd	4	I								
			pr1_edio_data_in0	5	I								
			pr1_edio_data_out0	6	O								
			gpio0_4	7	I/O								
B14	A12	TCK	TCK	0	I	H	H	0	VDDSHV6 / VDDSHV6	Yes	NA	PU/PD	LVCMOS
B13	B11	TDI	TDI	0	I	H	H	0	VDDSHV6 / VDDSHV6	Yes	NA	PU/PD	LVCMOS
A14	A11	TDO	TDO	0	O	H	H	0	VDDSHV6 / VDDSHV6	NA	4	PU/PD	LVCMOS
C14	C11	TMS	TMS	0	I	H	H	0	VDDSHV6 / VDDSHV6	Yes	NA	PU/PD	LVCMOS

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
A13	B10	TRSTn	nTRST	0	I	L	L	0	VDDSHV6 / VDDSHV6	Yes	NA	PU/PD	LVCMOS
F17	E16	UART0_TXD	uart0_txd	0	O	Z	H	7	VDDSHV6 / VDDSHV6	Yes	4	PU/PD	LVCMOS
			spi1_cs1	1	I/O								
			dcan0_rx	2	I								
			I2C2_SCL	3	I/OD								
			eCAP1_in_PWM1_out	4	I/O								
			pr1_pru1_pru_r30_15	5	O								
			pr1_pru1_pru_r31_15	6	I								
			gpio1_11	7	I/O								
F19	E18	UART0_CTSn	uart0_ctsn	0	I	Z	H	7	VDDSHV6 / VDDSHV6	Yes	4	PU/PD	LVCMOS
			uart4_rxd	1	I								
			dcan1_tx	2	O								
			I2C1_SDA	3	I/OD								
			spi1_d0	4	I/O								
			timer7	5	I/O								
			pr1_edc_sync0_out	6	O								
			gpio1_8	7	I/O								
E19	E15	UART0_RXD	uart0_rxd	0	I	Z	H	7	VDDSHV6 / VDDSHV6	Yes	4	PU/PD	LVCMOS
			spi1_cs0	1	I/O								
			dcan0_tx	2	O								
			I2C2_SDA	3	I/OD								
			eCAP2_in_PWM2_out	4	I/O								
			pr1_pru1_pru_r30_14	5	O								
			pr1_pru1_pru_r31_14	6	I								
			gpio1_10	7	I/O								
F18	E17	UART0_RTSn	uart0_rtsn	0	O	Z	H	7	VDDSHV6 / VDDSHV6	Yes	4	PU/PD	LVCMOS
			uart4_txd	1	O								
			dcan1_rx	2	I								
			I2C1_SCL	3	I/OD								
			spi1_d1	4	I/O								
			spi1_cs0	5	I/O								
			pr1_edc_sync1_out	6	O								
			gpio1_9	7	I/O								

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
C19	D15	UART1_TXD	uart1_txd	0	O	Z	H	7	VDDSHV6 / VDDSHV6	Yes	4	PU/PD	LVCMOS
			mmc2_sdwp	1	I								
			dcan1_rx	2	I								
			I2C1_SCL	3	I/OD								
			pr1_uart0_txd	5	O								
			pr1_pru0_pru_r31_16	6	I								
			gpio0_15	7	I/O								
D18	D16	UART1_RXD	uart1_rxd	0	I	Z	H	7	VDDSHV6 / VDDSHV6	Yes	4	PU/PD	LVCMOS
			mmc1_sdwp	1	I								
			dcan1_tx	2	O								
			I2C1_SDA	3	I/OD								
			pr1_uart0_rxd	5	I								
			pr1_pru1_pru_r31_16	6	I								
			gpio0_14	7	I/O								
D19	D17	UART1_RTSn	uart1_rtsn	0	O	Z	H	7	VDDSHV6 / VDDSHV6	Yes	4	PU/PD	LVCMOS
			timer5	1	I/O								
			dcan0_rx	2	I								
			I2C2_SCL	3	I/OD								
			spi1_cs1	4	I/O								
			pr1_uart0_rts_n	5	O								
			pr1_edc_latch1_in	6	I								
			gpio0_13	7	I/O								
E17	D18	UART1_CTSn	uart1_ctsn	0	I	Z	H	7	VDDSHV6 / VDDSHV6	Yes	4	PU/PD	LVCMOS
			timer6	1	I/O								
			dcan0_tx	2	O								
			I2C2_SDA	3	I/OD								
			spi1_cs0	4	I/O								
			pr1_uart0_cts_n	5	I								
			pr1_edc_latch0_in	6	I								
			gpio0_12	7	I/O								
T18	M15	USB0_CE	USB0_CE	0	A	Z	Z	0	VDDA*_USB0 / VDDA*_USB0 (16)	TBD	TBD	TBD	Analog
T19	P15	USB0_VBUS	USB0_VBUS	0	A	Z	Z	0	VDDA*_USB0 / VDDA*_USB0 (16)	TBD	TBD	TBD	Analog
U18	N18	USB0_DM	USB0_DM	0	A	Z	Z	0 (5)	VDDA*_USB0 / VDDA*_USB0	TBD	TBD	TBD	Analog
G16	F16	USB0_DRVVBUS	USB0_DRVVBUS	0	O	L	0(PD)	0	VDDSHV6 / VDDSHV6	Yes	4	PU/PD	LVCMOS
			gpio0_18	7	I/O								

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
V19	P16	USB0_ID	USB0_ID	0	A	Z	Z	0	VDDA*_USB0 / VDDA*_USB0 (16)	TBD	TBD	TBD	Analog
U19	N17	USB0_DP	USB0_DP	0	A	Z	Z	0 (5)	VDDA*_USB0 / VDDA*_USB0	TBD	TBD	TBD	Analog
NA	P18	USB1_CE	USB1_CE	0	A	Z	Z	0	NA / VDDA*_USB1 (17)	TBD	TBD	TBD	Analog
NA	P17	USB1_ID	USB1_ID	0	A	Z	Z	0	NA / VDDA*_USB1 (17)	TBD	TBD	TBD	Analog
NA	T18	USB1_VBUS	USB1_VBUS	0	A	Z	Z	0	NA / VDDA*_USB1 (17)	TBD	TBD	TBD	Analog
NA	R17	USB1_DP	USB1_DP	0	A	Z	Z	0 (6)	NA / VDDA*_USB1	TBD	TBD	TBD	Analog
NA	F15	USB1_DRVVBUS	USB1_DRVVBUS	0	O	L	0(PD)	0	NA / VDDSHV6	Yes	4	PU/PD	LVCMOS
			gpio3_13	7	I/O								
NA	R18	USB1_DM	USB1_DM	0	A	Z	Z	0 (6)	NA / VDDA*_USB1	TBD	TBD	TBD	Analog
R17	N16	VDDA1P8V_USB0	VDDA1P8V_USB0	NA	PWR								
NA	R16	VDDA1P8V_USB1	VDDA1P8V_USB1	NA	PWR								
R18	N15	VDDA3P3V_USB0	VDDA3P3V_USB0	NA	PWR								
NA	R15	VDDA3P3V_USB1	VDDA3P3V_USB1	NA	PWR								
D7	D8	VDDA_ADC	VDDA_ADC	NA	PWR								
D12, F16, M16, T6, T14	E6, E14, F9, K13, N6, P9, P14	VDDS	VDDS	NA	PWR								
R8, R9, R11, R12, R13	P7, P8	VDDSHV1	VDDSHV1	NA	PWR								
NA	P10, P11	VDDSHV2	VDDSHV2	NA	PWR								
NA	P12, P13	VDDSHV3	VDDSHV3	NA	PWR								
G15, H14, H15	H14, J14	VDDSHV4	VDDSHV4	NA	PWR								
M14, M15, N15	K14, L14	VDDSHV5	VDDSHV5	NA	PWR								
E11, E12, E13, F14, P6, R7	E10, E11, E12, E13, F14, G14, N5, P5, P6	VDDSHV6	VDDSHV6	NA	PWR								
G5, H5, H6, K4, K5, M5, M6, N5	E5, F5, G5, H5, J5, K5, L5	VDDS_DDR	VDDS_DDR	NA	PWR								
U10	R11	VDDS_OSC	VDDS_OSC	NA	PWR								
T8	R10	VDDS_PLL_CORE_LCD	VDDS_PLL_CORE_LCD	NA	PWR								
C5	E7	VDDS_PLL_DDR	VDDS_PLL_DDR	NA	PWR								

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
H16	H15	VDDS_PLL_MPU	VDDS_PLL_MPU	NA	PWR								
C6	D7	VDDS_RTC	VDDS_RTC	NA	PWR								
C10	E9	VDDS_SRAM_CORE_BG	VDDS_SRAM_CORE_BG	NA	PWR								
C12	D10	VDDS_SRAM_MPU_BB	VDDS_SRAM_MPU_BB	NA	PWR								
F9, F11, G9, G11, H7, H8, H12, H13, J7, J8, J12, J13, K15, K16, L7, L8, L12, L13, M7, M8, M12, M13, N9, N11, P9, P11	F6, F7, G6, G7, G10, H11, J12, K6, K8, K12, L6, L7, L8, L9, M11, M13, N8, N9, N12, N13	VDD_CORE	VDD_CORE	NA	PWR								
NA	F10, F11, F12, F13, G13, H13, J13	VDD_MPU	VDD_MPU	NA	PWR								
NA	A2	VDD_MPU_MON	VDD_MPU_MON	NA									
R5	M5	VPP	VPP	NA	PWR								
B9	A9	VREFN	VREFN	0	AP	Z	Z	0	VDDA_ADC / VDDA_ADC	NA	NA	NA	Analog
A9	B9	VREFP	VREFP	0	AP	Z	Z	0	VDDA_ADC / VDDA_ADC	NA	NA	NA	Analog
A1, A19, D10, E7, E8, E9, E10, F6, F7, F8, F12, F13, G8, G12, H9, H10, H11, J5, J6, J9, J11, J14, J15, K8, K9, K11, K12, L5, L6, L9, L11, L14, L15, M9, M10, M11, N8, N12, P7, P8, P12, P13, P14, R10, T10, W1, W19	A1, A18, F8, G8, G9, G11, G12, H6, H7, H8, H9, H10, H12, J6, J7, J8, J9, J10, J11, K7, K9, K10, K11, L10, L11, L12, L13, M6, M7, M8, M9, M10, M12, N7, N10, N11, V1, V18	VSS	VSS	NA	GND								
D8	E8	VSSA_ADC	VSSA_ADC	NA	GND								
P16	M14, N14	VSSA_USB	VSSA_USB	NA	GND								
V11	V11	VSS_OSC	VSS_OSC	NA	A								
NA	A5	VSS_RTC	VSS_RTC	NA	GND								
A16	A10	WARMRSTn	nRESETIN_OUT	0	I/OD	0	0	0	VDDSHV6 / VDDSHV6	Yes	4	PU/PD	LVCMOS

Table 2-7. Ball Characteristics (ZCE and ZCZ Packages) (continued)

ZCE BALL NUMBER [1]	ZCZ BALL NUMBER [1]	PIN NAME [2]	SIGNAL NAME [3]	MODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. STATE [7]	RESET REL. MODE [8]	ZCE POWER / ZCZ POWER [9]	HYS [10]	BUFFER STRENGTH (mA) [11]	PULLUP /DOWN TYPE [12]	I/O CELL [13]
C15	A15	XDMA_EVENT_INTR0	xdma_event_intr0	0	I	Z (8)	(7)	(4)	VDDSHV6 / VDDSHV6	Yes	4	PU/PD	LVCMOS
			timer4	2	I/O								
			clkout1	3	O								
			spi1_cs1	4	I/O								
			pr1_pru1_pru_r31_16	5	I								
			EMU2	6	I/O								
			gpio0_19	7	I/O								
B15	D14	XDMA_EVENT_INTR1	xdma_event_intr1	0	I	Z	L	7	VDDSHV6 / VDDSHV6	Yes	4	PU/PD	LVCMOS
			tclkin	2	I								
			clkout2	3	O								
			timer7	4	I/O								
			pr1_pru0_pru_r31_16	5	I								
			EMU3	6	I/O								
			gpio0_20	7	I/O								
W11	V10	XTALIN	OSC0_IN	0	I	Z	Z	0	VDDS_OSC / VDDS_OSC	Yes	NA	PD (1)	LVCMOS
W12	U11	XTALOUT	OSC0_OUT	0	O	(15)		0	VDDS_OSC / VDDS_OSC	NA	TBD	NA	LVCMOS

(1) A internal 200 ohm pull down is turned on when the oscillator is disabled. The oscillator is enabled by default after power is applied.

(2) An external pull-down resistor should be connected to this terminal to minmize leakage current when not using the oscillator.

(3) LCD_DATA[15:0] terminals are respectively SYSBOOT[15:0] inputs, latched on the rising edge of PWRONRSTn.

(4) Reset Release Mode = 7 if sysboot[5] is low. Mode = 3 if sysboot[5] is high.

(5) The internal USB PHY can be configured to multiplex the UART2_TX or UART2_RX signals to this terminal. For more details refer to TBD.

(6) The internal USB PHY can be configured to multiplex the UART3_TX or UART3_RX signals to this terminal. For more details refer to TBD.

(7) This terminal has an internal pull-down that remains on after reset is released if sysboot[5] is low on the rising edge or PWRONRSTn. This terminal will initially be driven low after reset is released if sysboot[5] is high on the rising edge or PWRONRSTn, then it begins to toggle at the same frequency of the XTALIN terminal.

(8) This terminal has an internal pull-down turned on while reset is asserted.

(9) This terminal is a analog input used to set the switching threshold of the DDR input buffers to (VDDS_DDR / 2).

(10) This terminal is a analog passive signal that connects to an external TBD ohm 2% reference resistor which is used to calibrate the DDR input/output buffers.

(11) This terminal is analog input that may also be configured as an open-drain output.

(12) This terminal is analog input that may also be configured as an open-source or open-drain output.

(13) This terminal is analog input that may also be configured as an open-source output.

(14) This terminal is high-Z when the oscillator is diasabled. This terminal is driven high if RTC_XTALIN is less than VIL, driven low if RTC_XTALIN is greater than VIH, and driven to a unknown value if RTC_XTALIN is between VIL and VIH when the oscillator is enabled. The oscillator is disabled by default after power is applied.

(15) This terminal is high-Z when the oscillator is diasabled. This terminal is driven high if XTALIN is less than VIL, driven low if XTALIN is greater than VIH, and driven to a unknown value if XTALIN is between VIL and VIH when the oscillator is enabled. The oscillator is enabled by default after power is applied.

(16) This terminal requires two power supplies, VDDA3p3v_USB0 and VDDA1p8v_USB0. The "*" character in the power supply name is a wild card that represents "3p3v" and "1p8v".

(17) This terminal requires two power supplies, VDDA3p3v_USB1 and VDDA1p8v_USB1. The "*" character in the power supply name is a wild card that represents "3p3v" and "1p8v".

2.3 Signal Description

Many signals are available on multiple pins according to the software configuration of the pin multiplexing options.

NOTE

The Subsystem Multiplexing Signals are not described in the following tables. For more information, see: TBD

(1) **SIGNAL NAME:** The signal name

(2) **DESCRIPTION:** Description of the signal

(3) **TYPE:** Ball type for this specific function:

- I = Input
- O = Output
- I/O = Input/Output
- D = Open drain
- DS = Differential
- A = Analog

(4) **BALL:** Package ball location

Table 2-8. ADC Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
AIN0	Analog Input/Output	A	B8	B6
AIN1	Analog Input/Output	A	A11	C7
AIN2	Analog Input/Output	A	A8	B7
AIN3	Analog Input/Output	A	B11	A7
AIN4	Analog Input/Output	A	C8	C8
AIN5	Analog Input/Output	A	B12	B8
AIN6	Analog Input/Output	A	A10	A8
AIN7	Analog Input/Output	A	A12	C9
VREFN	Analog Reference Input Negative Terminal	AP	B9	A9
VREFP	Analog Reference Input Positive Terminal	AP	A9	B9

Table 2-9. Debug Subsystem Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
EMU0	MISC EMULATION PIN	I/O	A15	C14
EMU1	MISC EMULATION PIN	I/O	D14	B14
EMU2	MISC EMULATION PIN	I/O	A18, C15	A15, A17, C13
EMU3	MISC EMULATION PIN	I/O	B15, B18	B17, D13, D14
EMU4	MISC EMULATION PIN	I/O	B16, U17	A14, C15, T13
nTRST	JTAG TEST RESET (ACTIVE LOW)	I	A13	B10
TCK	JTAG TEST CLOCK	I	B14	A12
TDI	JTAG TEST DATA INPUT	I	B13	B11
TDO	JTAG TEST DATA OUTPUT	O	A14	A11
TMS	JTAG TEST MODE SELECT	I	C14	C11

Table 2-10. ECAT Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
pr1_edc_latch0_in	Data In	I	E17	D18
pr1_edc_latch1_in	Data In	I	D19	D17

Table 2-10. ECAT Signals Description (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
pr1_edc_sync0_out	Data Out	O	F19	E18
pr1_edc_sync1_out	Data Out	O	F18	E17
pr1_edio_data_in0	Data In	I	B17	B16
pr1_edio_data_in1	Data In	I	A17	A16
pr1_edio_data_in2	Data In	I	U7	U5
pr1_edio_data_in3	Data In	I	T7	R5
pr1_edio_data_in4	Data In	I	W5	V5
pr1_edio_data_in5	Data In	I	W7	R6
pr1_edio_data_in6	Data In	I	V14, V3	T3, U9
pr1_edio_data_in7	Data In	I	U15, U3	T4, V9
pr1_edio_data_out0	Data Out	O	B17	B16
pr1_edio_data_out1	Data Out	O	A17	A16
pr1_edio_data_out2	Data Out	O	U7	U5
pr1_edio_data_out3	Data Out	O	T7	R5
pr1_edio_data_out4	Data Out	O	W5	V5
pr1_edio_data_out5	Data Out	O	W7	R6
pr1_edio_data_out6	Data Out	O	V14, V3	T3, U9
pr1_edio_data_out7	Data Out	O	U15, U3	T4, V9
pr1_edio_latch_in	Latch In	I	B18	B17
pr1_edio_sof	Start of Frame	O	A18	A17

Table 2-11. LCD Controller Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
lcd_ac_bias_en	LCD AC bias enable chip select	O	W7	R6
lcd_data0	LCD data bus	I/O	U1	R1
lcd_data1	LCD data bus	I/O	U2	R2
lcd_data10	LCD data bus	I/O	U5	U3
lcd_data11	LCD data bus	I/O	V5	U4
lcd_data12	LCD data bus	I/O	V6	V2
lcd_data13	LCD data bus	I/O	U6	V3
lcd_data14	LCD data bus	I/O	W6	V4
lcd_data15	LCD data bus	I/O	V7	T5
lcd_data16	LCD data bus	O	V17	U13
lcd_data17	LCD data bus	O	W17	V13
lcd_data18	LCD data bus	O	T13	R12
lcd_data19	LCD data bus	O	U13	T12
lcd_data2	LCD data bus	I/O	V1	R3
lcd_data20	LCD data bus	O	U12	U12
lcd_data21	LCD data bus	O	T12	T11
lcd_data22	LCD data bus	O	W16	T10
lcd_data23	LCD data bus	O	V15	U10
lcd_data3	LCD data bus	I/O	V2	R4
lcd_data4	LCD data bus	I/O	W2	T1
lcd_data5	LCD data bus	I/O	W3	T2
lcd_data6	LCD data bus	I/O	V3	T3
lcd_data7	LCD data bus	I/O	U3	T4

Table 2-11. LCD Controller Signals Description (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
lcd_data8	LCD data bus	I/O	V4	U1
lcd_data9	LCD data bus	I/O	W4	U2
lcd_hsync	LCD Horizontal Sync	O	T7	R5
lcd_memory_clk	LCD MCLK	O	L19, V16	J17, V12
lcd_pclk	LCD pixel clock	O	W5	V5
lcd_vsync	LCD Vertical Sync	O	U7	U5

2.3.1 External Memory Interfaces

Table 2-12. External Memory Interfaces/DDR Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
ddr_a0	DDR SDRAM ROW/COLUMN ADDRESS	O	F3	F3
ddr_a1	DDR SDRAM ROW/COLUMN ADDRESS	O	J2	H1
ddr_a10	DDR SDRAM ROW/COLUMN ADDRESS	O	E2	F4
ddr_a11	DDR SDRAM ROW/COLUMN ADDRESS	O	G4	F2
ddr_a12	DDR SDRAM ROW/COLUMN ADDRESS	O	F4	E3
ddr_a13	DDR SDRAM ROW/COLUMN ADDRESS	O	H1	H3
ddr_a14	DDR SDRAM ROW/COLUMN ADDRESS	O	H3	H4
ddr_a15	DDR SDRAM ROW/COLUMN ADDRESS	O	E3	D3
ddr_a2	DDR SDRAM ROW/COLUMN ADDRESS	O	D1	E4
ddr_a3	DDR SDRAM ROW/COLUMN ADDRESS	O	B3	C3
ddr_a4	DDR SDRAM ROW/COLUMN ADDRESS	O	E5	C2
ddr_a5	DDR SDRAM ROW/COLUMN ADDRESS	O	A2	B1
ddr_a6	DDR SDRAM ROW/COLUMN ADDRESS	O	B1	D5
ddr_a7	DDR SDRAM ROW/COLUMN ADDRESS	O	D2	E2
ddr_a8	DDR SDRAM ROW/COLUMN ADDRESS	O	C3	D4
ddr_a9	DDR SDRAM ROW/COLUMN ADDRESS	O	B2	C1
ddr_ba0	DDR SDRAM BANK ADDRESS	O	A3	C4
ddr_ba1	DDR SDRAM BANK ADDRESS	O	E1	E1
ddr_ba2	DDR SDRAM BANK ADDRESS	O	B4	B3
ddr_casn	DDR SDRAM COLUMN ADDRESS STROBE. (ACTIVE LOW)	O	F1	F1
ddr_ck	DDR SDRAM CLOCK (Differential+)	O	C2	D2
ddr_cke	DDR SDRAM CLOCK ENABLE	O	G3	G3
ddr_csn0	DDR SDRAM CHIP SELECT	O	H2	H2
ddr_d0	DDR SDRAM DATA	I/O	N4	M3
ddr_d1	DDR SDRAM DATA	I/O	P4	M4
ddr_d10	DDR SDRAM DATA	I/O	M3	K2
ddr_d11	DDR SDRAM DATA	I/O	M4	K3
ddr_d12	DDR SDRAM DATA	I/O	M2	K4
ddr_d13	DDR SDRAM DATA	I/O	M1	L3
ddr_d14	DDR SDRAM DATA	I/O	N2	L4
ddr_d15	DDR SDRAM DATA	I/O	N1	M1
ddr_d2	DDR SDRAM DATA	I/O	P2	N1
ddr_d3	DDR SDRAM DATA	I/O	P1	N2
ddr_d4	DDR SDRAM DATA	I/O	P3	N3
ddr_d5	DDR SDRAM DATA	I/O	T1	N4
ddr_d6	DDR SDRAM DATA	I/O	T2	P3
ddr_d7	DDR SDRAM DATA	I/O	R3	P4
ddr_d8	DDR SDRAM DATA	I/O	K2	J1
ddr_d9	DDR SDRAM DATA	I/O	K1	K1
ddr_dqm0	DDR WRITE ENABLE / DATA MASK FOR DATA[7:0]	O	N3	M2
ddr_dqm1	DDR WRITE ENABLE / DATA MASK FOR DATA[15:8]	O	K3	J2
ddr_dqs0	DDR DATA STROBE FOR DATA[7:0] (Differential+)	I/O	R1	P1

Table 2-12. External Memory Interfaces/DDR Signals Description (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
ddr_dqs1	DDR DATA STROBE FOR DATA[15:8] (Differential+)	I/O	L1	L1
ddr_dqsn0	DDR DATA STROBE FOR DATA[7:0] (Differential-)	I/O	R2	P2
ddr_dqsn1	DDR DATA STROBE FOR DATA[15:8] (Differential-)	I/O	L2	L2
ddr_nck	DDR SDRAM CLOCK (Differential-)	O	C1	D1
ddr_odt	ODT	O	G1	G1
ddr_rasn	DDR SDRAM ROW ADDRESS STROBE (ACTIVE LOW)	O	F2	G4
ddr_resetn	DDR3 resetn	O	G2	G2
ddr_vref	Voltage Reference	AP	H4	J4
ddr_vtp	VTP Compensation pin	I	J1	J3
ddr_wen	DDR SDRAM WRITE ENABLE (ACTIVE LOW)	O	A4	B2

Table 2-13. External Memory Interfaces/General Purpose Memory Controller Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
gpmc_a0	GPMC Address	O	U1	R1, R13
gpmc_a1	GPMC Address	O	U2	R2, V14
gpmc_a10	GPMC Address	O	W5	T16, V5
gpmc_a11	GPMC Address	O	W7	R6, V17
gpmc_a12	GPMC Address	O	V4	U1
gpmc_a13	GPMC Address	O	W4	U2
gpmc_a14	GPMC Address	O	U5	U3
gpmc_a15	GPMC Address	O	V5	U4
gpmc_a16	GPMC Address	O	V6	R13, V2
gpmc_a17	GPMC Address	O	U6	V14, V3
gpmc_a18	GPMC Address	O	W6	U14, V4
gpmc_a19	GPMC Address	O	V7	T14, T5
gpmc_a2	GPMC Address	O	V1	R3, U14
gpmc_a20	GPMC Address	O	H19	F17, R14
gpmc_a21	GPMC Address	O	H18	F18, V15
gpmc_a22	GPMC Address	O	H17	G15, U15
gpmc_a23	GPMC Address	O	G18	G16, T15
gpmc_a24	GPMC Address	O	G19	G17, V16
gpmc_a25	GPMC Address	O	G17	G18, U16
gpmc_a26	GPMC Address	O	NA	T16
gpmc_a27	GPMC Address	O	NA	V17
gpmc_a3	GPMC Address	O	V2	R4, T14
gpmc_a4	GPMC Address	O	W2	R14, T1
gpmc_a5	GPMC Address	O	W3	T2, V15
gpmc_a6	GPMC Address	O	V3	T3, U15
gpmc_a7	GPMC Address	O	U3	T15, T4
gpmc_a8	GPMC Address	O	U7	U5, V16
gpmc_a9	GPMC Address	O	T7	R5, U16
gpmc_ad0	GPMC Address & Data	I/O	W10	U7
gpmc_ad1	GPMC Address & Data	I/O	V9	V7

Table 2-13. External Memory Interfaces/General Purpose Memory Controller Signals Description (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
gpmc_ad10	GPMC Address & Data	I/O	T12	T11
gpmc_ad11	GPMC Address & Data	I/O	U12	U12
gpmc_ad12	GPMC Address & Data	I/O	U13	T12
gpmc_ad13	GPMC Address & Data	I/O	T13	R12
gpmc_ad14	GPMC Address & Data	I/O	W17	V13
gpmc_ad15	GPMC Address & Data	I/O	V17	U13
gpmc_ad2	GPMC Address & Data	I/O	V12	R8
gpmc_ad3	GPMC Address & Data	I/O	W13	T8
gpmc_ad4	GPMC Address & Data	I/O	V13	U8
gpmc_ad5	GPMC Address & Data	I/O	W14	V8
gpmc_ad6	GPMC Address & Data	I/O	U14	R9
gpmc_ad7	GPMC Address & Data	I/O	W15	T9
gpmc_ad8	GPMC Address & Data	I/O	V15	U10
gpmc_ad9	GPMC Address & Data	I/O	W16	T10
gpmc_advn_ale	GPMC Address Valid / Address Latch Enable	O	V10	R7
gpmc_be0n_cle	GPMC Byte Enable 0 / Command Latch Enable	O	V8	T6
gpmc_be1n	GPMC Byte Enable 1	O	U15, V18	U18, V9
gpmc_clk	GPMC Clock	I/O	V14, V16	U9, V12
gpmc_csn0	GPMC Chip Select	O	W8	V6
gpmc_csn1	GPMC Chip Select	O	V14	U9
gpmc_csn2	GPMC Chip Select	O	U15	V9
gpmc_csn3	GPMC Chip Select	O	U17	T13
gpmc_csn4	GPMC Chip Select	O	R15	T17
gpmc_csn5	GPMC Chip Select	O	W18	U17
gpmc_csn6	GPMC Chip Select	O	V18	U18
gpmc_dir	GPMC Data Direction	O	V18	U18
gpmc_oen_ren	GPMC Output / Read Enable	O	W9	T7
gpmc_wait0	GPMC Wait 0	I	R15	T17
gpmc_wait1	GPMC Wait 1	I	V16	V12
gpmc_wen	GPMC Write Enable	O	U8	U6
gpmc_wpn	GPMC Write Protect	O	W18	U17

2.3.2 General Purpose IOs

Table 2-14. General Purpose IOs/GPIO0 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
gpio0_0	GPIO	I/O	P17	M17
gpio0_1	GPIO	I/O	R19	M18
gpio0_10	GPIO	I/O	W6	V4
gpio0_11	GPIO	I/O	V7	T5
gpio0_12	GPIO	I/O	E17	D18
gpio0_13	GPIO	I/O	D19	D17
gpio0_14	GPIO	I/O	D18	D16
gpio0_15	GPIO	I/O	C19	D15
gpio0_16	GPIO	I/O	M17	J18
gpio0_17	GPIO	I/O	N18	K15
gpio0_18	GPIO	I/O	G16	F16
gpio0_19	GPIO	I/O	C15	A15
gpio0_2	GPIO	I/O	A18	A17
gpio0_20	GPIO	I/O	B15	D14
gpio0_21	GPIO	I/O	M18	K16
gpio0_22	GPIO	I/O	V15	U10
gpio0_23	GPIO	I/O	W16	T10
gpio0_26	GPIO	I/O	T12	T11
gpio0_27	GPIO	I/O	U12	U12
gpio0_28	GPIO	I/O	L18	K17
gpio0_29	GPIO	I/O	K18	H18
gpio0_3	GPIO	I/O	B18	B17
gpio0_30	GPIO	I/O	R15	T17
gpio0_31	GPIO	I/O	W18	U17
gpio0_4	GPIO	I/O	B17	B16
gpio0_5	GPIO	I/O	A17	A16
gpio0_6	GPIO	I/O	B16	C15
gpio0_7	GPIO	I/O	E18	C18
gpio0_8	GPIO	I/O	V6	V2
gpio0_9	GPIO	I/O	U6	V3

Table 2-15. General Purpose IOs/GPIO1 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
gpio1_0	GPIO	I/O	W10	U7
gpio1_1	GPIO	I/O	V9	V7
gpio1_10	GPIO	I/O	E19	E15
gpio1_11	GPIO	I/O	F17	E16
gpio1_12	GPIO	I/O	U13	T12
gpio1_13	GPIO	I/O	T13	R12
gpio1_14	GPIO	I/O	W17	V13
gpio1_15	GPIO	I/O	V17	U13
gpio1_16	GPIO	I/O	NA	R13
gpio1_17	GPIO	I/O	NA	V14
gpio1_18	GPIO	I/O	NA	U14

Table 2-15. General Purpose IOs/GPIO1 Signals Description (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
gpio1_19	GPIO	I/O	NA	T14
gpio1_2	GPIO	I/O	V12	R8
gpio1_20	GPIO	I/O	NA	R14
gpio1_21	GPIO	I/O	NA	V15
gpio1_22	GPIO	I/O	NA	U15
gpio1_23	GPIO	I/O	NA	T15
gpio1_24	GPIO	I/O	NA	V16
gpio1_25	GPIO	I/O	NA	U16
gpio1_26	GPIO	I/O	NA	T16
gpio1_27	GPIO	I/O	NA	V17
gpio1_28	GPIO	I/O	V18	U18
gpio1_29	GPIO	I/O	W8	V6
gpio1_3	GPIO	I/O	W13	T8
gpio1_30	GPIO	I/O	V14	U9
gpio1_31	GPIO	I/O	U15	V9
gpio1_4	GPIO	I/O	V13	U8
gpio1_5	GPIO	I/O	W14	V8
gpio1_6	GPIO	I/O	U14	R9
gpio1_7	GPIO	I/O	W15	T9
gpio1_8	GPIO	I/O	F19	E18
gpio1_9	GPIO	I/O	F18	E17

Table 2-16. General Purpose IOs/GPIO2 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
gpio2_0	GPIO	I/O	U17	T13
gpio2_1	GPIO	I/O	V16	V12
gpio2_10	GPIO	I/O	W2	T1
gpio2_11	GPIO	I/O	W3	T2
gpio2_12	GPIO	I/O	V3	T3
gpio2_13	GPIO	I/O	U3	T4
gpio2_14	GPIO	I/O	V4	U1
gpio2_15	GPIO	I/O	W4	U2
gpio2_16	GPIO	I/O	U5	U3
gpio2_17	GPIO	I/O	V5	U4
gpio2_18	GPIO	I/O	N17	L17
gpio2_19	GPIO	I/O	N16	L16
gpio2_2	GPIO	I/O	V10	R7
gpio2_20	GPIO	I/O	P19	L15
gpio2_21	GPIO	I/O	P18	M16
gpio2_22	GPIO	I/O	U7	U5
gpio2_23	GPIO	I/O	T7	R5
gpio2_24	GPIO	I/O	W5	V5
gpio2_25	GPIO	I/O	W7	R6
gpio2_26	GPIO	I/O	H19	F17
gpio2_27	GPIO	I/O	H18	F18
gpio2_28	GPIO	I/O	H17	G15

Table 2-16. General Purpose IOs/GPIO2 Signals Description (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
gpio2_29	GPIO	I/O	G18	G16
gpio2_3	GPIO	I/O	W9	T7
gpio2_30	GPIO	I/O	G19	G17
gpio2_31	GPIO	I/O	G17	G18
gpio2_4	GPIO	I/O	U8	U6
gpio2_5	GPIO	I/O	V8	T6
gpio2_6	GPIO	I/O	U1	R1
gpio2_7	GPIO	I/O	U2	R2
gpio2_8	GPIO	I/O	V1	R3
gpio2_9	GPIO	I/O	V2	R4

Table 2-17. General Purpose IOs/GPIO3 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
gpio3_0	GPIO	I/O	J19	H16
gpio3_1	GPIO	I/O	J18	H17
gpio3_10	GPIO	I/O	M19	L18
gpio3_13	GPIO	I/O	NA	F15
gpio3_14	GPIO	I/O	NA	A13
gpio3_15	GPIO	I/O	NA	B13
gpio3_16	GPIO	I/O	NA	D12
gpio3_17	GPIO	I/O	NA	C12
gpio3_18	GPIO	I/O	NA	B12
gpio3_19	GPIO	I/O	NA	C13
gpio3_2	GPIO	I/O	K19	J15
gpio3_20	GPIO	I/O	NA	D13
gpio3_21	GPIO	I/O	NA	A14
gpio3_3	GPIO	I/O	K17	J16
gpio3_4	GPIO	I/O	L19	J17
gpio3_5	GPIO	I/O	C18	C17
gpio3_6	GPIO	I/O	B19	C16
gpio3_7	GPIO	I/O	A15	C14
gpio3_8	GPIO	I/O	D14	B14
gpio3_9	GPIO	I/O	N19	K18

2.3.3 Miscellaneous

Table 2-18. Miscellaneous/Miscellaneous Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
clkout1	Clock out1	O	C15	A15
clkout2	Clock out2	O	B15	D14
ENZ_KALDO_1P8V	Analog Input/Output	I	A7	B4
EXT_WAKEUP	EXT_WAKEUP	I	B5	C5
nNMI	External Interrupt to ARM Cortex A8 Core	I	C17	B18
nRESETIN_OUT	Chip Reset	I/OD	A16	A10
OSC0_IN	HF OSCILLATOR RECEIVER	I	W11	V10
OSC0_OUT	HF OSCILLATOR DRIVER	O	W12	U11
PMIC_POWER_EN	PMIC_POWER_EN	O	C7	C6
porz	Power on Reset	I	E15	B15
tclkin	Timer Clock In	I	B15	D14
xdma_event_intr0	External DMA Event or Interrupt 0	I	C15	A15
xdma_event_intr1	External DMA Event or Interrupt 1	I	B15	D14
xdma_event_intr2	External DMA Event or Interrupt 2	I	B16, E18, K18	C15, C18, H18

2.3.3.1 eCAP

Table 2-19. eCAP/eCAP0 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
eCAP0_in_PWM0_out	enhanced capture 0 input or Auxiliary PWM0 out	I/O	E18	C18

Table 2-20. eCAP/eCAP1 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
eCAP1_in_PWM1_out	enhanced capture 1 input or Auxiliary PWM1 out	I/O	B16, B19, F17	C15, C16, E16

Table 2-21. eCAP/eCAP2 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
eCAP2_in_PWM2_out	enhanced capture 2 input or Auxiliary PWM2 out	I/O	C18, E19	C12, C17, E15

2.3.3.2 eHRPWM

Table 2-22. eHRPWM/eHRPWM0 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
ehrpwm0A	eHRPWM0 A output.	O	A18	A13, A17
ehrpwm0B	eHRPWM0 B output.	O	B18	B13, B17
ehrpwm0_synci	Sync input to eHRPWM0 module from an external pin	I	A17	A16, C12
ehrpwm0_synco	Sync Output from eHRPWM0 module to an external pin	O	U12, V2, W4	R4, U12, U2, V14
ehrpwm0_tripzone_input	eHRPWM0 trip zone input	I	B17	B16, D12

Table 2-23. eHRPWM/eHRPWM1 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
ehrpwm1A	eHRPWM1 A output.	O	U5	U14, U3
ehrpwm1B	eHRPWM1 B output.	O	V5	T14, U4
ehrpwm1_tripzone_input	eHRPWM1 trip zone input	I	V4	R13, U1

Table 2-24. eHRPWM/eHRPWM2 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
ehrpwm2A	eHRPWM2 A output.	O	U1, V15	R1, U10
ehrpwm2B	eHRPWM2 B output.	O	U2, W16	R2, T10
ehrpwm2_tripzone_input	eHRPWM2 trip zone input	I	T12, V1	R3, T11

2.3.3.3 eQEP

Table 2-25. eQEP/eQEP0 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
eQEP0A_in	eQEP0A quadrature input	I	M18	B12, K16
eQEP0B_in	eQEP0B quadrature input	I	L18	C13, K17
eQEP0_index	eQEP0 index.	I/O	K17	D13, J16
eQEP0_strobe	eQEP0 strobe.	I/O	P19	A14, L15

Table 2-26. eQEP/eQEP1 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
eQEP1A_in	eQEP1A quadrature input	I	V6	R14, V2
eQEP1B_in	eQEP1B quadrature input	I	U6	V15, V3
eQEP1_index	eQEP1 index.	I/O	W6	U15, V4
eQEP1_strobe	eQEP1 strobe.	I/O	V7	T15, T5

Table 2-27. eQEP/eQEP2 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
eQEP2A_in	eQEP2A quadrature input	I	U13, W2	T1, T12
eQEP2B_in	eQEP2B quadrature input	I	T13, W3	R12, T2
eQEP2_index	eQEP2 index.	I/O	V3, W17	T3, V13
eQEP2_strobe	eQEP2 strobe.	I/O	U3, V17	T4, U13

2.3.3.4 Timer

Table 2-28. Timer/Timer4 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
timer4	Timer trigger event / PWM out	I/O	C15, C18, K17, V10	A15, C17, J16, R7

Table 2-29. Timer/Timer5 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
timer5	Timer trigger event / PWM out	I/O	D19, H19, R19, V8	D17, F17, M18, T6

Table 2-30. Timer/Timer6 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
timer6	Timer trigger event / PWM out	I/O	E17, H18, P17, U8	D18, F18, M17, U6

Table 2-31. Timer/Timer7 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
timer7	Timer trigger event / PWM out	I/O	B15, B19, F19, W9	C16, D14, E18, T7

2.3.4 PRU Subsystem

Table 2-32. PRU Subsystem/MII0 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
pr1_mii0_col	MII Collision Detect	I	W16	T10
pr1_mii0_crs	MII Carrier Sense	I	U17, W5	T13, V5
pr1_mii0_rxd0	MII Receive Data bit 0	I	V5	U4
pr1_mii0_rxd1	MII Receive Data bit 1	I	U5	U3
pr1_mii0_rxd2	MII Receive Data bit 2	I	W4	U2
pr1_mii0_rxd3	MII Receive Data bit 3	I	V4	U1
pr1_mii0_rxdv	MII Receive Data Valid	I	V7	T5
pr1_mii0_rxer	MII Receive Data Error	I	U6	V3
pr1_mii0_rxlink	MII Receive Link	I	V6	V2
pr1_mii0_txd0	MII Transmit Data bit 0	O	W17, W3	T2, V13
pr1_mii0_txd1	MII Transmit Data bit 1	O	T13, W2	R12, T1
pr1_mii0_txd2	MII Transmit Data bit 2	O	U13, V2	R4, T12
pr1_mii0_txd3	MII Transmit Data bit 3	O	U12, V1	R3, U12
pr1_mii0_txen	MII Transmit Enable	O	T12, U2	R2, T11
pr1_mii_mr0_clk	MII Receive Clock	I	W6	V4
pr1_mii_mt0_clk	MII Transmit Clock	I	U1, V15	R1, U10

Table 2-33. PRU Subsystem/MII1 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
pr1_mii1_col	MII Collision Detect	I	R15	T17
pr1_mii1_crs	MII Carrier Sense	I	V16, W7	R6, V12
pr1_mii1_rxd0	MII Receive Data bit 0	I	NA	V16
pr1_mii1_rxd1	MII Receive Data bit 1	I	NA	T15
pr1_mii1_rxd2	MII Receive Data bit 2	I	NA	U15
pr1_mii1_rxd3	MII Receive Data bit 3	I	NA	V15
pr1_mii1_rxdv	MII Receive Data Valid	I	NA	T16
pr1_mii1_rxer	MII Receive Data Error	I	NA	V17
pr1_mii1_rxlink	MII Receive Link	I	V18	U18
pr1_mii1_txd0	MII Transmit Data bit 0	O	NA	R14
pr1_mii1_txd1	MII Transmit Data bit 1	O	NA	T14
pr1_mii1_txd2	MII Transmit Data bit 2	O	NA	U14
pr1_mii1_txd3	MII Transmit Data bit 3	O	NA	V14
pr1_mii1_txen	MII Transmit Enable	O	W18	U17
pr1_mii_mr1_clk	MII Receive Clock	I	NA	U16
pr1_mii_mt1_clk	MII Transmit Clock	I	NA	R13

Table 2-34. PRU Subsystem/UART0 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
pr1_uart0_cts_n	UART Clear to Send	I	A18, E17	A17, D18
pr1_uart0_rts_n	UART Request to Send	O	B18, D19	B17, D17
pr1_uart0_rxd	UART Receive Data	I	B17, D18	B16, D16
pr1_uart0_txd	UART Transmit Data	O	A17, C19	A16, D15

2.3.4.1 PRU0

Table 2-35. PRU0/General Purpose Inputs Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
pr1_pru0_pru_r31_0	PRU0 Data In	I	NA	A13
pr1_pru0_pru_r31_1	PRU0 Data In	I	NA	B13
pr1_pru0_pru_r31_10	PRU0 Data In	I	H17	G15
pr1_pru0_pru_r31_11	PRU0 Data In	I	G18	G16
pr1_pru0_pru_r31_12	PRU0 Data In	I	G19	G17
pr1_pru0_pru_r31_13	PRU0 Data In	I	G17	G18
pr1_pru0_pru_r31_14	PRU0 Data In	I	W17	V13
pr1_pru0_pru_r31_15	PRU0 Data In	I	V17	U13
pr1_pru0_pru_r31_16	PRU0 Data In Capture Enable	I	B15, C19	D14, D15
pr1_pru0_pru_r31_2	PRU0 Data In	I	NA	D12
pr1_pru0_pru_r31_3	PRU0 Data In	I	NA	C12
pr1_pru0_pru_r31_4	PRU0 Data In	I	NA	B12
pr1_pru0_pru_r31_5	PRU0 Data In	I	NA	C13
pr1_pru0_pru_r31_6	PRU0 Data In	I	NA	D13
pr1_pru0_pru_r31_7	PRU0 Data In	I	NA	A14
pr1_pru0_pru_r31_8	PRU0 Data In	I	H19	F17
pr1_pru0_pru_r31_9	PRU0 Data In	I	H18	F18

Table 2-36. PRU0/General Purpose Outputs Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
pr1_pru0_pru_r30_0	PRU0 Data Out	O	NA	A13
pr1_pru0_pru_r30_1	PRU0 Data Out	O	NA	B13
pr1_pru0_pru_r30_10	PRU0 Data Out	O	H17	G15
pr1_pru0_pru_r30_11	PRU0 Data Out	O	G18	G16
pr1_pru0_pru_r30_12	PRU0 Data Out	O	G19	G17
pr1_pru0_pru_r30_13	PRU0 Data Out	O	G17	G18
pr1_pru0_pru_r30_14	PRU0 Data Out	O	U13	T12
pr1_pru0_pru_r30_15	PRU0 Data Out	O	T13	R12
pr1_pru0_pru_r30_2	PRU0 Data Out	O	NA	D12
pr1_pru0_pru_r30_3	PRU0 Data Out	O	NA	C12
pr1_pru0_pru_r30_4	PRU0 Data Out	O	NA	B12
pr1_pru0_pru_r30_5	PRU0 Data Out	O	NA	C13
pr1_pru0_pru_r30_6	PRU0 Data Out	O	NA	D13
pr1_pru0_pru_r30_7	PRU0 Data Out	O	NA	A14
pr1_pru0_pru_r30_8	PRU0 Data Out	O	H19	F17
pr1_pru0_pru_r30_9	PRU0 Data Out	O	H18	F18

2.3.4.2 PRU1

Table 2-37. PRU1/General Purpose Inputs Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
pr1_pru1_pru_r31_0	PRU1 Data In	I	U1	R1
pr1_pru1_pru_r31_1	PRU1 Data In	I	U2	R2
pr1_pru1_pru_r31_10	PRU1 Data In	I	W5	V5
pr1_pru1_pru_r31_11	PRU1 Data In	I	W7	R6
pr1_pru1_pru_r31_12	PRU1 Data In	I	V14	U9
pr1_pru1_pru_r31_13	PRU1 Data In	I	U15	V9
pr1_pru1_pru_r31_14	PRU1 Data In	I	E19	E15
pr1_pru1_pru_r31_15	PRU1 Data In	I	F17	E16
pr1_pru1_pru_r31_16	PRU1 Data In Capture Enable	I	C15, D18	A15, D16
pr1_pru1_pru_r31_2	PRU1 Data In	I	V1	R3
pr1_pru1_pru_r31_3	PRU1 Data In	I	V2	R4
pr1_pru1_pru_r31_4	PRU1 Data In	I	W2	T1
pr1_pru1_pru_r31_5	PRU1 Data In	I	W3	T2
pr1_pru1_pru_r31_6	PRU1 Data In	I	V3	T3
pr1_pru1_pru_r31_7	PRU1 Data In	I	U3	T4
pr1_pru1_pru_r31_8	PRU1 Data In	I	U7	U5
pr1_pru1_pru_r31_9	PRU1 Data In	I	T7	R5

Table 2-38. PRU1/General Purpose Outputs Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
pr1_pru1_pru_r30_0	PRU1 Data Out	O	U1	R1
pr1_pru1_pru_r30_1	PRU1 Data Out	O	U2	R2
pr1_pru1_pru_r30_10	PRU1 Data Out	O	W5	V5
pr1_pru1_pru_r30_11	PRU1 Data Out	O	W7	R6
pr1_pru1_pru_r30_12	PRU1 Data Out	O	V14	U9
pr1_pru1_pru_r30_13	PRU1 Data Out	O	U15	V9
pr1_pru1_pru_r30_14	PRU1 Data Out	O	E19	E15
pr1_pru1_pru_r30_15	PRU1 Data Out	O	F17	E16
pr1_pru1_pru_r30_2	PRU1 Data Out	O	V1	R3
pr1_pru1_pru_r30_3	PRU1 Data Out	O	V2	R4
pr1_pru1_pru_r30_4	PRU1 Data Out	O	W2	T1
pr1_pru1_pru_r30_5	PRU1 Data Out	O	W3	T2
pr1_pru1_pru_r30_6	PRU1 Data Out	O	V3	T3
pr1_pru1_pru_r30_7	PRU1 Data Out	O	U3	T4
pr1_pru1_pru_r30_8	PRU1 Data Out	O	U7	U5
pr1_pru1_pru_r30_9	PRU1 Data Out	O	T7	R5

2.3.5 Removable Media Interfaces

Table 2-39. Removable Media Interfaces/MMC0 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
mmc0_clk	MMC/SD/SDIO Clock	I/O	G19	G17
mmc0_cmd	MMC/SD/SDIO Command	I/O	G17	G18
mmc0_dat0	MMC/SD/SDIO Data Bus	I/O	G18	G16
mmc0_dat1	MMC/SD/SDIO Data Bus	I/O	H17	G15
mmc0_dat2	MMC/SD/SDIO Data Bus	I/O	H18	F18
mmc0_dat3	MMC/SD/SDIO Data Bus	I/O	H19	F17
mmc0_dat4	MMC/SD/SDIO Data Bus	I/O	N16	L16
mmc0_dat5	MMC/SD/SDIO Data Bus	I/O	N17	L17
mmc0_dat6	MMC/SD/SDIO Data Bus	I/O	M19	L18
mmc0_dat7	MMC/SD/SDIO Data Bus	I/O	N19	K18
mmc0_pow	MMC/SD Power Switch Control	O	B16, K18	C15, H18
mmc0_sdcd	SD Card Detect	I	B16, P17	A13, C15, M17
mmc0_sdwp	SD Write Protect	I	E18, R19	B12, C18, M18

Table 2-40. Removable Media Interfaces/MMC1 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
mmc1_clk	MMC/SD/SDIO Clock	I/O	L18, R19, V14	K17, M18, U9
mmc1_cmd	MMC/SD/SDIO Command	I/O	M18, P17, U15	K16, M17, V9
mmc1_dat0	MMC/SD/SDIO Data Bus	I/O	N19, V15, W10	K18, U10, U7
mmc1_dat1	MMC/SD/SDIO Data Bus	I/O	M19, V9, W16	L18, T10, V7
mmc1_dat2	MMC/SD/SDIO Data Bus	I/O	N17, T12, V12	L17, R8, T11
mmc1_dat3	MMC/SD/SDIO Data Bus	I/O	N16, U12, W13	L16, T8, U12
mmc1_dat4	MMC/SD/SDIO Data Bus	I/O	U13, V13	T12, U8
mmc1_dat5	MMC/SD/SDIO Data Bus	I/O	T13, W14	R12, V8
mmc1_dat6	MMC/SD/SDIO Data Bus	I/O	U14, W17	R9, V13
mmc1_dat7	MMC/SD/SDIO Data Bus	I/O	V17, W15	T9, U13
mmc1_sdcd	SD Card Detect	I	R15	B13, T17
mmc1_sdwp	SD Write Protect	I	B17, D18	B16, D16

Table 2-41. Removable Media Interfaces/MMC2 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
mmc2_clk	MMC/SD/SDIO Clock	I/O	P19, R19, V16	L15, M18, V12
mmc2_cmd	MMC/SD/SDIO Command	I/O	K17, P17, U17	J16, M17, T13
mmc2_dat0	MMC/SD/SDIO Data Bus	I/O	L19, U13	J17, T12, V14
mmc2_dat1	MMC/SD/SDIO Data Bus	I/O	M17, T13	J18, R12, U14
mmc2_dat2	MMC/SD/SDIO Data Bus	I/O	N18, W17	K15, T14, V13
mmc2_dat3	MMC/SD/SDIO Data Bus	I/O	J19, V17, V18	H16, U13, U18
mmc2_dat4	MMC/SD/SDIO Data Bus	I/O	V15	U10, U15
mmc2_dat5	MMC/SD/SDIO Data Bus	I/O	W16	T10, T15
mmc2_dat6	MMC/SD/SDIO Data Bus	I/O	T12	T11, V16
mmc2_dat7	MMC/SD/SDIO Data Bus	I/O	U12	U12, U16
mmc2_sdcd	SD Card Detect	I	W18	D12, U17
mmc2_sdwp	SD Write Protect	I	A17, C19	A16, D15

2.3.6 Serial Communication Interfaces

2.3.6.1 CAN

Table 2-42. CAN/DCAN0 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
dcan0_rx	DCAN0 Receive Data	I	D19, F17, N18	D17, E16, K15
dcan0_tx	DCAN0 Transmit Data	O	E17, E19, M17	D18, E15, J18

Table 2-43. CAN/DCAN1 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
dcan1_rx	DCAN1 Receive Data	I	C19, F18, G17	D15, E17, G18
dcan1_tx	DCAN1 Transmit Data	O	D18, F19, G19	D16, E18, G17

2.3.6.2 GEMAC_CPSW

Table 2-44. GEMAC_CPSW/MII1 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
gmii1_col	MII Colision	I	J19	H16
gmii1_crs	MII Carrier Sense	I	J18	H17
gmii1_rxclk	MII Receive Clock	I	M19	L18
gmii1_rxd0	MII Receive Data bit 0	I	P18	M16
gmii1_rxd1	MII Receive Data bit 1	I	P19	L15
gmii1_rxd2	MII Receive Data bit 2	I	N16	L16
gmii1_rxd3	MII Receive Data bit 3	I	N17	L17
gmii1_rxdv	MII Receive Data Valid	I	L19	J17
gmii1_rxer	MII Receive Data Error	I	K19	J15
gmii1_txclk	MII Transmit Clock	I	N19	K18
gmii1_txd0	MII Transmit Data bit 0	O	L18	K17
gmii1_txd1	MII Transmit Data bit 1	O	M18	K16
gmii1_txd2	MII Transmit Data bit 2	O	N18	K15
gmii1_txd3	MII Transmit Data bit 3	O	M17	J18
gmii1_txen	MII Transmit Enable	O	K17	J16

Table 2-45. GEMAC_CPSW/MII2 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
gmii2_col	MII Colision	I	V18	U18
gmii2_crs	MII Carrier Sense	I	R15	T17
gmii2_rxclk	MII Receive Clock	I	NA	T15
gmii2_rxd0	MII Receive Data bit 0	I	NA	V17
gmii2_rxd1	MII Receive Data bit 1	I	NA	T16
gmii2_rxd2	MII Receive Data bit 2	I	NA	U16
gmii2_rxd3	MII Receive Data bit 3	I	NA	V16
gmii2_rxdv	MII Receive Data Valid	I	NA	V14
gmii2_rxer	MII Receive Data Error	I	W18	U17
gmii2_txclk	MII Transmit Clock	I	NA	U15
gmii2_txd0	MII Transmit Data bit 0	O	NA	V15
gmii2_txd1	MII Transmit Data bit 1	O	NA	R14
gmii2_txd2	MII Transmit Data bit 2	O	NA	T14
gmii2_txd3	MII Transmit Data bit 3	O	NA	U14
gmii2_txen	MII Transmit Enable	O	NA	R13

Table 2-46. GEMAC_CPSW/RGMII1 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
rgmii1_rclk	RGMII Receive Clock	I	M19	L18
rgmii1_rctl	RGMII Receive Control	I	L19	J17
rgmii1_rd0	RGMII Receive Data bit 0	I	P18	M16
rgmii1_rd1	RGMII Receive Data bit 1	I	P19	L15
rgmii1_rd2	RGMII Receive Data bit 2	I	N16	L16
rgmii1_rd3	RGMII Receive Data bit 3	I	N17	L17
rgmii1_tclk	RGMII Transmit Clock	O	N19	K18

Table 2-46. GEMAC_CPSW/RGMII1 Signals Description (continued)

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
rgmii1_tctl	RGMII Transmit Control	O	K17	J16
rgmii1_td0	RGMII Transmit Data bit 0	O	L18	K17
rgmii1_td1	RGMII Transmit Data bit 1	O	M18	K16
rgmii1_td2	RGMII Transmit Data bit 2	O	N18	K15
rgmii1_td3	RGMII Transmit Data bit 3	O	M17	J18

Table 2-47. GEMAC_CPSW/RGMII2 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
rgmii2_rclk	RGMII Receive Clock	I	NA	T15
rgmii2_rctl	RGMII Receive Control	I	NA	V14
rgmii2_rd0	RGMII Receive Data bit 0	I	NA	V17
rgmii2_rd1	RGMII Receive Data bit 1	I	NA	T16
rgmii2_rd2	RGMII Receive Data bit 2	I	NA	U16
rgmii2_rd3	RGMII Receive Data bit 3	I	NA	V16
rgmii2_tclk	RGMII Transmit Clock	O	NA	U15
rgmii2_tctl	RGMII Transmit Control	O	NA	R13
rgmii2_td0	RGMII Transmit Data bit 0	O	NA	V15
rgmii2_td1	RGMII Transmit Data bit 1	O	NA	R14
rgmii2_td2	RGMII Transmit Data bit 2	O	NA	T14
rgmii2_td3	RGMII Transmit Data bit 3	O	NA	U14

Table 2-48. GEMAC_CPSW/RMII1 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
rmii1_crs_dv	RMII Carrier Sense / Data Valid	I	J18	H17
rmii1_refclk	RMII Reference Clock	I/O	K18	H18
rmii1_rxd0	RMII Receive Data bit 0	I	P18	M16
rmii1_rxd1	RMII Receive Data bit 1	I	P19	L15
rmii1_rxer	RMII Receive Data Error	I	K19	J15
rmii1_txd0	RMII Transmit Data bit 0	O	L18	K17
rmii1_txd1	RMII Transmit Data bit 1	O	M18	K16
rmii1_txen	RMII Transmit Enable	O	K17	J16

Table 2-49. GEMAC_CPSW/RMII2 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
rmii2_crs_dv	RMII Carrier Sense / Data Valid	I	R15	T17
rmii2_refclk	RMII Reference Clock	I/O	J19	H16
rmii2_rxd0	RMII Receive Data bit 0	I	NA	V17
rmii2_rxd1	RMII Receive Data bit 1	I	NA	T16
rmii2_rxer	RMII Receive Data Error	I	W18	U17
rmii2_txd0	RMII Transmit Data bit 0	O	NA	V15
rmii2_txd1	RMII Transmit Data bit 1	O	NA	R14
rmii2_txen	RMII Transmit Enable	O	NA	R13

2.3.6.3 I2C

Table 2-50. I2C/I2C0 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
I2C0_SCL	I2C0 Clock	I/OD	B19	C16
I2C0_SDA	I2C0 Data	I/OD	C18	C17

Table 2-51. I2C/I2C1 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
I2C1_SCL	I2C1 Clock	I/OD	A17, C19, F18, K19	A16, D15, E17, J15
I2C1_SDA	I2C1 Data	I/OD	B17, D18, F19, J18	B16, D16, E18, H17

Table 2-52. I2C/I2C2 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
I2C2_SCL	I2C2 Clock	I/OD	B18, D19, F17	B17, D17, E16
I2C2_SDA	I2C2 Data	I/OD	A18, E17, E19	A17, D18, E15

2.3.6.4 McASP

Table 2-53. McASP/MCASP0 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
mcasp0_aclkr	McASP0 Receive Bit Clock	I/O	L19, V18, V6	B12, J17, U18, V2
mcasp0_aclkx	McASP0 Transmit Bit Clock	I/O	N19, V4	A13, K18, U1, V16
mcasp0_ahclkr	McASP0 Receive Master Clock	I/O	V5	C12, U4
mcasp0_ahclkx	McASP0 Transmit Master Clock	I/O	N18, V7	A14, K15, T5
mcasp0_axr0	McASP0 Serial Data (IN/OUT)	I/O	N17, U5	D12, L17, T16, U3
mcasp0_axr1	McASP0 Serial Data (IN/OUT)	I/O	N16, W6	D13, L16, V17, V4
mcasp0_axr2	McASP0 Serial Data (IN/OUT)	I/O	J19, V5, V6	B12, C12, H16, U4, V2
mcasp0_axr3	McASP0 Serial Data (IN/OUT)	I/O	P18, U6, V7	A14, C13, M16, T5, V3
mcasp0_fsr	McASP0 Receive Frame Sync	I/O	M17, U6, V16	C13, J18, V12, V3
mcasp0_fsx	McASP0 Transmit Frame Sync	I/O	M19, W4	B13, L18, U16, U2

Table 2-54. McASP/MCASP1 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
mcasp1_aclkr	McASP1 Receive Bit Clock	I/O	L18, P18	K17, M16
mcasp1_aclkx	McASP1 Transmit Bit Clock	I/O	J18, L19	B12, H17, J17
mcasp1_ahclkr	McASP1 Receive Master Clock	I/O	P18	M16
mcasp1_ahclkx	McASP1 Transmit Master Clock	I/O	K18, P18	H18, M16
mcasp1_axr0	McASP1 Serial Data (IN/OUT)	I/O	K17, N18	D13, J16, K15
mcasp1_axr1	McASP0 Serial Data (IN/OUT)	I/O	M18	A14, K16
mcasp1_axr2	McASP0 Serial Data (IN/OUT)	I/O	J19, L18	H16, K17
mcasp1_axr3	McASP0 Serial Data (IN/OUT)	I/O	K18, P19	H18, L15
mcasp1_fsr	McASP1 Receive Frame Sync	I/O	M18, P19	K16, L15
mcasp1_fsx	McASP1 Transmit Frame Sync	I/O	K19, M17	C13, J15, J18

2.3.6.5 SPI

Table 2-55. SPI/SPI0 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
spi0_cs0	SPI Chip Select	I/O	A17	A16
spi0_cs1	SPI Chip Select	I/O	B16	C15
spi0_d0	SPI Data	I/O	B18	B17
spi0_d1	SPI Data	I/O	B17	B16
spi0_sclk	SPI Clock	I/O	A18	A17

Table 2-56. SPI/SPI1 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
spi1_cs0	SPI Chip Select	I/O	E17, E19, F18, K18	C12, D18, E15, E17, H18
spi1_cs1	SPI Chip Select	I/O	C15, D19, E18, F17	A15, C18, D17, E16
spi1_d0	SPI Data	I/O	F19, J18	B13, E18, H17
spi1_d1	SPI Data	I/O	F18, K19	D12, E17, J15
spi1_sclk	SPI Clock	I/O	E18, J19	A13, C18, H16

2.3.6.6 UART

Table 2-57. UART/UART0 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
uart0_ctsn	UART Clear to Send	I	F19	E18
uart0_rtsn	UART Request to Send	O	F18	E17
uart0_rxd	UART Receive Data	I	E19	E15
uart0_txd	UART Transmit Data	O	F17	E16

Table 2-58. UART/UART1 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
uart1_ctsn	UART Clear to Send	I	E17	D18
uart1_dcdn	UART Clear to Send	I	H19, N19	F17, K18
uart1_dsrn	UART Request to Send	I	H18, M19	F18, L18
uart1_dtrn	UART Receive Data	O	H17, N17	G15, L17
uart1_rin	UART Transmit Data	I	G18, N16	G16, L16
uart1_rtsn	UART Request to Send	O	D19	D17
uart1_rxd	UART Receive Data	I	D18	D16
uart1_txd	UART Transmit Data	O	C19	D15

Table 2-59. UART/UART2 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
uart2_ctsn	UART Clear to Send	I	C18, V4	C17, U1
uart2_rtsn	UART Request to Send	O	B19, W4	C16, U2
uart2_rxd	UART Receive Data	I	A18, G19, J18, N19	A17, G17, H17, K18
uart2_txd	UART Transmit Data	O	B18, G17, K19, M19	B17, G18, J15, L18

Table 2-60. UART/UART3 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
uart3_ctsn	UART Clear to Send	I	G19, P17, U5	G17, M17, U3
uart3_rtsn	UART Request to Send	O	G17, R19, V5	G18, M18, U4
uart3_rxd	UART Receive Data	I	B16, H17, N17	C15, G15, L17
uart3_txd	UART Transmit Data	O	E18, G18, N16	C18, G16, L16

Table 2-61. UART/UART4 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
uart4_ctsn	UART Clear to Send	I	H19, V6	F17, V2
uart4_rtsn	UART Request to Send	O	H18, U6	F18, V3
uart4_rxd	UART Receive Data	I	F19, M17, R15	E18, J18, T17
uart4_txd	UART Transmit Data	O	F18, N18, W18	E17, K15, U17

Table 2-62. UART/UART5 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
uart5_ctsn	UART Clear to Send	I	H17, J18, W6	G15, H17, V4
uart5_rtsn	UART Request to Send	O	G18, K19, V7	G16, J15, T5
uart5_rxd	UART Receive Data	O	J19, P17, W4, W6	H16, M17, U2, V4
uart5_txd	UART Transmit Data	O	K18, L19, R19, V4	H18, J17, M18, U1

2.3.6.7 USB

Table 2-63. USB/USB0 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
USB0_CE	USB0 PHY Charger Enable	A	T18	M15
USB0_DM	USB0 PHY DATA PLUS	A	U18	N18
USB0_DP	USB0 PHY DATA MINUS	A	U19	N17
USB0_DRVVBUS	USB0 CONTROLLER VBUS CONTROL OUTPUT	O	G16	F16
USB0_ID	USB0 PHY IDENTIFICATION (Mini-A or Mini-B Plug)	A	V19	P16
USB0_VBUS	USB0 BUS VOLTAGE	A	T19	P15

Table 2-64. USB/USB1 Signals Description

SIGNAL NAME [1]	DESCRIPTION [2]	TYPE [3]	ZCE BALL [4]	ZCZ BALL [4]
USB1_CE	USB1 PHY Charger Enable	A	NA	P18
USB1_DM	USB0 PHY DATA MINUS	A	NA	R18
USB1_DP	USB0 PHY DATA PLUS	A	NA	R17
USB1_DRVVBUS	USB0 CONTROLLER VBUS CONTROL OUTPUT	O	NA	F15
USB1_ID	USB0 PHY IDENTIFICATION (Mini-A or Mini-B Plug)	A	NA	P17
USB1_VBUS	USB0 BUS VOLTAGE	A	NA	T18

3 Electrical Characteristics

3.1 Recommended Operating Conditions

Table 3-1. Operating Performance Points (1)

OPP	VDD	ARM (A8)	DDR3	DDR2	mDDR	L3/L4
SRTurbo(2)	1.26V +/- 5%	720 MHz	303 MHz	266 MHz	200 MHz	200/100 MHz
OPP120(2)	1.2V +/- 5%	600 MHz	303 MHz	266 MHz	200 MHz	200/100 MHz
OPP100	1.1V +/- 5%	500 MHz	303 MHz	266 MHz	200 MHz	200/100 MHz
OPP50 (3)	0.95V +/- 5%	275 MHz	-	125 MHz	90 MHz	100/50 MHz

(1) Frequencies in this table indicate maximum performance for a given OPP condition.

(2) Only available on ZCZ package.

(3) DDR3 is not available on OPP50.

4 Power

4.1 Power Supplies

4.1.1 External Power Source Requirements

The following table shows the preliminary external power supply requirements for the device. The supply rail will be updated once the target power IC for the device is frozen.

Table 4-1. External Power Source Requirements

Terminal	Nominal Rating	Max/Average Current	Special Requirements
VDD_CORE (1) (3)	1.1V +/- 4%	1000 mA / 500 mA	
VDD_MPU (1) (2) (3) (6)	1.1V – 1.3V +/- 4%	1500 mA / 750 mA	
VDD_RTC	1.1V +/- 4%	10 mA	
VDDS_RTC	1.8V +/- 5%	10 mA	
VDDS_DDR	1.8V +/- 5% 1.5V +/- 5%	200 mA	
DDR_VREF	VDDS_DDR/2 +/- 1%	TBD	Per JEDEC
VDDS	1.8V +/- 5%	100 mA	
VDDSHV1(7)	1.8V +/- 5% 3.3V +/- 5%	TBD	
VDDSHV2(7)	1.8V +/- 5% 3.3V +/- 5%	TBD	
VDDSHV3(7)	1.8V +/- 5% 3.3V +/- 5%	TBD	
VDDSHV4(7)	1.8V +/- 5% 3.3V +/- 5%	TBD	
VDDSHV5(7)	1.8V +/- 5% 3.3V +/- 5%	TBD	
VDDSHV6(7)	1.8V +/- 5% 3.3V +/- 5%	TBD	
VDDS_SRAM_CORE_BG	1.8V +/- 5%	40 mA	50mV pk-pk
VDDS_SRAM_MPU_BB	1.8V +/- 5%	40 mA	50mV pk-pk
VDDS_PLL_DDR	1.8V +/- 5%	25 mA	36 mV ripple (pk-pk) @any frequency
VDDS_PLL_CORE_LCD	1.8V +/- 5%	25 mA	36 mV ripple (pk-pk) @any frequency
VDDS_PLL_MPU	1.8V +/- 5%	25 mA	
VDDS_OSC	1.8V +/- 5%	10 mA	
VDDA1P8V_USB0/1 (5)	1.8V +/- 5%	50 mA	
VDDA3P3V_USB0/1 (5)	3.3V +/- 5%	10 mA	
USB_VBUS0/1 (5)	3.3V +/- 5%	TBD	
VDDA_ADC (4)	1.8V +/- 5%	TBD	

(1) VDD_MPU and VDD_CORE are shorted on the ZCE package. Please see TBD for list of power supplies available on ZCE and ZCZ package.

(2) VDD_MPU rating is quoted is for the highest OPP.

(3) Smart Reflex (SR) for VDD_CORE and VDD_MPU only.

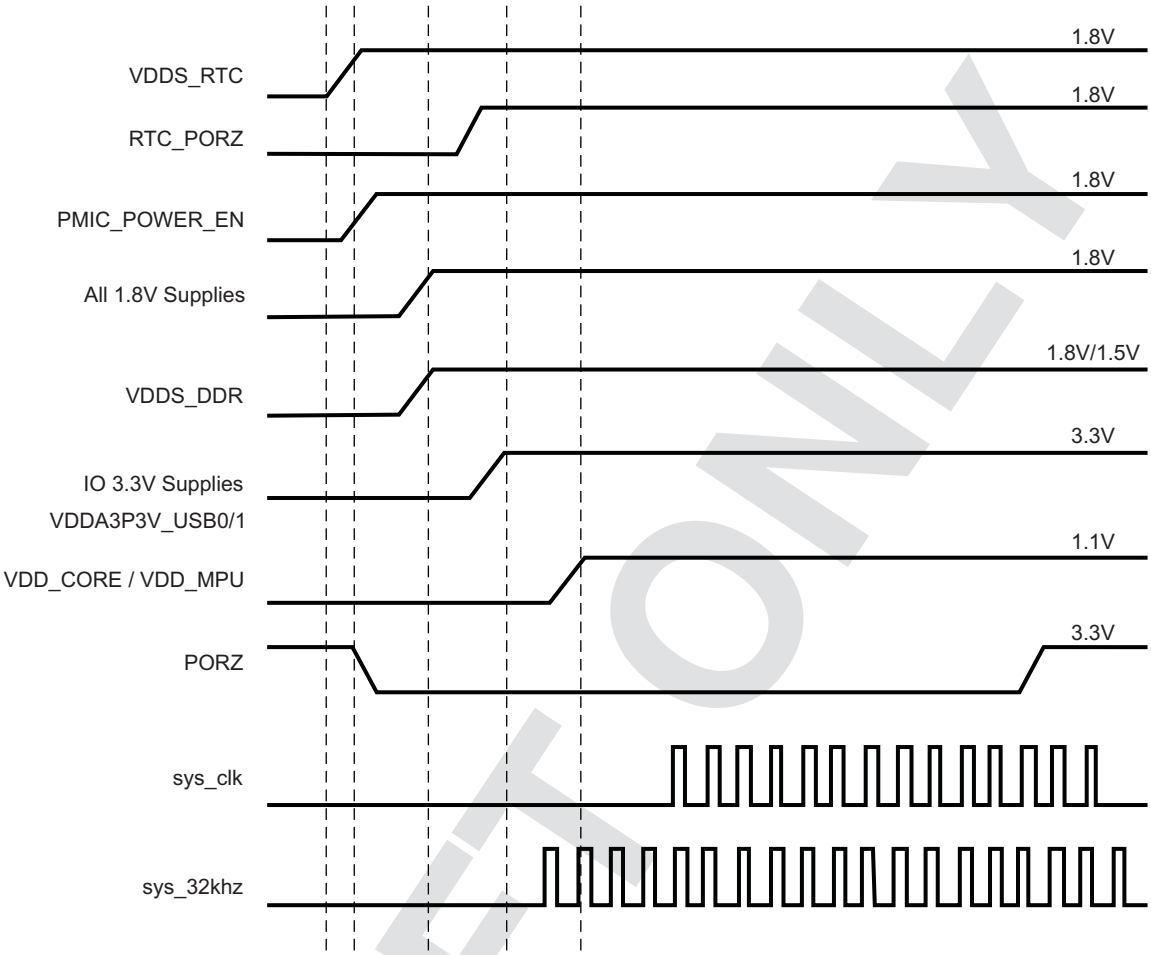
(4) Noise requirements on the Analog macros as per IP requirements.

(5) USB noise requirements – TBD.

(6) Initial values and not based off estimates. Current drawn can vary based off the exact device use conditions.

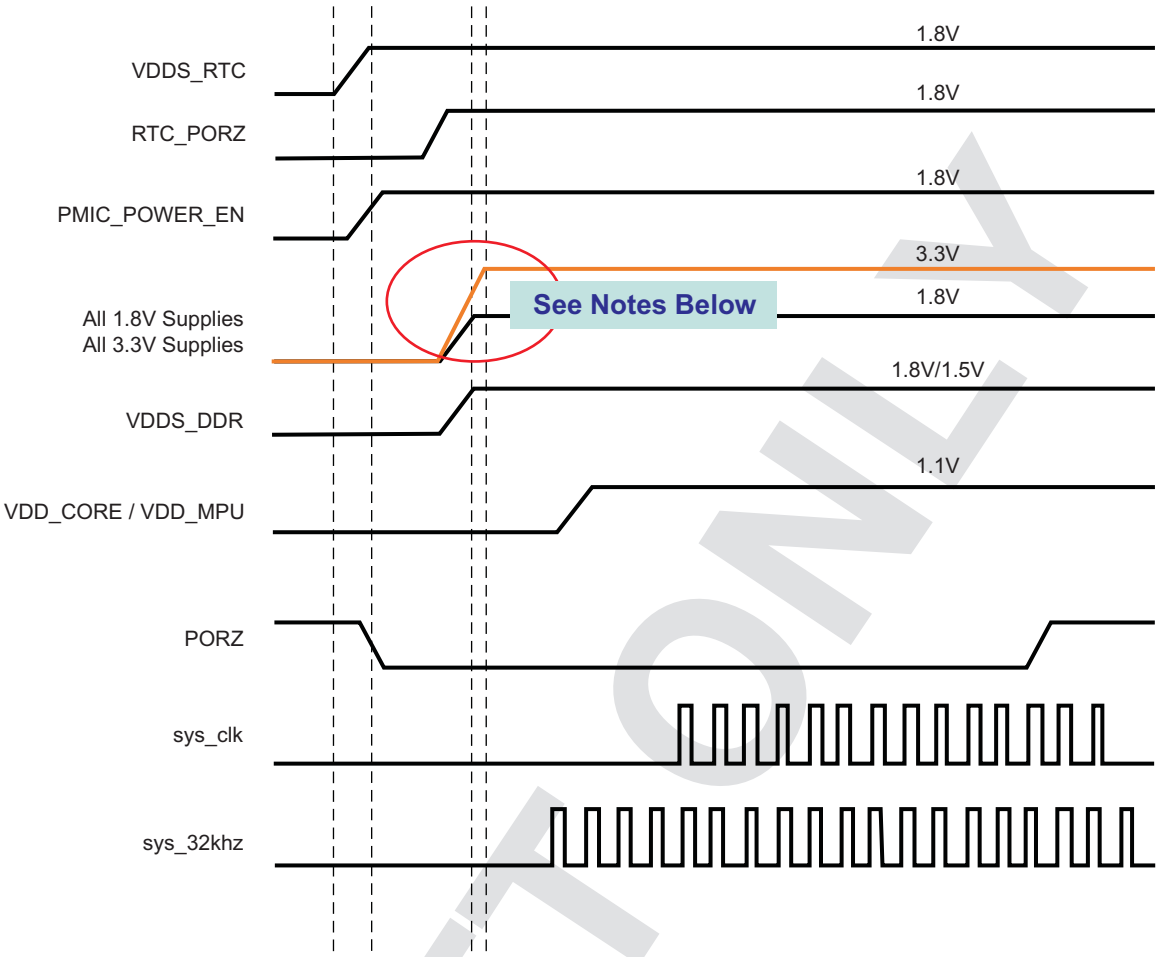
(7) VDDSHV can be either 1.8V or 3.3V depending on how whether the IO should be operated as 1.8V or 3.3V.

4.1.2 Power-Up Sequencing



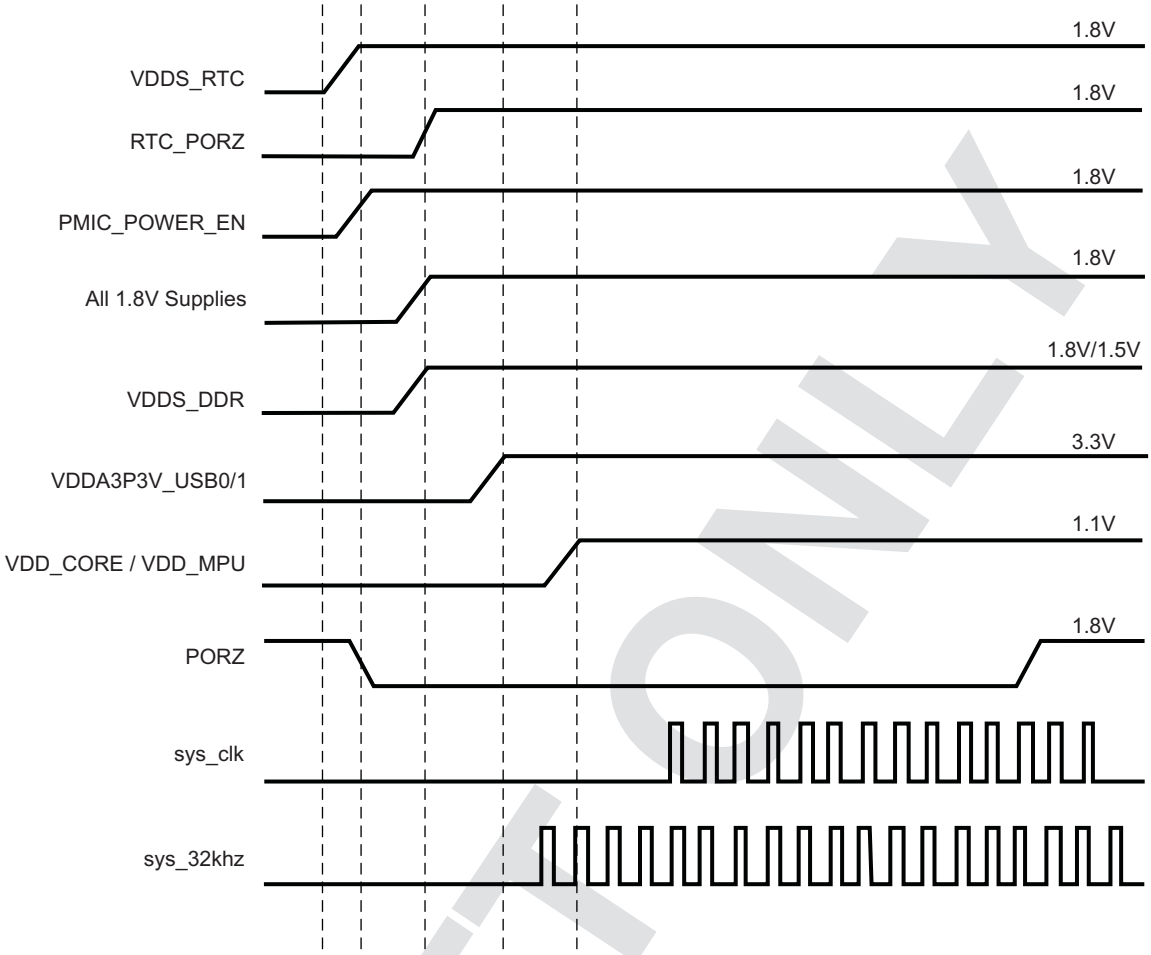
(1) RTC_PORZ should be asserted for at least 1ms and can be released before the 32KHz clock is stable.
(2) VDD_MPU and VDD_CORE can be shorted if higher OPPs are not required on VDD_MPU.
(3) If USB ports are not used, ensure the 1.8V/3.3V power pins of the USB are shorted to the 1.8V/3.3V supply available on the board. If a 3.3V supply is not available on the board, short all the 1.8V/3.3V pins to ground.
(4) If DDR2/LPDDR is planned, this supply can be ramped simultaneously with the other 1.8V I/O supplies.

Figure 4-1. Preferred Power Supply Sequencing with Dual Voltage I/Os configured as 3.3V



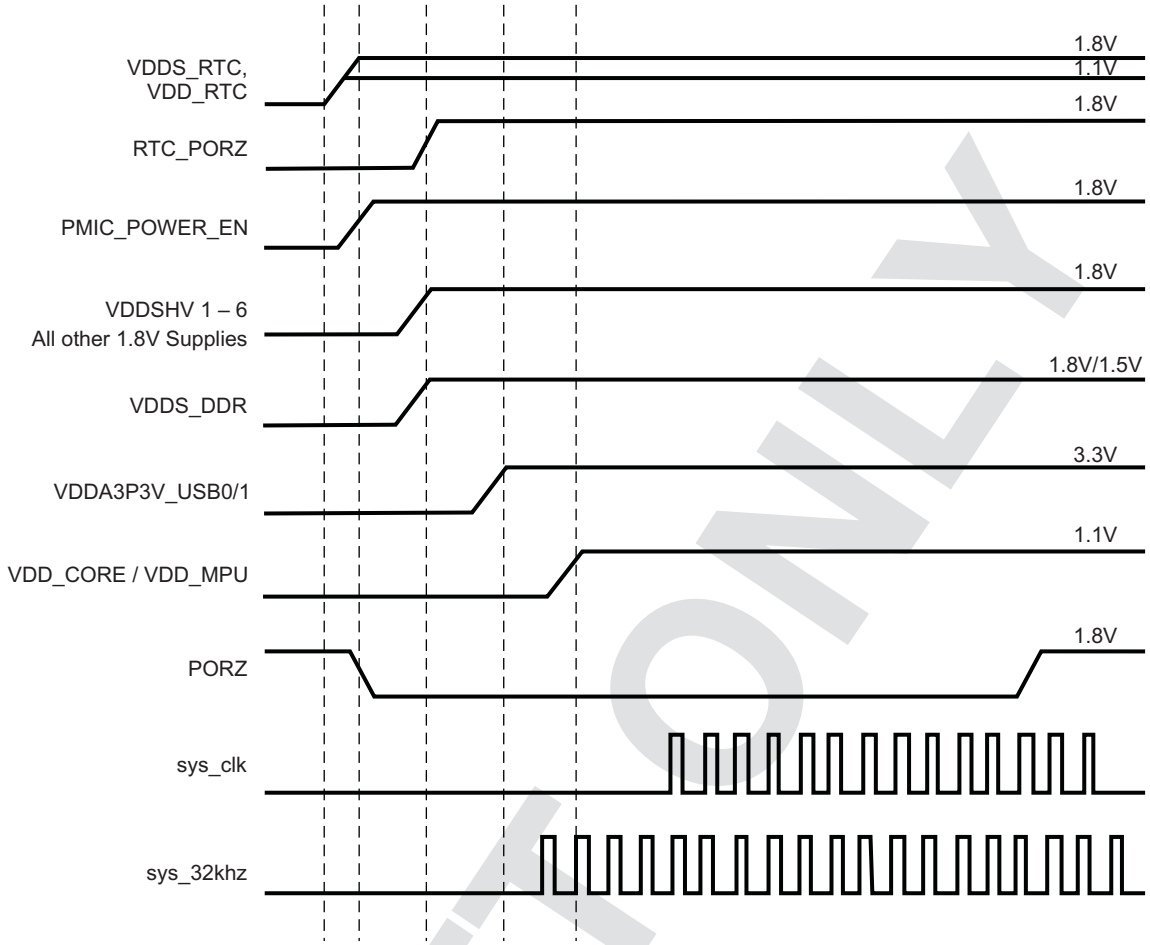
(1) RTC_PORZ should be asserted for at least 1ms and can be released before the 32KHz clock is stable.
(2) It is very important to maintain a differential of < 2V between 1.8V and 3.3V as the supplies ramp up. If this is not done, it can result in serious reliability issues.
(3) VDD_MPU and VDD_CORE can be shorted if higher OPPs are not required on VDD_MPU.
(4) If USB ports are not used, ensure the 1.8V/3.3V power pins of the USB are shorted to the 1.8V/3.3V supply available on the board. If a 3.3V supply is not available on the board, short all the 1.8V/3.3V pins to ground.
(5) If DDR2/LPDDR is planned, this supply can be ramped simultaneously with the other 1.8V I/O supplies.

Figure 4-2. Alternate Power Supply Sequencing with Dual Voltage I/Os configured as 3.3V



(1) RTC_PORZ should be asserted for at least 1ms and can be released before the 32KHz clock is stable.
(2) VDD_MPU and VDD_CORE can be shorted if higher OPPs are not required on VDD_MPU.
(3) If USB ports are not used, ensure the 1.8V/3.3V power pins of the USB are shorted to the 1.8V/3.3V supply available on the board. If a 3.3V supply is not available on the board, short all the 1.8V/3.3V pins to ground.
(4) If DDR2/LPDDR is planned, this supply can be ramped simultaneously with the other 1.8V I/O supplies.

Figure 4-3. Power Supply Sequencing with all Dual Voltage I/Os configured as 1.8V



(1) RTC_PORZ should be asserted for at least 1ms and can be released before the 32KHz clock is stable.

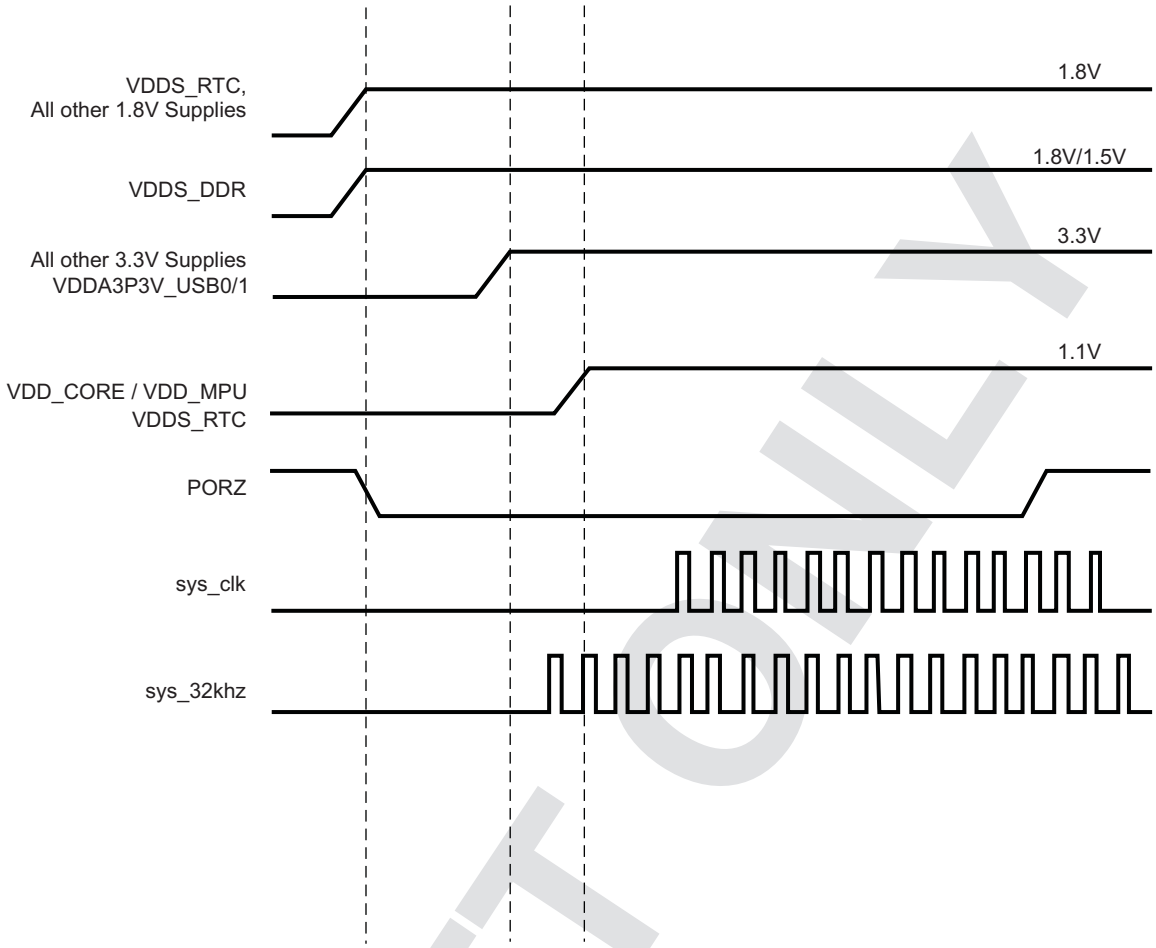
(2) If the RTC internal LDO is disabled, VDD_RTC (1.1V) should be supplied from the board. Ensure that the ENZ_KALDO_1P8V pin is shorted to VDDS_RTC on the board.

(3) VDD_MPU and VDD_CORE can be shorted if higher OPPs are not required on VDD_MPU.

(4) If USB ports are not used, ensure the 1.8V/3.3V power pins of the USB are shorted to the 1.8V/3.3V supply available on the board. If a 3.3V supply is not available on the board, short all the 1.8V/3.3V pins to ground.

(5) If DDR2/LPDDR is planned, this supply can be ramped simultaneously with the other 1.8V I/O supplies.

Figure 4-4. Power Supply Sequencing with internal RTC LDO disabled



(1) If the RTC feature is disabled, VDD_RTC (1.1V) should be supplied from the board. Ensure that the ENZ_KALDO_1P8V pin is shorted to VDDS_RTC on the board. PMIC_POWER_EN cannot be used in this case.

(2) VDD_MPU and VDD_CORE can be shorted if higher OPPs are not required on VDD_MPU.

(3) If USB ports are not used, ensure the 1.8V/3.3V power pins of the USB are shorted to the 1.8V/3.3V supply available on the board. If a 3.3V supply is not available on the board, short all the 1.8V/3.3V pins to ground.

(4) If DDR2/LPDDR is planned, this supply can be ramped simultaneously with the other 1.8V I/O supplies.

Figure 4-5. Power Supply Sequencing with RTC feature disabled

4.1.3 Power-Down Sequencing

The system is reset; sys_porz is asserted, the clock is stopped and all the power supplies are shut off.

The preferred way to sequence power down is to have all the power supplies ramped down sequentially in the exact reverse order of the power-up sequencing. In other words, the power supply that has been ramped up first should be the last one that should be ramped down. This will ensure there would be no spurious current paths during the power-down sequence.

At a minimum, ensure that the VDDS supply ramps down last after the 3.3V VDDSHVx supply is ramped down completely. If there is no 3.3V VDDSHVx supply in the system, it is recommended you ramp down VDDS last.

5 Mechanical Packaging and Orderable Information

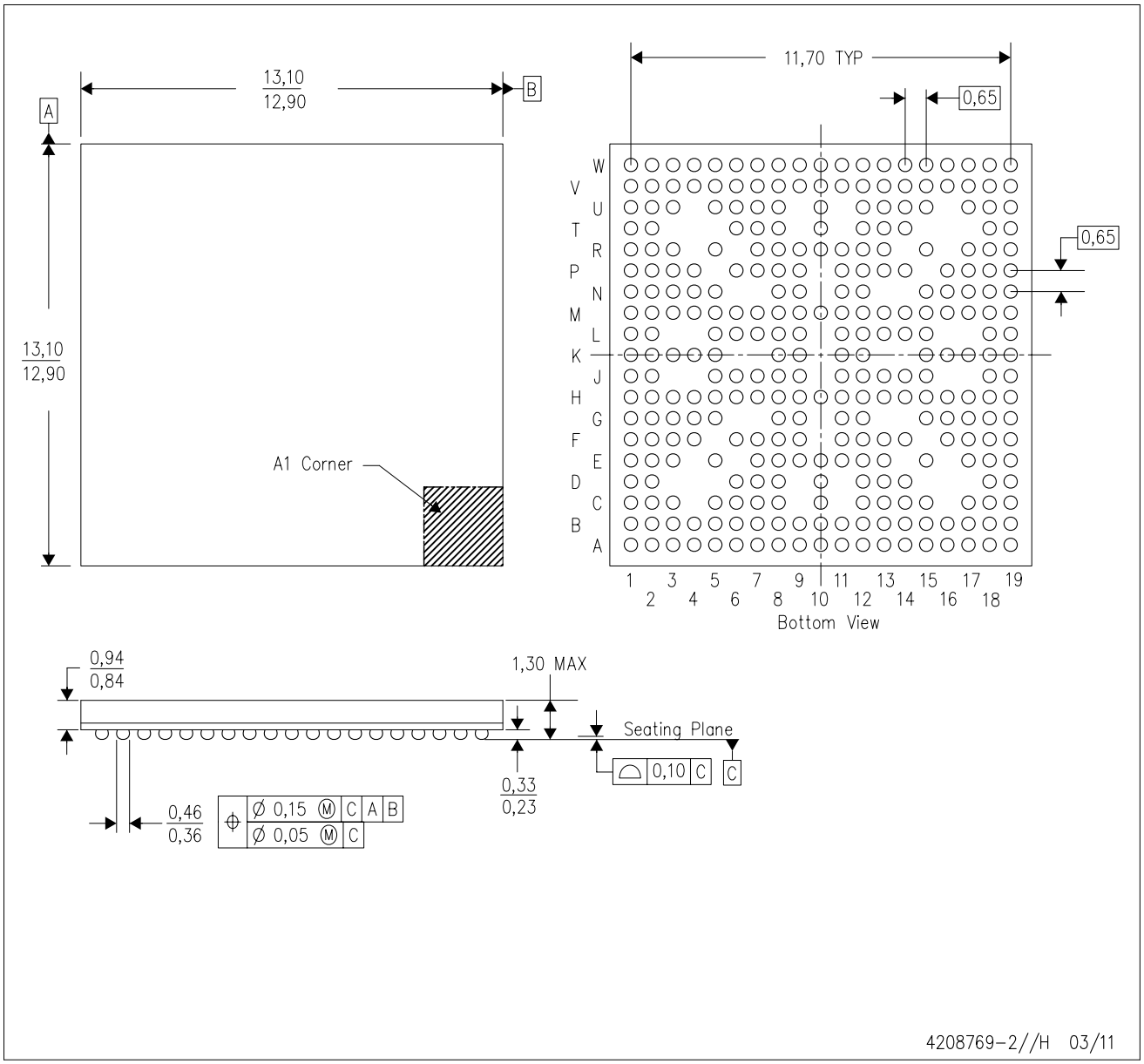
5.1 Packaging Information

The following packaging information and addendum reflect the most current data available for the designated device(s). This data is subject to change without notice and without revision of this document.

The figures below are package drawings for the ZCE and ZCZ package options.

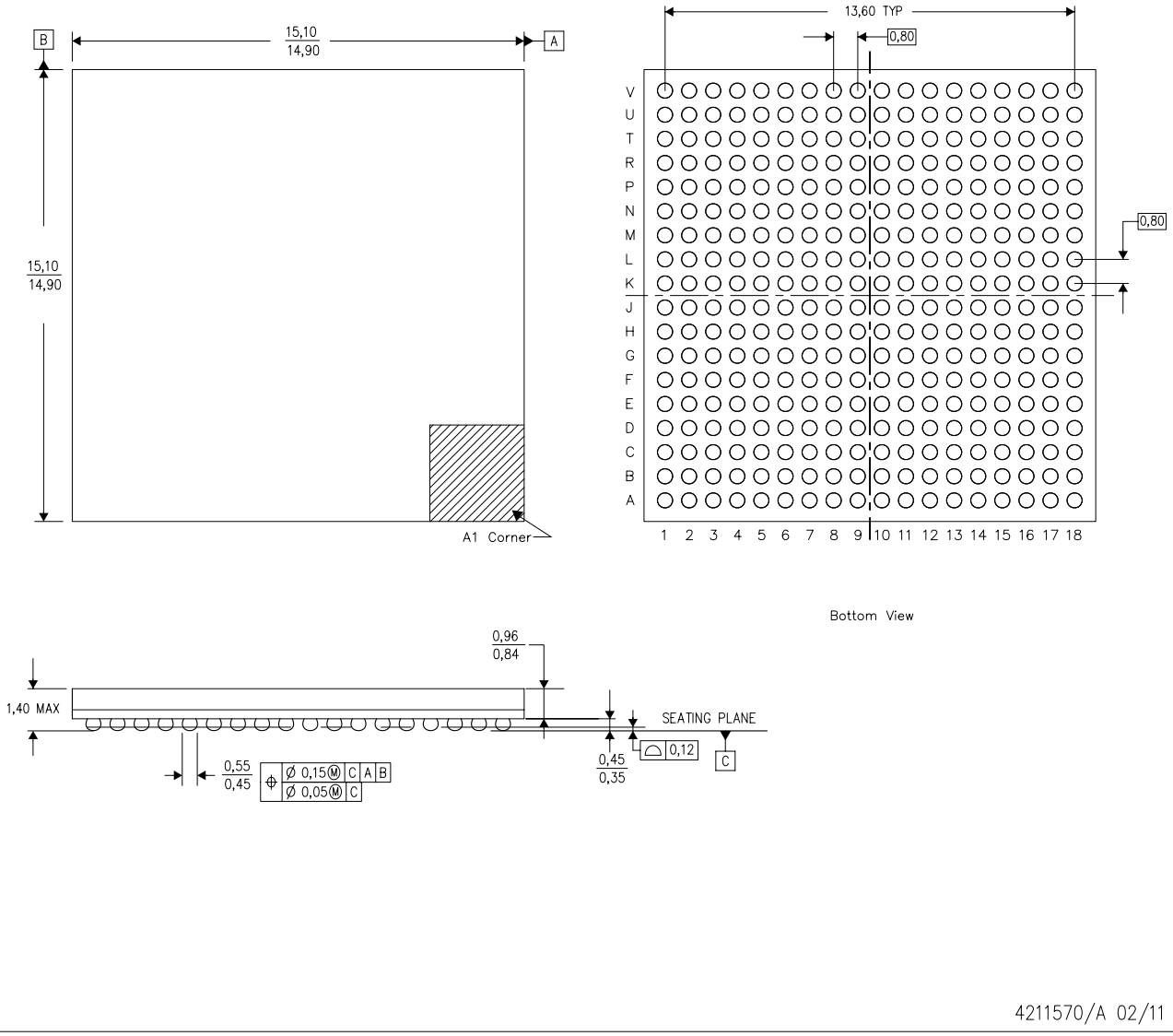
The ZCE package has been specially engineered with a new technology called Via Channel™. This allows larger than normal PCB via and trace sizes and reduced PCB signal layers to be used in a PCB design with this 0.65-mm pitch package, and will substantially reduce PCB costs. It allows PCB routing in only two signal layers (four layers total) due to the increased layer efficiency of the Via Channel™ BGA technology.

ZCE (S–PBGA–N298) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.

ZCZ (S–PBGA–N324) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a Pb–free solder ball design.

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