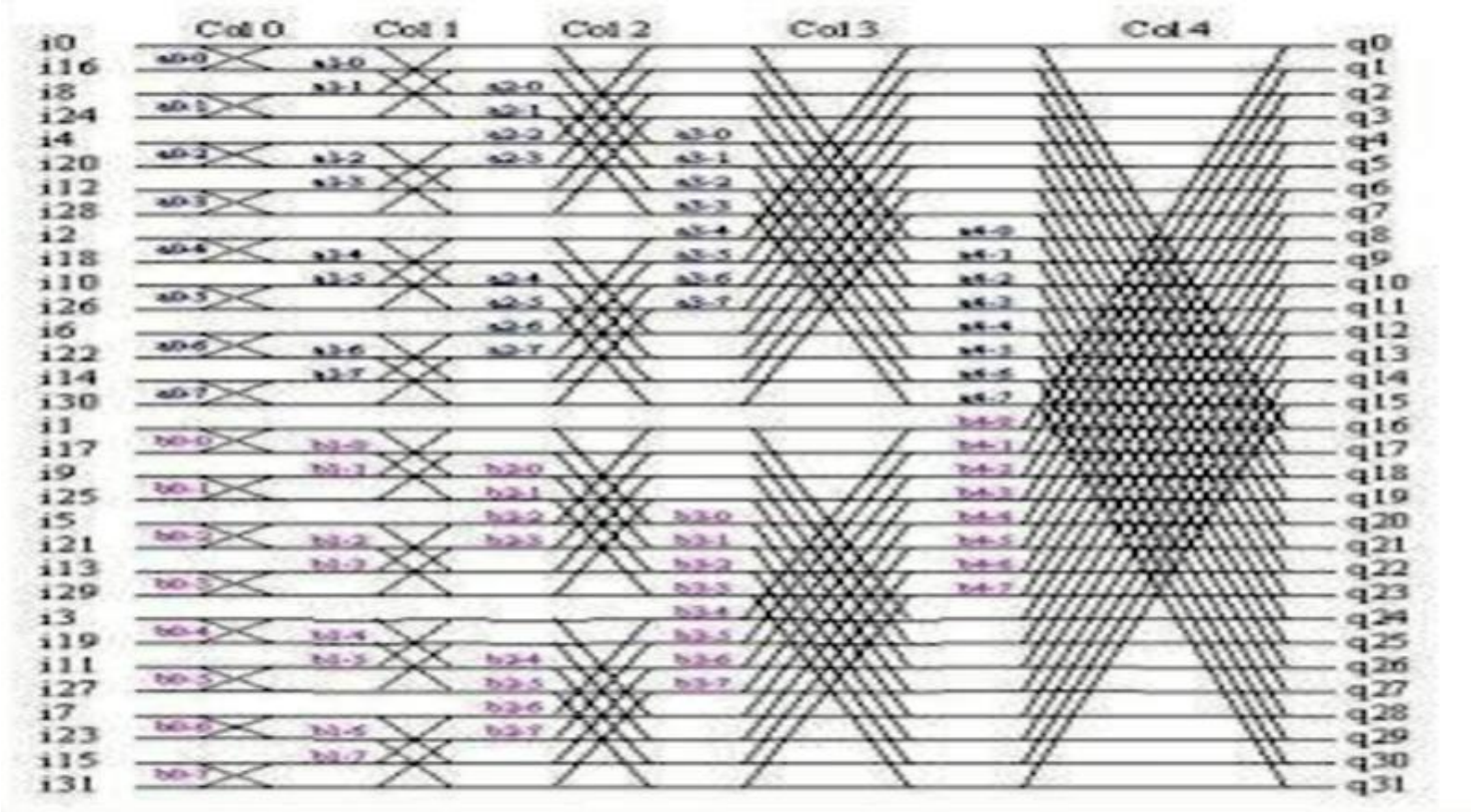
VLSI-2 project

Introduction

The problem of frequency selective channels is a significant one in wireless communications. An equalizer can be used to invert the channel and cancel the effect of channel selectivity, but it's too complex to implement if the channel is too selective. A better approach to combat selective channels Is orthogonal frequency division multiplexing (OFDM) in which the channel is divided into many small subchannels, converting the selective channel into small flat subchannels. At the transmitter, the subcarriers are modulated in frequency domain, then IFFT is used to transform this into time domain samples. At the receiver, the time domain samples are transformed back to frequency domain using FFT for further processing.

Project description

You are required to design a 32-point FFT in RTL. The Cooley-Tukey algorithm is the most used FFT algorithm, so please refer to it. To get the simplest design, use this algorithm and break down the FFT into 2-point FFT. The butterfly diagram for this is shown below:



To better understand this algorithm and the butterfly diagram, refer to the slides in the following link:

https://drive.google.com/file/d/1TuhFP-BMkrH79_ULNP4-7T09K2uaPOlO/view?usp=sharing

Try to go through the butterfly diagram for a 8-point or 16-point FFT as well as the math to get a better understanding of the algorithm.

Project requirements

- RTL design using vhdl or Verilog
- No ready-made blocks are to be used. All blocks or instances should be designed from scratch
- Pipelining must be included. Assume that the FFT block should output 20M samples per second. Place registers between columns in the butterfly diagram when necessary to meet this requirement.
- Serialization must be included. In FFT, you will find that you will need to design a multiply accumulate block (MAC) and instantiate it several times. Assume that the MAC works at a frequency of 100MHz. Re-use the MAC instances and try to reach full utilization for each instance if possible.
- Write a testbench and simulate the FFT block behaviorally
- Design must pass synthesis and function correctly in post synthesis simulation
- Information like resource usage and critical path should be extracted from synthesis report

Project assumptions

- Assume a pipelining clock with frequency 20MHz
- Assume a clock for the MAC units with frequency 100MHz
- Assume the samples input to the FFT block are output from an 8-bit ADC
- Assume input samples are real
- If you need to make any other assumption, state it clearly in the project report

Project notes

- Project is worth 25 points
- Since you worked with Xilinx and Altera tools in last semester's lab, you can use one of them since you will be already familiar with them. However, if you wish to use any other tool, it's okay
- Project should be done in teams of 2-3 students
- It would be better to draw a block diagram for the FFT block before writing the model to get a better picture of the design

Project deliverables

- Project report with names, bench numbers, and section number of students in each team on the first page
- Screenshots for the project requirements like pre & post synthesis simulations in the report
- If block diagram is drawn for the design, include it in the report
- Report should be submitted in pdf format
- Code for the design should be included in separate files

Project deadline

Project should be delivered on the course blackboard