

v8::bigint::ProcessorImpl  
::Divide

v8::bigint::ProcessorImpl  
::Modulo

v8::bigint::ProcessorImpl  
::DivideBurnikelZiegler

```
graph LR; A[v8::bigint::ProcessorImpl::Divide] --> C[v8::bigint::ProcessorImpl::DivideBurnikelZiegler]; B[v8::bigint::ProcessorImpl::Modulo] --> C;
```