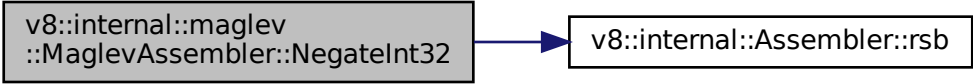


v8::internal::maglev
::MaglevAssembler::NegateInt32



```
graph LR; A["v8::internal::maglev  
::MaglevAssembler::NegateInt32"] --> B["v8::internal::Assembler::rsb"]
```

v8::internal::Assembler::rsb