

v8::internal::RegExpBytecode
Generator::CheckBitInTable

v8::internal::RegExpBytecode
Generator::SkipUntilBitInTable

v8::internal::RegExpBytecode
Generator::EmitSkipTable

```
graph LR; A[v8::internal::RegExpBytecodeGenerator::CheckBitInTable] --> C[v8::internal::RegExpBytecodeGenerator::EmitSkipTable]; B[v8::internal::RegExpBytecodeGenerator::SkipUntilBitInTable] --> C;
```

The diagram illustrates a code transformation or inlining process. On the left, two white rectangular boxes represent source functions: 'v8::internal::RegExpBytecode Generator::CheckBitInTable' (top) and 'v8::internal::RegExpBytecode Generator::SkipUntilBitInTable' (bottom). On the right, a gray rectangular box represents the target function: 'v8::internal::RegExpBytecode Generator::EmitSkipTable'. Two blue arrows point from the right side of each source box to the left side of the target box, indicating that the logic of both source functions is being moved into or replaced by the target function.