

v8::internal::compiler  
::RepresentationSelector  
::VisitNode

v8::internal::compiler  
::RepresentationSelector  
::VisitSpeculativeInt32Binop

v8::internal::compiler  
::RepresentationSelector  
::VisitSpeculativeNumberModulus

v8::internal::compiler  
::RepresentationSelector  
::VisitSpeculativeSmallIntegerAdditiveOp

v8::internal::compiler  
::anonymous\_namespace  
{simplified-lowering::cc}  
::CheckedUseInfoAsWord32FromHint

```
graph LR; A["v8::internal::compiler  
::RepresentationSelector  
::VisitNode"] --> D["v8::internal::compiler  
::anonymous_namespace  
{simplified-lowering::cc}  
::CheckedUseInfoAsWord32FromHint"]; B["v8::internal::compiler  
::RepresentationSelector  
::VisitSpeculativeInt32Binop"] --> D; C["v8::internal::compiler  
::RepresentationSelector  
::VisitSpeculativeNumberModulus"] --> D; E["v8::internal::compiler  
::RepresentationSelector  
::VisitSpeculativeSmallIntegerAdditiveOp"] --> D;
```

The diagram illustrates a mapping from four source nodes to a single target node. The source nodes are arranged vertically on the left, and the target node is on the right. Blue arrows point from each source node to the target node. The target node is shaded gray, while the source nodes are white with black borders.