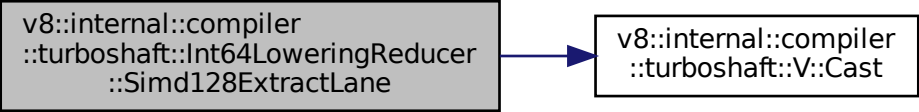


v8::internal::compiler  
::turbohaft::Int64LoweringReducer  
::Simd128ExtractLane



```
graph LR; A["v8::internal::compiler  
::turbohaft::Int64LoweringReducer  
::Simd128ExtractLane"] --> B["v8::internal::compiler  
::turbohaft::V::Cast"]
```

v8::internal::compiler  
::turbohaft::V::Cast