INDEX TO ECE 3210 Mircoelectronic Circuits

Download Word Document with the first set of notes, syllabus, and Design project 1

ECE 3210 - 3: Electronics I

Instructor: Professor J. Alspector, x3510, josh@eas.uccs.edu

Office hours: Mon. and Wed. 12:30 - 1:30 pm in EN 294

Classes: Mon. and Wed. 1:40 - 2:55 pm in EN 233 (Multimedia Education Lab)

Text: Sedra and Smith - Microelectronic Circuits (Fourth Edition)

Additional materials: Project descriptions, computerized class notes, P-Spice files

Software: P-Spice, (Rendezvous and RealAudio for distance learning mode)

Prerequisites: ECE 2210 - 3. Circuit Analysis I

Grading components: a) Homework (~20%) b) 3 class projects (~30%) c) 3 exams and final (~50%)

Syllabus: Weekly topics (approximate)

1. Introduction and review of Kirchoff's laws, signals, frequency spectrum, amplifiers
2. Ideal operational amplifiers and circuits
3. Realistic models and circuits using Op Amps, SPICE Intro
4. Asign design project 1, ideal diodes and circuits
5. Rectifiers, clamping circuits, semiconductor diode physics
6. Course questionnaire, quiz 1, design project 1 due
7. Bipolar junction transistors, device physics, models, characteristics
8. Transistor amplifiers, design techniques
9. Single stage amplifiers, switching circuits, second order effects
10. Quiz 2, design project 2
11. Field effect transistors, device physics, characteristics
12. DC analysis, FET amplifiers, single stage amplifier configurations
13. Quiz 3, design project 3
14. IC MOS amplifier, FET switches, CMOS logic
15. Review, final exam

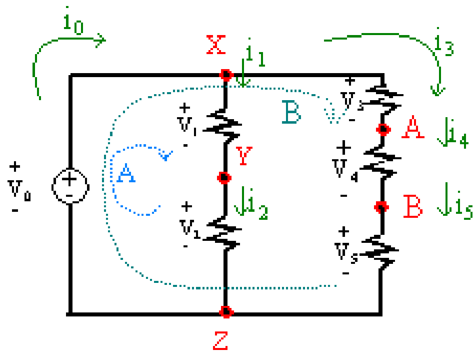
Kirchoff's Laws

Voltage

$$\sum_{loop} \Delta v = 0$$

Current

$$\sum_{node} i = 0$$



KVL

$V_0 = V_1 + V_2 = V_3 + V_4 + V_5$

Sum of voltages between any two nodes is the same regardless of path

KCL

$i_0 = i_1 + i_3$ at x

$i_1 = i_2$ at y

$i_3 = i_4 = i_5$ at A,B

Sum of current flowing into a node equal sum flowing out of a node

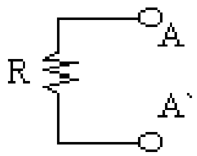
Q:

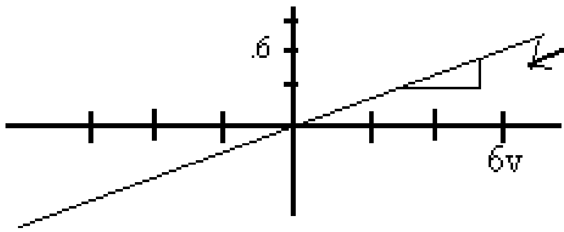
Does arrow direction matter?

What about capacitors?

Voltage - Current (V-I) Characteristics

Resistor





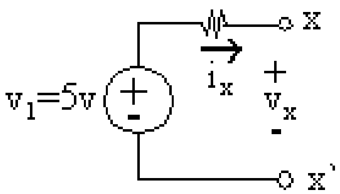
Slope = 0.1 mA/V

di / dv = 1/R

R = 10kΩ

-

Port Example – Plot V-I

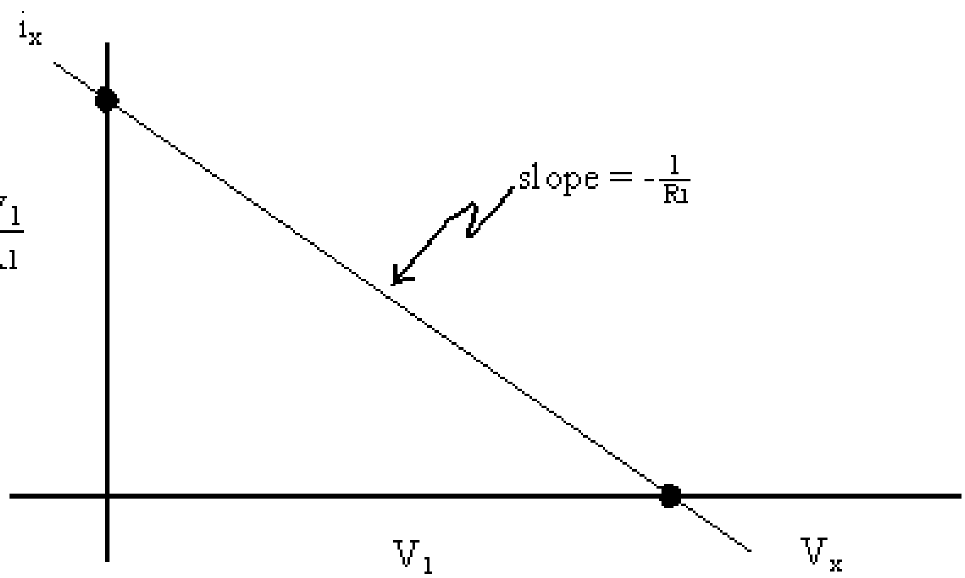


Not Passive, define i_x as positive out of x

KVL $$v_x = v_1 - i_x R_1 \Rightarrow i_x = \frac{v_1 - v_x}{R_1} = -\frac{1}{R_1} v_x + \frac{v_1}{R_1}$$

$\mathbf{v_x}$ **= intercept ($\mathbf{i_1 = 0}$)** **Slope** $\mathbf{i_x}$ **intercept**

$$\begin{pmatrix} \text{short} \\ \text{ekt} \\ \text{current} \\ v_x = 0 \end{pmatrix} \quad \frac{V_1}{R_1}$$



(Open ckt voltage)
$i_p = 0$

Superposition in Linear Circuits

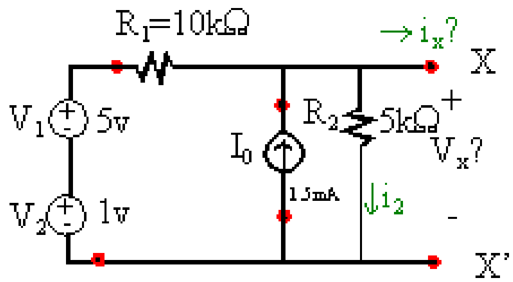
Linear Element has form

$V = ai_1 + bi_2$
or $i = cv_1 + dv_2$

(coefficient are constant or linear operators like I dt or d/dt
e.g. v=a (di_1/dt) + b I $i_2$dt)

Superposition:
Response of linear circuit to sum of inputs is sum of responses with each input applied individually
If $i_1 = f(v_1)$ and $i_2 = f(v_2)$ then $i_3 = f(v_1 + v_2) = f(v_1) + f(v_2) = i_1 + i_2$

Example:
Plot V-I



v_1 : set $v_2 = 0$ (short) and $I_0 = 0$ (open)

$$v_x' = R_2 i_2 = R_2 \frac{v_1}{R_1 + R_2} = 5k\Omega \frac{5v}{10k\Omega + 5k\Omega} = 1.67v$$

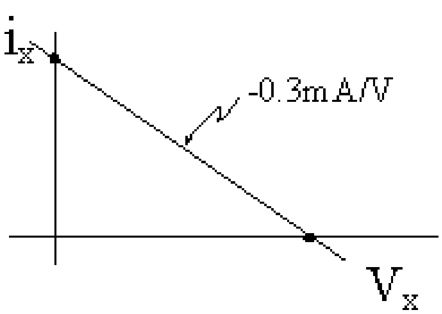
v_2 : $$v_x'' = R_2 i_2 = R_1 \frac{v_2}{R_1 + R_2} = 0.33v$$

v_2 : $$v''' = I_0(R_1 \parallel R_2) = 1.5mA(10m\Omega \parallel 5m) = 5V$$

By superposition: $v_x = v_x' + v_x'' + v_x''' = 1.67 + 0.33 + 5v =$ **7v** for no load (open ckt at x x')

Short ckt xx':

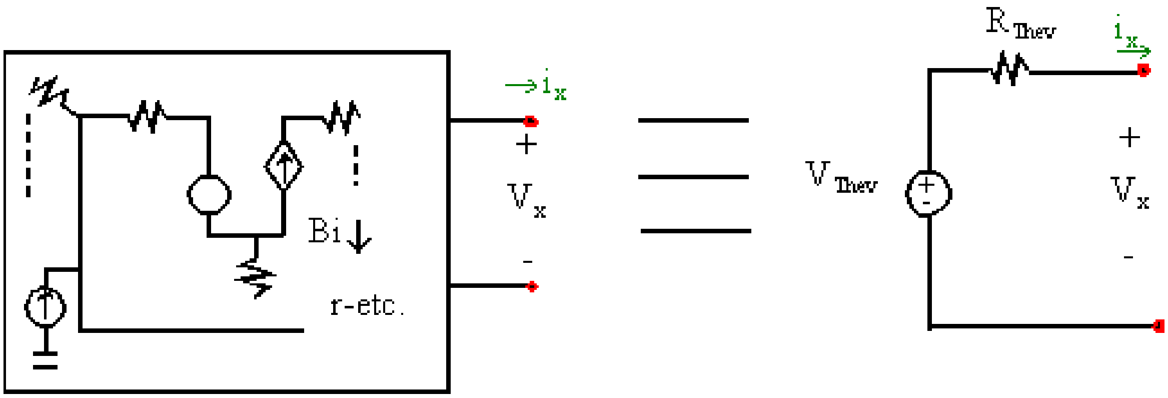
$$i_{sc} = i_x\Big|_{v_x=0} = I_0 + \frac{v_1 + v_2}{R_1} = 1.5mA + \frac{5v + 1v}{10m\Omega} = 2.1mA$$



Slope = $$-\frac{2.1mA}{7V} = -0.3\frac{mA}{V}$$

ANS: $$i_x = -0.3\frac{mA}{V}V_x + 2.1mA$$

Thevenin Equivalent Circuits



Any port of resistive ckt (resistors + linear sources) can be modeled by a voltage source and resistor

Find open circuit voltage V_{0c} at port. This is V_{thev}

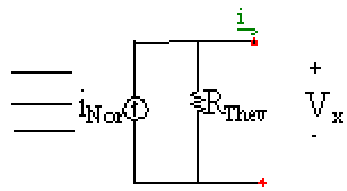
Find short-circuit current i_{sc} by connecting a short at port. $R_{thev} = V_{thev} / i_{sc}$

Applies also to capacitors and inductors with ac signals

$$\vec{z}_c = \frac{1}{jwc} \qquad \vec{z}_l = \frac{1}{jwL}$$

Norton Equivalent

is "dual" of Thevenin



$V_{oc} = I_{Nor}\, R_{thor}$

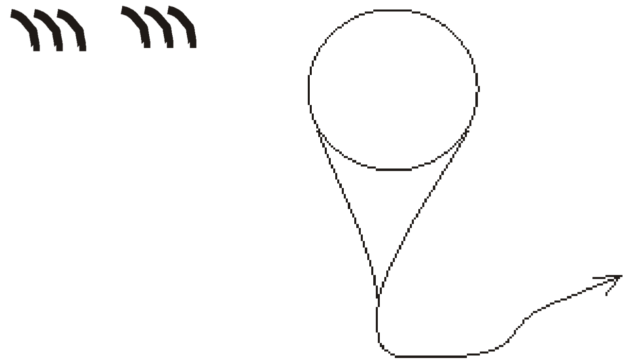
$i_{sc} = i_{nor}$

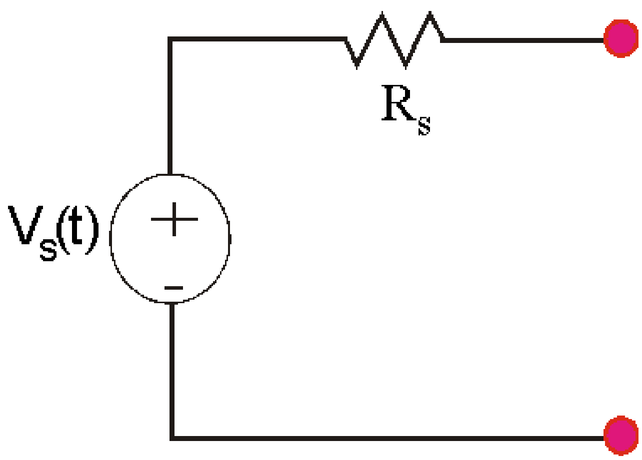
Resistance looking into port (open ckt current source) is R_{thev}

Review (Chapter 1 Sedra/Smith)

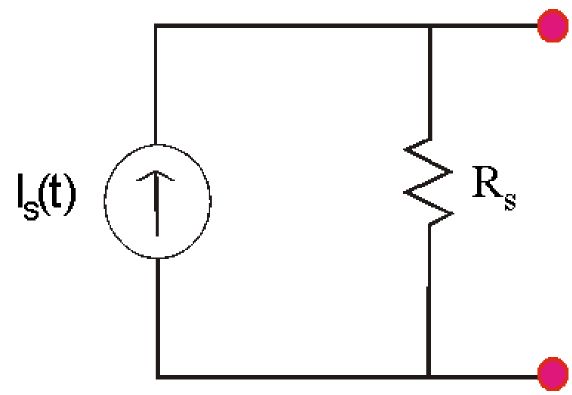
- Microelectronic Technology – 1 Cs 10^7-10^8 devise / 1 cm^2 chip

  - Signals Transducers





Thevenin form
(preferred for R_s low)



Norton Form
(preferred for R_s high)

- Frequency domain

$$v(t) = V \sin \pi t$$

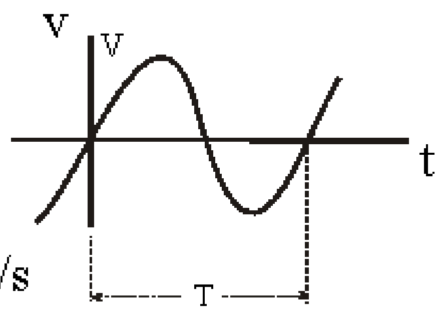
peak

$\wedge$

$2\pi f$ rad/s

$\frac{1}{T}$ Hz

period

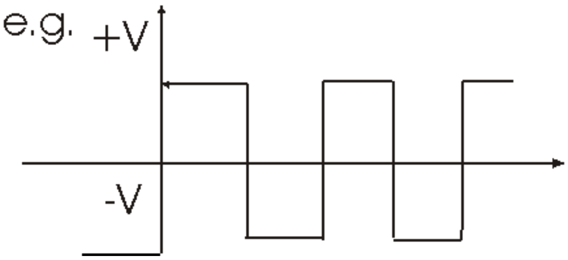


$$V_{rms} = \frac{V}{\sqrt{2}}$$

- sine wave

Fourier Transform

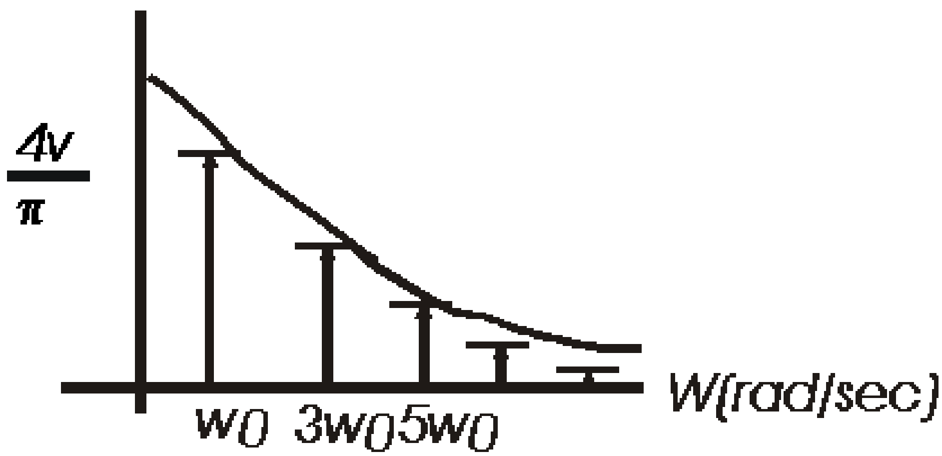
- Fourier series – any periodic function can be expressed as a sum of sines (possibly infinite series)



$$v(t) = \frac{4v}{\pi}\left(\sin wot + \tfrac{1}{3}\sin 3wot + \tfrac{1}{5}\sin 5wot + \ldots\right)$$

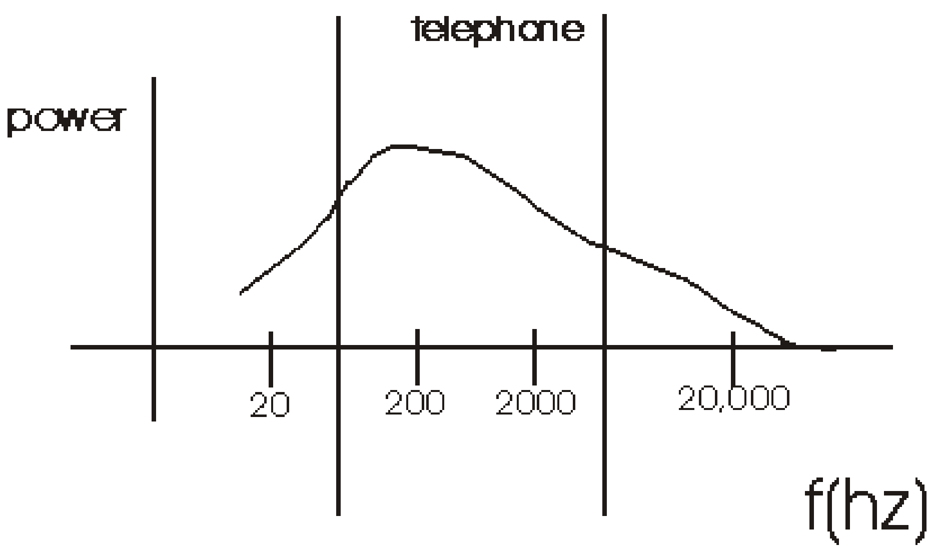
fundamental harmonics

- Frequency spectrum



- useful because spectrum has major components in small region of freq. space.

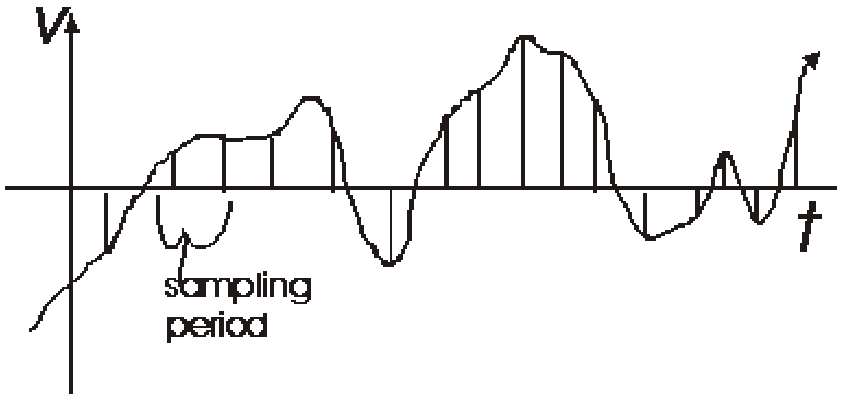
- Non-periodic sound – e.g. speech



Exercise 1.1-1.3

Signal Processing

- Analog & Digital Signals



- natural signals are analog

- analog circuits processing
  advantage in that signals analogous
  to real world

- sample the amplitude periodically
  -> discrete time signal

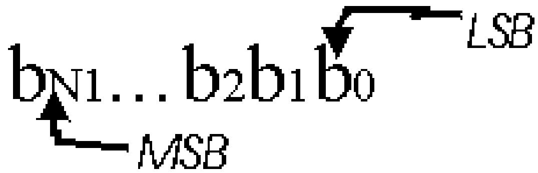
- sequence of numbers -> digital
  signal

- advantage of digital
  - Processed by digital computer-type circuits
  - Flexible

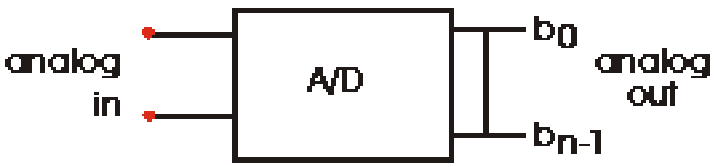
- Amplifiers (analog processing)
- why? Microphone (microvolts) -> speakers (amps)
  linearity – so signal is not distorted

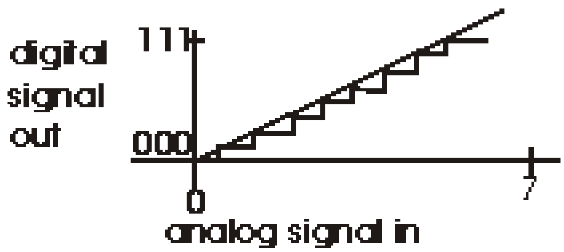
Digital Signal Processing

- Each sample is binary word



with value $D = b_0 2^0 + b_1 2^1 + \ldots + b_{n-1} 2^{n-1}$





- ADC quantizes signal into one of 2^n levels

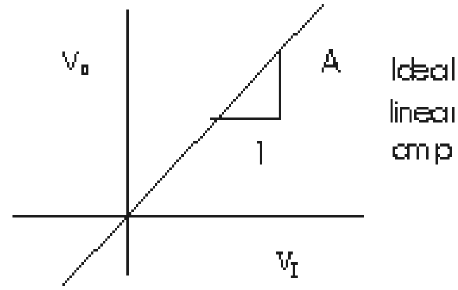
ex 1.4

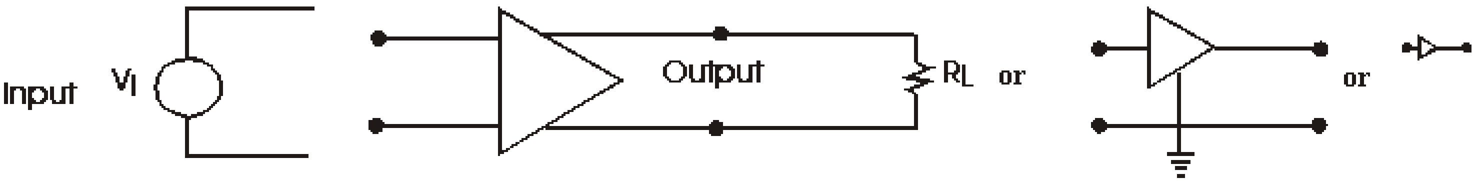
Amplifiers

- Voltage amp

$$V_0(t) = A_v V_I(t)$$

gain





Voltage gain $\quad A_v \equiv \dfrac{V_0}{V_I}$ (transformer)

Power gain $\quad A_p \equiv \dfrac{LoadPower(P_L)}{InputPower(P_I)} = \dfrac{V_0 I_0}{V_I I_I}$

Current gain $\quad A_i \equiv \dfrac{I_0}{I_I}$ N.B. $A_p = A_v A_I$

- Logarithmic measure – decibels

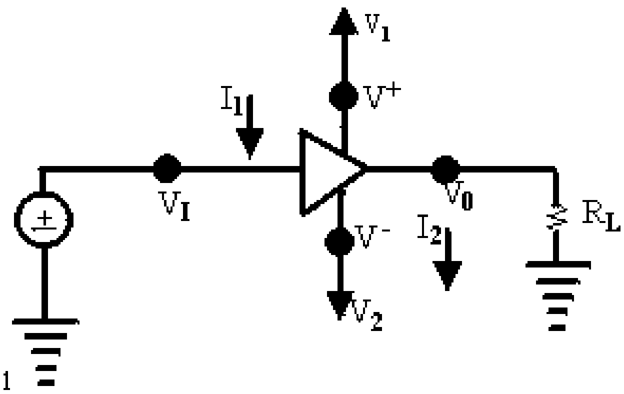
$20 \log_{10} |A_v| \leftarrow$ to remove phase shift

$20 \log_{10} |A_i|$ N.B. $-20 \rightarrow A_v = 0.1$

$10 \log_{10} A_p$ (power is i^2 or v^2)

Power Supply, Biasing, Saturation

Supply



e.g. 1.1

$$P_{dc} = V_1I_1 + V_2I_2$$

Power balance:

$$P_{dc} + \underbrace{P_I}_{\text{small}} = \underbrace{P_L}_{\text{power delivered}} + P_{\text{dissipated(in amp)}}$$

Efficiency : $\eta \equiv \frac{P_L}{P_{dc}} \times 100 \text{ (in percent)}$, $P_{dc} \approx P_L + P_{dissipated}$ (in percent)

Saturation – Non- linearity

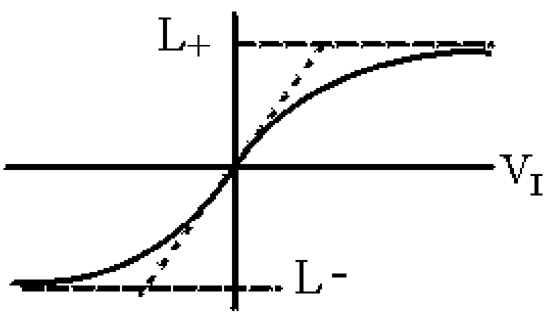
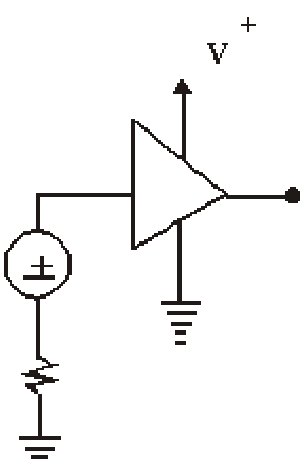


fig 1.13

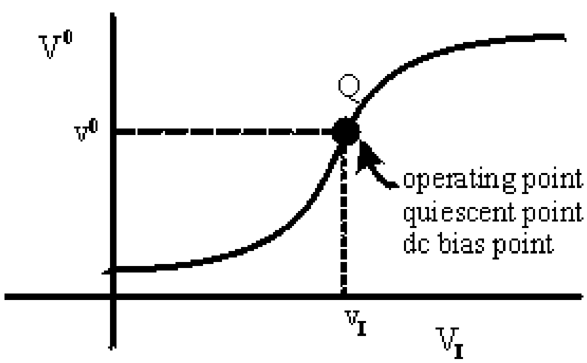
Output voltage doesn't usually exceed supply voltage

Linear range: $\frac{L_-}{A_v} \leq V_i \leq \frac{L_+}{A_v}$

Bias



Single bias input with V_s to operate in linear region



$V_I(t) = V_I + V_i(t)$

$V_0(t) = V_0 + V_0(t)$

$V_0(t) = A_v V_i(t)$

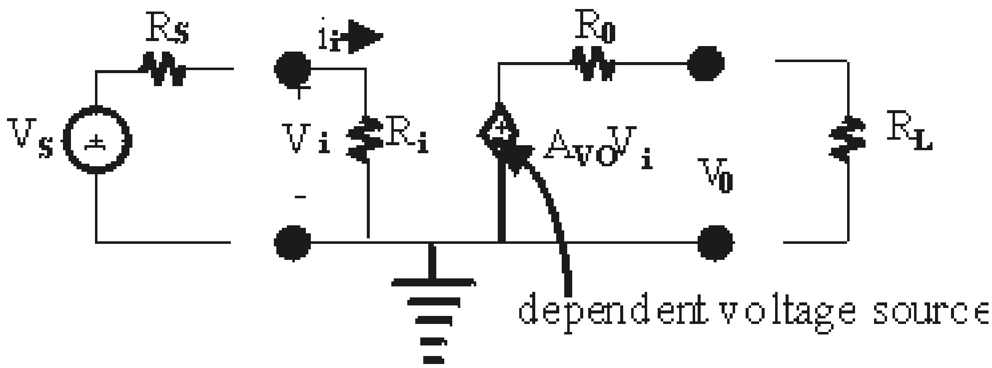
$$A_v = \left.\frac{dV_0}{dV_I}\right|_{at\,0}$$

e.g. 1.12

ex 1.5, 1.6, 1.7

Circuit Models for Amplifiers

Voltage Amp



$$V_0 = A_{v0} V_i \frac{R_L}{R_L + R_0}$$

want $R_0 << R_L$

$$A_v \equiv \frac{V_0}{V_i} = A_{v0} \frac{R_L}{R_L + R_0}$$

$\uparrow$ open circuit voltage gain ($R_L = \infty$)

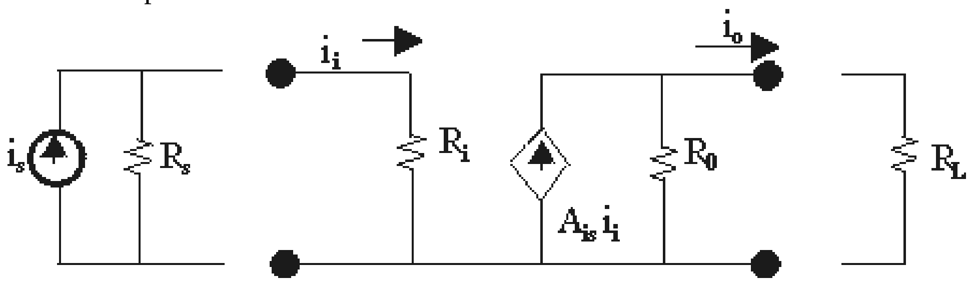
$$V_i = V_3 \frac{V_3}{R_i + R_S} \quad \text{want } R_i >> R_S$$

e.g. 1.3: 3 stage amp

ex 1.3, 1.9, 1.10

<u>Other Amplifer Models</u>

Current amp



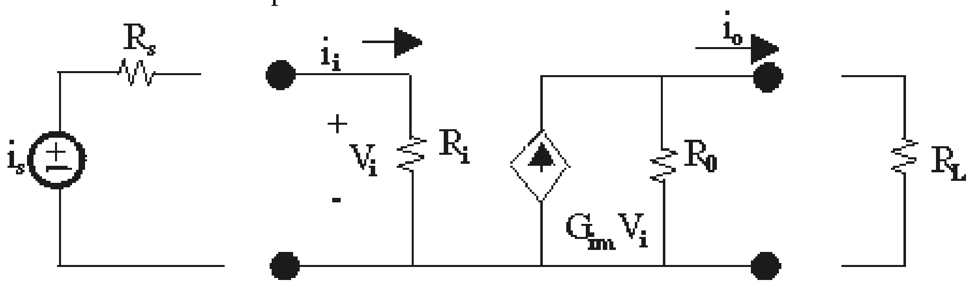
$$i_o = A_{is} i_i \frac{R_0}{R_0 + R_L}$$

$$A_i \equiv \frac{i_0}{i_i} = A_{is} \frac{R_0}{R_0 + R_L} \quad \text{want } R_0 << R_L$$

↑short circuit current gain ($R_L = 0$)

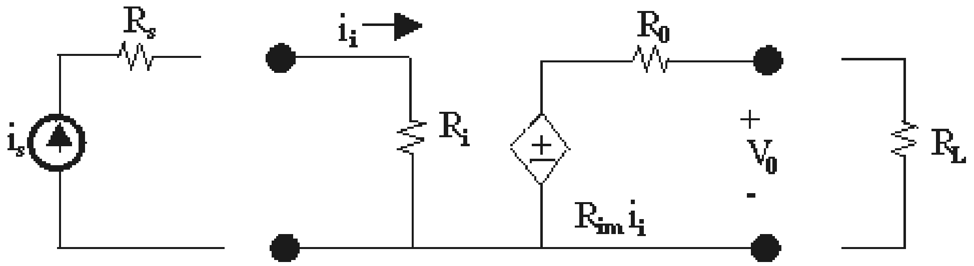
$$i_i = i_3 \frac{R_S}{R_S + R_i} \quad \text{want } R_i << R_3$$

Transconductance amp



Gm is short circuit transconductance (mhos A/V)

Transresistance (or trans impedance) amp



R_m is open circuit transresistance (ohms V/A)

Input R: apply V_S , measure i_i

Output R: apply V_i, V_x to output, measure i_x

Note that all these models are related (and unidirectional lateral)

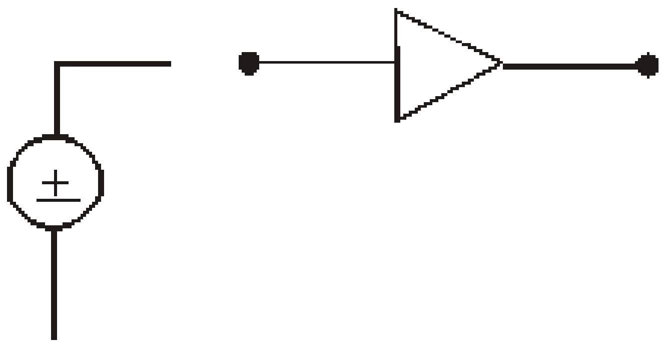
$$A_{v0} V_i = A_{is}\left(\frac{V_i}{R_i}\right) R_0 \rightarrow A_{v0} = A_{is} \frac{R_0}{R_i}$$

show $A_{v0} = G_m R_0$, Av0 = Rm/Ri ; e.g. 1.4 BJT;

Frequency Response of Amplifiers

Transfer function

$v_i = v_i \sin(wt)$



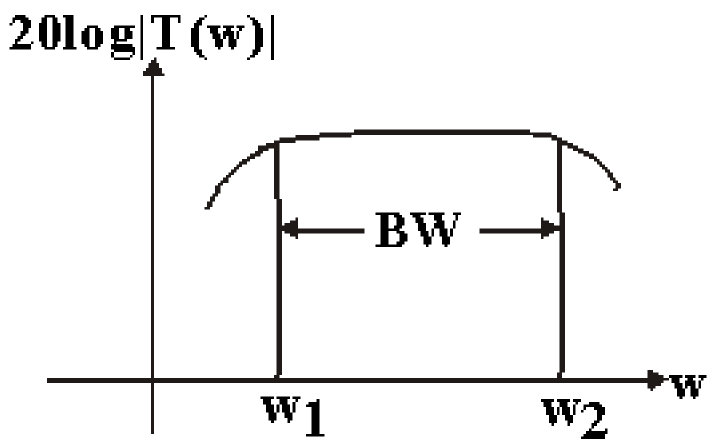
$v_0 = v_0 \sin(wt + \phi)$

Amplitude response $|T(w)| = \frac{V_0}{V_i}$

$$T(w) = \frac{V_0(w)}{V_i(w)}$$

Phase response $\angle T(w) = \phi$

Bandwidth



Complex frequency variables (includes both amplitude and phase)

Reactive components: Inductance L has impedance jwL or sL

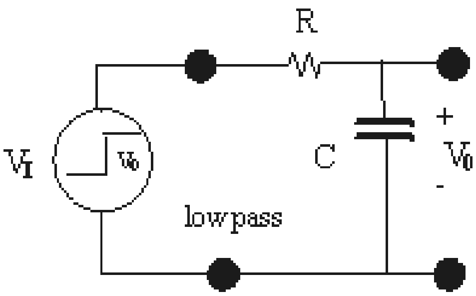
Capacitance C has impedance 1/jwC or 1/sC

T(w) is a complex function

$T(s) \equiv \frac{V_0(s)}{V_i(s)}$: replace s by jw to get physical frequencies

STC (single time constant) R-C circuits

Step response

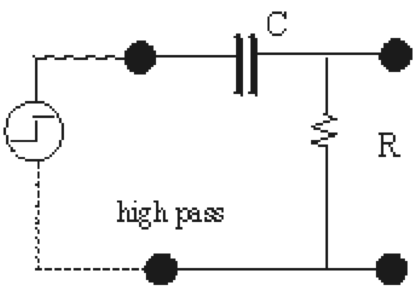


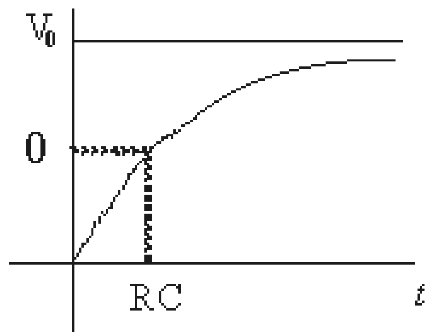
$$V_0(t=0)=0,\ V_0(t=\infty)=V_0$$

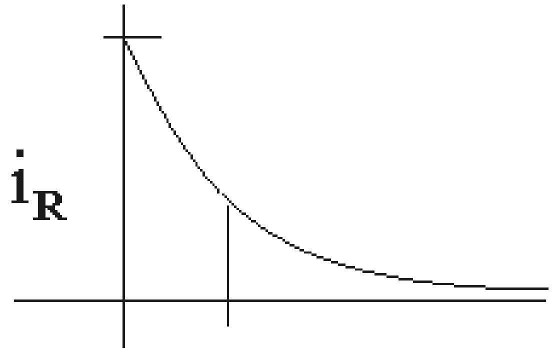
$$V_0(t)=V_0(1-e^{-t/RC})$$

$$i_R=\frac{V_I-V_0}{R}=\frac{V_0}{R}e^{-t/RC}$$

$$V_0=i_R R=V_0e^{-t/RC}$$







Sinusoidal Steady State

$$V_C(t)=R_e\left[\vec{v}ce^{jwt}\right]\ (\Leftarrow \text{phasor magnitude \& phase})$$

Capacitor eq. $\dfrac{dv_c}{dt}=\dfrac{i_c}{c}$ becomes $jw\vec{V}_c=\dfrac{\vec{I}_c}{C}$

Impedance $\vec{Z}_c=\dfrac{\vec{V}_c}{\vec{I}_c}=\dfrac{1}{jwC}$ (= jwL for inductor)

(= R for resistor)

Low pass

$$\vec{V}_0=\vec{V}_I\frac{\vec{Z}_C}{\vec{Z}_C+Z_R}=V_I\frac{\frac{1}{2}WC}{\frac{1}{2}WC+R}=\vec{V}_I\frac{1}{1+jwRC}$$

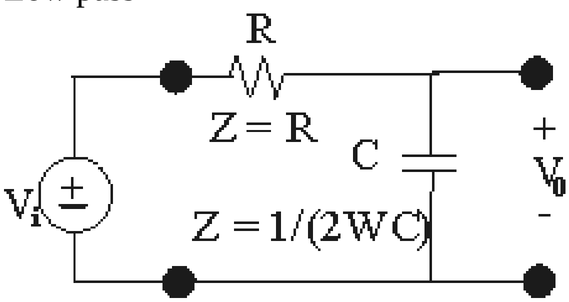
$$\left(\text{low pass response } \frac{K}{1+j\frac{w}{w_0}}\right)$$

magnitude: $\left|\dfrac{\vec{V}_0}{\vec{V}_I}\right|=\dfrac{1}{\left[1+(wRC)^2\right]^{1/2}}$ phase $\measuredangle\vec{V}_0=-\tan^{-1}wRC$

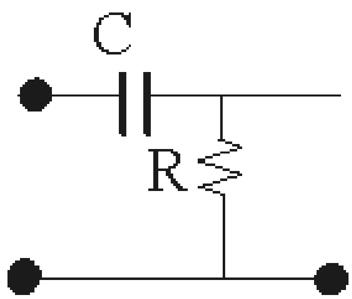
Single – time – constant Networks

STC nets: reduced to 1 reactive component and 1 resistance

Low pass



High Pass

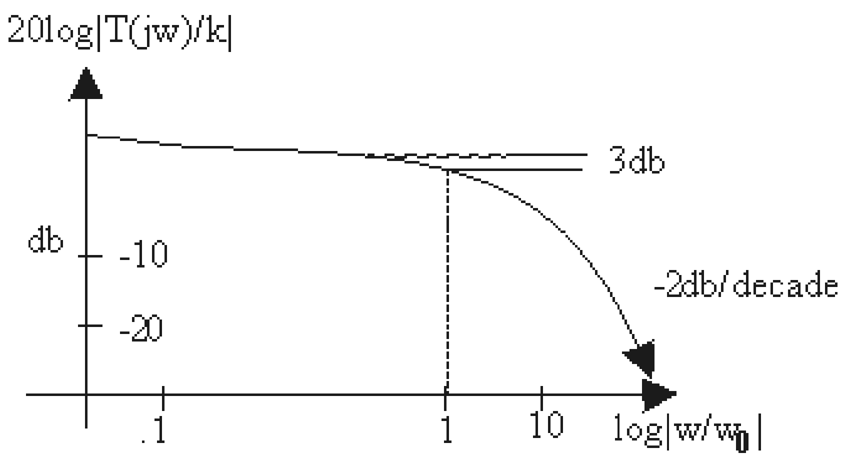


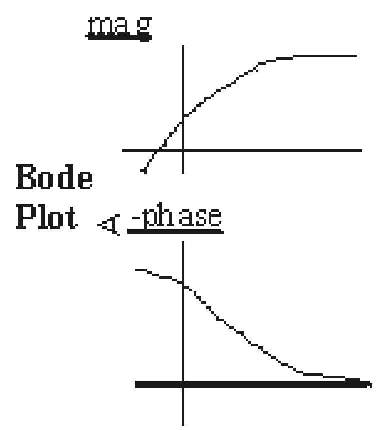
$$\left|\frac{V_0}{V_s}\right| = \frac{wRC}{\left[1+(WRC)^2\right]^{1/2}}$$

$$\angle \vec{V}_0 = -\tan^{-1} wRC$$

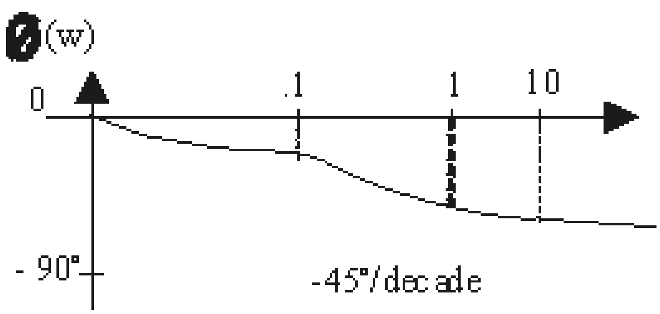
$$= \tan^{-1} w_0 / w$$

$$V_0 = \frac{\frac{1}{jwc}}{\frac{1}{jwc} + R} V_i$$



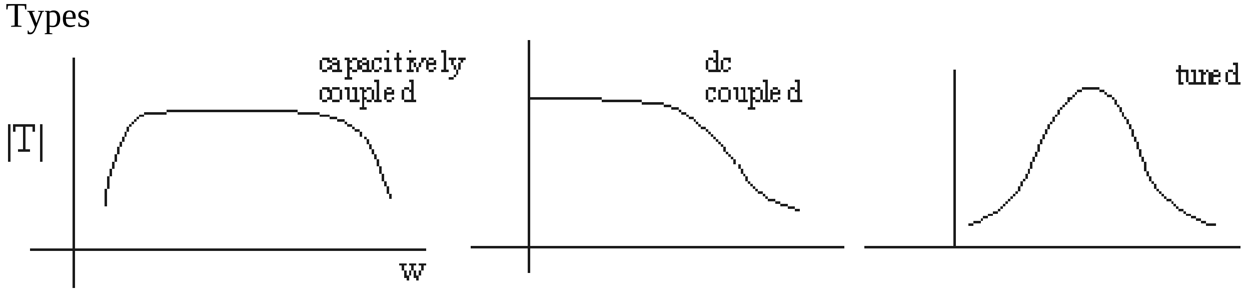


$$V_0 = \frac{1}{1 + jw\underbrace{CR}_{\tau}} V_i$$



e.g. 1.5

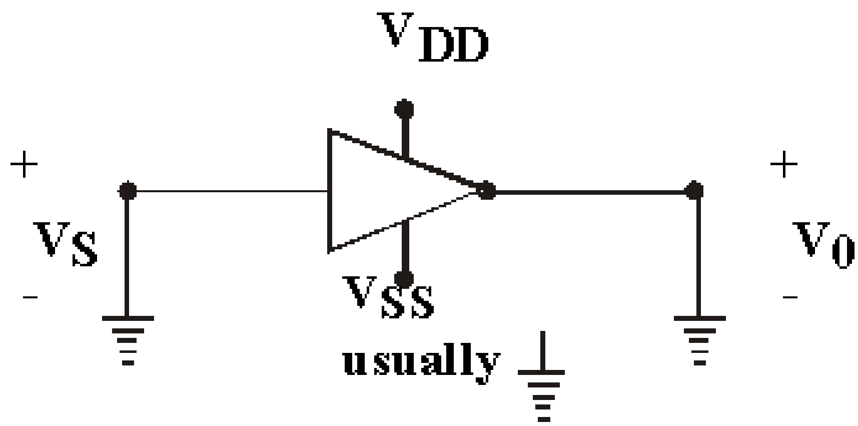
Types



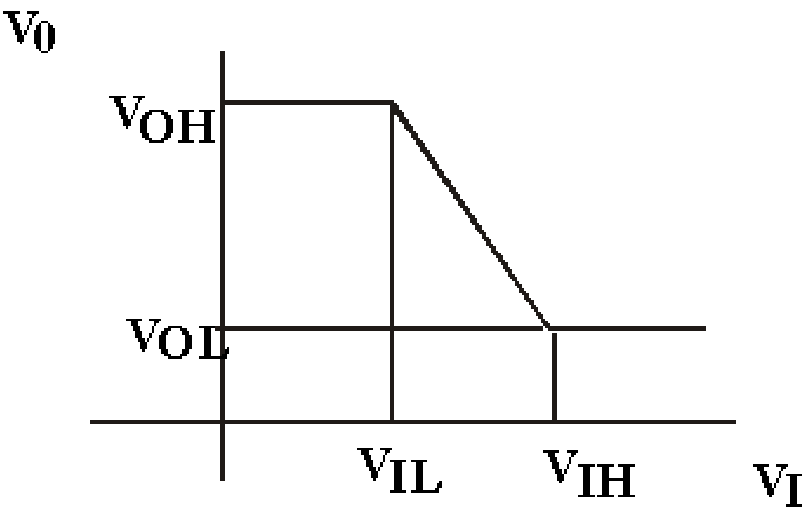
ex 1.15, 1.16, 1.19

Digital Logic

Inverter – basic building block



Transfer characteristic



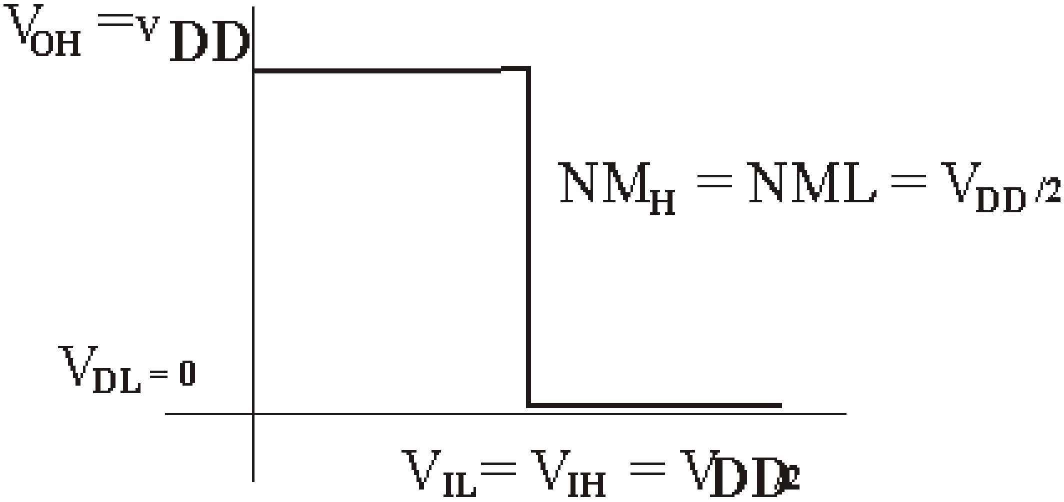
-

Noise Margins (for 1 inverter driving another)

$NM_H = V_{OH} - V_{IH}$

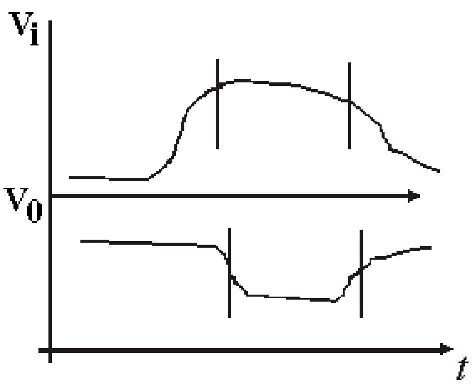
$NM_L = V_{IL} - V_{OL}$

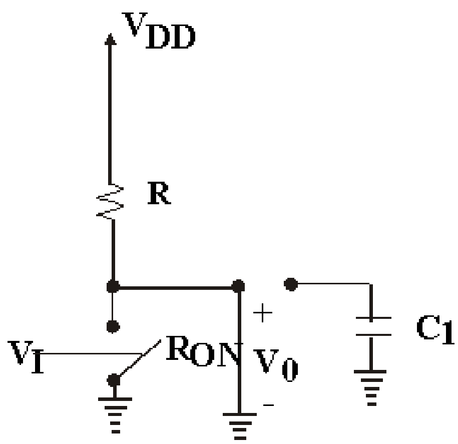
Ideal VTC



Homework : Read pp 60-92 D1.2, 1.33, 1.49

<u>Example Circuit</u>

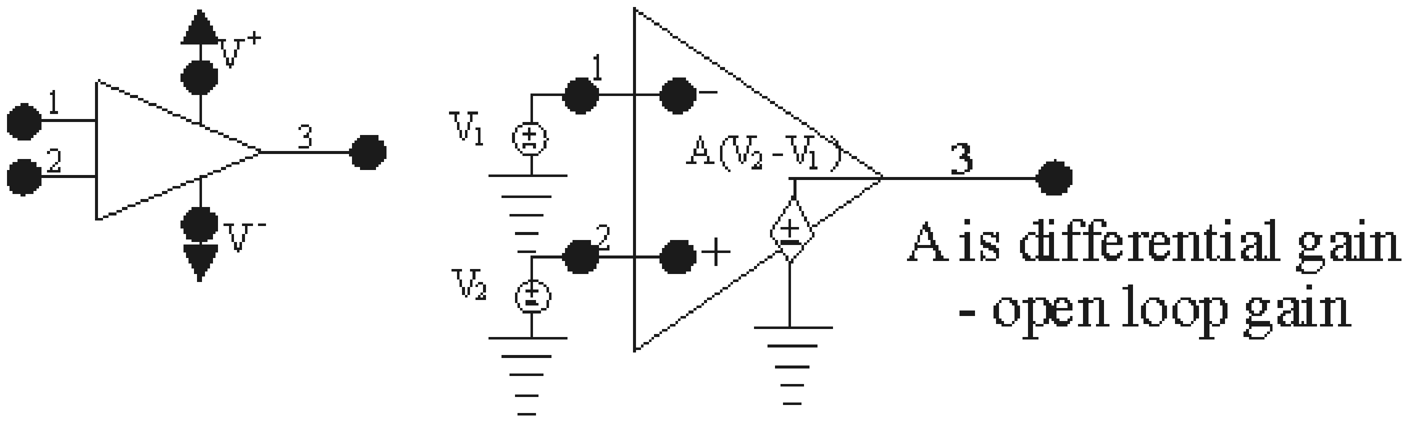




How can you make a NAND / NOR circuit?

Operational Amplifiers

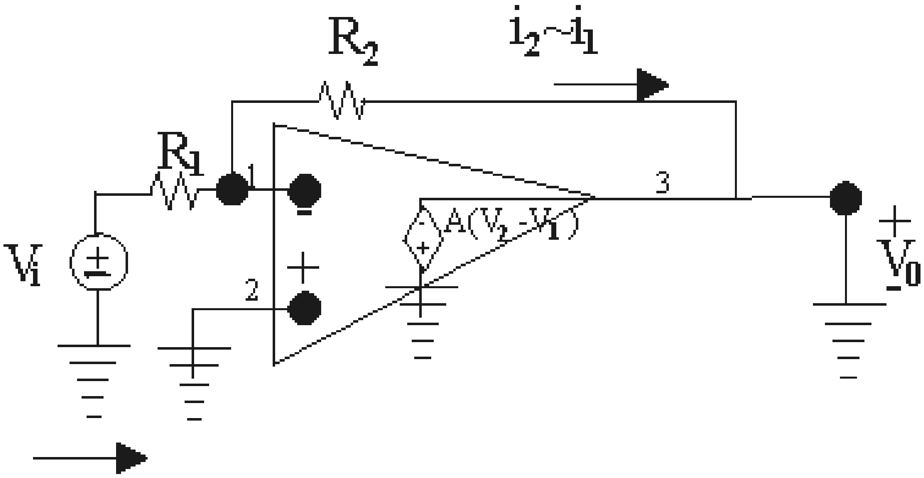
- IC opamp – versatile, easy to design with, not basic device but building block



- Ideal OpAmp
- infinite input impedance – no current drawn from terminals 1 & 2
- out $V_3 = A\,(V_2 - V_1)$
  - independent of current drawn
  - output impedance is zero
- $V_2 = V_1 \rightarrow V_3 = 0$ regardless of input offset – common mode rejection infinite
- dc coupled
- A constant from w = 0 to w = ∞
- A = ∞

ex 2.3

Inverting Configuration



$i_i = (V_I - V_1)/R_1 \not\approx V_I/R_1$

- Negative feedback – stable & accurate
- Virtual ground at $V_1 \sim 0$ (v_1 tracks v_1 not a short!)

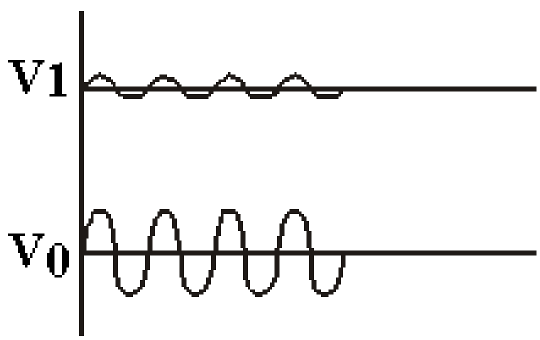
$$i_i = \frac{V_I - (\sim 0)}{R_1}$$ since A

- i_i goes into R_2 not into opamp since infinite input impedance

$$V_0 = V_1 - i_i R_2 = -\frac{V_i}{R_1} R_2 \qquad i_2 \sim i_1 \sim \frac{V_I}{R_1}$$

close loop gain

$$G \equiv \frac{V_0}{V_I} = -\frac{R_2}{R_1}$$



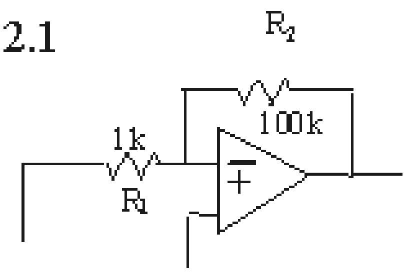
output is inverted and amplified

Finite Open Loop Gain

- $V_0 = A(V_2 - V_1) = -AV_1 \Rightarrow V_1 = -\frac{V_0}{A}$ (not zero)
- $i_1 = \frac{V_I - \left(-\frac{V_0}{A}\right)}{R_1} \approx i_2 = \frac{-\frac{V_0}{A} - V_0}{R_2}$
- $-\frac{R_1}{R_2} V_0\left(1+\frac{1}{A}\right) - \frac{V_0}{A} = V_I \Rightarrow V_0\left(1+\frac{1}{A}+\frac{R_2}{R_1}\frac{1}{A}\right) = -\frac{R_2}{R_1} V_I$
- $G \equiv \frac{V_0}{V_I} = \frac{-R_2/R_1}{1+(1+R_2/R_1)/A}$
- Want $1+\frac{R_2}{R_1} \ll A$ to minimize effect of finite open loop gain

e.g. 2.1

e.g. 2.1



a)

A	G	, =	$D = b_0 2^0 + b_1 2^1 + \ldots + b_{n-1} 2^{n-1}$
		$b_{n-1} \ldots b_2 b_1 b_0$ LSB MSB	
10^3	-91	-9%	-9 mv
10^4	-99	-1%	-.99 mv
10^T	-99.9	-0.1%	-0.1 mv

b) $A = 10^5 \rightarrow 0.5 \times 10^5$ $|G|$: $99.9 \rightarrow 99.8 \sim -0.1\%$

- Don't need extremely large open loop gain for G ~ 100

Input and Output Resistances

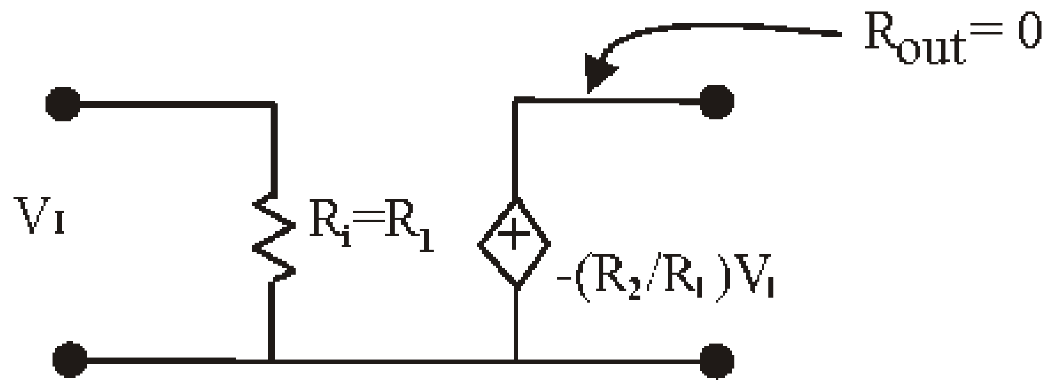
$$R_{in} \equiv \frac{V_I}{i_i} = \frac{V_I}{V_I/R_I} = R_1$$

–sine $V_1 = 0$ for $A = \infty$

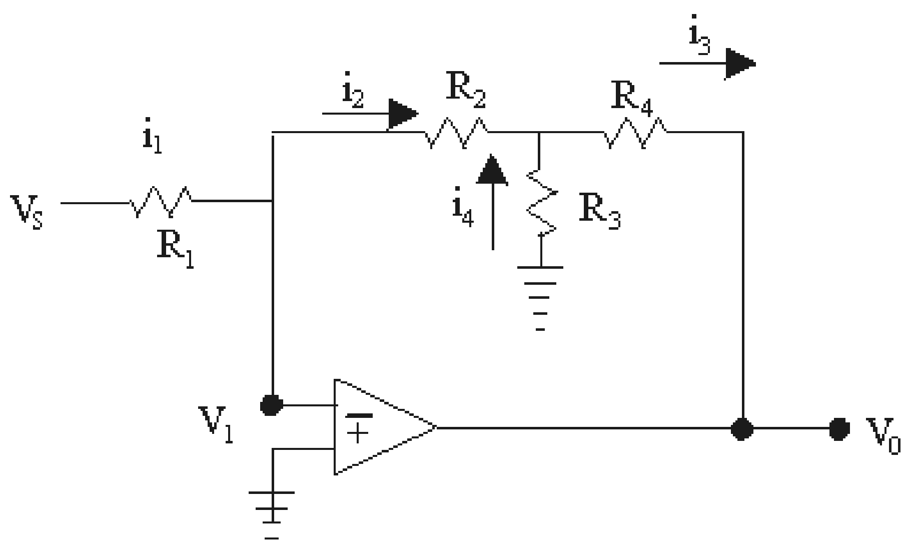
for high gain R_1 can't be too high (or R_2/R_1 is low) in inverting configuration

R_{out} ~ zero (ideal voltage source)

Equiv. Current



e.g. 2.2



$$V_1 = -\frac{V_0}{A} = 0 \qquad i_i = \frac{V_i - 0}{R_1} = i_2$$

$$V_2 = 0 - i_2R_2 = -\frac{V_I}{R_1}R_2$$

$$i_3 = \frac{-\left(-\frac{R_2}{R_1}V_s\right)}{R_3}$$

$$i_4 = i_3 + i_2 = \frac{V_I}{R_1} + \frac{R_2}{R_1R_3}V_I$$

$$V_0 = V_x - i_4R_4 = -V_I\frac{R_2}{R_1} - V_I\frac{R_4}{R_1} + \frac{R_2R_4}{R_1R_3}V_I$$

$$= -\frac{R_2}{R_1}V_I\left(1 + \frac{R_4}{R_2} + \frac{R_4}{R_3}\right)$$

Choose $R_1 = 1\Omega$, limit $R_2 = 1M\Omega$

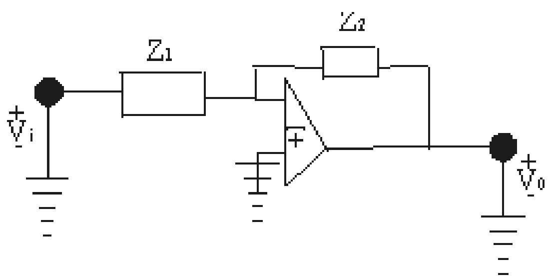
Can get G= -100 if $1+R/R_2 + R_4/R_3 = 100$

$R_4 = 1M\Omega \rightarrow R_4/R_3 = 100 - 2 = 98$; $R_3 = 10.2k\Omega$

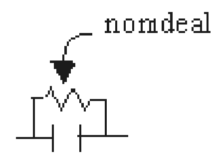
avoid a choice of

R_2 = 100 MΩ for R_{in} = 1MΩ

Other Applications of the Inverting Configuration



$$\frac{V_0}{V_I} = -\frac{Z_2}{Z_1}$$



Miller Integrator

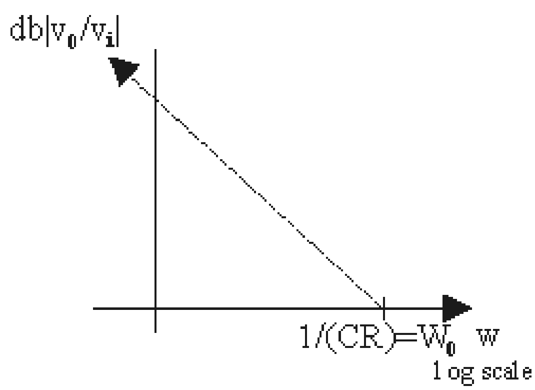
$$Z_1 = R,\ Z_2 = \frac{1}{SC} \Rightarrow \frac{V_0}{V_I} = -\frac{1}{jwCR} \qquad \left(\text{lowpass like } \frac{k}{1 + jw\underbrace{CR}_{\frac{1}{W_0}}} \text{but zero corner freq } \frac{w}{w_0} >> 1 \right)$$

$$i_1 = \frac{V_I(t)}{R} \Rightarrow V_0(t) = V_C - \frac{1}{C}\int_0^t i_1(t)dt = V_C - \frac{1}{CR}\int_0^t V_I(t)dt$$

initial voltage

inverting

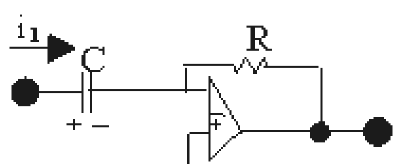
integration time constant



Differentiator $z_1 = 1/SC$, $Z_2 = R$

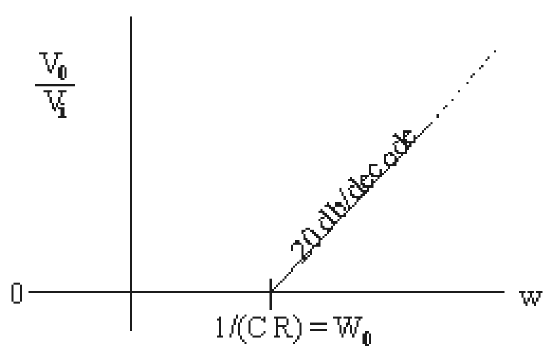
$$\frac{V_0}{V_i} = -sCR = -jwCR \qquad \left(\text{high pass like } \frac{k}{1 - jW_0/W} \text{ but od corner freq } \frac{W_0}{W} >> 1 \right)$$

$$\Rightarrow V_0(t) = -CR\frac{dV_I(t)}{dt}$$



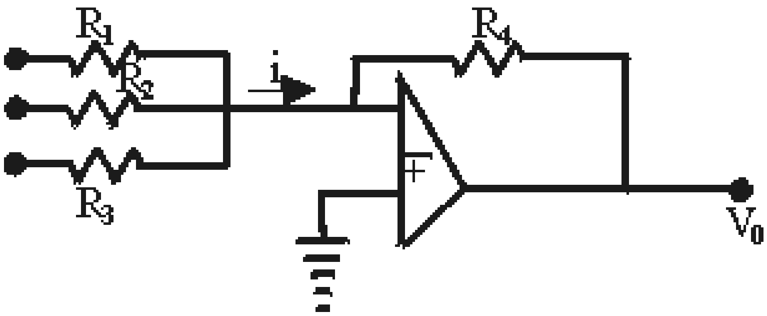
$$i_1 = c\frac{dv_c}{dt}$$

$$V_0 = -i_1 R$$



Other Applications (cont.)

Weighted Summer



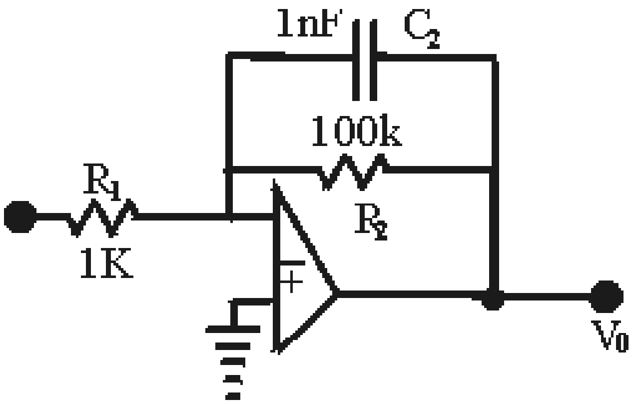
$$i_f = V_1 / R_f \qquad i = \sum_{e=1}^{n} i_l = i$$

$$V_0 = 0 - iR_f$$

$$\therefore \quad V_0 = -R_f\left(\frac{1}{R_1}V_1 + \frac{1}{R_2} + \ldots + \frac{1}{R_n}V_n\right)$$

Can integrate, differentiate, sum → math operations → "operational" amplifier (for analog computer)

ex, 2.6, D2.7, D2.8, D2.9



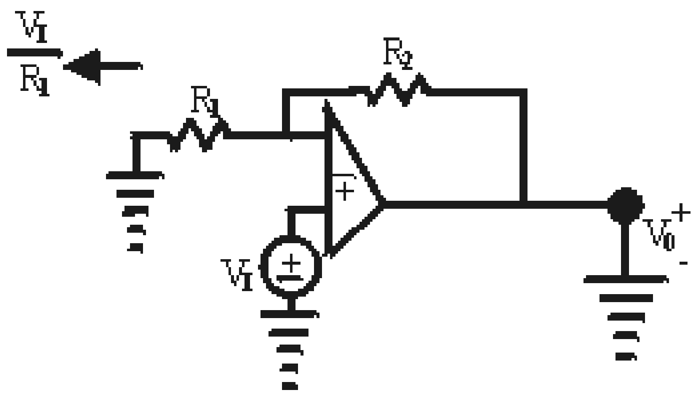
$$\frac{V_0}{V_i} = -\frac{Z_2}{Z_1} = -\frac{(R_2 \| C_2)}{R_1} = \frac{-\dfrac{1}{\frac{1}{R_2} + jwC_2}}{R_1}$$

$$= -\frac{R_2 / R_1}{1 + jw\underbrace{C_2R_2}_{j}} \qquad \underline{\text{LP type}} \qquad \left(\frac{k}{1 + jW / W_0}\right)$$

dcgain = $-R_2/R_1 = -100$ v/v

w(3db) = $1/C_2R_2 = 1/(10^{-9} \cdot 10^5) = 10^4$ rad/s

Non-inverting Configuration



virtual short between input

$$v_2 - v_1 = \frac{V_0}{A} \sim 0 \quad \text{for } A \to \infty$$

$$V_0 = V_I + \left(\frac{V_I}{R_1}\right) R_2$$

$$\frac{V_0}{V_I} = 1 + \frac{R_2}{R_1}$$

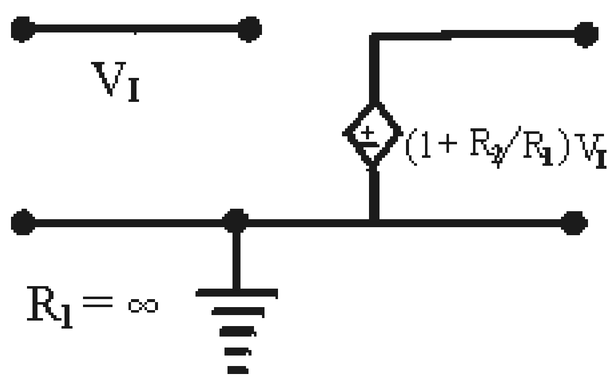
note voltage divider on V_0

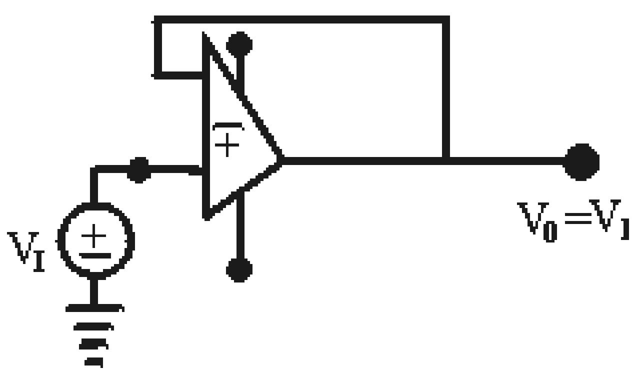
$$V_I \sim V_1 = V_0 \frac{R_1}{R_1 + R_2}$$

Positive gain

input impedance ~ ∞ (great as buffer amp)

output impedance ~ 0 (taken at voltage source)





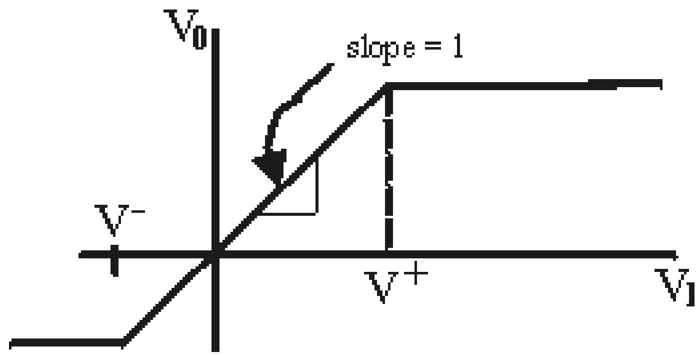
Unity Gain $R_2 = 0$

Buffer Amp $R_1 = \infty$

"Voltage Follower"

$$\mathbf{V_0 = V_I}$$

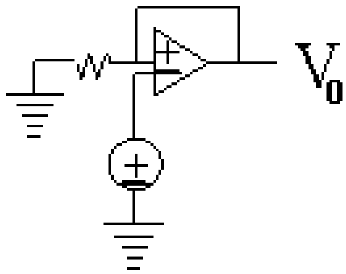
good to connect high output impedance source to low input impedance load (microphone to speaker)



ex 2.10, 2.11, D2.12, 2.13

Op-amp Exercises

Ex D2.12



Want $A_r = 2$ with $I_p = 10\mu$ A@10V

$$\frac{V_0}{V_I} = 1 + \frac{R_2}{R_1} = 2 \rightarrow \frac{R_2}{R_1} = 1$$

$$i = \frac{10v}{R_1 + R_2} = 10\mu A \qquad \frac{10v}{2R_1} = 10\mu A \qquad R_1 = \frac{5V}{10 \times 10^{-6} A} = .5\mu\Omega = R_2 = R_1$$

ex 2.13 if A_{V0} is finite

$$V_0 = V_I - V_0 / A = \frac{R_1}{R_1 + R_2} V_0 \qquad V_0\left(\frac{R_1}{R_1 + R_2} + \frac{1}{A}\right) = V_I$$

$$G \equiv \frac{V_0}{V_I} = \frac{A(R_1 + R_2)}{R_1 A + R_1 + R_2} = \frac{1 + R_2 / R_1}{1 + \frac{R_1 + R_2}{R_1}\frac{1}{A}} = \frac{1 + R_2 / R_1}{1 + \left(1 + R_2 / R_1\right)\frac{1}{A}} \quad Q \in D$$

b.

$$10^3 \qquad 10^4 \qquad 10^5$$

$$\epsilon \sim \left(1 + \frac{R_2}{R_1}\right)\frac{1}{A} = \frac{1+9}{10^3} \sim 10^{-2} = \qquad 1\% \qquad .1\% \qquad .01\%$$

$$\text{if } V_I = 1v \qquad V_2 - V_1 \sim 1 \sim (10^{-2}) \sim 10mV \quad 1mV \quad 0.1mV$$

$$= V_0 / A$$

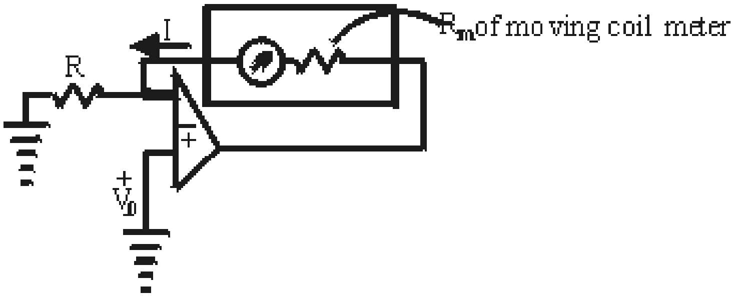
$$A \sim 10^2$$

H.W. Read pp 85-108

Probs. 2.2, 2.8, 2.28, 2.46

Examples of O_p Amp Circuits

e.g. 2.5 high input R voltmeter



100μ A full scale ?R for V= +10v

$$i = \frac{V}{R} = \frac{10V}{R} = 100\mu A \Rightarrow R = 100k\Omega$$

R_m does not matter! $R_{internal} = \infty$!

e.g. difference amp-combine inv + non-inv

$i_2 = i_1$, $i_4 = i_3$, $v_- = v_+$ (here, without superposition)

$$V_0 = V_1 + i_2R_2 + i_1R_1, \quad i_1 = \frac{V_- - V_1}{R_1}$$

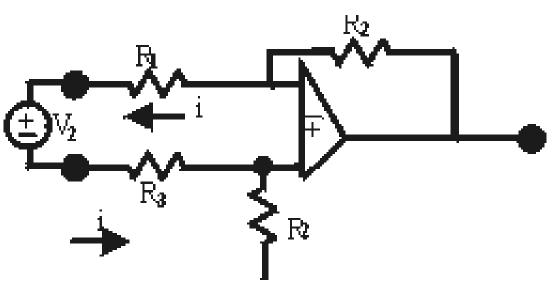
$$\downarrow$$

$$V_+ = V_2\frac{R_4}{R_3+R_4} \rightarrow \quad i_1 = \frac{V_2\frac{R_4}{R_3+R_4} - V_1}{R_1}$$

$$V_0 = V_1 + \left(\frac{V_2}{R_1}\frac{R_4}{R_3+R_4} - \frac{V_1}{R_1}\right)(R_2+R_1) = \frac{1+R_2/R_1}{1+R_3/R_4}V_2 - \frac{R_2}{R_1}V_1$$

For a true difference amp want $V_0 = 0$ for $V_2 = V_1 \Rightarrow$ set $R_2/R_1 = R_4/R_5$

$$\Rightarrow \quad V_0 = \frac{R_2}{R_1}(V_2 - V_1) \quad \text{simplify further } R_3 = R_1 \;\; R_4 = R_2, \;\; R_{in} \equiv \frac{V_2 - V_1}{i}$$



virtual short

$$V_2 - V_1 = R_1 i + 0 + R_1 i$$

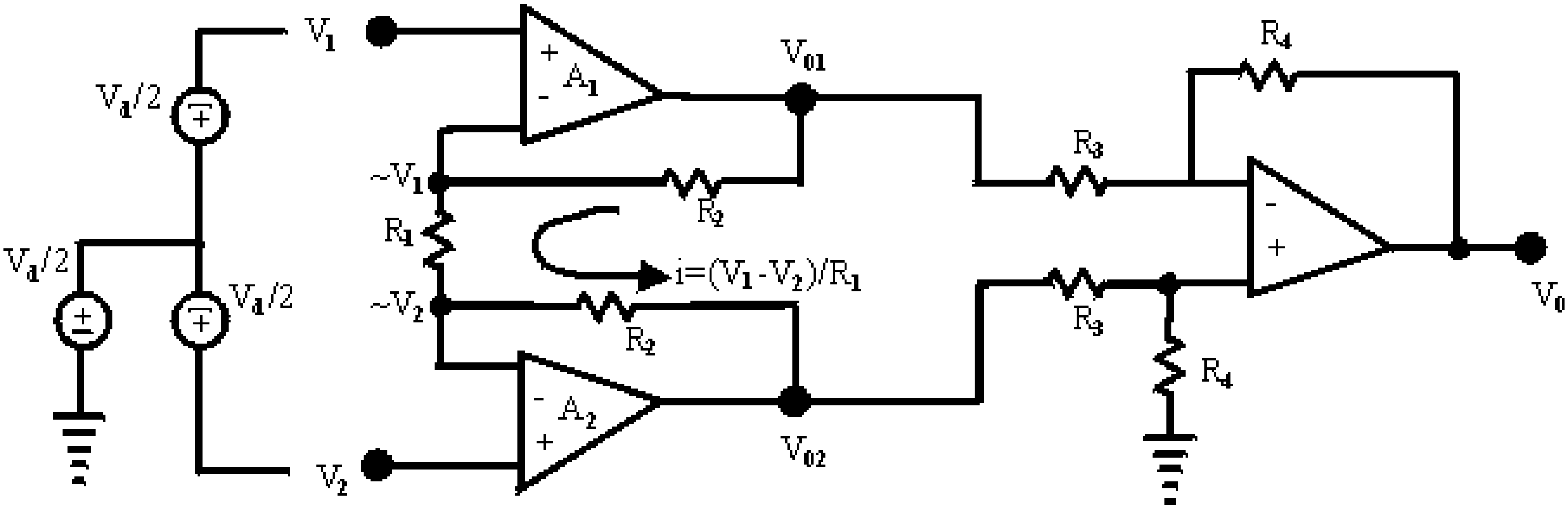
$$R_{in} \equiv \frac{V_2 - V_1}{i} = 2R_1$$

Note: can't have high R_{in} and high gain

Instrumentation Amp: rejection common mode with high input R and high gain

Instrumentation Amp

e.g. 2.7



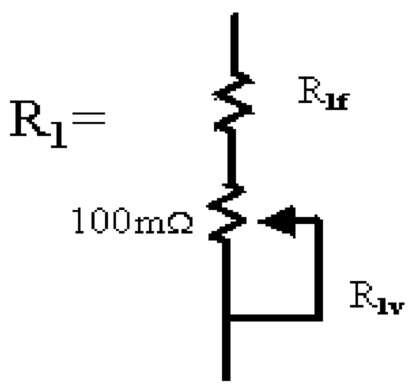
1st stage: $$V_{01}-V_{02}=\frac{V_1-V_2}{R_1}(R_2+R_1+R_2)=\left(1+\frac{2R_2}{R_1}\right)(V_1-V_2)$$

2nd stage: $$V_0=\frac{R_4}{R_4}(V_{02}-V_{01})=\underbrace{\frac{R_4}{R_3}\left(1+\frac{2R_2}{R_1}\right)}_{A_d\text{ is differential gain}}\overbrace{(V_2-V_1)}^{V_d}$$

V_{cm} appears as $V_{01} = V_{02}$ if $V_d = 0 \Rightarrow V_0 = 0$

Vary Gain by varying R_1

Input impedance ~ ∞

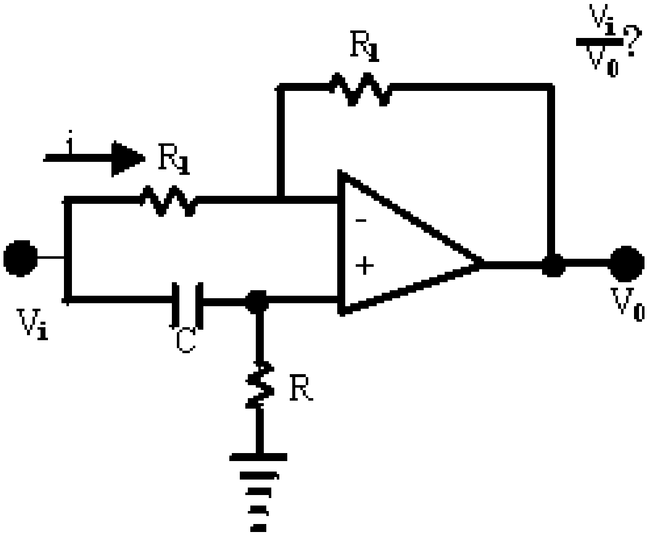


Usually design 2nd stage for gain = 1 → $R_3 = R_4$ =10 kΩ say

Problem: design 1st stage for gain of 2 → 1000 W_1 100 kΩ potentiometer

$$1+\frac{2R_2}{R_{1f}+R_{1v}}=2\to 100\Rightarrow 1+\frac{2R_2}{R_{1f}}=1000 \qquad 1+\frac{2R_2}{R_{1f}+100k\Omega}=2$$

Phase Shifter (1st order all-pass filter)



$$i = \frac{V_i - V_-}{R_1} = \frac{V_i}{R_1}\left[1 - \frac{R}{\underbrace{R + \frac{1}{s}C}_{\substack{\text{voltage divider on } V_+ = -V_- \\ V_- = V_+ = V_i \frac{R}{R+1/2C}}}}\right] = \frac{V_i}{R_1}\,\frac{\frac{1}{s}C}{R + \frac{1}{s}C}$$

$$V_0 = V_- - iR_1$$

$$= V_i \frac{R}{R + \frac{1}{sC}} - \frac{\frac{1}{sC}}{R + \frac{1}{s}C} V_i$$

$$\frac{V_0(s)}{V_i(s)} = \frac{R - \frac{1}{sC}}{R + \frac{1}{sC}} = \frac{S - \frac{1}{RC}}{S + \frac{1}{RC}} = -\frac{\frac{1}{RC} - jw}{\frac{1}{RC} + jw}$$

$$\left|\frac{V_0}{V_1}\right| = 1 \qquad \varnothing = 180^\circ - 2\tan^{-1}(wCR)$$

(-sign)

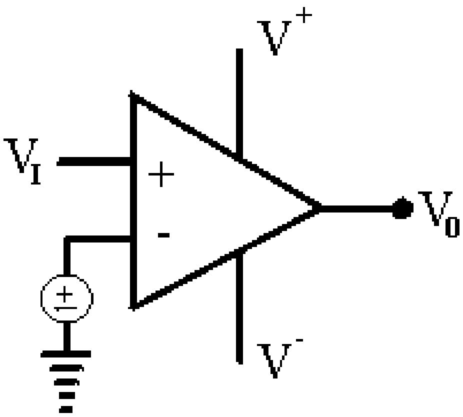
H.W. Read pp. 92-108

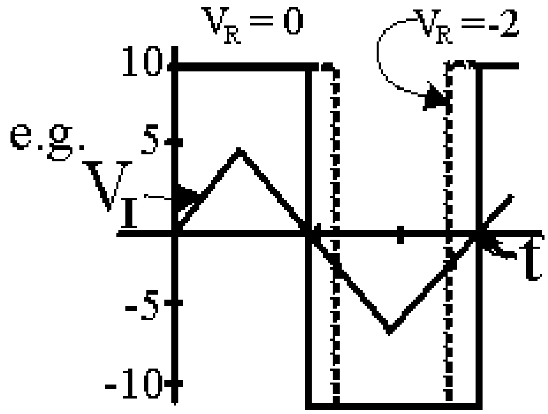
Prob D2.54 (due Sept 15 along with next week's assignments) + Project1

Next class in PC lab for PSpice - will not be on whiteboard but will have voice

Nonlinear Op Amp Circuits

Open-loop comparator



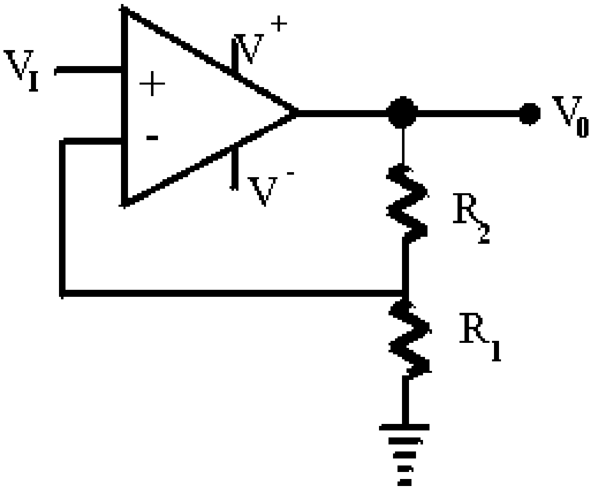


$V^+ = 10$

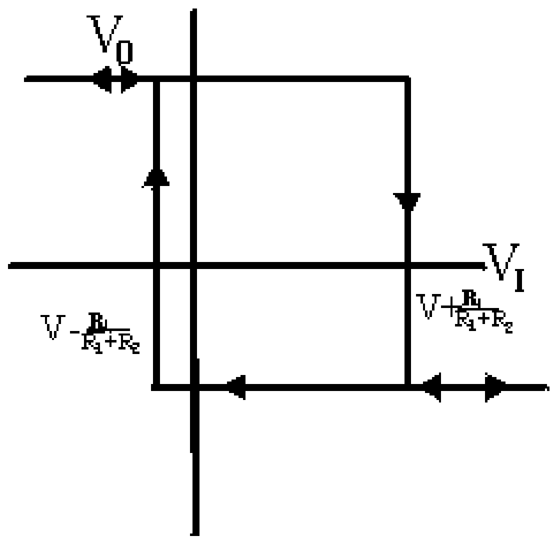
$V^- = -10$

Very susceptible to noise if $V_I \sim V_{RCF}$

Schmitt Trigger – use positive feedback to help hold state



$V_+ = \frac{R_1}{R_1 + R_2} V^+$ if output is positive; $= \frac{R_1}{R_1 + R_2} V^-$ if negative

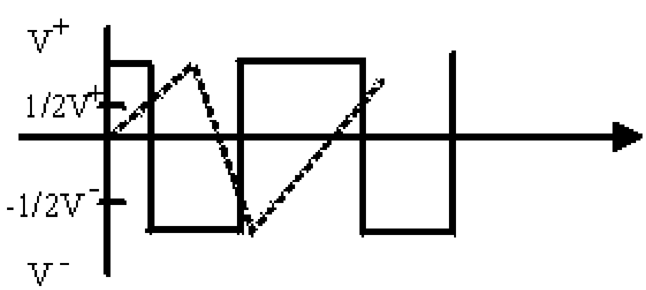


Hysteresis

bistable

used as memory

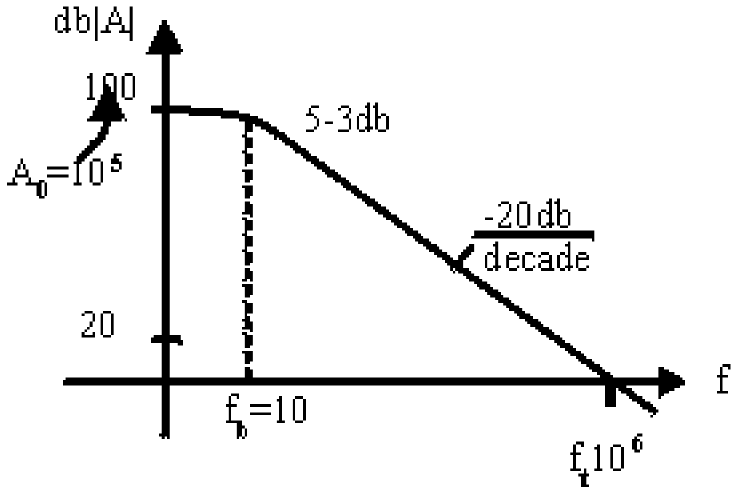
for $\frac{R_1}{R_1 + R_2} = \frac{1}{2}$



point at which switching takes place depends on state

Non-idea Performance of O_p Amps

Finite open-loop gain & band width



Typical of internally compensated (capacitor feedback for stability)

$$A(s) = \frac{A_0}{1 + s/w_b}$$ w_b is "break" frequency

($\cong 2\pi$ x 10 rad/s)

for $w >> w_b$

$$A(jw) \cong \frac{A_0 w_b}{jw}$$; reaches unit gain (0db) at $W_t = A_0 W_b$

$$A(jw) \cong \frac{w_t}{jw}$$; w_t is "unity gain bandwidth" integrator with $\tau = 1/w_t$

Gain Magnitude $$|A(jw)| \cong \frac{W_t}{W} = \frac{f_t}{f}$$

-20 db/decade is "single pole" or "dominant pole" model

W_t is important spec.

Effect on Closed-loop Amplifiers

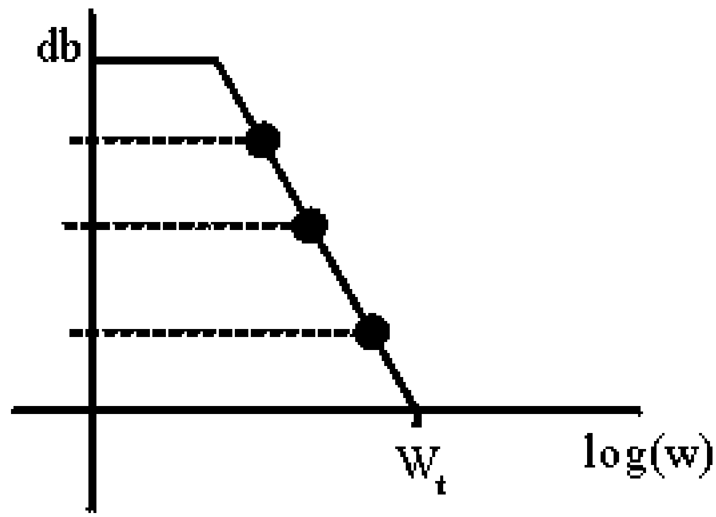
Inverting

$$\frac{V_0}{V_i} = \frac{-R_2/R_1}{1+(1+R_2/R_1)/A} \quad \text{where} \quad A = \frac{A_0}{1+S/W_b} \cong W_t/S \quad \text{for } W >> W_b$$

$$= \frac{-R_2/R_1}{1+\frac{1}{A_0}(1+\frac{R_2}{R_1})+\frac{s}{W_t}(H\,\frac{R_2}{R_1})}$$

if $A_0 >> 1+ R_2/R_1$ then $\frac{V_0(s)}{V_i(s)} \cong \frac{-R_2/R_1}{1+\frac{1}{A_0}(1+\frac{R_2}{R_1})+\frac{s}{W_t}(1+\frac{R_2}{R_1})}$ low pass STC $(k/1+s/W_0)$

Corner freq. $W_{3db} = \frac{W_t}{1+R_2/R_1}$



Non-inverting

similarly $\frac{V_0}{V_i} = \frac{1+R_2/R_1}{1+(1+R_2/R_1)/A}$

$$\Rightarrow \frac{V_0(s)}{V_i(s)} \cong \frac{1+R_2/R_1}{1+\frac{s}{W_t/(1+R_2/R_1)}}$$

low pass STC with same W_{3db}

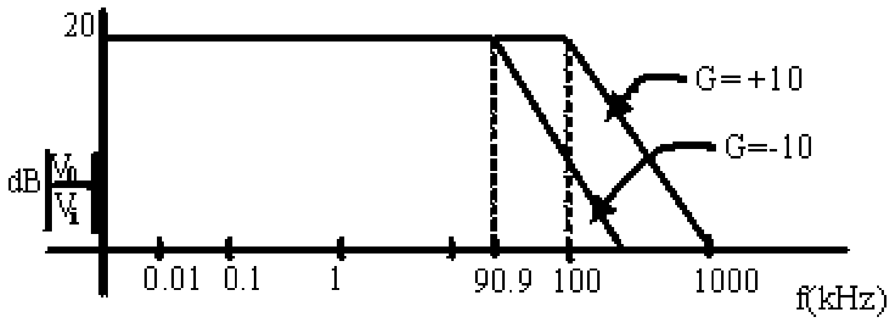
e.g. 2.8 f_t = 1MHz

$$f_{3dB} = \frac{f_t}{1 + R_2/R_1}$$

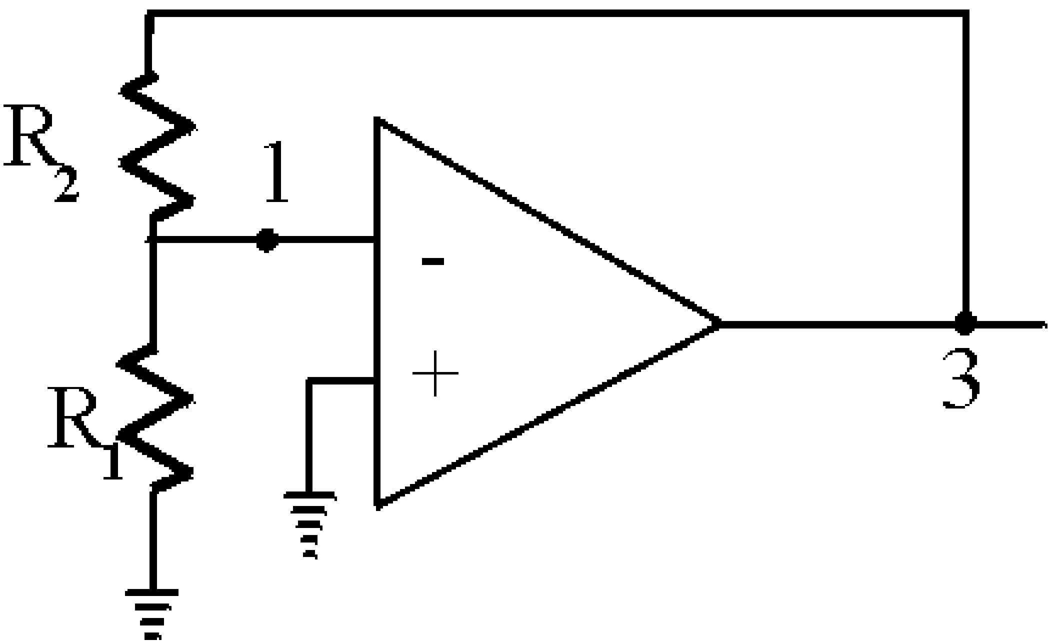
Nominal closed loop gain	- R_2/R_1 -	f_{3dB}
1000	999	$10^6/1000$ = 1 kHz
100	99	10 kHz
10	9	100 kHz
1	0	1 MHz
-1	1	10^6 / 2 = 0.5 MHZ
-10	10	10^6/ 11= 90.9 kHz
-100	100	9.9 kHz
-1000	1000	~ 1 kHz

$$G_{inv} = -\frac{R_2/R_1}{1+(1+R_2/R_1)/A} \sim -R_2/R_1$$

$$G_{n.i.} = \frac{1+R_2/R_1}{1+(1+R_2/R_1)/A} \sim 1+R_2/R_1$$



Feedback Interpretation



- both have same feedback loops (if short v_i)
- same dependence on finite gain and bandwidth (f_{3dB})

Voltage Divider feedback ratio

loop gain -AB negative feedback

Amount of feedback ≡ 1 – loop gain = 1 + Aβ

$f_{3db} = \beta f_t$

ex 2.18 – 2.19

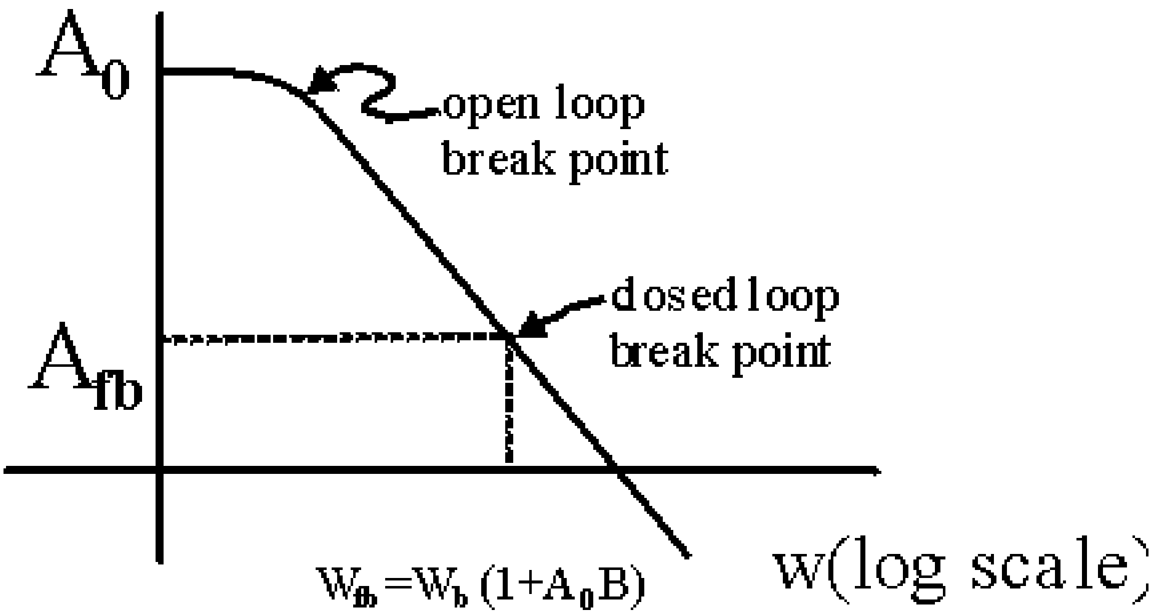
Gain- bandwidth Product

-

$W_{fb} = W_b\ (1+A_0\ \beta\ )$ where $1/\beta = 1 + R_2/R_1$

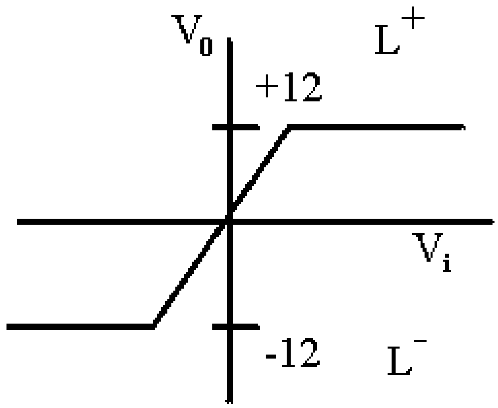
or 3dB

$$\frac{A_0}{1+A_0\beta} W_{fb} = A_0 W_b \qquad A_{fb} = \frac{A_0}{1+A_0\beta}$$



Large Signal operation of O_p Amps

Output Saturation

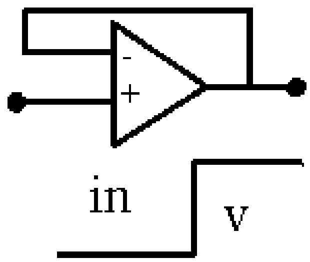


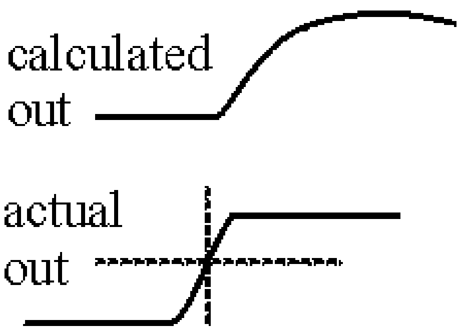
keep output below L^+ for linear rated output voltage V_{0max}

-

Slew rate

$$SR = \left.\frac{dV0}{dt}\right|_{max}$$



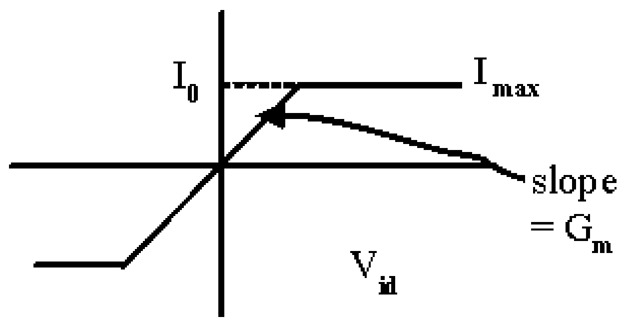


$$\frac{V_0}{V_i} = \frac{1}{1+S/W_t}$$

low pass STC response to step

$\Rightarrow V_0(t) = V\,(1-e^{t/\tau})$

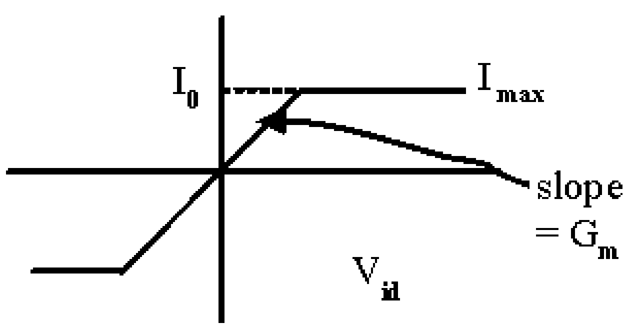
at step $V_- = V_+$ will be large transcond. stage supplies max I to 2nd stage



Full Power Bandwidth

$$V_i = \hat{V}_i \sin(wt) \qquad \frac{dV_i}{dt} = \underbrace{wV_i}_{\text{peak value}} \cos(wt)$$

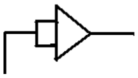
if $wV_i > SR \Rightarrow$ distortion



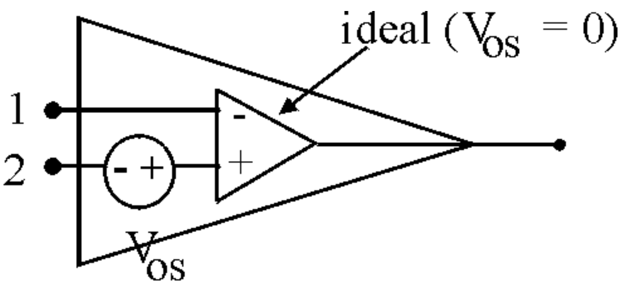
spec f_m = full power bandwidth is freq. at which output with ampl. at V_{0max} shows SR distortion

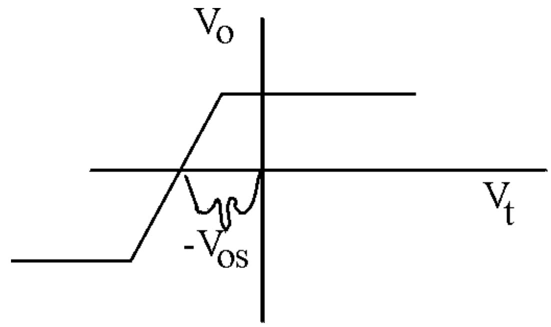
$W_m V_{0max} = SR$ $$f_m = \frac{SR}{2pV_{0max}};\ V_0 = V_{0max}\frac{W_m}{W}\ \text{for } w > w_m \text{ get distortion at } V_{0max}$$

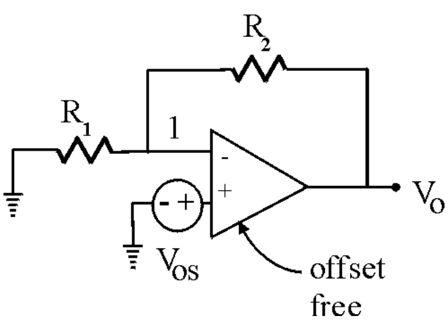
Input Offset Voltage



V_0 at L^+ or L^-, 1 nce gain is high V_{os} ~ 1-5 mV depends on temp





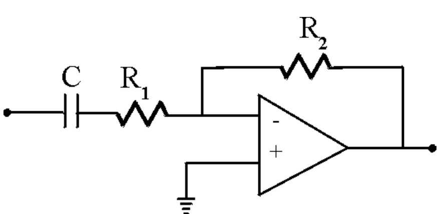


$V_0 = V_{0S}\,[1 + R_2 / R_1]$

e.g. $1 + R_2 / R_1 = 10^3$, V_{0S} = 5mv $\rightarrow$ V_0 = 5v zero V_-

741 op amp has add'd terminals to trim V_{0S}

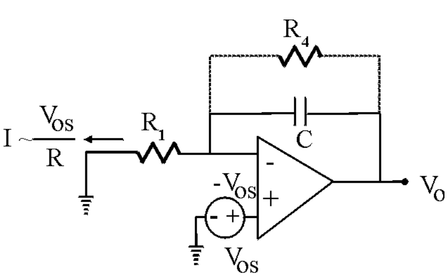
Capacitive coupling



R_1 dc ~ $\infty \rightarrow V_{0S}$ gain (dc) = 1

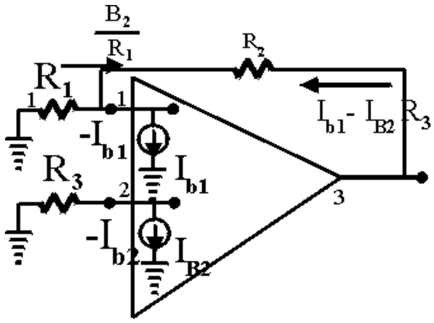
for $W >> W_0 = 1/CR_1$; gain = $-R_2/R_1$

Miller integrator



$V_0 = V_{0S} + \dfrac{V_{0S}}{CR}t$; integrates I to saturation add R_F so that V_0 has dc component $A(s) = \dfrac{A_0}{1 + s/W}$ low $R_F \rightarrow$ low output offset $\rightarrow$ less ideal integrator

Input Bias Current



To reduce V_{0dc} add R_3

spec:

input bias current: $\text{Average } I_B = \dfrac{I_{B1} + I_{B2}}{2}$ ~ 100 nA (B>T) ~ pA
(ε FT)

input offset current: $I_{0S} = |I_{B1} - I_{B2}|$ ~ 10 nA

output dc voltage (inv and ni) $V_{0dc} = I_{b1}R_2 \sim I_BR_2$

$V_{0dc}(V_I = 0) = - I_{B2}R_3 + R_2 [I_{B1}\text{-}I_{B2} (R_3/R_1)]$

If $I_{0S} = 0$, $I_{B1} = I_{B2} = I_B \Rightarrow V_0 = I_B [R_2 - R_3 (1+R_2 /R_1)]$

select R_3 s.t. $| A(jw) | \cong \dfrac{W_t}{W} = \dfrac{f_t}{f}$

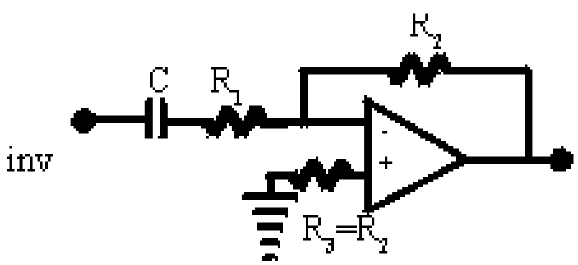
If $I_{0S} \neq 0$,

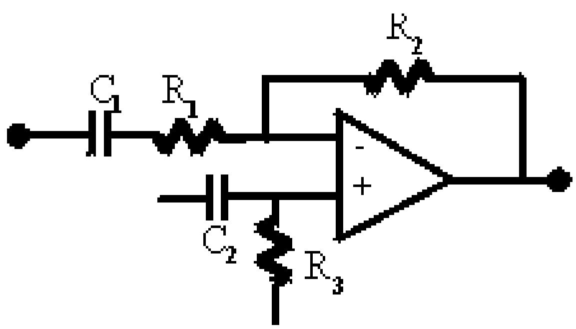
$I_{B1} = I_B + B_{0S} / 2,\ I_{B2} = I_B - I_{0S} / 2 \Rightarrow \underbrace{V_0 = I_{0S}}_{\sim 1/10\ G_BR} R_2$ for $R_3 = R_1 || R_2$

∴ make R_3 at + s.t. = R_{in} (=R_1 || R_3) at – input for dc coupling

for ac coupling

choose
R_3 =
R_2



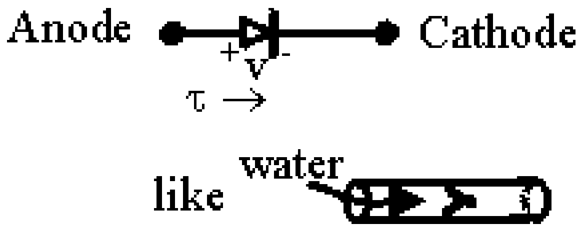


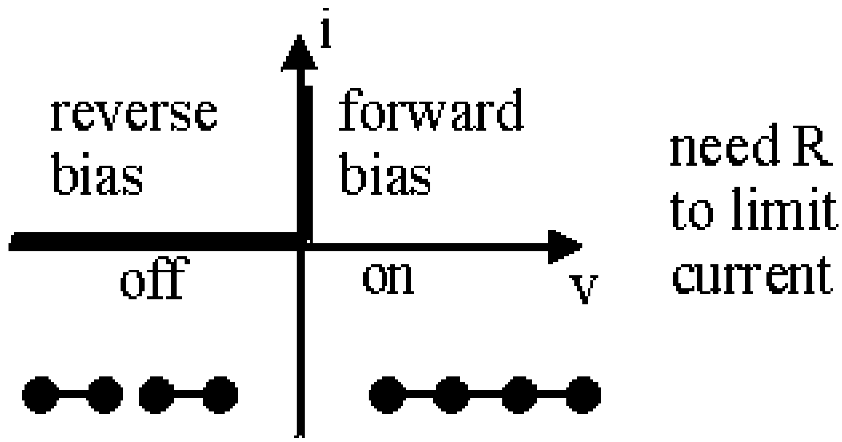
need dc to grd
→$R_{in} \neq \infty$
=R_3

H.W. 2.75, 2.80, 2.85

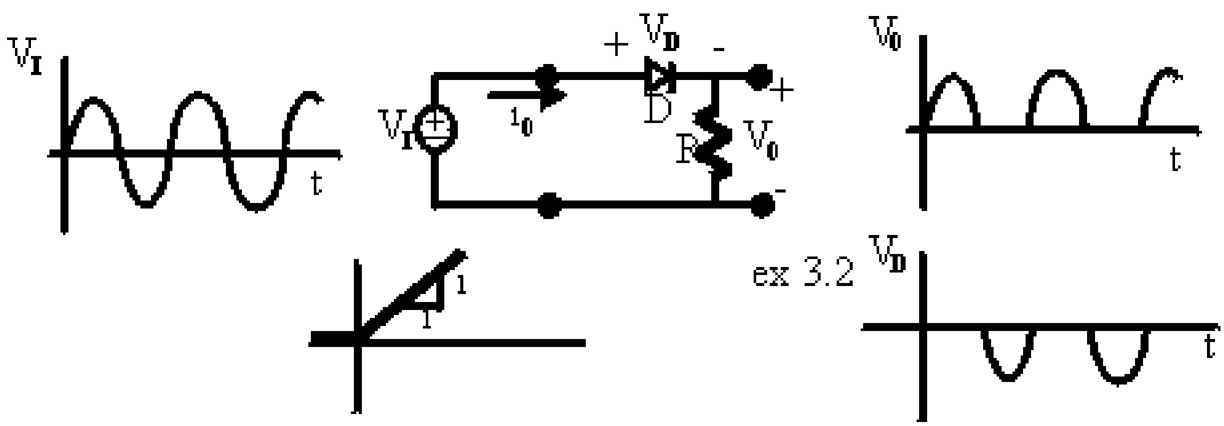
Read Chap 3 pp 122-137

Ideal Diode





Rectifier



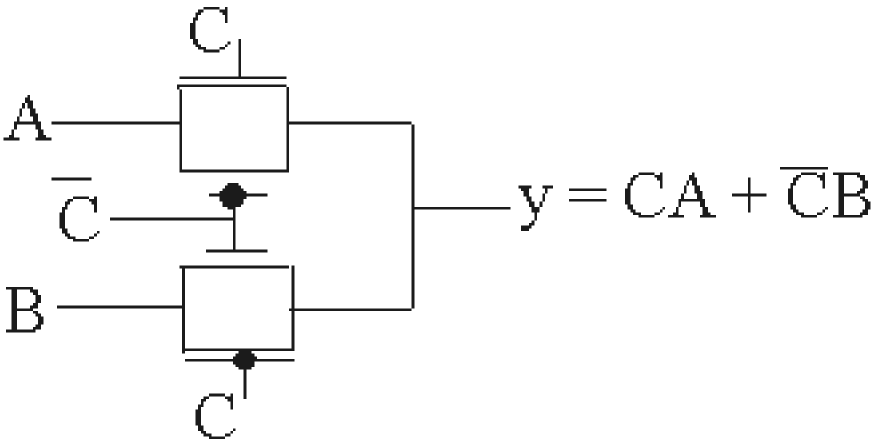
generates dc from ac

dc > 0

ex 3.3 V_{Ipeak} = 10V, R=1k $i_D$peak = 10V/1k =10 ma

$$\text{avg} \equiv V_{dc} = \frac{10\left[\int_0^{\pi} \sin\theta\, d\theta + \int_{\pi}^{2\pi} 0\, d\theta\right]}{\int_0^{2\pi} d\theta} = \frac{10V[2+0]}{2\pi} = \frac{10}{\pi} = 3.18V$$

Pass Transistor Logic



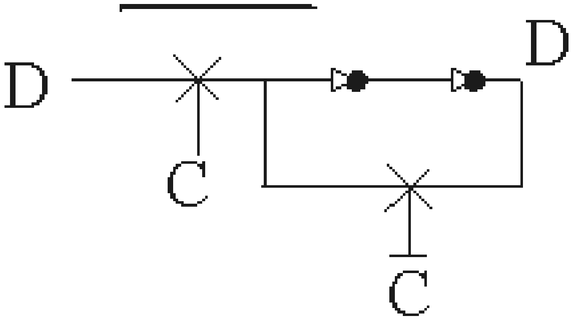
every circuit node must always have a low resistance path to V_{DD} or V_{SS} (gnd)

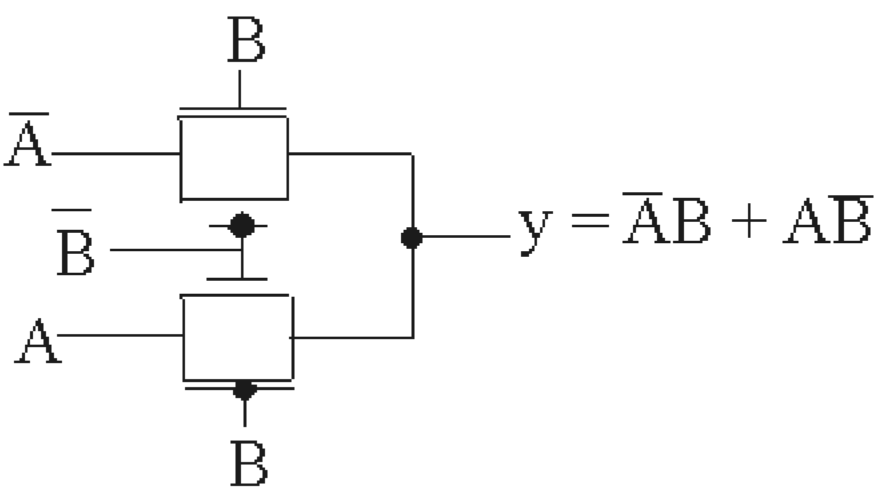
Input signals are driven by inverters or active eMOS logic

Can't cascade PTL circuits if y becomes a high impedance note

PTL - fast, area efficient

D latch



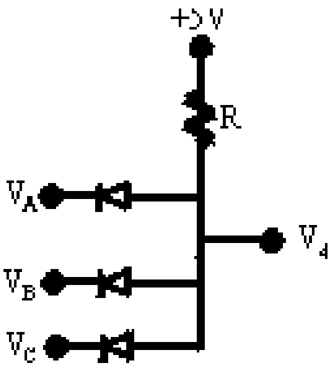


H.W. 5.92, 5.93, 5.100, 5.101. 5.107, 5.108

Simple Diode Circuits

-

Diode Logic



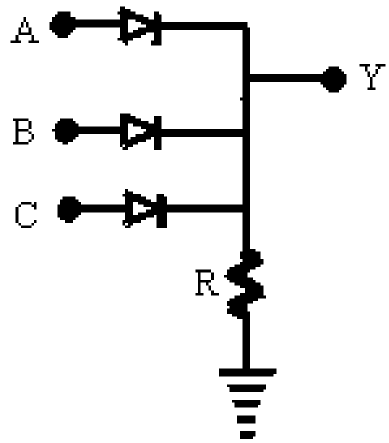
see e.g. 3.2

Logic	Voltage
1	+5v
0	0v

$Y = A \cdot B \cdot C$

since any of A, B, C, = low ⇒ Y low

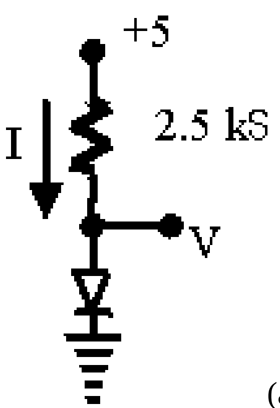
∴ all must high for Y to be high



?

-

ex 3.4



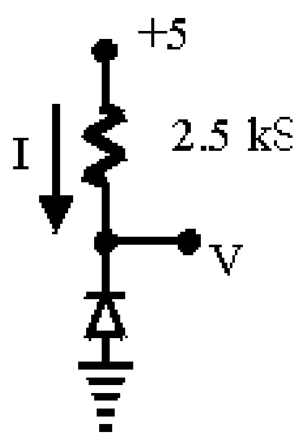
(a)

assume on

I = 5/2.5 k = 2 ma

V= 0 (really ε)

(b)

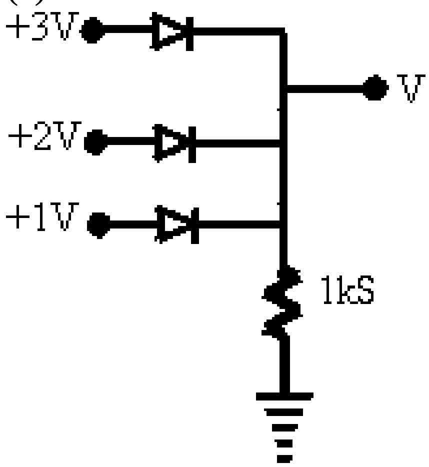


1) assume on I = 2 ma NOT POSSIBLE since reverse biased

2) assume off I =0; V= 5V

-

(e)



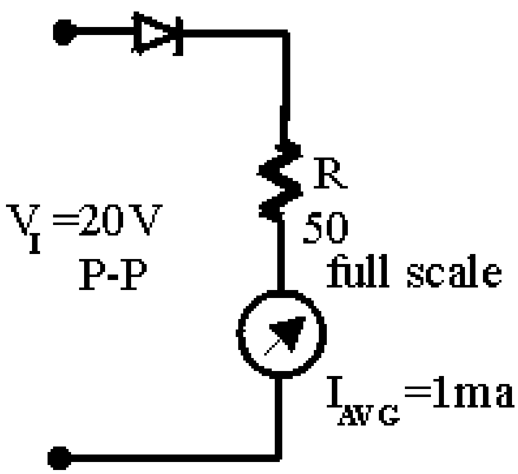
1. assume all on V = 3V

   0) 2, 1 reverse ⇒ off
2. 2,1 off

   I = 3V/1k = 3ma

   V = 3V

ex 3.5



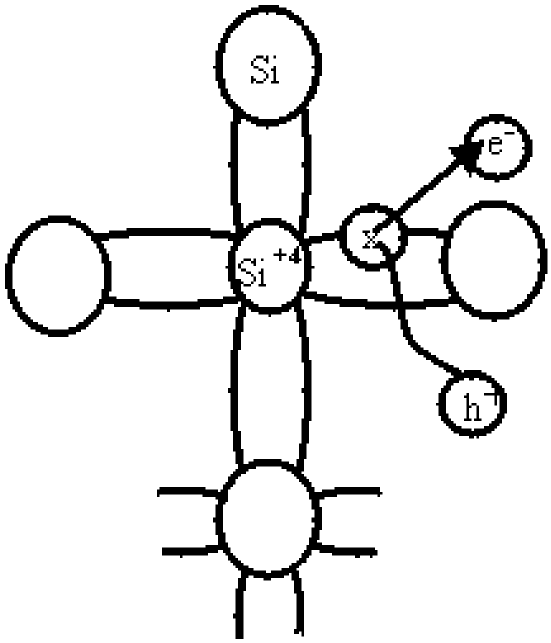
$$V_{avg} = \frac{10\int_0^{2\pi} \sin\theta\, d\theta}{\int_0^{2\pi} d\theta} = -\frac{-\cos\theta\big|_0^{\pi} - 10}{2\pi} = \frac{10}{\pi}$$

$$I_{avg} = \frac{V_{avg}}{R + 50}$$

$$R = \frac{V_{avg}}{I_{avg}} - 50 = \frac{3.18}{10^{-3}} - 50$$

$= 3.13\ k\Omega$

Crystalline Silicon



4 valence elections – Si`^{4} – Diamond x-tal structure

all bonds complete at 0ºk – insulator

"intrinstic semiconductors" – no imparities

T>0ºk – lattice vibrations – break bonds

thermal generation of mobile elections and "holes"

(also optical generation – silicon solar cell)

#of bonds = $4N_{Si} = 2x10^{23}$ cm^{-3}

Thermal Equilibrium

$$n_0\, p_0 = n_i^2(T) \qquad n_i \quad \text{doubles every } 10^\circ$$

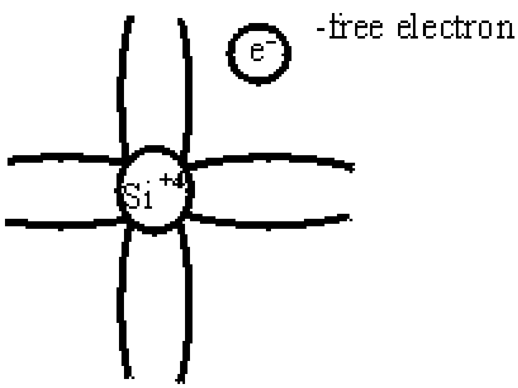
mobile election density

hole

$n_i \sim 10^{10}$ cm^{-3} at 300ºk (1 in 2 x 10^{13} bonds are broken)

-

Doping Donors- Group V – P, As, Sb - donate a free election to lattice



Still neutral since As^+ ion is bound in lattice

"extrinsic" silicon: $n_0 \cong N_d$ indep of T

-

# of donors $N_d >> n_i$ – "n-type"

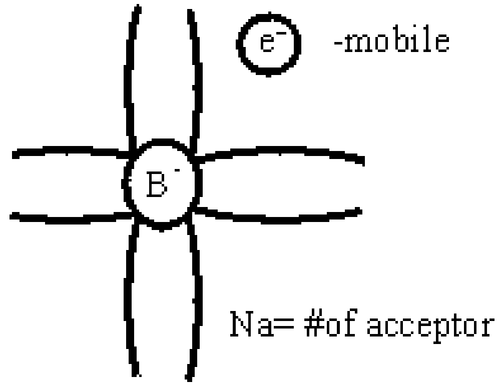
hole concentration suppressed since large # of e's combine

$n_0\, p_0 = n_i^2$

e's – majority carriers

h's – minority carriers

Acceptors – Group III Boron



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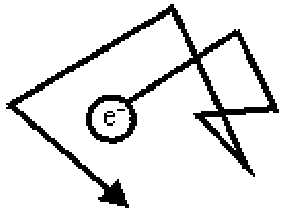
Transport of Carriers

Drift



$V_{thermal} \sim 10^7 cm/s$ at $300^\circ k$

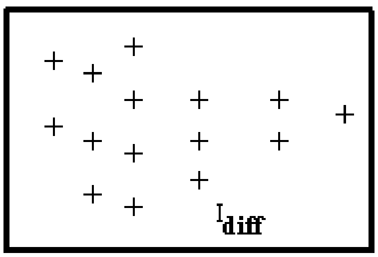
electron mobility ~1400 $cm^2/V\text{-}s$

$F_c = -qE$; on average $V_{dn} = \frac{\Delta \bar{x}}{\Delta t} = -\mu_n E$

$V_{dp} = \mu_p E$

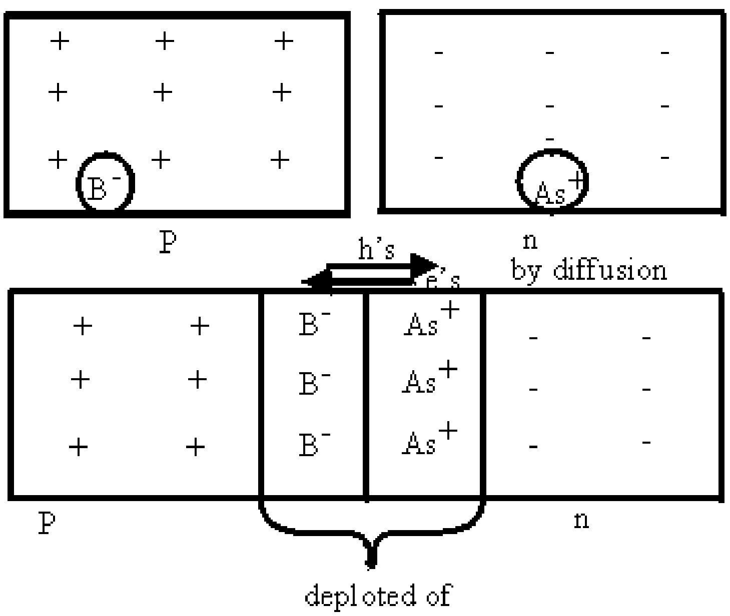
hole mobility ~ 500 $cm^2/V\text{-}s$

Diffusion



- carriers go from high concentration to low by thermal motion

ph junction



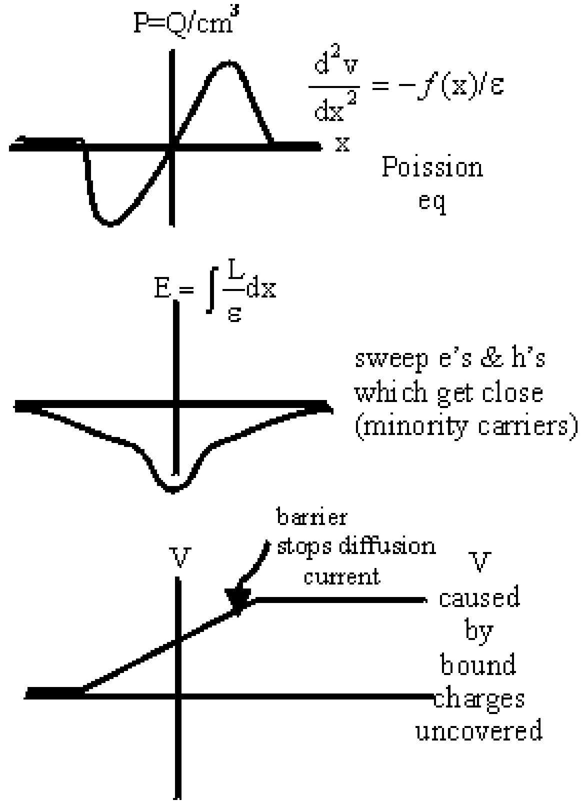
open current E field

←——

causes drift current α e^{kt}

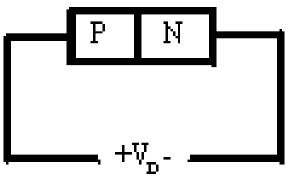
——→

diffusion current balances

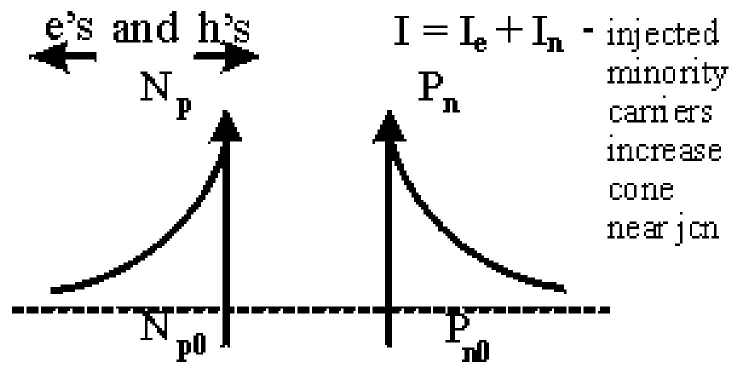


P_n junction under bias

Forward – carrier den sities $P_n = P_{n0}\, e^{Vd/Vt}$ $n_p = n_{p0} e^{Vd/Vt}$



decrease barrier by qV_D
allows



$$I_D = I_s(e^{V_D/nV_T} - 1)$$

emission coeff.

saturation or scale current

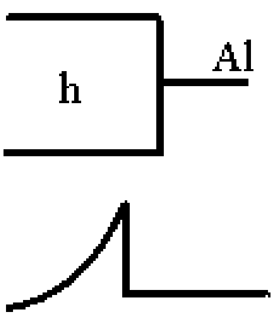
-

Reverse

- increase barrier by qV_D – decrease diffusion of majority carriers
- no effect on minority carriers which wander near jcn and are swept across
- upset in eq. $\rightarrow I_{sat}$ – due to thermal generation
- increase depletion layer width land charges it like a non-linear capacitor

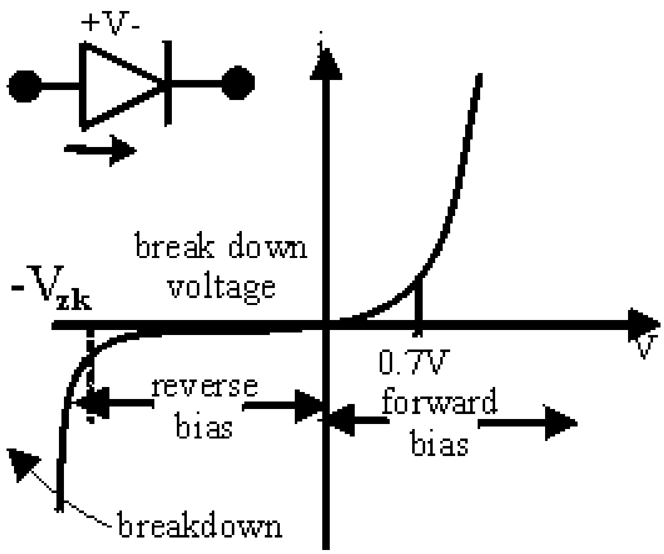
Contacts - Ohmic (non-rectifying)

junction potential V_0 is compensated at contracts under open circuits conditions



Characteristics of p-n Junction Diodes

-



Forward Bias

$$i = I_s\left(e^{\frac{v}{nV_T}} - 1\right)$$

I_s: saturation or scale current, prop to x-sect, $\sim 10^{-15}$A, depends on T

n: n~1 for IC, ~2 for disirete

V_T: thermal voltage

$V_t = \frac{kT}{q}$ ~25mV at room temp

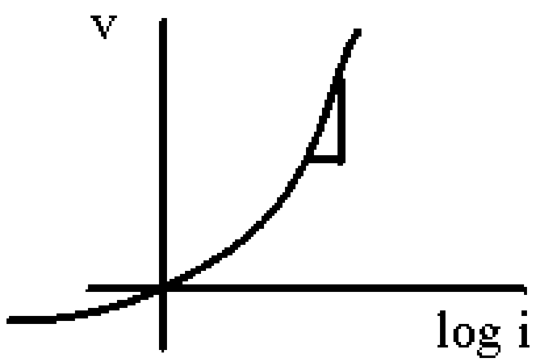
for $i \gg I_s$ $\quad i \cong I_s e^{\frac{v}{nV_T}} \quad \Rightarrow \quad V = nV_T \underbrace{\log_e}_{\ln} \frac{i}{I_s} = 2.3n\, V_T \log_{10} \frac{i}{I_s}$

at 2 different voltages V_1, V_2

$$\frac{I_2}{I_1} = e^{(V_2 - V_1)/nV_T} \quad \Rightarrow \quad V_2 - V_1 = 2.3n\, V_T \log_{10} \frac{I_2}{I_1}$$

$\therefore$ every factor of 10 increases in current $\rightarrow$ $2.3nV_T$ increase in V

rule of thumb : 0.1v/decade



60 mV for n = 1

120 mV n = 2

e.g. 3.3

1 mA dioade at V = 0.7

$$i = I_s e^{v/nV_T}$$

$$\Rightarrow I_s = i e^{-V/nV_T}$$

$$\left.\begin{array}{ll} n = 1 & Is = 10^{-3}\, e^{-0.7/0.025} = 6.4 \times 10^{-16} \\ n = 2 & Is = 10^{-3}\, e^{-0.7/0.050} = 8.3 \times 10^{-10} \end{array}\right\} \begin{array}{l} 10^{6} \text{ diff in } I_s \\ \text{because of exp in } n \end{array}$$

Temperature Dependence I_S and V_T depend on T

Rule: V decrease ~ 2mV for increase of 1° C → electronic thermometer

Ex 3.6 $\quad n = 1.5$ i_i 0.1 ma → 10ma, Δ V?

$$\Delta V = 2.3\, n\, V_T \log_{10}\frac{I_2}{I_1} = 2.3(1.5)(2.5mV)\, \underbrace{\log_{10}100}_{2} = 172.5\, mV$$

Ex 3.8 $\quad I_S$ rises by 15%/° C $I_S = 10^{-14}$A at 25° C, I_S (125° C)?

$$I_S\,(125°C) = \underbrace{(1.15)^{100}}_{\sim 10^6} 10^{-14}\, A = 1.17 \times 10^{-8}\, A \qquad (10^6 / 100°C)$$

Reverse bias region

$$i = I_S\,(\underbrace{e^{V/nV_T}}_{\text{small for } v = -\text{several } nV_T \sim -200mV} - 1)$$

ö i = I_S hence saturation current

but real divides have $|i| >> |I_S|$ by ~ $10^4 - 10^5$ due to leakage defects

($10^{-14} \rightarrow 10^{-9}$ A still small)

Breakdown region

breakdown voltage at "knee" of i-v curve is

V_{zk}

knee

zener

Skim pp 138-155

Read pp 155-171

HW 3.9, 3.16, 3.23

Review for Exam

Op-Amps 1> Two inputs track each other 2> No current flows input inputs

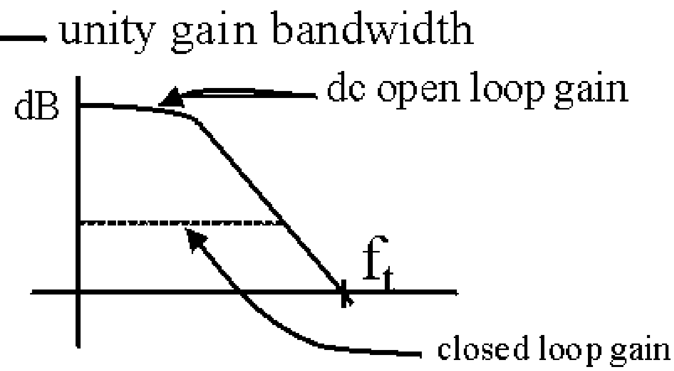
(first order approximation)

Derive V_0 / V_I for

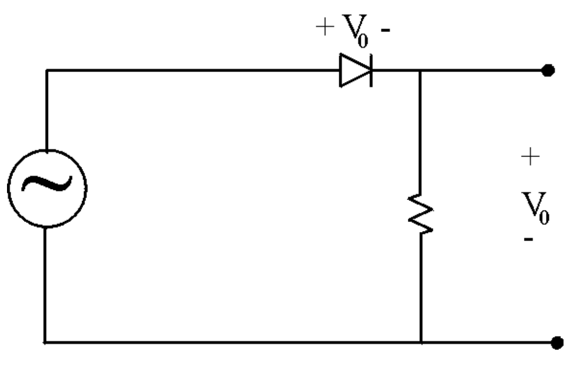
. Non-inverting amp
b. Inverting
c. Summer
d. Difference amplified

Finite Open Loop Gain and Bandwidth

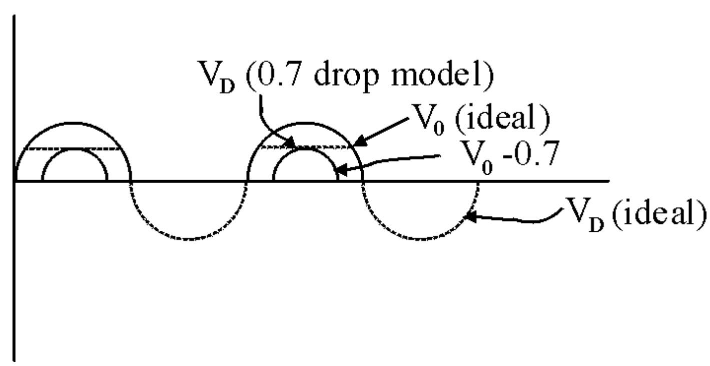
$$|A(jw)| \cong \frac{W_t}{W} = \frac{f_t}{f}$$



Diodes



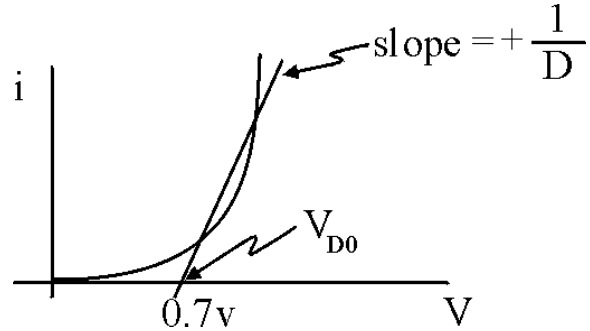
simplest model



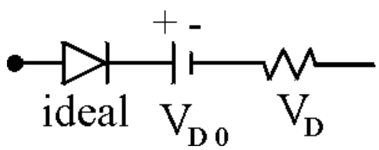
$i_D = I_S\,(e^{V_D/nV_T} - 1) \sim I_S\, e^{V_D/nV_T}$

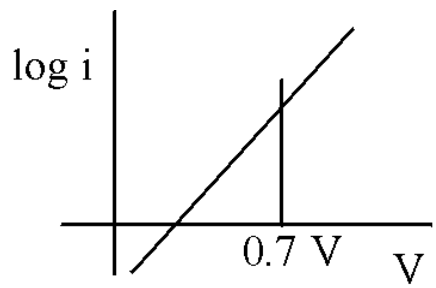
V_T = kT/q = 25mV at 25°

$$V_2 - V_1 = \underbrace{2.3\, n V_T}_{\approx 0.1 \text{ volts}} \log I_2/I_1$$



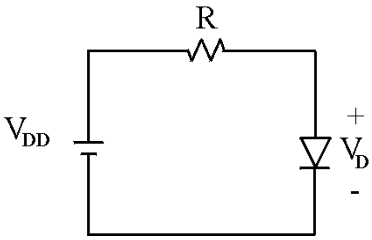
PWL model





Analysis of Diode Circuits

-

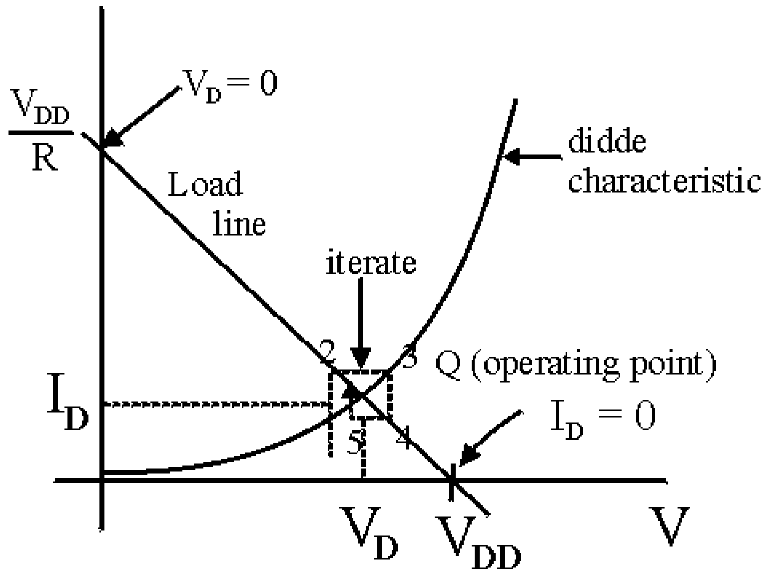


Algebraic method:

$$\left.\begin{array}{l} I_D = I_S\, e^{\frac{V_0}{nV_T}} \\ I_D = \dfrac{V_{DD}\ V_P}{R} \end{array}\right\}\ \text{Solve for } I_D \text{ and } I_D$$

(May need a computer program)

Graphical Method



e.g. 3.4 V_{DD} = 5V, R = 1kΩ , I_D = 1mm V_D = 0.7V, V_D changes by 0.1V/(decade I_D)

Iterative method

$$(1)\ \text{assume } V_D = \underbrace{0.7v}_{V_1\ \ I_1 = 1mm},\ (2)\ I_D = \frac{V_{DD} - V_D}{R} = \frac{5-0.7}{1k\Omega} = \underbrace{4.3mA}_{I_2}\ (\text{estimate } 1)$$

use in

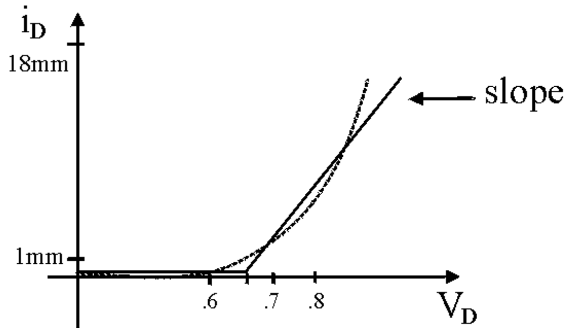
$$V_2 - V_1 = \underbrace{2.3n\ V_T}_{0.1}\log\frac{I_2}{I_1} \Rightarrow (3)\ V_2 = 0.7v + 0.1\log\frac{4.3\ ma}{1\ ma} = 0.7631$$

(4) assume V_D = 0.763 I_D = (5-.763)/1 = 4.237 ma

(5) V_D = 0.763 + 0.1 log 4.237/4.3 = 0.762 stop

p-spice works this way

Piece-Wise Linear Model



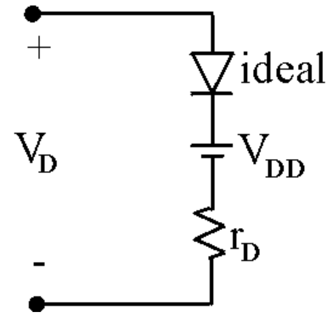
$i_D = 0$ for $V_D \le V_{DD} \leftarrow$ eg 0.65v

$i_D = \dfrac{V_D - V_{DD}}{r_D}$ for $V_D > V_{DD}$

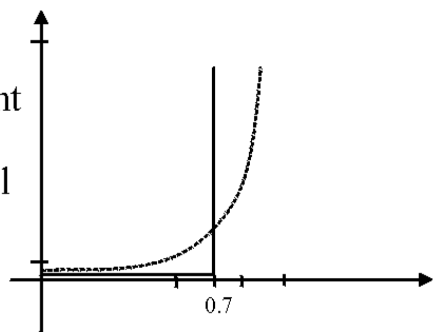
e.g. 20 Ω

if diode 10x area $\rightarrow V_D = 2\Omega$,

$V_{DD} = 0.65$v

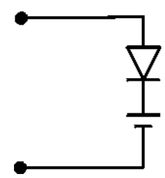


constant
V_D
model

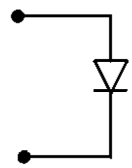


correct to ± 0.1V from 0.1 → 10mA good 1st approx

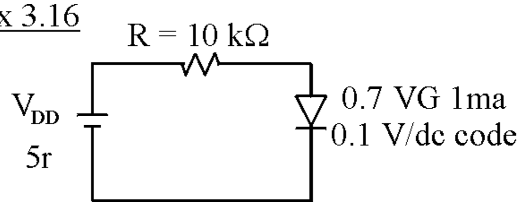
see eg 3.5



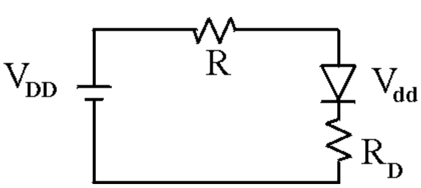
ideal
model
$V_D > 0.8$



ex 3.16



b) PWL $V_{DD} = 0.65$ $r_D = 20\Omega$



c) const V_D =0.7

. Iterative

$$V_D = 0.7\text{v} \rightarrow I_D = \frac{V_{DD} - V_D}{R} = \frac{5 - 0.7}{10k} = 0.43\text{ma}$$

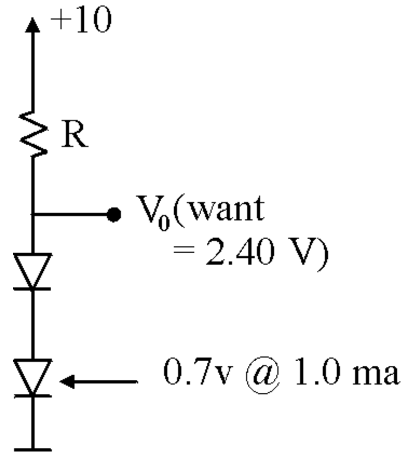
$$V_2 = 0.7\text{v} + 0.1\log_{10}\frac{.43}{1} = 0.663 \rightarrow I_D = .434\text{mA}$$

$$I_D = \frac{V_{DD} + V_{D0}}{R + r_D} = \frac{5 - 0.65}{10k + 20} = \frac{4.35}{1020} = 0.434\text{mA}$$

$$I_D = V_{DD} + I_D V_D = 0.65 + 0.434\text{x}10^{-3}(20) = 0.659\text{V}$$

$$I_D = \frac{V_{DD} - V_{D0}}{R} = \frac{5 - 0.7}{10k} = 0.43\text{mA} \qquad V_D = 0.7\text{V}$$

Ex D3.18

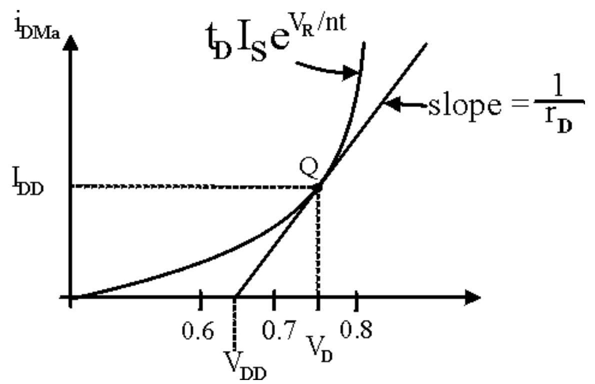


Want each diode to drop 0.8v

∴ need 10mA current since 0.761 + 0.1 v/decade

$V_2 = 0.7 + 0.1 \log I_2/ = 0.8$

Small Signal Model

		$i_D(t) \cong I_S e^{(V_D+V_d)/nV_T}$ $= \underbrace{I_S e^{V_D/nV_T}}_{I_D} e^{V_d/nV_T}$
If $V_d << nV_T$ (<10mV) $\Rightarrow i_D \cong I_D (1+V_d/nV_T)$		small signal approximation
$i_D(t) = \underbrace{I_{D0}}_{\text{dc current}} + \underbrace{\frac{\overbrace{I_{D0}}^{1/r_D}}{nV_T} V_d(t)}_{\text{small signal componet}}$	$r_d = \frac{nV_d}{I_D}$	diode small signal resistance

Note:

$$r_d = \frac{1}{\left.\frac{\delta i_D}{\delta V_D}\right|_{i_D=I_D}}$$

$$\text{since } \left.\frac{\partial i_D}{\partial V_D}\right|_{i_D=I_{DQ}} = I_D \frac{1}{nV_T} e^{V_d/nV_T} = \left.\frac{i_D}{nV_T}\right|_{i_D=I_{DR}} = \frac{I_D}{nV_T} = \frac{1}{\sqrt{d}}$$

diode small signal conduct

total current

$$\text{at } I_D,\ V_D = V_{d0} \Rightarrow i_D = \frac{1}{r_D}(V_D - V_{D0})$$

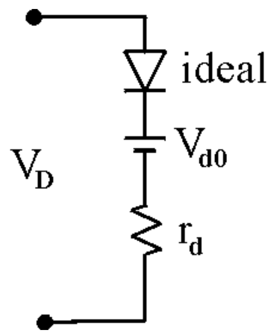
$I_D + i_d$

$$\Rightarrow V_D = V_D + \underbrace{i_d\, r_d}_{V_d}$$

total voltage

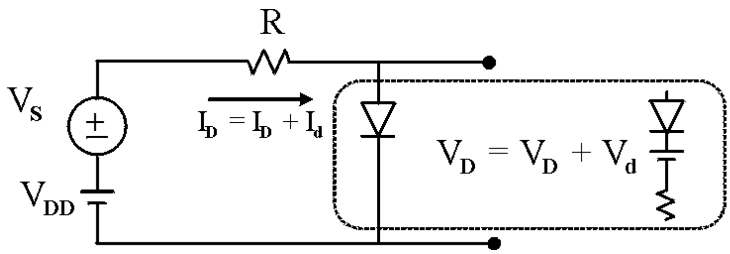
bias pt dc voltage

incremental voltage



small signal model

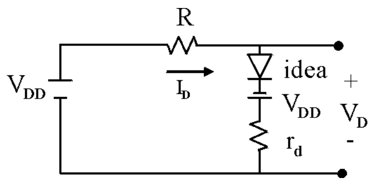
Separate dc bias analysis & signal analysis



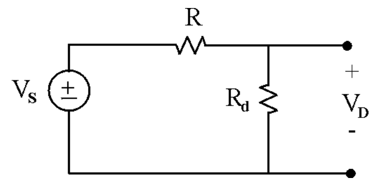
$$\underbrace{V_{DD}} + \underbrace{V_S} = i_D R + V_{D0} + i_d r_d$$

$$= \underbrace{I_D R + V_D} + \underbrace{i_d(R + r_d)}$$

Sum the results of 2 analyses:



$V_{DD} = I_D R + V_d$
dc analysis



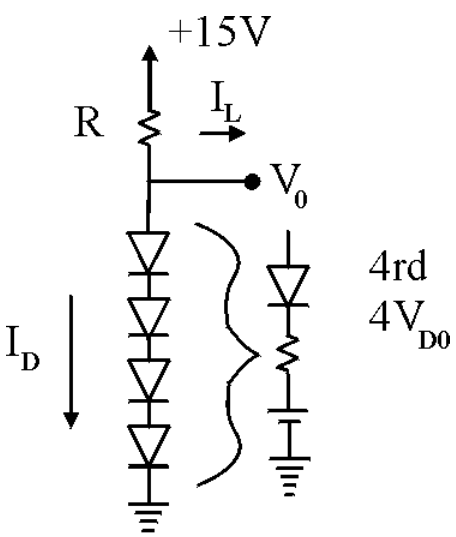
$V_S = i_d(R + r_d)$

small signal analysis

note:

$$V_d = V_S \frac{r_d}{R + r_d} \text{ (voltage divide)}$$

ex D 3.23



want V_0 = 3V when I_L = 0; r V_0/ r I_L = 40mV/1ma;

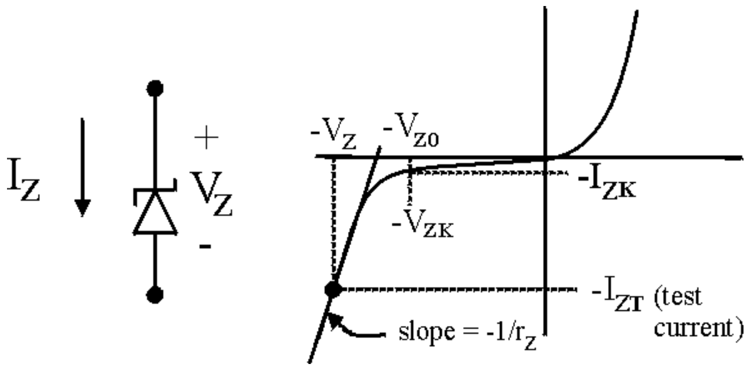
what is R? what's Area of VEN rel. to 1ma, n=1

- $4V_D = 3V$ @ $I_L = 0 \Rightarrow V_D = 0.75V$
- $4r_d = 40mV/1ma \Rightarrow r_d = 10\Omega$; $r_d = nV_T/I_D = 25mV/I_D$ for n = 1 $\Rightarrow I_D = 35mV/10\Omega = 2.5mA$
- at $I_L = 0$, $(15\text{-}3)V = (2.5mA)R \Rightarrow R = 4.8k\Omega$
- Relative Junction Area α I_S

$$I_D \cong I_S e^{V_0/nV_T}\ ;\ \left.\begin{array}{l} 2.5mA = I_S\, e^{.75/25mV} \\ 1\ mA = Is_1 e^{.7/25mV} \end{array}\right\} \frac{I_S}{Is_1} = \frac{2.5/e^{.75/.025}}{1/e^{.7/.025}} = \frac{2.5}{e^2} = .338$$

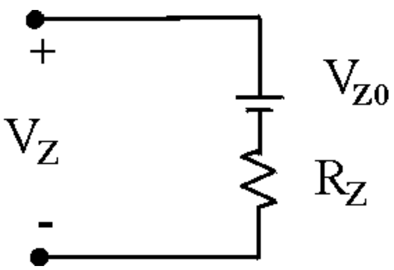
H.W. Probs 3.48, 3.57, D3.50, 3.68; Collect on Monday

Zener Diodes



- operate in breakdown region
- good for regulation because of steep slope
- close to linear; incremental or dynamic resistance r_z

Model



$$V_Z = V_{Z0} + r_Z I_Z$$

intercept (get from test spor)

a few Ω

I increases rapidly from I_{sat} at $-V_{zk}$ → avoid knee region of operation $I > I_{zk}$

see e.g. 3.8

Zener Shunt Regulator

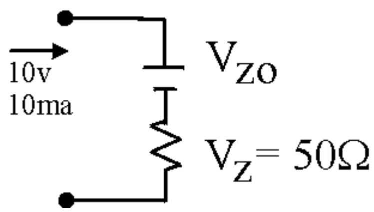
e.g. 3.9 choose $R = \dfrac{V_{smin} - V_{Z0} - r_Z I_{zmin}}{I_{zmin} + I_{Lmax}}$ from $I = \dfrac{V_S - \overbrace{V_Z}^{V_{Z0} + r_Z I_Z}}{R} = I_{zmin} + I_{Lmax}$

Note: V_Z is temperature dependent TC in mV/° C

<5V → neg TC   >5v→posTC   design w. combo

forward diode -2mV/0C

ex 3.24

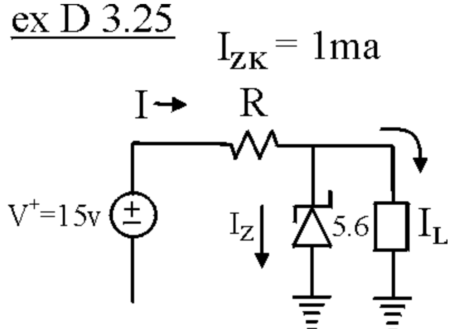


$V_Z = V_{Z0} + I_Z T_Z V_{Z0} = 10v – 10ma (50) = 9.5V$

V_Z (5ma) = 9.5 + (5ma)(50) = 9.75V

V_Z (20ma) = 9.5 + (20ma)(50) = 10.5V

ex D 3.25



$V_z (I_z > 5I_{ZK}) = 5.6V$ const I_z: 0-15ma, R?

$R_Z = 0, V_{Z0} = 5.6$

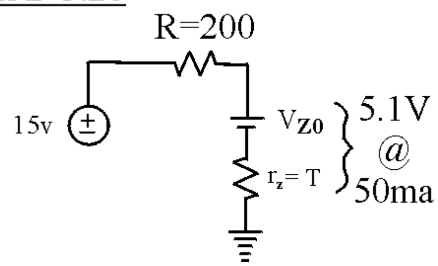
want I_{zmin} = 5ma I_{Lmax} = 15 ma

$$R = \frac{VsVz}{I_{Zmin} + I_{Lmax}} = \frac{15 - 5.6}{20ma} = 470\Omega$$

$$Pz\,(\text{max power})\text{ at } Iz(I_L = 0) = \frac{Vs - Vz}{R} = \frac{15 - 5.6}{470} = 20ma;\; Pz = Iz \cdot Vz = 20ma \cdot 5.6V$$

112mW

ex D 3.26



I_Z = (15-4.75)/(200 + 7) = 20

V_{Z0} = 5.1V – (50ma) 7 = 4.75V

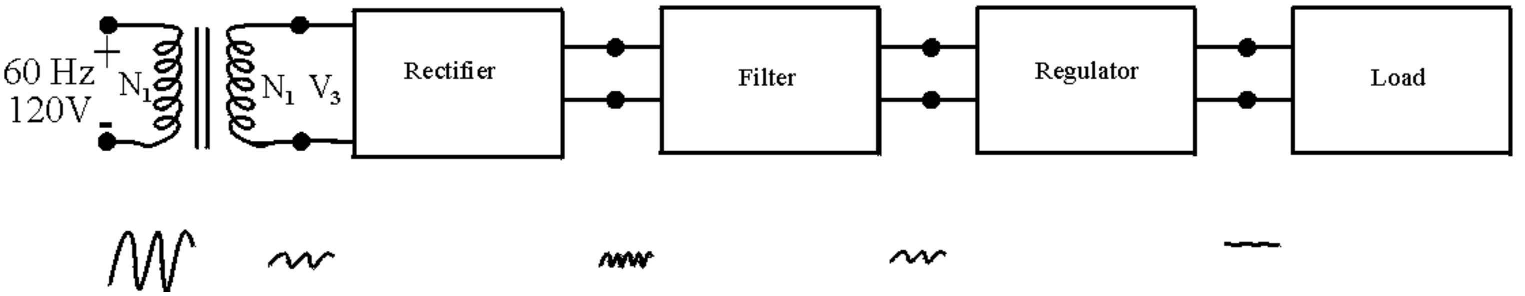
V_Z (I_L = 0) = V_{Z0} + $I_Z r_z$ = 4.75 + (50ma) 7 = 5.1V

line reg = r_z / (R + R_Z) = 7/207 = 33.8 mV/V

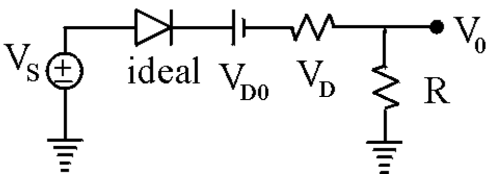
Load reg = -(r_z || R) 1/LR = 1/r_z + 1/R = (R + r_z)/(R r_z)

= -7(200)/207 = -6.8 mV/mA

Rectifier Circuits

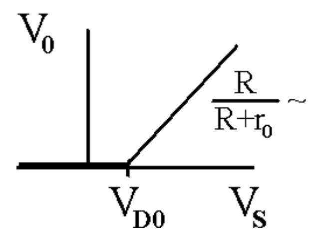


Half-wave rectifier



$V_0 = 0$; $V_S < V_{V0}$

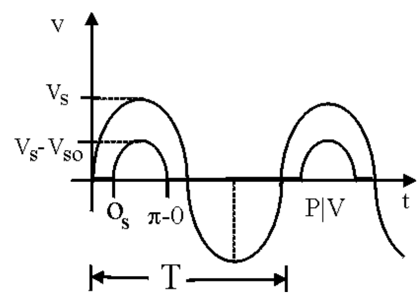
$V_0 = R/(R + r_D)V_S - V_{D0}\, R/(R+r_D)$; $V_S \geq V_{D0} \cong V_S - V_{D0}$ ($r_s << R$)



Important Specs: -peak current, P| voltage

- choose ~ 50% greater than 1/3

<u>ex 3.27</u> neglect r_D; $V_S = V_S \sin\theta$, $V_0 = V_S \sin\theta - V_{D0}$ ($V_S > V_{D0}$)



$$\sin\theta = \frac{V_{D0}}{V_S} \text{ at conduction} \Rightarrow \theta_{start} = \sin^{-1}\frac{V_{\infty}}{V_S};\ \theta_{end} = \pi - \theta_{start};\ \text{total} = \frac{\pi - 20}{\text{cycle}}$$

.

b)

$$\text{average dc level } \frac{\int_{\theta_s}^{\theta_c} V_0(\theta)d\theta}{\int_0^{2\pi} d\theta} = \frac{V_S}{2\pi}\left[\cos(\sin^{-1}\frac{V_{D0}}{V_S}) - \cos(\pi - \sin^{-1}\frac{V_{D0}}{V_S})\right] - \frac{V_{D0}}{2\pi}[2\theta - \pi]$$

$$\text{if } V_{D0} << V_S \qquad \cong \frac{V_S}{\pi} - \frac{V_{D0}}{2}$$

c) Peak diode current $I_{peak} = (V_S - V_{D0})/R$

V_S(rms) = 12 V_{D0}=0.7V, R = 100

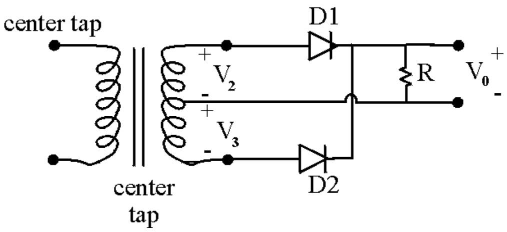
V_S(peak)=12 √ 2

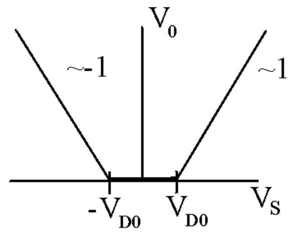
. θ = sin^{-1}(.7/17) = 2.4° conduction Û = 175° /360°

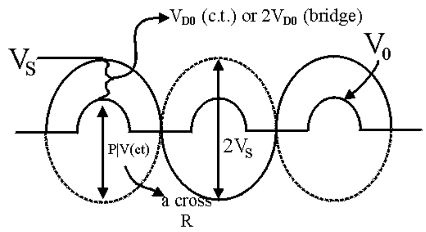
b. V_{dc} = 1/π 17 - .7/2 = 5.4-.34 = 5.06V

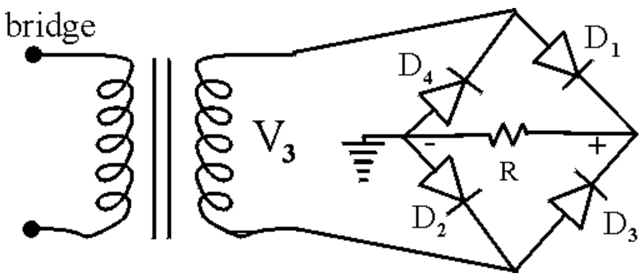
c. I_{peak} = 17-.7/ = 163ma ; P|V = 12√ 2 = 17V

Full Wave Rectifiers





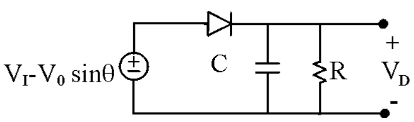


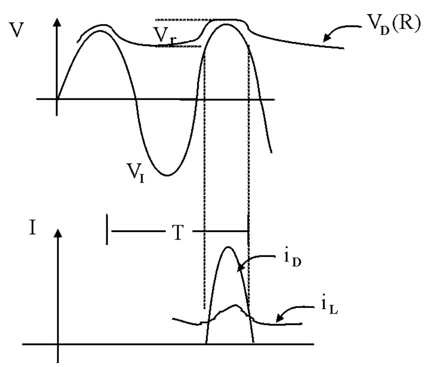


P|V = $2V_S - V_{DD}$ (center top)

P|V = $V_3 - 2V_{D0} + V_S - V_{D0}$ (bridge)

Peak Rectifier





want CR >> T

$i_L = V_0/R$

$i_D = i_C + i_L$

$= C(dV_0/dt) + i_L$

V_R is peak to peak ripple voltage

V_0 varies from V_P to $V_P - V_T \sim V_P$ for CR >>T

V_{0avg} = output dc voltage = $V_p - 1/2V_r$

during diode off $V_0 = V_p$ e , at end of T $V_P - V_r \cong V_p$

$\Rightarrow V_r \cong V_p$ T/CR for CR >> T ; for $V_r \ll V_p$ $I_L \cong V_P/R$ (~ const)

conduction interval r t; V_p cos (w r t) = $V_P - V_r$

for small lw r t cos(w r t) $\cong 1 - ½$ (w r t)^2

$$\Rightarrow w\Delta t = \sqrt{\frac{2V_r}{V_p}}$$

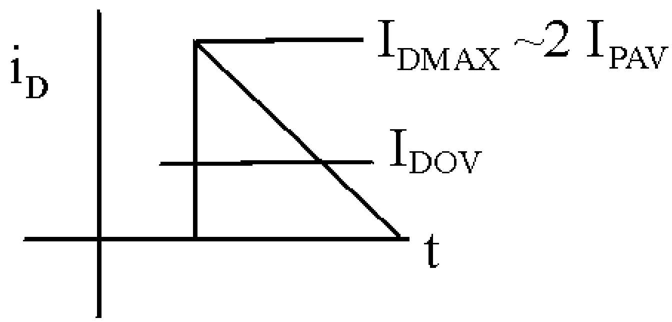
$Q_{supplied}$ (r t) to C = i_{cavg} r t Q_{lost} = CV_r

$$i_{Davg} = I_L\left(1+\pi\sqrt{\frac{2V_P}{V_R}}\right) \gg I_L \text{ for } V_r << V_P$$

i_D at onset ($t = -\Delta t$) use $i_D = C\frac{dv}{dt} + i_L$

$V_r \cos(w\varepsilon\Delta t)$

$$i_{Dmax} = I_L\left(1+2\pi\sqrt{\frac{2V_P}{V_r}}\right)$$



<u>Full wave peak rectifier</u>

$V_r = \frac{V_P}{2fCR}$ - need C only half as large (ripple freq is 2x $T \rightarrow T/2$)

$i_{Dav} = I_L\left(1+\pi\sqrt{\frac{V_P}{2V_r}}\right)$; $i_{Dmax} = I_L\left(1+2\pi\sqrt{V_P/2V_r}\right)$ currents in each diode are half size

Take V_{D0} into account $V_P \rightarrow V_P - V_{D0}$ ½ w + CT $V_P \rightarrow V_P - 2V_{D0}$ bridge

Bridge rect + filter C across R, trans. secondary 12V(rms)@6V $V_{D0} = 0.8V$, $R = 100\Omega$

ex D3.30 ? C for IV p-p ripple

$$V_r = \frac{V_P - 2V_{D0}}{2fCR} = 1V \Rightarrow C = \frac{V_P - 2V_{D0}}{2fRV_r} = \frac{12\sqrt{2} - 1.6}{2 \cdot 60s^{-1} \cdot 100\Omega} = 1283\mu F$$

$$V_0 \cong V_P - 2V_{D0} = 15.4 \quad V_0(\text{better est.}) = V_P - 2V_{D0} - V_r/2 = 14.9V$$

$$I_L = V_0/R = 0.149A$$

$$\text{condition angle } W\Delta t \cong \sqrt{\frac{2V_r}{V_p - 2V_{D0}}} = \sqrt{\frac{2}{15.4}} = .36 \text{ rad} = 20.6^\circ$$

$$\dot{i}_{DaV} = I_L\left(1 + \pi\sqrt{\frac{V_P - 2V_{P0}}{2V_r}}\right) = .15\left(1 + 3.14\sqrt{\frac{15.4}{2}}\right) = 1.44A$$

$$P|V = V_D - V_{D0} = 17 - 0.8 = 16.2V$$

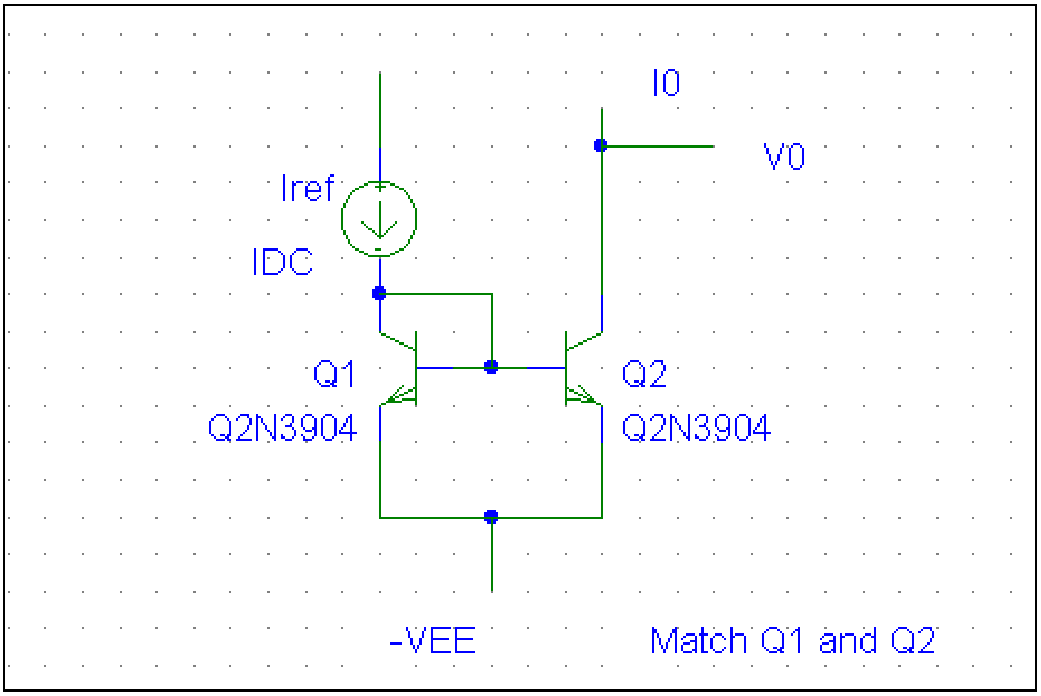
$$\dot{i}_{Dmax} = I_L\left(1 + 2\pi\sqrt{\frac{V_P - 2V_{\pi 0}}{2V_r}}\right) \cong 2.7A$$

$\Bigg\}$ Select diode w 30% margin

<u>4A, 20V</u>

Simple BJT Current Source

Current Mirror



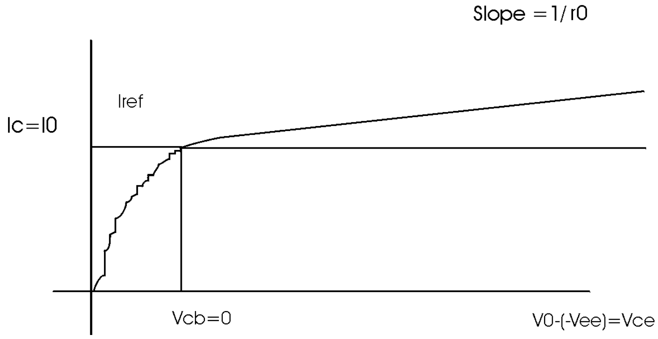
$I_0 = I_{REF}$ if:

. Q2 is in the active region [$V_0 > V_B(Q_2)$]

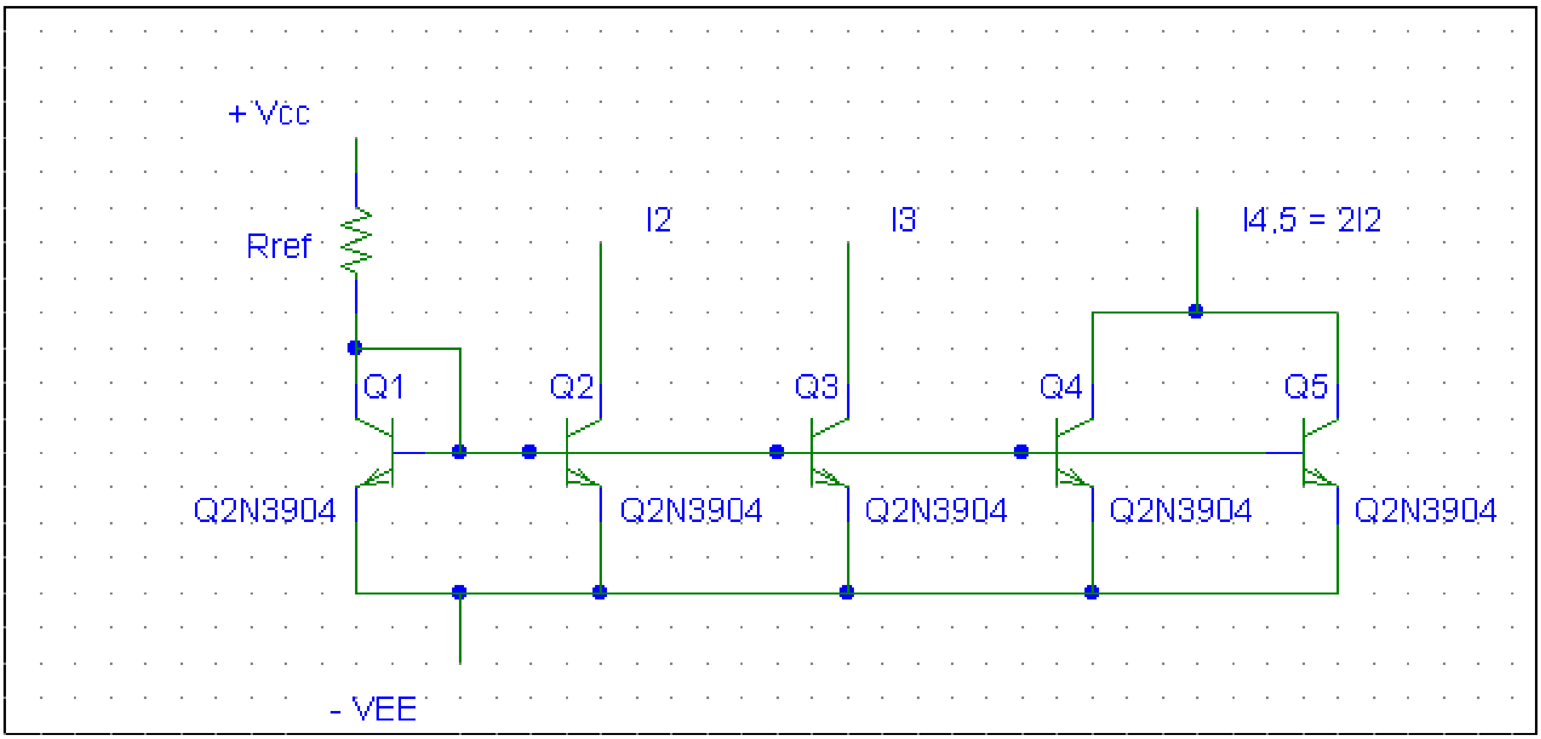
b. B goes to infinity

c. r_0(Q2) goes to infinity

$$I_0 \approx \frac{I_{REF}}{1+\frac{2}{B}}\left(1+\frac{V_0+V_{EE}-V_{BE}}{V_A}\right)$$



Current Source Circuit



Choose R_{REF} so that:

$$I_{REF} = \frac{V_{CC} - V_{BE} - (-V_{EE})}{R_{REF}}$$

MOSFETs or IG FETs

These is a four terminal device consisting of the Body, source Gate and Drain.

IG FET (Insulated Gate Field Effect Transistor)

unipolar device ie current is: electrons for nFET

holes for pFET

MOSFET (Metal –Oxide- Semiconductor FET)- only silicon has a good oxide

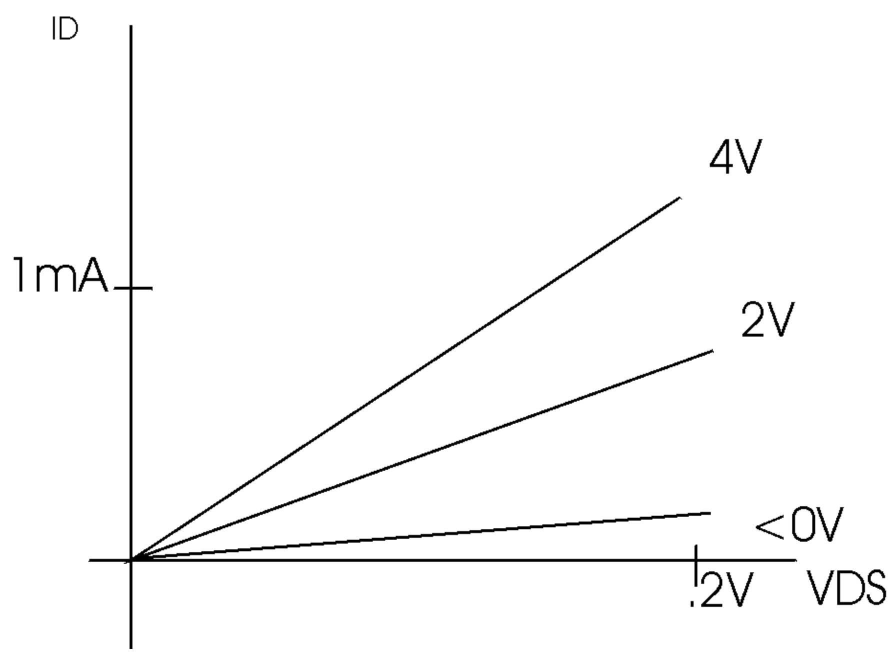
As V_{GS} increases from zero, holes are repelled from surface (depletion) and electrons are attracted from the source and drain (accumulation).

An n-inversion layer forms creating a path (channel) from the source to the drain at

$V_{GS} = V_t$ (threshold voltage) {Note: this is not V_T which is the thermal voltage = 25mV @ T = 25 C.}

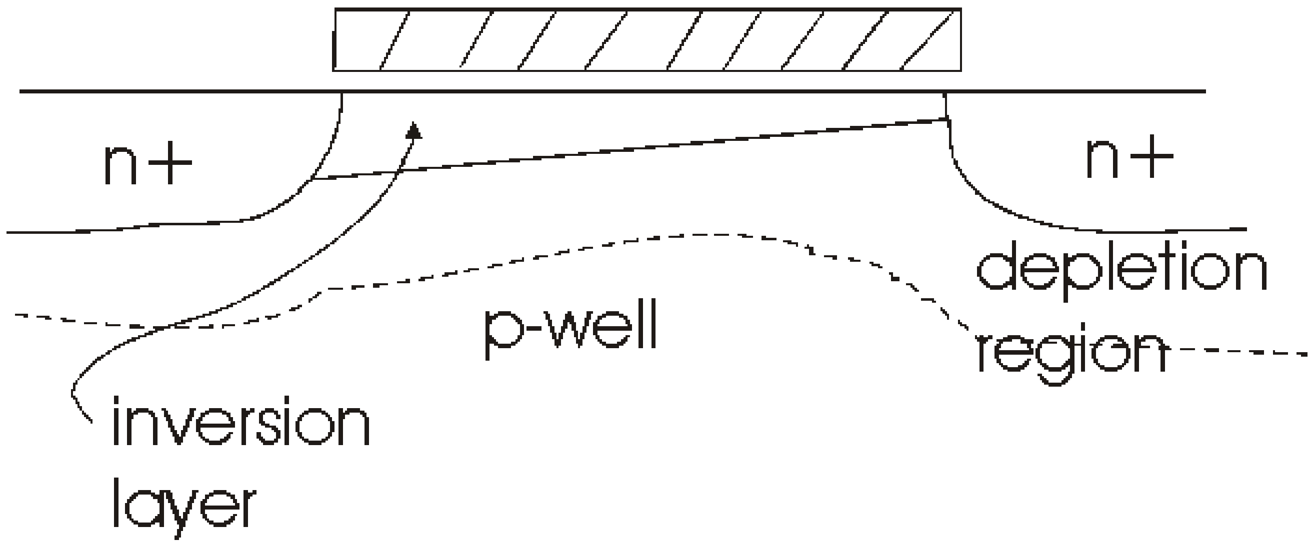
If V_{DS} is above zero, current flows across channel

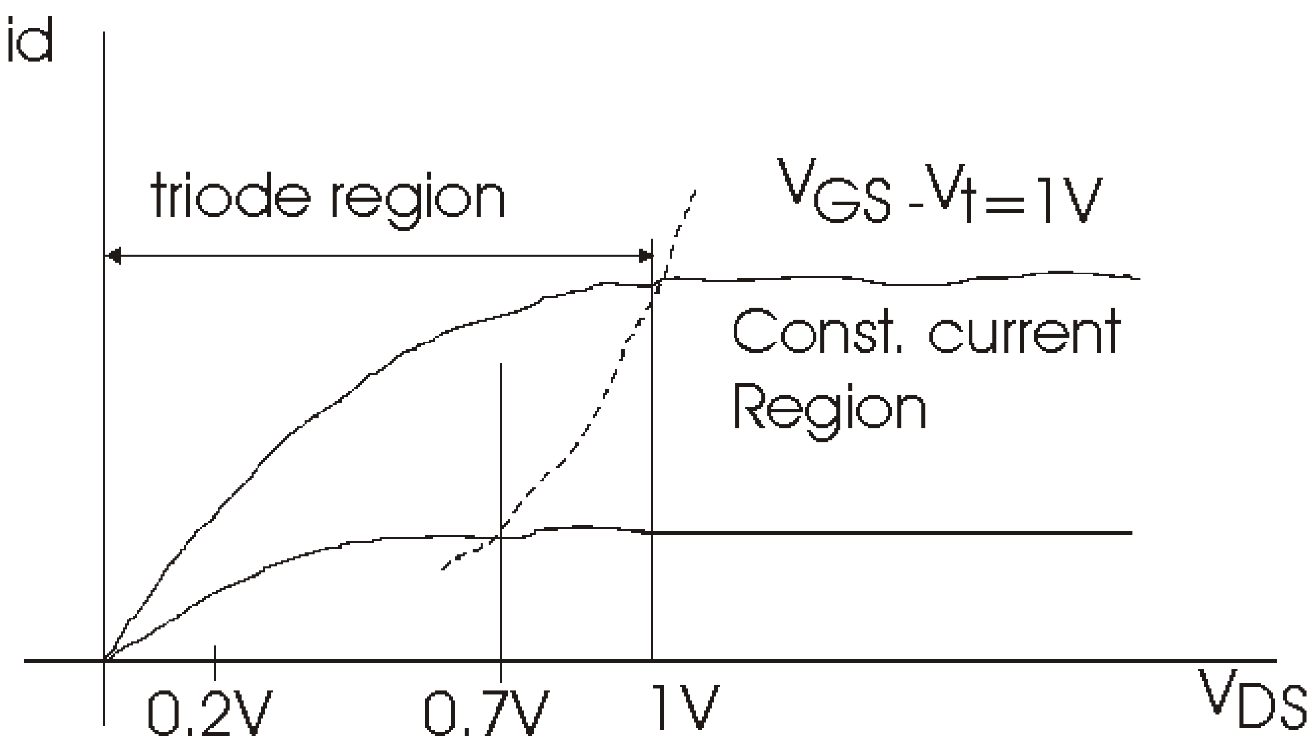
For small V_{DS} this current is linear with $V_{GS} - V_t$ (excess gate voltage) and is also linear with V_{DS} (voltage controlled resistor)



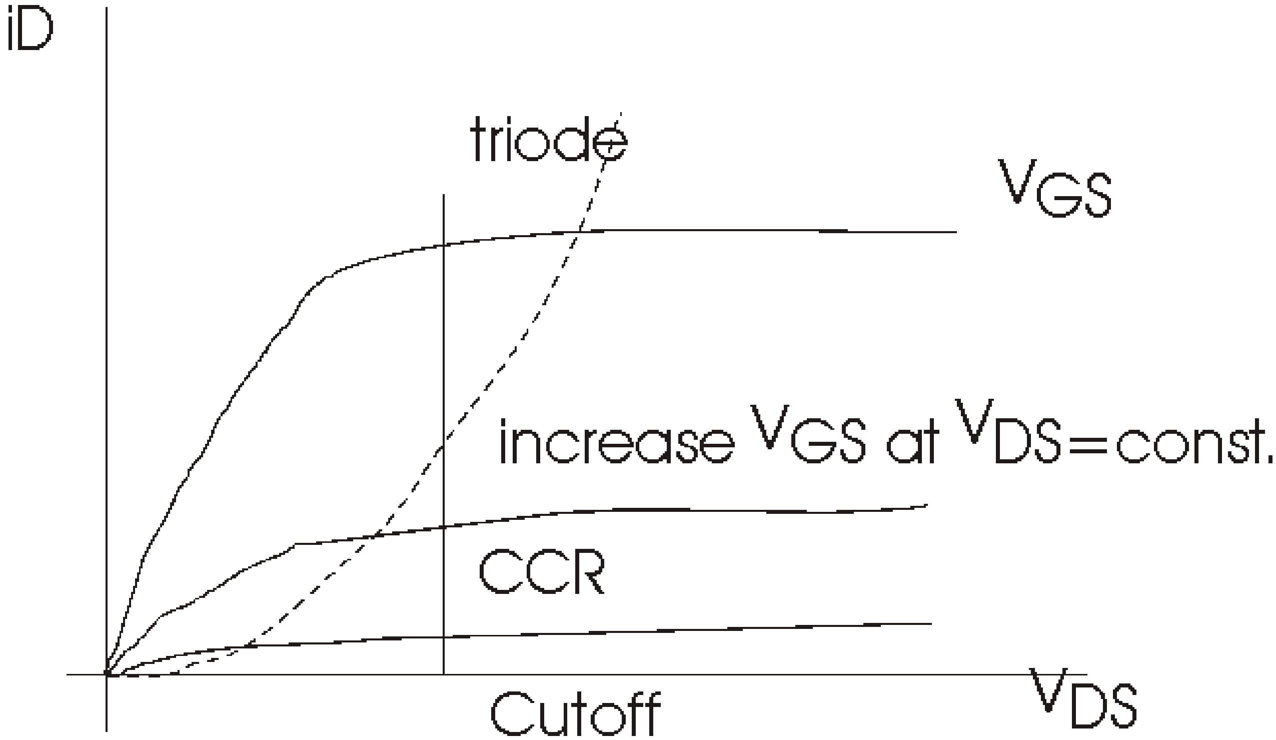
Effect of Increasing V_{DS}

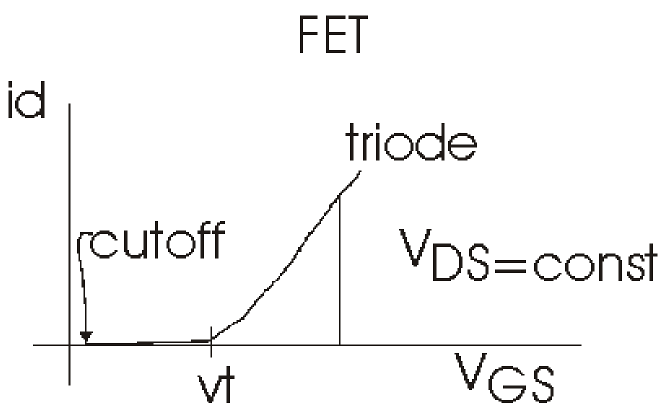
The voltage between the gate and channel depends on location along channel length and decreases from source to drain. As V_{DS} increases, channel tapers and becomes more resistive at the drain end. When V_{GS}-V_{DS} =V_t , the channel "pinches off" at the drain. Increasing V_{DS} beyond V_{GS}-V_t does not increase current. (This is known as the constant current region; and is also known as saturation, unfortunately).

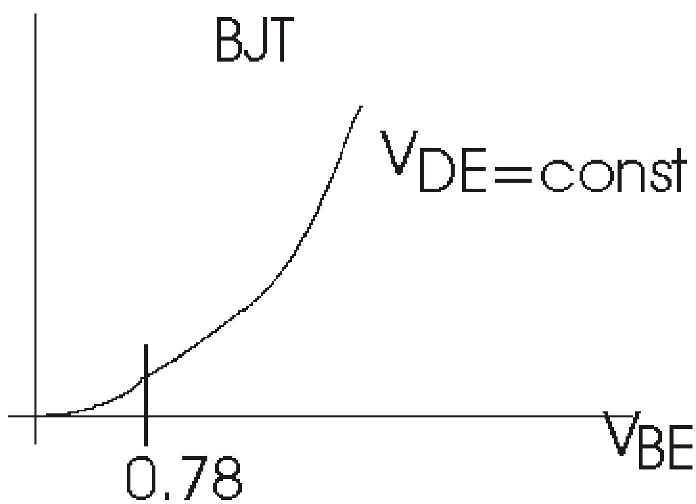


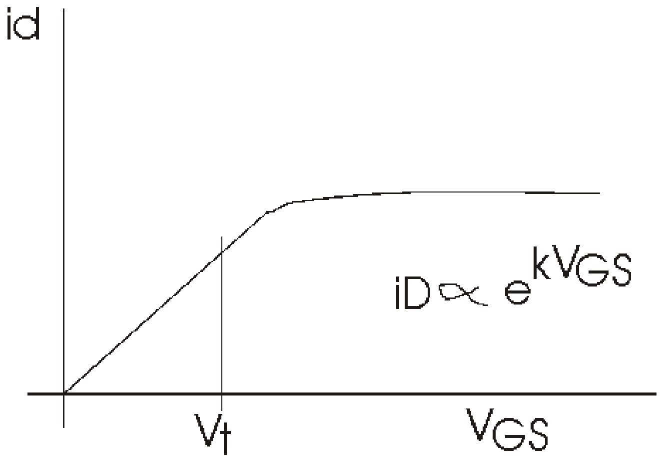


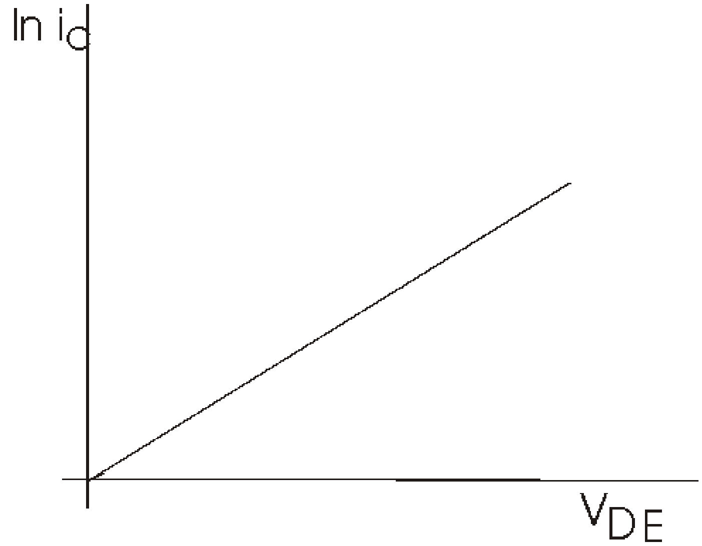
Sub-Threshold Region



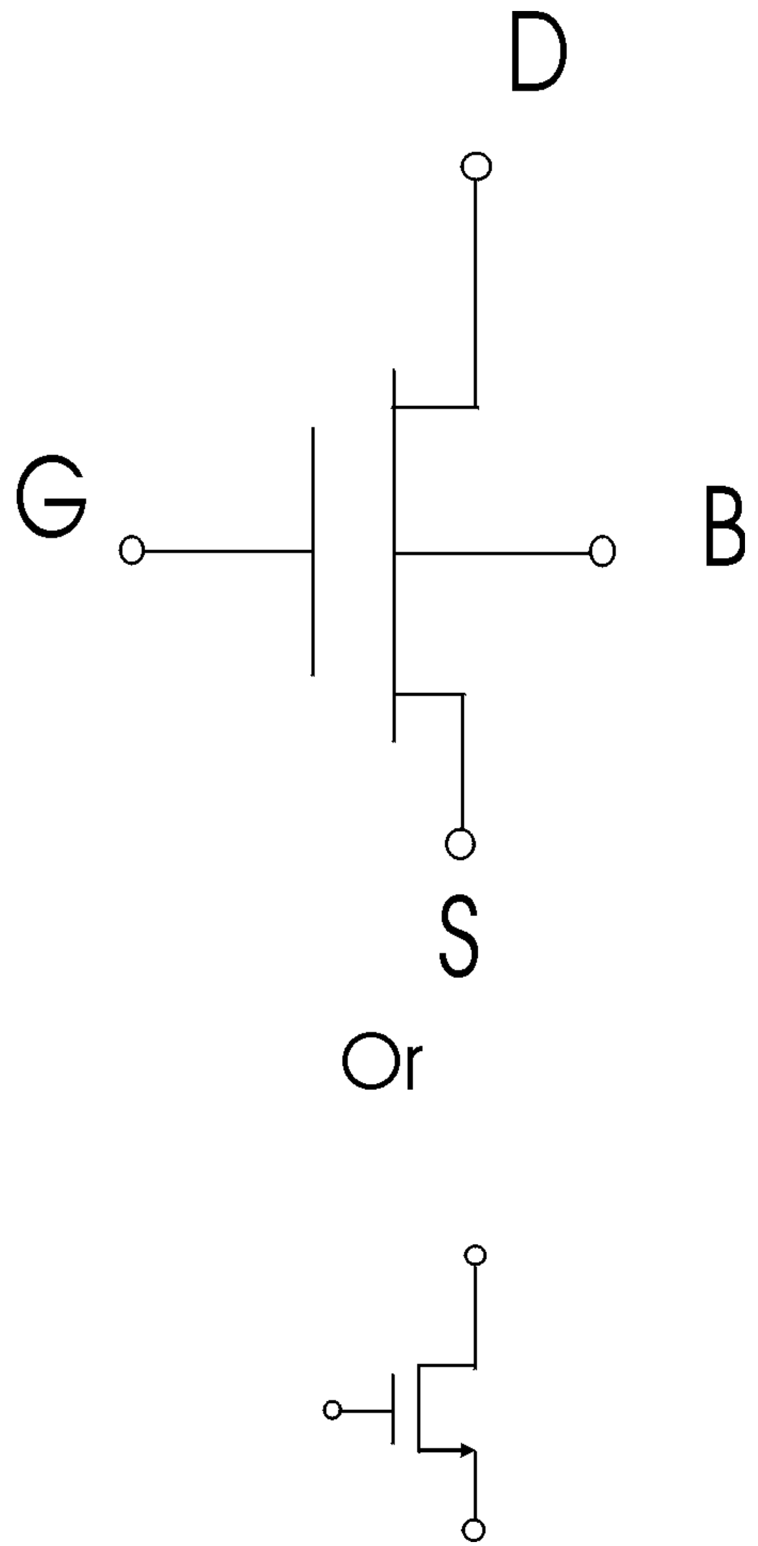


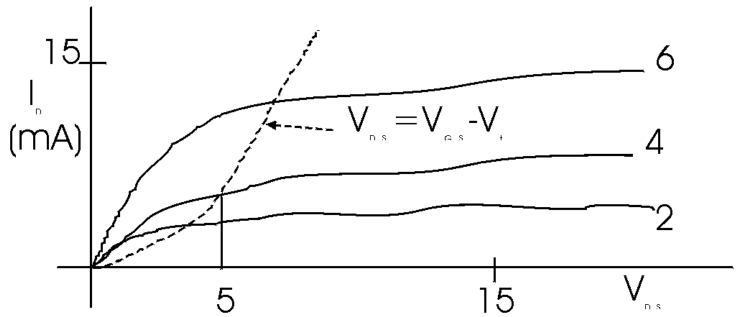



id
iD ∝ e^kVGS
Vt
VGS


ln ic
VDE

MOSFET I-V Characteristics





Triode Region:

$$V_{GD} \equiv V_{GS} - V_{DS} > V_t \quad \text{where } V_{DS} \text{ is small}$$

$$i_D = K\left[2(V_{GS} - V_t)V_{DS} - V_{DS}^2\right] \text{ where } K = \frac{1}{2}u_n C_{ox}\left(\frac{w}{l}\right)$$

u_n : electron mobility in n channel

C_{ox} : oxide capacitance

Constant Current Region (pinchoff):

$$V_{GS} - V_{DS} \equiv V_{GD} \leq V_t$$
$$V_{DS} \geq V_{GS} - V_t$$

The constant current I_D equation is as follows:

$$i_D = K(V_{GS} - V_t)^2$$

The equation comes from substituting $V_{DS} = V_{GS} - V_t$ into the triode equation.

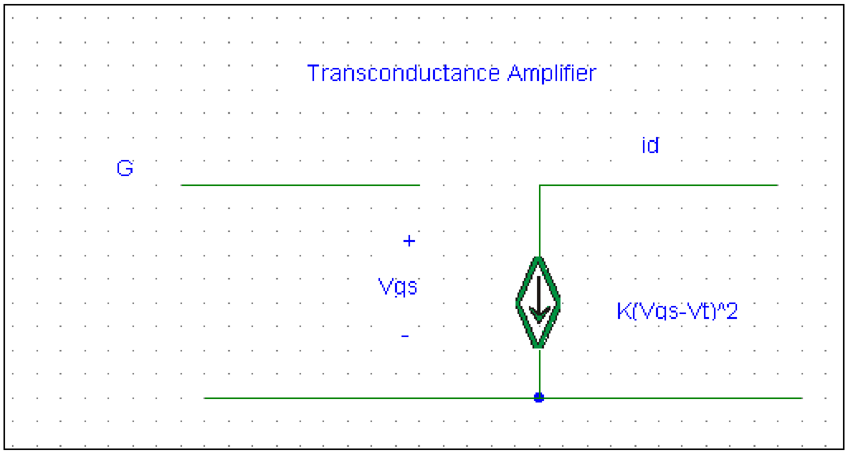
The boundary of the constant current region is given by:

$$i_D = K V_{DS}^2$$

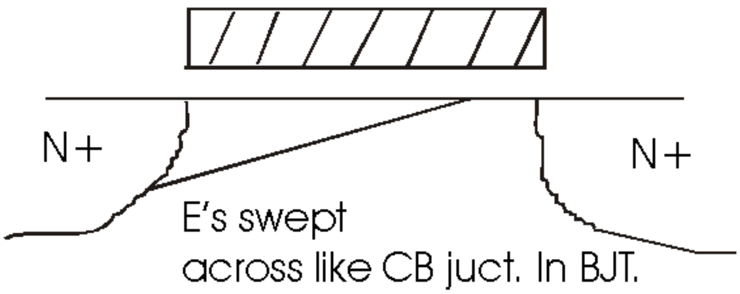
Notes:

$k'_n = u_0 C_{ox}$: process transconductance parameter.

$K = \frac{1}{2}k'_n\left(\frac{w}{l}\right)$: can be set by the designer.


Transconductance Amplifier
id
G
+
Vgs
-
K(Vgs-Vt)^2

Finite Output Resistance ro



As V_{DS} increases, pinch off point moves toward source -channel length modulation.

$$K \alpha \frac{w}{l}; \ \frac{\Delta l}{L} = \lambda_n V_{DS}$$

$$\lambda \approx \frac{0.1 \mu n V^{-1}}{L}$$

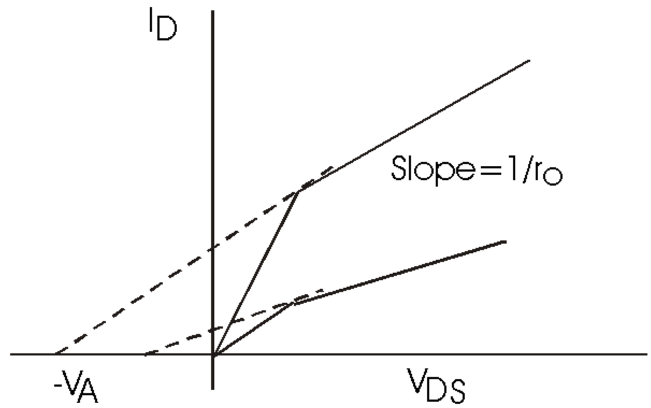
So, K (effective increases)

$$i_D = K(V_{GS} - V_t)^2 [1 + \lambda v_{DS}]$$

$$\text{x - intercept at } v_{DS} = \frac{1}{-\lambda} = -V_A$$

$$\text{if } V_A \approx 100V, \quad \lambda \approx 0.01$$

$$i_D = K(V_{GS} - V_t)^2 \left[1 + \frac{v_{DS}}{V_A}\right]$$

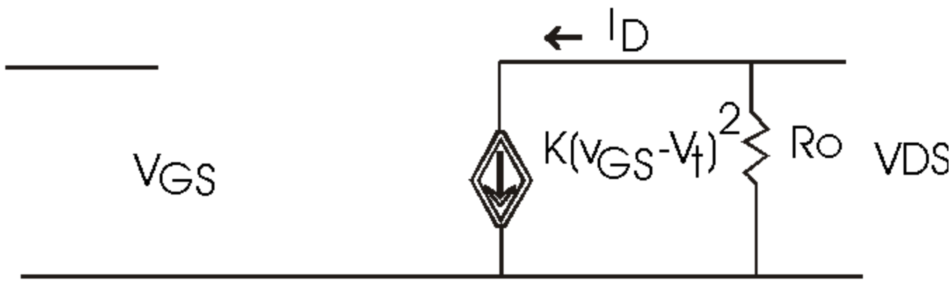


$$r_0 \equiv \frac{1/\partial i_D}{\partial v_{GS}} \text{ evaluated at } v_{GS} = const.$$

$$= \frac{1}{\lambda K (v_{GS} - v_t)^2} \approx \frac{1}{\lambda I_D} \quad \text{or we can say}$$

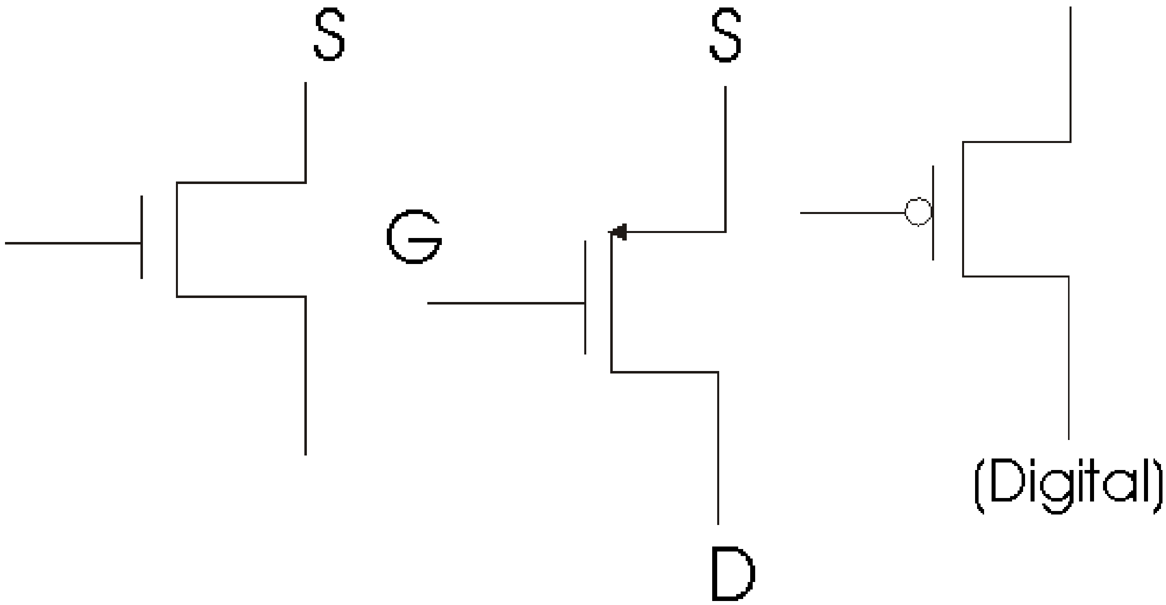
$$r_0 = \frac{V_A}{I_D}$$

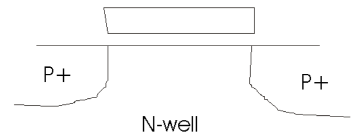
Large Signal nMOS Model in CCR



ID
VGS
K(vGS-Vt)2
Ro
VDS

P-Channel MOSFET





$$V_{GS} < V_t \text{ to induce channel}$$
$$\text{(enhancement normally off)}$$

$$i_{D(\text{triode})} = K\left[2\left(v_{GS} - V_t\right)v_{DS} - v_{DS}^{\;2}\right] \qquad \mu p \approx \frac{1}{2}\mu n$$

$$K = \frac{1}{2}\mu p Cox\left(\frac{w}{l}\right)$$

$$k'p = \mu p Cox$$

$$v_{DS} \le v_{GS} - V_t \text{ for pinchoff} \quad (\text{"}\ge\text{" for nFET})$$

CCR:

$$i_{D(CCR)} = K\left(v_{GS} - V_t\right)^2\left(1 + \lambda v_{DS}\right)$$

MOSFET vs. BJT Circuits

1. MOS

- infinite output resistance
- very useful for voltage source with high R's in common source ckt
- can't be used for current source input

2. MOS

BJT

$-\, gm \,\alpha \sqrt{I_D}$ - relatively small $< 1 \frac{\mathrm{mA}}{\mathrm{V}^2}$

$gm \,\alpha\, \mathrm{I_C}$ - relativley large

good for amplifiers

3. CMOS

-high density, low power.(approx. zero static power)

- dominant technology for digital ckts.

Body Effect- Backgate Bias

As V_{BS} (backgate bias) goes negative, the depletion region deepens; Also, V_t increases

B is like another gate; (back gate)

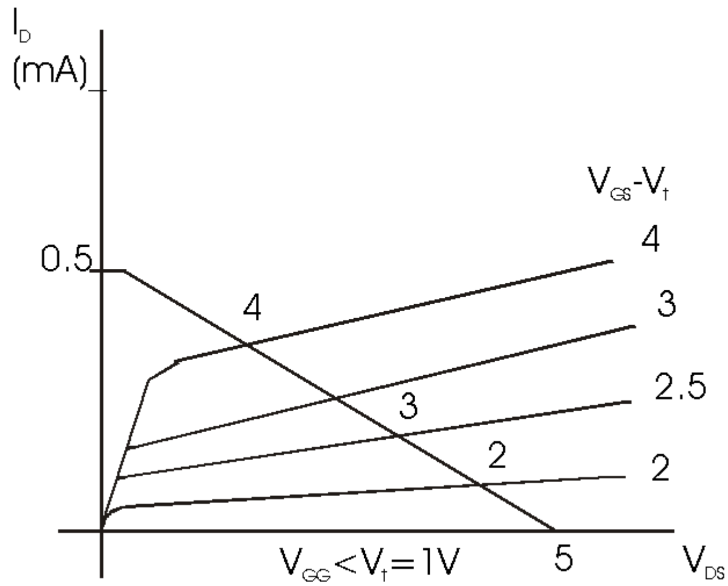
<u>Punch-Through</u> - at V_{DS} > 20V or so, the depletion region from the drain "reaches through" to source and current increases rapidly.

<u>Avalanche Breakdown</u> V_{gB} > 50V electron/hole pair creation at junction.

<u>Oxide Breakdown</u> V_{GS} >50V current between the gate and substrate causes permanent damage; usually due to static buildup.

- input protection is important at the pads.

MOSFET Bias



Source Resistor bias

Want $V_{DS} > V_{GS} - V_t$ for CCR region

$I_S = I_D$ (like β = infinity);

Set this by $K(V_{GS} - V_t)^2$

And $V_S = -V_{SS} + I_S R_S$

And $V_D = V_{DD} - I_D R_D$

Can set V_{GG} by a parallel resistor setup (See figure below)

FET-DC exercises

Ex 5.12 (5.1)

0.4mA=I_D = K $(V_{GS}-V_t)^2 = 0.4\frac{mA}{V^2}(V_{GS}-2)^2$

$(V_{GS}-2)^2 = 1$; $V_{GS} = 3, \text{need } V_{GS} > V_t$

Since, V_G = 0 V_S =-3V.

$$R_S = \frac{V_S - V_{SS}}{I_D} = \frac{-3-(-5)}{0.4} = 5k \text{ ohms}$$

For V_D =1V; $R_D = \frac{V_{DD} - V_D}{I_D} = \frac{(5-1)mA}{0.4V} = 10k \text{ ohms}$

<u>What is the largest R_D for the CCR region?</u>

-

Need $V_{DS} > V_{GS} - V_t$ (like $V_C > V_B$ in BJT.)

$$V_D - (-3V) > 0 - (-3V) - 2V \Rightarrow V_{D\,\mathrm{MIN}} > -2V$$

$$R_{D\,\mathrm{MAX}} = \frac{V_{DD} - V_{D\,\mathrm{MIN}}}{I_D} = \frac{[5-(-2)]V}{0.4mA} = 17.5k \text{ ohms}$$

ex 5.13 (eg 5.2)

<u>Q1: Design R for I_D = 0.4mA</u>

$$V_D - V_G = 0 \Rightarrow V_D > V_G - V_t$$

$$\therefore\ I_D = K\left(V_{GS} - V_t\right)^2 = 0.1\frac{mA}{V^2}\left(V_G - 2\right)^2 = 0.4mA$$

$$V_G = 4, \text{and } V_D = 4$$

$$\therefore\ R = \frac{V_{DD} - V_D}{I_D} = \frac{10-4}{0.4} = 15k \text{ ohms}$$

Q2:

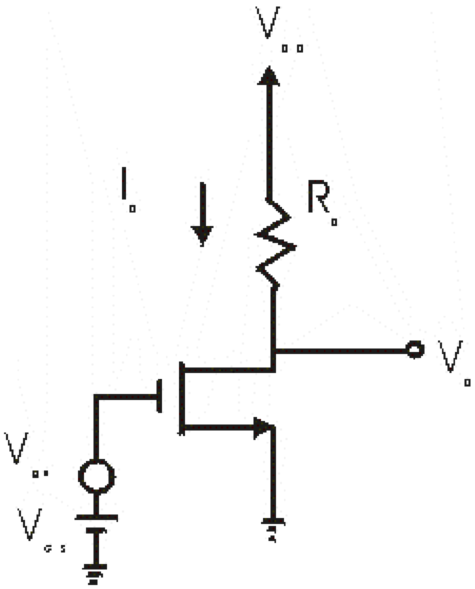
$$I_{D2} = K\left(V_{GS} - V_t\right)^2 = 0.1(4-2)^2 = .4mA \ \text{(Curent Mirror)}$$

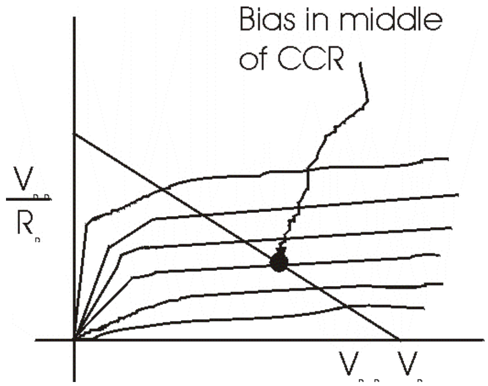
Note : V_{GS} and V_t are the same values as in Q1.

$$\mathrm{V}_{\mathrm{D2}} = 10V - 0.4(10) = 6V$$

ex 5.14

MOSFET Amplifier





$$I_D = K(V_{GS} - V_t)^2$$
$$V_D = V_{DD} - I_D R_D$$

Small Signal:

$$V_{GS} = V_{GS} + V_{gs}$$
$$i_D = K\left[\left(V_{GS} + v_{gs}\right) - V_t\right]^2 = K(V_{GS} - V_t)^2 + 2K(V_{GS} - V_t)V_{gs} + \mathrm{K}\,V_{gs}^{\ 2}$$

In the previous equation:

$$K(V_{GS} - V_t)^2 = I_D$$
$$2K(V_{GS} - V_t)V_{gs} = i_d \quad \text{and}$$
$$\mathrm{K}\ \mathrm{V}_{gs}^{\ 2} \text{ is small for } \mathrm{V}_{gs} << 2(V_{GS} - V_t)$$

$$gm \equiv \frac{i_d}{V_{gs}} \ \ 2K(V_{GS} - V_t) \ \text{ where } 2K = u_n C_{ox} \frac{w}{l}$$

Increase g_m with $\frac{w}{l}$, excess V_{GS} reduces signal swing.

note: $(V_{GS} - V_t) = \sqrt{\dfrac{I_D}{K}}$

$$g_m = \sqrt{2k'n}\sqrt{\frac{w}{l}}\sqrt{I_D}$$

$$k'n = u_n C_{ox}$$

$\sqrt{\frac{w}{l}}$ is independent of junct. area in BJT.

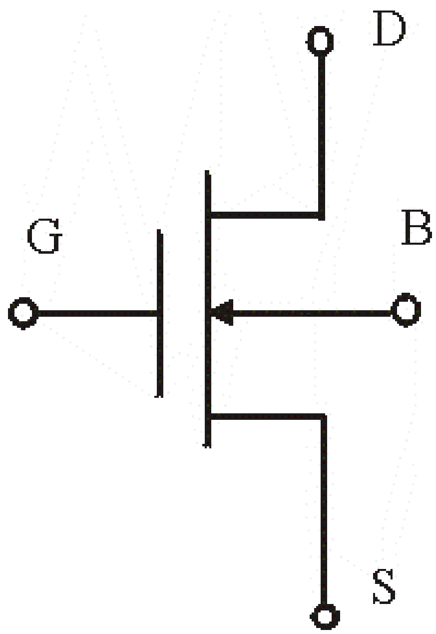
$I_D \,\alpha\, \mathrm{I_C}$ in BJT.

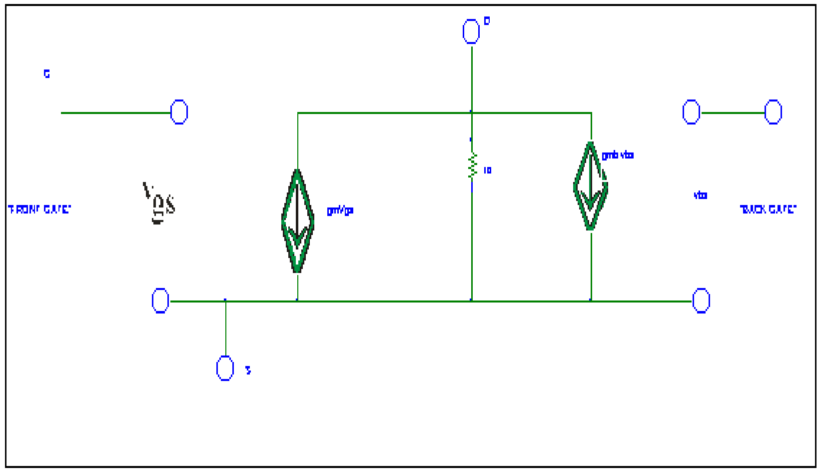
For $k'n = 20\,\frac{uA}{V^2}$ at $I_D = 1mA$

$g_m = 0.2\,\frac{mA}{V}$ for $\frac{w}{l} = 100$

g_m of BJT at $1mA = 40\,\frac{mA}{V}$

Small Signal Model of Body Effect





$$g_m \equiv \frac{\partial i_D}{\partial V_{GS}} \text{ evaluated at: } \mathrm{V_{DS}} = \text{constant}$$

$$\mathrm{V_{BS}} = \text{constant (0)}$$

$$\mathrm{V_{GS}} = V_{GS}$$

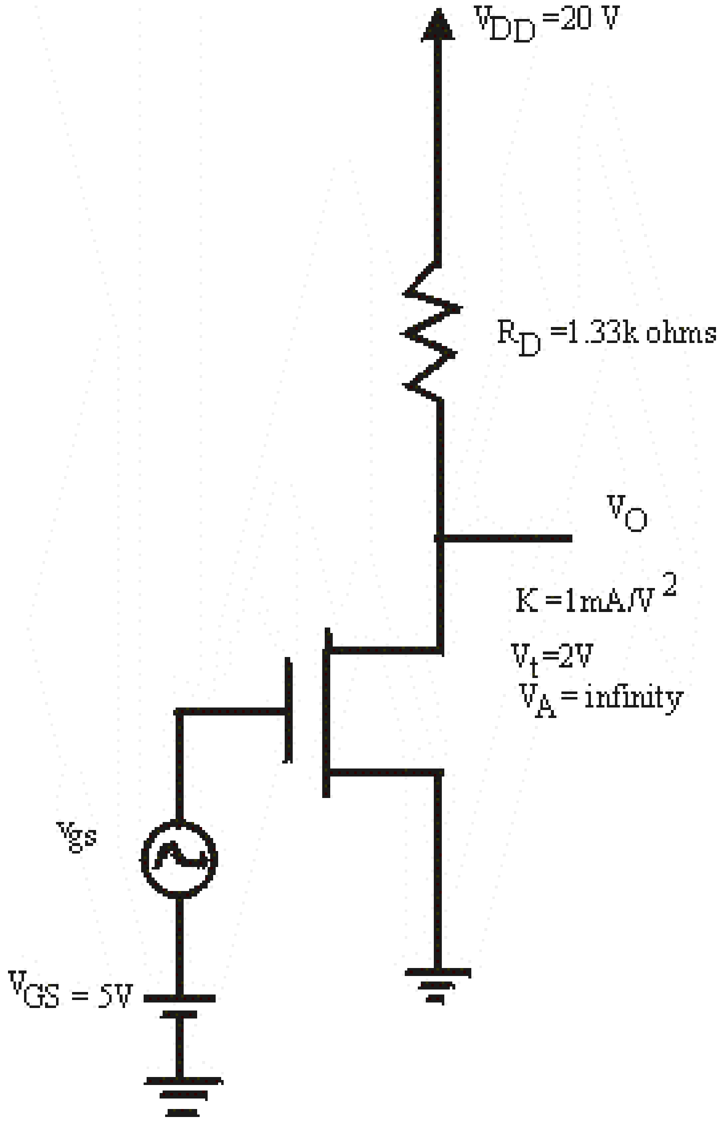
$$g_{mb} \equiv \frac{\partial i_D}{\partial V_{BS}} \text{ evaluated at: } V_{DS} = \text{constant}$$

$$V_{GS} = \text{constant}$$

$$V_{BS} = V_{BS}$$

$$g_{mb} = \chi\, g_m \quad \text{where } \chi \equiv \frac{\partial \mathrm{V_t}}{\partial \mathrm{V_{SB}}} \text{ typically } 0.1 \rightarrow 0.3$$

Can be ignored when the substrate is connected to the source.



Harmonic Distortion:

$$I_D = 1\frac{mA}{V^2}\left[5-2\right]^2 = 9mA$$

. $$V_D = 20V - 9mA \times 1.33k\Omega = 8\text{V}$$

b. $$g_m = 2K\left(V_{GS} - V_t\right) = 2 \bullet 1 \bullet \left(5-2\right) = 6\,\frac{mA}{V}$$

c. Voltage Gain: $\dfrac{v_d}{v_{gs}} = -g_m R_D = -6(1.33) = -8\dfrac{V}{V}$

d. $v_{gs} = .5\sin\ wt\ ;\ v_d = -8(0.5)\sin\ wt = -4\sin\ wt$ assumes a small signal.

$v_{D\,MIN} = 8-4 = 4V\ ;\ \ v_{D\,MAX} = 8+4 = 12V$ both $v_D > V_{GS} - V_t$

e) Total Current:

$i_D = K(V_{GS}-V_t)^2 + 2K(V_{GS}-V_t)v_{gs} + K\,v_{gs}^{\ 2}$; where $K\,v_{gs}^{\ 2}$ is the non - linear distortion term

$= 1\bullet(5-2)^2 + 2\bullet1\bullet(5-2)\bullet0.5\sin\ wt + 1(0.5)^2\sin^2 wt$; recall that $\sin^2 wt = \dfrac{1}{2} - \dfrac{1}{2}\cos 2wt$

$= 9.125 + 3\text{sinwt} - 0.125\cos 2\text{wt}$

From the 9.125 term we can see that the dc shift from 9mA is .125mA

The 0.125cos2wt gives the 2nd harmonic componet which is $\dfrac{0.125}{3} = \dfrac{1}{24} = 4.16\%$

Ex. 5.18 NMOS

$u_n C_{ox} = 20\dfrac{uA}{V^2},\ \dfrac{w}{l} = 64,\ \ V_t = 1V\ \ \lambda = 0.01 = \dfrac{1}{V_A},\ \ g_m, r_O = ?$

. $V_{GS} = 2V;\quad g_m = k'n\dfrac{w}{l}(V_{GS}-V_t) = 2K(V_{GS}-V_t)$

$= 20\times64(2-1) = 1.28\dfrac{mA}{V}$

$I_D = K(V_{GS}-V_t)^2 = \dfrac{1}{2}k'n\dfrac{w}{l}(V_{GS}-V_t)^2 = \dfrac{1}{2}\bullet20\bullet64(2-1)^2 = 0.64mA$

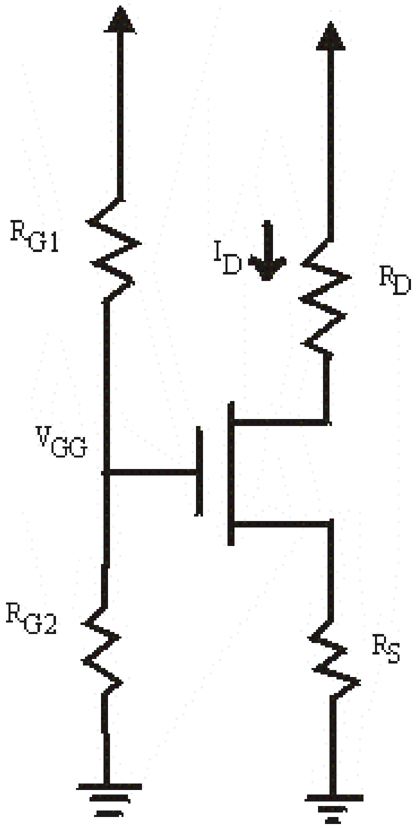
$r_O \cong \dfrac{V_A}{I_D} = \dfrac{1}{\lambda I_D} = \dfrac{1}{0.01\times0.64} = 156k\Omega$

b. $I_D = 1mA$

$$g_m = \sqrt{2k'n\left(\frac{w}{l}\right)I_D} = \sqrt{2 \bullet 20 \bullet 64 \bullet 1000} = 1600\frac{uA}{V} = 1.6\frac{mA}{V}$$

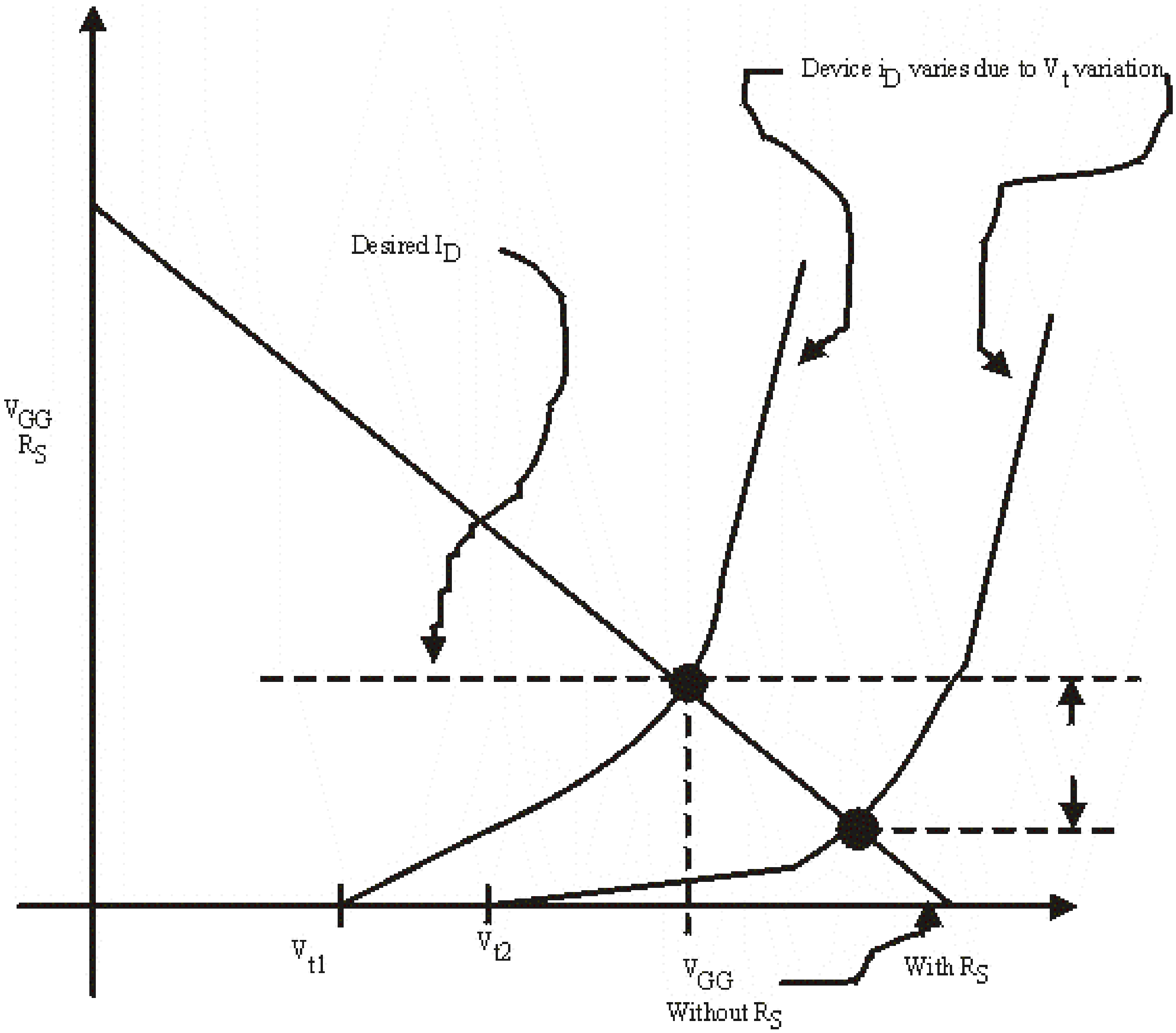
$$r_O = \frac{1}{\lambda I_D} = \frac{1}{0.01 \times 1.0} = 100k\Omega$$

Biasing MOSFETs with Resistors



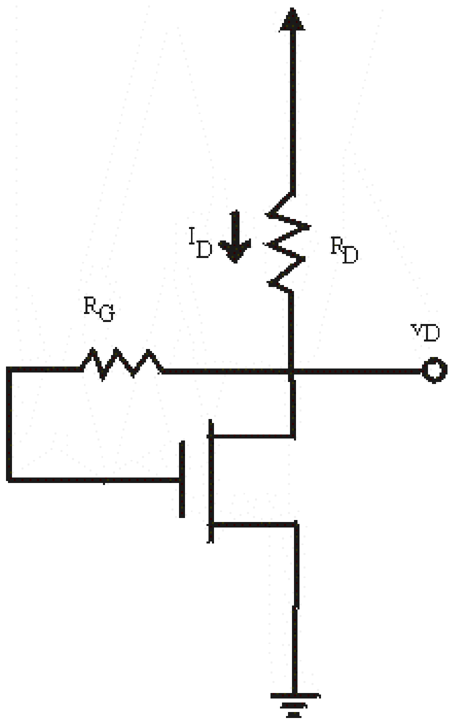
$$V_{GG} = V_{GS} + I_D R_S$$

$$\Rightarrow I_D = \frac{V_{GG}}{R_S} - \frac{1}{R_S} V_{GS}$$



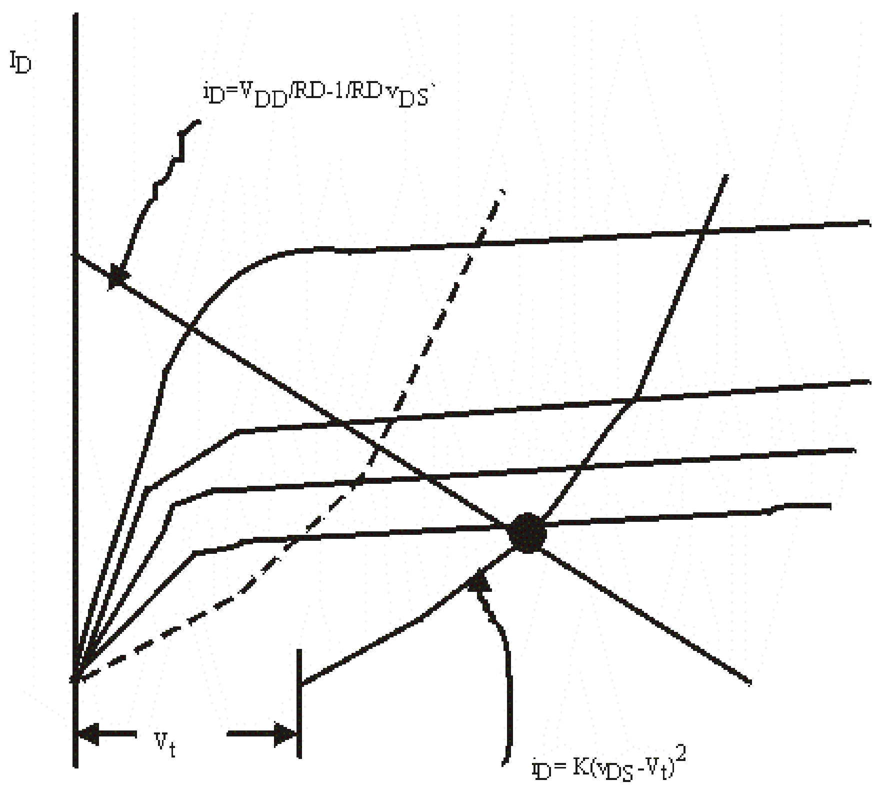
Negative Feedback action of R_S tends to keep I_D stable as i_D increases

$$\Delta v_s = R_S \Delta i_D \Rightarrow \Delta v_{GS} = -\Delta v_s = -R_S \Delta i_D \Rightarrow \text{reduces } i_D$$



Use large R_G to set gate voltage at drain voltage.

$v_{DS} = v_{GS} > v_{GS} - V_T$ at dc,
so always in CCR.
(unless signal swing forces $v_{ds} < V_T$)

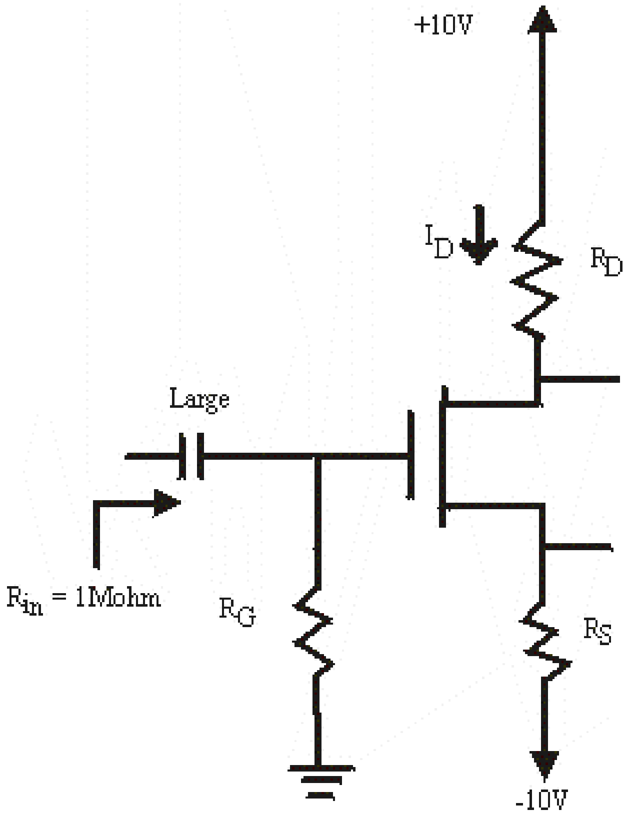


Negative feedback action of R_G tends to keep I_D stable. As i_D increases, v_D decreases by $R_D \Delta i_D$.

$\Rightarrow v_G$ decreases by $R_D \Delta i_D$ also $\Rightarrow$ reduces i_D

Ex. 5.22

$$K = 0.25\frac{mA}{V^2} V_t = 2V,\ V_{DD} = +10V,\ V_{SS} = -10V,\ I_D = 1mA,\ V_{Dswing} = \pm 2V,\ R_{in} = 1M\Omega,\ \lambda = 0$$



$$R_G = 1M\Omega$$

$$I_D = 1mA = K(V_{GS} - V_t)^2 = 0.25(V_{GS} - 2)^2 \Rightarrow V_{GS} = 4V$$

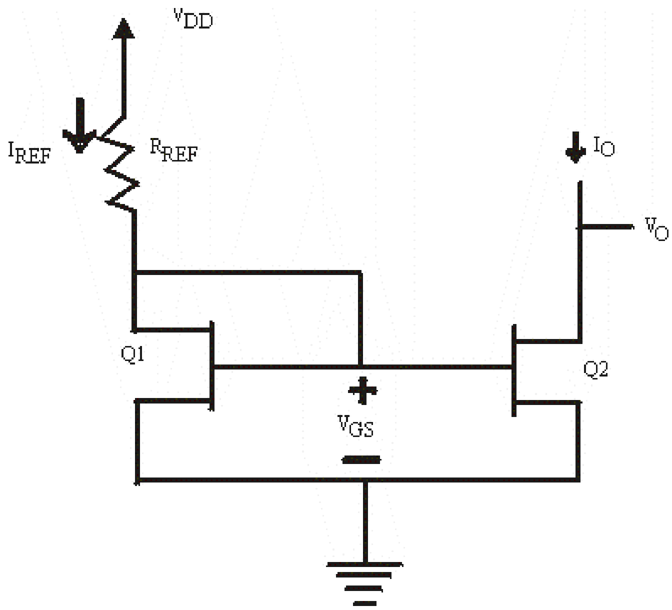
$$V_G = 0, \Rightarrow V_S = -4V$$

$$R_S = \frac{-4V - (-10)}{1mA} = 6k\Omega$$

Signal Swing $V_{D\min} = v_G - V_t \cong 0 - 2 = -2V$ neglecting signal og v_G(assume << 2V)

so, set $V_D = 0V \Rightarrow R_D = \dfrac{10 - 0}{1mA} = 10k\Omega$

MOS Current Source



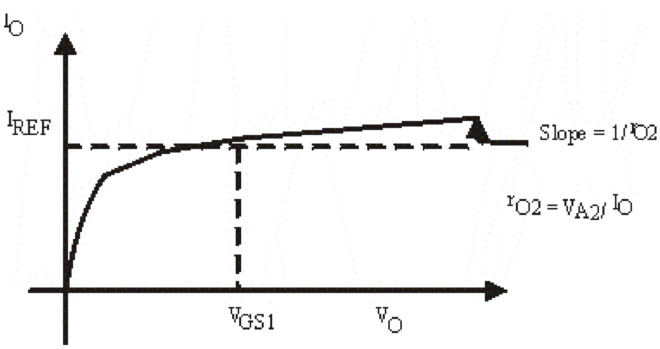
$$I_{D1} = K(V_{GS} - V_t)^2 \qquad \text{neglect } r_O$$

$$I_{D1} = I_{REF} = \frac{V_{DD} - V_{GS}}{R_{REF}}$$

Solve for V_{GS} and R_{REF} given a desired I_{REF}

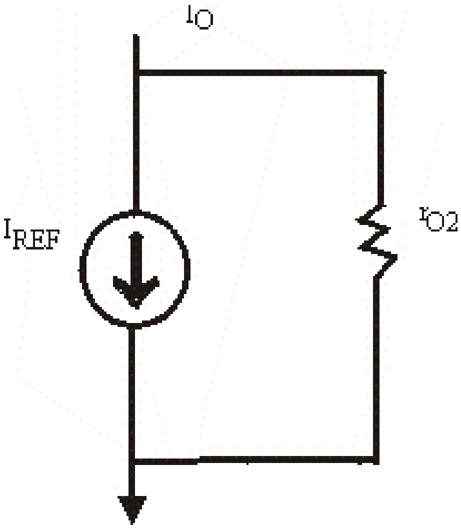
$$I_O = \frac{\left(\frac{w}{l}\right)_2}{\left(\frac{w}{l}\right)_1} I_{REF}$$ Can adjust $\frac{w}{l}$ for desired current level

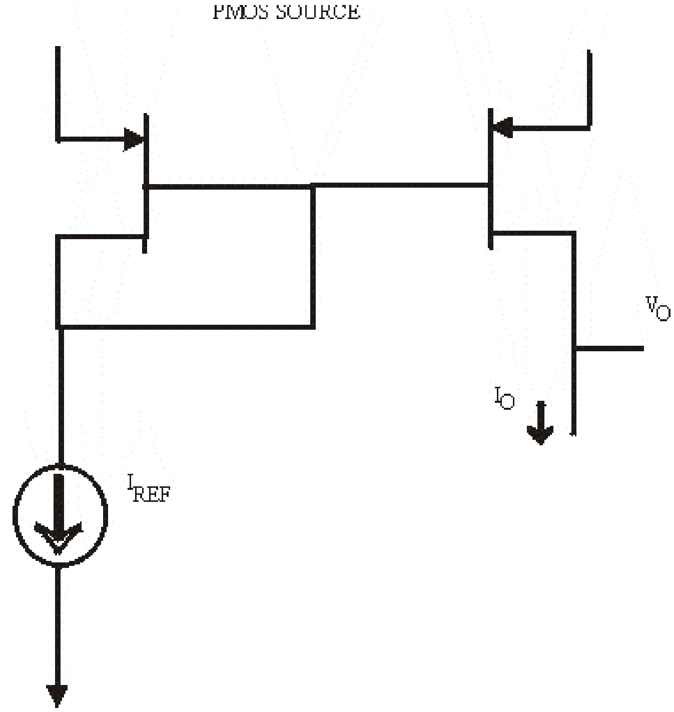
No β effect as in BJT source, but r_O of Q_2 must be considered



$$I_O = I_{REF}\left(1 + \frac{V_O - V_{GS1}}{V_{A2}}\right)$$

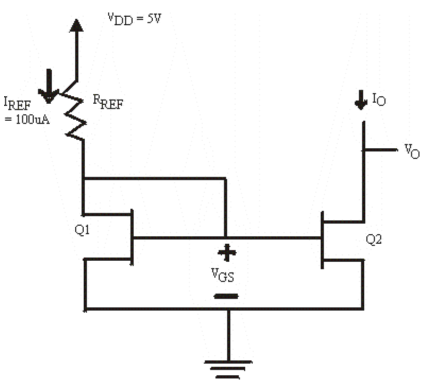
For $\left(\frac{w}{l}\right)_1 = \left(\frac{w}{l}\right)_2$ Matched Transistor s





Ex 5.24 and eq. 5.9

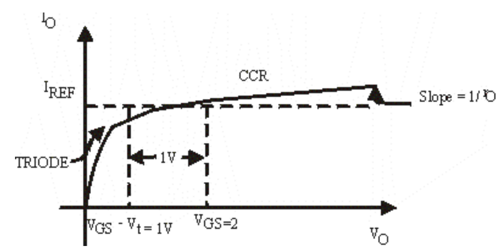
$$k'n = 20\frac{uA}{V^2}\ \ L_{1,2} = 10\,\mu m\ \ W_{1,2} = 100\,\mu m\ \ \mathrm{V_t} = 1V,\ V_A = 10L\,\frac{V}{\mu m}$$



$$I_{REF} = 100\mu A = \frac{1}{2} \bullet 20 \bullet \frac{100}{10}(V_{GS1} - 1)^2$$

$$\Rightarrow V_{GS1} = 2V$$

$$R = \frac{5-2}{100\mu A} = 30k\Omega$$



For V_{OMIN} keep V_{DS2} in CCR $> V_{GS} - V_t$

$V_{OMIN} = 2 - 1 = 1\text{V}$ - below 1V current source in triode and curent drops rapidly.

$$\text{V}_{\text{A}} = 10L = 10\frac{V}{\mu m} \bullet 10\mu m = 100V$$

$$r_O = \frac{V_A}{I_D} = 1M\Omega$$

$I_O = 100\mu A$ at $\text{V}_0 = V_{GS} = 2V$

If $\text{V}_0 \rightarrow V_O + 3 = 5V$ $\quad \Delta\text{I}_0 = \frac{\Delta V_O}{r_O} = \frac{3V}{1M\Omega} = +3\mu A$ (3% greater)

If we want I_O =200uA by changing W_2 , then:

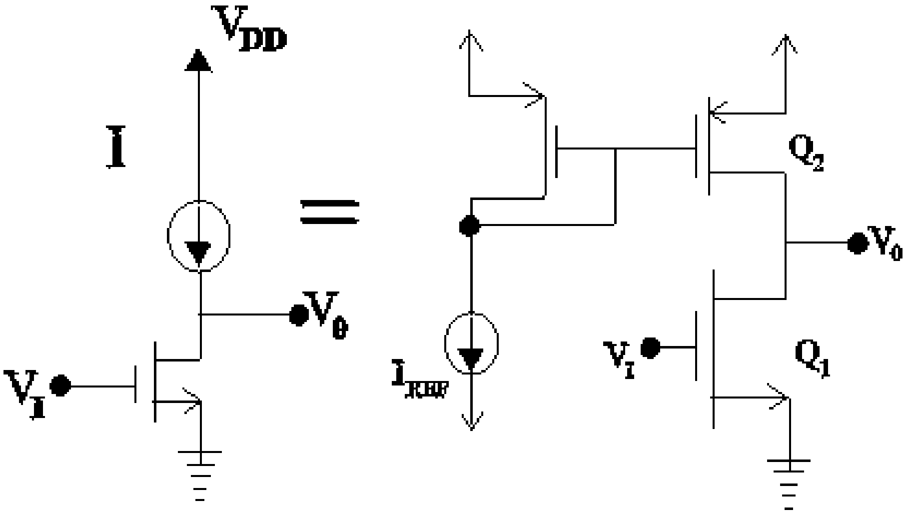
Need $\text{W}_2 = 2 \times 100\mu m = 200\,\mu m$

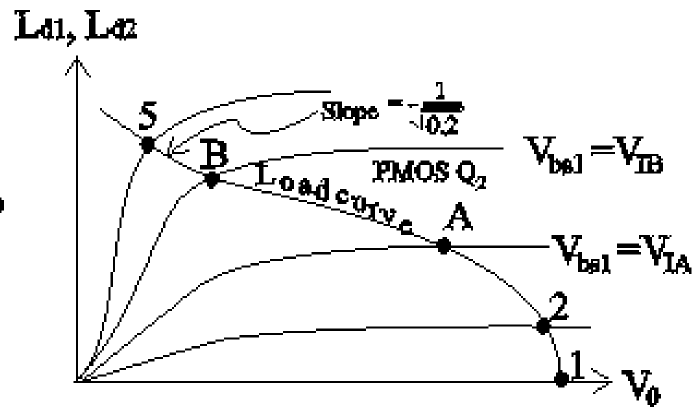
$$r_O = \frac{100V}{200\,\mu A} = 0.5M\Omega$$

At $V_O = 5V$ $\Delta\text{I}_0 = \frac{\Delta V_O}{r_O} = \frac{3V}{0.5M\Omega} = 6\mu A$

I_O at $V_O = 2V = 200\,\mu A$, so at $\text{V}_0 = 5V$, $I_O = 206\mu A$ (also 3% greater)

Active load CMOS Common Source Amplifier



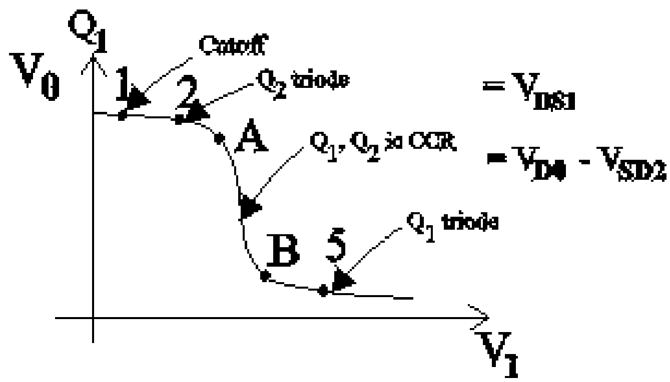


$$gm1=\sqrt{2k_n^1\left(\frac{W}{L}\right)I_{REF}}$$

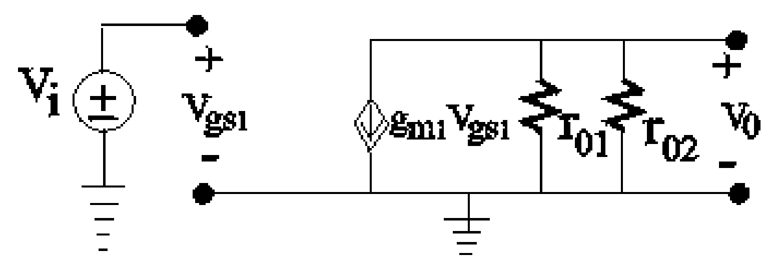
$$r01=\frac{|V_{A1}|}{I_{Ref}}$$

$$r02=\frac{|V_{A2}|}{I_{Ref}}$$

For Q_1,Q_2 in CCR



Small signal model



$$A_{v0}\equiv\frac{V_0}{V_i}=-g_{m1}(r_{01}||r_{02})$$

for $K_1=\frac{1}{2}k_n^1\left(\frac{W}{L}\right)_1$ and $|V_{A1}|\sim|V_{A2}|=V_A$ and no load

$R_{in}=\infty$

$R_{out}=r_{01}\,||\,r_{02}$

$$A_{v0}=-\sqrt{k_1}\frac{V_A}{\sqrt{I_{REF}}}$$

ex 5.26 CMOS common source amp $W/L_{np}=\frac{100\mu\,m}{1.6\mu\,m},\ k_n^1=90\frac{\mu\,A}{r^2},\ k_p^1=30\mu\,A/V^2$

$I_{REF}=100\mu\,A$, $V_{An}=8L\ V/\mu\,m$ $|V_{AP}|=12LV/\mu\,m$

$$g_{m1} = \sqrt{2k_n^1\left(\frac{W}{L}\right)I_{REF}} = \sqrt{2 \cdot 90 \cdot \frac{100}{1.6} \cdot 100} = \underline{\underline{1.06\,\tfrac{mA}{V}}}\ \underline{\text{fairly low}}$$

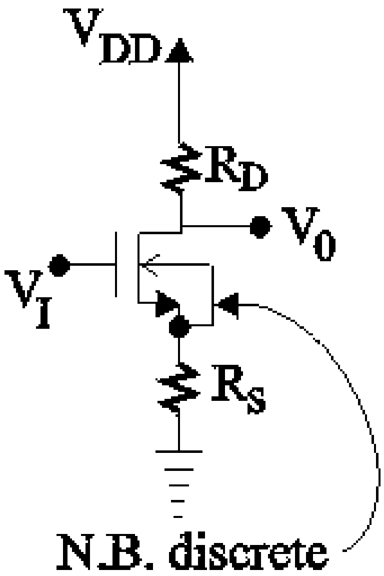
$$\left.\begin{aligned} r_{01} &= \frac{V_{A1}}{I_{REF}} = \frac{8 \cdot 1.6}{0.1mA} = \underline{\underline{127k\Omega}} \\ r_{02} &= \frac{|V_{A2}|}{I_{REF}} = \frac{12 \cdot 1.6}{0.1} = \underline{\underline{192k\Omega}} \end{aligned}\right\} \underline{\textbf{High!}}$$

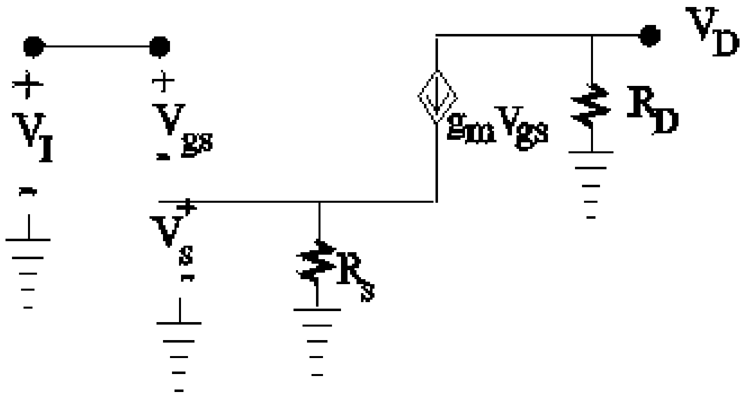
$A_V = -g_{m1}(r_{01} || r_{02}) = -1.06\ (128 || 192) = \underline{-81.4V/V}$

So get good gain with mall g_m due to high r_0 [Active loads can also be used with BJT's, but may not give same voltage gain effect - Why?]

Resistive Load Common Source Amplifier with feedback Resistor

assume $r_0 >> R_D$



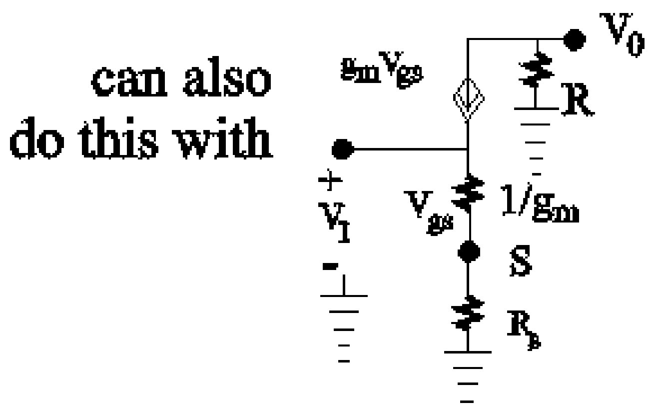


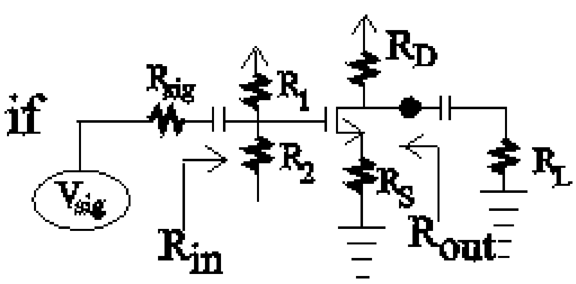
$V_S = g_m v_{gs} R_s$

$V_I = V_{gs} + V_s = (1+ g_m R_S)V_{gs}$

$V_0 = -g_m V_{gs} R_D$

$$A_{vo} \equiv \frac{V_0}{V_I} = \frac{-g_m R_D}{1+g_m R_S}$$

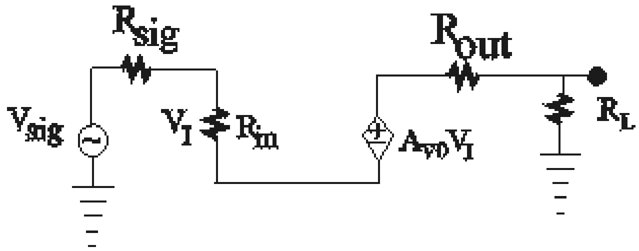




$R_{in} = R_1 \| R_2$ $R_{out} = R_D$

Thevenin equivalent

Voltage amplifier

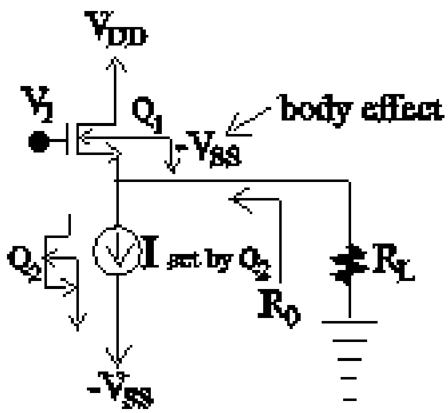


$$A_v = A_{v0} \cdot \frac{R_{in}}{R_{in} + R_{sig}} \cdot \frac{R_L}{R_L + R_{out}}$$

from

$$A_v = \frac{V_{0L}}{V_{sig}} = \frac{V_I}{V_{sig}} \frac{V_0}{V_I} \frac{V_{0L}}{V_0}$$

Source Follower (Common Drain)



Voltage gain

$$Av = \frac{g_{m1}}{g_{m1} + g_{mb1} + \frac{1}{\sqrt{01}} + \frac{1}{\sqrt{02}} + \frac{1}{R_L}} \le 1$$

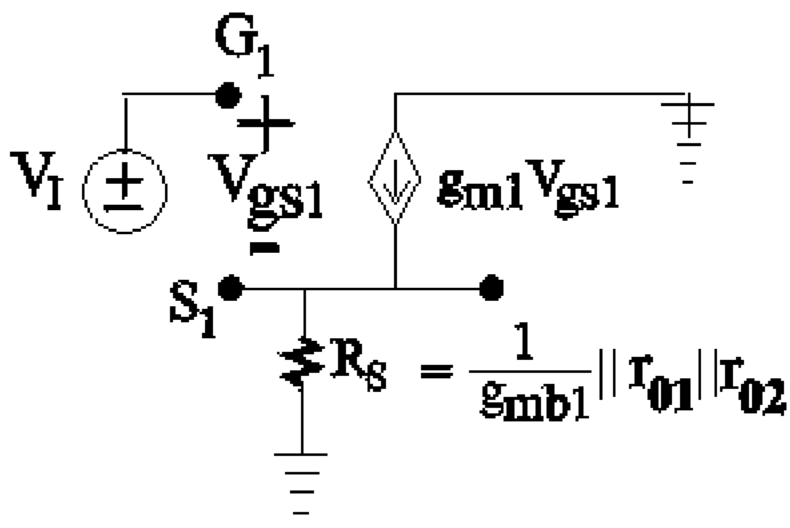
body effect $g_{mb1} = x g_{m1}$ reduces gain by 10% to 30%

$$R_0 = \left(\frac{1}{g_{m1}}\right) \Big\| \left(\frac{1}{g_{mb1}}\right) \Big\| r_{01} || r_{02} \sim \frac{1}{g_{m1}(1+x)} \quad \text{for } r_{01,02} >> \frac{1}{g_{mv}}$$

$R_{in} = \infty$

If p-well: can avoid body effect by trying well to source of Q_1 or descrete

note: $Av|_{R_L} = Av|_{R_L = \infty} \dfrac{R_L}{R_0 + R_L}$



H.W. 5.61 $\mu_n \rightarrow k_n^1$ so it reads $k_n^1 \dfrac{W}{L} = 2mA / V^2$; D5.70

D 5.72, 5.80

Read 425-441

$$g_{m1} = \sqrt{2k_n^1 \left(\frac{W}{L}\right)_1 I_{REF}} = \sqrt{2 \cdot 90 \cdot \frac{100}{1.6} \times 100} = \underline{\underline{1.06 mA / V}}$$

$$g_{mb1} = X g_{m1} = 0.15 \times 1.06 = \underline{\underline{0.16 mA / V}}$$

$$r_{01} = \frac{V_{A1}}{I_{REF}} = \frac{8 \times 16}{01} = \underline{\underline{128k\Omega}}$$

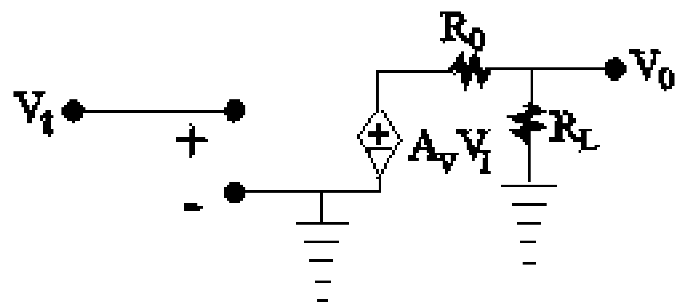
$$r_{02} = \frac{V_{A2}}{I_{REF}} = \underline{\underline{128k\Omega}}$$

Note: $\frac{1}{r_{01}} = \frac{1}{128k} \sim .008mA/V$ is small compared to g_{m1}

$$A_v \cong \frac{g_{m1}}{g_{m1} + g_{mb1}} = \frac{1}{1+x} = \frac{1}{1.15} = 0.87V/V \quad \text{neglect } r_{01}, r_{02}$$

$$R_0 = \frac{1}{g_{m1}} \| \frac{1}{g_{mb1}} \| r_{01} \| r_{02} = \frac{1}{1.06} \| \frac{1}{0.16} \| 128 \| 128 \quad k\Omega = 809\Omega$$

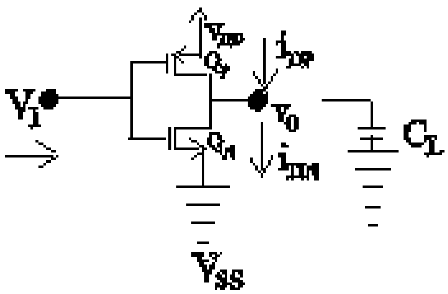
If connect to a 10kΩ resistance

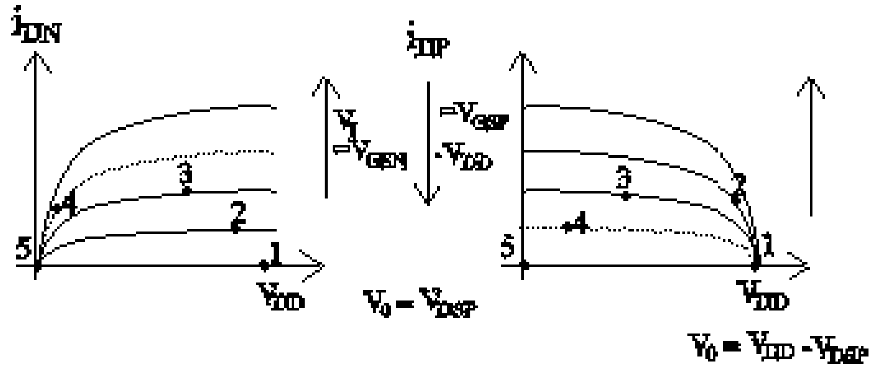


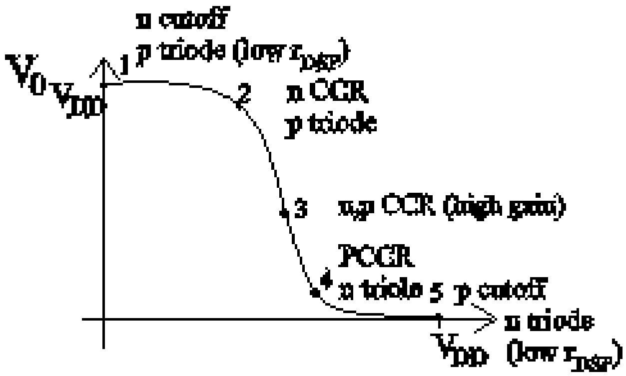
$$A_v = A_v|_{R_L=\infty} \frac{R_L}{R_L + R_0} = 0$$

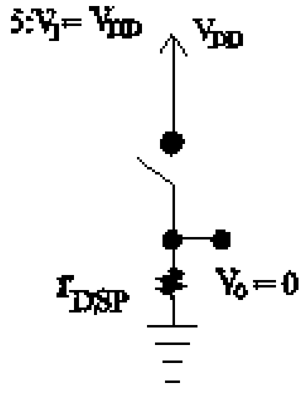
$$= 0.87 \times \frac{10}{10 + 0.809} = \underline{\underline{0.8\ V/V}}$$

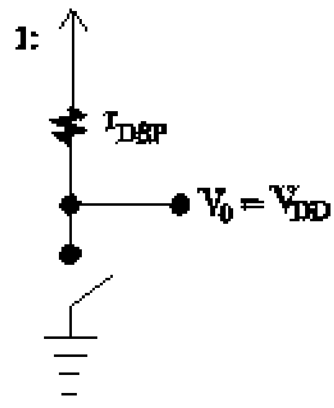
CMOS Inverter - Static











5: triode $i_{DN} = k_n^1 \frac{W}{L}\left[(V_{0S} - V_{tn})V_{DS} - \frac{1}{2}V_{DS}^2\right]$

near $V_{0sp} = 0$ $\qquad i_{DN} \sim k_n^1 \left(\frac{W}{L}\right)_n (V_{DD} - V_{tn}) V_{0S}$

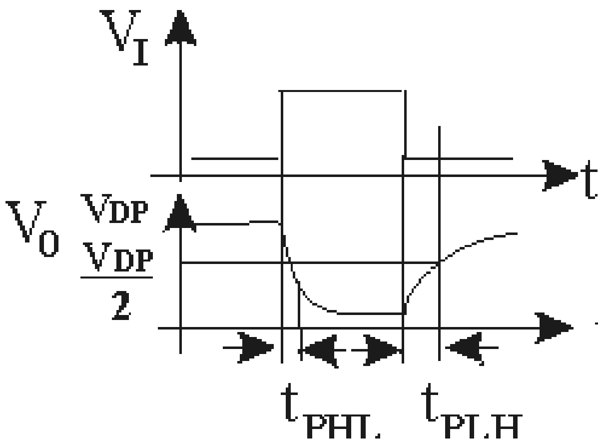
$$V_{GSN} = V_{DD} \qquad r_{DSN} = \frac{V_{DS}}{i_D} = \frac{1}{k_n^1 \left(\frac{W}{L}\right)_n (V_{DD} - V_{tn})}$$

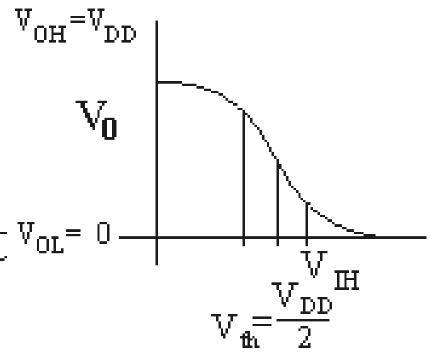
1: near $V_{DSP} = 0$, $V_{GSP} = -V_{DD}$

$$r_{DSP} = \frac{1}{k_p^1 \left(\frac{W}{L}\right)_p \underbrace{(V_{DD} - |V_{tp}|)}_{-(-V_{DD}+V_{tp})}}$$

N, B_1 zero static power, current only follows during switching

CMOS Inverter - Dynamic





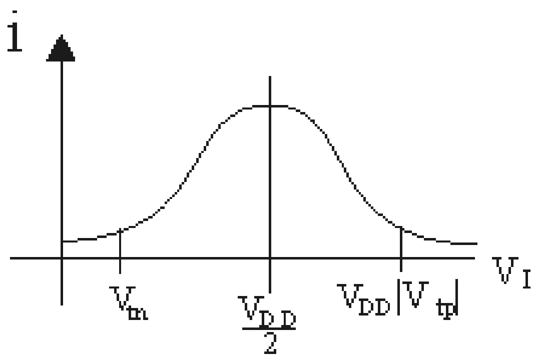
If $V_t \sim 0.2\, V_{DD}$

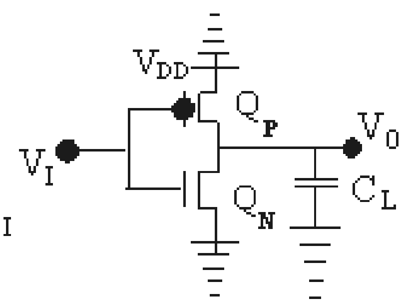
$$T_{PHL} \sim \frac{1.6\, C_L}{k_n^1 \left(\frac{W}{L}\right)_n V_{DD}}$$

$$NM_H = V_{OH} - V_{IH} \sim \frac{1}{8}(3V_{DD} + 2V_T)$$

$$\sim \frac{3.4 V_{DD}}{8} \quad (\sim 2.1\text{V for } \tfrac{5\text{V}}{V_{DD}})$$

$E_C = \frac{1}{2} C_L V_{DD}^2$ stored in capacitor





$P_D = f C_2 V_{DD}^2$

Dissipate $\frac{1}{2} C_L V_{DD}^2$ in Q_P during charging

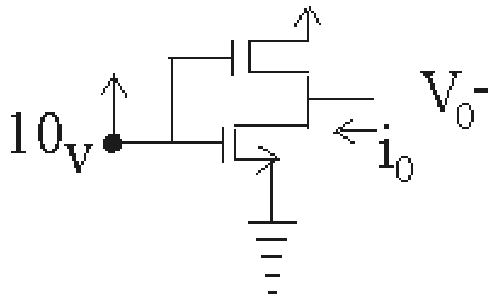
Dissipate $\frac{1}{2} C_L V_{DD}^2$ in Q_N during discharging

(also dissipate some during switching, not in C_r)

Delay Power Product

ex 5.32 $V_{tn} = |V_{tp}| = 2V$, $2\,(W/L)_n = (W/L)_P = 40$, $\mu_n C_{0X} = 20\mu\ A/V^2$, $V_{DD} = 10V$

Max sink current for $V_0 \leq 0.5V$ at $V_I = V_{DD}$



$V_{DS} \leq 0.5 < V_{GS} - V_t = 10 - 8 = 8$ trode

$i_{0max} = \mu_n C_{ox}(w/L)_n[(V_I - V_{tn})V_0 - 1/2 V_0^2]$

$= 20 \cdot 20\,[(10-2)0.5 - 1/2\,(0.5)^2$

$= 400\,[4 - 0.125]\mu A = \underline{1.55mA}$

5.36 if $C_L = 15$ pF

$$t_P = \frac{1.6 C_L}{k_n^1 (\frac{W}{L})_n V_{DD}} = \frac{1.6 \times 15 \times 10^{-12}}{20 \times 10^{-6} \times 20 \times 10} = \underline{\underline{6ns}}$$

5.37 no C_L

Peak current at $V_I = V_{th} = V_{DD} / 2 = 5V$, both n & p in CCP

$$i_{peak} = \frac{1}{2} k_n^1 (\frac{W}{L})_n (V_{th} - V_{tn})^2 \qquad \{also = \frac{1}{2} k_p^1 (\frac{W}{L})_p (|V_{tp}| - V_{th})^2\}$$

$$= \frac{1}{2}\, 20\, 20\, (5-2)^2 \mu\ A = \underline{\underline{1.8\ mA}}$$

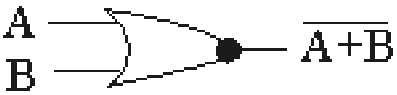
5.38 $C_L = 15$pf f = 2 MHz

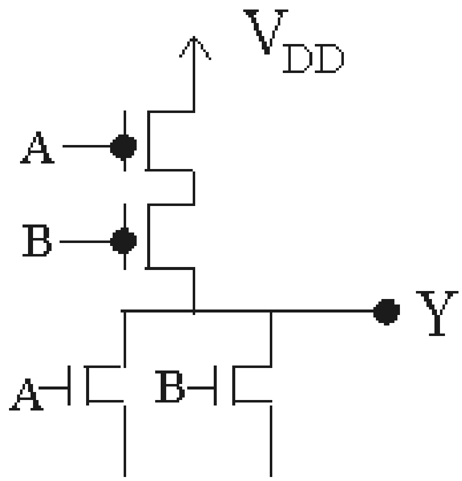
$P_D = fCV_{DD}^2 = 2 \times 10^6 \times 15 \times 10^{-12} * 100 = \underline{3mW}$

$$I_{av} = \frac{P_D}{V_{DD}} = \frac{3 \times 10^{-3}}{10} = \underline{\underline{0.3mA}}$$

CMOS NAND and NOR gates

NOR

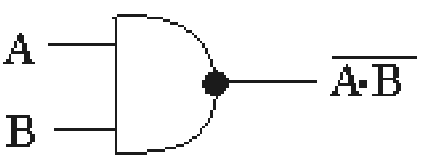


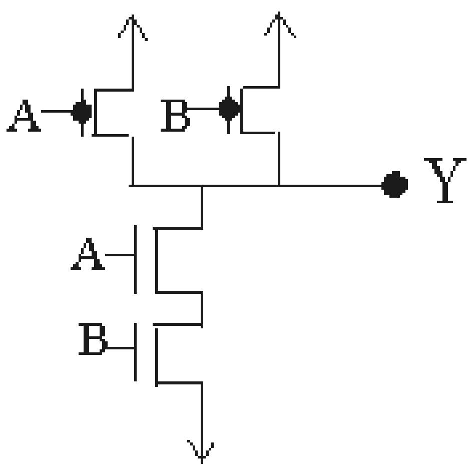


if A,B are both low n's off, P's on $V_0 = V_{DD}$ = logic 1

else at least 1 p off, 1n on $V_0=0$ = logic 0

NAND





if A, B are both high p's off, n's on $V_0 = 0$ = logic 0

else at least 1 p A, 1 n off $V_0=V_{DD}$ = logic 1

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Sizing

arrange

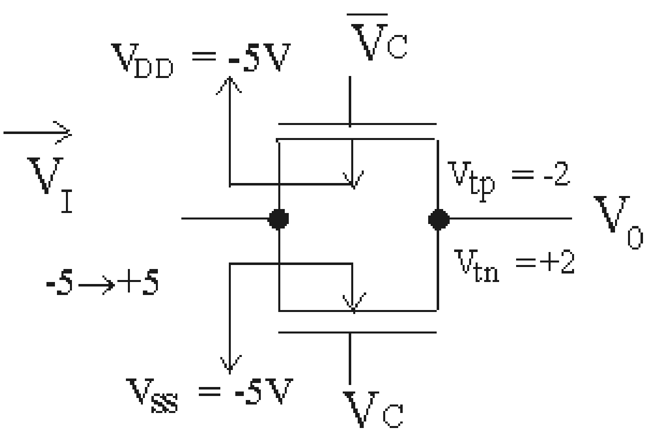
$\left(\frac{W}{L}\right)_N, \left(\frac{W}{L}\right)_P$ for equal pull-up and pull-down

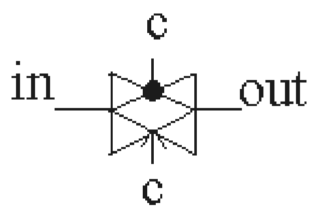
$$\mu_n \sim 2 \cdot \mu_p \Rightarrow \left(\frac{W}{L}\right)_n = \left(\frac{W}{L}\right)_P \text{ for NAND}$$

$$\left(\frac{W}{L}\right)_n = \left(\frac{W}{L}\right)_P \text{ for NAND}$$

A	B	$\overline{A + B}$	$\overline{A \cdot B}$
0	0	1	1
0	1	0	1
1	0	0	1
1	1	0	0

CMOS Transmission Gate





C	
0	Open
1	low resistance

bi-directional analog switch

V_{BP} = - 5V, V_{BN} = -5V to avoid forward biasing junctions

transmits analog signals from
-5V to +5V

set $(W/L)_P = 2(W/L)_n$ for equal r_{DS}

OFF

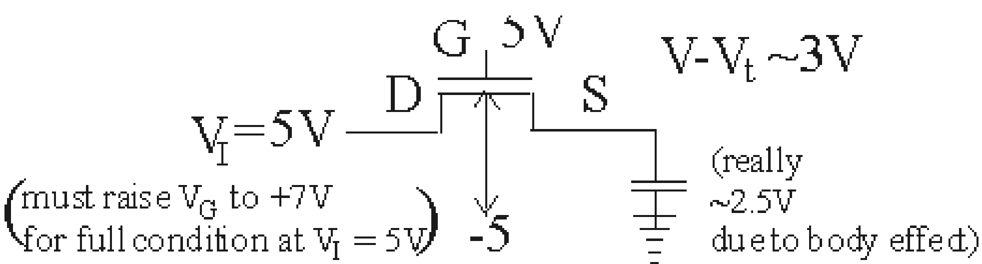
$\overline{V}_c = +5V,\ V_c = -5V$ - both n and p utoff for all signals between -5 and +5

ON

$\overline{V}_c = +5V,\ V_c = -5V$ - both n and p utoff for all signals between -3 and +3
for V_{in} < - 3V only nFET conducts; pFET: $V_{GSp} = -5-(-3)=-2 \Rightarrow V_{GSp} - V_{tp} = 0$
for V_{in} < + 3V only pFET conducts; nFET: $V_{GSN} = 5-3 = 2 \Rightarrow V_{GSN} - V_{tN} = 0$

∴ using only nFET or pFET makes for a limiting design
using both: as r_{DS} one increases, other decreases ⇒

nFET only switch



Vgs = V_t so it just starts conducting

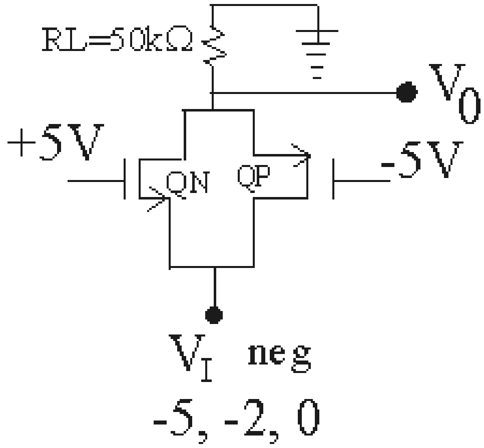
if $V_S > V - V_t$, $V_{GS} < V_t$ and nFET is cut off

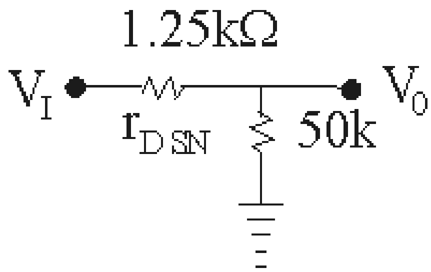
ex 5.40 $|V_t|_{p,n} = 2$ $(k^1 w/l)_{p;n} = 100\mu\ A/r^2$, $R_i = 50k\Omega$ r_{switch}, V_0

a) V_I = -5V, V_0 will approx -5V (a little less due to t_{switch})
QP off since $|V_{Gs}| < |V_t| = 2V$ $r_{DSP} = \infty$
QN in triode region since V_{DS} small < $V_{GS}-V_t$ =10 -2

for V_{DS} small

$$r_{DSN} = \frac{1}{k_n^1 (\frac{W}{L})_n (V_{GS} - V_t)} = \frac{1}{0.1\frac{mA}{r^2}(5-(-5)-2)} = 1.25k\Omega$$





$$V_0 = \frac{50k}{50k + 1.25k}(-5) = \underline{\underline{-4.9V}}$$

b) V_I = -2V V_{SGP} -$|V_t|$ ~ -2-2-(-5) ~ 1V > V_{DSP} since V_0 ~ 2 V (a bit less)

both in triode region

$$r_{DSN} \cong \frac{1}{0.1(5-(-2)-2)} = 2k\Omega \qquad r_{DSP} \cong \frac{1}{k_p^1(\frac{W}{L})_p(V_{SGP}|V_t|_p)} = \frac{1}{0.1(V_0-(-5)-2)}$$

$$r_{switch} \sim \frac{(10)(2)}{10+2} \sim 2k\Omega \qquad \sim \underline{\underline{10k\Omega}}\text{ (a bit less)}$$

$$V_0 = \frac{50k}{51.66k}(-2) = \underline{\underline{-1.9V}}$$

$$r_{DSN} \cong \frac{1}{0.1(5-(-2)-2)} = 2k\Omega \qquad r_{DSP} \cong \frac{1}{k_p^1(\frac{W}{L})_p(V_{SGP}|V_t|_p)} = \frac{1}{0.1(V_0-(-5)-2)}$$

$\leq \sim 2$

$$r_{switch} \sim \frac{(10)(2)}{10+2} \sim 2k\Omega \qquad \sim \underline{\underline{10k\Omega}}\text{(a bit less)}$$

$$V_0 = \frac{50k}{51.66k}(-2) = \underline{\underline{-1.9V}}$$

c) V_I = 0V ⇒ no conduction ⇒ $\underline{V_0 = 0V}$

r_{switch}=(.5)(3.33kΩ) = 1.67kΩ

$$r_{DSN} = \frac{1}{0.1(5-0-2)} = 3.33k\Omega \qquad V_{DSP} = \frac{1}{(0.1)(0-(-5)-2)} = 3.33k\Omega$$