4.1 Number Systems & Boolean Algebra

1. The 100110_2 is numerically equivalent to

1. 26_{16} 2. 36_{10} 3. 46_8 4. 212_4

The correct answer are

(A) 1, 2, and 3 (B) 2, 3, and 4

(C) 1, 2, and 4 (D) 1, 3, and 4

2. If $(211)_x = (152)_8$, then the value of base x is

(A) 6 (B) 5

(C) 7 (D) 9

3. 11001, 1001 and 111001 correspond to the 2's complement representation of the following set of numbers

(A) 25, 9 and 57 respectively

(B) –6, –6 and –6 respectively

(C) –7, –7 and –7 respectively

(D) –25, –9 and –57 respectively

4. A signed integer has been stored in a byte using 2's complement format. We wish to store the same integer in 16-bit word. We should copy the original byte to the less significant byte of the word and fill the more significant byte with

(A) 0

(B) 1

(C) equal to the MSB of the original byte

(D) complement of the MSB of the original byte.

5. A computer has the following negative numbers stored in binary form as shown. The wrongly stored number is

(A) –37 as 1101 1011 (B) –89 as 1010 0111

(C) –48 as 1110 1000 (D) –32 as 1110 0000

6. Consider the signed binary number $A = 01010110$ and $B = 1110\,1100$ where B is the 1's complement and MSB is the sign bit. In list-I operation is given, and in list-II resultant binary number is given.

List–I	List-II
P. $A + B$ Q. $B - A$ R. $A - B$ S. $-A - B$	1. 0 1 0 0 0 0 1 1 2. 0 1 1 0 1 0 0 1 3. 0 1 0 0 0 0 1 0 4. 1 0 0 1 0 1 0 1 5. 1 0 1 1 1 1 0 0 6. 1 0 0 1 0 1 1 0 7. 1 0 1 1 1 1 0 1 8. 0 1 1 0 1 0 1 0

The correct match is

	P	Q	R	S
(A)	3	4	2	5
(B)	3	6	8	7
(C)	1	4	8	7
(D)	1	6	2	5

7. Consider the signed binary number $A = 0100\,0110$ and $B = 11010011$, where B is in 2's complement and MSB is the sign bit. In list-I operation is given and in List-II resultant binary number is given

List–I	List-II
P. $A + B$ Q. $A - B$ R. $B - A$ S. $-A - B$	1. 1 0 0 0 1 1 0 1 2. 1 1 1 0 0 1 1 1 3. 0 1 1 1 0 0 1 1 4. 1 0 0 0 1 1 1 0 5. 0 0 0 1 1 0 1 0 6. 0 0 0 1 1 0 0 1 7. 0 1 0 1 1 0 1 1

The correct match is

	P	Q	R	S
(A)	5	7	4	2
(B)	6	3	1	2
(C)	6	7	1	3
(D)	5	3	4	2

8. The decimal number 11.3 in binary is

(A) $1011.\overline{1101}$ (B) $1011.0\overline{1001}$

(C) $1011.\overline{1001}$ (D) $1011.0\overline{1101}$

9. A 7 bit Hamming code groups consisting of 4 information bits and 3 parity bits is transmitted. The group 1101100 is received in which at most a single error has occurred. The transmitted code is

(A) 1111100 (B) 1100100

(C) 1001100 (D) 1101000

10. X =?

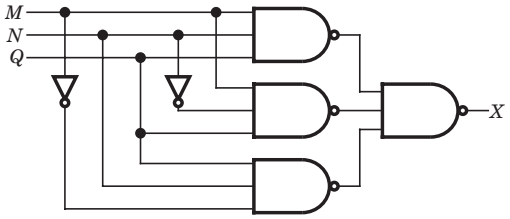


Fig. P4.1.10

(A) MNQ (B) $N(Q + M)$

(C) $M(Q + N)$ (D) $Q(M + N)$

11. Z = ?

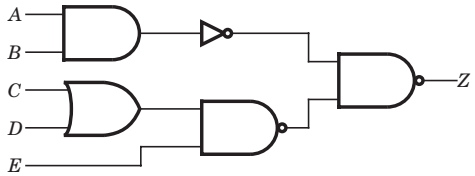


Fig. P4.1.11

(A) $AB + (C + D)E$ (B) $AB(C + D)E$

(C) $AB + CD + E$ (D) $AB + CDE$

12. Z =?

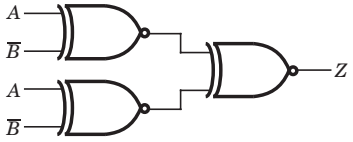


Fig. P4.1.12

(A) $\overline{A}B + A\overline{B}$ (B) $AB + \overline{A}\,\overline{B}$

(C) 0 (D) 1

13. Z =?

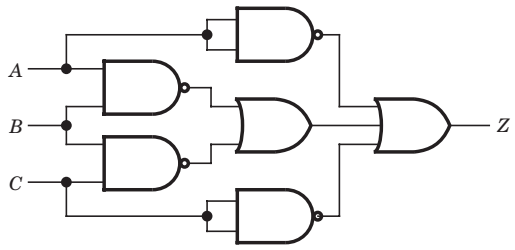


Fig. P4.1.13

(A) $\overline{A} + \overline{B} + \overline{C}$ (B) $\overline{ABC}$

(C) $\overline{AB} + \overline{BC} + \overline{AC}$ (D) Above all

14. The Boolean expression $(X + Y)(X + \overline{Y})(\overline{X} + Y)$ is equivalent to

(A) $\overline{X}Y$ (B) $X\overline{Y}$

(C) XY (D) $\overline{X}\,\overline{Y}$

15. Given that $AB + \overline{A}C + BC = AB + \overline{A}C$, then $(\overline{A} + C)(B + C)(A + B)$ is equivalent to

(A) $(\overline{A} + B)(A + C)$ (B) $(A + B)(\overline{A} + C)$

(C) $(A + \overline{B})(\overline{A} + C)$ (D) $(A + \overline{B})(\overline{A} + \overline{C})$

16. Z =?

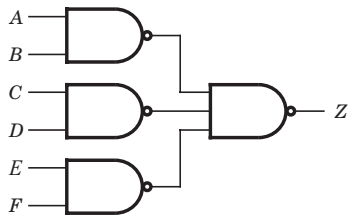


Fig. P4.1.16

(A) $(\overline{A} + \overline{B})(\overline{C} + \overline{D})(E + F)$ (B) $AB + CD + EF$

(C) $(A + B)(C + D)(E + F)$ (D) $\overline{AB} + \overline{CD} + \overline{EF}$

17. X =?

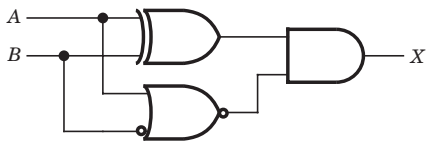


Fig. P4.1.17

(A) $\overline{A}B$ (B) AB

(C) $A\overline{B}$ (D) 0

18. Y =?

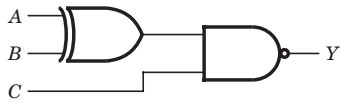


Fig. P4.1.18

(A) $A\overline{B} + \overline{A}B + C$ (B) $\overline{A}\,\overline{B} + AB + C$

(C) $\overline{A}B + A\overline{B} + C$ (D) $A\overline{B} + \overline{A}B + \overline{C}$

19. Z =?

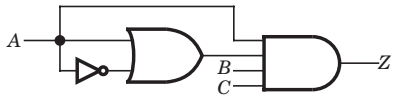


Fig. P4.1.19

(A) $A\overline{B}C$ (B) $\overline{A}BC$

(C) ABC (D) 0

20. Z =?

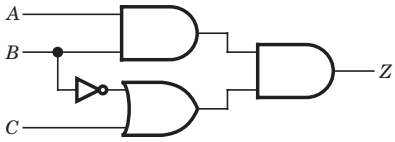


Fig. P4.1.20

(A) ABC (B) $AB(\overline{C} + B)$

(C) $A\overline{B}C$ (D) $A\overline{B}(\overline{C} + B)$

21. Z =?

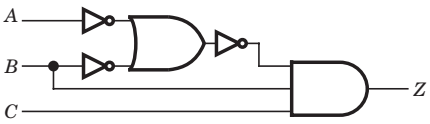


Fig. P4.1.21

(A) ABC (B) $\overline{A}\,\overline{B}C$

(C) 0 (D) $\overline{A}\,BC$

22. The minimum number of NOR gates required to implement $A(A + \overline{B})(A + \overline{B} + C)$ is equal to

(A) 0 (B) 3

(C) 4 (D) 7

23. $A + BC$ is equivalent to

(A) $(A + B)(A + C)$ (B) $A + B$

(C) $A + C$ (D) $(A + \overline{B})(A + C)$

24. For the truth table shown in fig. P.4.1.24, Boolean expression for $\overline{X}$ is

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Fig. P.4.1.24

(A) $\overline{A}B + BC + \overline{A}\,\overline{C} + \overline{B}\,\overline{C}$ (B) $\overline{B}C + AB\overline{C}$

(C) $\overline{B}C$ (D) $AB\overline{C}$

25. The truth table of a circuit is shown in fig. P.4.1.23.

A	B	C	Z
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

Fig. P.4.1.25

The Boolean expression for Z is

(A) $(\overline{A + B})(\overline{B + \overline{C}})$ (B) $\overline{(\overline{A + B})(\overline{B + \overline{C}})}$

(C) $(\overline{\overline{A} + B)(\overline{B + C}})$ (D) Above all

26. The Boolean expression $AC + B\overline{C}$ is equivalent to

(A) $\overline{A}C + B\overline{C} + AC$

(B) $\overline{B}C + AC + B\overline{C} + \overline{A}C\overline{B}$

(C) $AC + B\overline{C} + \overline{B}C + ABC$

(D) $ABC + \overline{A}B\overline{C} + AB\overline{C} + A\overline{B}C$

27. Expression $A + \overline{A}B + \overline{A}\overline{B}C + \overline{A}\overline{B}\overline{C}D + \overline{A}\overline{B}\overline{C}\overline{D}E$ would be simplified to

(A) $A + \overline{A}B + CD + E$ (B) $A + B + CDE$

(C) $A + BC + CD + DE$ (D) $A + B + C + D + E$

28. The simplified form of a logic function $Y = A(B + C(\overline{AB + AC}))$ is

(A) $\overline{A}\,\overline{B}$ (B) AB

(C) $\overline{A}B$ (D) $A\overline{B}$

29. The reduced form of the Boolean expression of $Y = (\overline{A\overline{B}}) \cdot (\overline{\overline{A}B})$ is

(A) $A + B$ (B) $\overline{A} + \overline{B}$

(C) $A\overline{B} + \overline{A}B$ (D) $\overline{A}\,\overline{B} + AB$

30. If $X\overline{Y} + \overline{X}Y = Z$ then $X\overline{Z} + \overline{X}Z$ is equal to

(A) $\overline{Y}$ (B) Y

(C) 0 (D) 1

31. If $XY = 0$ then $X \oplus Y$ is equal to

(A) $X + Y$ (B) $\overline{X} + \overline{Y}$

(C) XY (D) $\overline{X}\,\overline{Y}$

32. From a four-input OR gate the number of input condition, that will produce HIGH output are

(A) 1 (B) 3

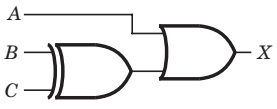
(C) 15 (D) 0

33. A logic circuit control the passage of a signal according to the following requirements :

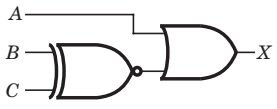
1. Output X will equal A when control input B and C are the same.

2. X will remain HIGH when B and C are different.

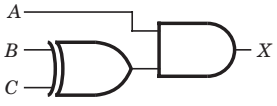
The logic circuit would be



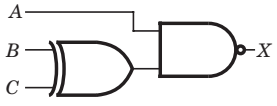
(A)



(B)

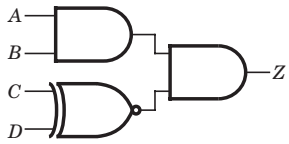


(C)

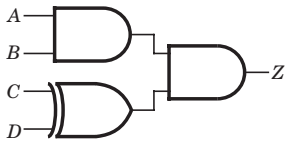


(D)

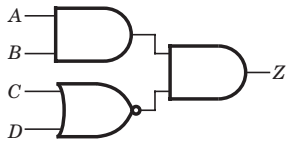
34. The output of logic circuit is HIGH whenever A and B are both HIGH as long as C and D are either both LOW or both HIGH. The logic circuit is



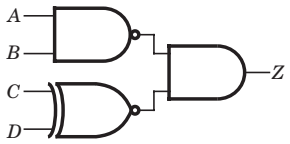
(A)



(B)



(C)



(D)

35. In fig. P.4.1.35 the input condition, needed to produce $X = 1$, is

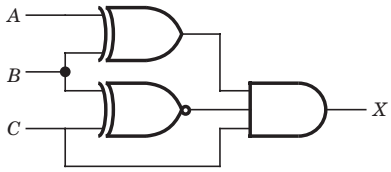


Fig. P4.1.34

(A) $A = 1,\ B = 1,\ C = 0$ (B) $A = 1,\ B = 1,\ C = 1$

(C) $A = 0,\ B = 1,\ C = 1$ (D) $A = 1,\ B = 0,\ C = 0$

36. Consider the statements below:

1. If the output waveform from an OR gate is the same as the waveform at one of its inputs, the other input is being held permanently LOW.

2. If the output waveform from an OR gate is always HIGH, one of its input is being held permanently HIGH.

The statement, which is always true, is

(A) Both 1 and 2 (B) Only 1

(C) Only 2 (D) None of the above

37. To implement $y = ABCD$ using only two-input NAND gates, minimum number of requirement of gate is

(A) 3 (B) 4

(C) 5 (D) 6

38. If the X and Y logic inputs are available and their complements $\overline{X}$ and $\overline{Y}$ are not available, the minimum number of two-input NAND required to implement $X \oplus Y$ is

(A) 4 (B) 5

(C) 6 (D) 7

Statement for Q.39–40:

A Boolean function $Z = A\overline{B}C$ is to be implement using NAND and NOR gate. Each gate has unit cost. Only A, B and C are available.

39. If both gate are available then minimum cost is

(A) 2 units (B) 3 units

(C) 4 units (D) 6 units

40. If NAND gate are available then minimum cost is

(A) 2 units (B) 3 units

(C) 5 units (D) 6 units

41. In fig. P4.1.41 the LED emits light when

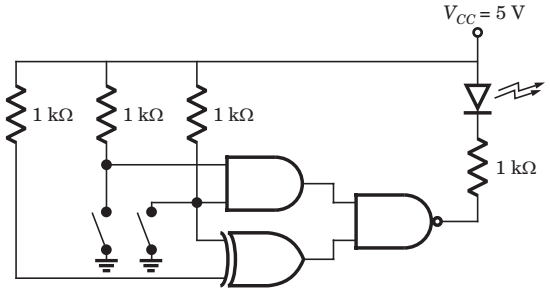


Fig. P4.1.41

(A) both switch are closed

(B) both switch are open

(C) only one switch is closed

(D) LED does not emit light irrespective of the switch positions

42. If the input to the digital circuit shown in fig. P.4.1.42 consisting of a cascade of 20 XOR gates is X, then the output Y is equal to

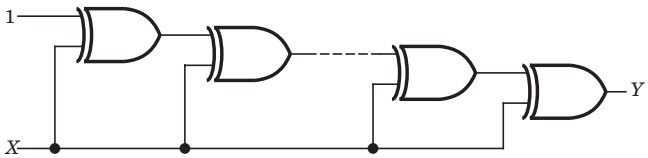


Fig. P4.1.42

(A) X (B) $\overline{X}$

(C) 0 (D) 1

43. A Boolean function of two variables x and y is defined as follows :

$$f(0, 0) = f(0, 1) = f(1, 1) = 1;\ f(1, 0) = 0$$

Assuming complements of x and y are not available, a minimum cost solution for realizing f using 2-input NOR gates and 2-input OR gates (each having unit cost) would have a total cost of

(A) 1 units (B) 2 units

(C) 3 units (D) 4 units

44. The gates G_1 and G_2 in Fig. P.4.2.44 have propagation delays of 10 ns and 20 ns respectively.

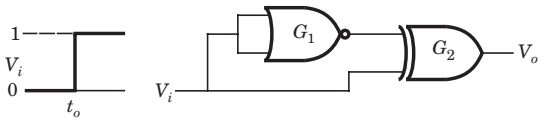
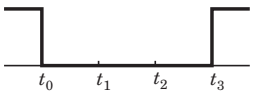


Fig. P4.1.44

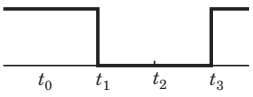
If the input V_i makes an abrupt change from logic 0 to 1 at $t = t_0$ then the output waveform V_o is

$[t_1 = t_0 + 10 \text{ ns},\ t_2 = t_1 + 10 \text{ ns},\ t_3 = t_2 + 10 \text{ ns}]$

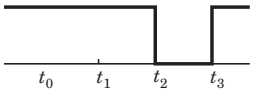
(A)



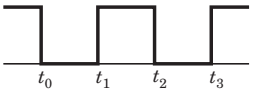
(B)



(C)



(D)



45. In the network of fig. P4.1.45 f can be written as

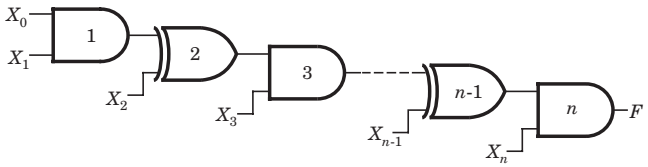


Fig. P4.1.45

(A) $X_0X_1X_3X_5 + X_2X_4X_5 \ldots X_{n-1} + \ldots X_{n-1}X_n$

(B) $X_0X_1X_3X_5 + X_2X_3X_4 \ldots X_n + \ldots X_{n-1}X_n$

(C) $X_0X_1X_3X_5 \ldots X_n + X_2X_3X_5 \ldots X_n + \ldots + X_{n-1}X_n$

(D) $X_0X_1X_3X_5 \ldots X_{n-1} + X_2X_3X_5 \ldots X_n + .. + X_{n-1}X_{n-2} + X_n$

****

Solutions

1. (C) $100110_2 = 2^5 + 2^2 + 2^1 = 38_{10}$

$26_{16} = 2 \times 16 + 6 = 38_{10}$

$46_8 = 4 \times 8 + 6 = 38_{10}$

$212_4 = 2 \times 4^2 + 4^1 = 38_{10}$

So 36_{10} is not equivalent.

2. (C) $2x^2 + x + 1 = 64 + 5 \times 8 + 2 \quad \Rightarrow \quad x = 7$

3. (C) All are 2's complement of 7

$$\begin{array}{lll} 11001 \Rightarrow & 00110 & \\ & +\ \ 1 & \\ & \hline 00111 & = 7_{10} \end{array}$$

$$\begin{array}{lll} 1001 \Rightarrow & 0110 & \\ & +\ \ 1 & \\ & \hline 0111 & = 7_{10} \end{array}$$

$$\begin{array}{lll} 111001 \Rightarrow & 000110 & \\ & +\ \ 1 & \\ & \hline 000111 & = 7_{10} \end{array}$$

4. (C) See a example

42 in a byte 0 0 1 0 1 0 1 0

42in a word 0 0 0 0 0 0 0 0 0 0 1 0 1 0 1 0

–42 in a byte 1 1 0 1 0 1 1 0

–42 in a word 1 1 1 1 1 1 1 1 1 1 0 1 0 1 1 0

Therefore (C) is correct.

5. (C) $48_{10} = 00110000_2$

$$\begin{array}{rl} -48_{10} = & 1100\,1111 \\ & +\ \ \ \ \ \ 1 \\ \hline & 1101\,0000 \end{array}$$

6. (D) Here $\overline{A}$, $\overline{B}$ are 1's complement

$$\begin{array}{lll} A + B, & A & 0101\,0110 \\ & B & +\ 1110\,1100 \\ \hline & & 1\ 0100\,0010, \\ & & +\ \ \ \ \ \ \ 1 \\ \hline & & 0100\,0011 \end{array}$$

$$\begin{array}{lll} B - A = B + \overline{A}, & B & 1110\,1100 \\ & \overline{A} & +\ 1010\,1001 \\ \hline & & 1\ 1001\,0101 \\ & & +\ \ \ \ \ \ \ 1 \\ \hline & & 1001\,0110 \end{array}$$

$$\begin{array}{lll} A - B = A + \overline{B}, & A & 0101\,0110 \\ & \overline{B} & +\ 0001\,0011 \\ \hline & & 0111\,0001 \end{array}$$

$$\begin{array}{lll} -A - B = \overline{A} + \overline{B}, & \overline{A} & 1010\,1001 \\ & \overline{B} & +\ 0001\,0011 \\ \hline & & 1011\,1100 \end{array}$$

7. (B) Here $\overline{A}$, $\overline{B}$ are 2's complement

$$\begin{array}{lll} A + B, & A & 0100\,0110 \\ & B & +\ 1101\,0011 \\ \hline & & 1\ 0001\,1001 \end{array}$$

Discard the carry 1

$$\begin{array}{lll} A - B = A + \overline{B}, & A & 0100\,0110 \\ & \overline{B} & +\ 0010\,1101 \\ \hline & & 0111\,0011 \end{array}$$

$$\begin{array}{lll} B - A, & B & 1101\,0011 \\ & \overline{A} & +\ 1011\,1010 \\ \hline & & 1\ 1000\,1101 \end{array}$$

Discard the carry 1

$$\begin{array}{lll} -A - B = \overline{A} + \overline{B}, & \overline{A} & 1011\,1010 \\ & \overline{B} & +\ 0010\,1101 \\ \hline & & 1110\,0111 \end{array}$$

8. (B) $11_{10} = 1011_2$

0.3	$2F_{i-1}$	B_i	F_i
	0.6	0	0.6
	1.2	1	0.2
	0.4	0	0.4
	0.8	0	0.8
	1.6	1	0.6

Repeat from the second line $0.3_{10} = 0.\overline{01001}_2$

9. (C)

	b_4	b_3	b_2	p_3	b_1	p_2	p_1
Received	1	1	0	1	1	0	0

$C_1^* = b_4 \oplus b_2 \oplus b_1 \oplus p_1 = 0$

$C_2^* = b_4 \oplus b_3 \oplus b_1 \oplus p_2 = 1$

$C_3^* = b_4 \oplus b_3 \oplus b_2 \oplus p_3 = 1$

$C_3^*\, C_2^*\, C_1^* =$ 110 which indicate position 6 in error Transmitted code 1001100.

10. (D) $X = MNQ + M\overline{N}Q + \overline{M}NQ$

$= MQ + \overline{M}NQ = Q(M + \overline{M}N) = Q(M + N)$

11. (A) The logic circuit can be modified as shown in fig. S. 4.1.11

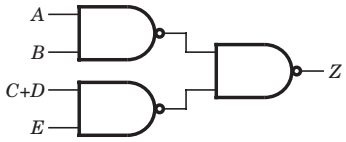


Fig. S4.1.11

Now $Z = AB + (C + D)E$

12. (D) You can see that input to last XNOR gate is same. So output will be HIGH.

13. (D) $Z = \overline{A} + (\overline{AB} + \overline{BC}) + \overline{C}$

$= \overline{A} + (\overline{A} + \overline{B} + \overline{B} + \overline{C}) + \overline{C} = \overline{A} + \overline{B} + \overline{C}$

$\overline{ABC} = \overline{A} + \overline{B} + \overline{C}$

$\overline{AB} + \overline{BC} + \overline{AC} = \overline{A} + \overline{B} + \overline{B} + \overline{C} + \overline{A} + \overline{C} = \overline{A} + \overline{B} + \overline{C}$

14. (C) $(X + \overline{Y})(\overline{X} + Y) = XY + \overline{X}\,\overline{Y}$

$(X + Y)(X + \overline{Y})(\overline{X} + Y) = (X + Y)(XY + \overline{X}\,\overline{Y})$

$= XY + XY = XY$

15. (B) Using duality

$(A + B)(\overline{A} + C)(B + C) = (A + B)(\overline{A} + C)$

Thus (B) is correct option.

16. (B) $Z = \overline{(\overline{AB})(\overline{CD})(\overline{EF})} = AB + CD + EF$

17. (A) $X = (A\,\overline{B} + \overline{A}B)\overline{(A + \overline{B})} = (A\overline{B} + \overline{A}\,B)(\overline{A}B) = \overline{A}B$

18. (B) $Y = \overline{(A \oplus B) \cdot C} = \overline{(A\overline{B} + \overline{A}C) \cdot C}$

$= \overline{(A\overline{B} + \overline{A}B)} + \overline{C} = \overline{A}\,\overline{B} + AB + \overline{C}$

19. (C) $Z = A(A + \overline{A})BC = ABC$

20. (A) $Z = AB(\overline{B} + C) = ABC$

21. (A) $Z = \overline{(\overline{A} + \overline{B})} \cdot BC = (AB) \cdot BC = ABC$

22. (A) $A(A + \overline{B})(A + \overline{B} + C)$

$= (AA + A\overline{B})(A + \overline{B} + C) = A(A + \overline{B} + C) = A$

Therefore No gate is required to implement this function.

23. (A)

A	B	C	$(A + BC)$	$(A + B)(A + C)$
0	0	0	0	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	1
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

Fig. S 4.1.23

24. (B) $\overline{X} = \overline{A}\,\overline{B}C + A\overline{B}C + AB\overline{C} = \overline{B}C + AB\overline{C}$

25. (B) $(\overline{A + B})\overline{(B + \overline{C})} = (\overline{A}\,\overline{B})(\overline{B}C) = \overline{A}\,\overline{B}C$

$\overline{(\overline{A + B})\overline{(B + \overline{C})}} = (A + B) + (B + \overline{C}) = A + B + \overline{C}$

$\overline{(\overline{A} + B)(\overline{B + C})} = \overline{(\overline{A} + B)} + (B + C)$

$= A\overline{B} + B + C = A + B + C$

From truth table $Z = A + B + \overline{C}$

Thus (B) is correct.

26. (D) $AC + B\overline{C} = AC(B + \overline{B}) + (A + \overline{A})B\overline{C}$

$= ABC + A\overline{B}C + AB\overline{C} + \overline{A}B\overline{C}$

27. (D) $F = A + \overline{A}B + \overline{A}\,\overline{B}C + \overline{A}\,\overline{B}\,\overline{C}(D + \overline{D}E)$

$= A + \overline{A}B + \overline{A}\,\overline{B}(C + \overline{C}(D + E))$

$= A + \overline{A}(B + \overline{B}(C + D + E)) = A + B + C + D + E$

28. (B) $A(B + C\,\overline{(AB + AC)}) = AB + AC\,(\overline{AB} \cdot \overline{AC})$

$= AB + AC[(\overline{A} + \overline{B})(\overline{A} + \overline{C})]$

$= AB + AC\,(\overline{A} + \overline{A}\,\overline{C} + \overline{A}\,\overline{B} + \overline{B}\,\overline{C}) = AB$

29. (C) $\overline{\overline{(A\overline{B})} \cdot \overline{(\overline{A}B)}} = \overline{\overline{A\overline{B}}} + \overline{\overline{\overline{A}B}} = A\overline{B} + \overline{A}B$

30. (B) $X\overline{Z} + \overline{X}Z = X\overline{(X\overline{Y} + \overline{X}\overline{Y})} + \overline{X}(X\overline{Y} + \overline{X}Y)$

$= X(XY + \overline{X}\,\overline{Y}) + \overline{X}Y = XY + \overline{X}Y = Y$

31. (A) $X \oplus Y = X\overline{Y} + \overline{X}Y = \overline{(XY + \overline{X}\overline{Y})} = \overline{(\overline{X}\overline{Y})} = X + Y$

32. (C) There are $2^4 = 16$ different input condition. Only one of these (0 0 0 0) produces a LOW output.

33. (A) $X = A + B \oplus C$

34. (A) $X = (AB)(CD + \overline{C}\overline{D})$

35. (C) X will be HIGH when $A \neq B$, $B = C$, and $C = 1$, thus $C = 1,\ B = 1,\ A = 0$ is the input condition.

36. (D) For both statement here are case that refutes statements

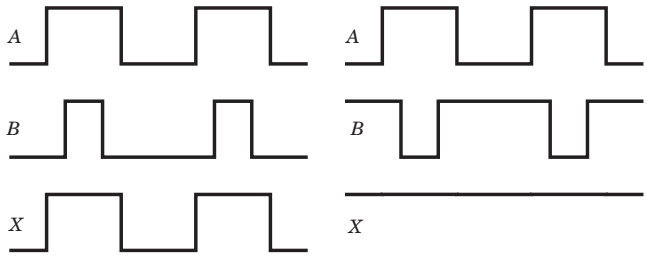


Fig. S4.1.36

37. (D)

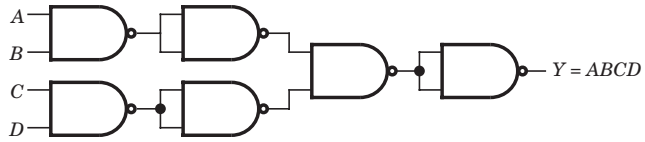


Fig. S4.1.37

38. (A)

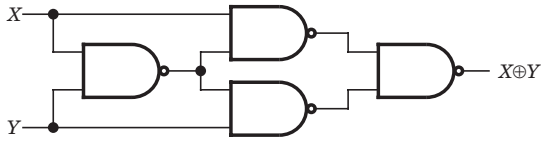


Fig. S4.1.38

output $= (\overline{XY})X + (\overline{XY})Y$

$= (\overline{X} + \overline{Y})X + (\overline{X} + \overline{Y})Y = X\overline{Y} + Y\overline{X} = X \oplus Y$

39. (A) $Z = A\overline{B}C = \overline{\overline{AC\overline{B}}} = \overline{\overline{AC} + B}$

If $\overline{AC} = D$ Then $Z = \overline{D + B}$

Therefore one NAND and one NOR gate is required and cost will be 2 unit.

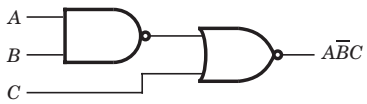


Fig. S4.1.39

40. (C) 4 NAND is required to made a NOR

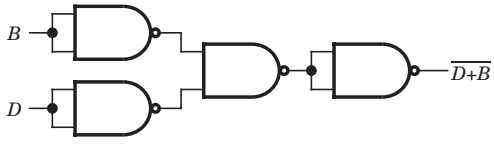


Fig. S4.1.40

41. (D) Output of NAND must be LOW for LED to emit light. So both input to NAND must be HIGH. If any one or both switch are closed, output of AND will be LOW. If both switch are open, output of XOR will be LOW. So there can't be both input HIGH to NAND. So LED doesn't emit light.

42. (D) Output of 1st XOR $= \overline{X}1 + X\overline{1} = \overline{X}$

Output of 2nd XOR $= \overline{X}\overline{X} + XX = 1$

So after 4, 6, 8,.....20 XOR output will be 1.

43. (B) $\bar{f} = x\bar{y}$, $f = \bar{x} + y$

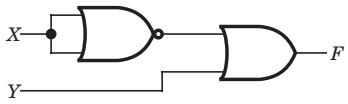


Fig. S4.1.43

44. (C)

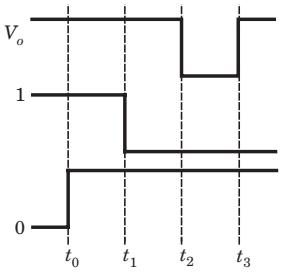


Fig. S4.1.44

45. (C) Output of gate 1 is X_0X_1

Output of gate 2 is $X_0X_1 + X_2$

Output of gate 3 is $(X_0X_1 + X_2)X_3 = X_0X_1X_3 + X_2X_3$

Output of gate 4 would be $X_0X_1X_3 + X_2X_3 + X_4$

Output of gate 5 would be $X_0X_1X_3X_5 + X_2X_3X_5 + X_4X_5$

So output of gate n would be

$X_0X_1X_3X_5 \ldots X_n + X_2X_3X_5 \ldots X_n + X_4X_5X_7 \ldots X_n + X_{n-1}X_n$

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