coherentmusings

Things i enjoy

PCB Design Fundamentals – Impedance Matching

January 19, 2013 by *coherentmusings*

About three years ago, when I used to think that the printed circuit boards were nothing, but, just a means for connecting the various components to each other and the system design was much more important. Working in the industry for the past two and half years, has made me realize that even though the system design is quiet important, a well designed system is not going to work without proper attention being paid to the PCB Design.

There are various aspects to PCB design like crosstalk, EMI and EMC, differential signalling and one of them is impedance matching. All this is known in the industry under the broad term and umbrella name of "Signal Integrity". An impedance mismatch can affect the signal integrity to a great extent and the damage done depends on the impedance mismatch and the complexity of the interconnect network in which the impedance mismatch is occurring.

The concept of impedance mismatch will be known to anyone who has studied Transmission Lines in Electromagnetics or Microwave Engineering. Now, you might be wondering how does transmission lines come into the picture??!!.

At high frequencies, the interconnect lines do not function as simple interconnects, but, start acting as transmission lines at high frequencies. Also, if you remember control systems, at low frequencies a lumped parameter model is applicable, while at high frequencies, distributed parameter model becomes applicable. If i were to put it more simply, when the wavelength of the signal is less than the length of the interconnect on which it is propagating, you can treat them as simple interconnects and apply the lumped parameter model, meaning that you can model the behavior of the interconnect using a simple RC model. The response of a RC model is well-known to all in the field of electronics. At high frequencies, where the wavelength of the signal is less than the length of the interconnect on which it is propagating, you can no longer consider them as mere interconnects, but, the distributed parameter model becomes applicable and the transmission line concepts need to be applied now. A simple RC model will no longer suffice for modelling the behavior of interconnects.

In actual production environments and industry, PCB design and signal integrity issues like impedance mismatch are done and checked using software like PADS and Allegro. For a demonstration, I will show you how an impedance mismatch degrades signal integrity by using an example and lattice diagrams.

An impedance mismatch occurs, when the characteristic impedance of the transmission line doesn't

match the load or another transmission line which it is driving. If you remember the formula for reflection co-efficient $\tau = (Zl - Zo)/(Zl + Zo)$. So, if the load impedance is not equivalent to the characteristic impedance, the reflection co-efficient will have a value, ideally which should have been zero. This impedance mismatch results in a part of the signal being transmitted and part of it being reflected. The reflected signal then propagates back towards the source, where depending on the impedance of the source and the line, another reflection might or might not occur. This goes on till this reaches steady state.

A lattice diagram is a graphical technique used to solve the multiple reflections on a transmission line with linear loads. The left- and right-hand vertical lines represent the source end (z = 0) and load end (z = l) of the transmission line. The diagonal lines contained between the vertical lines represent the signal bouncing back and forth between the source and the load. The diagram progressing from top to bottom represents increasing time. Notice that the time increment is equal to the time delay τd of the transmission line, and the reflection coefficients looking into the source and into the load are labeled at the top of the vertical bars. The lowercase letters represent the magnitude of the reflected signal traveling on the line. The uppercase letters represent the voltages seen at the source, and the primed uppercase letters represent the voltage seen at the load end of the line. The delay for the signal to propagate from one end of the transmission line to the other is given by " $l\sqrt{LC}$ ", where l is the length of the transmission line and L and C are the inductance and capacitance values per unit length.

Consider the case of reflections when the impedance of the source Rs is less than the load impedance Zo.

The lattice diagram will come out as like shown below. The calculations for the lattice diagram will be as below.

1. A 2V signal is going to be driven on the line. Using a simple voltage divider, the voltage driven at point A will be 2 x 50/(25 + 50) = 1.33V. When 1.33V reaches the load end, this will be multiplied by the reflection co-efficient at the load end, viz. 1. So, the entire signal will be reflected back onto the line, and the voltage will be 1.33V as shown, propagating towards the source. At the load end, 1.33V + 1.33V = 2.66V will be the voltage.

2. The reflection co-efficient at the source end is (25 – 50)/(25 + 50) = (-1/3). The incoming 1.33V signal toward the source will be multiplied by (-1/3) and then propagate back towards the load. So, (-1/3) x 1.33 = -0.443V signal will now propagate towards the load end. At the source, the voltage is given by 1.33V + 1.33V + (-0.44V) = 2.22V.

3. Again at the load end, the -0.443V signal will be reflected back fully due to the reflection co-efficient being 1 and you can see a -0.443V signal propagating back toward the source in the above lattice diagram. At the load end, the voltage will be 2.66-0.443-0.443 = 1.77V.

4. On reaching the source end, the (-0.443V) signal will be multiplied by a reflection co-efficient of (-1/3) giving a 0.148V signal again propagating towards the load as shown in the lattice diagram. The voltage at the source end will be 2.22-0.443+0.148 = 1.92V.

5. On reaching the load end, the 0.148V signal will be multiplied by the load reflection co-efficient of 1 and this will travel back towards the source. At the load end, the voltage will be 1.77+0.148+0.148 = 2.07V.

Carrying out the calculations similarly for the falling edge and using the above calculations for rising edge, will result in a waveform as shown below.

As you can see, a 2V signal driven on the transmission line resulted in a signal much different than what it should have been, due to the impedance mismatch.

Also, notice the particular ringing effect in the waveform. This happens when the impedance of the source Rs is less than the load impedance Zo, so called an over driven transmission line. The opposite case of an under drive transmission line, with Rs > Zo, will not show ringing, but will result in such a distortion.

The above is just a very simple case. An analysis in the manner of above for multiple cascaded transmission lines will be much involved and such a case can severely degrade the signal integrity.

The impedance matching is taken care of by controlling the length of the transmission line, it's width and height of the line from the reference ground plane while designing the PCB using EDA software tools.

N.B. The example is an unsolved example taken from the book "Advanced Signal Integrity for High Speed Digital Designs" by Stephen Hall and Howard Heck. The calculations are done by me and the figures have been copied from the book. In case any publisher or author of the book has any copyright issue with this, drop me a mail on victorascroft@gmail.com. I will take them down and replace them with different photographs and example.

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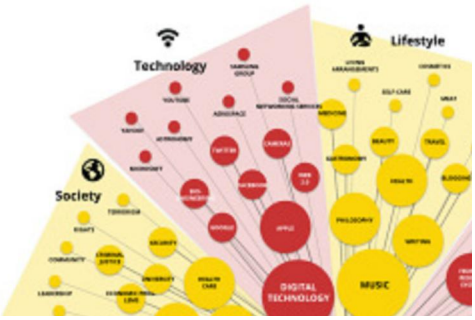

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14 thoughts on "PCB Design Fundamentals – Impedance Matching"

1. Bazar Gorj Free Directory Listing says:
   January 26, 2013 at 12:45 AM
   I used to be suggested this blog by way of my cousin. I'm now not certain whether or not this put up is written by way of him as nobody else recognise such designated about my difficulty. You are incredible! Thanks!

   Reply
2. Bazar Gorj Free Directory Listing says:
   January 26, 2013 at 4:56 AM
   Useful information. Fortunate me I found your site by accident, and I am stunned why this accident did not took place in advance! I bookmarked it.

   Reply
3. lista de emails says:
   January 28, 2013 at 6:21 PM
   thanks for the post.. lista de emails lista de emails lista de emails lista de emails lista de emails

   Reply
4. Anonymous says:
   January 29, 2013 at 2:05 AM
   the most incredible things about your website are the structure and the information you provide. seo seo seo seo seo

   Reply
5. How to make private server aion says:
   February 3, 2013 at 11:18 PM
   Magnificent points altogether, you just gained emblem new|a new} reader. What may you recommend in regards to your post that you just made a few days ago? Any sure?

Reply

6. cabal online guide dungeon says:
February 4, 2013 at 1:53 AM
A person essentially assist to make significantly articles I might state. That is the very first time I frequented your web page and up to now? I amazed with the analysis you made to make this actual publish incredible. Great process!

Reply

7. cabal online guide dungeon says:
February 4, 2013 at 1:54 AM
Just desire to say your article is as astonishing. The clarity in your put up is just spectacular and i can assume you are an expert in this subject. Fine along with your permission let me to snatch your RSS feed to stay up to date with impending post. Thanks a million and please carry on the enjoyable work.

Reply

8. cabal online hack says:
February 4, 2013 at 1:58 AM
Hello there, You've done an incredible job. I will certainly digg it and personally suggest to my friends. I'm sure they'll be benefited from this website.

Reply

9. RUSH PCB says:
February 8, 2013 at 3:55 AM
I have found this article very exciting. Do you have any others on this topic? I am also sending it to my friend to enjoy your writing style. Thanks

Reply

    - coherentmusings says:
    February 9, 2013 at 10:33 PM
    Hello. Thanks for the appreciation. I intend to write an article on differential signalling and crosstalk. Hopefully, i will get around to doing it soon.

    Reply

10. matasari says:
February 12, 2013 at 11:41 PM
I used to be suggested this website via my cousin. I am now not sure whether or not this post is written via him as no one else recognise such designated approximately my difficulty. You're amazing! Thanks!

Reply

11. Britney Lollie says:
February 18, 2013 at 3:36 AM
Nice read, I just passed this onto a colleague who was doing a little research on that. And he actually bought me lunch because I found it for him smile Therefore let me rephrase that: Thank you for lunch! "Not only is the universe stranger than we imagine, it is stranger than we can imagine." by Sir Arthur Eddington.

Reply

12. Avi says:
February 20, 2013 at 5:37 PM
Hello,

I have designed a 2 layer board in AWR Microwave Office, How do I ensure that all the copper tracks are of 50 ohms impedance ?

Reply

- coherentmusings says:
  February 26, 2013 at 12:34 PM
  I have never used AWR Microwave Office. The general idea is to adjust the width of the track, length of the track from the source to destination point and height of the copper track from the ground plane to achieve the required impedance.

  Reply