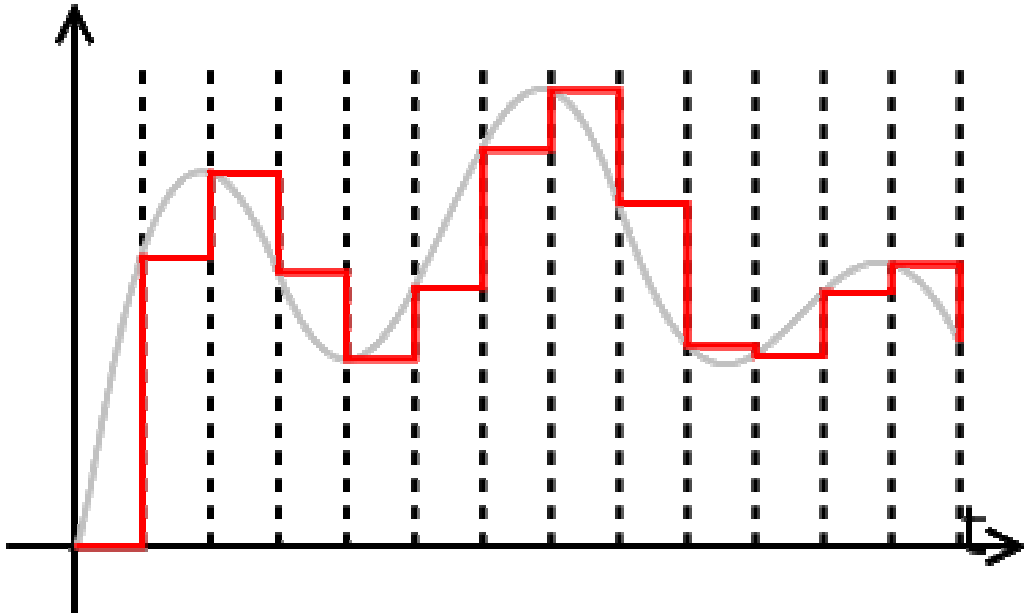
Chapter 8

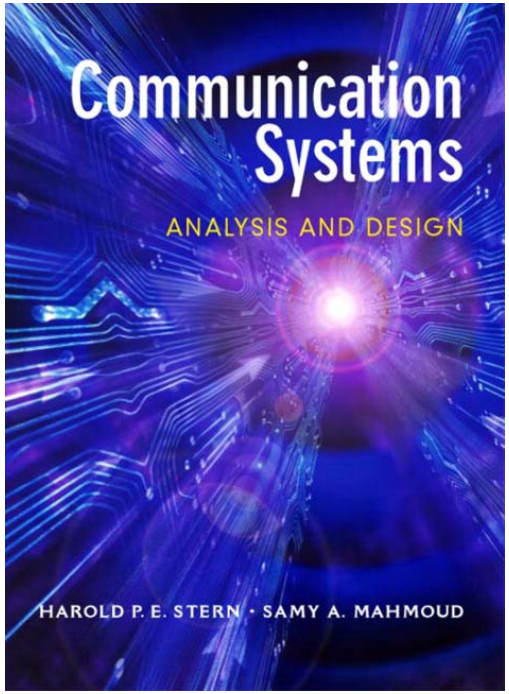
Analog-to-Digital and Digital to Analog Conversion



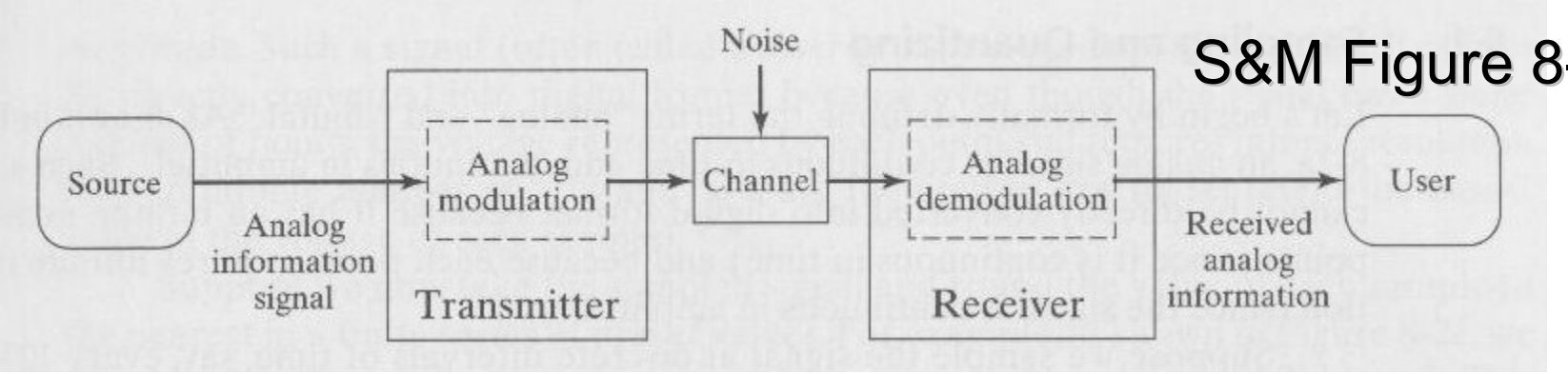
Chapter 8

Analog-to-Digital and Digital-to-Analog Conversion

- *Sampling and Quantization*
- Pages 390-391

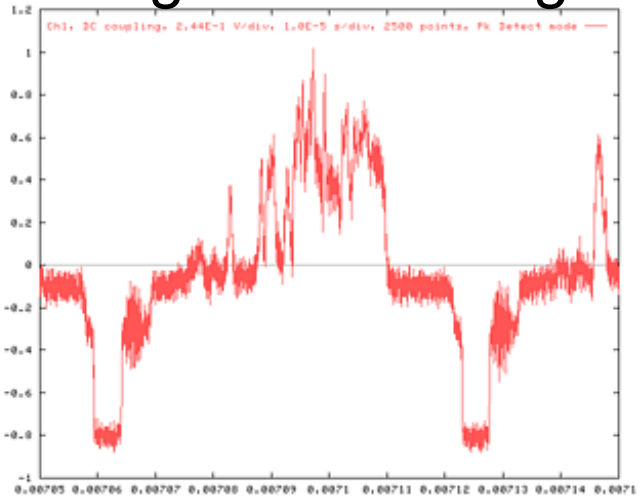


- Traditional *analog transmission* (AM, FM and PM) are less complex than digital data transmission have been the basis of broadcasting and communication for 100 years.

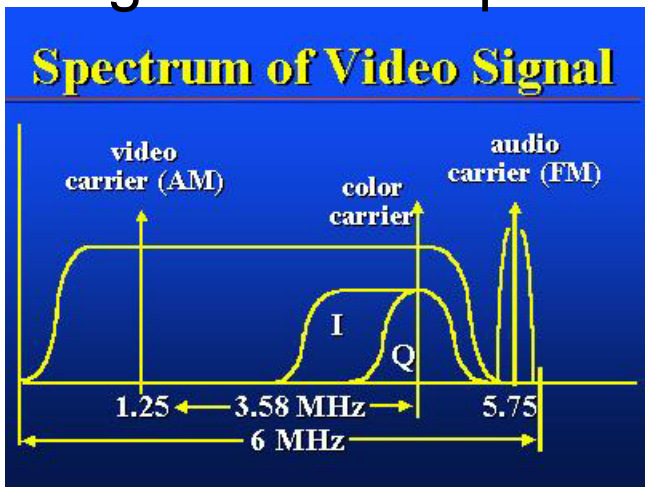


S&M Figure 8-1a

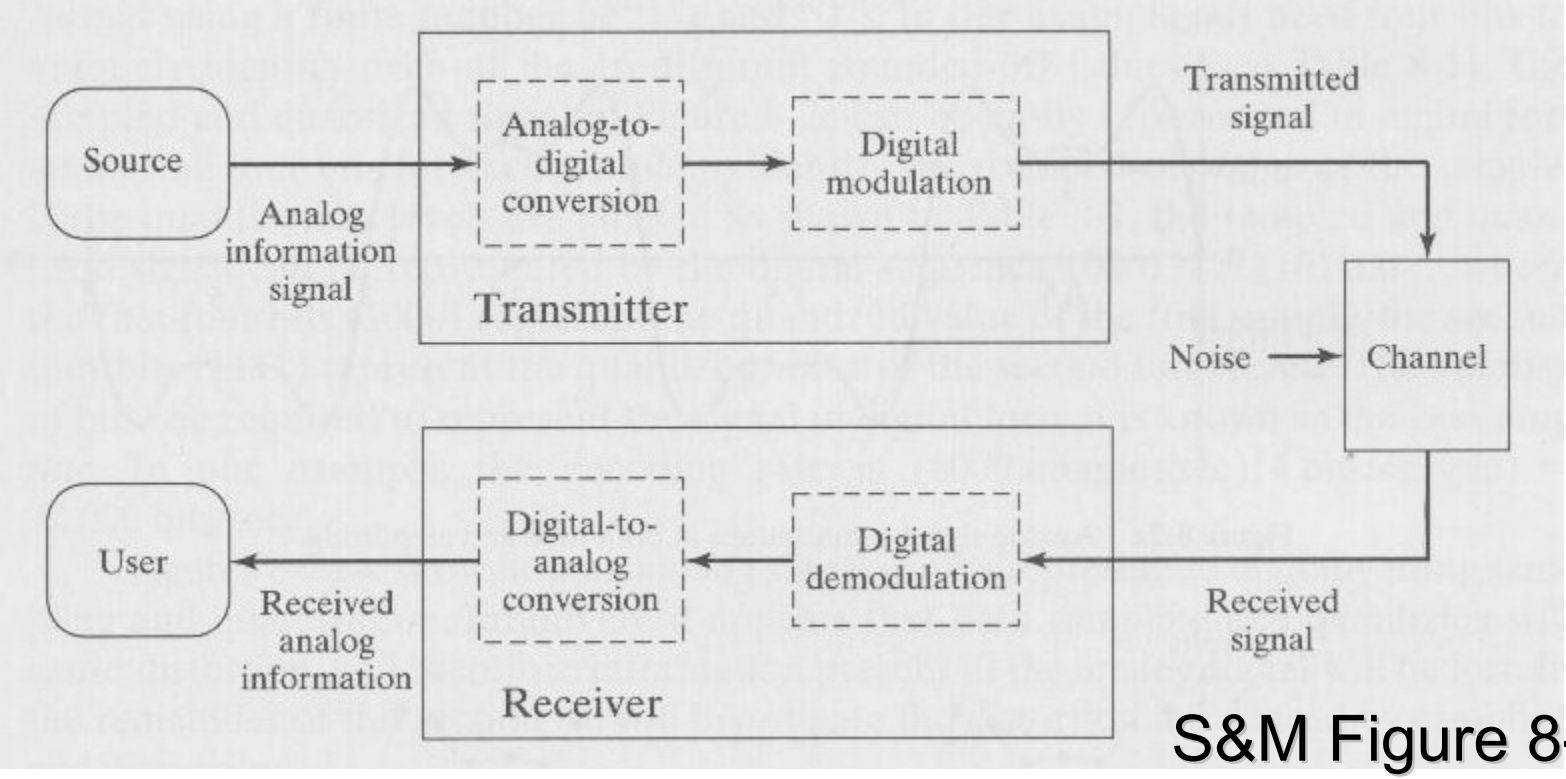
Analog television signal



Analog television spectrum

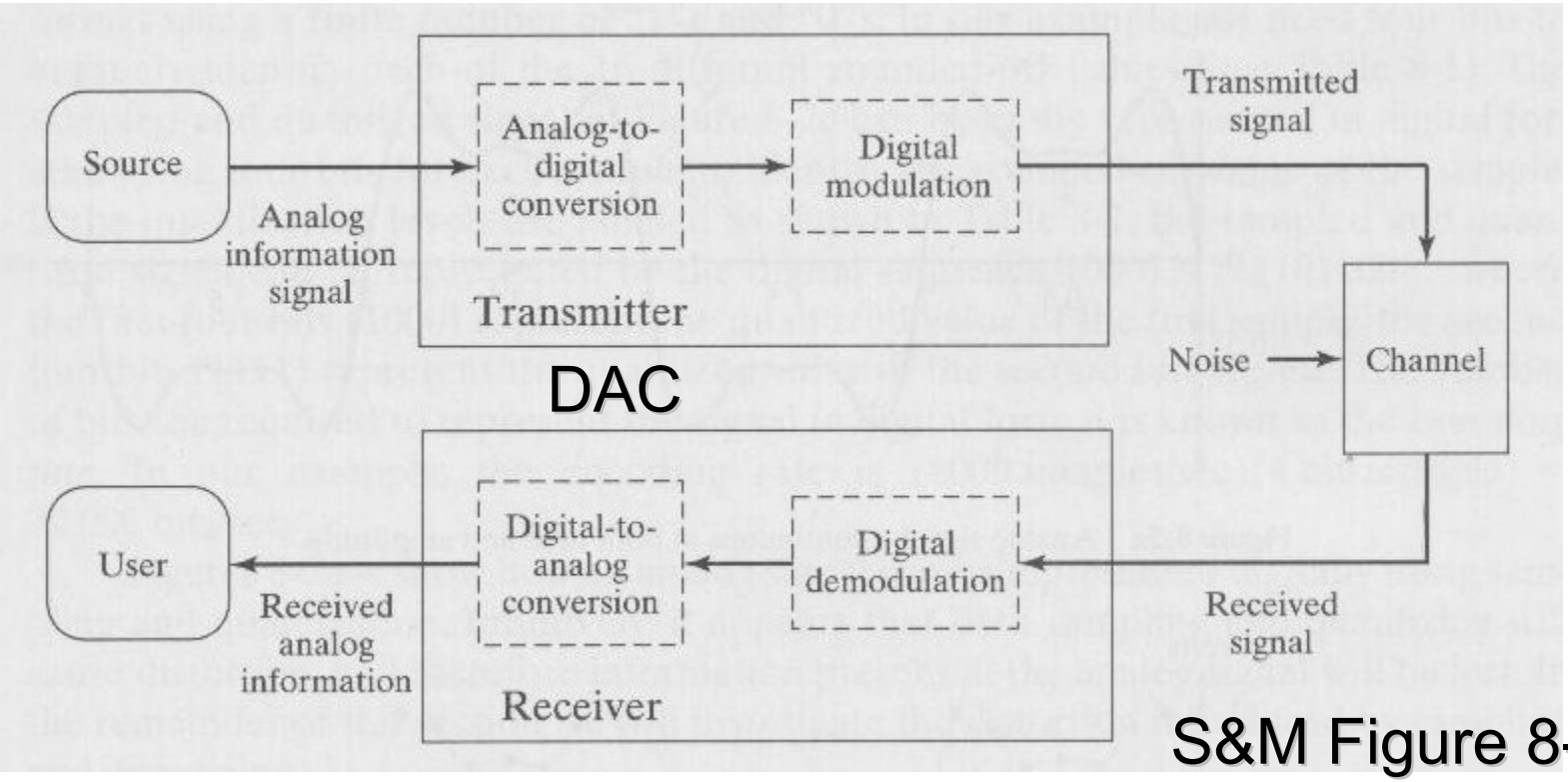


- *Digital data transmission* (PAM, ASK, PSK, FSK and QAM) is more complex but (perhaps) offers higher performance with control of accuracy and easier storage, simpler signal processing for noise reduction, error detection and correction and encryption.



S&M Figure 8-1b

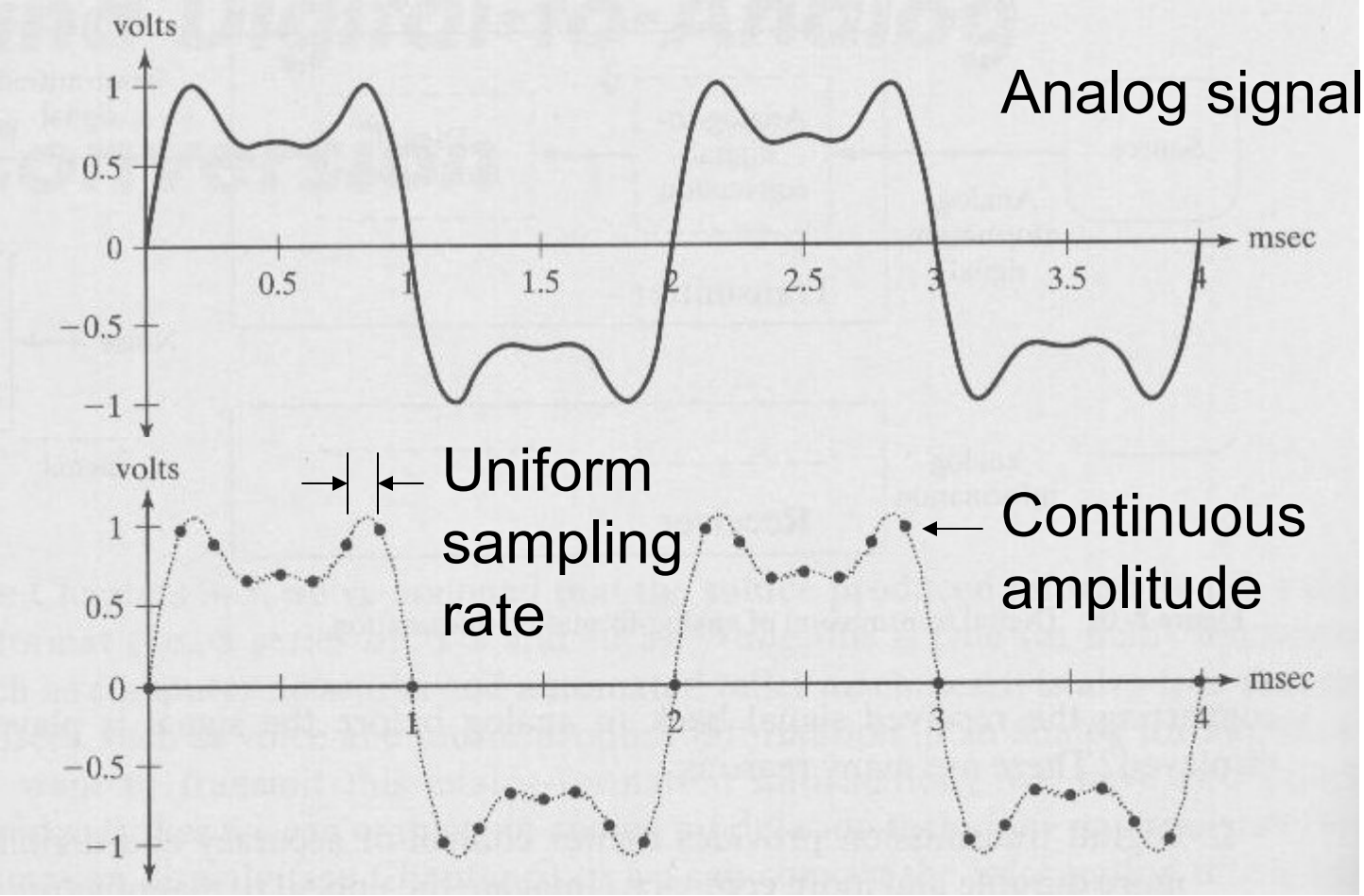
- Digital data transmission requires analog-to-digital (ADC) and digital-to-analog (DAC) converters. The ADC process utilizes sampling and quantization of the continuous analog signal.



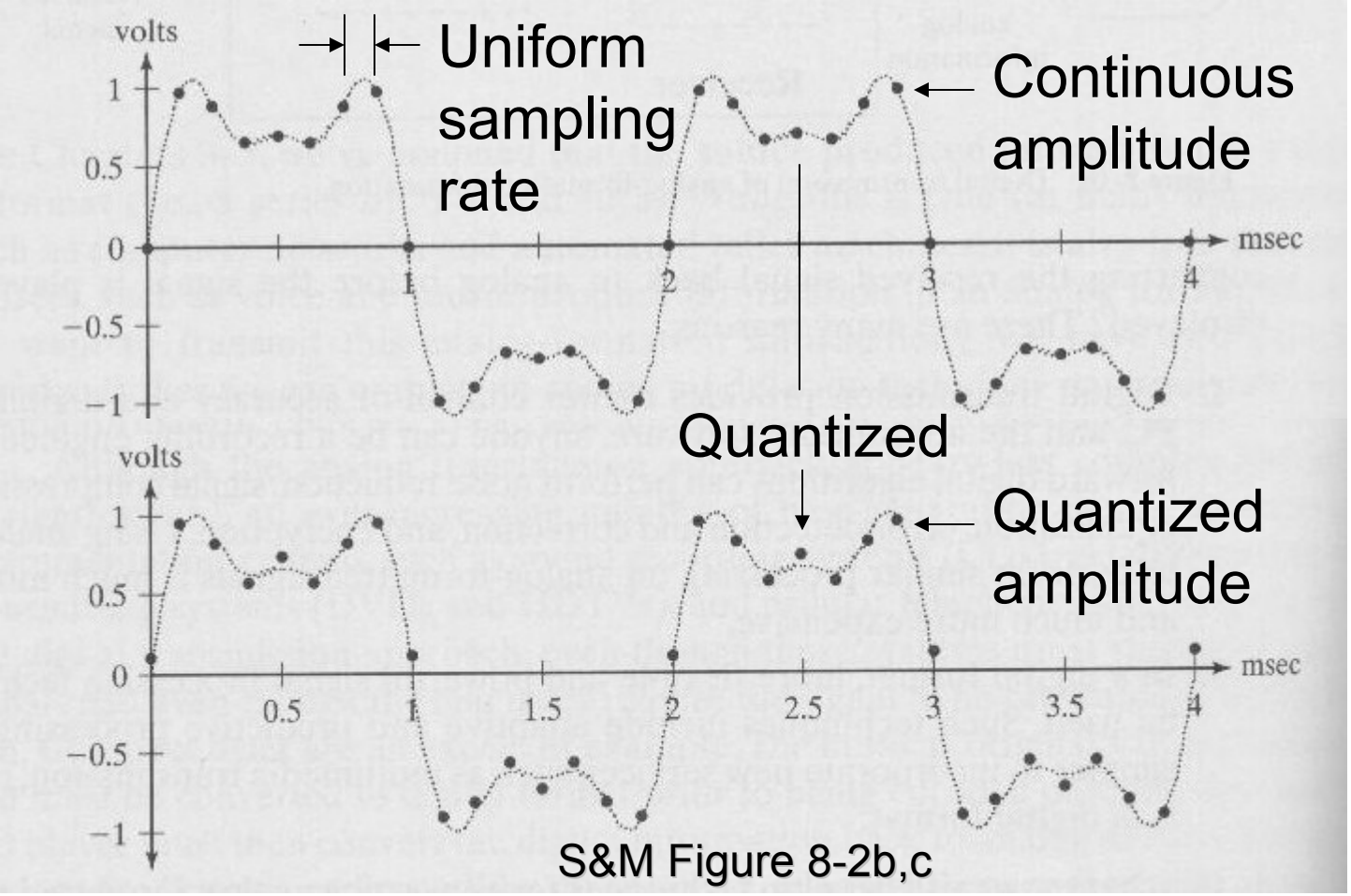
S&M Figure 8-1b

- ADC sampling occurs at a uniform rate (the *sampling rate*) and has a continuous amplitude.

S&M Figure 8-2a,b



- The continuous amplitude sample is then quantized to *n* bits or resolution for the *full scale* input or 2^n *levels*.



S&M Figure 8-2b,c

- Here n = 4 and there are $2^4 = 16$ levels for a full scale input of 2 V (± 1 V). The *step size* = 2 V / 16 = 0.125 V and the *quantized value* is the *midpoint* of the *voltage range*.

S&M Table 8.1

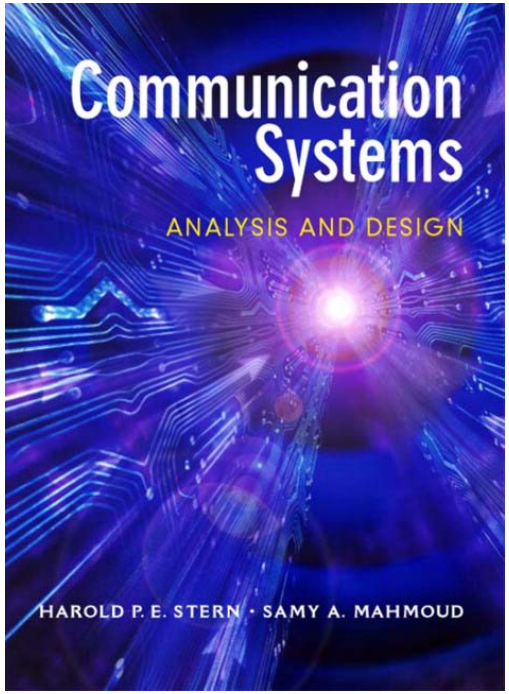
Table 8-1 Quantization Values and Binary Assignments for the Sampled Signal

Voltage Range of Signal $x(t)$	Rounded-off (Quantized) Value	Binary Assignment for Quantized Value
$-1.000 \le x(t) < -0.875$ v	−0.9375 v	0000
$-0.875 \le x(t) < -0.750$ v	−0.8125 v	0001
$-0.750 \le x(t) < -0.625$ v	−0.6875 v	0010
$-0.625 \le x(t) < -0.500$ v	−0.5625 v	0011
$-0.500 \le x(t) < -0.375$ v	−0.4375 v	0100
$-0.375 \le x(t) < -0.250$ v	−0.3125 v	0101
$-0.250 \le x(t) < -0.125$ v	−0.1875 v	0110
$-0.125 \le x(t) < 0.000$ v	−0.0625 v	0111
$0.000 \le x(t) < 0.125$ v	0.0625 v	1000
$0.125 \le x(t) < 0.250$ v	0.1875 v	1001
$0.250 \le x(t) < 0.375$ v	0.3125 v	1010
$0.375 \le x(t) < 0.500$ v	0.4375 v	1011
$0.500 \le x(t) < 0.625$ v	0.5625 v	1100
$0.625 \le x(t) < 0.750$ v	0.6875 v	1101
$0.750 \le x(t) < 0.875$ v	0.8125 v	1110
$0.875 \le x(t) \le 1.000$ v	0.9375 v	1111

Chapter 8

Analog-to-Digital and Digital-to-Analog Conversion

- *Sampling Baseband Analog Signals*
- Pages 392-399



- The analog signal x(t) which is continuously, uniformly sampled is represented by:

$$x_s(t) = x(t) \sum_{k=-\infty}^{\infty} \delta(t - kT_S) \qquad \text{S\&M Eq. 8.1}$$

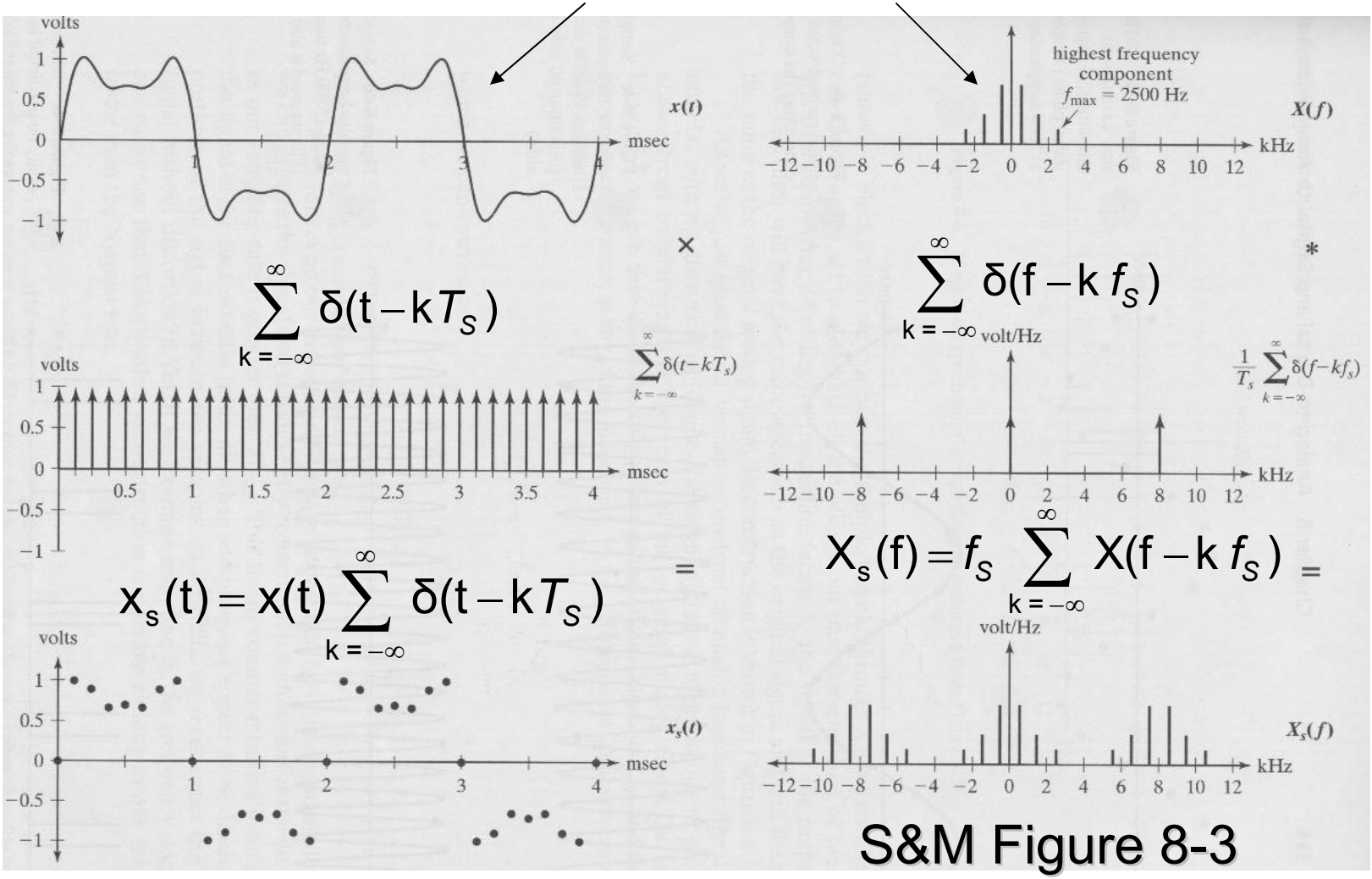
Multiplication in the temporal domain is convolution in the frequency domain and the frequency domain representation is:

$$X_s(f) = X(f) * \mathbb{F}\left\{ \sum_{k=-\infty}^{\infty} \delta(t - k\,T_S) \right\}$$

$$X_s(f) = X(f) * \left\{ f_S \sum_{k=-\infty}^{\infty} \delta(f - k\,f_S) \right\} \qquad \text{S\&M Eq. 8.2}$$

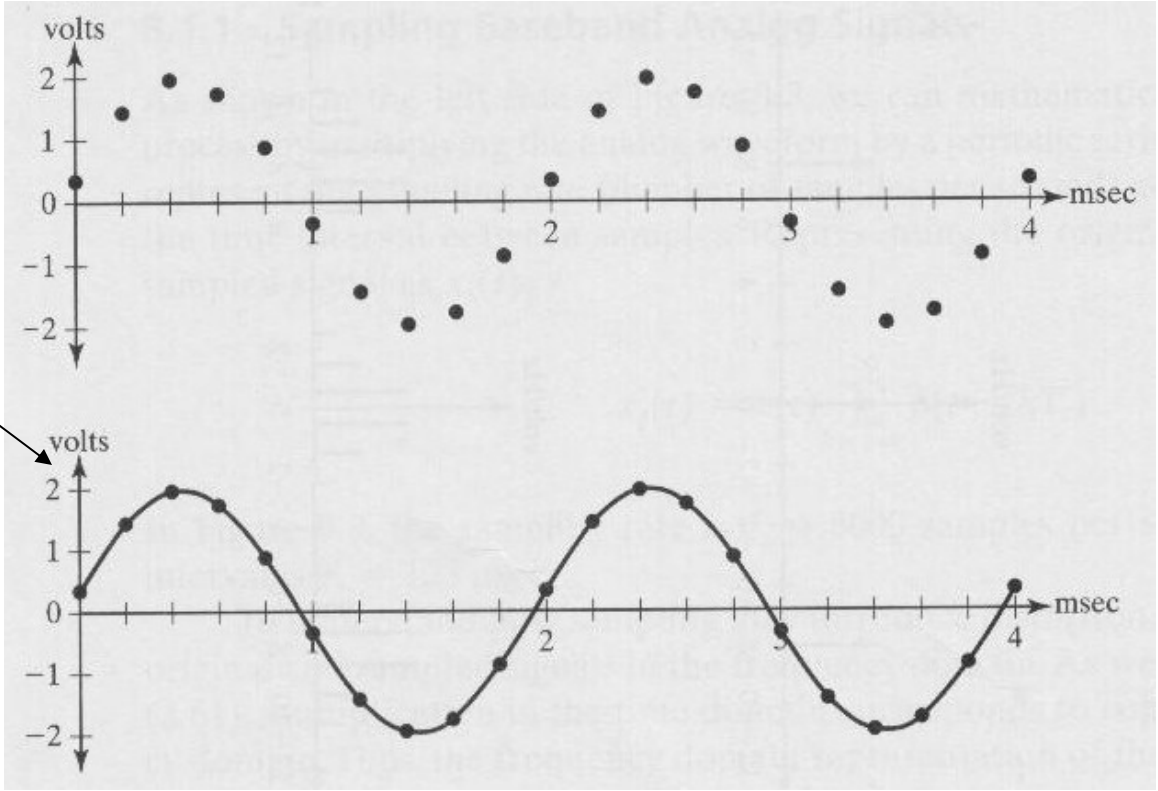
$$X_s(f) = f_S \sum_{k=-\infty}^{\infty} X(f - k\,f_S)$$

- Temporal and spectral representation of the continuous sampling process for a sum of three sinusoids.



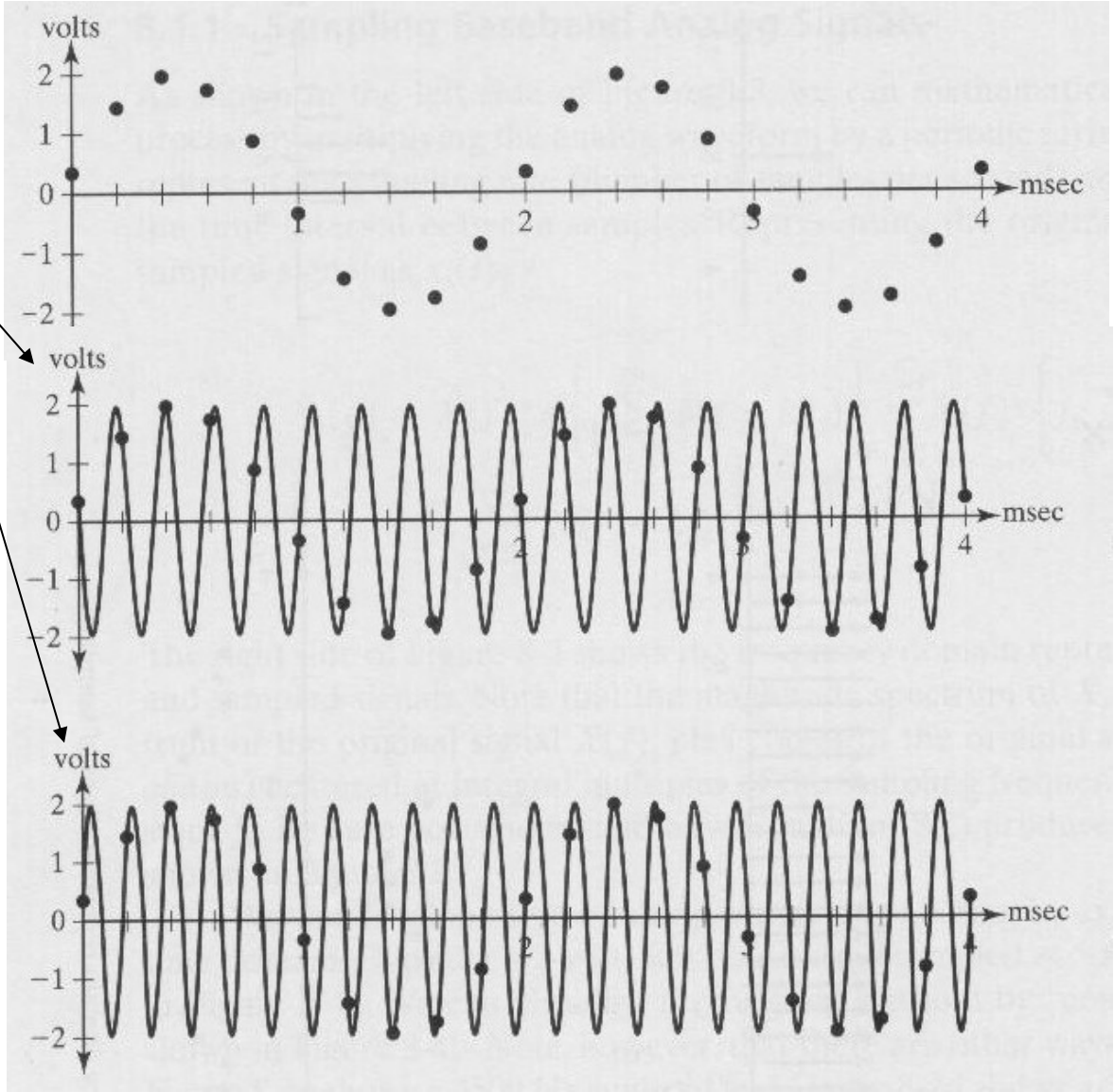
S&M Figure 8-3

- 2 V, 20° initial phase, 500 Hz sinusoid sampled at 5 k samples/sec



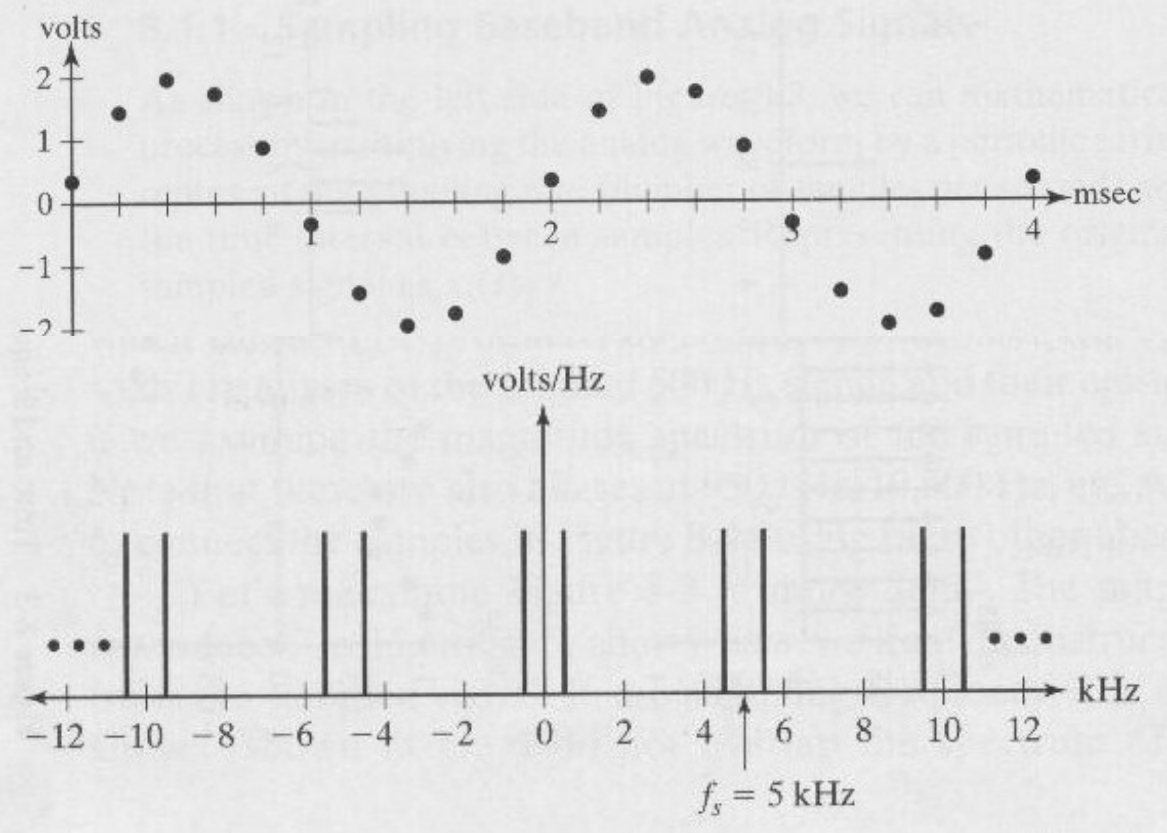
S&M Figure 8-4a,b

- Aliased samples can be reconstructed for a 4500 Hz and a 5500 Hz sinusoid that appears to be a 500 Hz sinusoid



S&M
Figure 8-4a,c,d

- The *aliasing* of the signal can be predicted by the magnitude spectrum of the original 500 Hz sampled signal.

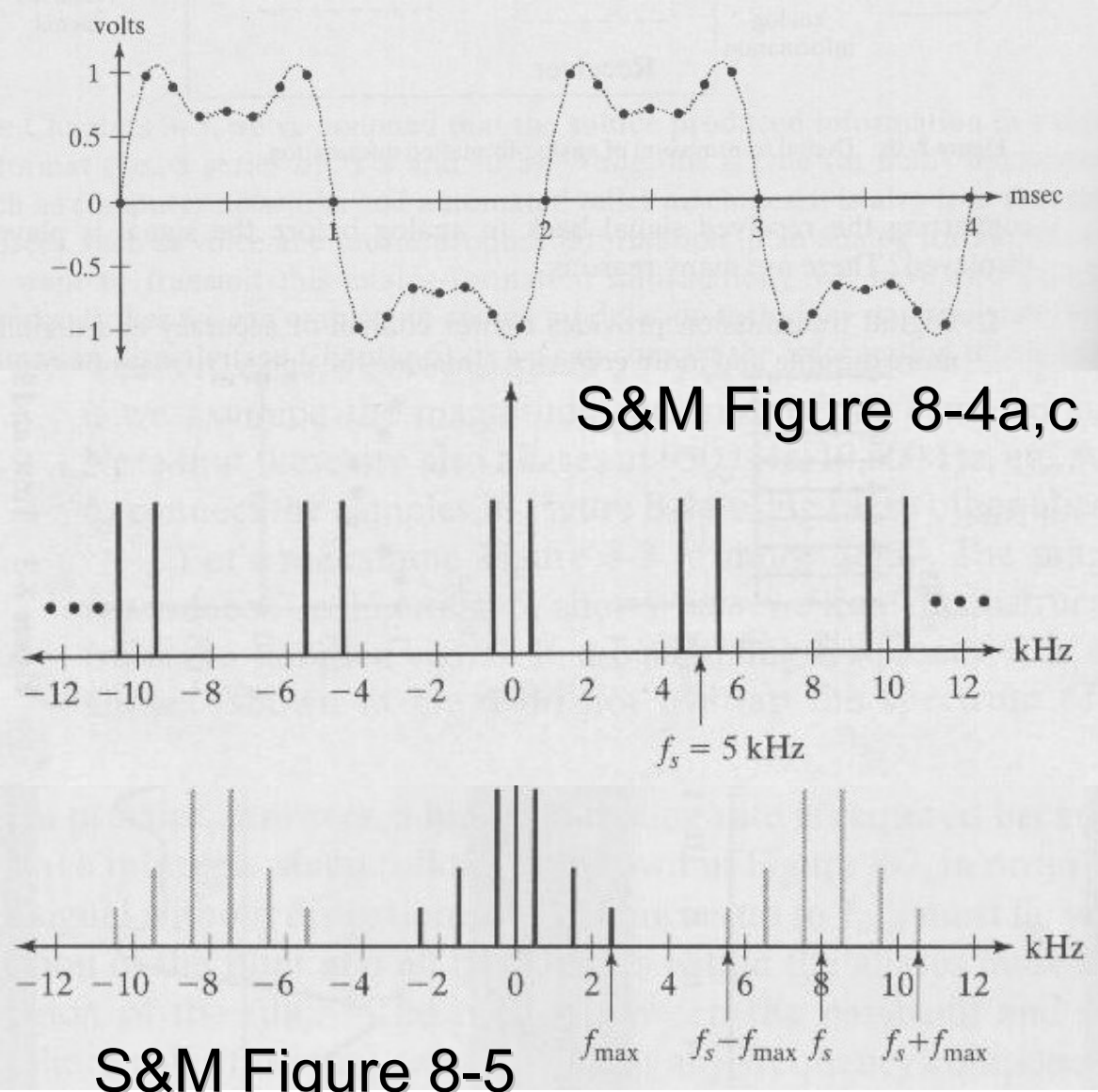


S&M Figure 8-4a,b

If the 4500 Hz and 5500 Hz signals are then sampled at 5 k samples/sec aliasing at occurs at | 4500 – 5000 | and (5500 – 5000) Hz

- The sum of three sinusoids does not have any aliased frequencies since the sampling frequency f_S is greater than twice the highest frequency f_{max}

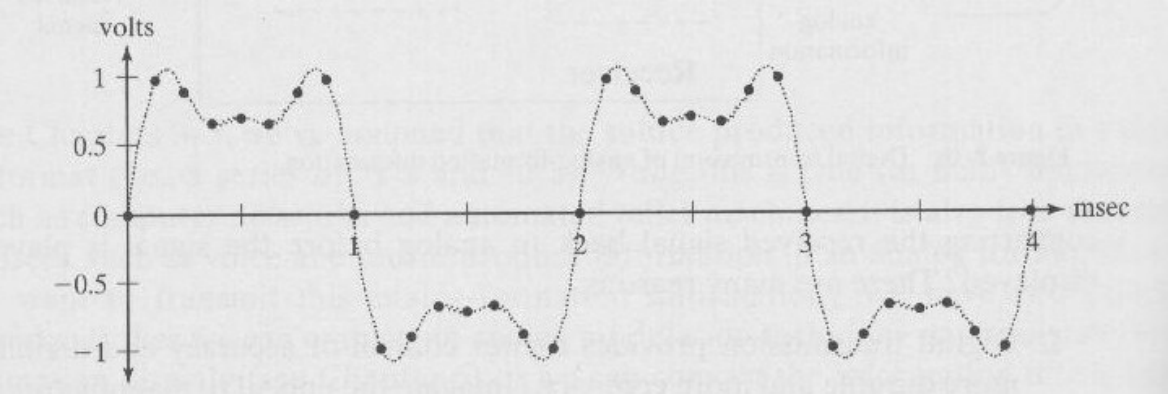
$$f_S > 2\, f_{max}$$



S&M Figure 8-4a,c

S&M Figure 8-5

- The frequency 2 f_{max} is called the *Nyquist frequency*.



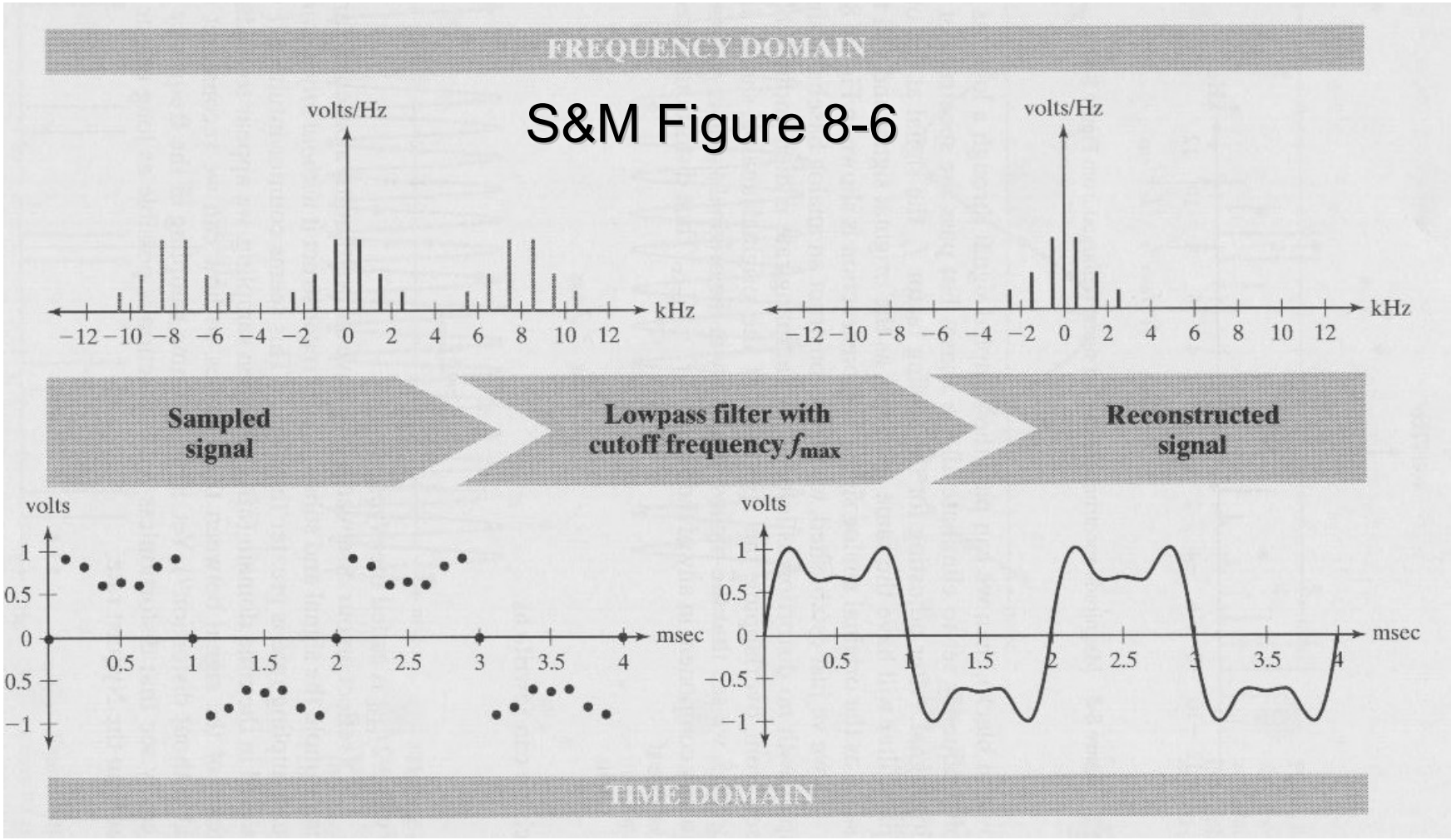
S&M Figure 8-4a

Harry Nyquist, who contributed to the understanding of thermal noise while at Bell Labs, is also remembered in electrotechnology for his analysis of sampled data signals.

Harry Nyquist
1889-1976

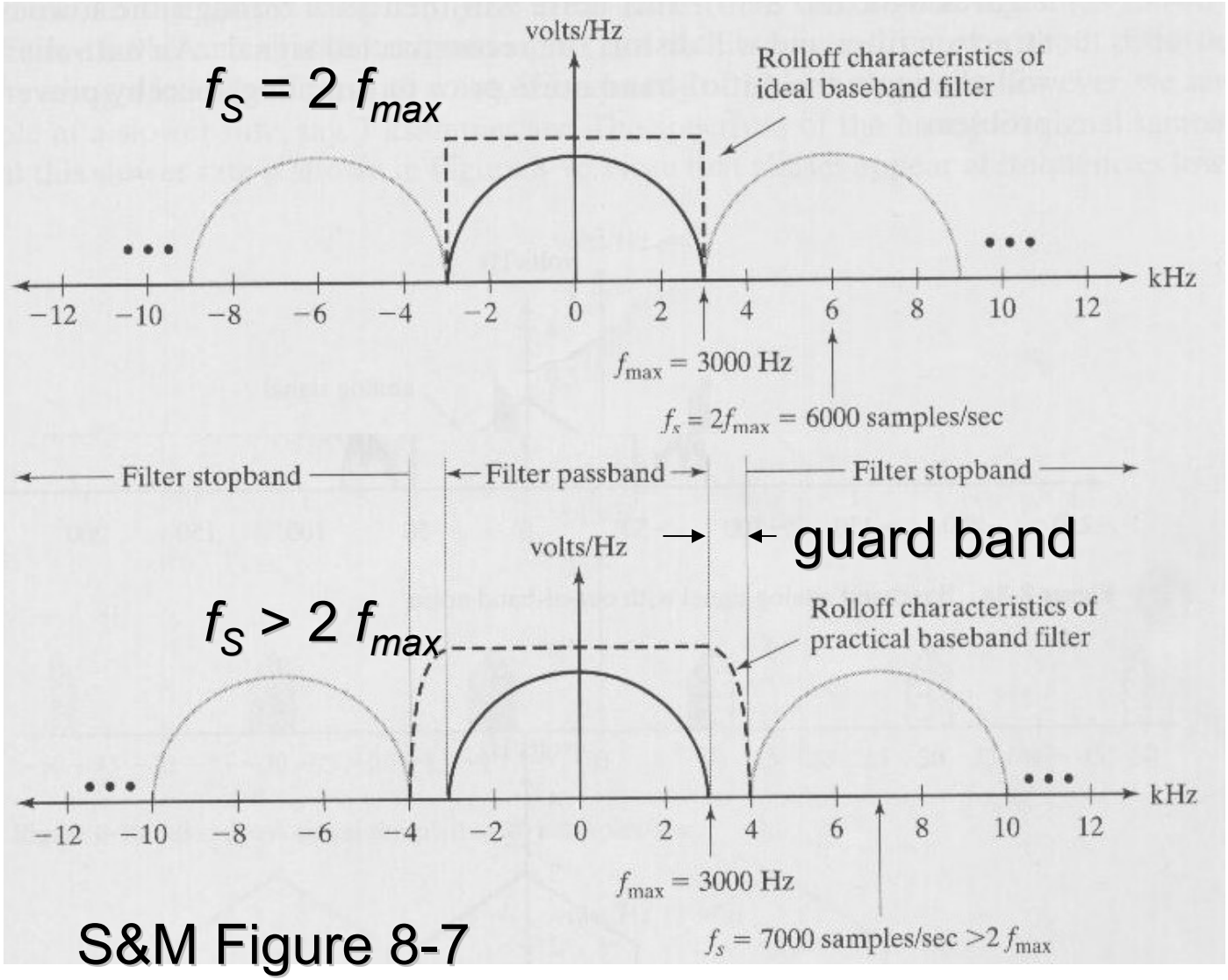
Bell Laboratories

- The analog signal is *reconstructed* from the quantized samples by a DAC and a low pass filter (LFP).



S&M Figure 8-6

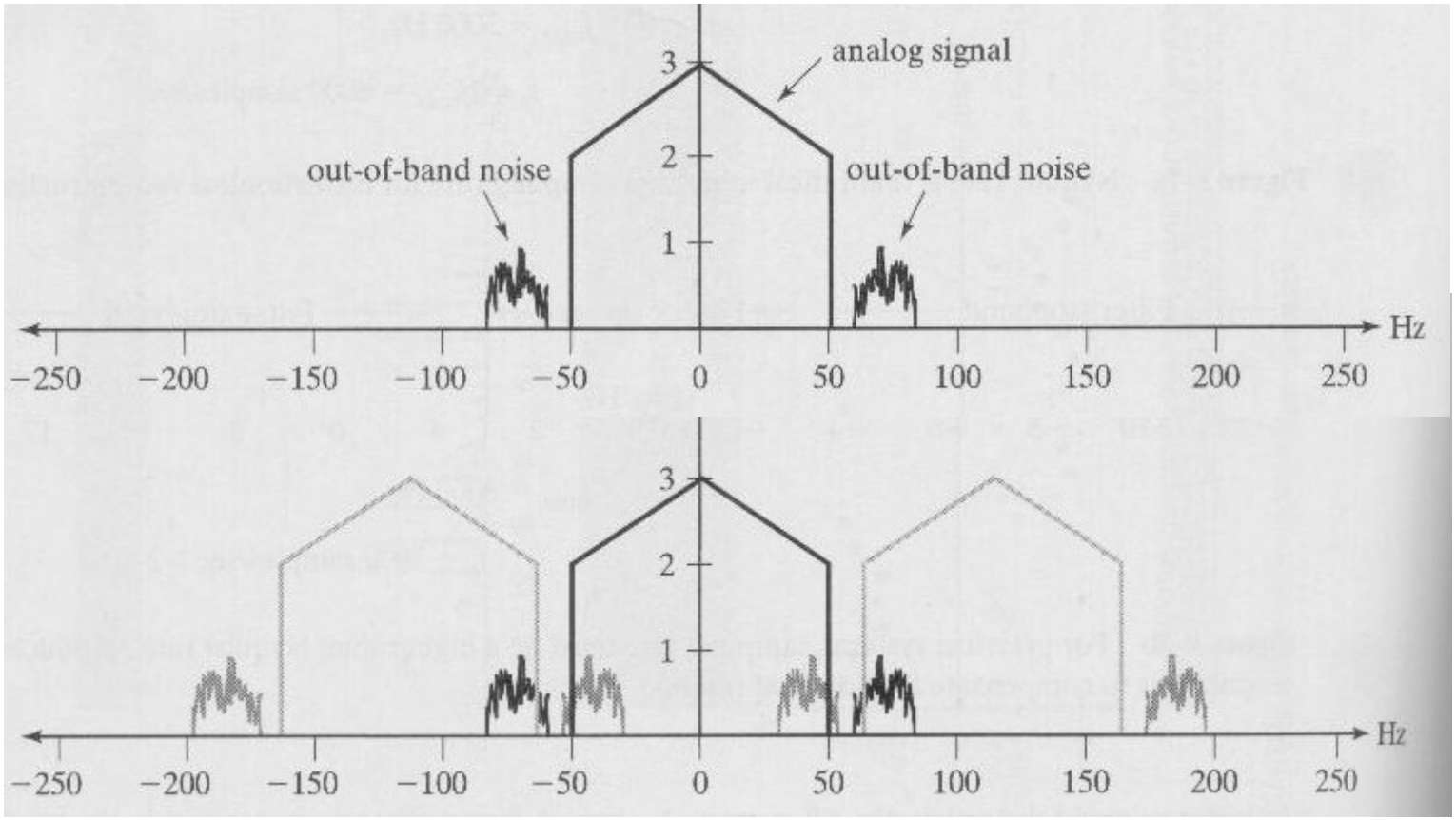
- For *practical signals* $f_S > 2\, f_{max}$ using a *guard band* for LPFs



S&M Figure 8-7

- With *out-of-band noise* and sample signals, aliases of the noise now appear *in-band* and should be filtered before the sampling process.

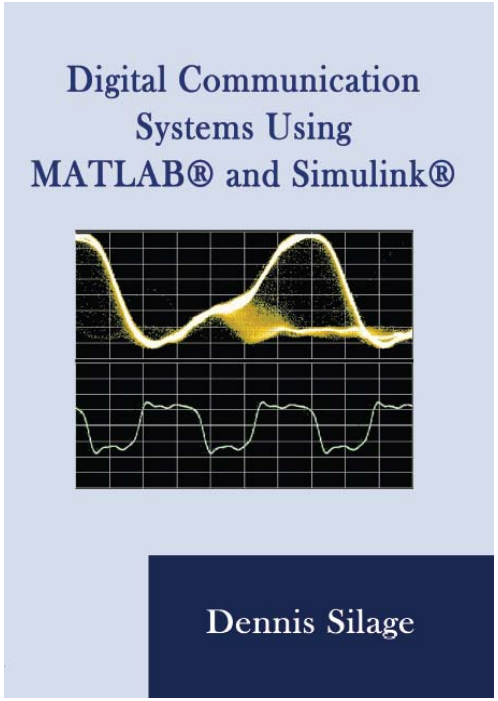
S&M Figure 8-8



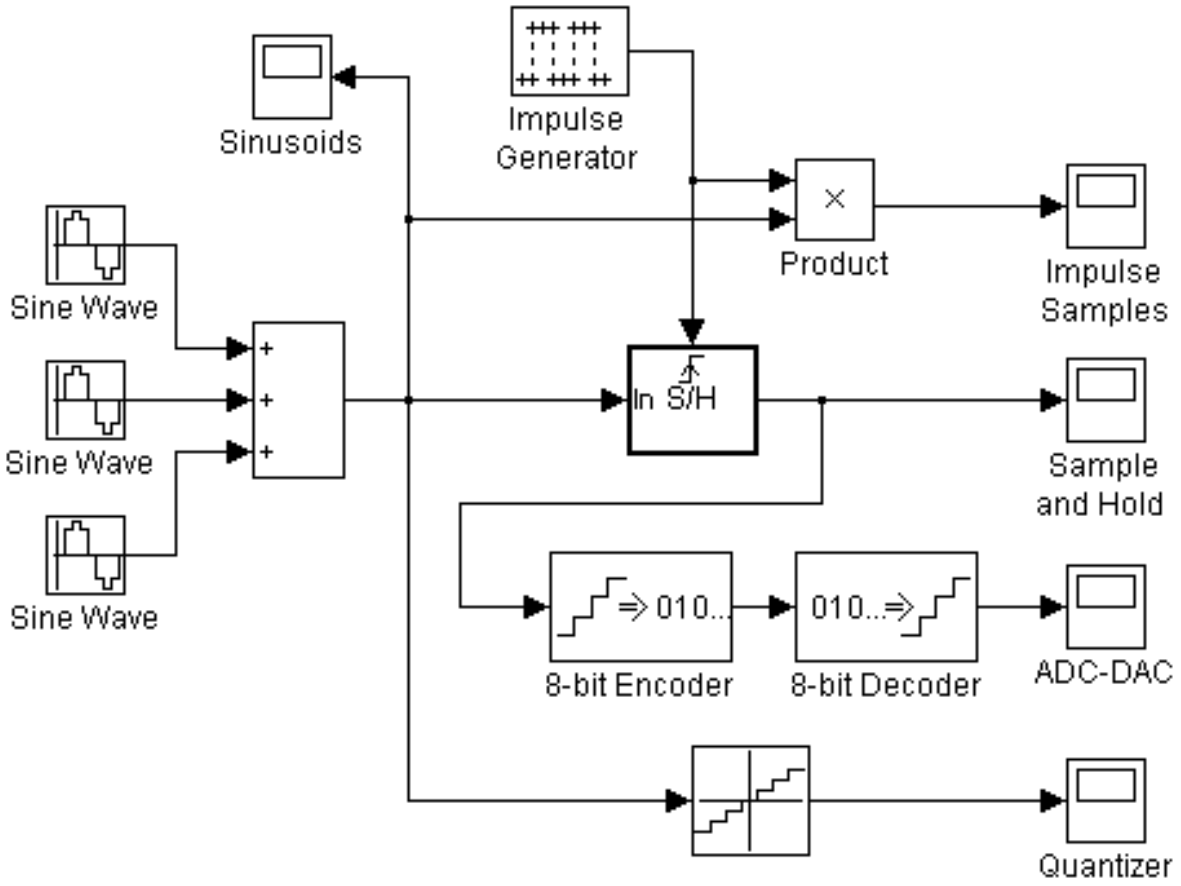
Chapter 8

Analog-to-Digital and Digital-to-Analog Conversion

- *Sampling Baseband Analog Signals*
- Pages 149-182



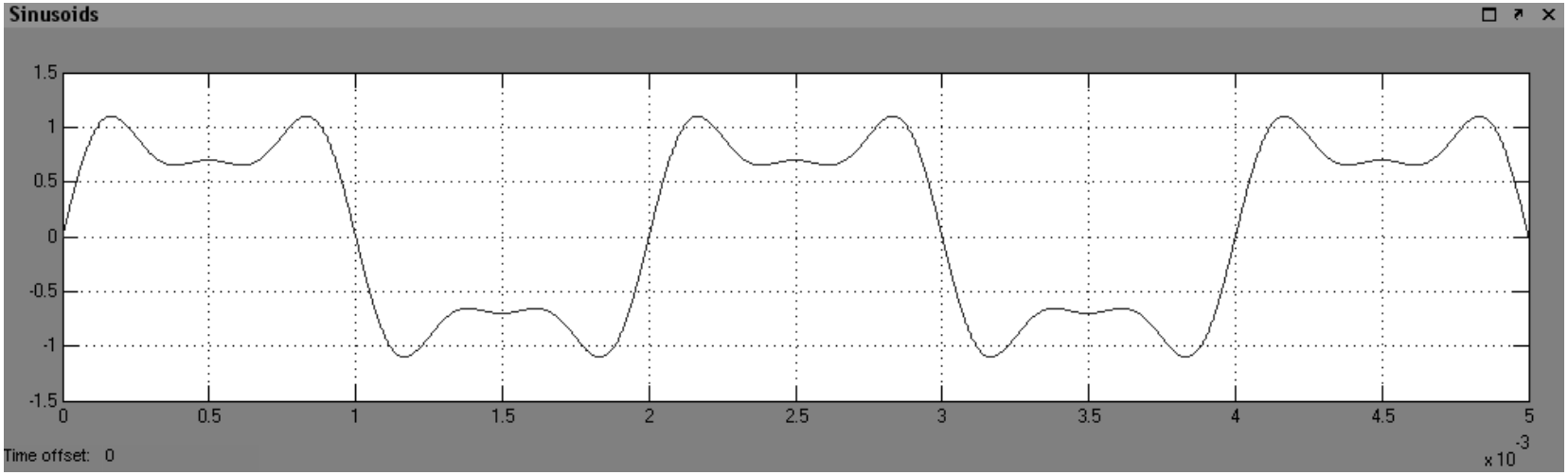
- The periodic baseband signal consisting of three sinusoids is *impulse sampled*, *sampled-and-held*, processed by an 8-bit ADC-DAC and a *quantizer* in *Simulink*.



MS Figure 4.1

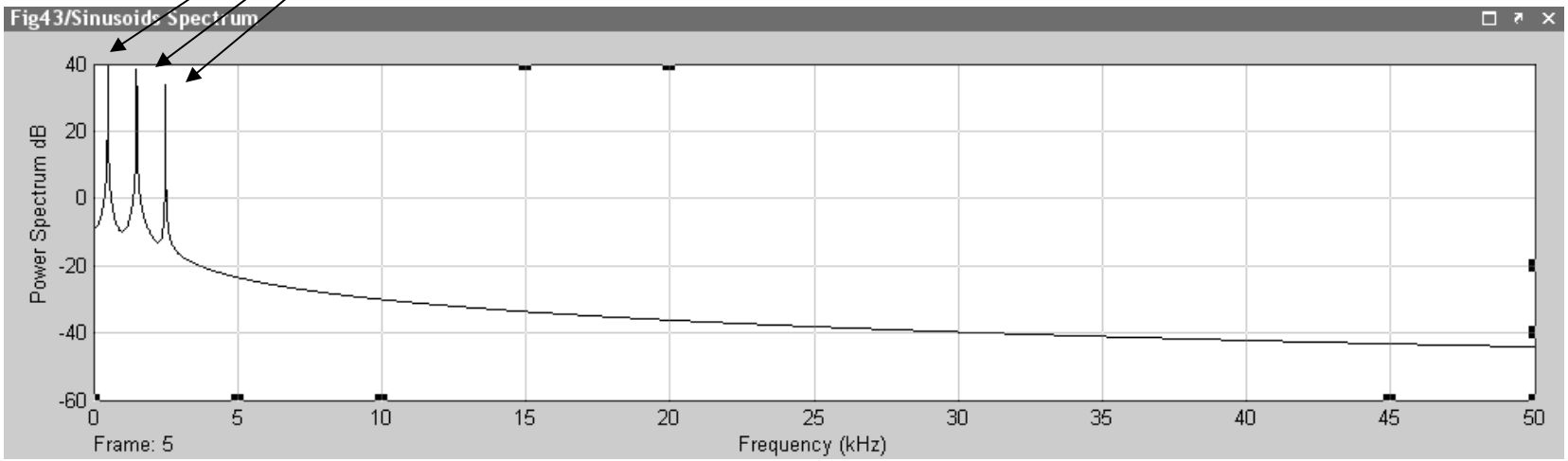
- The periodic baseband signal is the sum of a 1 V 500 Hz, a 0.5 V 1.5 kHz and a 0.2 V 2.5 kHz sinusoid.

MS Figure 4.2



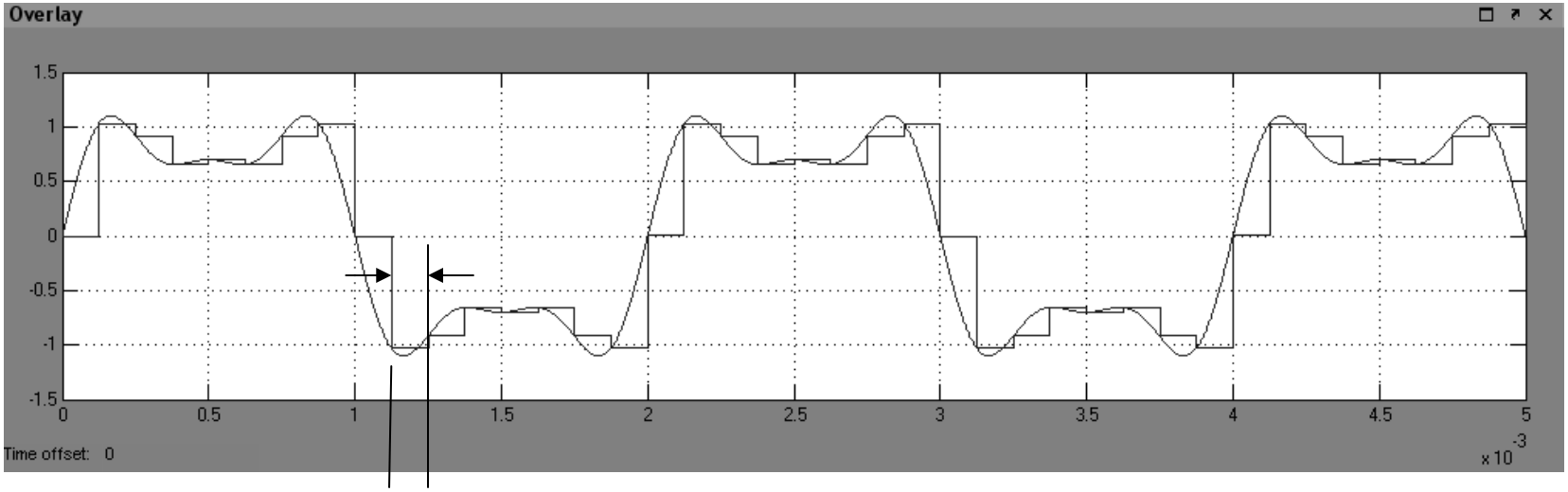
- The power spectral density (PSD) of the periodic baseband signal has the expected peaks at 0.5, 1.5 and 2.5 kHz.

Three sinusoids MS Figure 4.3



- The periodic baseband signal is overlaid with the continuous amplitude sample-and-hold signal with f_S = 8 kHz.

MS Figure 4.4



0.125 msec

- The analog signal x(t) here is sampled and held rather than impulse sampled:

$$y_{s\text{-}h}(t) = \sum_{n} x(nT_S)\ h(t - nT_S) \quad h(t) = 1 \quad 0 \le t \le T_S$$

$$h(t) = 0 \quad \textit{otherwise} \qquad \text{MS Eq. 4.3}$$

The power spectral density ($PSD_{s\text{-}h}$) of the sample and hold operation is:

$$PSD_{s\text{-}h} = f_S^{\,2} \sum_{k=-\infty}^{\infty} |X(f - k f_S)|^2\ T_S^2\ \mathrm{sinc}^2(2\pi f T_S)$$

$$PSD_{s\text{-}h} = \sum_{k=-\infty}^{\infty} |X(f - k f_S)|^2\ \mathrm{sinc}^2(2\pi f T_S)$$

MS Eq. 4.4

- However, if the analog signal x(t) is impulse sampled:

$$x(n T_S) = \sum_n x(t)\,\delta(t - n T_S) \qquad \text{MS Eq. 4.1}$$

Then the power spectral density (PSD) does not have a sinc^2 term:

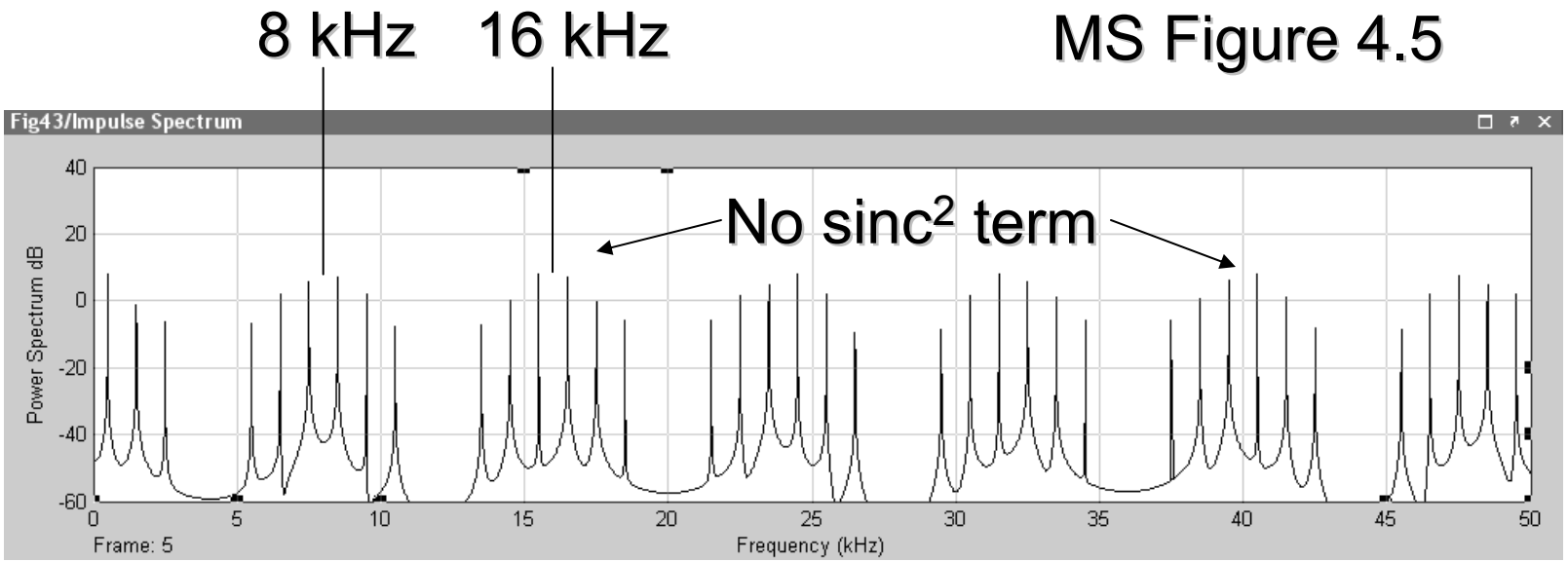
$$\text{PSD} = f_S^{\,2} \sum_{k=-\infty}^{\infty} |X(f - k f_S)|^2 \qquad \text{MS Eq. 4.2}$$

The $\text{PSD}_{\text{s-h}}$ does have the sinc^2 term:

$$\text{PSD}_{\text{s-h}} = \sum_{k=-\infty}^{\infty} |X(f - k f_S)|^2 \,\text{sinc}^2\left(2\pi f T_S\right)$$

MS Eq. 4.4

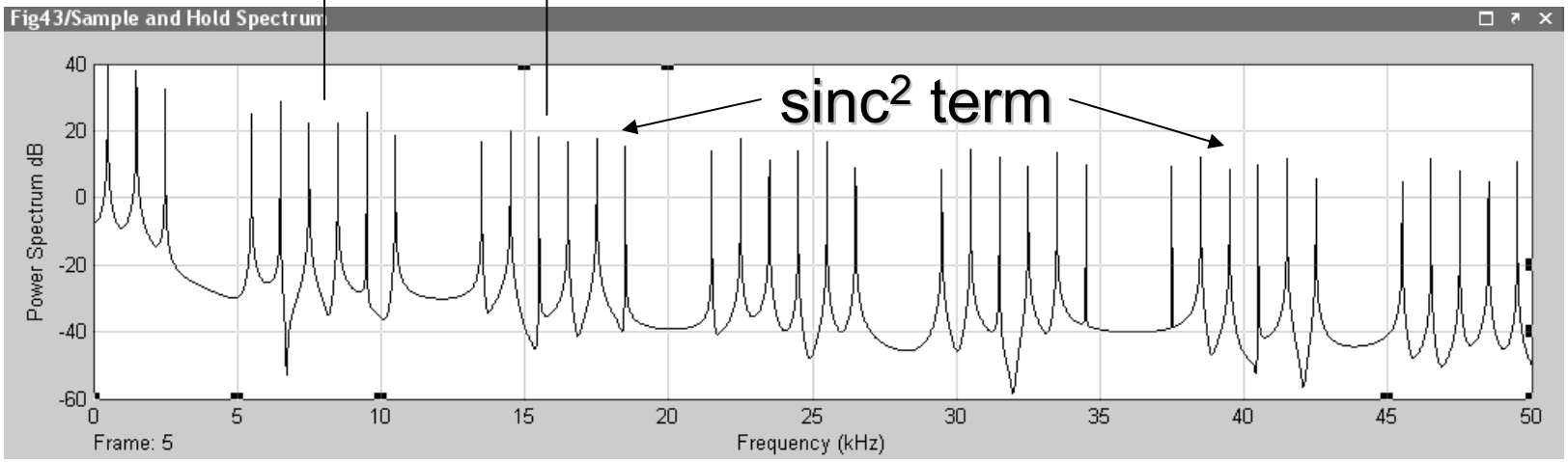
- The PSD of the impulse sampled sum of three sinusoid signal with f_S = 8 kHz is:



$$PSD = f_s^2 \sum_{k=-\infty}^{\infty} |X(f - k f_s)|^2 \qquad \text{MS Eq. 4.2}$$

- The PSD of the continuous amplitude sample and hold sum of three sinusoid signal with f_S = 8 kHz is:

8 kHz 16 kHz MS Figure 4.6



$$PSD_{s\text{-}h} = f_S^2 \sum_{k=-\infty}^{\infty} |X(f - k f_S)|^2 T_S^2 \, \mathrm{sinc}^2(2\pi f T_S)$$

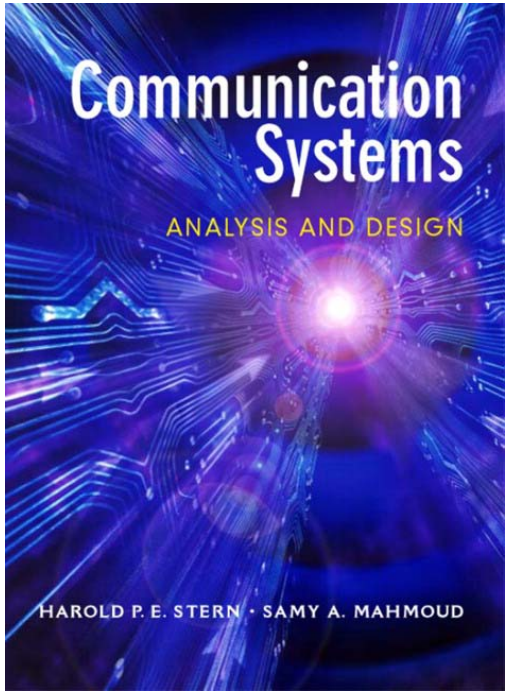
MS Eq. 4.4

$$PSD_{s\text{-}h} = \sum_{k=-\infty}^{\infty} |X(f - k f_S)|^2 \, \mathrm{sinc}^2(2\pi f T_S)$$

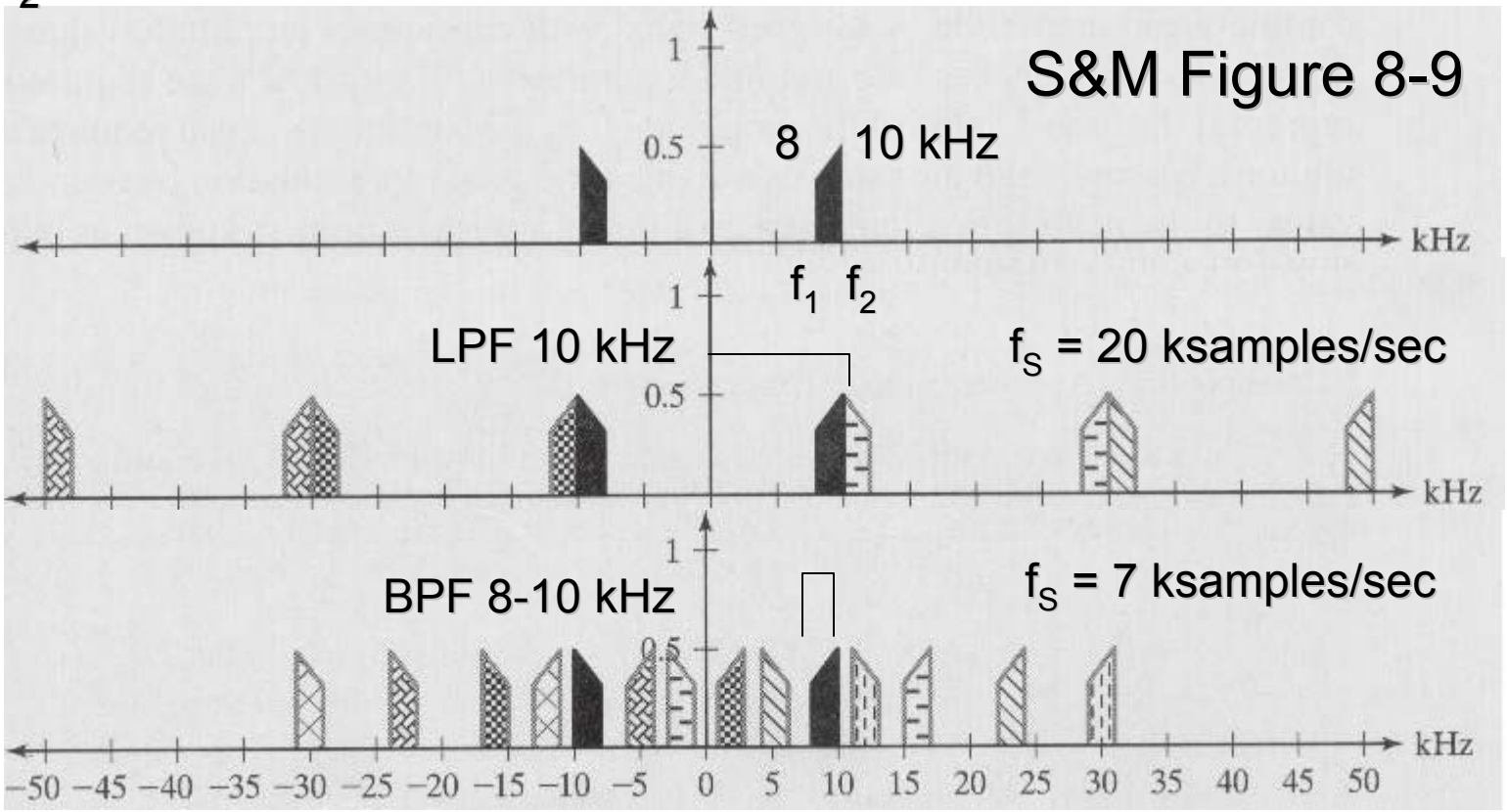
Chapter 8

Analog-to-Digital and Digital-to-Analog Conversion

- *Sampling Bandpass Analog Signals*
- Pages 399-400



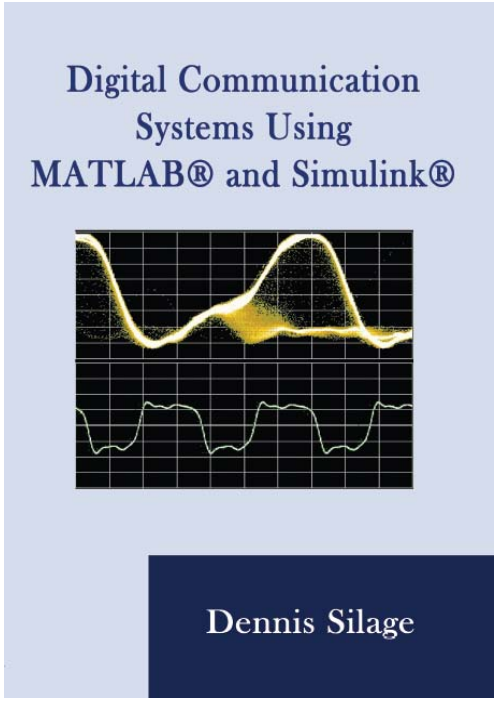
- A bandpass signal does not need to be sampled at 2 f_2. Nyquist's bandpass sampling theory states that the sampling rate $f_S > 2(f_2 - f_1)$ which is substantially less than 2 f_2



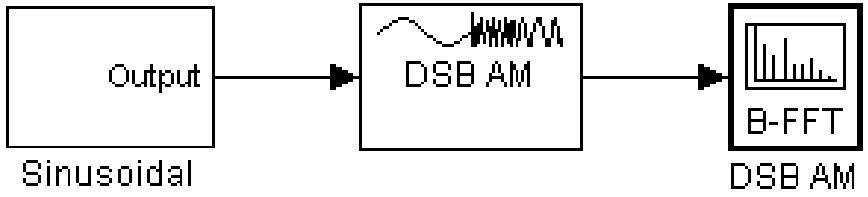
Chapter 8

Analog-to-Digital and Digital-to-Analog Conversion

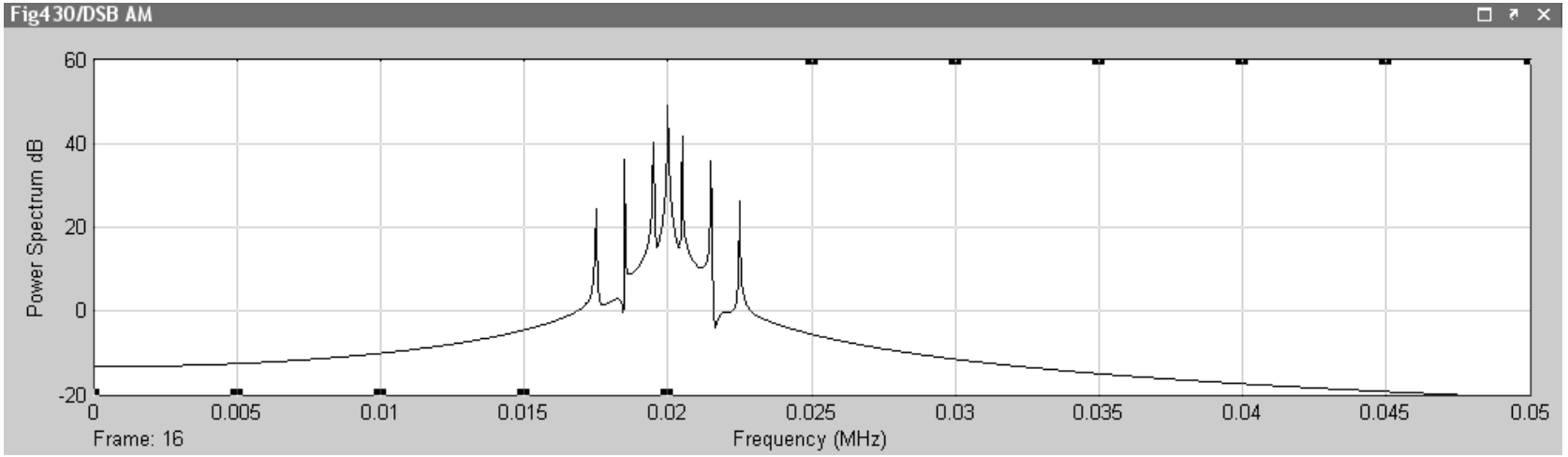
- *Sampling Bandpass Analog Signals*
- Pages 180-181



- The *Simulink* simulation uses the DSB AM modulation block and the sum of three sinusoids source.

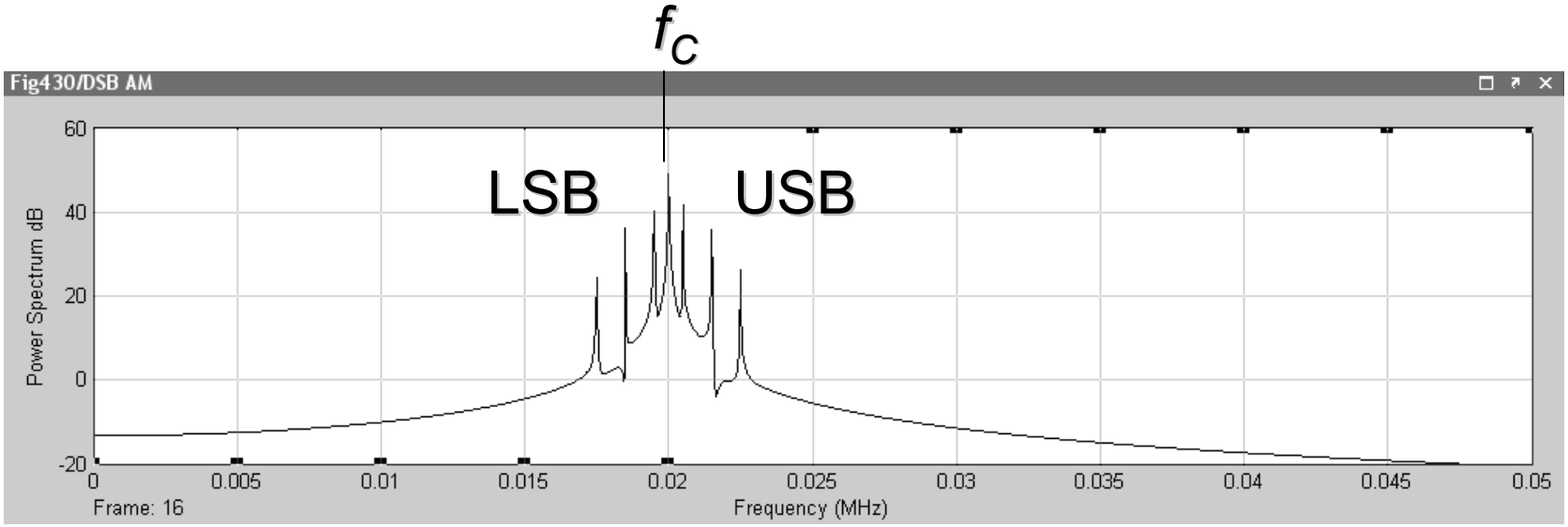


MS Figure 4-32



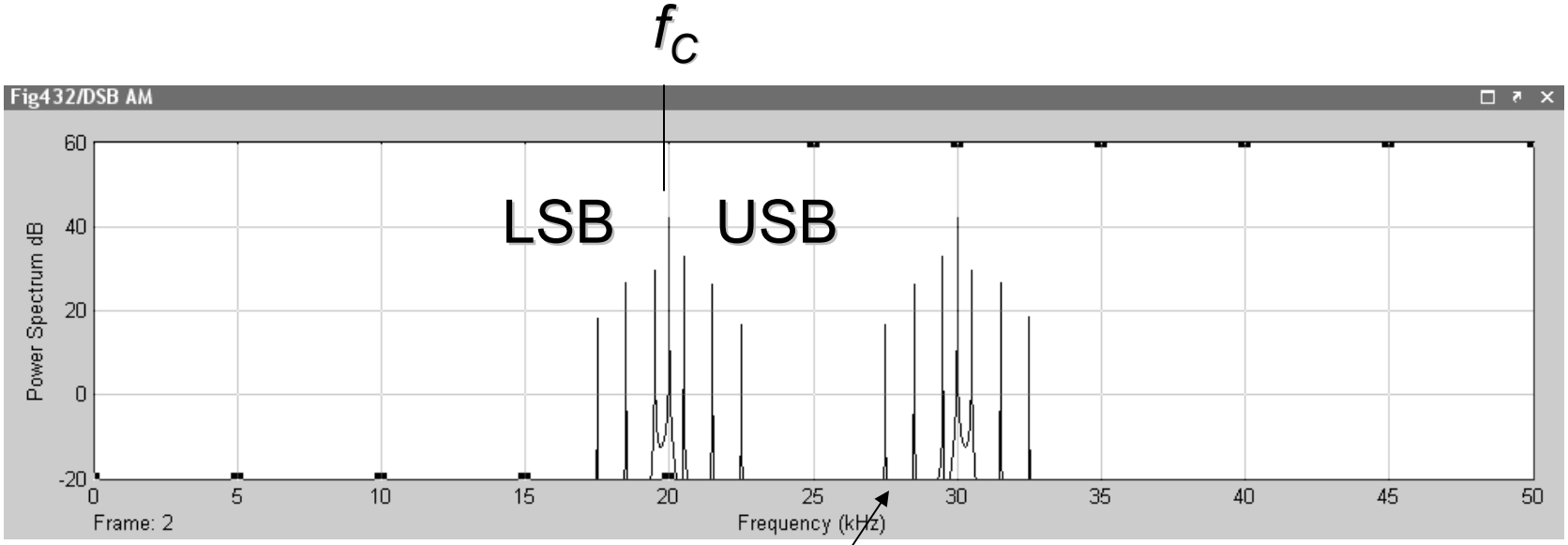
MS Figure 4-33

- The *Simulink* simulation initially uses a sampling rate of 5 MHz and results in 4 194 304 = 2^{22} sampling points. The PSD shows the DSB-LC AM signal with the LSB and USB.



Scaled PSD f_{max} = 50 kHz MS Figure 4-33

- The bandwidth of the bandpass signal is $f_2 - f_1 = 22.5 - 17.5 = 5$ kHz and the *Simulink* sampling rate is set to 50 kHz and results in only 32 768 = 2^{15} sampling points.

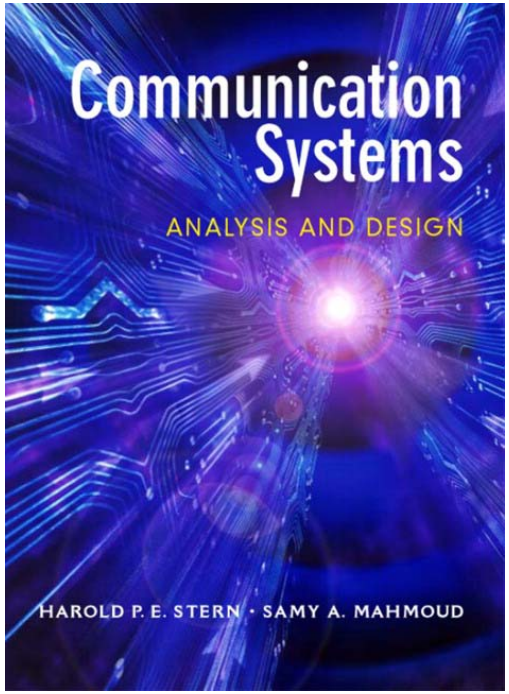


Scaled PSD f_{max} = 50 kHz MS Figure 4-34

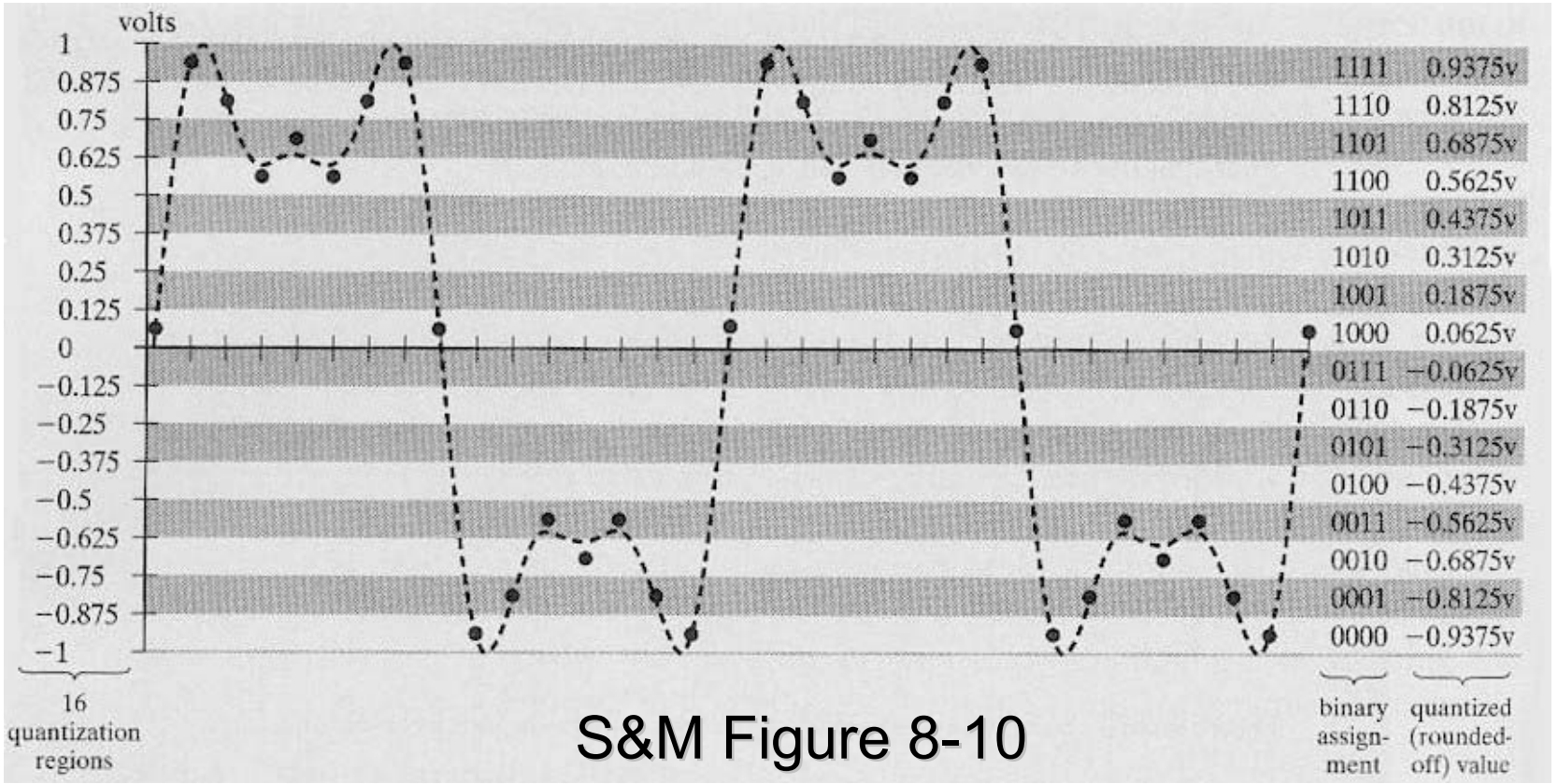
Chapter 8

Analog-to-Digital and Digital-to-Analog Conversion

- *Quantizing Process: Uniform Quantization*
- Pages 400-404



- The *quantizing process* divides the *range* (± full scale) into 2^n (n = 4 here) regions which are assigned an n-bit binary code.



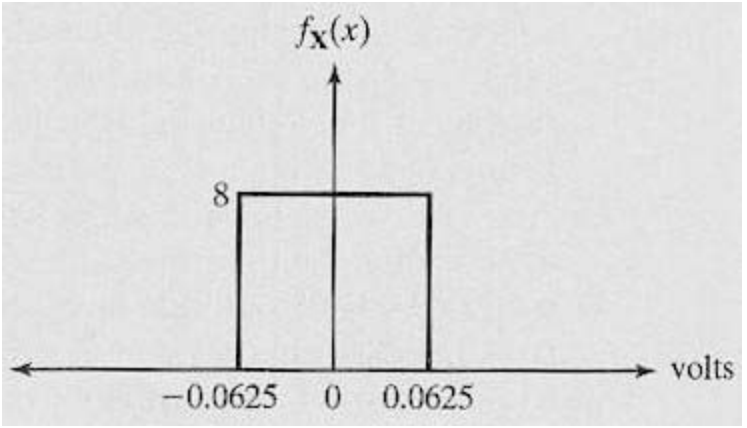
S&M Figure 8-10

- The *error* associated with the quantizing process is assumed to have a uniform probability density function. The maximum error for uniform quantization is:

$$q = \pm 0.5\left(\frac{2\,V_{max}}{2^n}\right) = \pm\frac{V_{max}}{2^n}$$

The quantizer range is ± V_{max} and the uniform quantizer voltage step size is:

$$\Delta = \frac{2\,V_{max}}{2^n} = \frac{V_{max}}{2^{n-1}}$$ MS Eq. 4.6



S&M Figure 8-11

The mean square quantizing E_q is the normalized quantizing noise power:

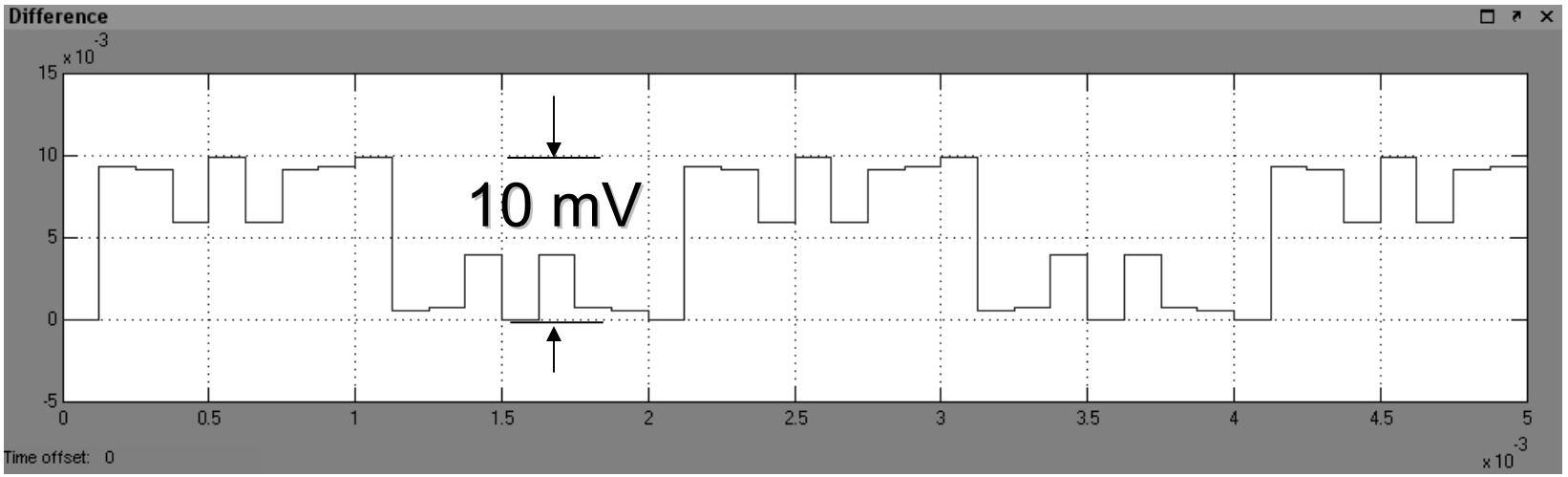
$$E_q = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} q^2\,dq = \frac{\Delta^2}{12} = \frac{V_{max}^2}{3\left(2^n\right)^2} = \frac{V_{max}^2}{3\left(2^{2n}\right)}$$ MS Eq. 4.7

- The *signal to quantizing noise power* (SNR_q) is:

$$SNR_q = \frac{12 P_S}{\Delta^2} = 3\left(2^{2n}\right)\frac{P_S}{V_{max}^2} \qquad \text{MS Eq. 4.8}$$

P_S is the normalized power of the signal that is quantized.

For the ADC here Δ = 10 mV and n = 8. The sum of three sinusoids as the input signal has a peak amplitude of 1.1 V and the quantizing noise has a peak amplitude of 10 mV.

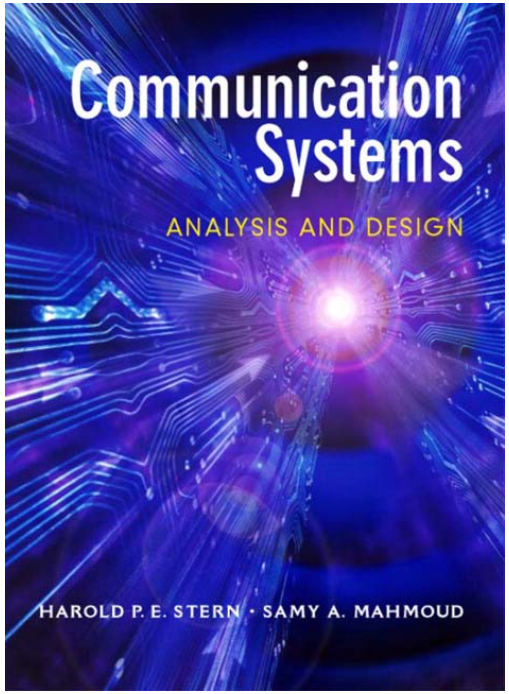


MS Figure 4.7

Chapter 8

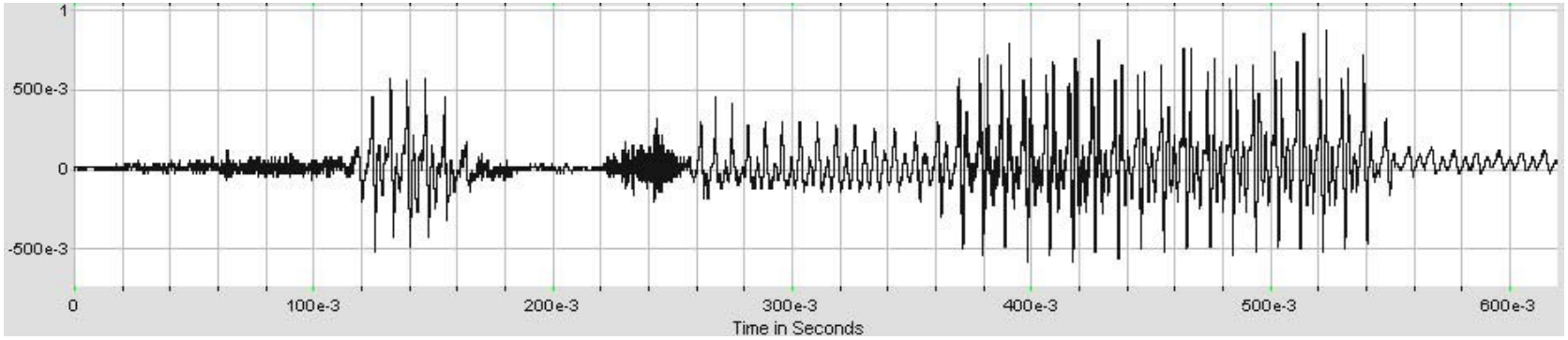
Analog-to-Digital and Digital-to-Analog Conversion

- *Quantizing Process: Nonuniform Quantization*
- Pages 400-404



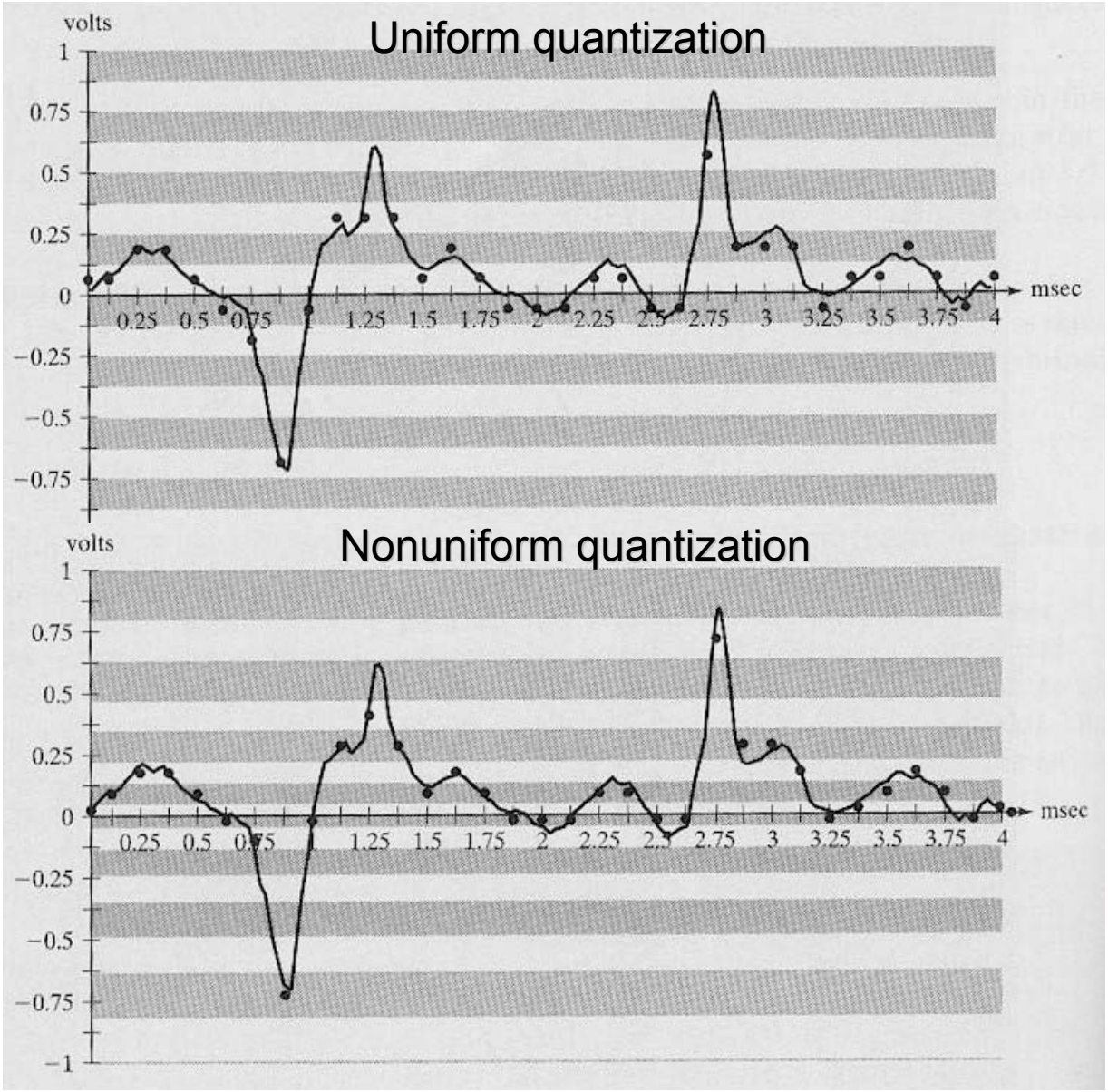
- Nonuniform quantization divides the dynamic range of an analog signal into nonuniform quantization regions. Lower magnitudes have smaller quantization regions than high magnitudes.

  The quantization of speech benefits from nonuniform quantization since the perception of hearing is *logarithmical* rather than linear.



- Uniform quantization (top) results in a large amount of error for small sample amplitude.

  Non-uniform quantization (bottom) reduces the error for small sample amplitudes.

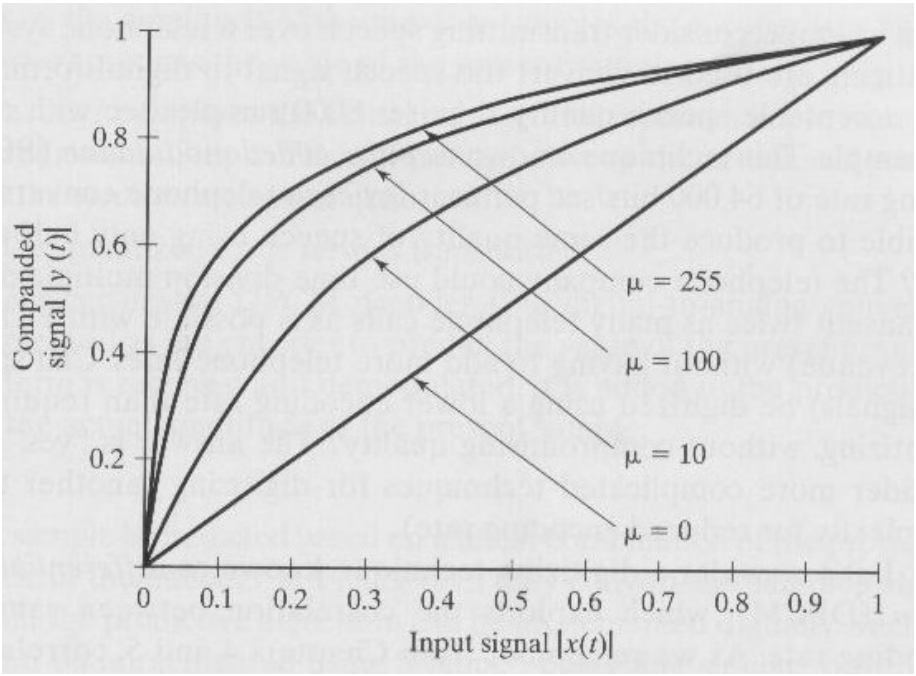


- Uniform quantization is simpler to implement so a *compressor* (a non-linear transfer function) is used before the quantizer.

The *μ-Law compressor* is used in telephony with μ = 255. At the receiver an expander has the inverse non-linear transfer function and results in *companding* (COMpressing and exPANDING).

$$\left|V_{out}\right| = \frac{\ln\left(1+\mu\left|\frac{V_{in}}{V_{max}}\right|\right)}{\ln(1+\mu)}\left|V_{max}\right| \quad 0 \le \left|\frac{V_{in}}{V_{max}}\right| \le 1$$

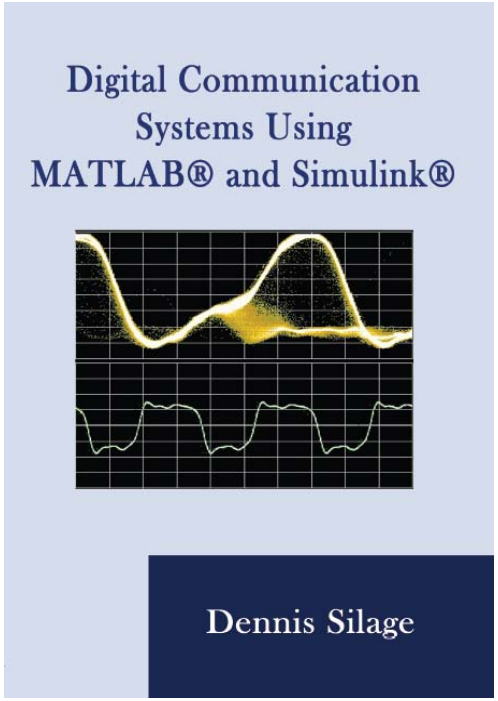
MS Eq. 4.9



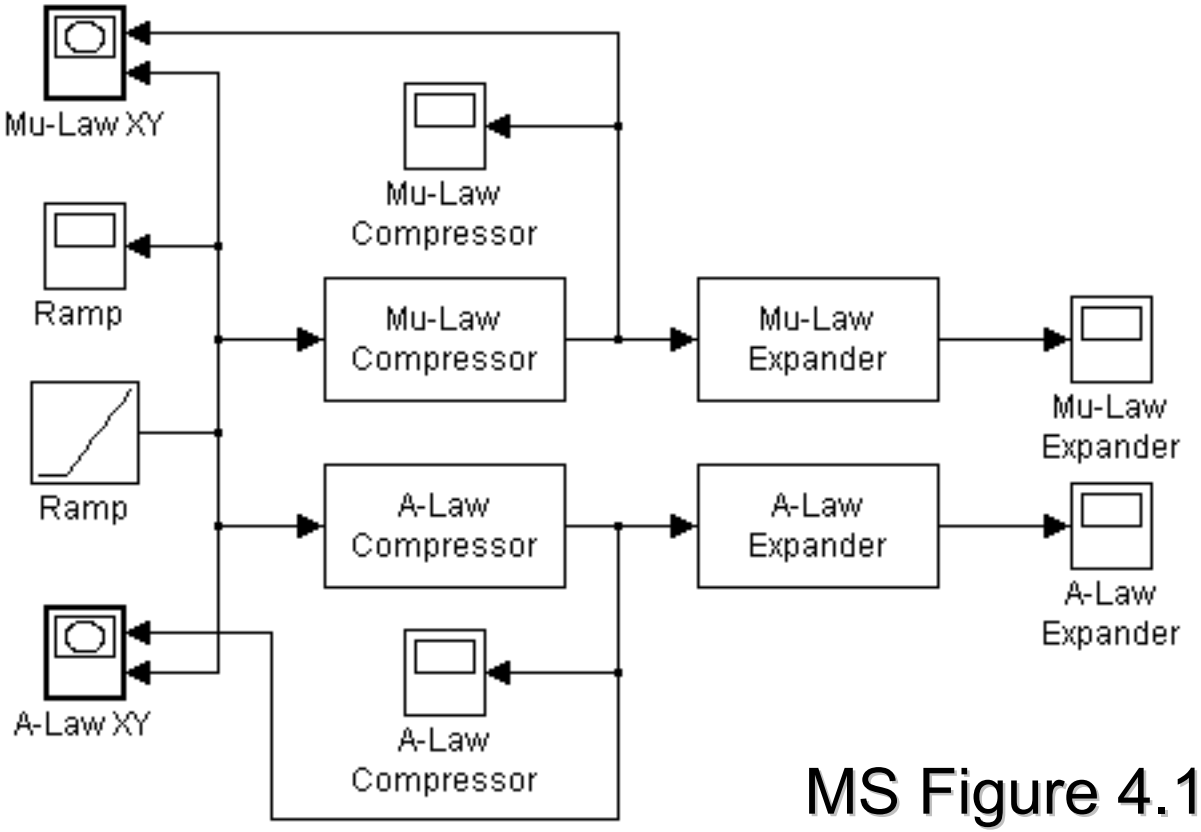
Chapter 8

Analog-to-Digital and Digital-to-Analog Conversion

- *Companding*
- Pages 157-159

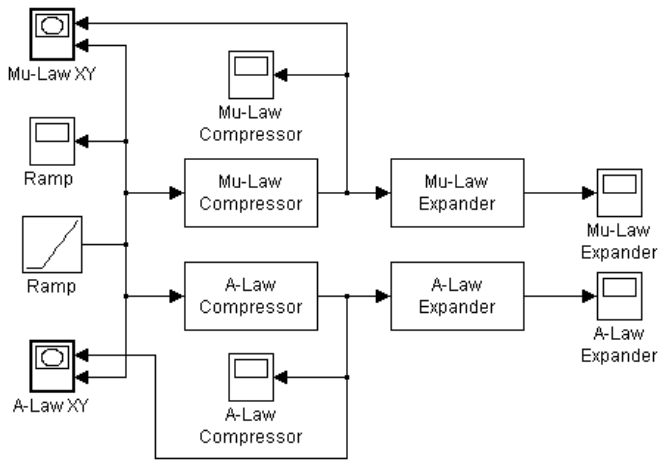


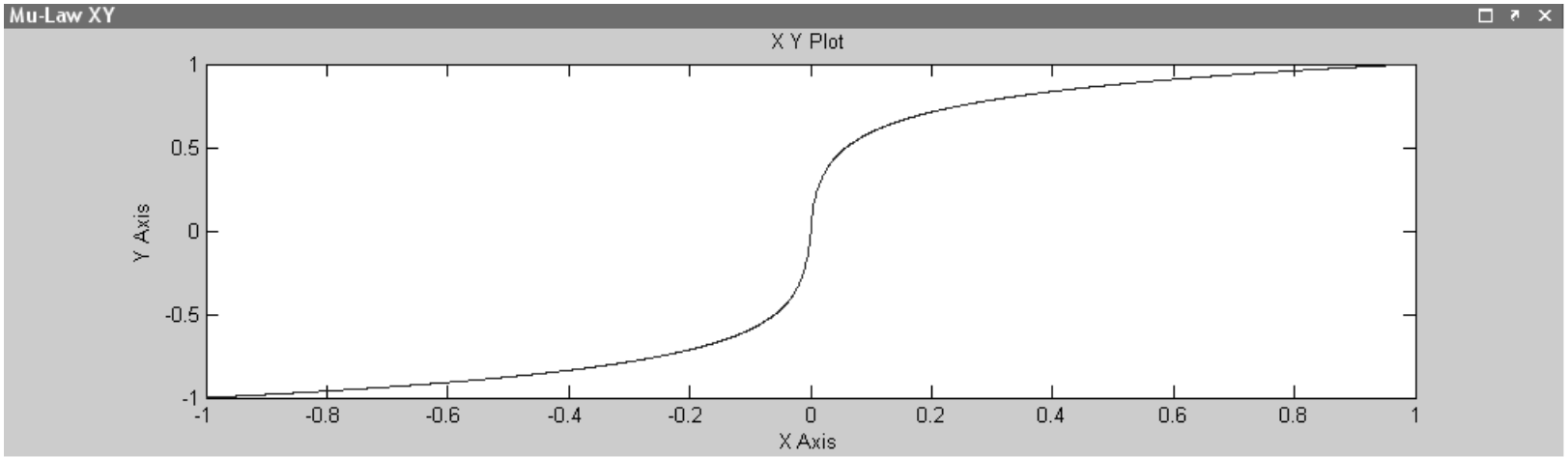
- The μ-Law compander concept can be simulated in *Simulink* with the μ-Law Compressor and μ-Law Expander blocks. The A-Law Compressor and A-Law Expander blocks are included for comparison.



MS Figure 4.13

- The μ-Law compressor voltage transfer function is *sigmoidal* (S-shaped).



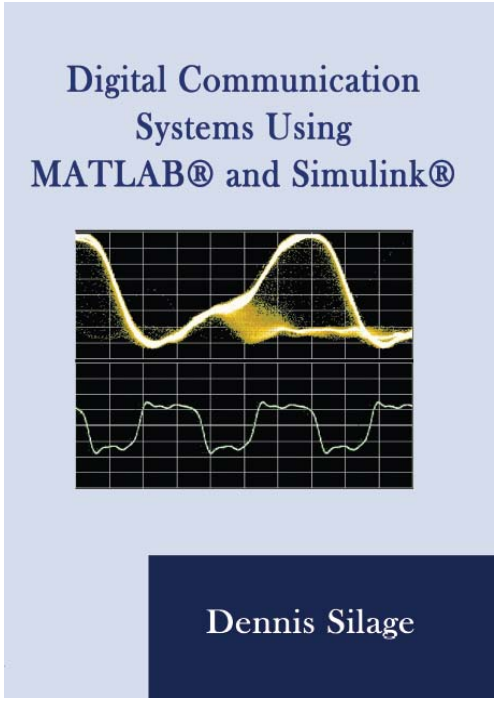


MS Figure 4.14

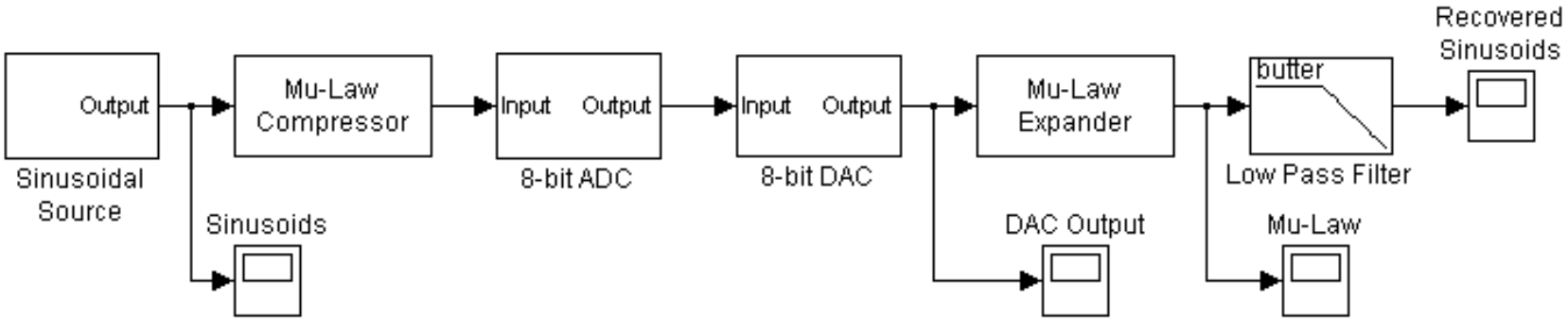
Chapter 8

Analog-to-Digital and Digital-to-Analog Conversion

- *Pulse Code Modulation*
- Pages 171-175

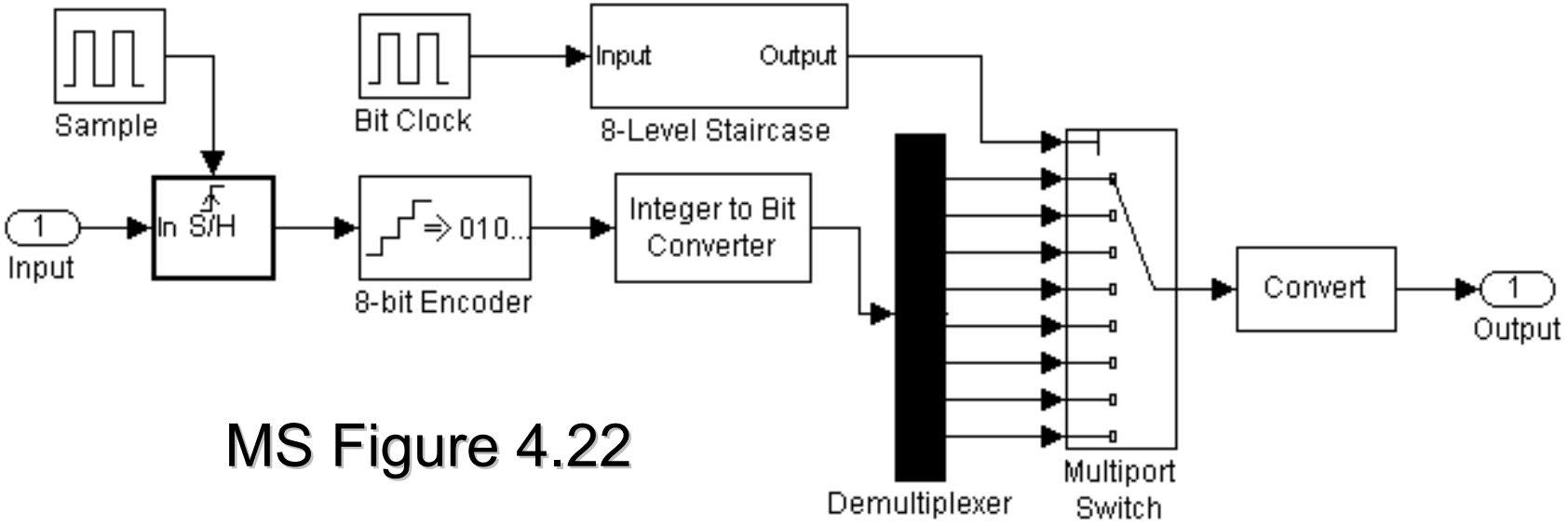


- The pulse code modulator (PCM) transmitter utilizes a *Simulink* μ-Law compressor block, an 8-bit ADC subsystem, an 8-bit DAC subsystem and a μ-Law expander block.



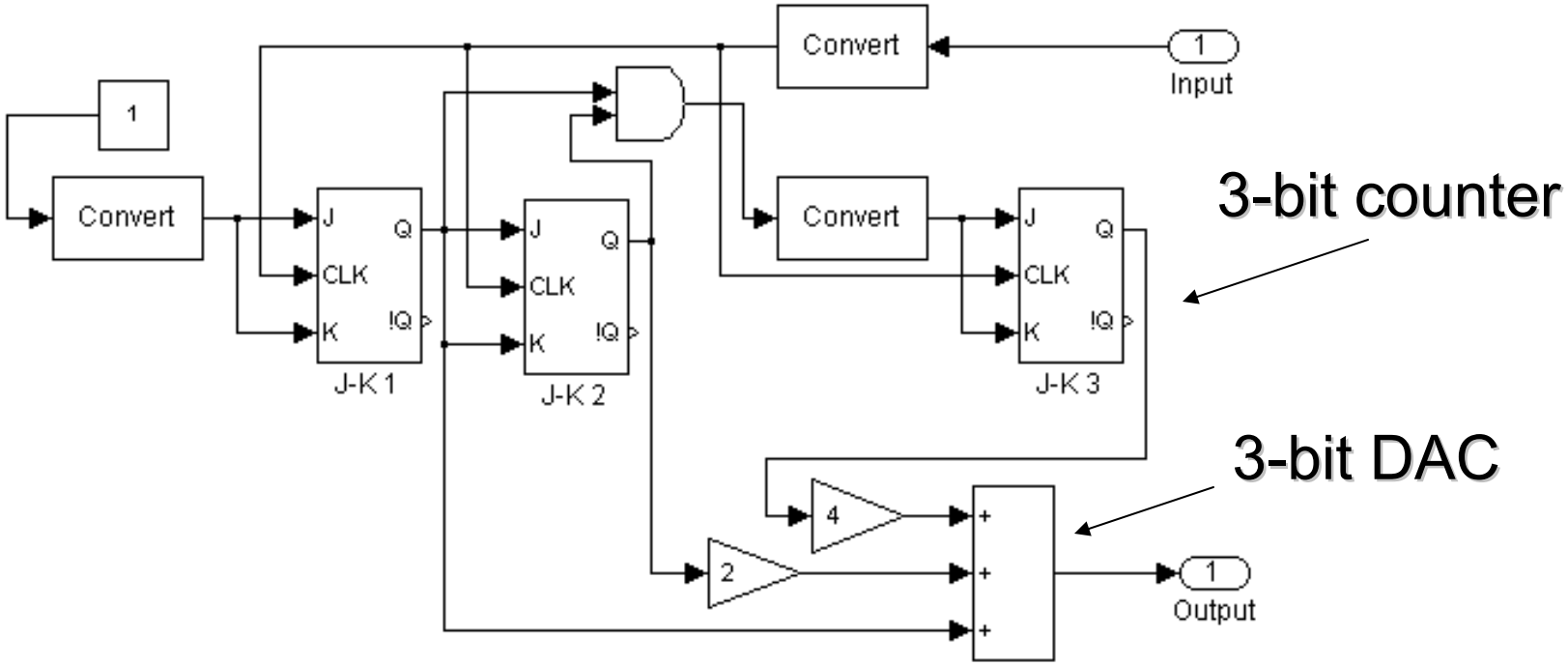
MS Figure 4.21

- The *Simulink* 8-bit ADC subsystem has a sample-and-hold block controlled by a *sampling* pulse generator, an 8-bit encoder block, an integer-to-bit converter block which provides an 8-bit *vector* to a demultiplexer block and a multiport switch. An 8-level *staircase* subsystem sequences the multiport switch to select 1 of the 8 inputs for bit serial output.



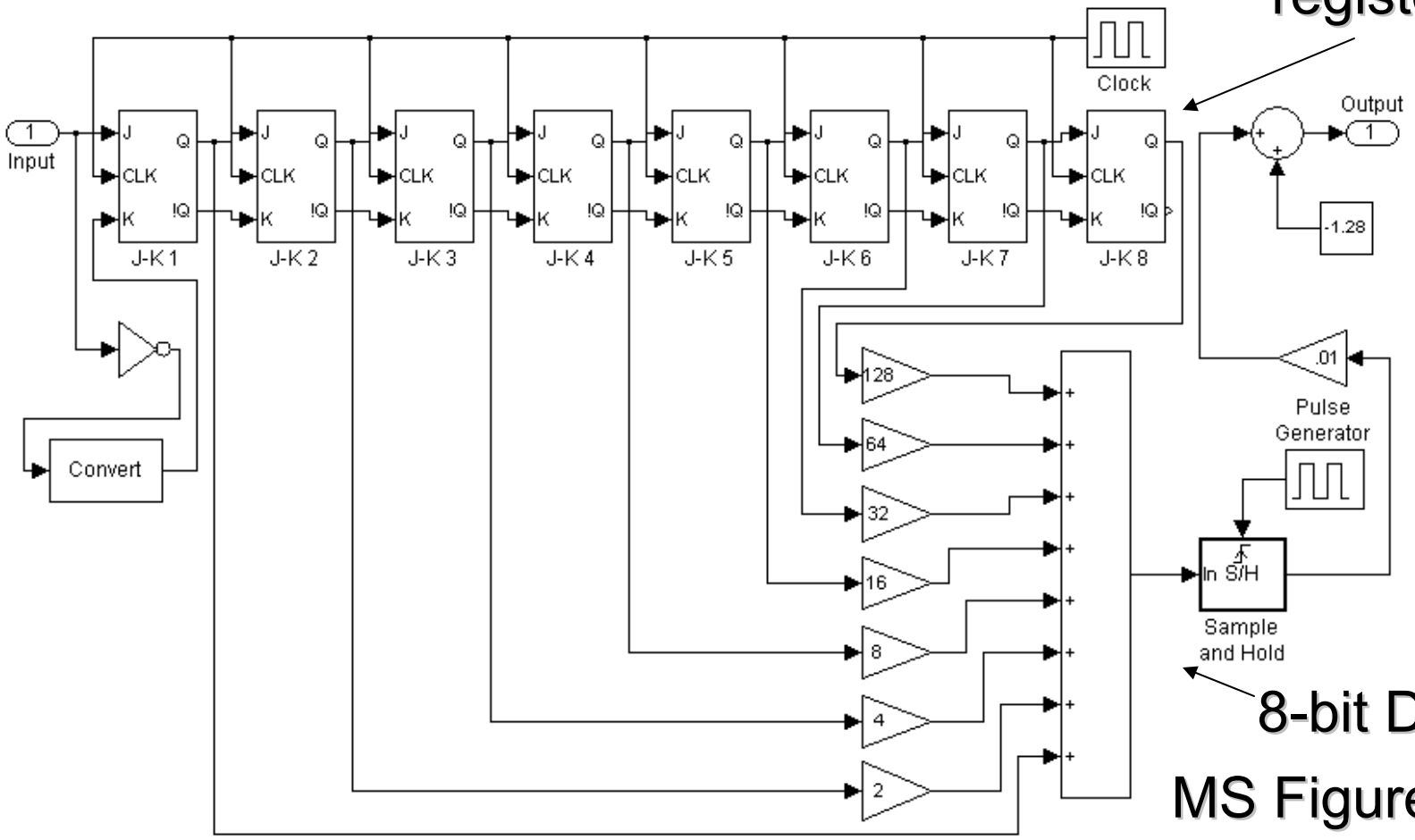
MS Figure 4.22

- The 8-level *staircase Simulink* subsystem sequences the multiport switch with a 3-bit counter and a 3-bit DAC for the output.



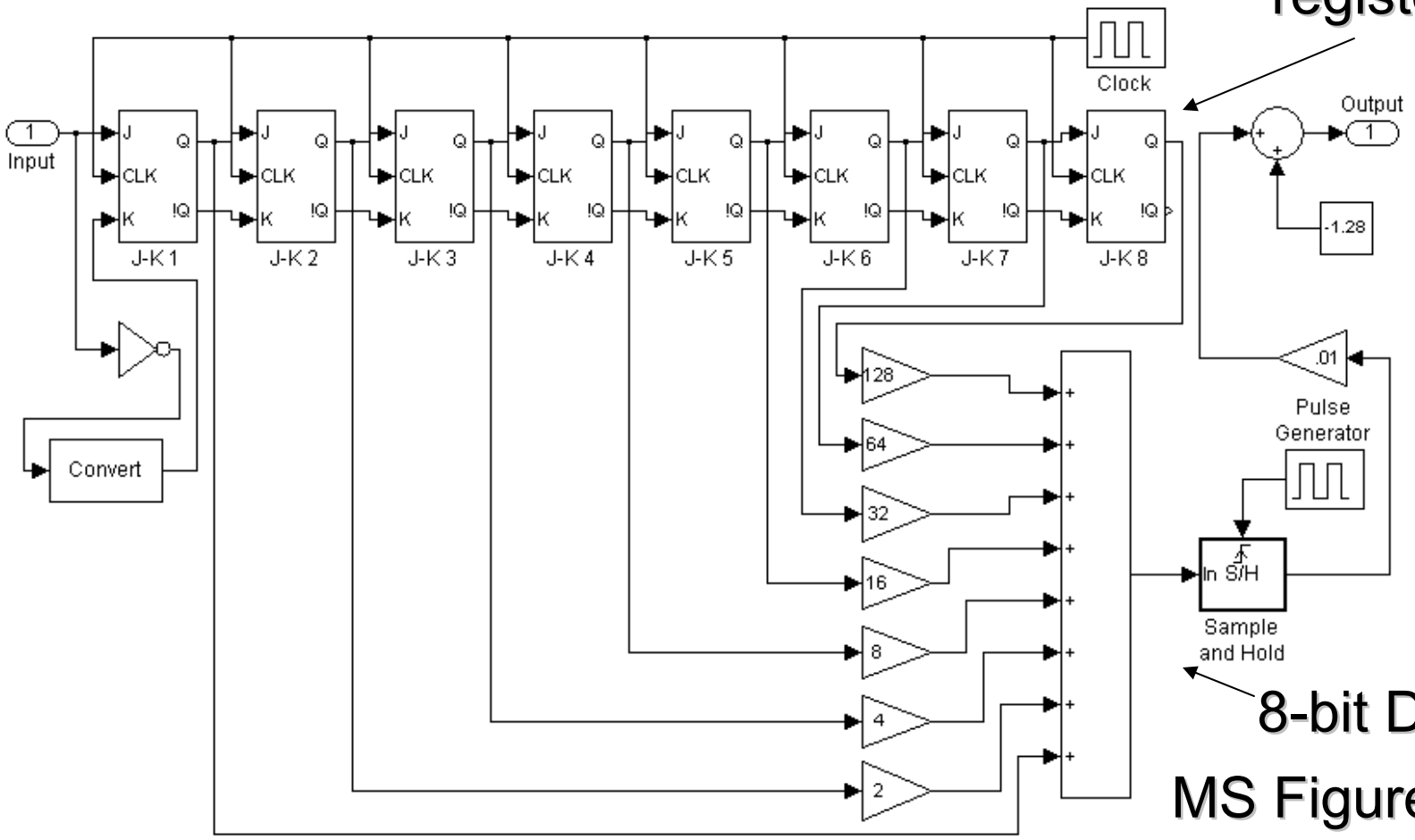
MS Figure 4.22

- The 8-bit DAC *Simulink* subsystem for the PCM system uses a 8-bit *shift register* and an 8-bit DAC.



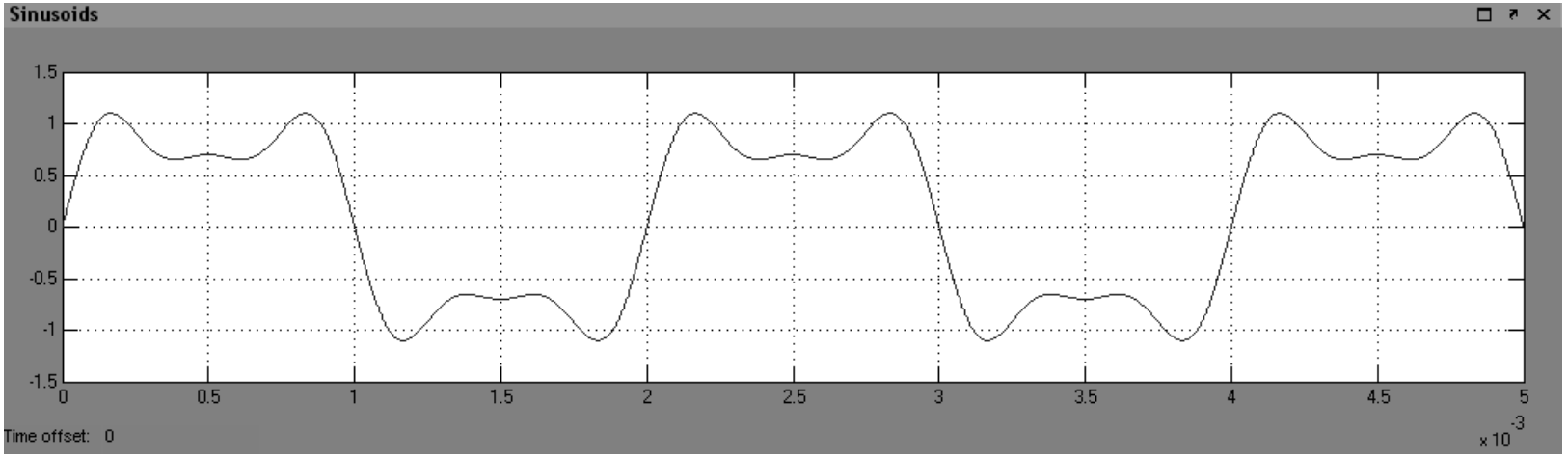
MS Figure 4.24

- The 8-bit DAC *Simulink* subsystem for the PCM system uses a 8-bit *shift register* and an 8-bit DAC.

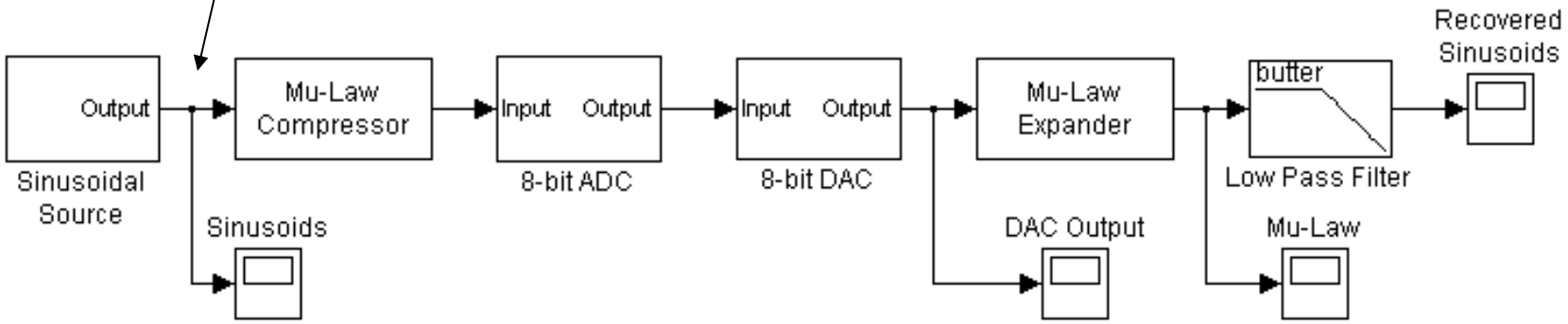


MS Figure 4.24

- Analog input signal to the PCM system

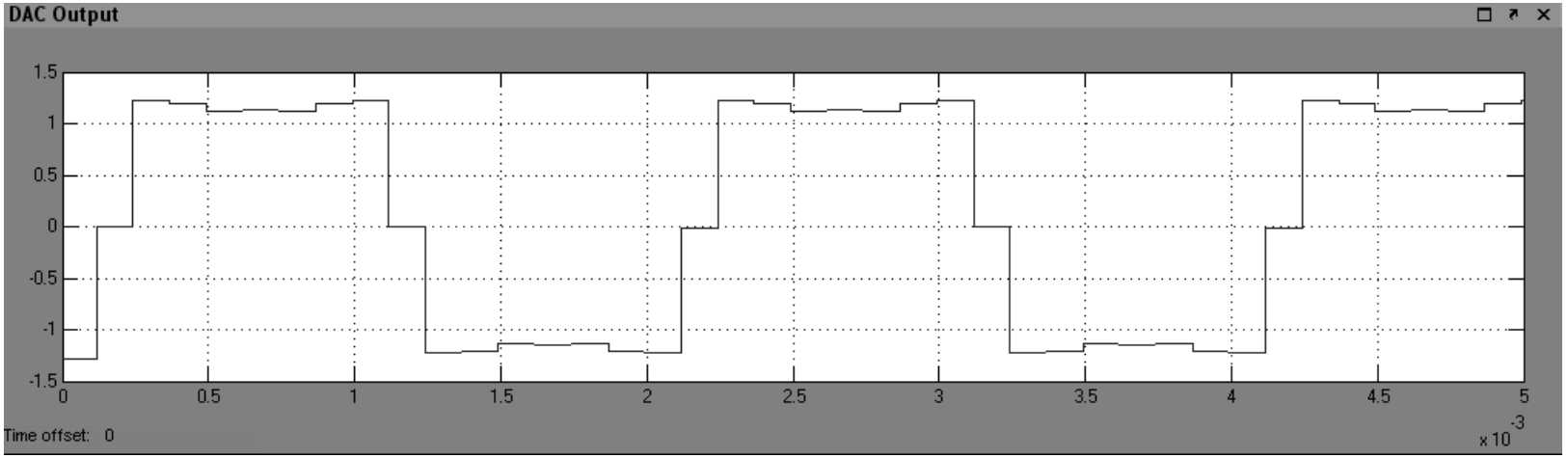


MS Figure 4.25

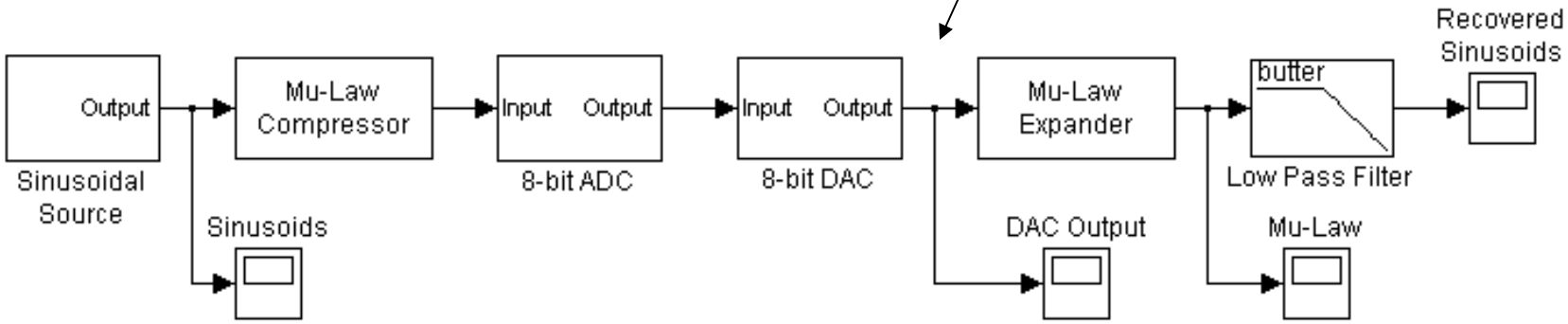


MS Figure 4.21

- 8-bit DAC output after 8-bit ADC and μ-Law Compressor

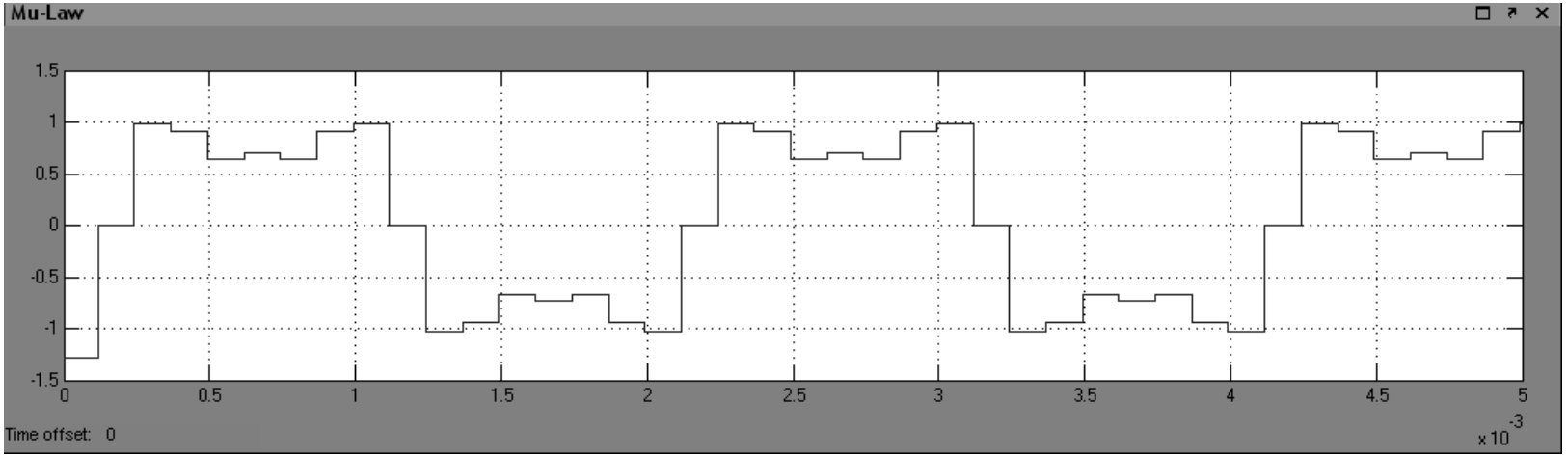


MS Figure 4.25

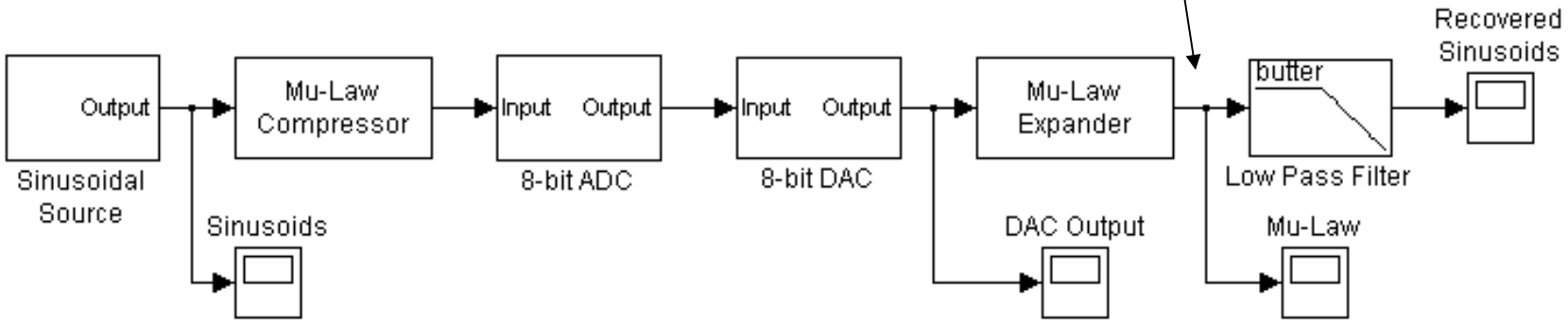


MS Figure 4.21

- μ-Law Expander block output of the PCM system

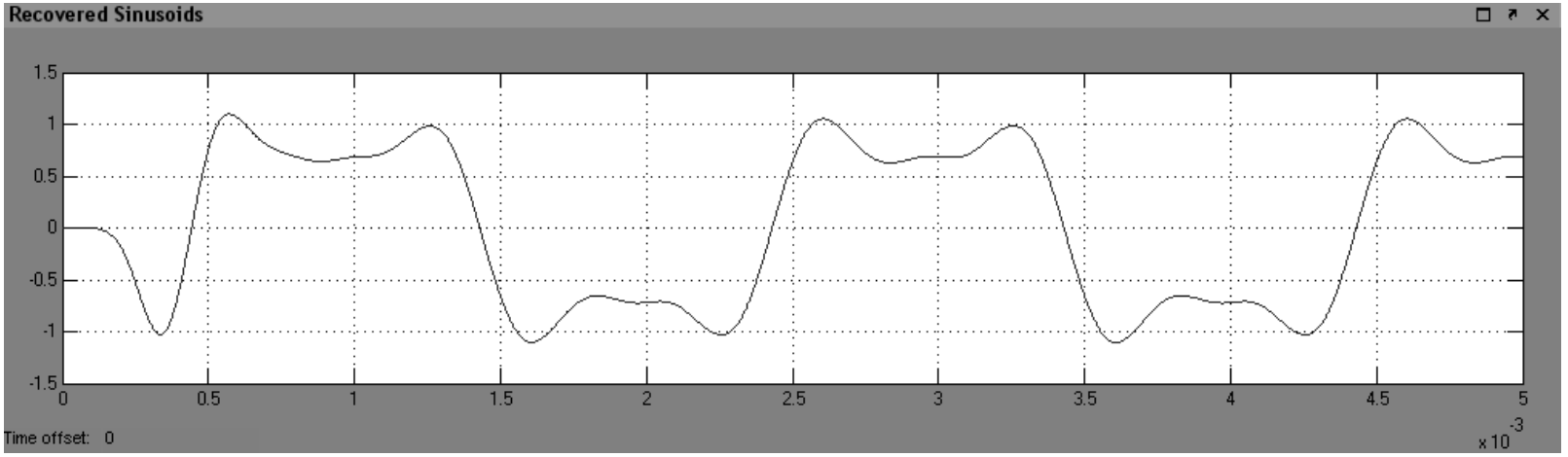


MS Figure 4.25

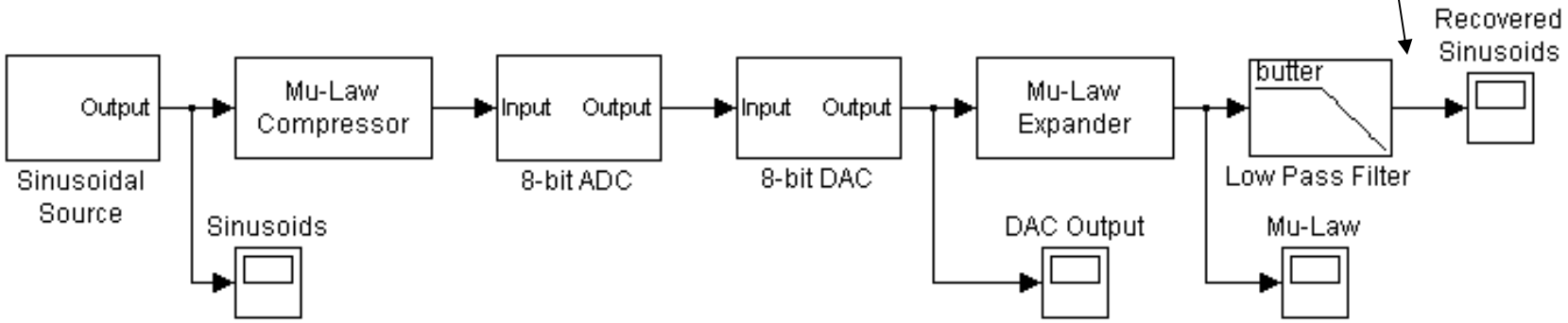


MS Figure 4.21

- LPF output of the PCM system

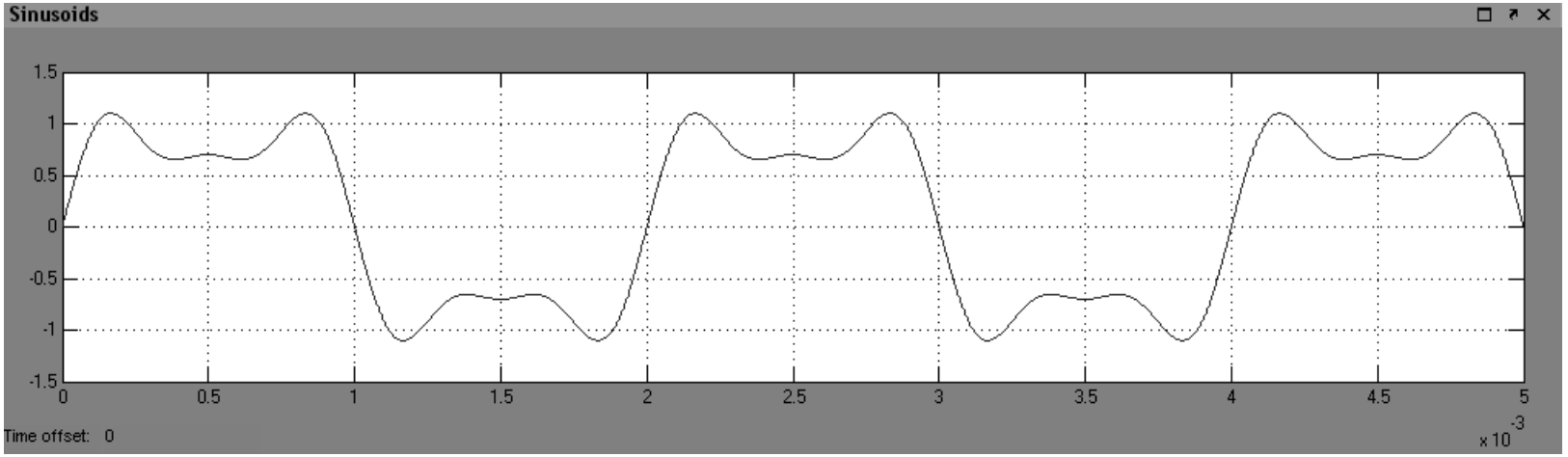


MS Figure 4.25

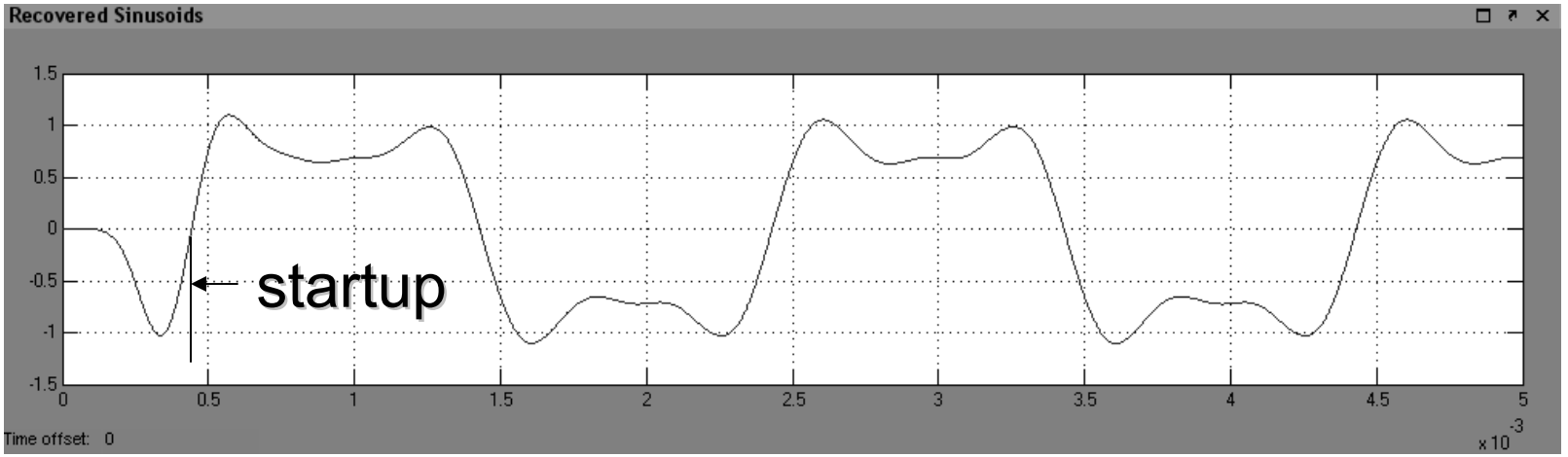


MS Figure 4.21

- Analog input signal to the PCM system



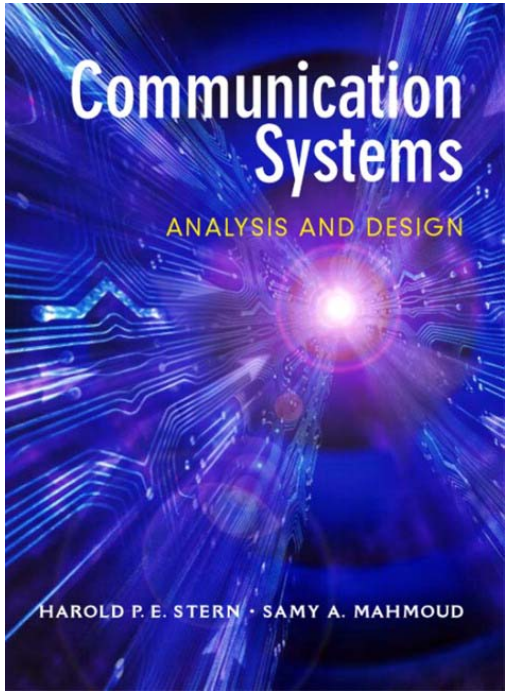
- LPF output of the PCM system MS Figure 4.25



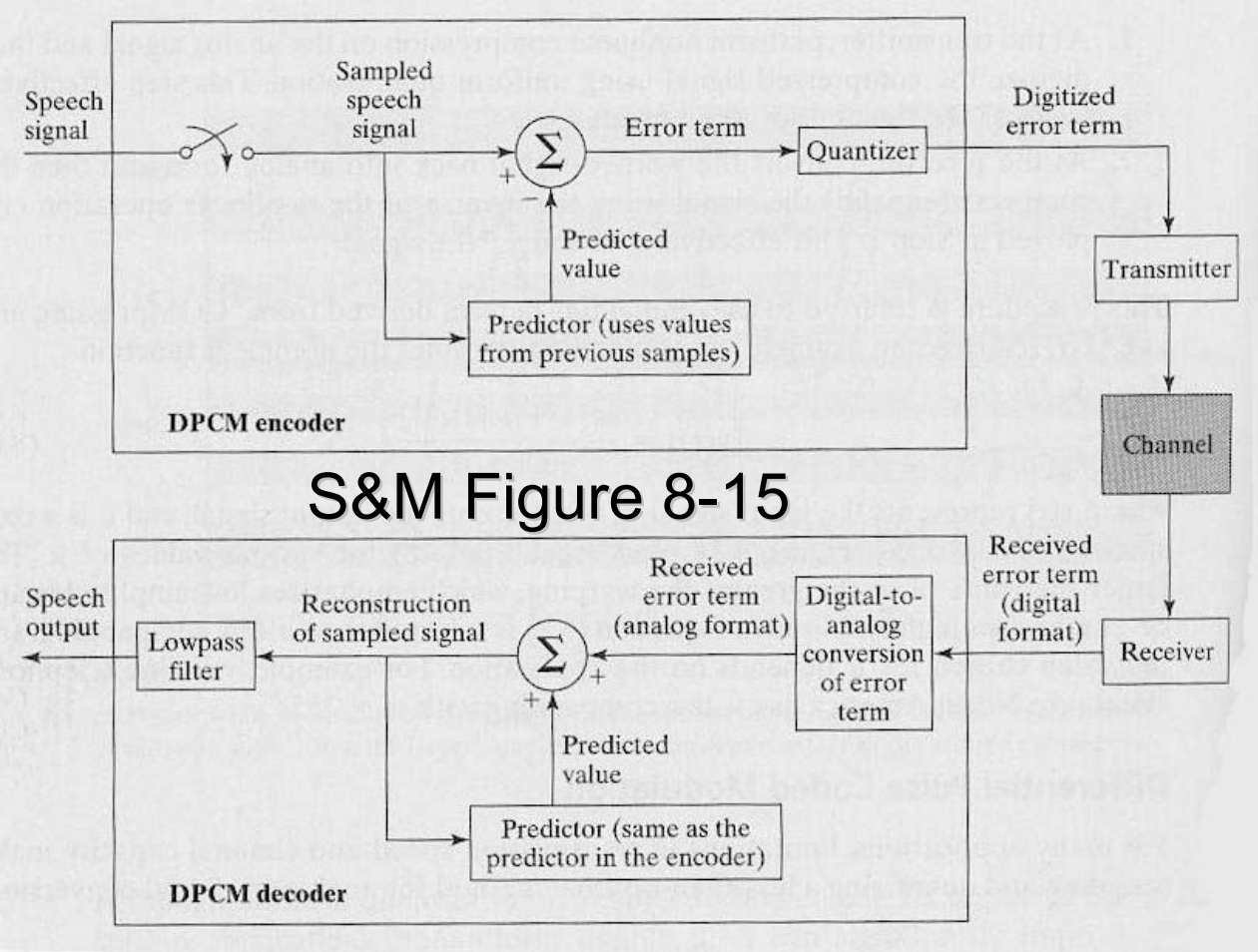
Chapter 8

Analog-to-Digital and Digital-to-Analog Conversion

- *Differential Pulse Code Modulation*
- Pages 407-411



- Sampled speech data are *highly correlated* and *differential pulse code modulation* (DPCM) exploits this to lower the overall data rate. DPCM uses a *predictor* to subtract a predicted value from the input. The *error difference* is sent.

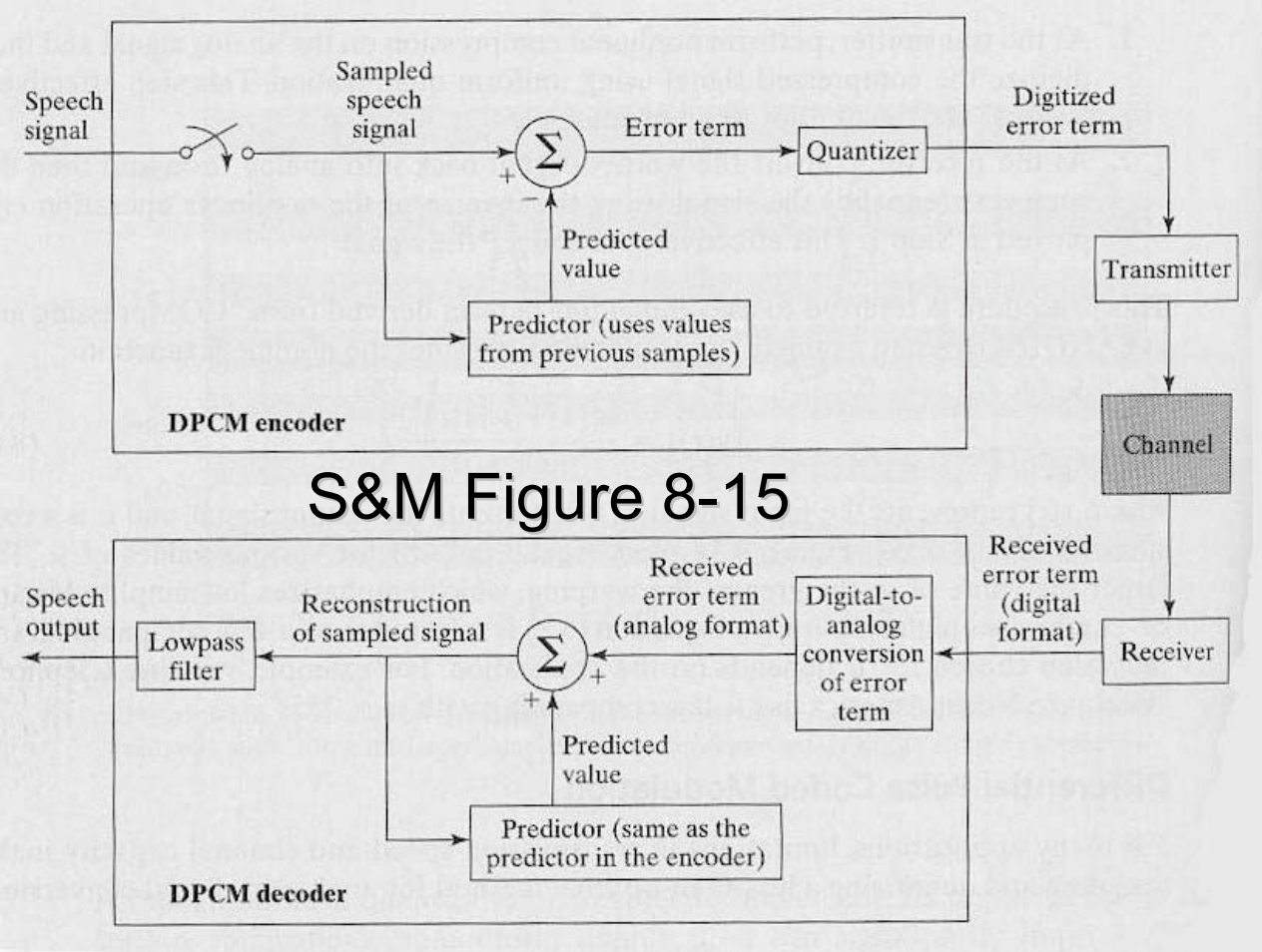


S&M Figure 8-15

- The predictor is a recursive equation, for example:

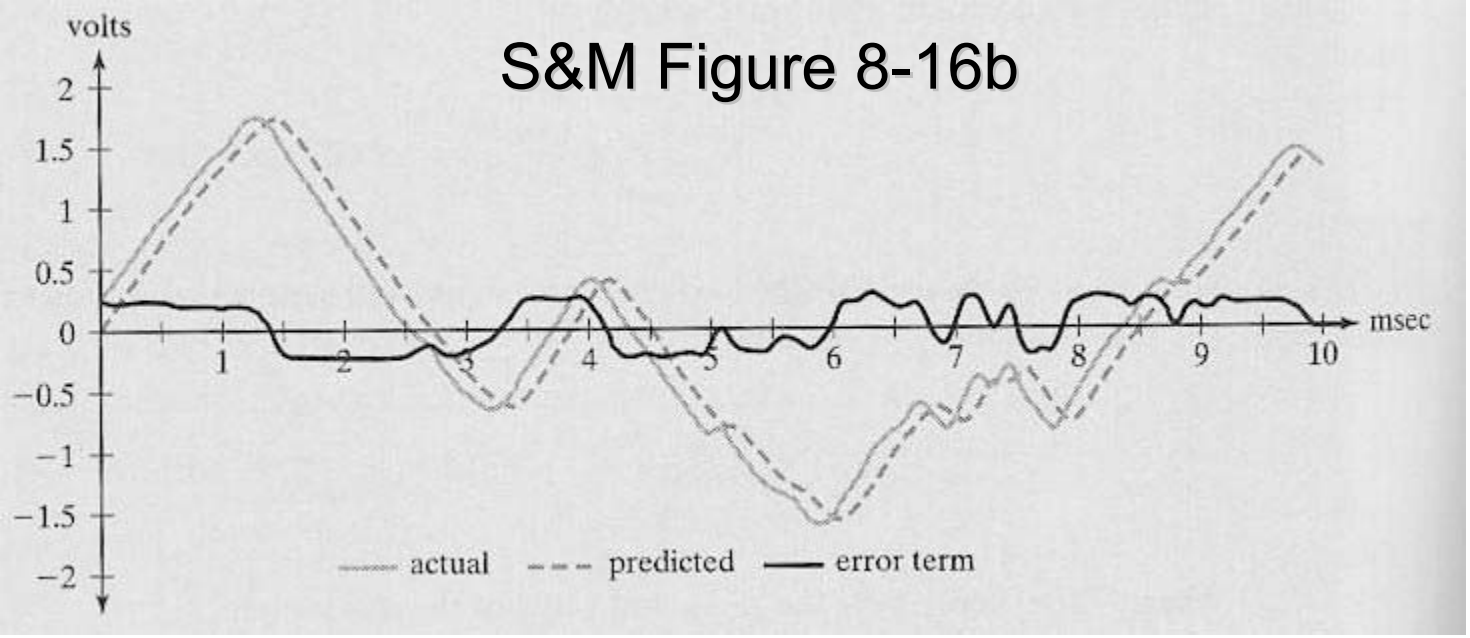
$$S(n) = 0.75\, s(n-1) + 0.2\, s(n-2) + 0.05\, s(n-3)$$

where $S(n)$ is the predicted value of the n th sample and s(n-i) is the n-i th sample. The error signal is $s(n) - S(n)$



S&M Figure 8-15

- A typical continuous analog signal is sampled and results in a discrete signal s(n), The discrete predicted signal *S*(n) is recursively computed. The discrete error signal is transmitted and has less quantizing bits than the actual discrete signal.



- A DPCM example of actual discrete values, predicted values and the error terms:

Table 8-3 Actual Values, Predicted Values, and Error Terms for Figure 8-16a Using DPCM

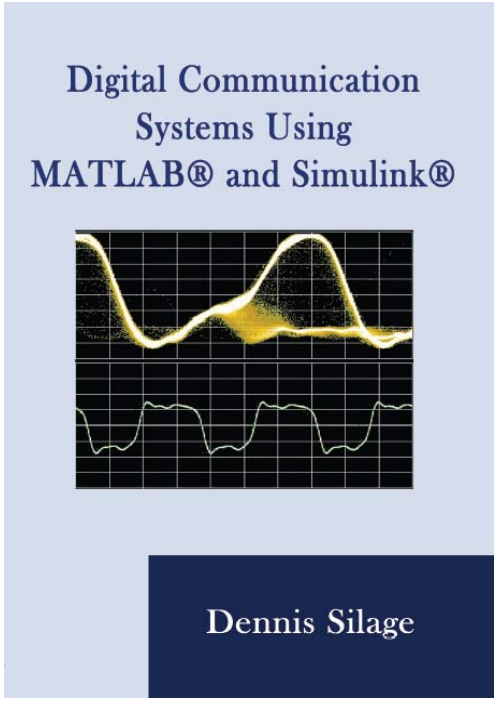
Time (msec)	Predicted Values				Actual Values	Error Terms
0	0.75(0)	+ 0.20(0)	+ 0.05(0)	= 0v	0.23v	0.23v
0.125	0.75(0.23)	+ 0.20(0)	+ 0.05(0)	= 0.1725v	0.38v	0.2075v
0.25	0.75(0.38)	+ 0.20(0.23)	+ 0.05(0)	= 0.33v	0.56v	0.229v
0.375	0.75(0.56)	+ 0.20(0.38)	+ 0.05(0.23)	= 0.5075v	0.73v	0.2225v
0.5	0.75(0.73)	+ 0.20(0.56)	+ 0.05(0.38)	= 0.6785v	0.90v	0.2215v
0.625	0.75(0.90)	+ 0.20(0.73)	+ 0.05(0.56)	= 0.849v	1.05v	0.201v
0.7				1.004v	1.2v	0.196v
0.875				1.155v	1.35v	0.195v
1				1.305v	1.48v	0.175v
1.125				1.440v	1.62v	0.18v
etc.				etc.	etc.	etc.

S&M Table 8-3

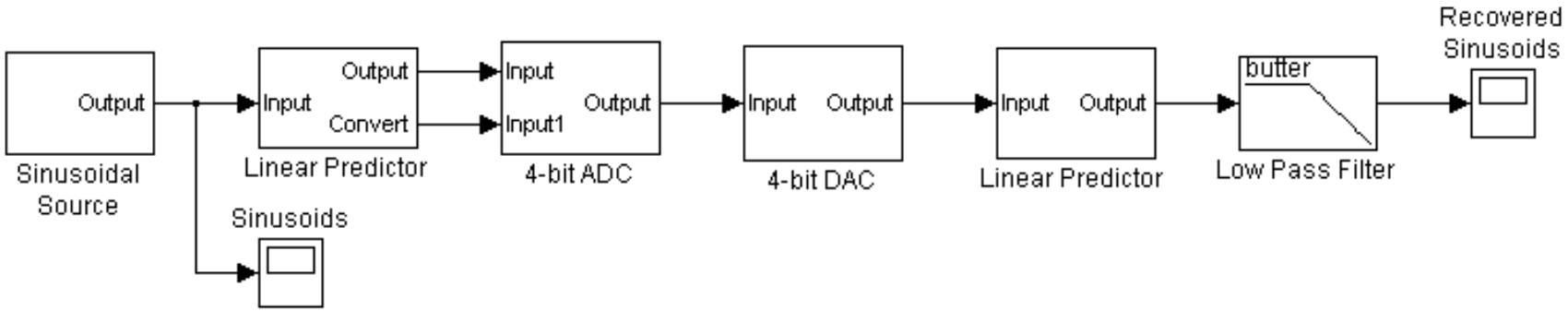
Chapter 8

Analog-to-Digital and Digital-to-Analog Conversion

- *Differential Pulse Code Modulation*
- Pages 175-180

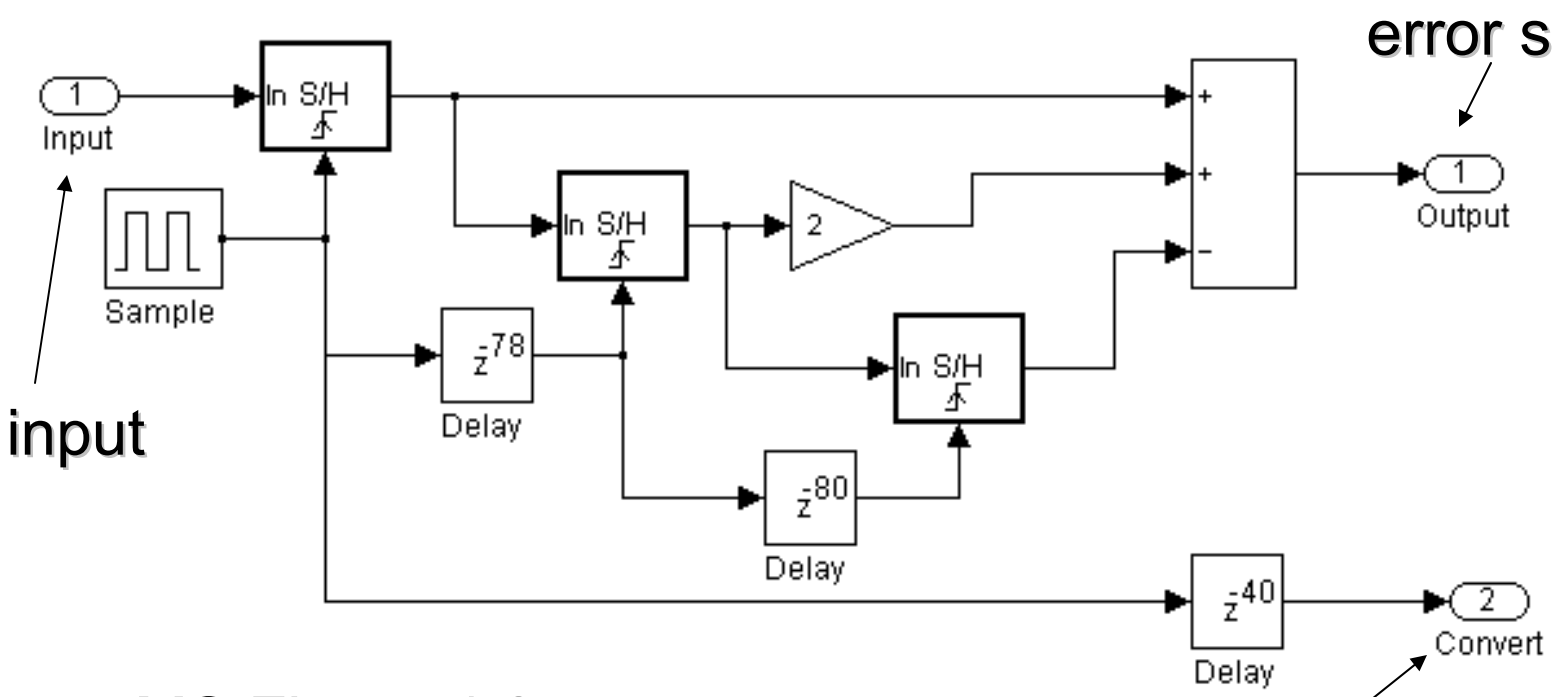


- A 4-bit first order *differential pulse code modulator* (DPCM) can be simulated in *Simulink*.



MS Figure 4.26

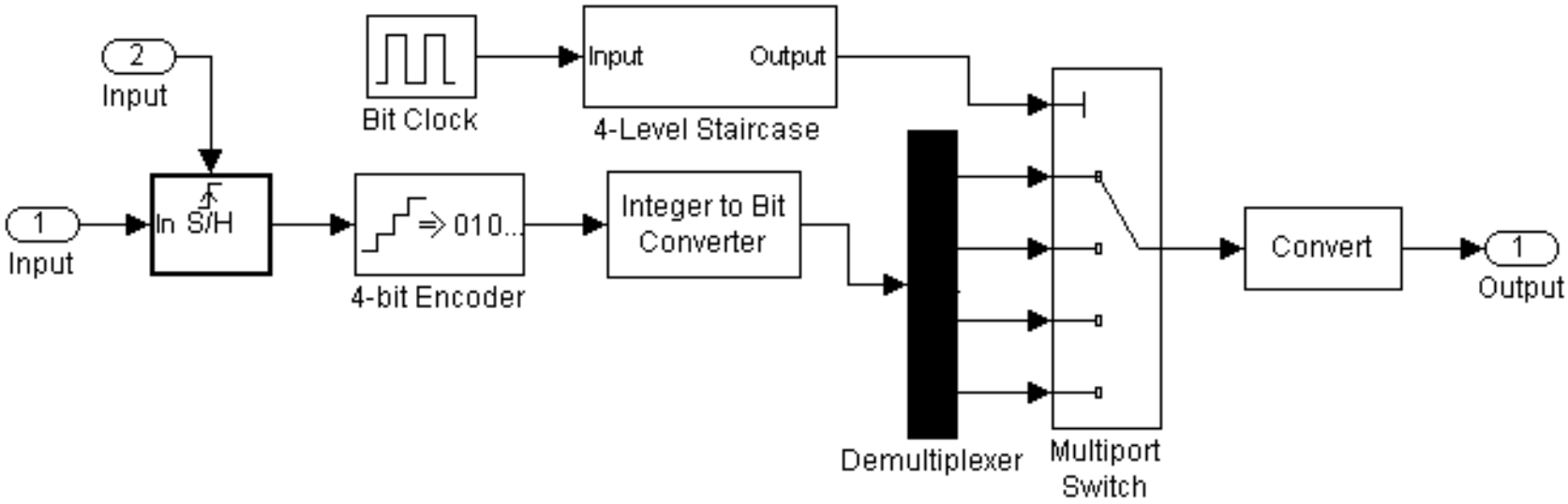
- The first order linear predictor MetaSystem determines the error signal: $e(n) = s(n+1) - 2\,s(n) + s(n-1)$



MS Figure 4.27

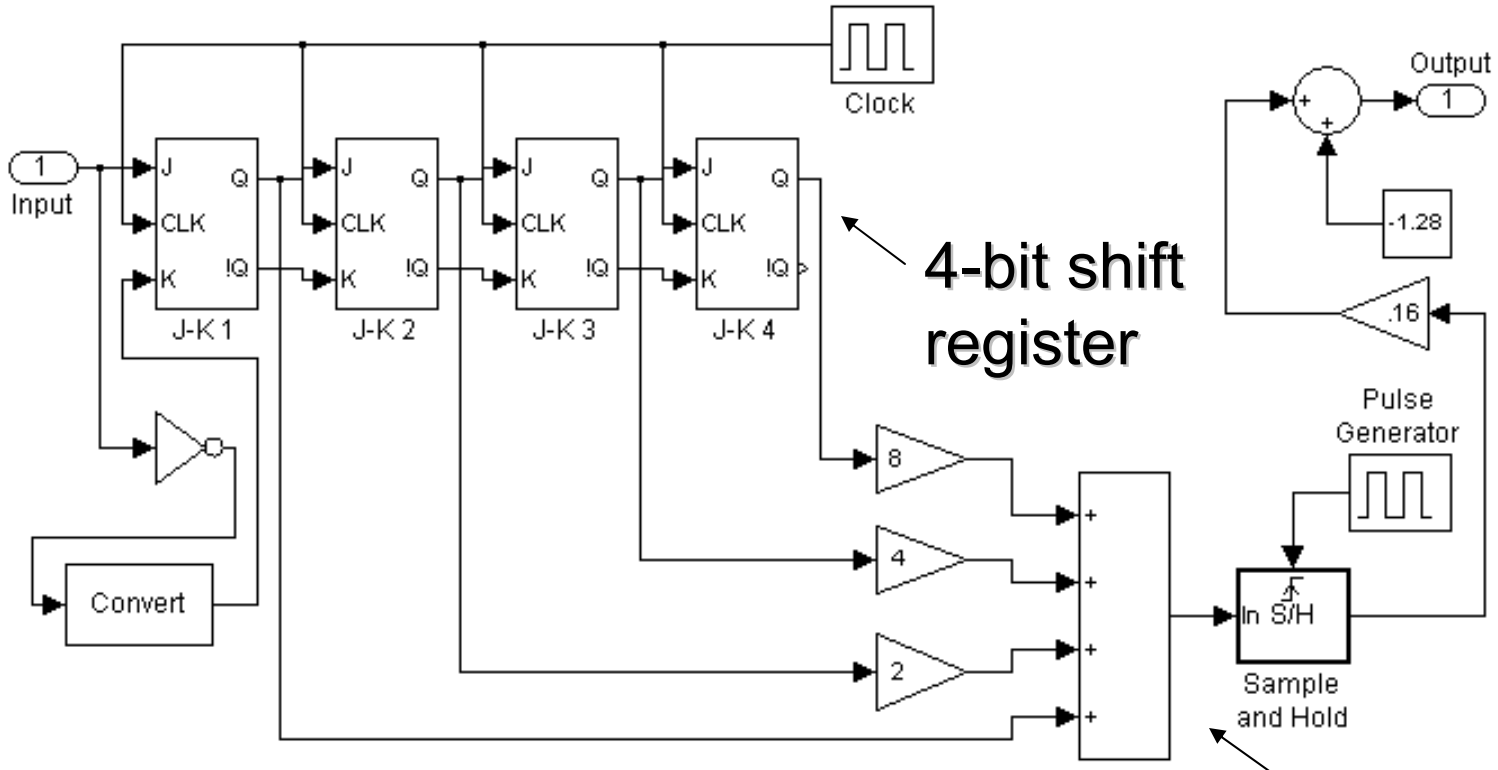
ADC conversion command

- The *Simulink* 4-bit ADC subsystem of the DPCM system is similar to the 8-bit ADC of the PCM system and illustrates *design reuse*.



MS Figure 4.28

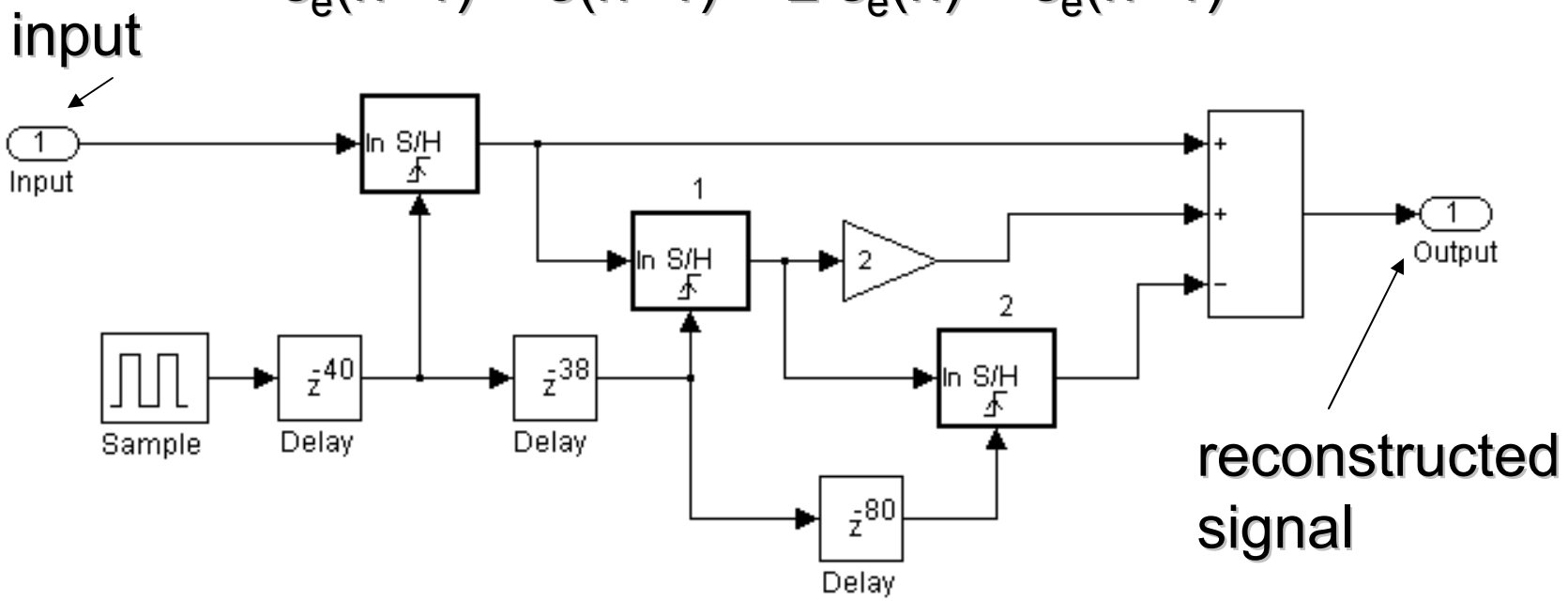
- The *Simulink* 4-bit DAC subsystem of the DPCM system is also similar to the 8-bit DAC of the PCM system and again illustrates *design reuse*.



MS Figure 4.29

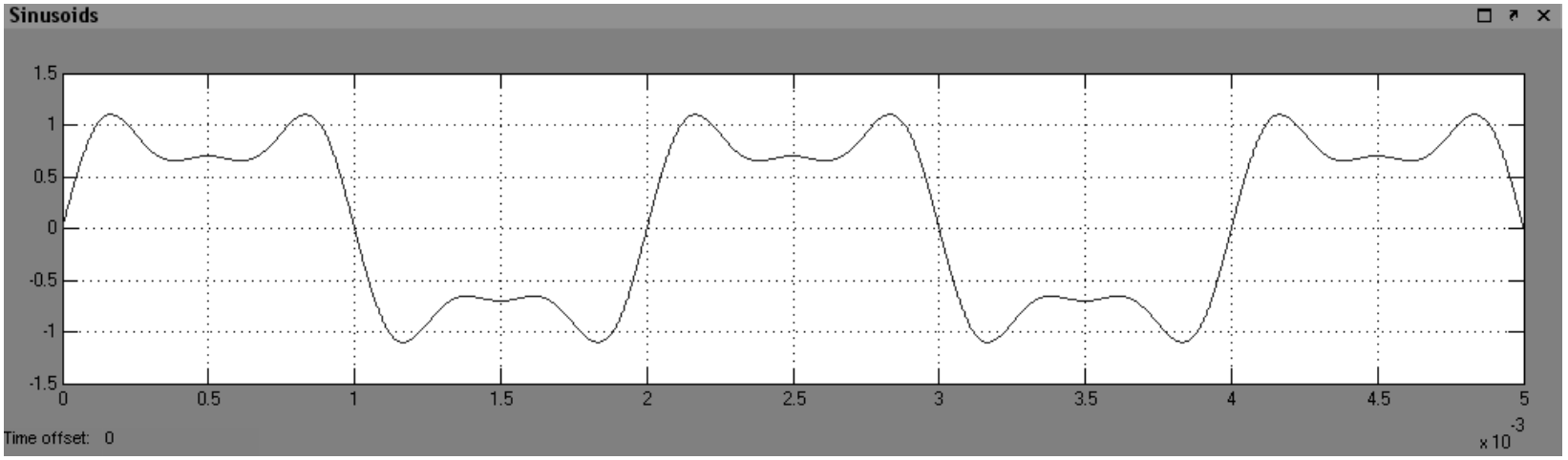
- The first order linear predictor *Simulink* subsystem reconstructs an estimate of the signal $s_e(n)$ from the error signal e(n) received and past estimates:

$$s_e(n+1) = e(n+1) + 2\,s_e(n) - s_e(n-1)$$

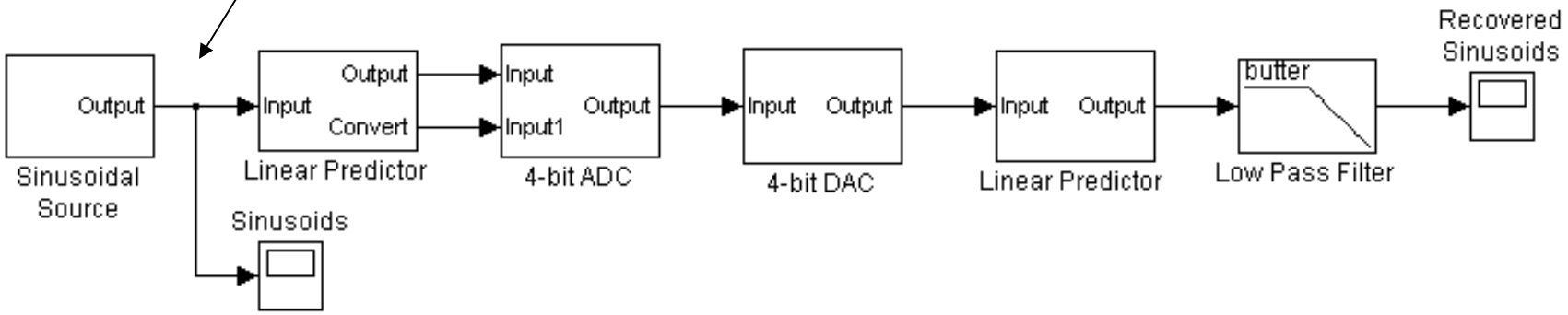


MS Figure 4.30

- Analog input signal of the DPCM system

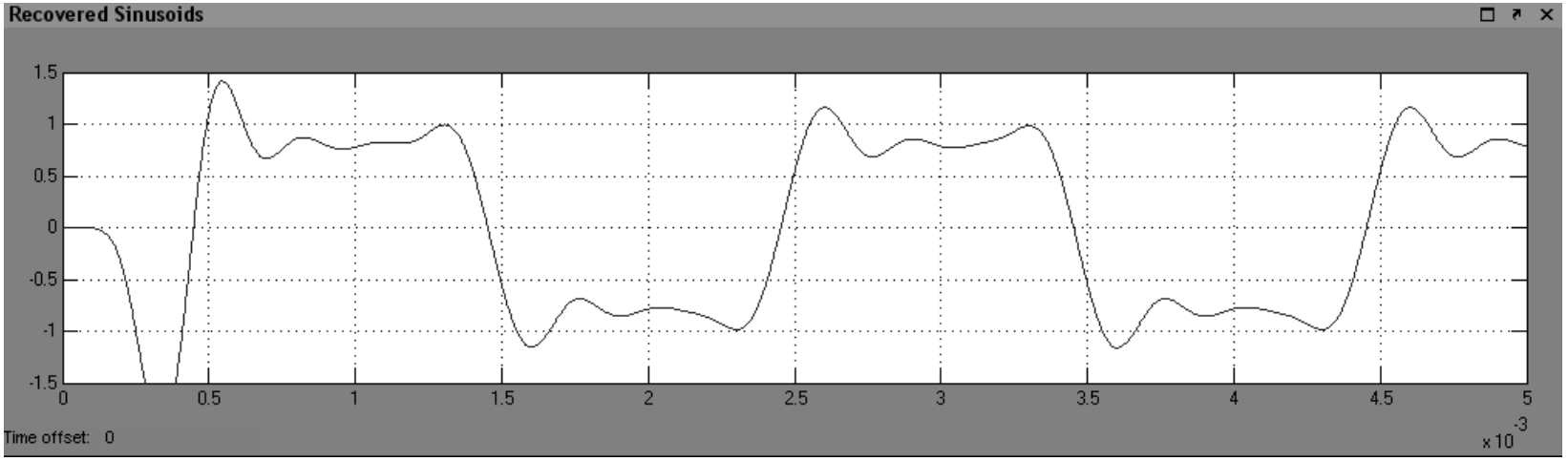


MS Figure 4.31

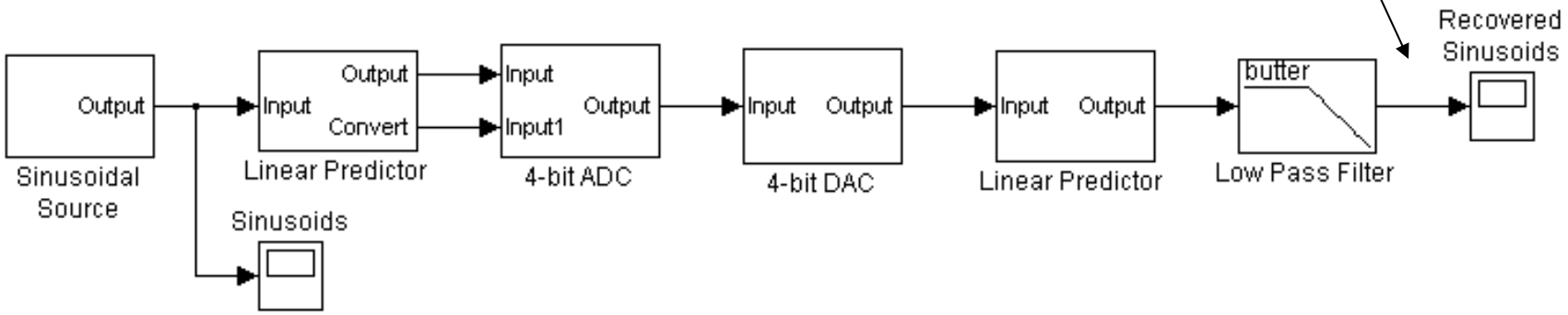


MS Figure 4.31

- Output of the 4-bit first order DPCM system

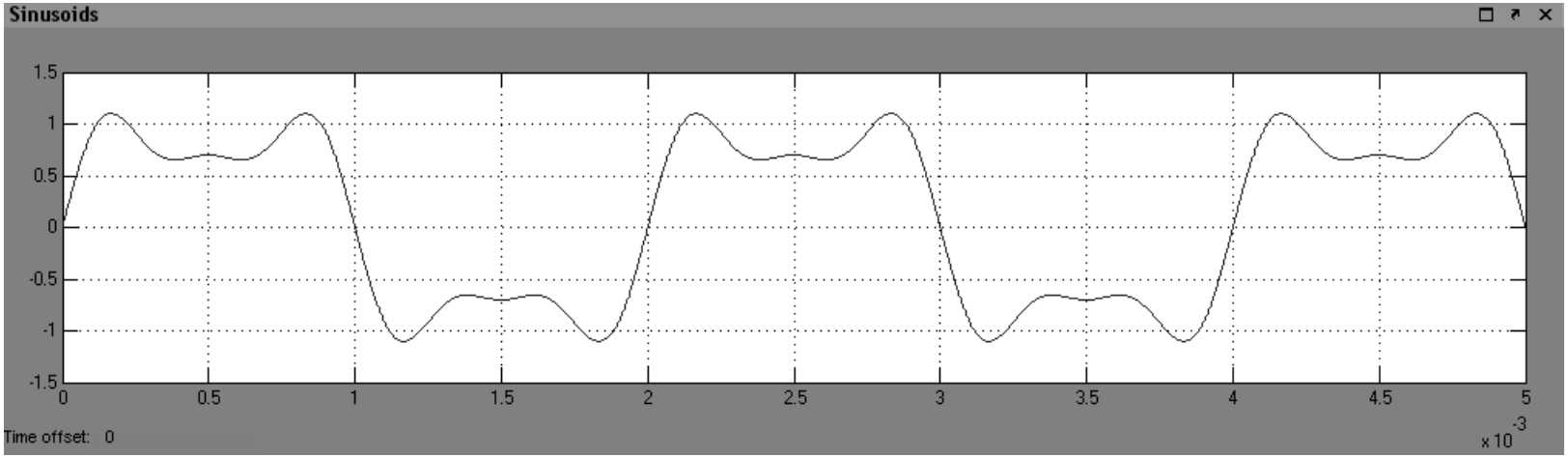


MS Figure 4.31

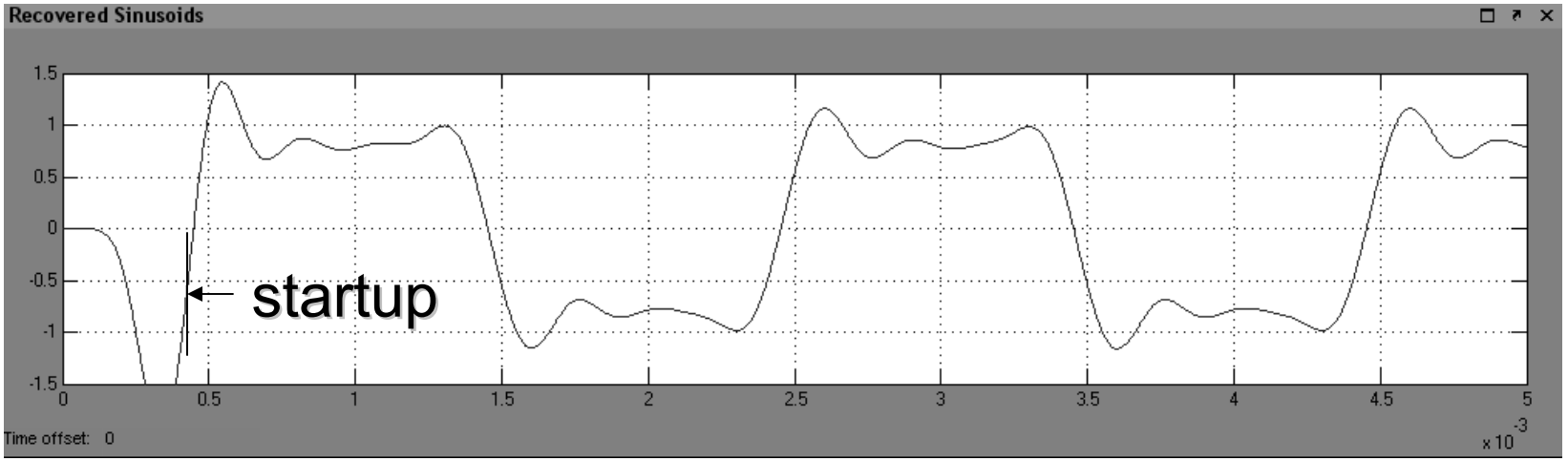


MS Figure 4.31

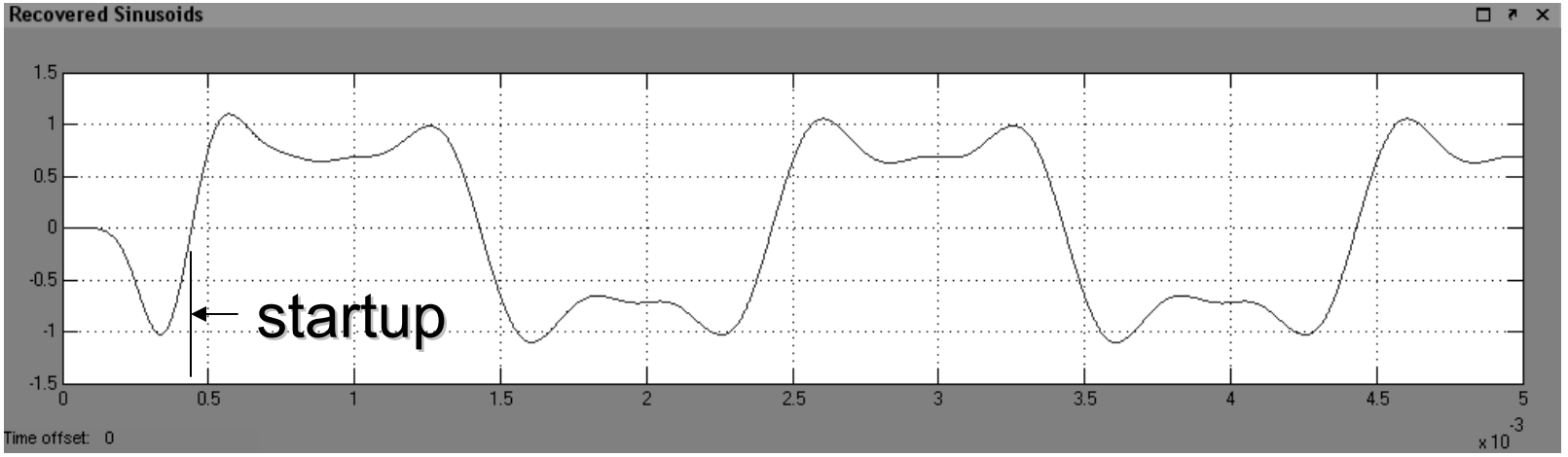
- Analog input signal to the DPCM system



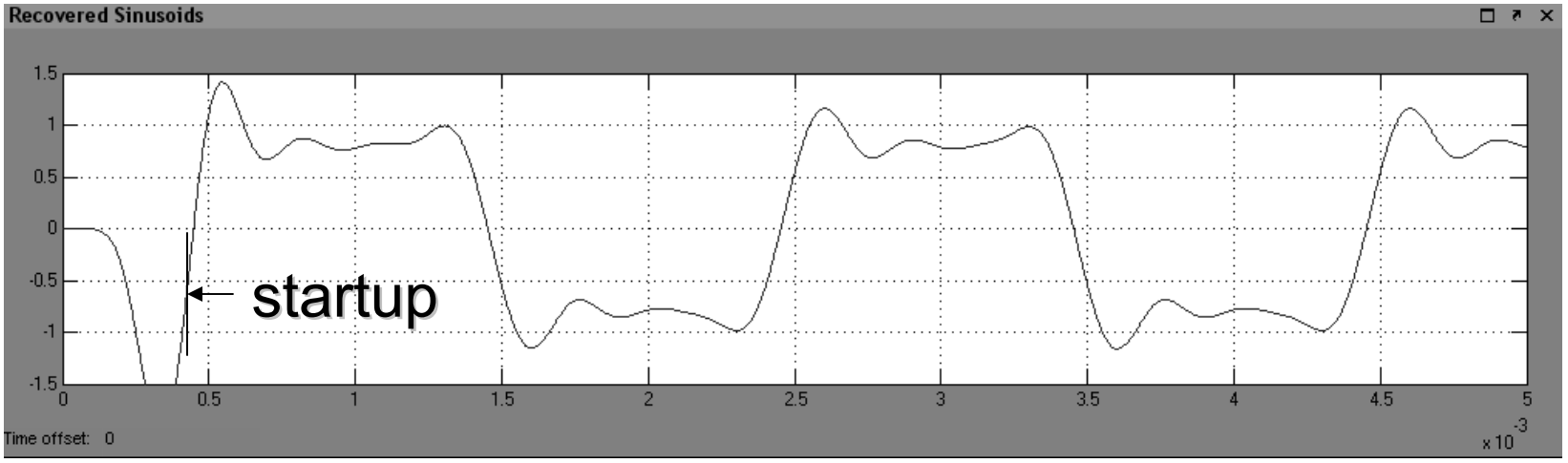
- Output of the 4-bit first order DPCM system MS Figure 4.31



- Output of the 8-bit PCM system MS Figure 4.25



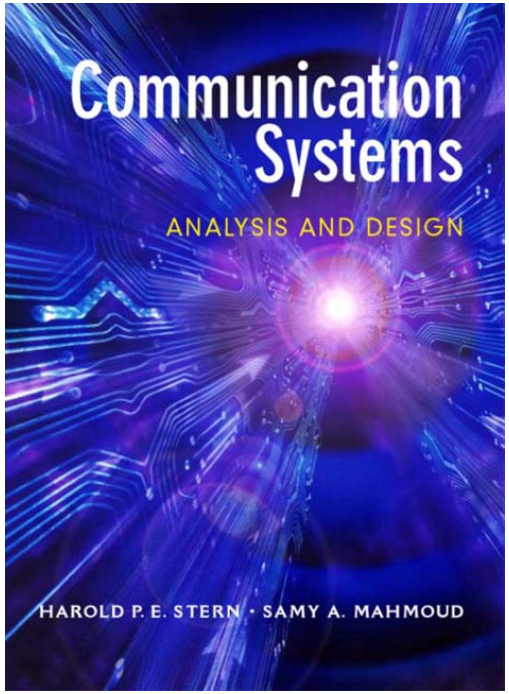
- Output of the 4-bit first order DPCM system MS Figure 4.31



Chapter 8

Analog-to-Digital and Digital-to-Analog Conversion

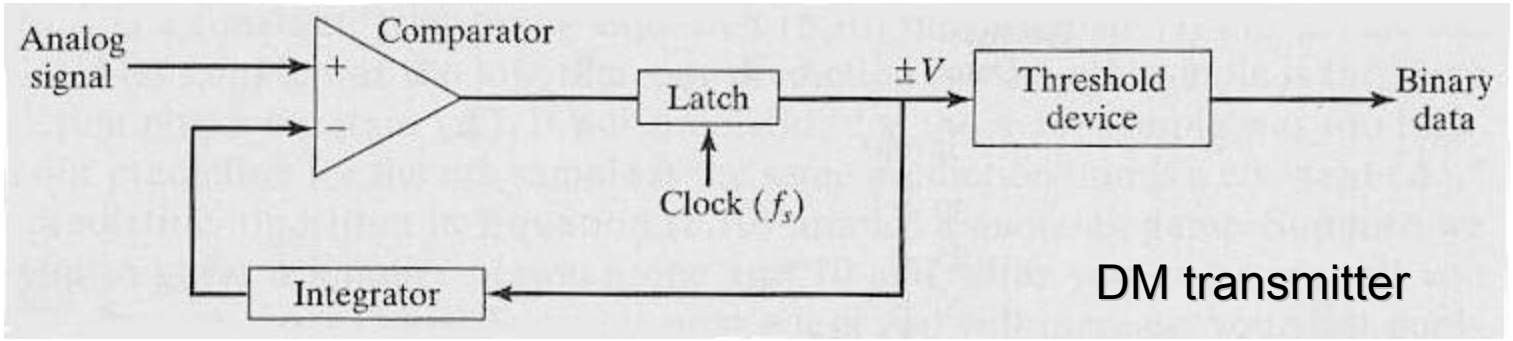
- *Delta Modulation*
- Pages 411-415

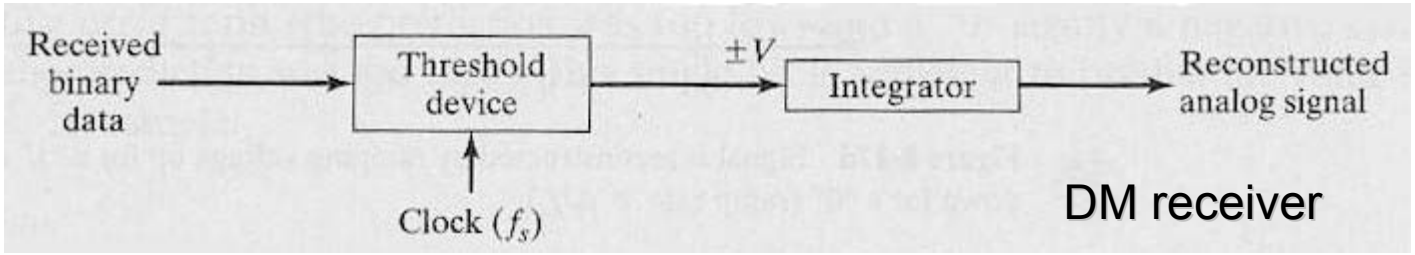


- *Delta modulation* is an extreme example of DPCM using 1-bit data representing ± Δ:

$$S(n) = S(n-1) + \Delta \quad b_i = 1 \quad \text{if } S(n-1) \le s(n-1)$$
$$S(n) = S(n-1) - \Delta \quad b_i = 0 \quad \text{if } S(n-1) > s(n-1)$$

S&M Eq. 8.10

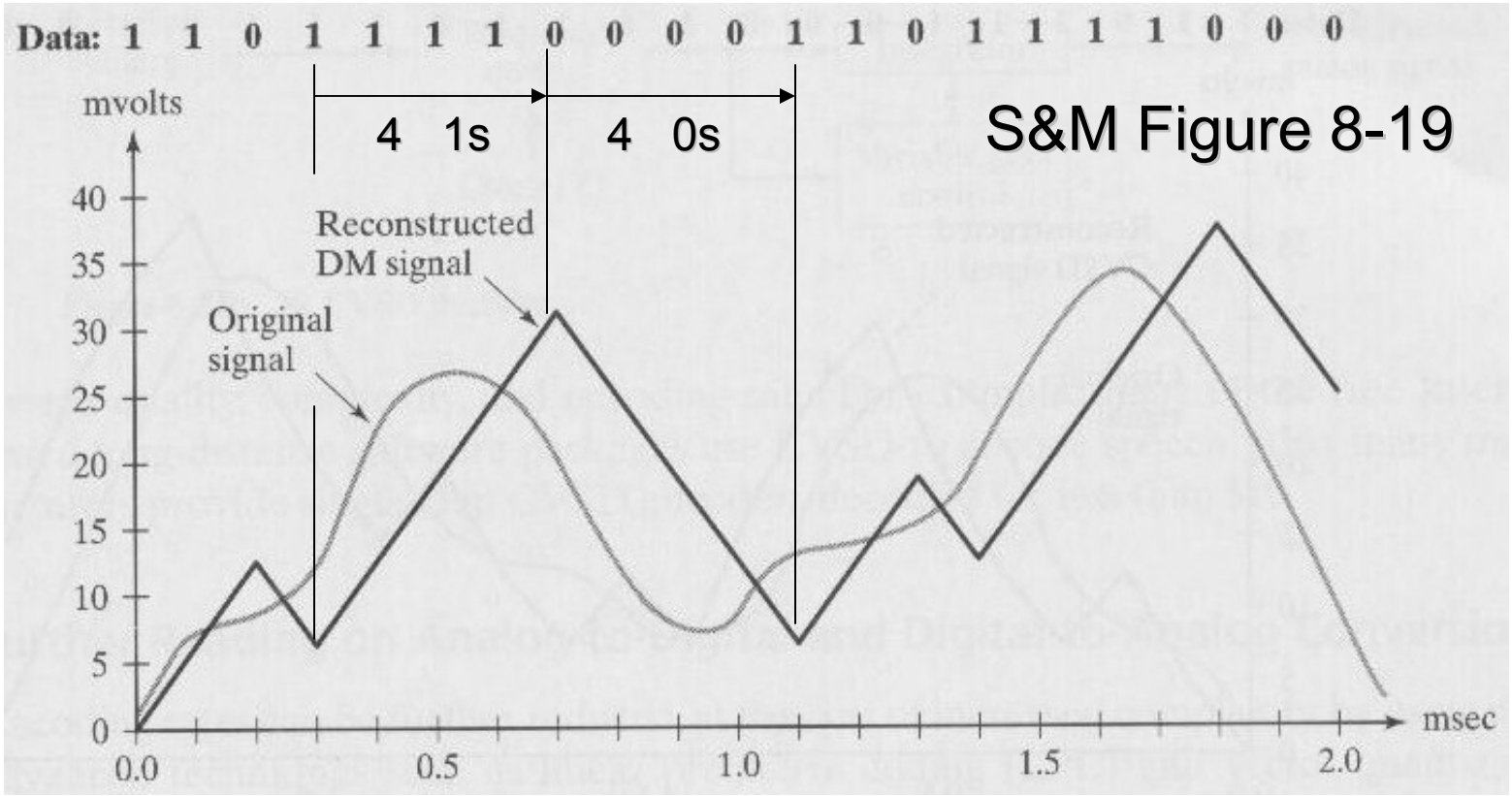




S&M Figure 8-18

- The reconstructed signal increments ± Δ on each transmitted bit.

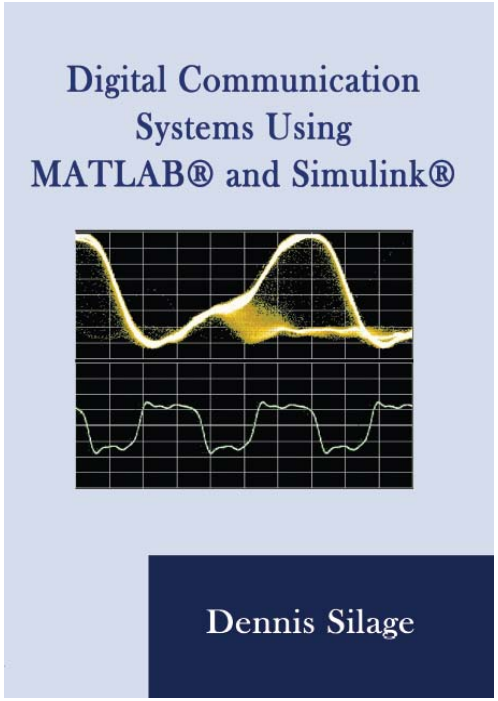
$b_i = 1 \;\; S(n) = S(n-1) + \Delta \qquad b_i = 0 \;\; S(n) = S(n-1) - \Delta$



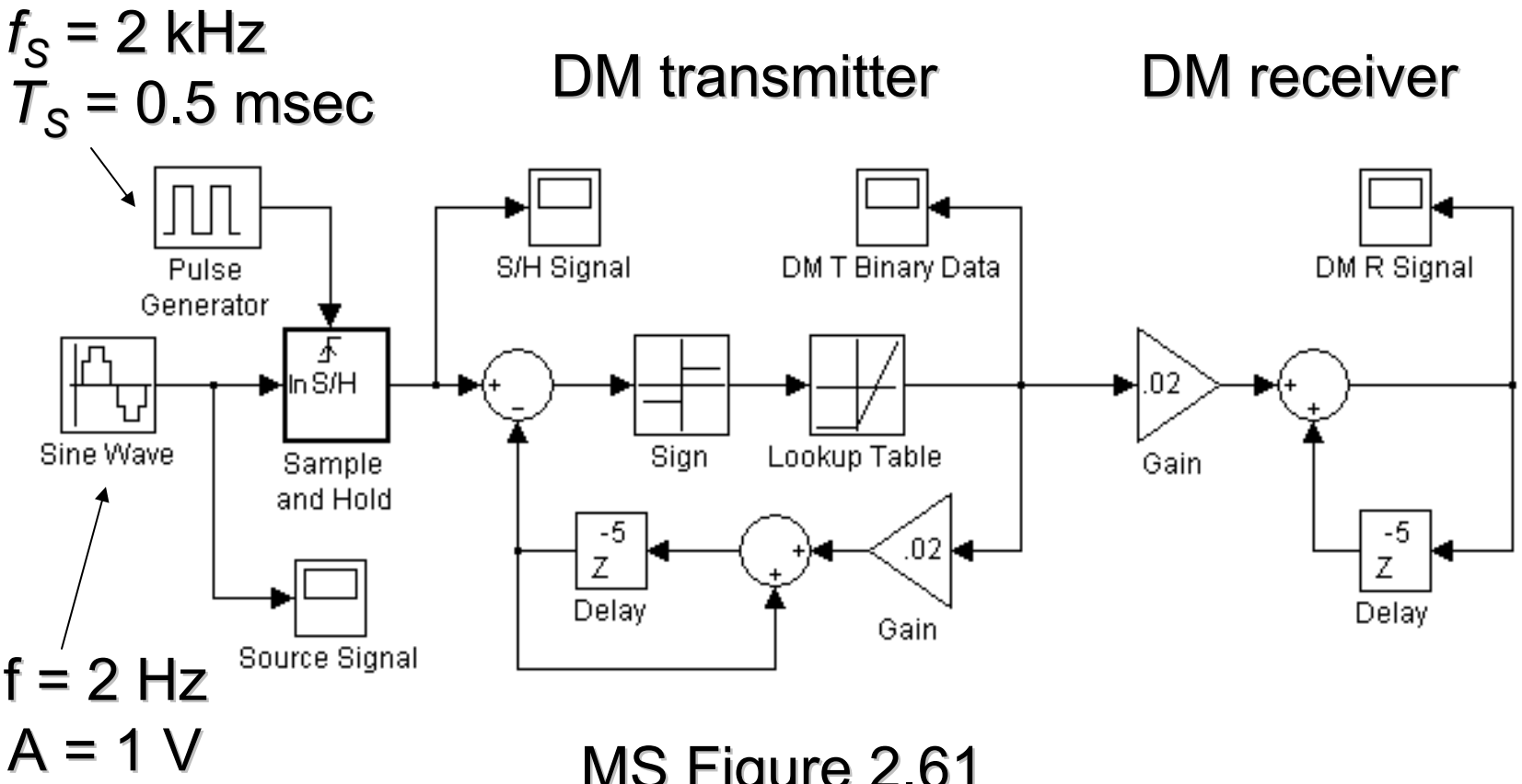
Chapter 8

Analog-to-Digital and Digital-to-Analog Conversion

- *Delta Modulation*
- Pages 72-75



- Delta modulation (DM) can be simulated in *Simulink*. The DM receiver utilizes a sample and hold token as an accumulator and the step size Δ = 20 mV.



MS Figure 2.61

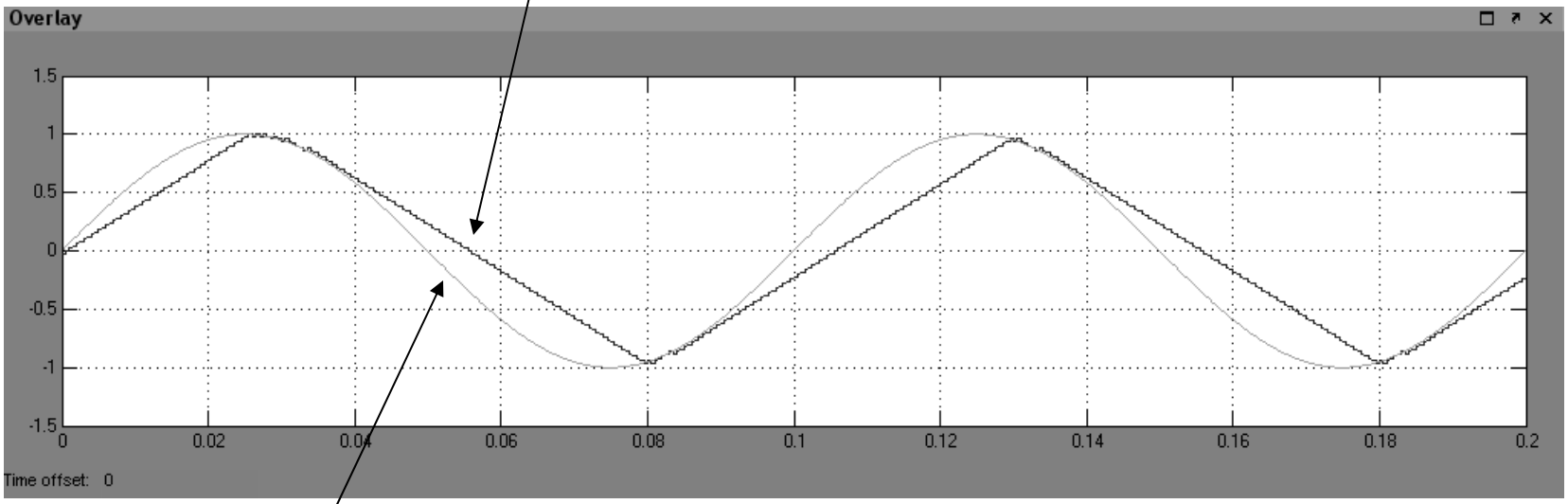
- DM can be subject to *slope overload* which occurs when:

$$\Delta / T_S < \max | d\, m(t) / dt | \qquad \text{SVU Eq. 2.61 modified}$$

Here the sinusoid has A = 1 but f = 10 Hz and:

$$\Delta / T_S = 20 \text{ mV} / 0.5 \text{ msec} = 40 < \max | d\, m(t) / dt | = 80\pi$$

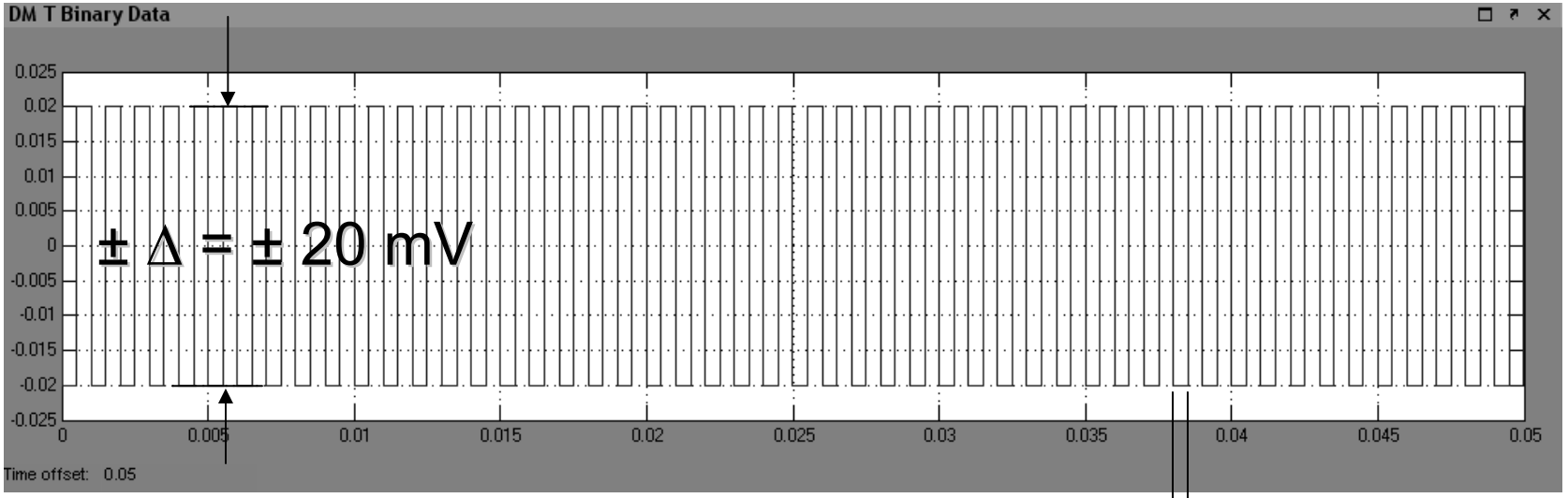
and slope overload occurs.



sinusoidal input signal

MS Figure 2.63

- *Granular noise* occurs in DM because if the input m(t) is constant the received signal *oscillates* by ± Δ because there is no *0* possible. *Clocking* occurs at the DM symbol interval T_S = 0.5 msec.

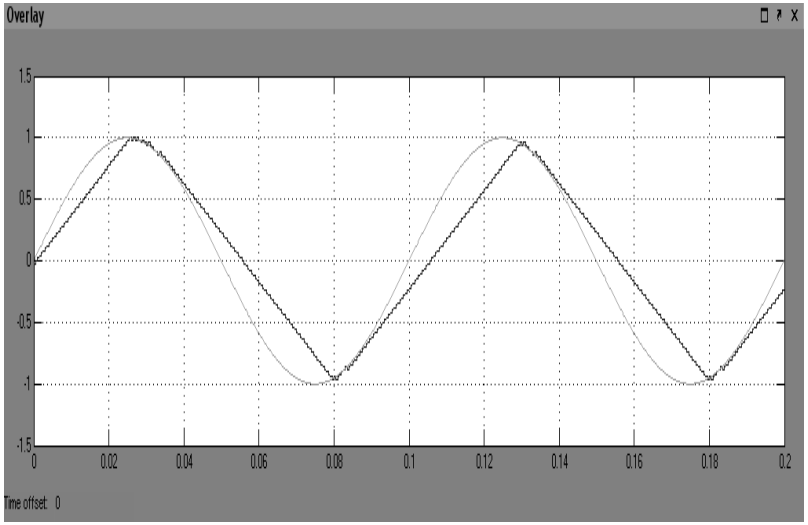


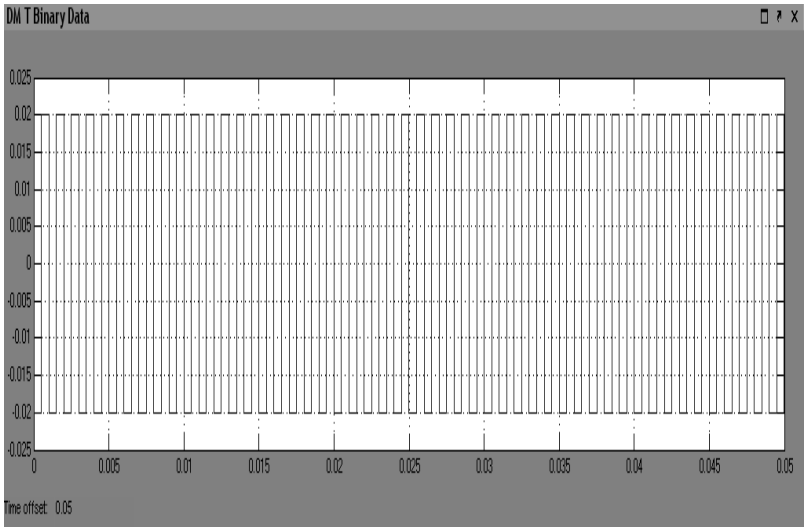
Δ = 20 mV

MS Figure 2.64

T_S = 0.5 msec

- The tradeoff between slope overload and granular noise is that a large value of Δ (to avoid slope overload) would increase granular noise. A decrease in T_s (again to avoid slope overload) would increase the data rate r_S.
- The step size Δ = 20 mV and T_S = 0.5 msec (r_S = 2 kb/sec) here.



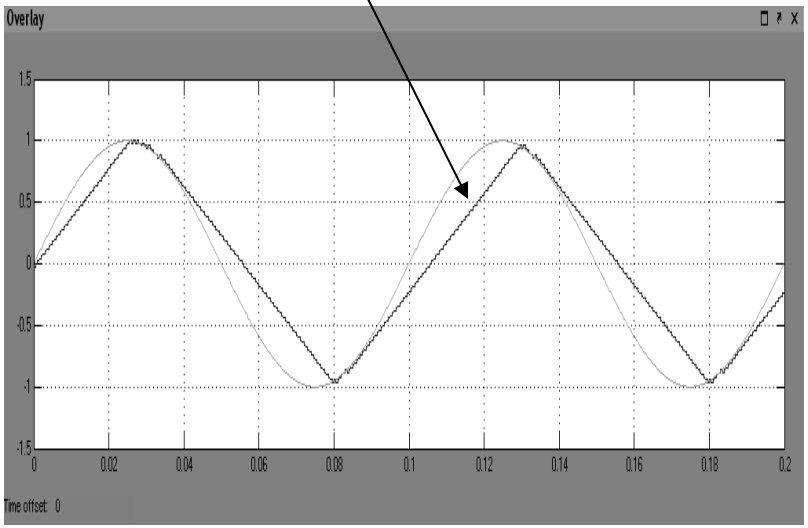


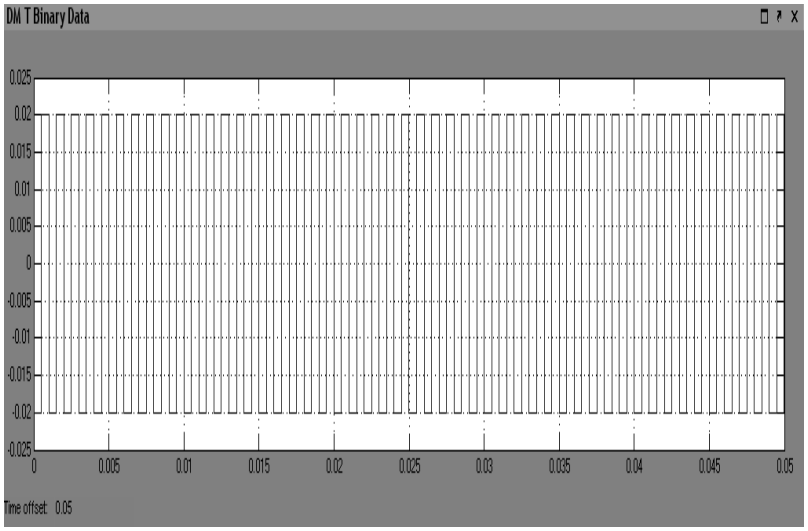
- For a 10 Hz sinusoidal input signal to a DM:

  $m(t) = \sin(2\pi\ 10t)$

  $\max \left| d\, m(t) / dt \right| = 20\pi$

- If step size $\Delta = 20$ mV and $T_S = 0.5$ msec then $\Delta / T_S = 40 < \max \left| d\, m(t) / dt \right| = 20\pi$ so *slope overload is predicted to occur*.



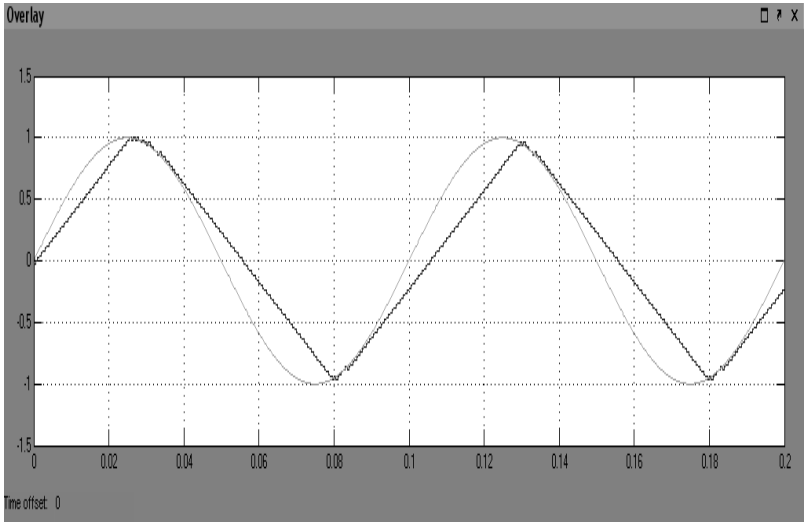


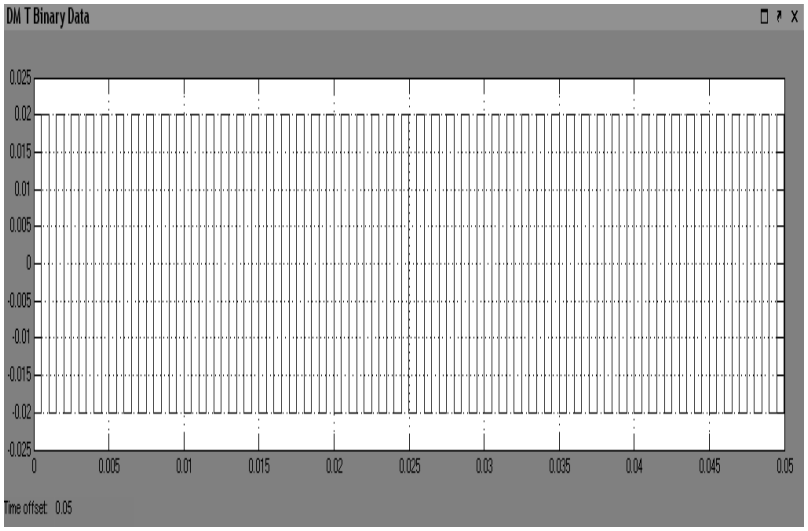
- For the 10 Hz sinusoidal input signal to a DM

$$m(t) = \sin(2\pi\, 10t)$$

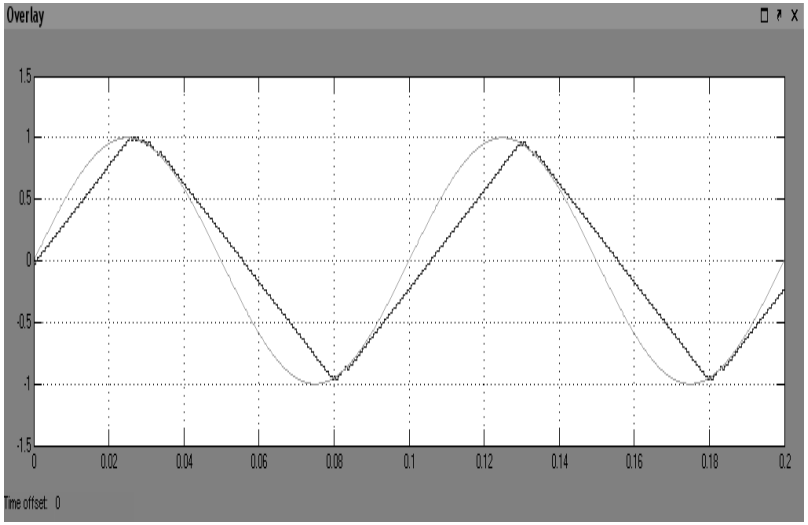
$$\max \left| \frac{d\, m(t)}{dt} \right| = 20\pi$$

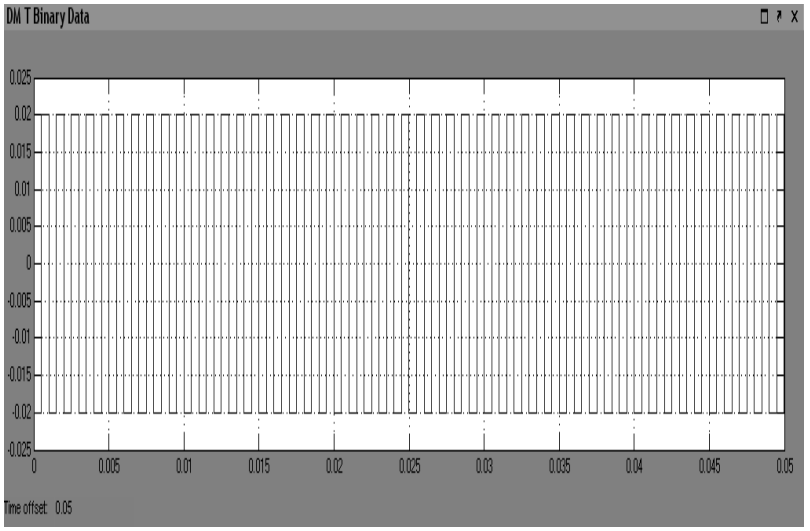
and the step size remains $\Delta = 20$ mV but $T_S = 0.25$ msec then $\Delta / T_S = 80 > \max \left| \frac{d\, m(t)}{dt} \right|$ and slope overload is mitigated but $r_S =$ 4 kb/sec.





- In comparison, an 8-bit PCM system sampling a 10 Hz sinusoid at a reasonable sampling rate of 500 Hz (50 sampling points/period) has $r_b = 8(500) = 4$ kb/sec or $r_b = r_S$ but PCM is more complicated than DM.





End of Chapter 8

Analog-to-Digital and Digital-to-Analog Conversion