INTRODUCTION TO POWER ELECTRONICS

Power Electronics is a field which combines Power (electric power), Electronics and Control systems.

Power engineering deals with the static and rotating power equipment for the generation, transmission and distribution of electric power.

Electronics deals with the study of solid state semiconductor power devices and circuits for Power conversion to meet the desired control objectives (to control the output voltage and output power).

Power electronics may be defined as the subject of applications of solid state power semiconductor devices (Thyristors) for the control and conversion of electric power.

Power electronics deals with the study and design of Thyristorised power controllers for variety of application like Heat control, Light/Illumination control, Motor control – AC/DC motor drives used in industries, High voltage power supplies, Vehicle propulsion systems, High voltage direct current (HVDC) transmission.

BRIEF HISTORY OF POWER ELECTRONICS

The first Power Electronic Device developed was the Mercury Arc Rectifier during the year 1900. Then the other Power devices like metal tank rectifier, grid controlled vacuum tube rectifier, ignitron, phanotron, thyratron and magnetic amplifier, were developed & used gradually for power control applications until 1950.

The first SCR (silicon controlled rectifier) or Thyristor was invented and developed by Bell Lab's in 1956 which was the first PNPN triggering transistor.

The second electronic revolution began in the year 1958 with the development of the commercial grade Thyristor by the General Electric Company (GE). Thus the new era of power electronics was born. After that many different types of power semiconductor devices & power conversion techniques have been introduced.The power electronics revolution is giving us the ability to convert, shape and control large amounts of power.

SOME APPLICATIONS OF POWER ELECTRONICS

Advertising, air conditioning, aircraft power supplies, alarms, appliances – (domestic and industrial), audio amplifiers, battery chargers, blenders, blowers, boilers, burglar alarms, cement kiln, chemical processing, clothes dryers, computers, conveyors, cranes and hoists, dimmers (light dimmers), displays, electric door openers, electric dryers, electric fans, electric vehicles, electromagnets, electro mechanical electro plating, electronic ignition, electrostatic precipitators, elevators, fans, flashers, food mixers, food warmer trays, fork lift trucks, furnaces, games, garage door openers, gas turbine starting, generator exciters, grinders, hand power tools, heat controls, high frequency lighting, HVDC transmission, induction heating, laser power supplies, latching relays, light flashers, linear induction motor controls, locomotives, machine tools, magnetic recording, magnets, mass transit railway system, mercury arc lamp ballasts, mining, model trains, motor controls, motor drives, movie projectors, nuclear reactor control rod, oil well drilling, oven controls, paper mills, particle accelerators, phonographs, photo copiers, power suppliers, printing press, pumps and compressors, radar/sonar power supplies,

refrigerators, regulators, RF amplifiers, security systems, servo systems, sewing machines, solar power supplies, solid-state contactors, solid-state relays, static circuit breakers, static relays, steel mills, synchronous motor starting, TV circuits, temperature controls, timers and toys, traffic signal controls, trains, TV deflection circuits, ultrasonic generators, UPS, vacuum cleaners, VAR compensation, vending machines, VLF transmitters, voltage regulators, washing machines, welding equipment.

POWER ELECTRONIC APPLICATIONS

COMMERCIAL APPLICATIONS

Heating Systems Ventilating, Air Conditioners, Central Refrigeration, Lighting, Computers and Office equipments, Uninterruptible Power Supplies (UPS), Elevators, and Emergency Lamps.

DOMESTIC APPLICATIONS

Cooking Equipments, Lighting, Heating, Air Conditioners, Refrigerators & Freezers, Personal Computers, Entertainment Equipments, UPS.

INDUSTRIAL APPLICATIONS

Pumps, compressors, blowers and fans. Machine tools, arc furnaces, induction furnaces, lighting control circuits, industrial lasers, induction heating, welding equipments.

AEROSPACE APPLICATIONS

Space shuttle power supply systems, satellite power systems, aircraft power systems.

TELECOMMUNICATIONS

Battery chargers, power supplies (DC and UPS), mobile cell phone battery chargers.

TRANSPORTATION

Traction control of electric vehicles, battery chargers for electric vehicles, electric locomotives, street cars, trolley buses, automobile electronics including engine controls.

UTILITY SYSTEMS

High voltage DC transmission (HVDC), static VAR compensation (SVC), Alternative energy sources (wind, photovoltaic), fuel cells, energy storage systems, induced draft fans and boiler feed water pumps.

POWER SEMICONDUCTOR DEVICES

- Power Diodes.
- Power Transistors (BJT's).
- Power MOSFETS.
- IGBT's.
- Thyristors

Thyristors are a family of p-n-p-n structured power semiconductor switching devices

- SCR's (Silicon Controlled Rectifier)

  The silicon controlled rectifier is the most commonly and widely used member of the thyristor family. The family of thyristor devices include SCR's, Diacs, Triacs, SCS, SUS, LASCR's and so on.

POWER SEMICONDUCTOR DEVICES USED IN POWER ELECTRONICS

The first thyristor or the SCR was developed in 1957. The conventional Thyristors (SCR's) were exclusively used for power control in industrial applications until 1970. After 1970, various types of power semiconductor devices were developed and became commercially available. The power semiconductor devices can be divided broadly into five types

- Power Diodes.
- Thyristors.
- Power BJT's.
- Power MOSFET's.
- Insulated Gate Bipolar Transistors (IGBT's).
- Static Induction Transistors (SIT's).

The Thyristors can be subdivided into different types

- Forced-commutated Thyristors (Inverter grade Thyristors)
- Line-commutated Thyristors (converter-grade Thyristors)
- Gate-turn off Thyristors (GTO).
- Reverse conducting Thyristors (RCT's).
- Static Induction Thyristors (SITH).
- Gate assisted turn-off Thyristors (GATT).
- Light activated silicon controlled rectifier (LASCR) or Photo SCR's.
- MOS-Controlled Thyristors (MCT's).

POWER DIODES

Power diodes are made of silicon p-n junction with two terminals, anode and cathode. P-N junction is formed by alloying, diffusion and epitaxial growth. Modern techniques in diffusion and epitaxial processes permit desired device characteristics.

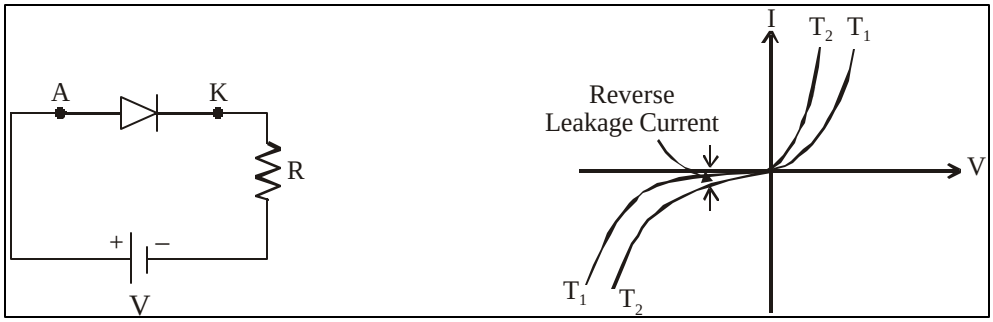
The diodes have the following advantages

- High mechanical and thermal reliability
- High peak inverse voltage

- Low reverse current
- Low forward voltage drop
- High efficiency
- Compactness.

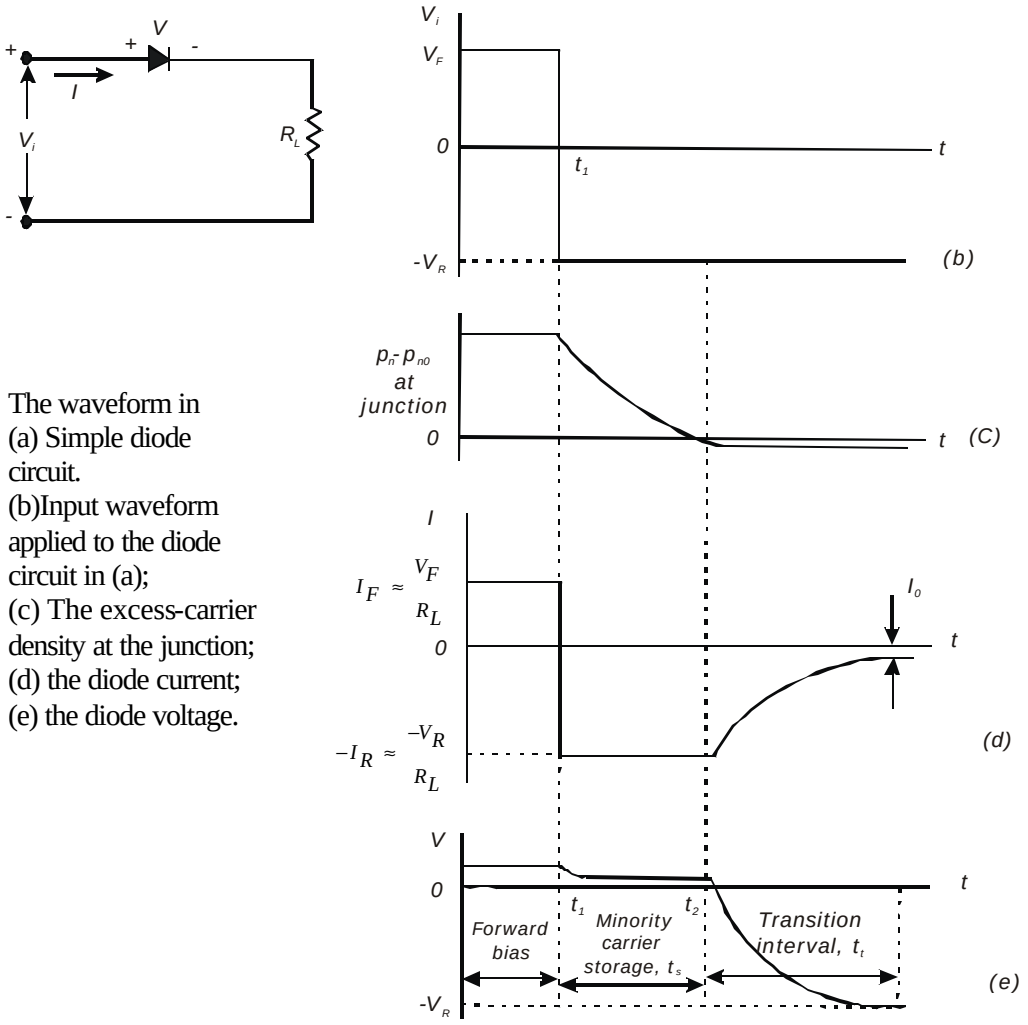
Diode is forward biased when anode is made positive with respect to the cathode. Diode conducts fully when the diode voltage is more than the cut-in voltage (0.7 V for Si). Conducting diode will have a small voltage drop across it.

Diode is reverse biased when cathode is made positive with respect to anode. When reverse biased, a small reverse current known as leakage current flows. This leakage current increases with increase in magnitude of reverse voltage until avalanche voltage is reached (breakdown voltage).



DYNAMIC CHARACTERISTICS OF POWER SWITCHING DIODES

At low frequency and low current, the diode may be assumed to act as a perfect switch and the dynamic characteristics (turn on & turn off characteristics) are not very important. But at high frequency and high current, the dynamic characteristics plays an important role because it increases power loss and gives rise to large voltage spikes which may damage the device if proper protection is not given to the device.



The waveform in
(a) Simple diode circuit.
(b)Input waveform applied to the diode circuit in (a);
(c) The excess-carrier density at the junction;
(d) the diode current;
(e) the diode voltage.

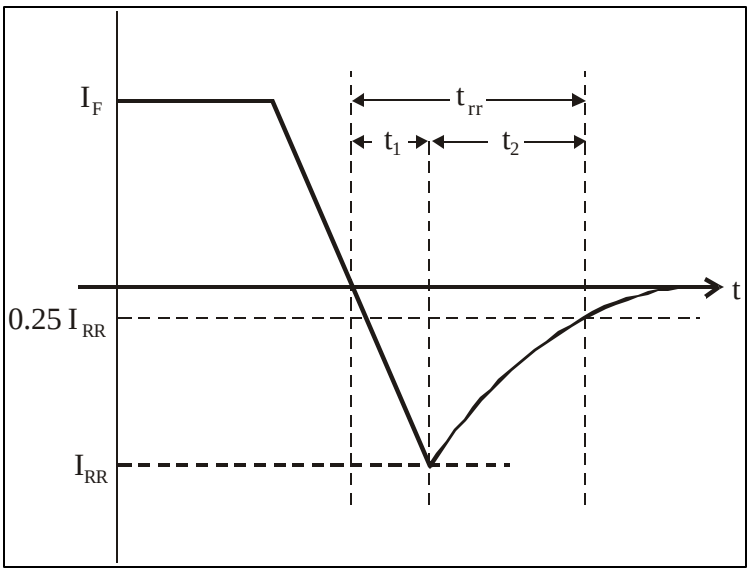
Fig: Storage & Transition Times during the Diode Switching

REVERSE RECOVERY CHARACTERISTIC

Reverse recovery characteristic is much more important than forward recovery characteristics because it adds recovery losses to the forward loss. Current when diode is forward biased is due to net effect of majority and minority carriers. When diode is in forward conduction mode and then its forward current is reduced to zero (by applying reverse voltage) the diode continues to conduct due to minority carriers which remains stored in the p-n junction and in the bulk of semi-conductor material. The minority carriers take some time to recombine with opposite charges and to be neutralized. This time is called the ***reverse recovery time.*** The reverse recovery time (t_{rr}) is measured from the initial zero crossing of the diode current to 25% of maximum reverse current I_{rr}. t_{rr} has 2 components, t_1 and t_2. t_1 is as a result of charge storage in the depletion region of the junction i.e., it is the time between the zero crossing and the peak reverse current I_{rr}. t_2 is as a result of charge storage in the bulk semi-conductor material.

$$t_{rr} = t_1 + t_2$$

$$I_{RR} = t_1 \left(di/dt \right)$$



The reverse recovery time depends on the junction temperature, rate of fall of forward current and the magnitude of forward current prior to commutation (turning off).

When diode is in reverse biased condition the flow of leakage current is due to minority carriers. Then application of forward voltage would force the diode to carry current in the forward direction. But a certain time known as forward recovery time (turn-ON time) is required before all the majority carriers over the whole junction can contribute to current flow. Normally forward recovery time is less than the reverse recovery time. The forward recovery time limits the rate of rise of forward current and the switching speed.

Reverse recovery charge Q_{RR}**,** is the amount of charge carriers that flow across the diode in the reverse direction due to the change of state from forward conduction to reverse blocking condition. The value of reverse recovery charge Q_{RR} is determined form the area enclosed by the path of the reverse recovery current.

$$Q_{RR} \cong \left(\frac{1}{2} I_{RR} t_1 + \frac{1}{2} I_{RR} t_2\right) = \frac{1}{2} I_{RR} t_{RR} \qquad \therefore Q_{RR} = \frac{1}{2} I_{RR} t_{RR}$$

POWER DIODES TYPES

Power diodes can be classified as

- General purpose diodes.
- High speed (fast recovery) diodes.
- Schottky diode.

GENERAL PURPOSE DIODES

The diodes have high reverse recovery time of about 25 microsecs (μsec). They are used in low speed (frequency) applications. e.g., line commutated converters, diode rectifiers and converters for a low input frequency upto 1 KHz. Diode ratings cover a very wide

range with current ratings less than 1 A to several thousand amps (2000 A) and with voltage ratings from 50 V to 5 KV. These diodes are generally manufactured by diffusion process. Alloyed type rectifier diodes are used in welding power supplies. They are most cost effective and rugged and their ratings can go upto 300A and 1KV.

FAST RECOVERY DIODES

The diodes have low recovery time, generally less than 5 μs. The major field of applications is in electrical power conversion i.e., in free-wheeling ac-dc and dc-ac converter circuits. Their current ratings is from less than 1 A to hundreds of amperes with voltage ratings from 50 V to about 3 KV. Use of fast recovery diodes are preferable for free-wheeling in SCR circuits because of low recovery loss, lower junction temperature and reduced di/dt. For high voltage ratings greater than 400 V they are manufactured by diffusion process and the recovery time is controlled by platinum or gold diffusion. For less than 400 V rating epitaxial diodes provide faster switching speeds than diffused diodes. Epitaxial diodes have a very narrow base width resulting in a fast recovery time of about 50 ns.

SCHOTTKY DIODES

A Schottky diode has metal (aluminium) and semi-conductor junction. A layer of metal is deposited on a thin epitaxial layer of the n-type silicon. In Schottky diode there is a larger barrier for electron flow from metal to semi-conductor.

When Schottky diode is forward biased free electrons on n-side gain enough energy to flow into the metal causing forward current. Since the metal does not have any holes there is no charge storage, decreasing the recovery time. Therefore a Schottky diode can switch-off faster than an ordinary p-n junction diode. A Schottky diode has a relatively low forward voltage drop and reverse recovery losses. The leakage current is higher than a p-n junction diode. The maximum allowable voltage is about 100 V. Current ratings vary from about 1 to 300 A. They are mostly used in low voltage and high current dc power supplies. The operating frequency may be as high 100-300 kHz as the device is suitable for high frequency application. Schottky diode is also known as hot carrier diode.

General Purpose Diodes are available upto 5000V, 3500A. The rating of fast-recovery diodes can go upto 3000V, 1000A. The reverse recovery time varies between 0.1 and 5μsec. The fast recovery diodes are essential for high frequency switching of power converters. Schottky diodes have low-on-state voltage drop and very small recovery time, typically a few nanoseconds. Hence turn-off time is very low for schottky diodes. The leakage current increases with the voltage rating and their ratings are limited to 100V, 300A. The diode turns on and begins to conduct when it is forward biased. When the anode voltage is greater than the cathode voltage diode conducts.

The forward voltage drop of a power diode is low typically 0.5V to 1.2V. If the cathode voltage is higher than its anode voltage then the diode is said to be reverse biased.

Power diodes of high current rating are available in

- Stud or stud-mounted type.
- Disk or press pack or Hockey-pack type.

In a stud mounted type, either the anode or the cathode could be the stud.

COMPARISON BETWEEN DIFFERENT TYPES OF DIODES

General Purpose Diodes	**Fast Recovery Diodes**	**Schottky Diodes**
Upto 5000V & 3500A	Upto 3000V and 1000A	Upto 100V and 300A
Reverse recovery time – High	Reverse recovery time – Low	Reverse recovery time – Extremely low.
$t_{rr} \approx 25ms$	$t_{rr} = 0.1ms$ to $5ms$	t_{rr} = a few nanoseconds
Turn off time - High	Turn off time - Low	Turn off time – Extremely low
Switching frequency – Low	Switching frequency – High	Switching frequency – Very high.
V_F = 0.7V to 1.2V	V_F = 0.8V to 1.5V	$V_F \approx$ 0.4V to 0.6V

Natural or AC line commutated Thyristors are available with ratings upto 6000V, 3500A.

The turn-off time of high speed reverse blocking Thyristors have been improved substantially and now devices are available with t_{OFF} = 10 to 20μsec for a 1200V, 2000A Thyristors.

RCT's (reverse conducting Thyristors) and GATT's (gate assisted turn-off Thyristors) are widely used for high speed switching especially in traction applications. An RCT can be considered as a thyristor with an inverse parallel diode. RCT's are available up to 2500V, 1000A (& 400A in reverse conduction) with a switching time of 40μsec. GATT's are available upto 1200V, 400A with a switching speed of 8μsec. LASCR's which are available upto 6000V, 1500A with a switching speed of 200μsec to 400μsec are suitable for high voltage power systems especially in HVDC.

For low power AC applications, triac's are widely used in all types of simple heat controls, light controls, AC motor controls, and AC switches. The characteristics of triac's are similar to two SCR's connected in inverse parallel and having only one gate terminal. The current flow through a triac can be controlled in either direction.

GTO's & SITH's are self turn-off Thyristors. GTO's & SITH's are turned ON by applying and short positive pulse to the gate and are turned off by applying short negative pulse to the gates. They do not require any commutation circuits.

GTO's are very attractive for forced commutation of converters and are available upto 4000V, 3000A.

SITH's with rating as high as 1200V and 300A are expected to be used in medium power converters with a frequency of several hundred KHz and beyond the frequency range of GTO.

An MCT (MOS controlled thyristor) can be turned ON by a small negative voltage pulse on the MOS gate (with respect to its anode) and turned OFF by a small positive voltage

pulse. It is like a GTO, except that the turn off gain is very high. MCT's are available upto 1000V and 100A.

High power bipolar transistors (high power BJT's) are commonly used in power converters at a frequency below 10KHz and are effectively used in circuits with power ratings upto 1200V, 400A.

A high power BJT is normally operated as a switch in the common emitter configuration.

The forward voltage drop of a conducting transistor (in the ON state) is in the range of 0.5V to 1.5V across collector and emitter. That is $V_{CE} = 0.5V$ to 1.5V in the ON state.

POWER TRANSISTORS

Transistors which have high voltage and high current rating are called power transistors. Power transistors used as switching elements, are operated in saturation region resulting in a low - on state voltage drop. Switching speed of transistors is much higher than the thyristors. And they are extensively used in dc-dc and dc-ac converters with inverse parallel connected diodes to provide bi-directional current flow. However, voltage and current ratings of power transistor are much lower than the thyristors. Transistors are used in low to medium power applications. Transistors are current controlled device and to keep it in the conducting state, a continuous base current is required.

Power transistors are classified as follows

- Bi-Polar Junction Transistors (BJTs)
- Metal-Oxide Semi-Conductor Field Effect Transistors (MOSFETs)
- Insulated Gate Bi-Polar Transistors (IGBTs)
- Static Induction Transistors (SITs)

BI-POLAR JUNCTION TRANSISTOR

A Bi-Polar Junction Transistor is a 3 layer, 3 terminals device. The 3 terminals are base, emitter and collector. It has 2 junctions' collector-base junction (CB) and emitter-base junction (EB). Transistors are of 2 types, NPN and PNP transistors.

The different configurations are common base, common collector and common emitter. Common emitter configuration is generally used in switching applications.

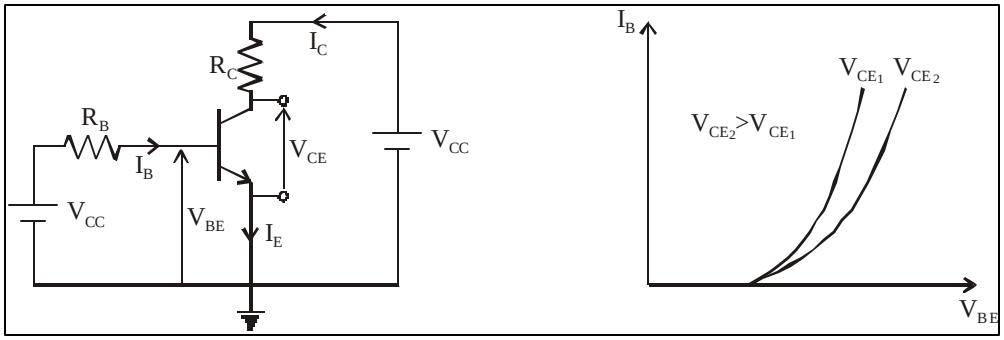


Fig: NPN Transistor

Fig: Input Characteristic

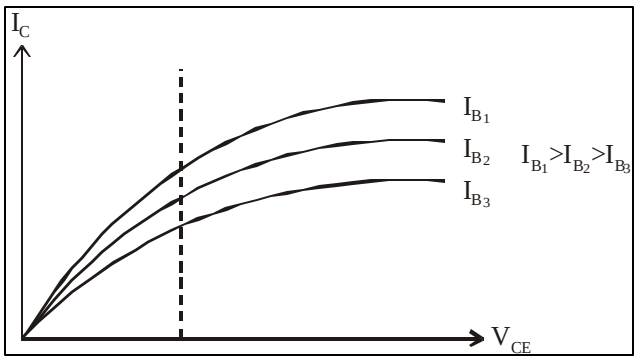


Fig: Output / Collector Characteristics

Transistors can be operated in 3 regions i.e., cut-off, active and saturation.

In the cut-of region transistor is OFF, both junctions (EB and CB) are reverse biased. In the cut-off state the transistor acts as an open switch between the collector and emitter.

In the active region, transistor acts as an amplifier (CB junction is reverse biased and EB junction is forward biased),

In saturation region the transistor acts as a closed switch and both the junctions CB and EB are forward biased.

SWITCHING CHARACTERISTICS

An important application of transistor is in switching circuits. When transistor is used as a switch it is operated either in cut-off state or in saturation state. When the transistor is driven into the cut-off state it operates in the non-conducting state. When the transistor is operated in saturation state it is in the conduction state.

Thus the non-conduction state is operation in the cut-off region while the conducting state is operation in the saturation region.

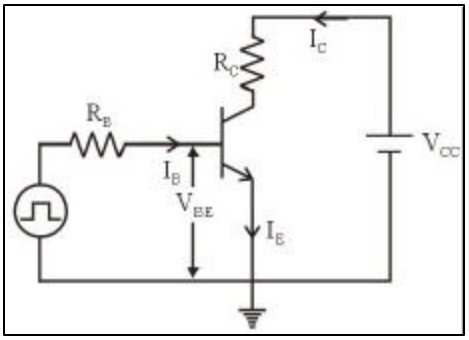


Fig: Switching Transistor in CE Configuration

As the base voltage V_B rises from 0 to V_B, the base current rises to I_B, but the collector current does not rise immediately. Collector current will begin to increase only when the base emitter junction is forward biased and V_{BE} > 0.6V. The collector current I_C will gradually increase towards saturation level $I_{C(sat)}$. The time required for the collector current to rise to 10% of its final value is called delay time t_d. The time taken by the collector current to rise from 10% to 90% of its final value is called rise time t_r. Turn on times is sum of t_d and t_r. $t_{on} = t_d + t_r$

The turn-on time depends on

- Transistor junction capacitances which prevent the transistors voltages from changing instantaneously.
- Time required for emitter current to diffuse across the base region into the collector region once the base emitter junction is forward biased. The turn on time t_{on} ranges from 10 to 300 ns. Base current is normally more than the minimum required to saturate the transistor. As a result excess minority carrier charge is stored in the base region.

When the input voltage is reversed from V_{B1} to $-V_{B2}$ the base current also abruptly changes but the collector current remains constant for a short time interval t_S called the storage time.

The reverse base current helps to discharge the minority charge carries in the base region and to remove the excess stored charge form the base region. Once the excess stored charge is removed the baser region the base current begins to fall towards zero. The fall-time t_f is the time taken for the collector current to fall from 90% to 10% of $I_{C(sat)}$. The turn off time t_{off} is the sum of storage time and the fall time. $t_{off} = t_s + t_f$

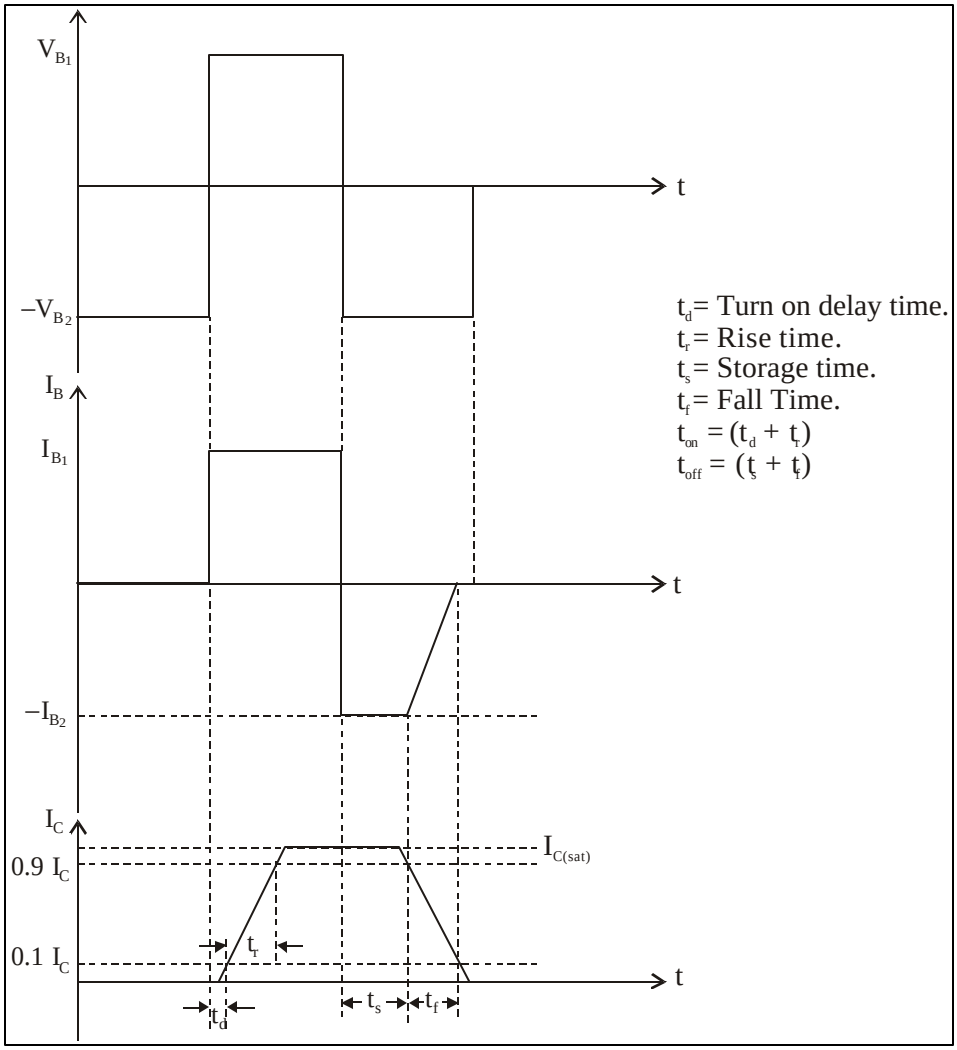


Fig: Switching Times of Bipolar Junction Transistor

DIAC

A diac is a two terminal five layer semi-conductor bi-directional switching device. It can conduct in both directions. The device consists of two p-n-p-n sections in anti parallel as shown in figure. T_1 and T_2 are the two terminals of the device.

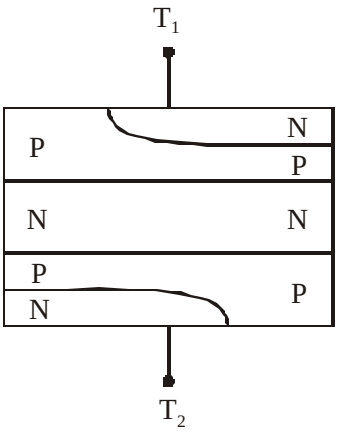


Fig.: Diac Structure

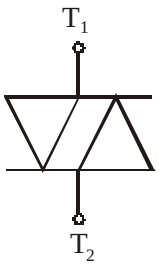


Fig.: Diac symbol

Figure above shows the symbol of diac. Diac will conduct when the voltage applied across the device terminals T_1 & T_2 exceeds the break over voltage..

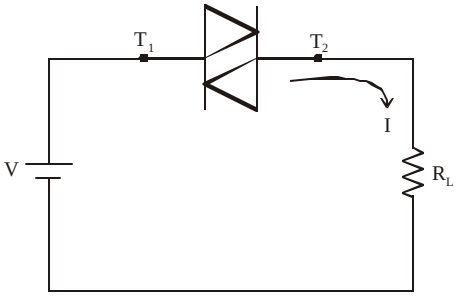


Fig. 1.1

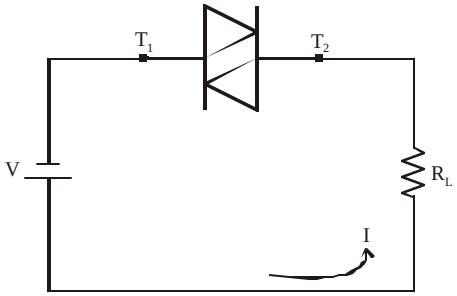


Fig. 1.2

Figure 1.1 shows the circuit diagram with T_1 positive with respect to T_2. When the voltage across the device is less than the break over voltage V_{B01} a very small amount of current called leakage current flows through the device. During this period the device is in non-conducting or blocking mode. But once the voltage across the diac exceeds the break over voltage V_{B01} the diac turns on and begins to conduct. Once it starts conducting the current through diac becomes large and the device current has to be limited by connecting an external load resistance R_L, at the same time the voltage across the diac decreases in the conduction state. This explain the forward characteristics.

Figure 1.2 shows the circuit diagram with T_2 positive with respect to T_1. The reverse characteristics obtained by varying the supply voltage are identical with the forward characteristic as the device construction is symmetrical in both the directions.

In both the cases the diac exhibits negative resistance switching characteristic during conduction. i.e., current flowing through the device increases whereas the voltage across it decreases.

Figure below shows forward and reverse characteristics of a diac. Diac is mainly used for triggering triacs.

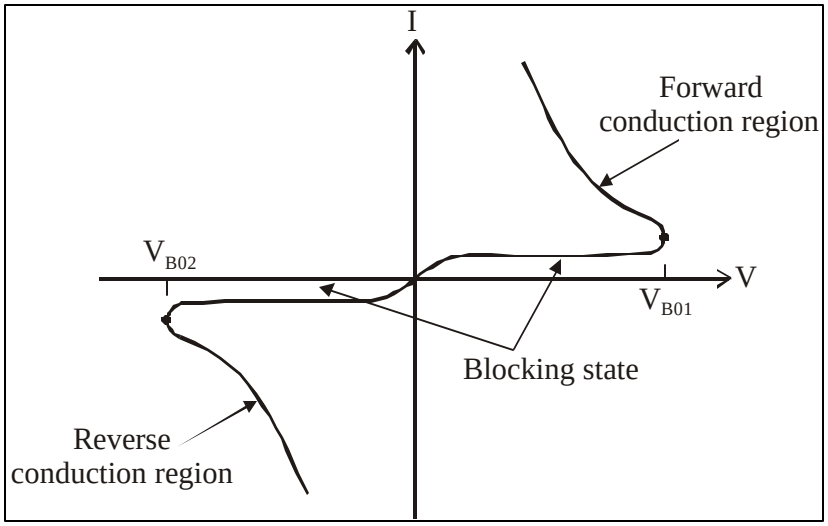


Fig.: Diac Characteristics

TRIAC

A triac is a three terminal bi-directional switching thyristor device. It can conduct in both directions when it is triggered into the conduction state. The triac is equivalent to two SCRs connected in anti-parallel with a common gate. Figure below shows the triac structure. It consists of three terminals viz., MT_2 , MT_1 and gate G.

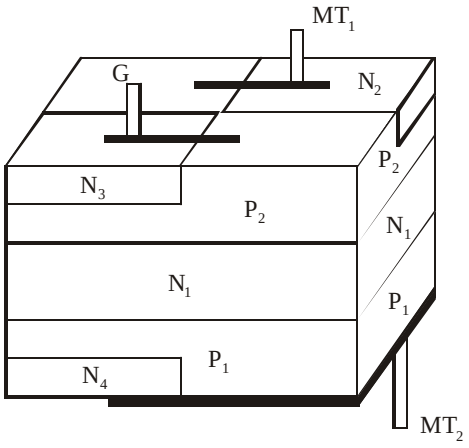


Fig. : Triac Structure

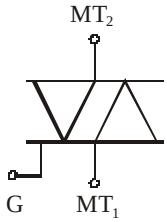


Fig. : Triac Symbol

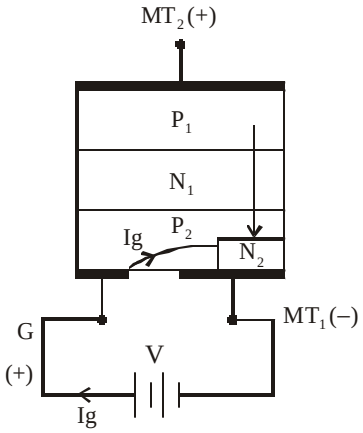
The gate terminal G is near the MT_1 terminal. Figure above shows the triac symbol. MT_1 is the reference terminal to obtain the characteristics of the triac. A triac can be operated in four different modes depending upon the polarity of the voltage on the terminal MT_2 with respect to MT_1 and based on the gate current polarity.

The characteristics of a triac is similar to that of an SCR, both in blocking and conducting states. A SCR can conduct in only one direction whereas triac can conduct in both directions.

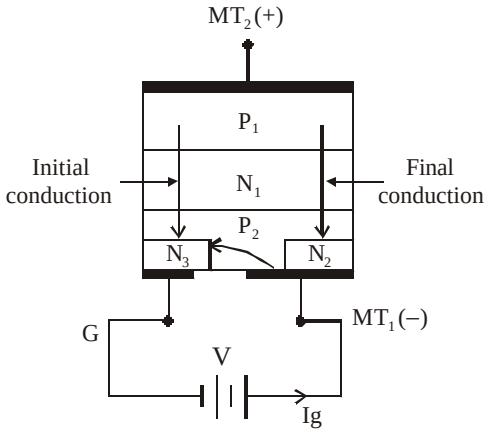
TRIGGERING MODES OF TRIAC

MODE 1 : MT_2 **positive, Positive gate current (**I^+ **mode of operation)**

When MT_2 and gate current are positive with respect to MT_1, the gate current flows through P_2-N_2 junction as shown in figure below. The junction P_1-N_1 and P_2-N_2 are forward biased but junction N_1-P_2 is reverse biased. When sufficient number of charge carriers are injected in P_2 layer by the gate current the junction N_1-P_2 breakdown and triac starts conducting through $P_1N_1P_2N_2$ layers. Once triac starts conducting the current increases and its V-I characteristics is similar to that of thyristor. Triac in this mode operates in the first-quadrant.



MODE 2 : MT_2 positive, Negative gate current (I^- mode of operation)

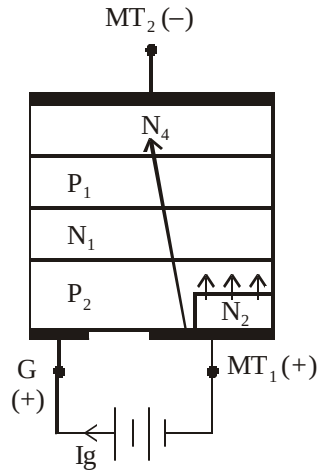


When MT_2 is positive and gate G is negative with respect to MT_1 the gate current flows through P_2-N_3 junction as shown in figure above. The junction P_1-N_1 and P_2-N_3 are forward biased but junction N_1-P_2 is reverse biased. Hence, the triac initially starts conducting through $P_1N_1P_2N_3$ layers. As a result the potential of layer between P_2-N_3 rises towards the potential of MT_2. Thus, a potential gradient exists across the layer P_2 with left hand region at a higher potential than the right hand region. This results in a current flow in P_2 layer from left to right, forward biasing the P_2N_2 junction. Now the right hand portion P_1-N_1 - P_2-N_2 starts conducting. The device operates in first quadrant. When compared to Mode 1, triac with MT_2 positive and negative gate current is less sensitive and therefore requires higher gate current for triggering.

MODE 3 : MT_2 negative, Positive gate current (III^+ mode of operation)

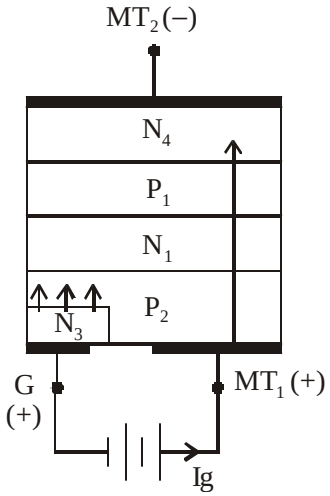
When MT_2 is negative and gate is positive with respect to MT_1 junction P_2N_2 is forward biased and junction P_1-N_1 is reverse biased. N_2 layer injects electrons into P_2 layer as shown by arrows in figure below. This causes an increase in current flow through junction P_2-N_1. Resulting in breakdown of reverse biased junction N_1-P_1. Now the

device conducts through layers $P_2N_1P_1N_4$ and the current starts increasing, which is limited by an external load.



The device operates in third quadrant in this mode. Triac in this mode is less sensitive and requires higher gate current for triggering.

MODE 4 : MT_2 negative, Negative gate current (*III*⁻ mode of operation)



In this mode both MT_2 and gate G are negative with respect to MT_1, the gate current flows through P_2N_3 junction as shown in figure above. Layer N_3 injects electrons as shown by arrows into P_2 layer. This results in increase in current flow across P_1N_1 and the device will turn ON due to increased current in layer N_1. The current flows through layers $P_2N_1P_1N_4$. Triac is more sensitive in this mode compared to turn ON with positive gate current. (Mode 3).

Triac sensitivity is greatest in the first quadrant when turned ON with positive gate current and also in third quadrant when turned ON with negative gate current. when MT_2 is positive with respect to MT_1 it is recommended to turn on the triac by a positive gate current. When MT_2 is negative with respect to MT_1 it is recommended to turn on the triac

by negative gate current. Therefore Mode 1 and Mode 4 are the preferred modes of operation of a triac (I^+ mode and III^- mode of operation are normally used).

TRIAC CHARACTERISTICS

Figure below shows the circuit to obtain the characteristics of a triac. To obtain the characteristics in the third quadrant the supply to gate and between MT_2 and MT_1 are reversed.

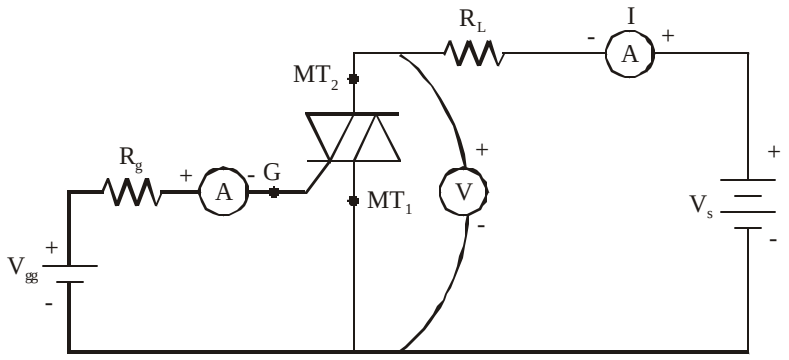


Figure below shows the V-I Characteristics of a triac. Triac is a bidirectional switching device. Hence its characteristics are identical in the first and third quadrant. When gate current is increased the break over voltage decreases.

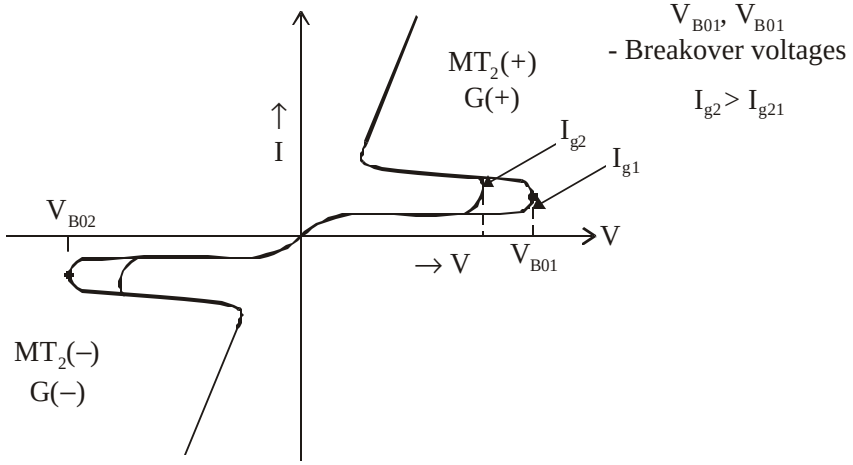


Fig.: Triac Characteristic

Triac is widely used to control the speed of single phase induction motors. It is also used in domestic lamp dimmers and heat control circuits, and full wave AC voltage controllers.

POWER MOSFET

Power MOSFET is a metal oxide semiconductor field effect transistor. It is a voltage controlled device requiring a small input gate voltage. It has high input impedance. MOSFET is operated in two states viz., ON STATE and OFF STATE. Switching speed of MOSFET is very high. Switching time is of the order of nanoseconds.

MOSFETs are of two types

- Depletion MOSFETs
- Enhancement MOSFETs.

MOSFET is a three terminal device. The three terminals are gate (G), drain (D) and source (S).

DEPLETION MOSFET

Depletion type MOSFET can be either a n-channel or p-channel depletion type MOSFET.

A depletion type n-channel MOSFET consists of a p-type silicon substrate with two highly doped n^+ silicon for low resistance connections. A n-channel is diffused between drain and source. Figure below shows a n-channel depletion type MOSFET. Gate is isolated from the channel by a thin silicon dioxide layer.

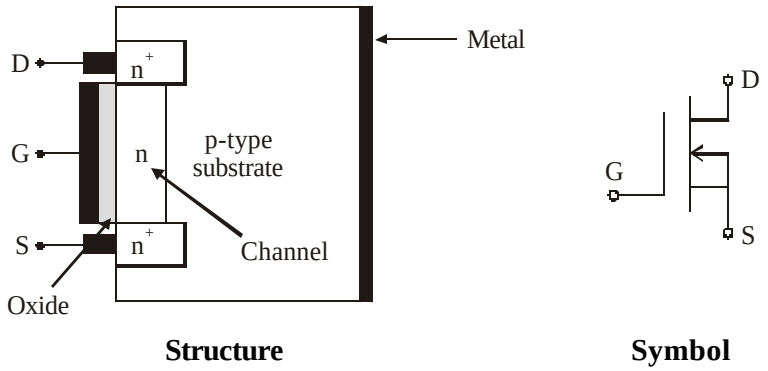


Fig. : n-channel depletion type MOSFET

Gate to source voltage (V_{GS}) can be either positive or negative. If V_{GS} is negative, electrons present in the n-channel are repelled leaving positive ions. This creates a depletion.

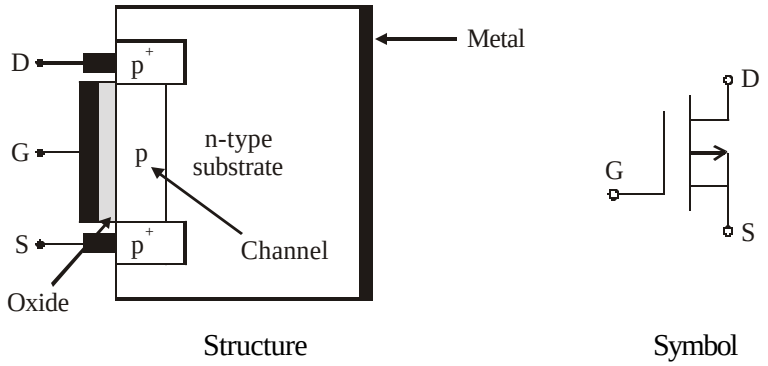


Fig. : P-channel depletion type MOSFET

Figure above shows a p-channel depletion type MOSFET. A P-channel depletion type MOSFET consists of a n-type substrate into which highly doped p-regions and a P-channel are diffused. The two P^+ regions act as drain and source P-channel operation is same except that the polarities of voltages are opposite to that of n-channel.

ENHANCEMENT MOSFET

Enhancement type MOSFET has no physical channel. Enhancement type MOSFET can be either a n-channel or p-channel enhancement type MOSFET.

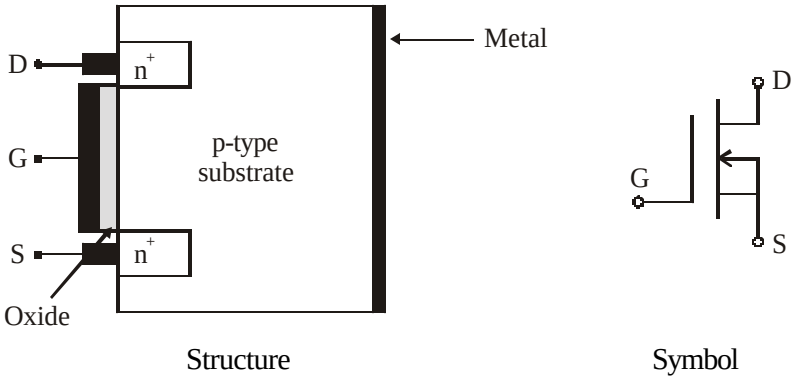


Fig. : n-channel enhancement type MOSFET

Figure above shows a n-channel enhancement type MOSFET. The P-substrate extends upto the silicon dioxide layer. The two highly doped n regions act as drain and source.

When gate is positive (V_{GS}) free electrons are attracted from P-substrate and they collect near the oxide layer. When gate to source voltage, V_{GS} becomes greater than or equal to a value called threshold voltage (V_T). Sufficient numbers of electrons are accumulated to form a virtual n-channel and current flows from drain to source.

Figure below shows a p-channel enhancement type of MOSFET. The n-substrate extends upto the silicon dioxide layer. The two highly doped P regions act as drain and source. For p-channel the polarities of voltages are opposite to that of n-channel.

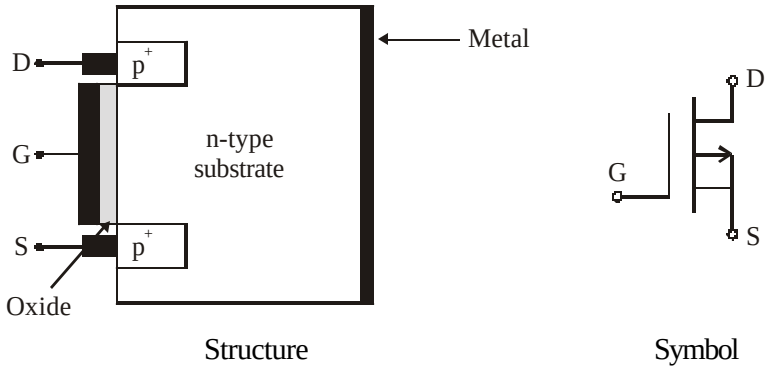


Fig. : P-channel enhancement type MOSFET.

CHARACTERISTICS OF MOSFET

Depletion MOSFET

Figure below shows n-channel depletion type MOSFET with gate positive with respect to source. I_D, V_{DS} and V_{GS} are drain current, drain source voltage and gate-source voltage. A plot of variation of I_D with V_{DS} for a given value of V_{GS} gives the Drain characteristics or Output characteristics.

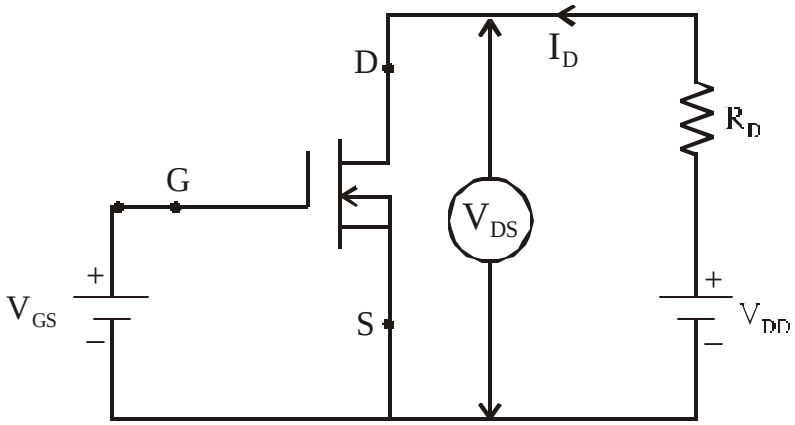


Fig: n-channel Depletion MOSFET

n-channel Depletion type MOSFET

V_{GS} & V_{DS} are positive. I_D is positive for n channel MOSFET . V_{GS} is negative for depletion mode. V_{GS} is positive for enhancement mode.

Figure below shows the drain characteristic. MOSFET can be operated in three regions

- Cut-off region,
- Saturation region (pinch-off region) and
- Linear region.

In the linear region I_D varies linearly with V_{DS}. i.e., increases with increase in V_{DS}. Power MOSFETs are operated in the linear region for switching actions. In saturation region I_D almost remains constant for any increase in V_{DS}.

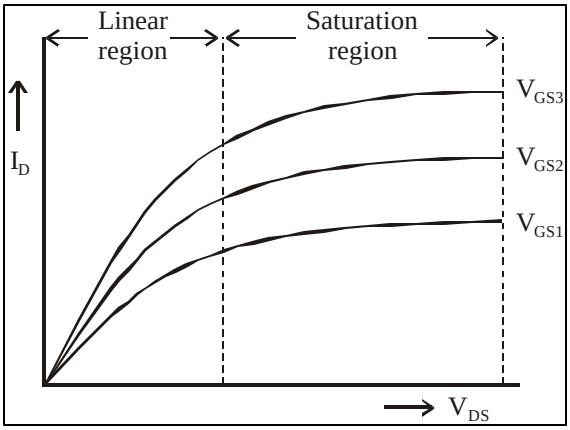


Fig.: Drain Characteristic

Figure below shows the transfer characteristic. Transfer characteristic gives the variation of I_D with V_{GS} for a given value of V_{DS}. I_{DSS} is the drain current with shorted gate. As curve extends on both sides V_{GS} can be negative as well as positive.

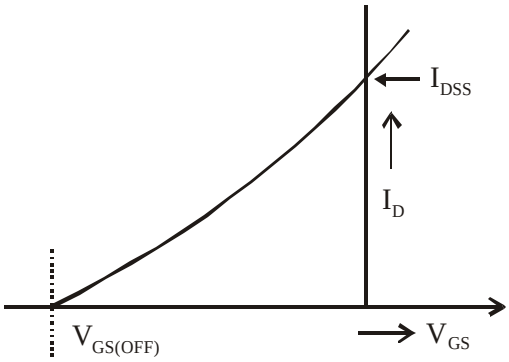


Fig.: Transfer characteristic

Enhancement MOSFET

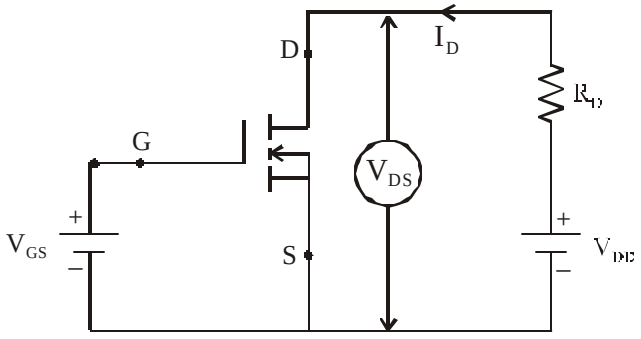
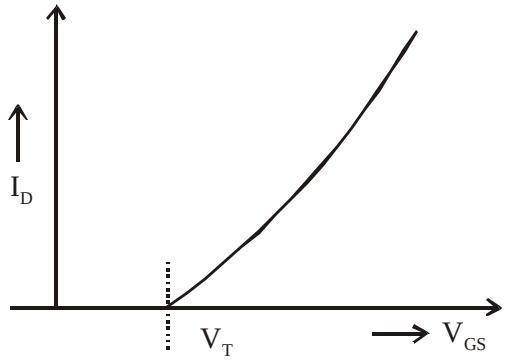


Fig: n-channel Enhancement MOSFET

Enhancement type MOSFET

V_{GS} is positive for a n-channel enhancement MOSFET. V_{DS} & I_D are also positive for n channel enhancement MOSFET

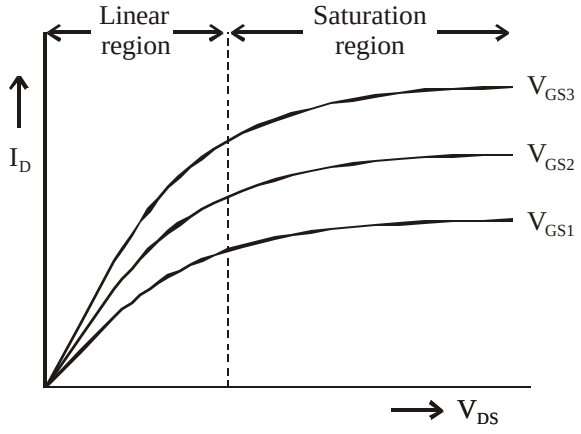
Figure above shows circuit to obtain characteristic of n channel enhancement type MOSFET. Figure below shows the drain characteristic. Drain characteristic gives the variation of I_D with V_{DS} for a given value of V_{GS} .



$V_T = V_{GS(TH)}$ = Gate Source Threshold Voltage

Fig.: Transfer Characteristic

Figure below shows the transfer characteristic which gives the variation of I_D with V_{GS} for a given value of V_{DS} .



$V_{GS3} > V_{GS2} > V_{GS1}$

Fig. : Drain Characteristic

MOSFET PARAMETERS

The parameters of MOSFET can be obtained from the graph as follows.

Mutual Transconductance $g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right/ V_{DS} = \text{Constant}$.

Output or Drain Resistance $R_{ds} = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right/ V_{GS} = \text{Constant}$.

Amplification factor $m = R_{ds}$ x g_m

Power MOSFETs are generally of enhancement type. Power MOSFETs are used in switched mode power supplies.

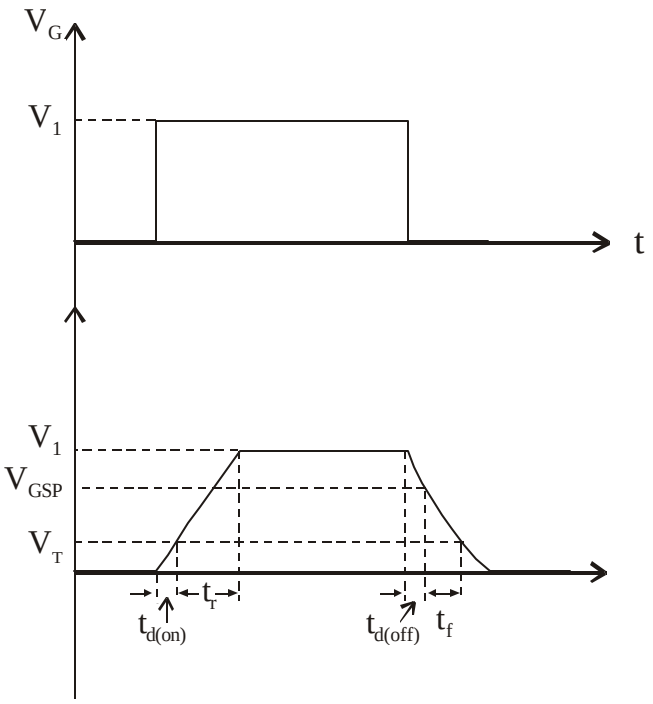
Power MOSFET's are used in high speed power converters and are available at a relatively low power rating in the range of 1000V, 50A at a frequency range of several tens of KHz $(f_{\max} = 100KHz)$.

SWITCHING CHARACTERISTICS OF MOSFET

Power MOSFETs are often used as switching devices. The switching characteristic of a power MOSFET depends on the capacitances between gate to source C_{GS}, gate to drain C_{GD} and drain to source C_{GS}. It also depends on the impedance of the gate drive circuit. During turn-on there is a turn-on delay $t_{d(on)}$, which is the time required for the input capacitance C_{GS} to charge to threshold voltage level V_T . During the rise time t_r, C_{GS} charges to full gate voltage V_{GSP} and the device operate in the linear region (ON state). During rise time t_r drain current I_D rises from zero to full on state current I_D.

- Total turn-on time, $t_{on} = t_{d(on)} + t_r$

MOSFET can be turned off by discharging capacitance C_{GS}. $t_{d(off)}$ is the turn-off delay time required for input capacitance C_{GS} to discharge from V_1 to V_{GSP}. Fall time t_f is the time required for input capacitance to discharge from V_{GSP} to threshold voltage V_T . During fall time t_f drain current falls from I_D to zero. Figure below shows the switching waveforms of power MOSFET.


V_G
V_1
t
V_1
V_GSP
V_T
t_r
t_d(on)
t_d(off)
t_f

INSULATED GATE BIPOLAR TRANSISTOR (IGBT)

IGBT is a voltage controlled device. It has high input impedance like a MOSFET and low on-state conduction losses like a BJT.

Figure below shows the basic silicon cross-section of an IGBT. Its construction is same as power MOSFET except that n^+ layer at the drain in a power MOSFET is replaced by P^+ substrate called collector.

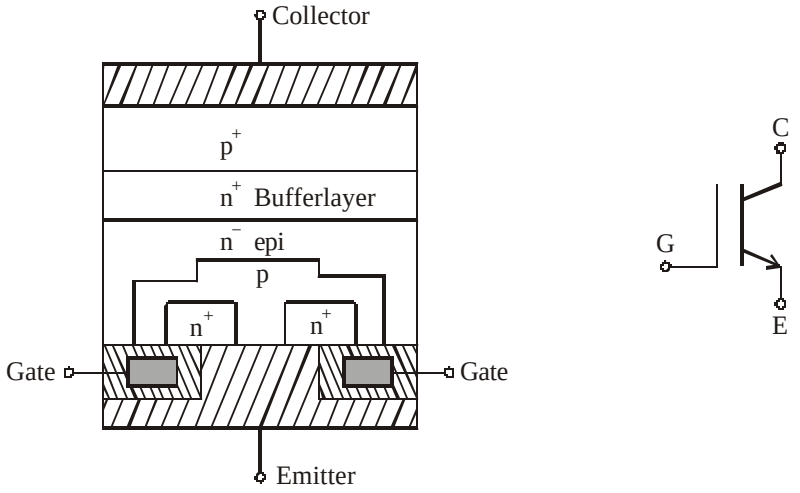


Fig.: Insulated Gate Bipolar Transistor

IGBT has three terminals gate (G), collector (C) and emitter (E). With collector and gate voltage positive with respect to emitter the device is in forward blocking mode. When gate to emitter voltage becomes greater than the threshold voltage of IGBT, a n-channel is formed in the P-region. Now device is in forward conducting state. In this state p^+ substrate injects holes into the epitaxial n^- layer. Increase in collector to emitter voltage will result in increase of injected hole concentration and finally a forward current is established.

CHARACTERISTIC OF IGBT

Figure below shows circuit diagram to obtain the characteristic of an IGBT. An output characteristic is a plot of collector current I_C versus collector to emitter voltage V_{CE} for given values of gate to emitter voltage V_{GE}.

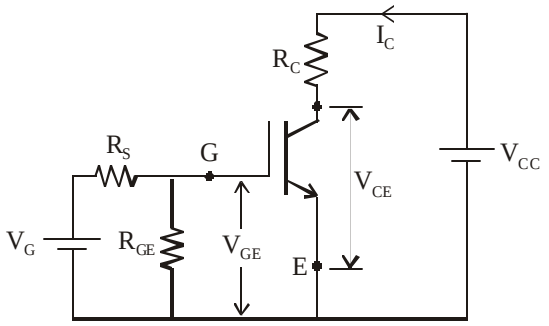


Fig.: Circuit Diagram to Obtain Characteristics

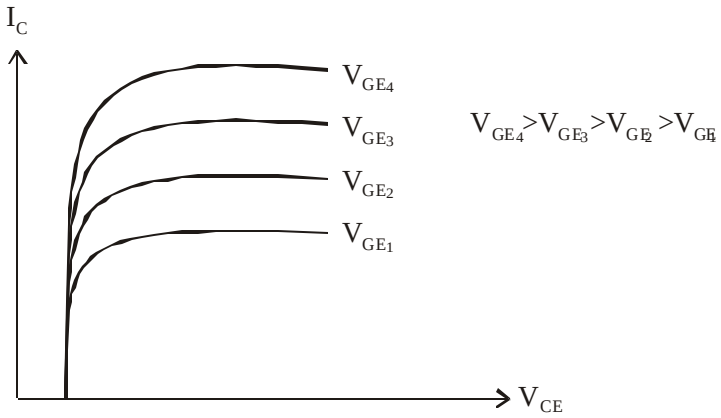


Fig. : Output Characteristics

A plot of collector current I_C versus gate-emitter voltage V_{GE} for a given value of V_{CE} gives the transfer characteristic. Figure below shows the transfer characteristic.

Note

Controlling parameter is the gate-emitter voltage V_{GE} in IGBT. If V_{GE} is less than the threshold voltage V_T then IGBT is in OFF state. If V_{GE} is greater than the threshold voltage V_T then the IGBT is in ON state.

IGBTs are used in medium power applications such as ac and dc motor drives, power supplies and solid state relays.

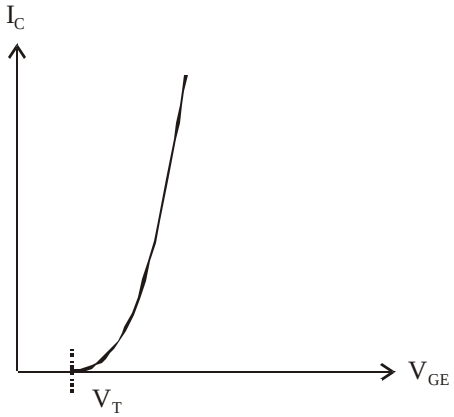


Fig. : Transfer Characteristic

SWITCHING CHARACTERISTIC OF IGBT

Figure below shows the switching characteristic of an IGBT. Turn-on time consists of delay time $t_{d(on)}$ and rise time t_r.

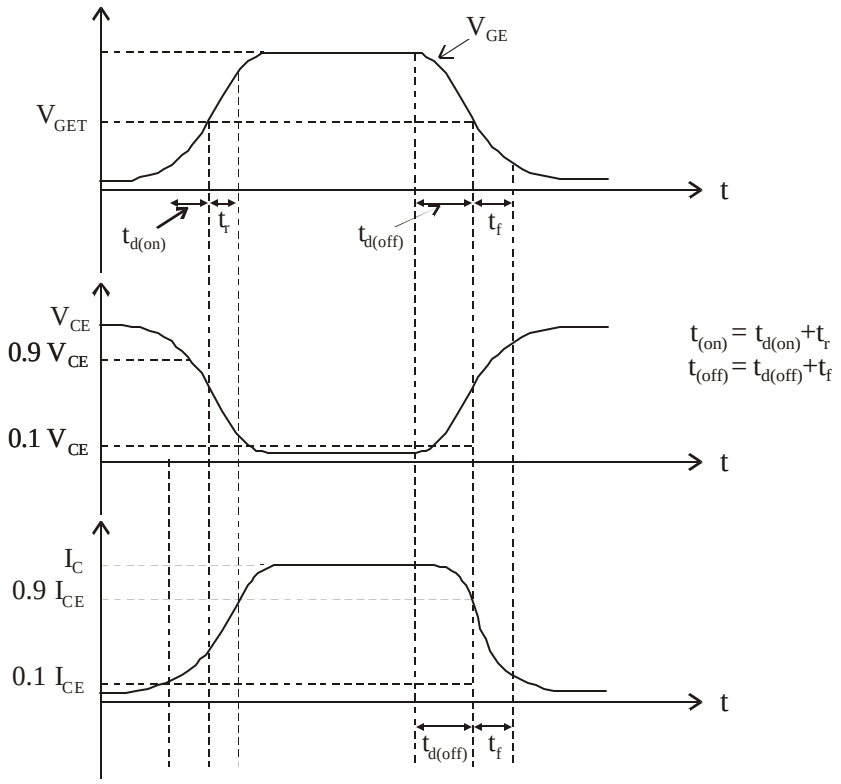


Fig.: Switching Characteristics

The turn on delay time is the time required by the leakage current I_{CE} to rise to $0.1I_C$, where I_C is the final value of collector current. Rise time is the time required for collector current to rise from 0.1 I_C to its final value I_C. After turn-on collector-emitter voltage V_{CE} will be very small during the steady state conduction of the device.

The turn-off time consists of delay off time $t_{d(off)}$ and fall time t_f. Off time delay is the time during which collector current falls from I_C to 0.9 I_C and V_{GE} falls to threshold voltage V_{GET}. During the fall time t_f the collector current falls from $0.90I_C$ to $0.1I_C$. During the turn-off time interval collector-emitter voltage rises to its final value V_{CE}.

IGBT's are voltage controlled power transistor. They are faster than BJT's, but still not quite as fast as MOSFET's. the IGBT's offer for superior drive and output characteristics when compared to BJT's. IGBT's are suitable for high voltage, high current and frequencies upto 20KHz. IGBT's are available upto 1400V, 600A and 1200V, 1000A.

IGBT APPLICATIONS

Medium power applications like DC and AC motor drives, medium power supplies, solid state relays and contractors, general purpose inverters, UPS, welder equipments, servo controls, robotics, cutting tools, induction heating

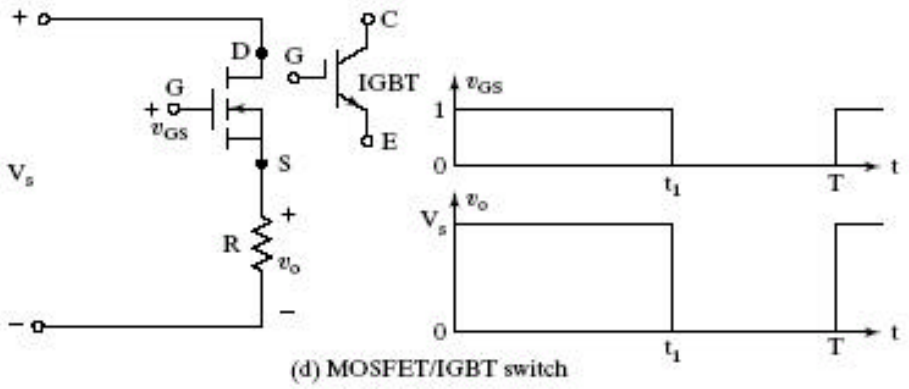
TYPICAL RATINGS OF IGBT

Voltage rating = 1400V. Current rating = 600A. Maximum operating frequency = 20KHz. Switching time $\approx 2.3ms$ $(t_{ON} \approx t_{OFF})$. ON state resistance = 600mΩ = $60x10^{-3}\Omega$.

POWER MOSFET RATINGS

Voltage rating = 500V. Current rating = 50A. Maximum operating frequency = 100KHz. Switching time $\approx 0.6ms$ to $1ms$ $(t_{ON} \approx t_{OFF})$. ON state resistance $R_{D(ON)}$ = 0.4mΩ to $0.6m\Omega$.

A MOSFET/ IGBT SWITCH



(d) MOSFET/IGBT switch

MOSFET / IGBT can be used as a switch in the circuit shown above. If a n-channel enhancement MOSFET is used then the input pulse is V_{GS} which is the pulse applied between gate and source, which is a positive going voltage pulse.

IGBT's

Minority carrier devices, superior conduction characteristics, ease of drive, wide SOA, peak current capability and ruggedness. Generally the switching speed of an IGBT is inferior to that of a power MOSFET.

POWER MOSFET'S (MAJORITY CARRIER DEVICES)

Higher switching speed, peak current capability, ease of drive, wide SOA, avalanche and $\frac{d_v}{d_t}$ capability have made power MOSFET is the ideal choice in new power electronic circuit designs.

IGBT (INSULATED GATE BIPOLAR TRANSISTORS) FEATURES

IGBT combines the advantages of BJT's and MOSFET's. Features of IGBT are

- IGBT has high input impedance like MOSFET's.
- Low ON state conduction power losses like BJT's.
- There is no secondary breakdown problem like BJT's.
- By chip design and structure design, the equivalent drain to source resistance R_{DS} is controlled to behave like that of BJT.

DATA SHEET DETAILS OF THE IGBT MODULE CM400HA-24H

High power switching device by Mitsubishi Semiconductors Company $I_C = 400A, V_{CES} = 1200V$.

APPLICATIONS OF IGBT CM400HA-24H

AC and DC motor controls, general purpose inverters, UPS, welders, servo controls, numeric control, robotics, cutting tools, induction heating.

MAXIMUM RATINGS

V_{CES}	Collector-Emitter (G-E short) voltage	1200V
V_{GES}	Gate-Emitter (C-E short) voltage	$\pm 20V$.
I_C	Collector Current (steady / average current)	400A, at $T_C = 25^0 C$.
I_{CM}	Pulsed Collector Current	800A
I_E	Emitter Current	400A, at $T_C = 25^0 C$.
I_{EM}	Maximum Pulsed Emitter Current	800A
$P_{C(\max)}$	Maximum Collector Power Dissipation	2800W, at $T_C = 25^0 C$.
$T_{storage}$	Maximum Storage Temperature	$-40^0 c$ to $125^0 c$
T_J	Junction Temperature	$-40^0 c$ to $150^0 c$
Weight Typical Value		400gm (0.4Kg)
Electrical Characteristics		$T_J = 25^0 c$
$V_{GE_{(TH)}} = V_{TH} = Gate-Emitter$ Threshold Voltage.		$V_{GE_{(TH)}} = 6V\,(Typ)$.
$V_{GE_{(TH)}} = 4.5V\,(\min)$ to 7.5V maximum at $I_C = 40mA$ and $V_{CE} = 10V$.		
I_{CES}	Collector cut-off current = 2mA (maximum) at $V_{CE} = V_{CES}, V_{GE} = 0$	
I_{GES}	Gate leakage current $= 0.5mA$ (maximum) at $V_{GE} = V_{GES}, V_{CE} = 0$	

$V_{CE(sat)}$ Collector-Emitter saturation voltage $\left(T_J = 25^0 C, I_C = 400A, V_{GE} = 15V\right)$

$V_{CE(sat)}$: 2.5V (typical), 3.5V (maximum)

$t_{d_{(ON)}}$ Turn ON delay time 300nsec (maximum) at $V_{CC} = 600V$, $I_C = 400A$.

t_r Turn ON rise time 500nsec (maximum), at $V_{GE1} = V_{GE2} = 15V$.

$t_{ON} = 800ns\left(\max\right) = \left(t_d + t_r\right)$

$t_{d(OFF)}$ Turn off delay time = 350nsec.

t_f Turn off fall time = 350nsec.

$t_{OFF} = t_{d(OFF)} + t_f = 700n\sec$ (maximum)

t_{rr} Reverse recovery time 250nsec.

Q_{rr} Reverse recovery charge = 2.97μc (typical).

CHARACTERISTICS OF THE EMITTER TO COLLECTOR FWD CM 400HA-24H IGBT CHARACTERISTICS

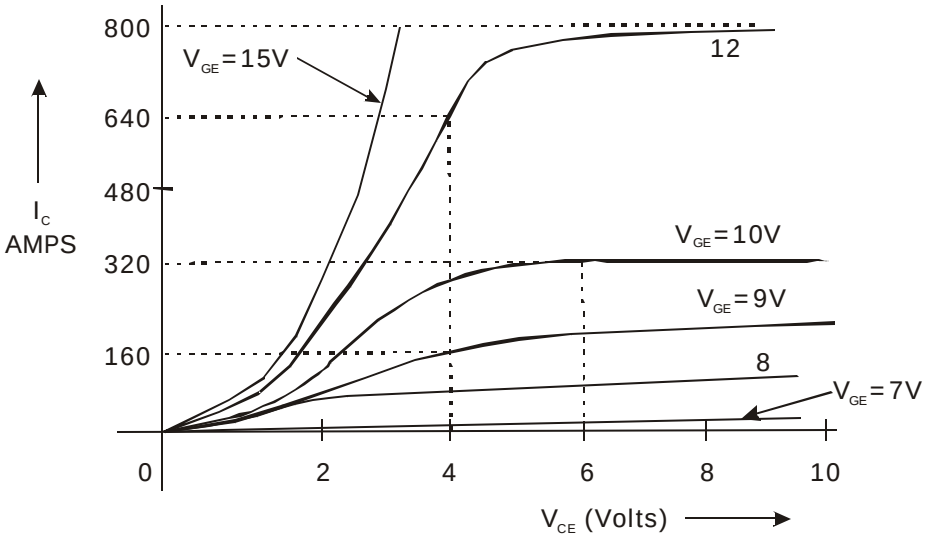


Fig: Output Collector Characteristics

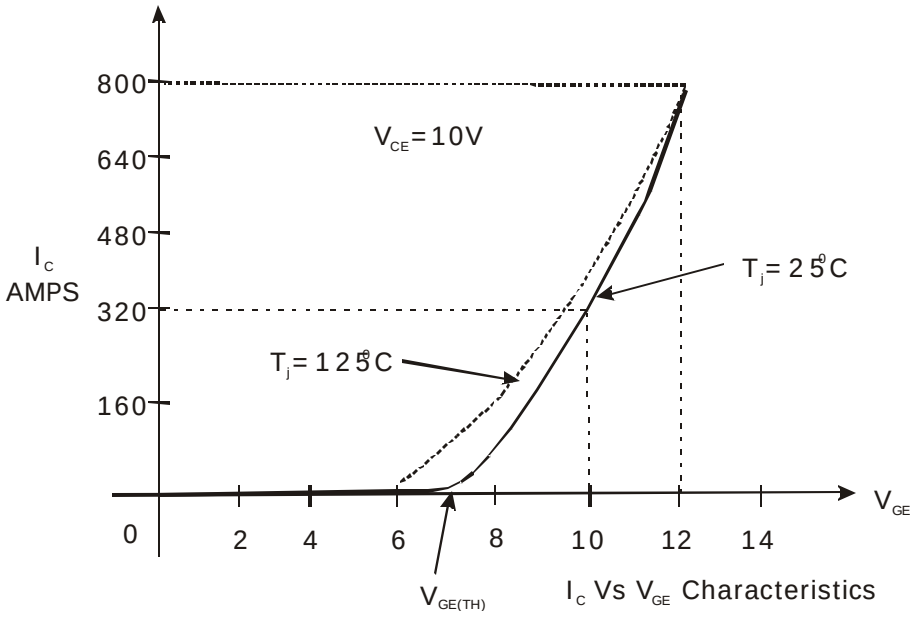
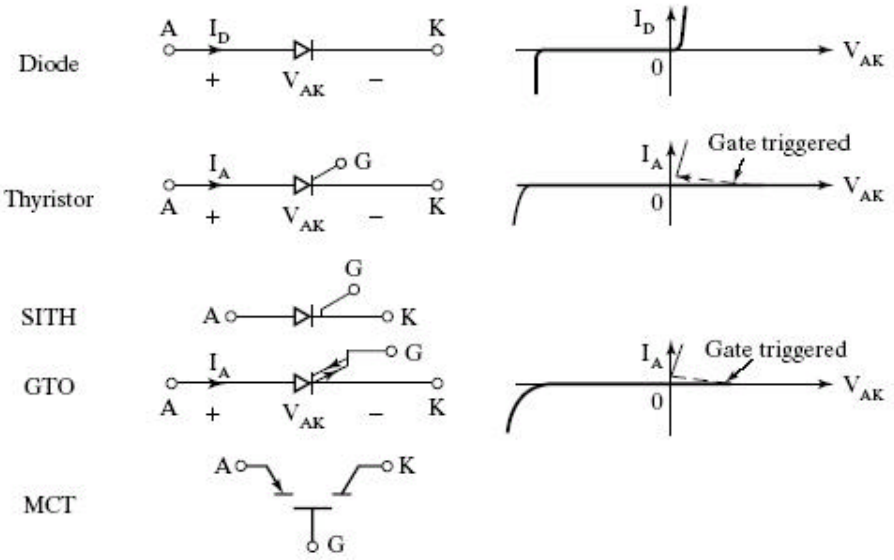
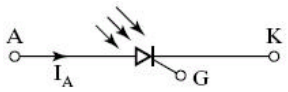


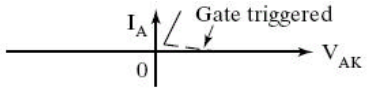
Fig: Transfer Characteristics

POWER SEMICONDUCTOR DEVICES, THEIR SYMBOLS AND CHARACTERISTICS

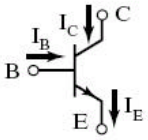


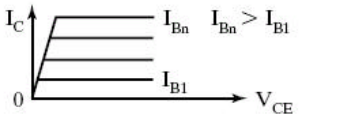
LASCR



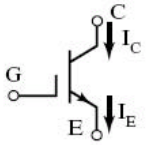


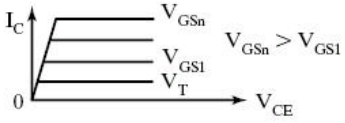
NPN BJT



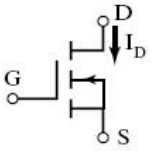


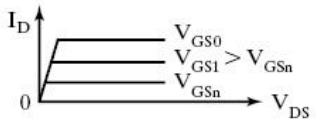
IGBT



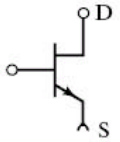


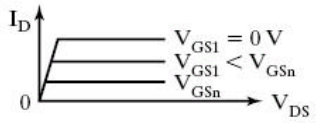
N-Channel MOSFET





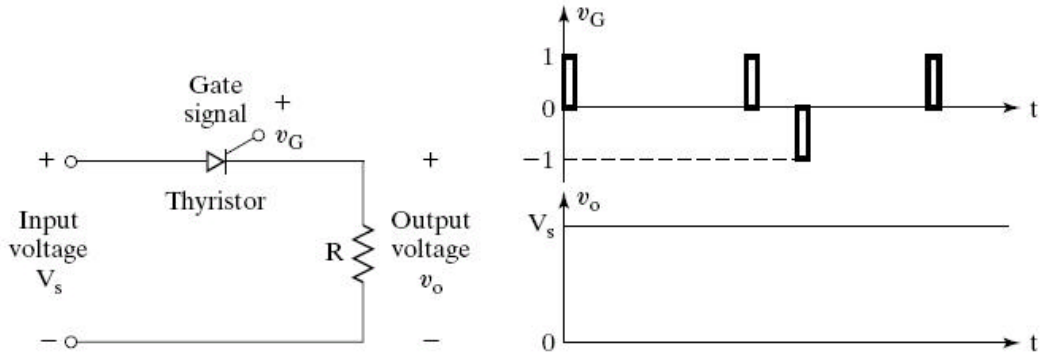
SIT



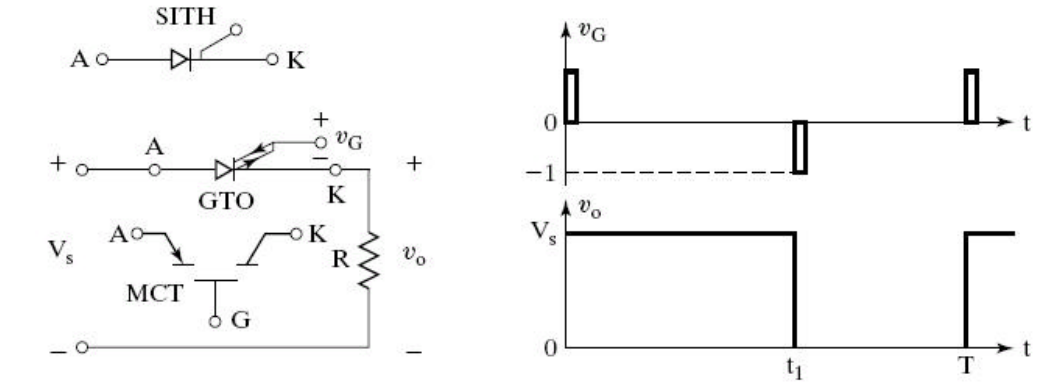


CONTROL CHARACTERISTICS OF POWER DEVICES

The power semiconductor devices can be operated as switches by applying control signals to the gate terminal of Thyristors (and to the base of bi-polar transistor). The required output is obtained by varying the conduction time of these switching devices. Figure below shows the output voltages and control characteristics of commonly used power switching devices. Once a thyristor is in a conduction mode, the gate signal of either positive or negative magnitude has no effect. When a power semiconductor device is in a normal conduction mode, there is a small voltage drop across the device. In the output voltage waveforms shown, these voltage drops are considered negligible.



(a) Thyristor switch



(b) GTO/MTO/ETO/IGCT/MCT/SITH switch (For MCT, the polarity of V_G is reversed as shown)

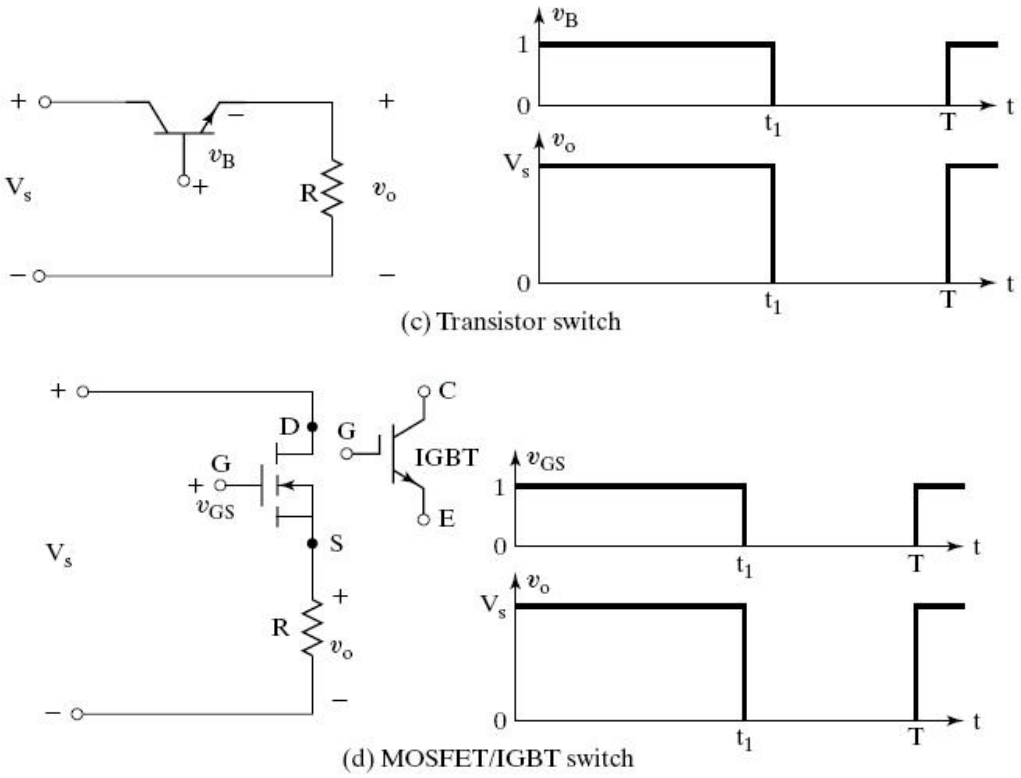


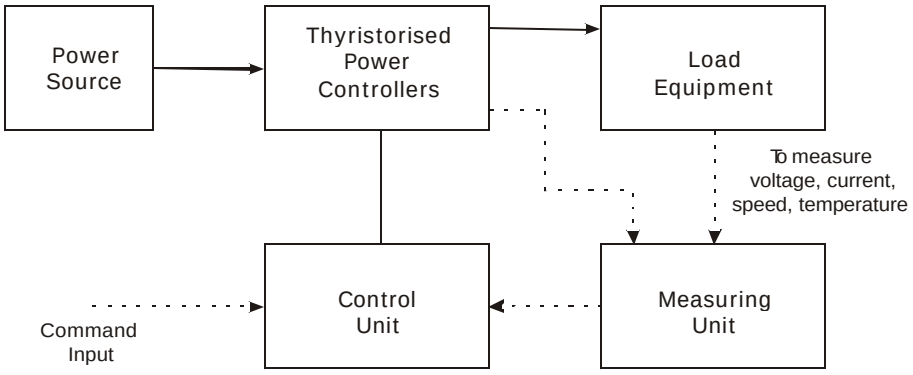
Fig: Control Characteristics of Power Switching Devices

The power semiconductor switching devices can be classified on the basis of

- Uncontrolled turn on and turn off (e.g.: diode).
- Controlled turn on and uncontrolled turn off (e.g. SCR)
- Controlled turn on and off characteristics (e.g. BJT, MOSFET, GTO, SITH, IGBT, SIT, MCT).
- Continuous gate signal requirement (e.g. BJT, MOSFET, IGBT, SIT).
- Pulse gate requirement (e.g. SCR, GTO, MCT).
- Bipolar voltage withstanding capability (e.g. SCR, GTO).
- Unipolar voltage withstanding capability (e.g. BJT, MOSFET, GTO, IGBT, MCT).
- Bidirectional current capability (e.g.: Triac, RCT).
- Unidirectional current capability (e.g. SCR, GTO, BJT, MOSFET, MCT, IGBT, SITH, SIT & Diode).

THYRISTORISED POWER CONTROLLERS

Block diagram given below, shows the system employing a thyristorised power controller. The main power flow between the input power source and the load is shown by solid lines.



Thyristorised power controllers are widely used in the industry. Old/conventional controllers including magnetic amplifiers, mercury arc rectifiers, thyratrons, ignitrons, rotating amplifiers, resistance controllers have been replaced by thyristorised power controllers in almost all the applications.

A typical block diagram of a thyristorised power converter is shown in the above figure.

The thyristor power converter converts the available power from the source into a suitable form to run the load or the equipment. For example the load may be a DC motor drive which requires DC voltage for its operation. The available power supply is AC power supply as is often the case. The thyristor power converter used in this case is a AC to DC power converter which converts the input AC power into DC output voltage to feed to the DC motor. Very often a measuring unit or an instrumentation unit is used so as to measure and monitor the output parameters like the output voltage, the load current, the speed of the motor or the temperature etc. The measuring unit will be provided with meters and display devices so that the output parameters can be seen and noted. The control unit is employed to control the output of the thyristorised power converter so as to adjust the output voltage / current to the desired value to obtain optimum performance of the load or equipment. The signal from the control unit is used to adjust the phase angle / trigger angle of the Thyristors in the power controller so as to vary the output voltage to the desired value.

SOME IMPORTANT APPLICATIONS OF THYRISTORISED POWER CONTROLLERS

- Control of AC and DC motor drives in rolling mills, paper and textile mills, traction vehicles, mine winders, cranes, excavators, rotary kilns, ventilation fans, compression etc.
- Uninterruptible and stand by power supplies for critical loads such as computers, special high tech power supplies for aircraft and space applications.

- Power control in metallurgical and chemical processes using arc welding, induction heating, melting, resistance heating, arc melting, electrolysis, etc.
- Static power compensators, transformer tap changers and static contactors for industrial power systems.
- Power conversion at the terminals of a HVDC transmission systems.
- High voltage supplies for electrostatic precipitators and x-ray generators.
- Illumination/light control for lighting in stages, theaters, homes and studios.
- Solid state power controllers for home/domestic appliances.

ADVANTAGES OF THYRISTORISED POWER CONTROLLERS

- High efficiency due to low losses in the Thyristors.
- Long life and reduced/minimal maintenance due to the absence of mechanical wear.
- Control equipments using Thyristors are compact in size.
- Easy and flexibility in operation due to digital controls.
- Faster dynamic response compared to the electro mechanical converters.
- Lower acoustic noise when compared to electro magnetic controllers, relays and contactors.

DISADVANTAGES OF THYRISTORISED POWER CONTROLLERS

- All the thyristorised power controllers generate harmonics (unwanted frequency components) due to the switching ON and OFF of the thyristors. These harmionics adversely affect the performance of the load connected to them. For example when the load are motors, there are additional power losses (harmonic power loss) torque harmonics, and increase in acoustic noise.
- The generated harmonics are injected into the supply lines and thus adversely affect the other loads/equipments connected to the supply lines.
- In some applications example: traction, there is interference with the commutation circuits due to the power supply line harmonics and due to electromagnetic radiation.
- The thyristorised AC to DC converters and AC to AC converters can operate at low power factor under some conditions.
- Special steps are then taken for correcting the line supply power factor (by installing PF improvement apparatus).
- The thyristorised power controllers have no short time over loading capacity and therefore they must be rated for maximum loading conditions. This leads to an increase in the cost of the equipment.
- Special protection circuits must be employed in thyristorised power controllers in order to protect and safe guard the expensive thyristor devices. This again adds to the system cost.

TYPES OF POWER CONVERTERS or THYRISTORISED POWER CONTROLLERS

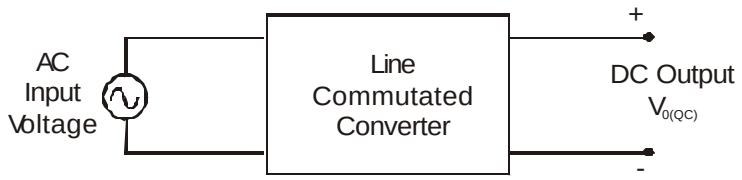
For the control of electric power supplied to the load or the equipment/machinery or for power conditioning the conversion of electric power from one form to other is necessary and the switching characteristic of power semiconductor devices (Thyristors) facilitate these conversions

The thyristorised power converters are referred to as the static power converters and they perform the function of power conversion by converting the available input power supply in to output power of desired form.

The different types of thyristor power converters are

- Diode rectifiers (uncontrolled rectifiers).
- Line commutated converters or AC to DC converters (controlled rectifiers)
- AC voltage (RMS voltage) controllers (AC to AC converters).
- Cyclo converters (AC to AC converters at low output frequency).
- DC choppers (DC to DC converters).
- Inverters (DC to AC converters).

LINE COMMUTATED CONVERTERS
(AC TO DC CONVERTERS)



These are AC to DC converters. The line commutated converters are AC to DC power converters. These are also referred to as controlled rectifiers. The line commutated converters (controlled rectifiers) are used to convert a fixed voltage, fixed frequency AC power supply to obtain a variable DC output voltage. They use natural or AC line commutation of the Thyristors.

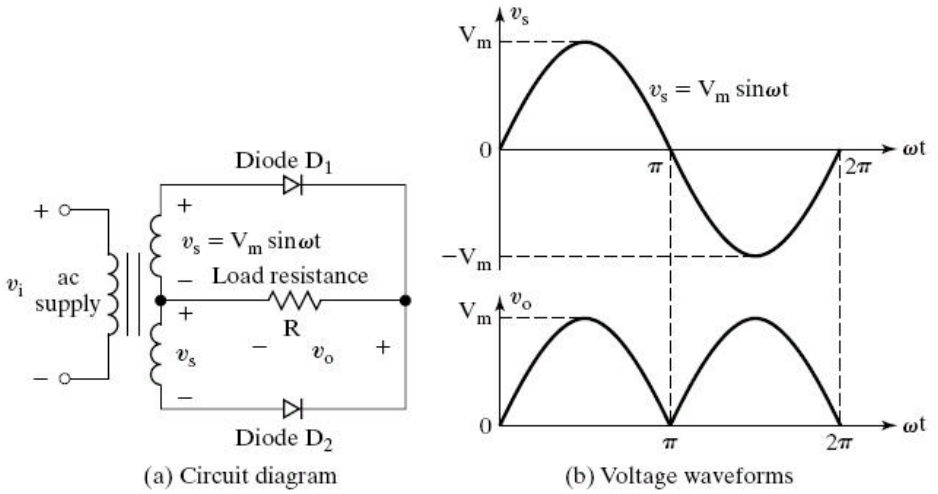


Fig: A Single Phase Full Wave Uncontrolled Rectifier Circuit (Diode Full Wave Rectifier) using a Center Tap ped Transformer

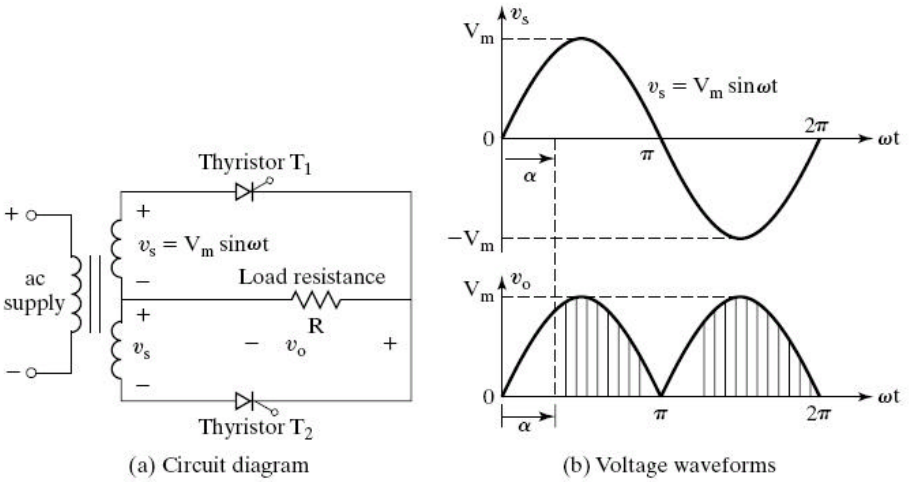


Fig: A Single Phase Full Wave Controlled Rectifier Circuit (using SCRs) using a Center Tapped Transformer

Different type s of line commutated AC to DC converters circuits are

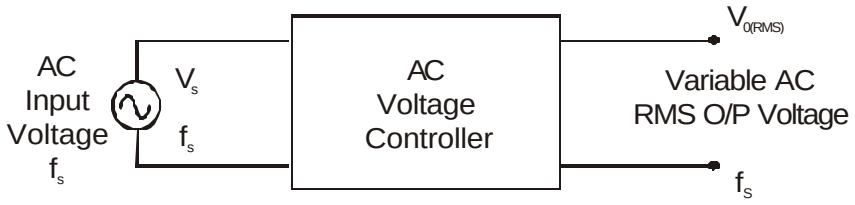
- Diode rectifiers – Uncontrolled Rectifiers
- Controlled rectifiers using SCR's.
  - Single phase controlled rectifier.
  - Three phase controlled rectifiers.

Applications Of Line Commutated Converters

AC to DC power converters are widely used in

- Speed control of DC motor in DC drives.
- UPS.
- HVDC transmission.
- Battery Chargers.

AC VOLTAGE REGULATORS OR RMS VOLTAGE CONTROLLERS (AC TO AC CONVERTERS)



The AC voltage controllers convert the constant frequency, fixed voltage AC supply into variable AC voltage at the same frequency using line commutation.

AC regulators (RMS voltage controllers) are mainly used for

- Speed control of AC motor.
- Speed control of fans (domestic and industrial fans).
- AC pumps.

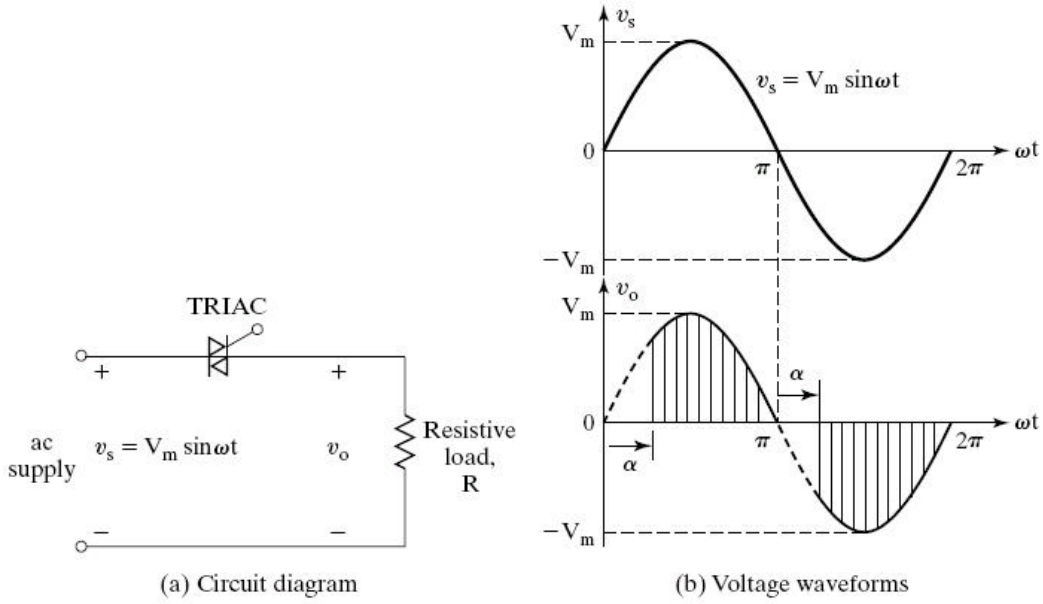
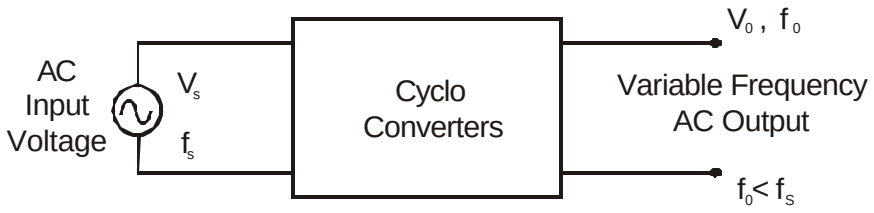


Fig: A Single Phase AC voltage Controller Circuit (AC-AC Converter using a TRIAC)

CYCLO CONVERTERS (AC TO AC CONVERTERS WITH LOW OUTPUT FREQUENCY)

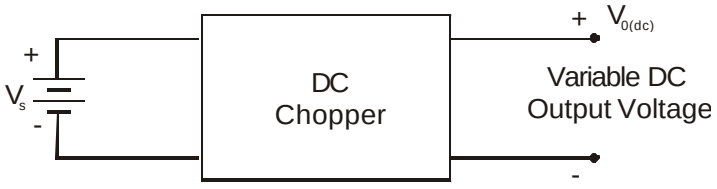


The cyclo converters convert power from a fixed voltage fixed frequency AC supply to a variable frequency and variable AC voltage at the output.

The cyclo converters generally produce output AC voltage at a lower output frequency. That is output frequency of the AC output is less than input AC supply frequency.

Applications of cyclo converters are traction vehicles and gearless rotary kilns.

CHOPPERS (DC TO DC CONVERTERS)



The choppers are power circuits which obtain power from a fixed voltage DC supply and convert it into a variable DC voltage. They are also called as DC choppers or DC to DC converters. Choppers employ forced commutation to turn off the Thyristors. DC choppers are further classified into several types depending on the direction of power flow and the type of commutation. DC choppers are widely used in

- Speed control of DC motors from a DC supply.
- DC drives for sub-urban traction.
- Switching power supplies.

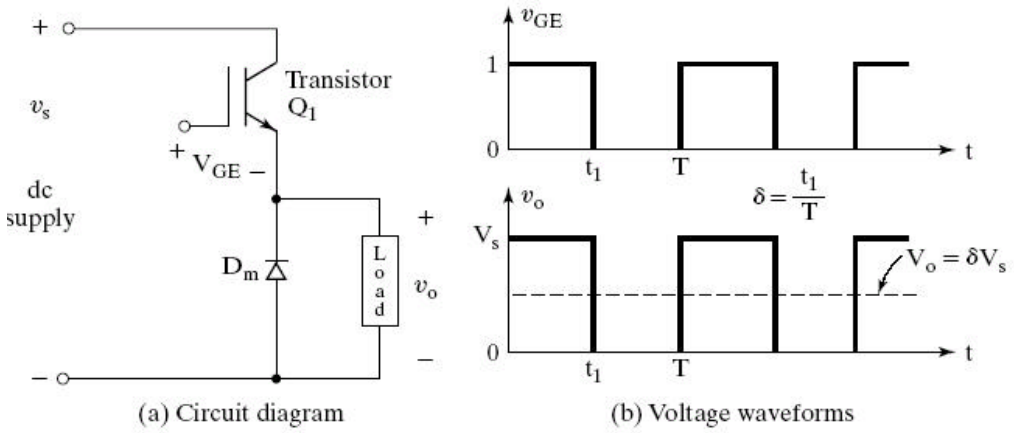
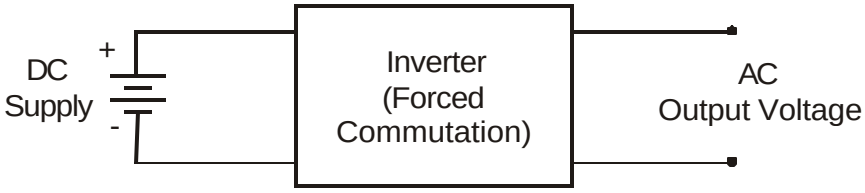


Fig: A DC Chopper Circuit (DC-DC Converter) using IGBT

INVERTERS (DC TO AC CONVERTERS)



The inverters are used for converting DC power from a fixed voltage DC supply into an AC output voltage of variable frequency and fixed or variable output AC voltage. The inverters also employ force commutation method to turn off the Thyristors.

Application of inverters are in

- Industrial AC drives using induction and synchronous motors.
- Uninterrupted power supplies (UPS system) used for computers, computer labs.

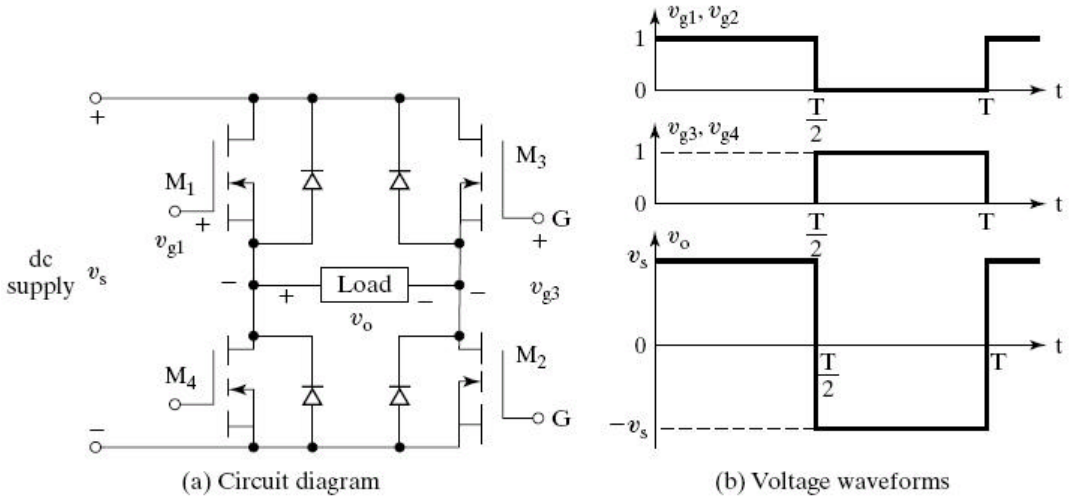


Fig: Single Phase DC-AC Converter (Inverter) using MOSFETS

DESIGN OF POWER ELECTRONICS CIRCUITS

The design and study of power electronic circuits involve

- Design and study of power circuits using Thyristors, Diodes, BJT's or MOSFETS.
- Design and study of control circuits.
- Design and study of logic and gating circuits and associated digital circuits.
- Design and study of protection devices and circuits for the protection of thyristor power devices in power electronic circuits.

The power electronic circuits can be classified into six types

- Diode rectifiers (uncontrolled rectifiers)
- AC to DC converters (Controlled rectifiers)
- AC to AC converters (AC voltage controllers)
- DC to DC converters (DC choppers)
- DC to AC converters (Inverters)
- Static Switches (Thyristorized contactors)

PERIPHERAL EFFECTS

The power converter operations are based mainly on the switching of power semiconductor devices and as a result the power converters introduce current and voltage harmonics (unwanted AC signal components) into the supply system and on the output of the converters.

These induced harmonics can cause problems of distortion of the output voltage, harmonic generation into the supply system, and interference with the communication and signaling circuits. It is normally necessary to introduce filters on the input side and output side of a power converter system so as to reduce the harmonic level to an acceptable magnitude. The figure below shows the block diagram of a generalized power converter

with filters added. The application of power electronics to supply the sensitive electronic loads poses a challenge on the power quality issues and raises the problems and concerns to be resolved by the researchers. The input and output quantities of power converters could be either AC or DC. Factors such as total harmonic distortion (THD), displacement factor or harmonic factor (HF), and input power factor (IPF), are measures of the quality of the waveforms. To determine these factors it is required to find the harmonic content of the waveforms. To evaluate the performance of a converter, the input and output voltages/currents of a converter are expressed in Fourier series. The quality of a power converter is judged by the quality of its voltage and current waveforms.

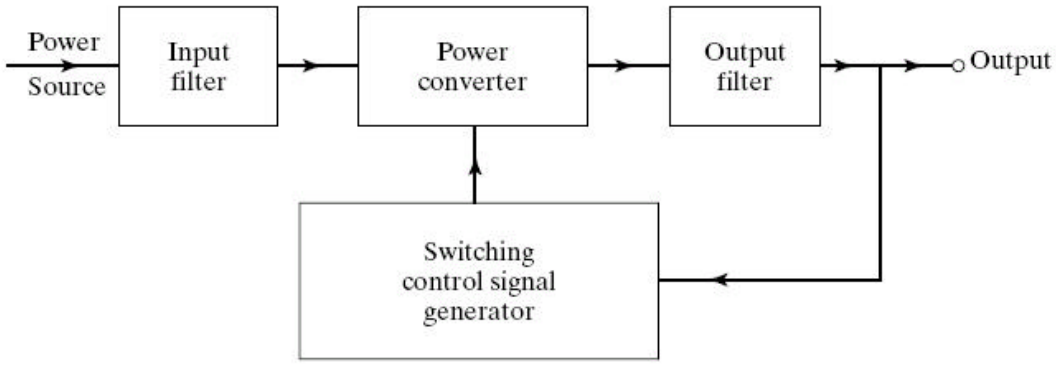


Fig: A General Power Converter System

The control strategy for the power converters plays an important part on the harmonic generation and the output waveform distortion and can be aimed to minimize or reduce these problems. The power converters can cause radio frequency interference due to electromagnetic radiation and the gating circuits may generate erroneous signals. This interference can be avoided by proper grounding and shielding.

POWER TRANSISTORS

Power transistors are devices that have controlled turn-on and turn-off characteristics. These devices are used a switching devices and are operated in the saturation region resulting in low on-state voltage drop. They are turned on when a current signal is given to base or control terminal. The transistor remains on so long as the control signal is present. The switching speed of modern transistors is much higher than that of thyristors and are used extensively in dc-dc and dc-ac converters. However their voltage and current ratings are lower than those of thyristors and are therefore used in low to medium power applications.

Power transistors are classified as follows

- Bipolar junction transistors(BJTs)
- Metal-oxide semiconductor filed-effect transistors(MOSFETs)
- Static Induction transistors(SITs)
- Insulated-gate bipolar transistors(IGBTs)

BIPOLAR JUNCTION TRANSISTORS

The need for a large blocking voltage in the off state and a high current carrying capability in the on state means that a power BJT must have substantially different structure than its small signal equivalent. The modified structure leads to significant differences in the I-V characteristics and switching behavior between power transistors and its logic level counterpart.

POWER TRANSISTOR STRUCTURE

If we recall the structure of conventional transistor we see a thin p-layer is sandwiched between two n-layers or vice versa to form a three terminal device with the terminals named as Emitter, Base and Collector.

The structure of a power transistor is as shown below

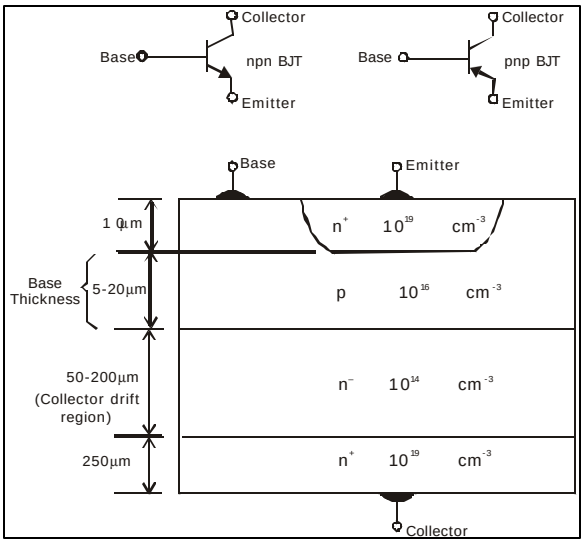


Fig. 1: Structure of Power Transistor

The difference in the two structures is obvious.

A power transistor is a vertically oriented four layer structure of alternating p-type and n type. The vertical structure is preferred because it maximizes the cross sectional area and through which the current in the device is flowing. This also minimizes on-state resistance and thus power dissipation in the transistor.

The doping of emitter layer and collector layer is quite large typically 10^{19} cm^{-3}. A special layer called the collector drift region (n^-) has a light doping level of 10^{14}.

The thickness of the drift region determines the breakdown voltage of the transistor. The base thickness is made as small as possible in order to have good amplification capabilities, however if the base thickness is small the breakdown voltage capability of the transistor is compromised.

Practical power transistors have their emitters and bases interleaved as narrow fingers as shown. The purpose of this arrangement is to reduce the effects of current crowding. This multiple emitter layout also reduces parasitic ohmic resistance in the base current path which reduces power dissipation in the transistor.

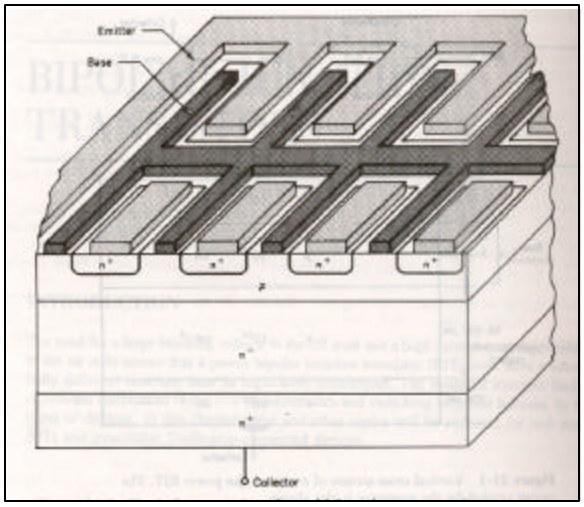


Fig. 2

STEADY STATE CHARACTERISTICS

Figure 3(a) shows the circuit to obtain the steady state characteristics. Fig 3(b) shows the input characteristics of the transistor which is a plot of I_B versus V_{BE}. Fig 3(c) shows the output characteristics of the transistor which is a plot I_C versus V_{CE}. The characteristics shown are that for a signal level transistor.

The power transistor has steady state characteristics almost similar to signal level transistors except that the V-I characteristics has a region of quasi saturation as shown by figure 4.

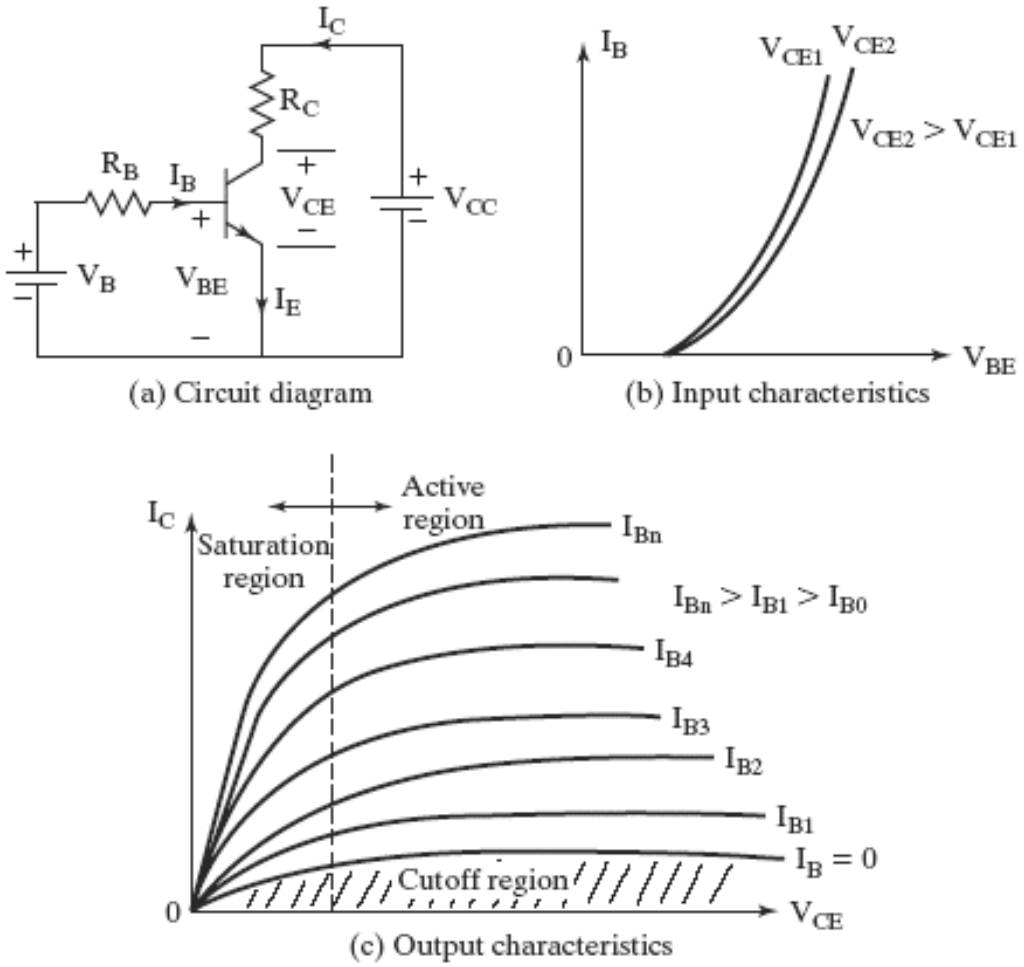


Fig. 3: Characteristics of NPN Transistors

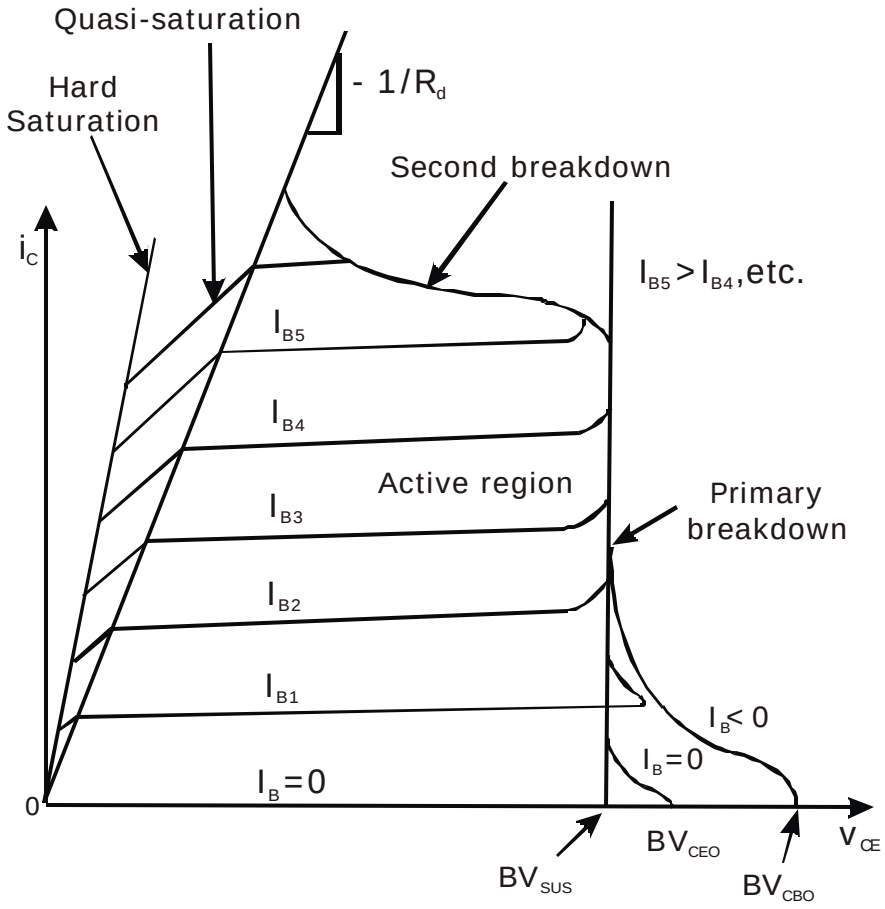


Fig. 4: Characteristics of NPN Power Transistors

There are four regions clearly shown: Cutoff region, Active region, quasi saturation and hard saturation. The cutoff region is the area where base current is almost zero. Hence no collector current flows and transistor is off. In the quasi saturation and hard saturation, the base drive is applied and transistor is said to be on. Hence collector current flows depending upon the load. The power BJT is never operated in the active region (i.e. as an amplifier) it is always operated between cutoff and saturation. The BV_{SUS} is the maximum collector to emitter voltage that can be sustained when BJT is carrying substantial collector current. The BV_{CEO} is the maximum collector to emitter breakdown voltage that can be sustained when base current is zero and BV_{CBO} is the collector base breakdown voltage when the emitter is open circuited.

The primary breakdown shown takes place because of avalanche breakdown of collector base junction. Large power dissipation normally leads to primary breakdown.

The second breakdown shown is due to localized thermal runaway. This is explained in detail later.

TRANSFER CHARACTERISTICS

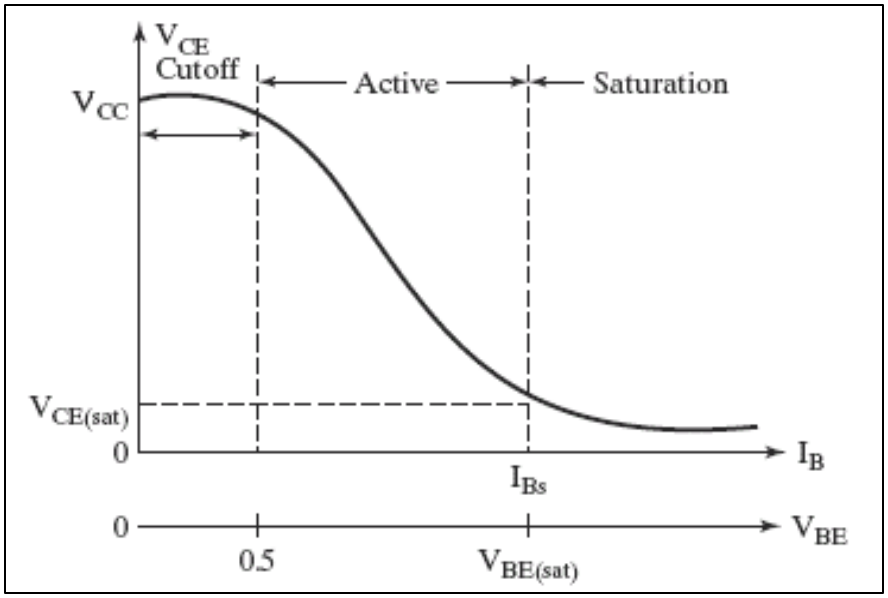


Fig. 5: Transfer Characteristics

$$I_E = I_C + I_B$$

$$b = h_{fE} = \frac{I_C}{I_B}$$

$$I_C = b\, I_B + I_{CEO}$$

$$a = \frac{b}{b+1}$$

$$b = \frac{a}{1-a}$$

TRANSISTOR AS A SWITCH

The transistor is used as a switch therefore it is used only between saturation and cutoff. From fig. 5 we can write the following equations

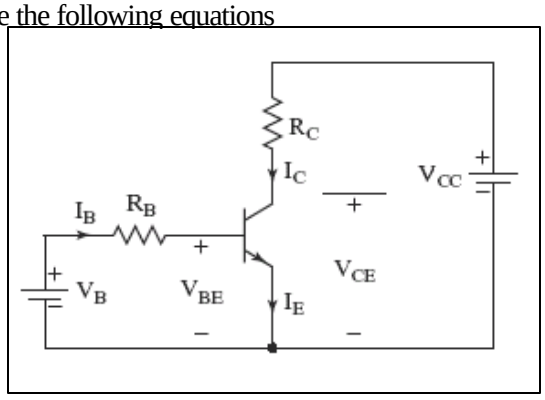


Fig. 6: Transistor Switch

$$I_B = \frac{V_B - V_{BE}}{R_B}$$

$$V_C = V_{CE} = V_{CC} - I_C R_C$$

$$V_C = V_{CC} - b\,\frac{R_C (V_B - V_{BE})}{R_B}$$

$$V_{CE} = V_{CB} + V_{BE}$$

$$V_{CB} = V_{CE} - V_{BE} \qquad \ldots.(1)$$

Equation (1) shows that as long as $V_{CE} > V_{BE}$ the CBJ is reverse biased and transistor is in active region, The maximum collector current in the active region, which can be obtained by setting $V_{CB} = 0$ and $V_{BE} = V_{CE}$ is given as

$$I_{CM} = \frac{V_{CC} - V_{CE}}{R_C} \qquad \therefore \quad I_{BM} = \frac{I_{CM}}{b_F}$$

If the base current is increased above I_{BM}, V_{BE} increases, the collector current increases and V_{CE} falls below V_{BE}. This continues until the CBJ is forward biased with V_{BC} of about 0.4 to 0.5V, the transistor than goes into saturation. The transistor saturation may be defined as the point above which any increase in the base current does not increase the collector current significantly.

In saturation, the collector current remains almost constant. If the collector emitter voltage is $V_{CE(sat)}$ the collector current is

$$I_{CS} = \frac{V_{CC} - V_{CESAT}}{R_C}$$

$$I_{BS} = \frac{I_{CS}}{b}$$

Normally the circuit is designed so that I_B is higher that I_{BS}. The ratio of I_B to I_{BS} is called to overdrive factor ODF.

$$ODF = \frac{I_B}{I_{BS}}$$

The ratio of I_{CS} to I_B is called as forced b.

$$b_{forced} = \frac{I_{CS}}{I_B}$$

The total power loss in the two functions is

$$P_T = V_{BE} I_B + V_{CE} I_C$$

A high value of ODF cannot reduce the CE voltage significantly. However V_{BE} increases due to increased base current resulting in increased power loss. Once the transistor is saturated, the CE voltage is not reduced in relation to increase in base current. However the power is increased at a high value of ODF, the transistor may be damaged due to

thermal runaway. On the other hand if the transistor is under driven $(I_B < I_{BS})$ it may operate in active region, V_{CE} increases resulting in increased power loss.

PROBLEMS

1. The BJT is specified to have a range of 8 to 40. The load resistance in $R_e = 11\Omega$. The dc supply voltage is V_{CC}=200V and the input voltage to the base circuit is V_B=10V. If $V_{CE(sat)}$=1.0V and $V_{BE(sat)}$=1.5V. Find
   a. The value of R_B that results in saturation with a overdrive factor of 5.
   b. The forced b_f.
   c. The power loss P_T in the transistor.

Solution

(a) $$I_{CS} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{200 - 1.0}{11\Omega} = 18.1A$$

Therefore $$I_{BS} = \frac{I_{CS}}{b_{\min}} = \frac{18.1}{8} = 2.2625A$$

Therefore $$I_B = ODF \times I_{BS} = 11.3125A$$

$$I_B = \frac{V_B - V_{BE(sat)}}{R_B}$$

Therefore $$R_B = \frac{V_B - V_{BE(sat)}}{I_B} = \frac{10 - 1.5}{11.3125} = 0.715\Omega$$

(b) Therefore $$b_f = \frac{I_{CS}}{I_B} = \frac{18.1}{11.3125} = 1.6$$

$$P_T = V_{BE} I_B + V_{CE} I_C$$

(c) $$P_T = 1.5 \times 11.3125 + 1.0 \times 18.1$$

$$P_T = 16.97 + 18.1 = 35.07W$$

2. The b of a bipolar transistor varies from 12 to 75. The load resistance is $R_C = 1.5\Omega$. The dc supply voltage is V_{CC}=40V and the input voltage base circuit is V_B=6V. If $V_{CE(sat)}$=1.2V, $V_{BE(sat)}$=1.6V and R_B=0.7Ω determine
   a. The overdrive factor ODF.
   b. The forced β_f.
   c. Power loss in transistor P_T

Solution

$$I_{CS} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{40 - 1.2}{1.5} = 25.86A$$

$$I_{BS} = \frac{I_{CS}}{b_{\min}} = \frac{25.86}{12} = 2.15A$$

Also $$I_B = \frac{V_B - V_{BE(sat)}}{R_B} = \frac{6 - 1.6}{0.7} = 6.28A$$

(a) Therefore $$ODF = \frac{I_B}{I_{BS}} = \frac{6.28}{2.15} = 2.92$$

Forced $$b_f = \frac{I_{CS}}{I_B} = \frac{25.86}{6.28} = 4.11$$

(c) $$P_T = V_{BE} I_B + V_{CE} I_C$$

$$P_T = 1.6 \times 6.25 \; + \; 1.2 \times 25.86$$

$$P_T = 41.032 Watts$$

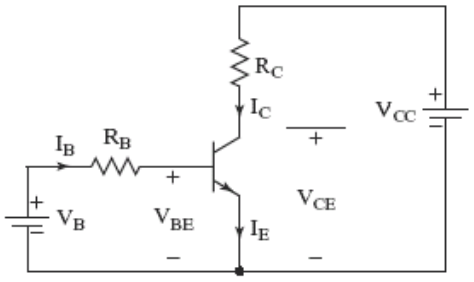
(JULY / AUGUST 2004)

3. For the transistor switch as shown in figure

   a. Calculate forced beta, b_f of transistor.

   b. If the manufacturers specified b is in the range of 8 to 40, calculate the minimum overdrive factor (ODF).

   c. Obtain power loss P_T in the transistor.



$V_B = 10V, \quad R_B = 0.75\Omega,$
$V_{BE(sat)} = 1.5V, \; R_C = 11\Omega,$
$V_{CE(sat)} = 1V, \quad V_{CC} = 200V$

Solution

(i) $$I_B = \frac{V_B - V_{BE(sat)}}{R_B} = \frac{10 - 1.5}{0.75} = 11.33A$$

$$I_{CS} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{200 - 1.0}{11} = 18.09A$$

Therefore $$I_{BS} = \frac{I_{CS}}{b_{\min}} = \frac{18.09}{8} = 2.26A$$

$$b_f = \frac{I_{CS}}{I_B} = \frac{18.09}{11.33} = 1.6$$

(ii) $$ODF = \frac{I_B}{I_{BS}} = \frac{11.33}{2.26} = 5.01$$

(iii) $$P_T = V_{BE}I_B + V_{CE}I_C = 1.5 \times 11.33 + 1.0 \times 18.09 = 35.085W$$

(JAN / FEB 2005)

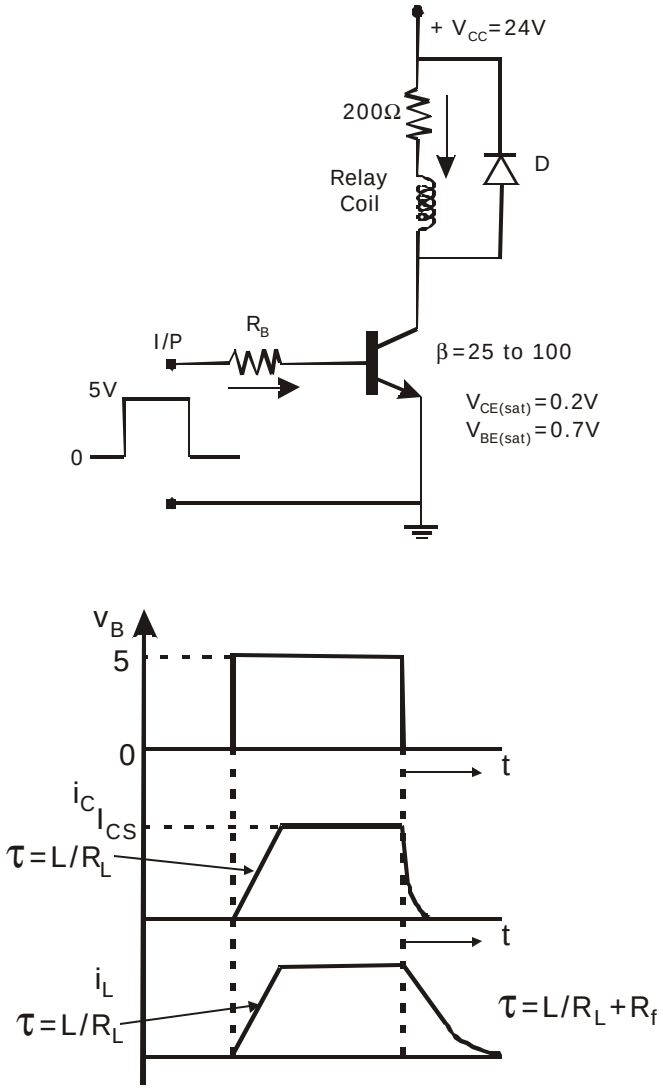
4. A simple transistor switch is used to connect a 24V DC supply across a relay coil, which has a DC resistance of 200Ω. An input pulse of 0 to 5V amplitude is applied through series base resistor R_B at the base so as to turn on the transistor switch. Sketch the device current waveform with reference to the input pulse.

   Calculate

   a. I_{CS} .

   b. Value of resistor R_B, required to obtain over drive factor of two.

   c. Total power dissipation in the transistor that occurs during the saturation state.



Solution

To sketch the device current waveforms; current through the device cannot rise fast to the saturating level of I_{CS} since the inductive nature of the coil opposes any change in current through it. Rate of rise of collector current can be determined by the time constant $t_1 = \frac{L}{R}$. Where L is inductive in Henry of coil and R is resistance of coil. Once steady state value of I_{CS} is reached the coil acts as a short circuit. The collector current stays put at I_{CS} till the base pulse is present.

Similarly once input pulse drops to zero, the current I_C does not fall to zero immediately since inductor will now act as a current source. This current will now decay at the fall to zero. Also the current has an alternate path and now can flow through the diode.

(i) $$I_{CS} = \frac{V_{CC} - V_{CE(sat)}}{R_C} = \frac{24 - 0.2}{200} = 0.119A$$

(ii) Value of R_B

$$I_{BS} = \frac{I_{CS}}{b_{\min}} = \frac{0.119}{25} = 4.76mA$$

$$\therefore \quad I_B = ODF \times I_{BS} = 2 \times 4.76 = 9.52mA$$

$$\therefore \quad R_B = \frac{V_B - V_{BE(sat)}}{I_B} = \frac{5 - 0.7}{9.52} = 450\Omega$$

(iii) $$P_T = V_{BE(sat)} \times I_B + V_{CE(sat)} \times I_{CS} = 0.7 \times 9.52 + 0.2 \times 0.119 = 6.68W$$

SWITCHING CHARACTERISTICS

A forward biased p-n junction exhibits two parallel capacitances; a depletion layer capacitance and a diffusion capacitance. On the other hand, a reverse biased p-n junction has only depletion capacitance. Under steady state the capacitances do not play any role. However under transient conditions, they influence turn-on and turn-off behavior of the transistor.

TRANSIENT MODEL OF BJT

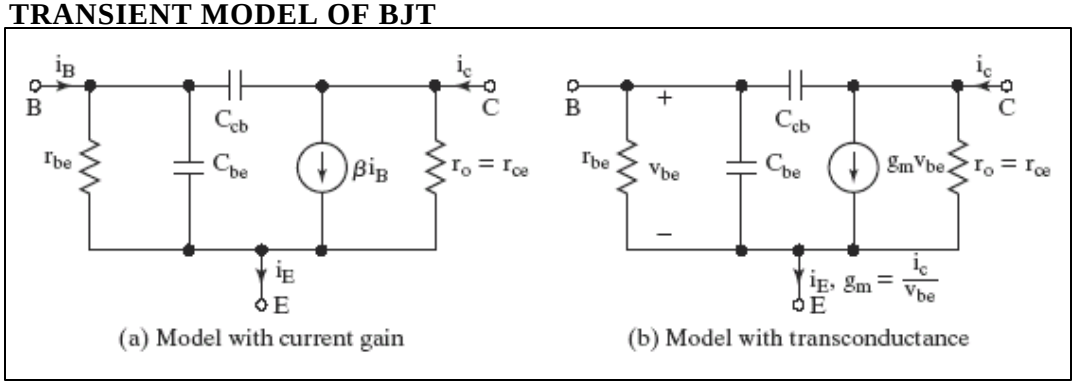


Fig. 7: Transient Model of BJT

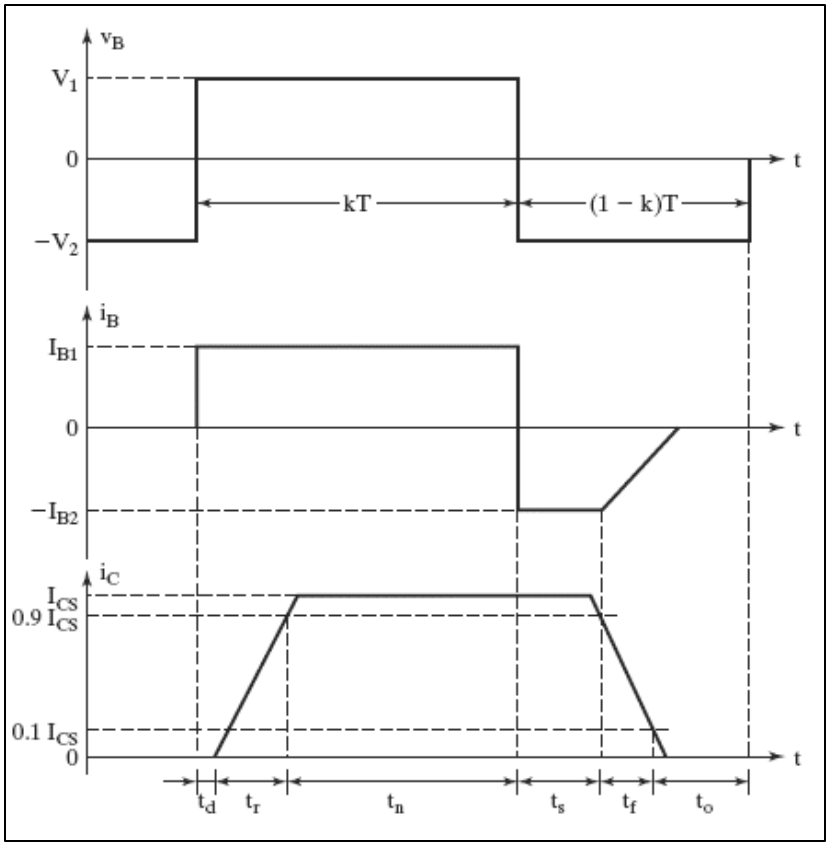


Fig. 8: Switching Times of BJT

Due to internal capacitances, the transistor does not turn on instantly. As the voltage V_B rises from zero to V_1 and the base current rises to I_{B1}, the collector current does not respond immediately. There is a delay known as delay time td, before any collector current flows. The delay is due to the time required to charge up the BEJ to the forward bias voltage V_{BE}(0.7V). The collector current rises to the steady value of I_{CS} and this time is called rise time t_r.

The base current is normally more than that required to saturate the transistor. As a result excess minority carrier charge is stored in the base region. The higher the ODF, the greater is the amount of extra charge stored in the base. This extra charge which is called the saturating charge is proportional to the excess base drive.

This extra charge which is called the saturating charge, is proportional to the excess base drive and the corresponding current I_e.

$$I_e = I_B - \frac{I_{CS}}{b} = ODFI_{BS} - I_{BS} = I_{BS}\left(ODF - 1\right)$$

Saturating charge $Q_S = t_s I_e = t_s I_{BS}(ODF - 1)$ where t_s is known as the storage time constant.

When the input voltage is reversed from V_1 to $-V_2$, the reverse current $-I_{B2}$ helps to discharge the base. Without $-I_{B2}$ the saturating charge has to be removed entirely due to recombination and the storage time t_s would be longer.

Once the extra charge is removed, BEJ charges to the input voltage $-V_2$ and the base current falls to zero. t_f depends on the time constant which is determined by the reverse biased BEJ capacitance.

$$\therefore \quad t_{on} = t_d + t_r$$
$$t_{off} = t_s + t_f$$

PROBLEMS

1. For a power transistor, typical switching waveforms are shown. The various parameters of the transistor circuit are as under $V_{cc} = 220V$, $V_{CE(sat)} = 2V$, $I_{CS} = 80A$, $td = 0.4ms$, $t_r = 1ms$, $t_n = 50ms$, $t_s = 3ms$, $t_f = 2ms$, $t_0 = 40ms$, $f = 5Khz$, $I_{CEO} = 2mA$. Determine average power loss due to collector current during t_{on} and t_n. Find also the peak instantaneous power loss, due to collector current during turn-on time.

Solution

During delay time, the time limits are $0 \le t \le td$. Figure shows that in this time $i_c(t) = I_{CEO}$ and $V_{CE}(t) = V_{CC}$. Therefore instantaneous power loss during delay time is $P_d(t) = i_C V_{CE} = I_{CEO} V_{CC} = 2x10^{-3} x220 = 0.44W$

Average power loss during delay time $0 \le t \le td$ is given by

$$Pd = \frac{1}{T}\int_0^{td} i_c(t) v_{CE}(t)\, dt$$

$$Pd = \frac{1}{T}\int_0^{td} I_{CEO} V_{CC}\, dt$$

$$Pd = f.I_{CEO} V_{CC} td$$

$$Pd = 5x10^3 \times 2\times 10^{-3} \times 220 \times 0.4 \times 10^{-6} = 0.88mW$$

During rise time $0 \le t \le t_r$

$$i_c(t) = \frac{I_{CS}}{t_r} t$$

$$v_{CE}(t) = \left[V_{CC} - \left(\frac{V_{CC} - V_{CE(sat)}}{t_r} \right) t \right]$$

$$v_{CE}(t) = V_{CC} + \left[V_{CE(sat)} - V_{CC} \right] \frac{t}{t_r}$$

Therefore average power loss during rise time is

$$P_r = \frac{1}{T}\int_0^{t_r} \frac{I_{CS}}{t_r} t\left[V_{CC} + \left(V_{CE(sat)} - V_{CC}\right)\frac{t}{t_r}\right]dt$$

$$P_r = f.I_{CS}t_r\left[\frac{V_{CC}}{2} - \frac{V_{CC} - V_{CES}}{3}\right]$$

$$P_r = 5x10^3 \times 80 \times 1 \times 10^{-6}\left[\frac{220}{2} - \frac{220-2}{3}\right] = 14.933W$$

Instantaneous power loss during rise time is

$$P_r(t) = \frac{I_{CS}}{t_r} t\left[V_{CC} - \frac{V_{CC} - V_{CE}(sat)}{t_r} t\right]$$

$$P_r(t) = \frac{I_{CS}}{t_r} tV_{CC} - \frac{I_{CSt}^{\ 2}}{t_r^{\ 2}}\left[V_{CC} - V_{CE(sat)}\right]$$

Differentiating the above equation and equating it to zero will give the time t_m at which instantaneous power loss during t_r would be maximum.

Therefore $\quad \frac{dP_r(t)}{dt} = \frac{I_{CS}V_{CC}}{t_r} - \frac{I_{CS}2t}{t_r^{\ 2}}\left[V_{CC} - V_{CEsat}\right]$

At $t = t_m$, $\quad \frac{dP_r(t)}{dt} = 0$

Therefore $\quad 0 = \frac{I_{CS}}{t_r}V_{CC} - \frac{2I_{CS}t_m}{t_r^{\ 2}}\left[V_{CC} - V_{CE(sat)}\right]$

$$\frac{\not{I}_{CS}}{\not{t}_r}V_{cc} = \frac{2\not{I}_{CS}t_m}{\not{t}_r^{\ 2}}\left[V_{CC} - V_{CE(sat)}\right]$$

$$\frac{t_r V_{CC}}{2} = t_m\left[V_{CC} - V_{CE(sat)}\right]$$

Therefore $\quad t_m = \frac{t_r V_{CC}}{2\left[V_{CC} - V_{CE(sat)}\right]}$

Therefore $\quad t_m = \frac{V_{CC}t_r}{2\left[V_{CC} - V_{CE(sat)}\right]} = \frac{220 \times 1 \times 10^{-6}}{2[200-2]} = 0.5046ms$

Peak instantaneous power loss P_{rm} during rise time is obtained by substituting the value of t=tm in equation (1) we get

$$P_{rm} = \frac{I_{CS}}{t_r}\frac{V_{CC}{}^2 t_r}{2\left[V_{CC} - V_{CE(sat)}\right]} - \frac{I_{CS}}{t_r{}^2}\frac{(V_{CC}t_r)^2\left[V_{CC} - V_{CE(sat)}\right]}{4\left[V_{CC} - V_{CE(sat)}\right]^2}$$

$$P_{rm} = \frac{80\times 220^2}{4[220-2]} = 4440.4W$$

Total average power loss during turn-on

$$P_{on} = Pd + P_r = 0.00088 + 14.933 = 14.9339W$$

During conduction time $0 \le t \le t_n$

$$i_C(t) = I_{CS} \;\&\; v_{CE}(t) = V_{CE(sat)}$$

Instantaneous power loss during t_n is

$$P_n(t) = i_C v_{CE} = I_{CS}V_{CE(sat)} = 80\ x\ 2 = 160W$$

Average power loss during conduction period is

$$P_n = \frac{1}{T}\int_0^{t_n} i_C v_{CE}\,dt = fI_{CS}V_{CES}t_n = 5\times 10^3 \times 80 \times 2\ \times 50 \times 10^{-6} = 40W$$

PERFORMANCE PARAMETERS

DC gain h_{FE} $b = \frac{I_C}{I_B}[V_{CE}]$: Gain is dependent on temperature. A high gain would reduce the values of forced b & $V_{CE(sat)}$.

$V_{CE(sat)}$: A low value of $V_{CE(sat)}$ will reduce the on-state losses. $V_{CE(sat)}$ is a function of the collector circuit, base current, current gain and junction temperature. A small value of forced β decreases the value of $V_{CE(sat)}$.

$V_{BE(sat)}$**:** A low value of $V_{BE(sat)}$ will decrease the power loss in the base emitter junction. $V_{BE(sat)}$ increases with collector current and forced β.

Turn-on time t_{on}**:** The turn-on time can be decreased by increasing the base drive for a fixed value of collector current. t_d is dependent on input capacitance does not change significantly with I_C. However t_r increases with increase in I_C.

Turn off time t_{off}: The storage time t_s is dependent on over drive factor and does not change significantly with I_C. t_f is a function of capacitance and increases with I_C.

t_s & t_f can be reduced by providing negative base drive during turn-off. t_f is less sensitive to negative base drive.

Cross-over t_C **:** The crossover time t_C is defined as the interval during which the collector voltage V_{CE} rises from 10% of its peak off state value and collector current. I_C falls to 10% of its on-state value. t_C is a function of collector current negative base drive.

Switching Limits

SECOND BREAKDOWN

It is a destructive phenomenon that results from the current flow to a small portion of the base, producing localized hot spots. If the energy in these hot spots is sufficient the excessive localized heating may damage the transistor. Thus secondary breakdown is caused by a localized thermal runaway. The SB occurs at certain combinations of voltage, current and time. Since time is involved, the secondary breakdown is basically an energy dependent phenomenon.

FORWARD BIASED SAFE OPERATING AREA FBSOA

During turn-on and on-state conditions, the average junction temperature and second breakdown limit the power handling capability of a transistor. The manufacturer usually provide the FBSOA curves under specified test conditions. FBSOA indicates the $I_c - V_{ce}$ limits of the transistor and for reliable operation the transistor must not be subjected to greater power dissipation than that shown by the FBSOA curve.

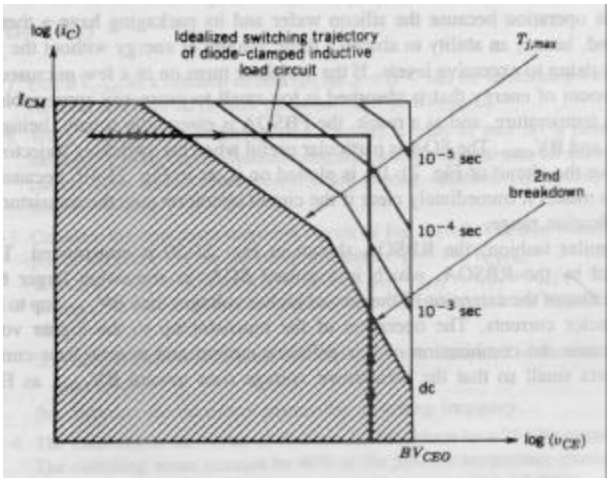


Fig. 9: FBSOA of Power BJT

The dc FBSOA is shown as shaded area and the expansion of the area for pulsed operation of the BJT with shorter switching times which leads to larger FBSOA. The second break down boundary represents the maximum permissible combinations of voltage and current without getting into the region of $i_c - v_{ce}$ plane where second breakdown may occur. The final portion of the boundary of the FBSOA is breakdown voltage limit BV_{CEO}.

REVERSE BIASED SAFE OPERATING AREA RBSOA

During turn-off, a high current and high voltage must be sustained by the transistor, in most cases with the base-emitter junction reverse biased. The collector emitter voltage must be held to a safe level at or below a specified value of collector current. The manufacturer provide $I_c - V_{ce}$ limits during reverse-biased turn off as reverse biased safe area (RBSOA).

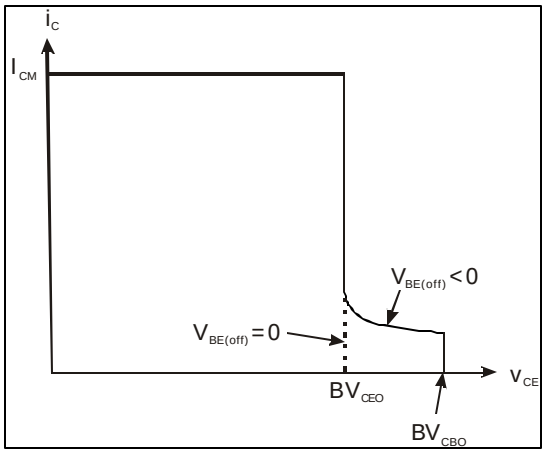


Fig. 10: RBSOA of a Power BJT

The area encompassed by the RBSOA is some what larger than FBSOA because of the extension of the area of higher voltages than BV_{CEO} upto BV_{CBO} at low collector currents. This operation of the transistor upto higher voltage is possible because the combination of low collector current and reverse base current has made the beta so small that break down voltage rises towards BV_{CBO}.

POWER DERATING

The thermal equivalent is shown. If the total average power loss is P_T,

The case temperature is $T_c = T_j - P_T T_{jc}$.

The sink temperature is $T_s = T_c - P_T T_{CS}$

The ambient temperature is $T_A = T_S - P_T R_{SA}$ and $T_j - T_A = P_T \left(R_{jc} + R_{cs} + R_{SA} \right)$

R_{jc} : Thermal resistance from junction to case $^{a}/_{w}$.

R_{CS} : Thermal resistance from case to sink $^{0}C/_{w}$.

R_{SA} : Thermal resistance from sink to ambient $^{0}C/_{w}$.

The maximum power dissipation in P_T is specified at $T_C = 25^0 C$.

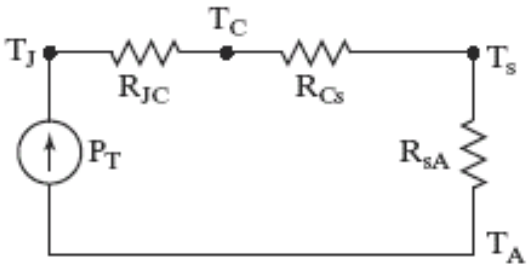


Fig. 11: Thermal Equivalent Circuit of Transistor

BREAK DOWN VOLTAGES

A break down voltage is defined as the absolute maximum voltage between two terminals with the third terminal open, shorted or biased in either forward or reverse direction.

BV_{SUS} : The maximum voltage between the collector and emitter that can be sustained across the transistor when it is carrying substantial collector current.

BV_{CEO} : The maximum voltage between the collector and emitter terminal with base open circuited.

BV_{CBO} : This is the collector to base break down voltage when emitter is open circuited.

BASE DRIVE CONTROL

This is required to optimize the base drive of transistor. Optimization is required to increase switching speeds. t_{on} can be reduced by allowing base current peaking during turn-on, $\left(b_F = \frac{I_{CS}}{I_B} [\, forced\, b\,] \right)$ resulting in low forces β at the beginning. After turn on, b_F can be increased to a sufficiently high value to maintain the transistor in quasi-saturation region. t_{off} can be reduced by reversing base current and allowing base current peaking during turn off since increasing I_{B2} decreases storage time.

A typical waveform for base current is shown.

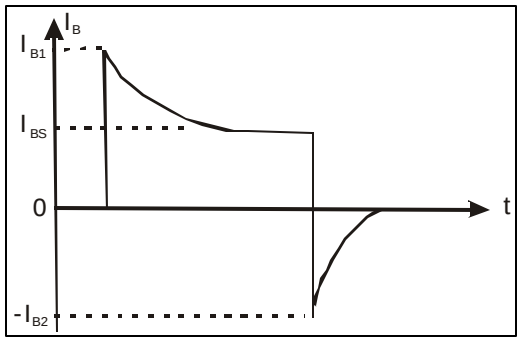


Fig. 12: Base Drive Current Waveform

Some common types of optimizing base drive of transistor are

- Turn-on Control.
- Turn-off Control.
- Proportional Base Control.
- Antisaturation Control

TURN-ON CONTROL

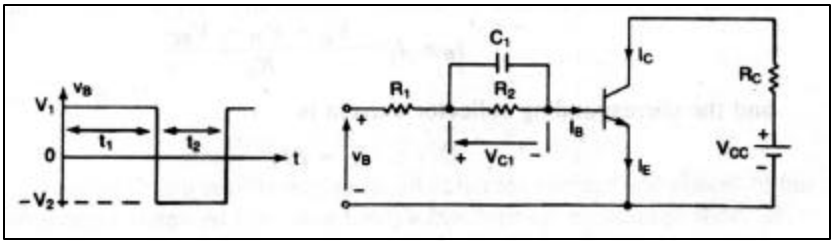


Fig. 13: Base current peaking during turn-on

When input voltage is turned on, the base current is limited by resistor R_1 and therefore initial value of base current is $I_{BO} = \frac{V_1 - V_{BE}}{R_1}$, $I_{BF} = \frac{V_1 - V_{BE}}{R_1 + R_2}$.

Capacitor voltage $V_C = V_1 \frac{R_2}{R_1 + R_2}$.

Therefore $$t_1 = \left(\frac{R_1 R_2}{R_1 + R_2} \right) C_1$$

Once input voltage v_B becomes zero, the base-emitter junction is reverse biased and C_1 discharges through R_2. The discharging time constant is $t_2 = R_2 C_1$. To allow sufficient charging and discharging time, the width of base pulse must be $t_1 \geq 5t_1$ and off period of the pulse must be $t_2 \geq 5t_2$.The maximum switching frequency is $f_s = \frac{1}{T} = \frac{1}{t_1 + t_2} = \frac{0.2}{t_1 + t_2}$.

TURN-OFF CONTROL

If the input voltage is changed to during turn-off the capacitor voltage V_C is added to V_2 as reverse voltage across the transistor. There will be base current peaking during turn off. As the capacitor C_1 discharges, the reverse voltage will be reduced to a steady state value, V_2. If different turn-on and turn-off characteristics are required, a turn-off circuit using $(C_2, R_3 \& R_4)$ may be added. The diode D_1 isolates the forward base drive circuit from the reverse base drive circuit during turn off.

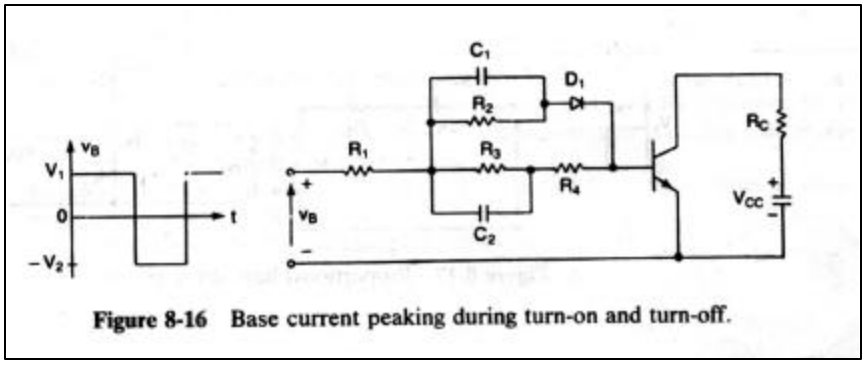


Figure 8-16 Base current peaking during turn-on and turn-off.

Fig: 14. Base current peaking during turn-on and turn-off

PROPORTIONAL BASE CONTROL

This type of control has advantages over the constant drive circuit. If the collector current changes due to change in load demand, the base drive current is changed in proportion to collector current.

When switch S_1 is turned on a pulse current of short duration would flow through the base of transistor Q_1 and Q_1 is turned on into saturation. Once the collector current starts to flow, a corresponding base current is induced due to transformer action. The transistor would latch on itself and S_1 can be turned off. The turns ratio is $N_2 / N_1 = I_C / I_B = b$. For proper operation of the circuit, the magnetizing current which must be much smaller than the collector current should be as small as possible. The switch S_1 can be implemented by a small signal transistor and additional arrangement is necessary to discharge capacitor C_1 and reset the transformer core during turn-off of the power transistor.

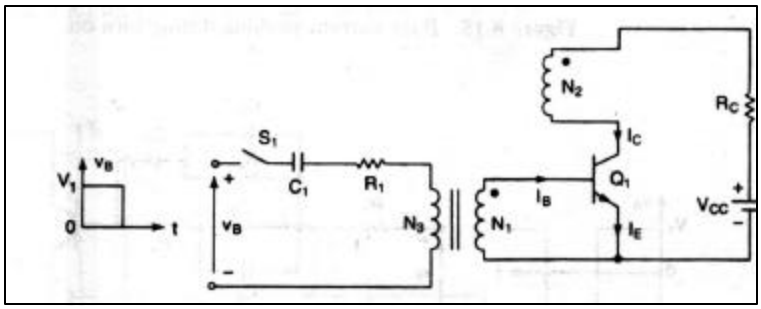


Fig. 15: Proportional base drive circuit

ANTISATURATION CONTROL

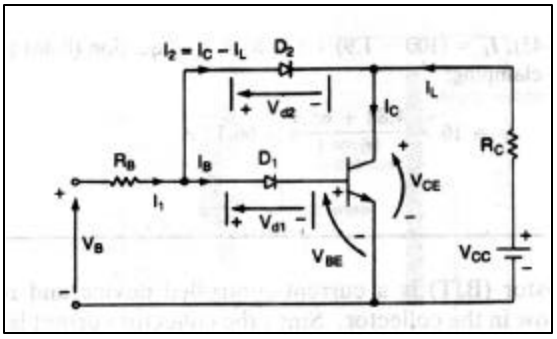


Fig: 16: Collector Clamping Circuit

If a transistor is driven hard, the storage time which is proportional to the base current increases and the switching speed is reduced. The storage time can be reduced by operating the transistor in soft saturation rather than hard saturation. This can be accomplished by clamping CE voltage to a pre-determined level and the collector current is given by $I_C = \frac{V_{CC} - V_{CM}}{R_C}$.

Where V_{CM} is the clamping voltage and $V_{CM} > V_{CE(sat)}$.

The base current which is adequate to drive the transistor hard, can be found from $I_B = I_1 = \frac{V_B - V_{D1} - V_{BE}}{R_B}$ and the corresponding collector current is $I_C = I_L = b\, I_B$.

Writing the loop equation for the input base circuit,

$$V_{ab} = V_{D_1} + V_{BE}$$

Similarly $V_{ab} = V_{D_2} + V_{CE}$

Therefore $V_{CE} = V_{BE} + V_{D_1} - V_{D_2}$

For clamping $V_{D_1} > V_{D_2}$

Therefore $V_{CE} = 0.7 + ...$

This means that the CE voltage is raised above saturation level and there are no excess carriers in the base and storage time is reduced.

The load current is $I_L = \frac{V_{CC} - V_{CE}}{R_C} = \frac{V_{CC} - V_{BE} - V_{D_1} + V_{D_2}}{R_C}$ and the collector current with clamping is $I_C = b\, I_B = b\left[I_1 - I_C + I_L\right] = \frac{b}{1+b}\left(I_1 + I_L\right)$

For clamping, $V_{D_1} > V_{D_2}$ and this can be accomplished by connecting two or more diodes in place of D_1. The load resistance R_C should satisfy the condition $b\, I_B > I_L$, $b\, I_B R_C > \left(V_{CC} - V_{BE} - V_{D_1} + V_{D_2}\right)$.

The clamping action thus results a reduced collector current and almost elimination of the storage time. At the same time, a fast turn-on is accomplished.

However, due to increased V_{CE}, the on-state power dissipation in the transistor is increased, whereas the switching power loss is decreased.

ADVANTAGES OF BJT'S

- BJT's have high switching frequencies since their turn-on and turn-off time are low.
- The turn-on losses of a BJT are small.
- BJT has controlled turn-on and turn-off characteristics since base drive control is possible.
- BJT does not require commutation circuits.

DEMERITS OF BJT

- Drive circuit of BJT is complex.
- It has the problem of charge storage which sets a limit on switching frequencies.

It cannot be used in parallel operation due to problems of negative temperature coefficient.

POWER MOSFETS

INTRODUCTION TO FET'S

FET's use field effect for their operation. FET is manufactured by diffusing two areas of p-type into the n-type semiconductor as shown. Each p-region is connected to a gate terminal; the gate is a p-region while source and drain are n-region. Since it is similar to two diodes one is a gate source diode and the other is a gate drain diode.

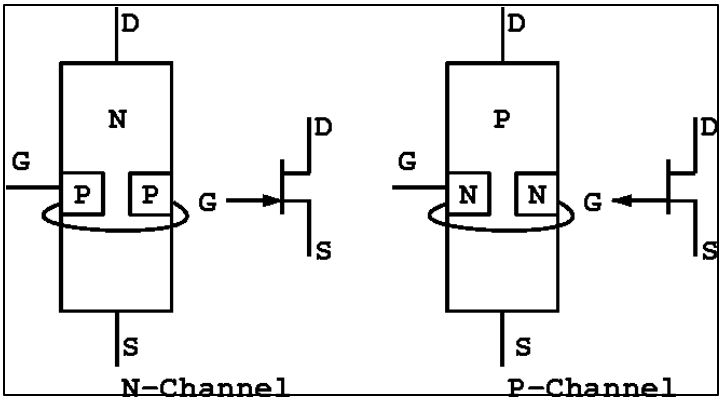


Fig:1: Schematic symbol of JFET

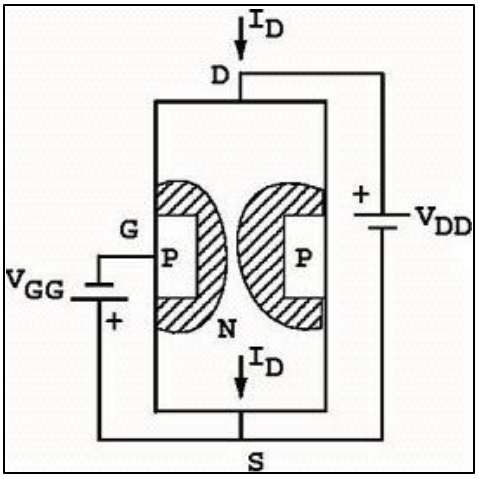


Fig. 2: Structure of FET with biasing

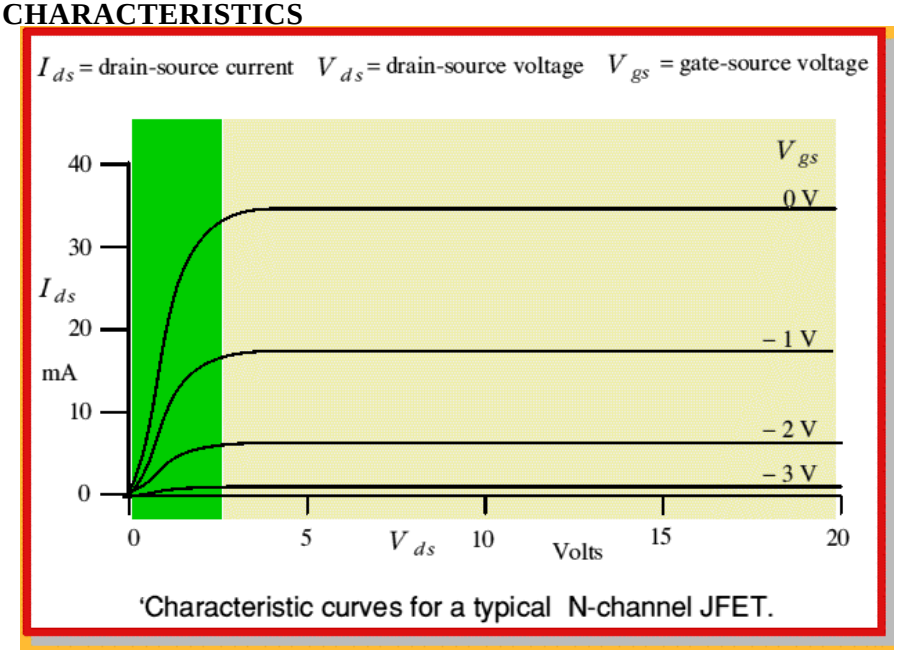
In BJT's we forward bias the B-E diode but in a JFET, we always reverse bias the gate-source diode. Since only a small reverse current can exist in the gate lead. Therefore $I_G = 0$, therefore $R_{in} = \infty\,(ideal)$.

The term field effect is related to the depletion layers around each p-region as shown. When the supply voltage V_{DD} is applied as shown it forces free electrons to flow from source to drain. With gate reverse biased, the electrons need to flow from source to drain, they must pass through the narrow channel between the two depletion layers. The more the negative gate voltage is the tighter the channel becomes.

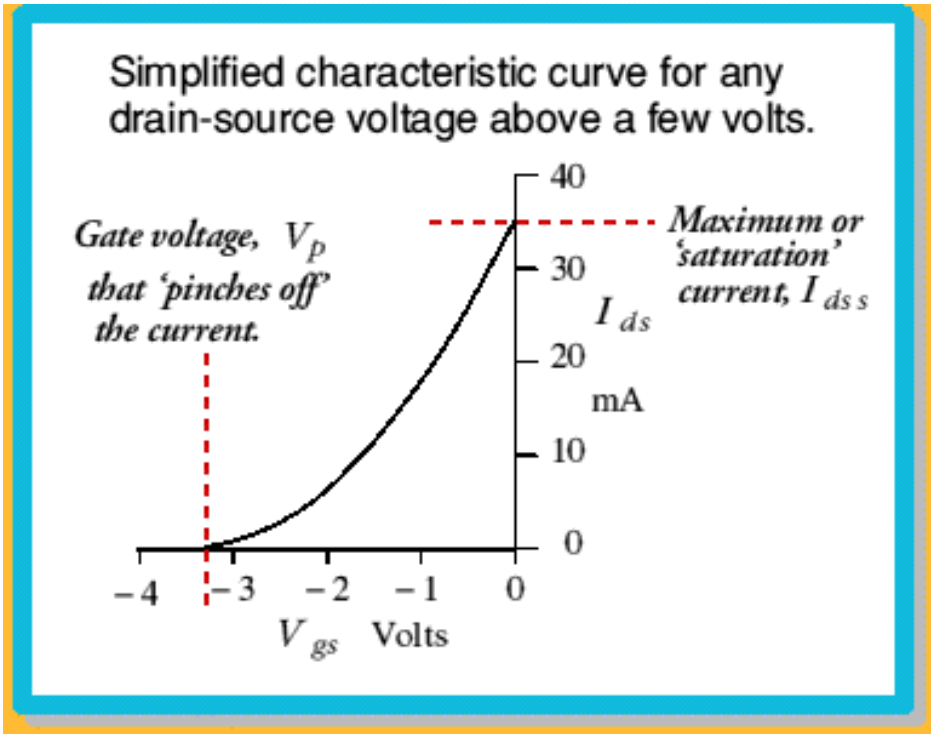
Therefore JFET acts as a voltage controlled device rather than a current controlled device.

JFET has almost infinite input impedance but the price paid for this is loss of control over the output current, since JFET is less sensitive to changes in the output voltage than a BJT.

JFET CHARACTERISTICS



'Characteristic curves for a typical N-channel JFET.



The maximum drain current out of a JFET occurs when $V_{GS} = 0$. As V_{DS} is increased for 0 to a few volts, the current will increase as determined by ohms law. As V_{DS} approaches V_P the depletion region will widen, carrying a noticeable reduction in channel width. If V_{DS} is increased to a level where the two depletion region would touch a pinch-off will result. I_D now maintains a saturation level I_{DSS}. Between 0 volts and pinch off voltage V_P is the ohmic region. After V_P, the regions constant current or active region.

If negative voltage is applied between gate and source the depletion region similar to those obtained with $V_{GS} = 0$ are formed but at lower values of V_{DS}. Therefore saturation level is reached earlier.

We can find two important parameters from the above characteristics

- r_{ds} = drain to source resistance = $\frac{\Delta V_{DS}}{\Delta I_D}$.
- g_m = transconductance of the device = $\frac{\Delta I_D}{\Delta V_{GS}}$.
- The gain of the device, amplification factor $m = r_{ds} g_m$.

SHOCKLEY EQUATION

The FET is a square law device and the drain current I_D is given by the Shockley equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

and $$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

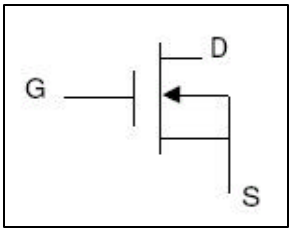
MOSFET

MOSFET stands for metal oxide semiconductor field effect transistor. There are two types of MOSFET

- Depletion type MOSFET
- Enhancement type MOSFET

DEPLETION TYPE MOSFET

CONSTRUCTION



Symbol of n-channel depletion type MOSFET

It consists of a highly doped p-type substrate into which two blocks of heavily doped n-type material are diffused to form a source and drain. A n-channel is formed by diffusing between source and drain. A thin layer of SiO_2 is grown over the entire surface and holes are cut in SiO_2 to make contact with n-type blocks. The gate is also connected to a metal contact surface but remains insulated from the n-channel by the SiO_2 layer. SiO_2 layer results in an extremely high input impedance of the order of 10^{10} to $10^{15}\,\Omega$ for this area.

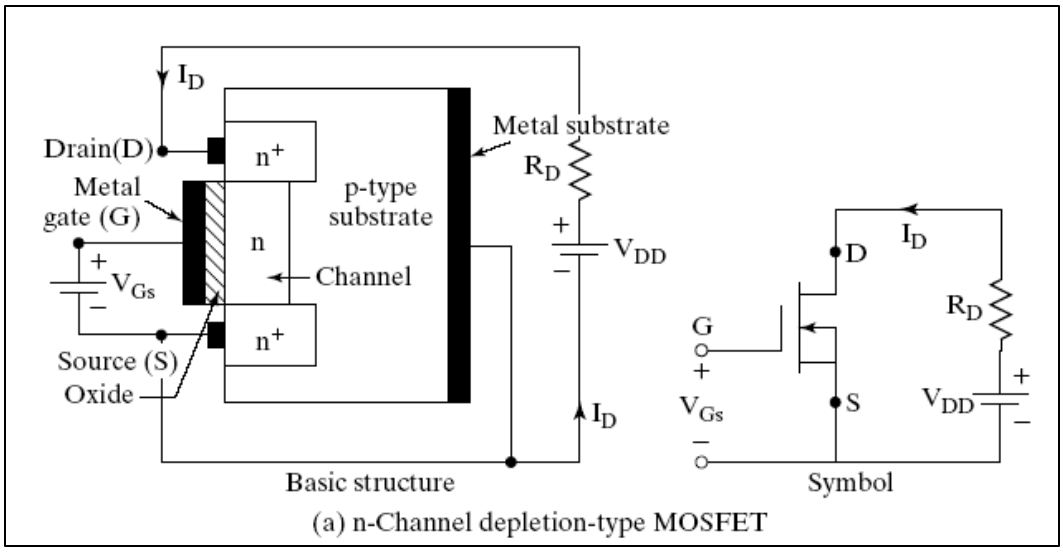


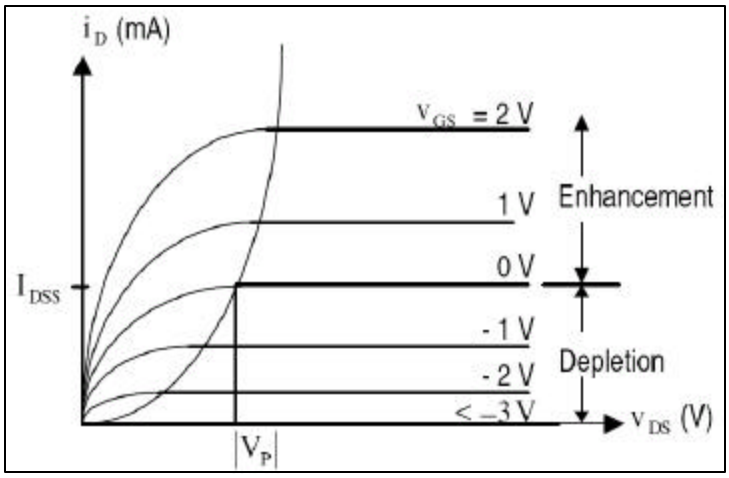
Fig. 4: Structure of n-channel depletion type MOSFET

OPERATION

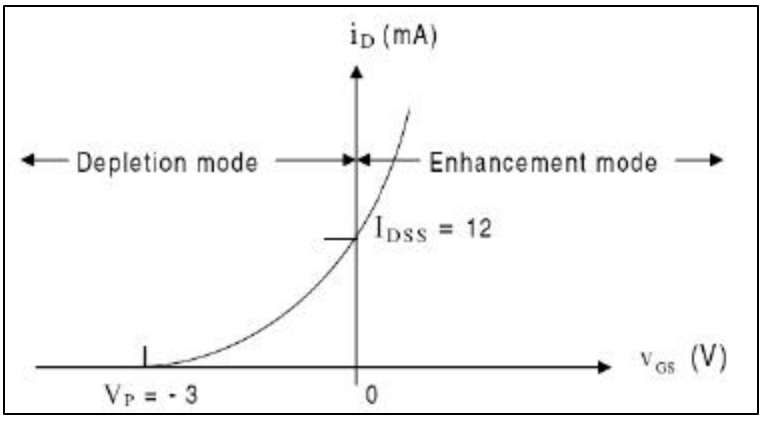
When $V_{GS} = 0V$ and V_{DS} is applied and current flows from drain to source similar to JFET. When $V_{GS} = -1V$, the negative potential will tend to pressure electrons towards the p-type substrate and attracts hole from p-type substrate. Therefore recombination occurs and will reduce the number of free electrons in the n-channel for conduction. Therefore with increased negative gate voltage I_D reduces.

For positive values, V_{gs}, additional electrons from p-substrate will flow into the channel and establish new carriers which will result in an increase in drain current with positive gate voltage.

DRAIN CHARACTERISTICS



TRANSFER CHARACTERISTICS



ENHANCEMENT TYPE MOSFET

Here current control in an n-channel device is now affected by positive gate to source voltage rather than the range of negative voltages of JFET's and depletion type MOSFET.

BASIC CONSTRUCTION

A slab of p-type material is formed and two n-regions are formed in the substrate. The source and drain terminals are connected through metallic contacts to n-doped regions, but the absence of a channel between the doped n-regions. The SiO_2 layer is still present to isolate the gate metallic platform from the region between drain and source, but now it is separated by a section of p-type material.

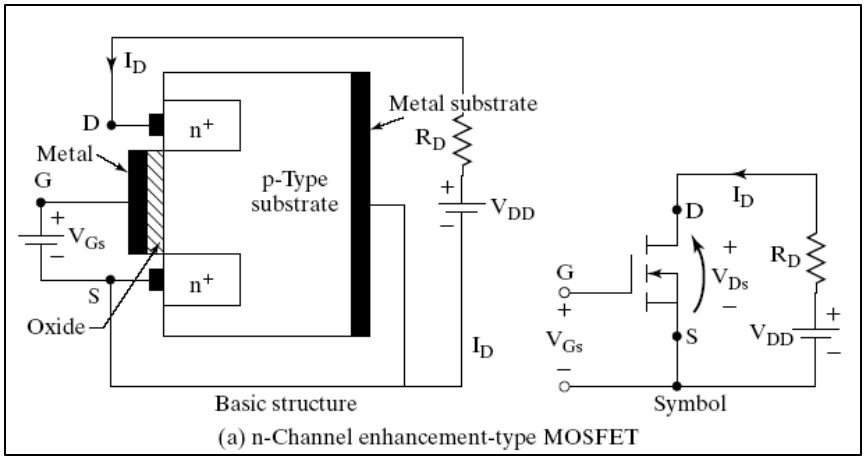


Fig. 5: Structure of n-channel enhancement type MOSFET

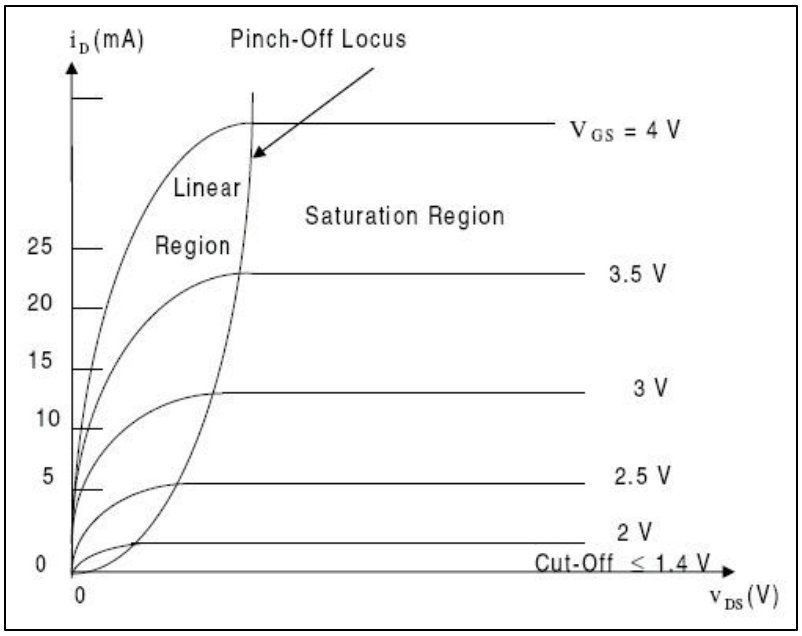
OPERATION

If $V_{GS} = 0V$ and a voltage is applied between the drain and source, the absence of a n-channel will result in a current of effectively zero amperes. With V_{DS} set at some positive voltage and V_{GS} set at 0V, there are two reverse biased pn junction between the n-doped regions and p substrate to oppose any significant flow between drain and source.

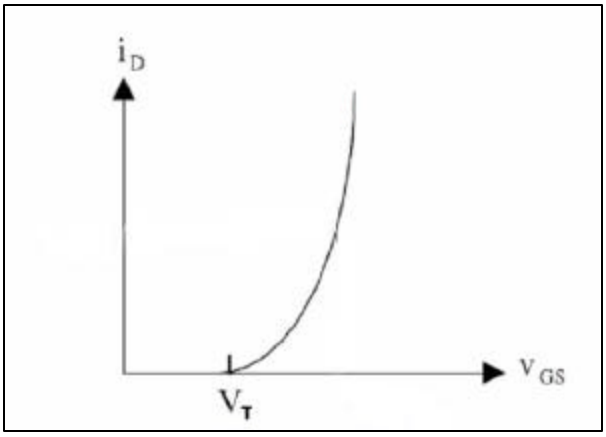
If both V_{DS} and V_{GS} have been set at some positive voltage, then positive potential at the gate will pressure the holes in the p-substrate along the edge of SiO_2 layer to leave the area and enter deeper region of p-substrate. However the electrons in the p-substrate will be attracted to the positive gate and accumulate in the region near the surface of the SiO_2 layer. The negative carriers will not be absorbed due to insulating SiO_2 layer, forming an inversion layer which results in current flow from drain to source.

The level of V_{GS} that results in significant increase in drain current is called threshold voltage V_T. As V_{GS} increases the density of free carriers will increase resulting in increased level of drain current. If V_{GS} is constant V_{DS} is increased; the drain current will eventually reach a saturation level as occurred in JFET.

DRAIN CHARACTERISTICS



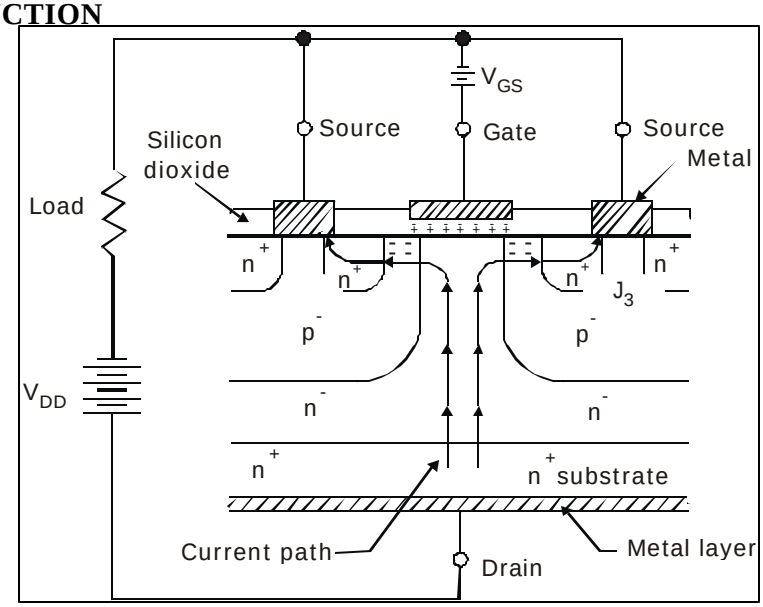
TRANSFER CHARACTERISTICS



POWER MOSFET'S

Power MOSFET's are generally of enhancement type only. This MOSFET is turned 'ON' when a voltage is applied between gate and source. The MOSFET can be turned 'OFF' by removing the gate to source voltage. Thus gate has control over the conduction of the MOSFET. The turn-on and turn-off times of MOSFET's are very small. Hence they operate at very high frequencies; hence MOSFET's are preferred in applications such as choppers and inverters. Since only voltage drive (gate-source) is required, the drive circuits of MOSFET are very simple. The paralleling of MOSFET's is easier due to their positive temperature coefficient. But MOSFTS's have high on-state resistance hence for higher currents; losses in the MOSFET's are substantially increased. Hence MOSFET's are used for low power applications.

CONSTRUCTION



Power MOSFET's have additional features to handle larger powers. On the n^+ substrate high resistivity n^- layer is epitaxially grown. The thickness of n^- layer determines the voltage blocking capability of the device. On the other side of n^+ substrate, a metal layer is deposited to form the drain terminal. Now p^- regions are diffused in the epitaxially grown n^- layer. Further n^+ regions are diffused in the p^- regions as shown. SiO_2 layer is added, which is then etched so as to fit metallic source and gate terminals.

A power MOSFET actually consists of a parallel connection of thousands of basic MOSFET cells on the same single chip of silicon.

When gate circuit voltage is zero and V_{DD} is present, $n^+ - p^-$ junctions are reverse biased and no current flows from drain to source. When gate terminal is made positive with respect to source, an electric field is established and electrons from n^- channel in the p^- regions. Therefore a current from drain to source is established.

Power MOSFET conduction is due to majority carriers therefore time delays caused by removal of recombination of minority carriers is removed.

Because of the drift region the ON state drop of MOSFET increases. The thickness of the drift region determines the breakdown voltage of MOSFET. As seen a parasitic BJT is formed, since emitter base is shorted to source it does not conduct.

SWITCHING CHARACTERISTICS

The switching model of MOSFET's is as shown in the figure 6(a). The various inter electrode capacitance of the MOSFET which cannot be ignored during high frequency switching are represented by C_{gs}, C_{gd} & C_{ds}. The switching waveforms are as shown in figure 7 . The turn on time t_d is the time that is required to charge the input capacitance to the threshold voltage level. The rise time t_r is the gate charging time from this threshold level to the full gate voltage V_{gsp}. The turn off delay time t_{doff} is the time required for the input capacitance to discharge from overdriving the voltage V_1 to the pinch off region. The fall time is the time required for the input capacitance to discharge from pinch off region to the threshold voltage. Thus basically switching ON and OFF depend on the charging time of the input gate capacitance.

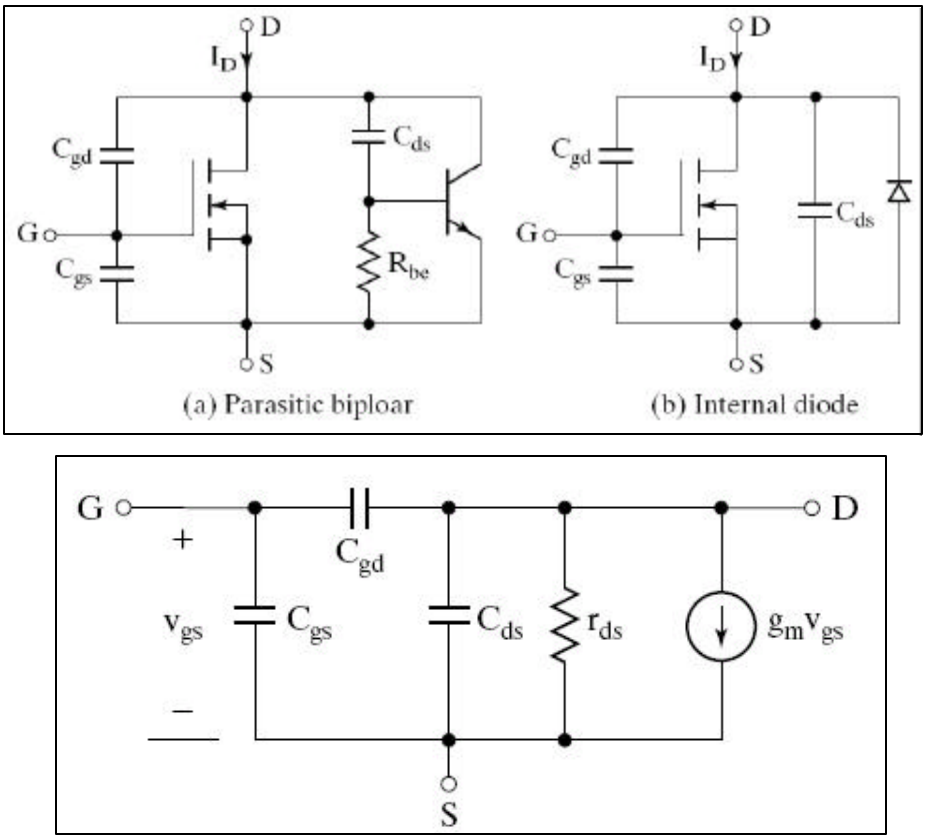
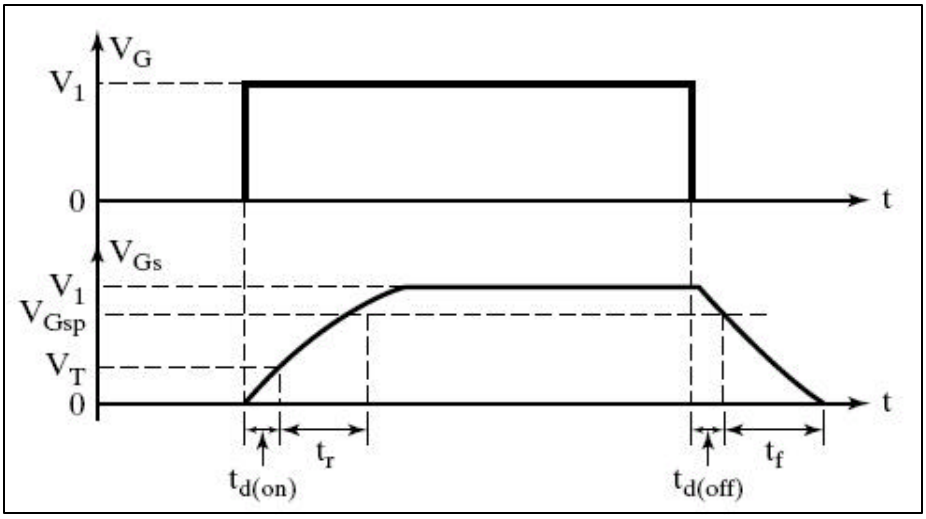


Fig.6: Switching model of MOSFET

Fig.7:



Switching waveforms and times of Power MOSFET

GATE DRIVE

The turn-on time can be reduced by connecting a RC circuit as shown to charge the capacitance faster. When the gate voltage is turned on, the initial charging current of the capacitance is

$$I_G = \frac{V_G}{R_S}.$$

The steady state value of gate voltage is

$$V_{GS} = \frac{R_G V_G}{R_S + R_1 + R_G}.$$

Where R_S is the internal resistance of gate drive force.

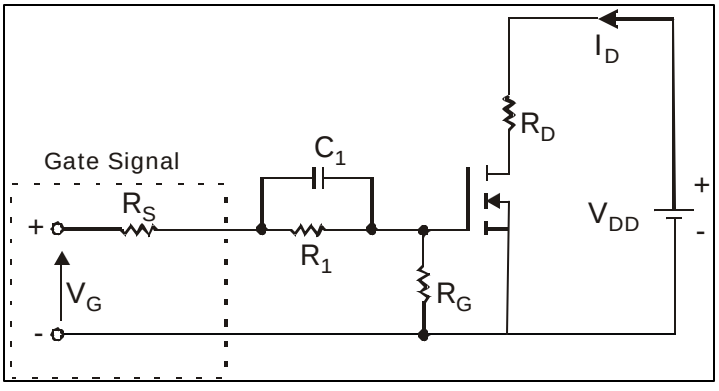


Fig. 8: Fast turn on gate drive circuit 1

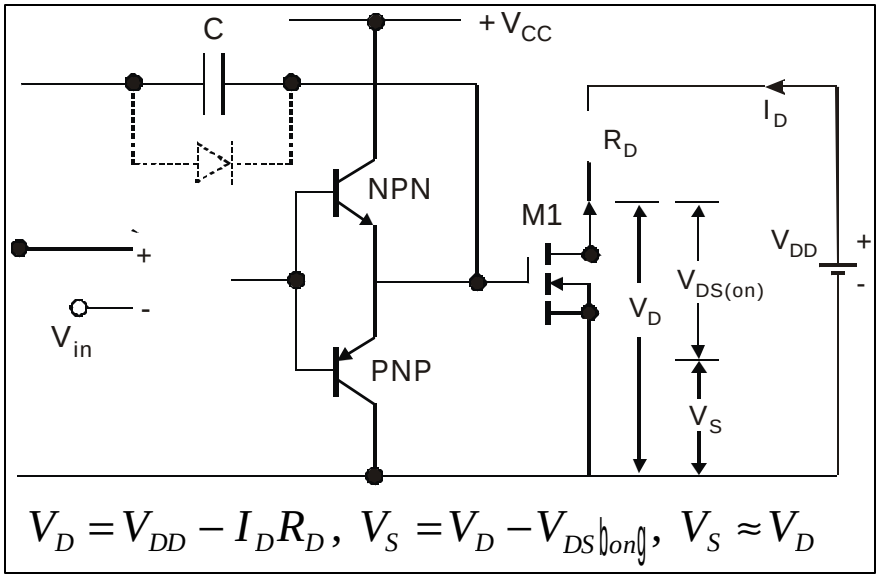


Fig. 8: Fast turn on gate drive circuit 2

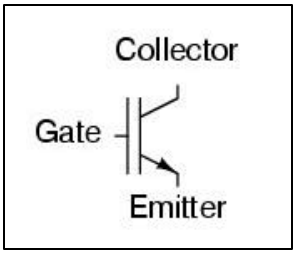
The above circuit is used in order to achieve switching speeds of the order of 100nsec or less. The above circuit as low output impedance and the ability to sink and source large currents. A totem poll arrangement that is capable of sourcing and sinking a large current is achieved by the PNP and NPN transistors. These transistors act as emitter followers and offer a low output impedance. These transistors operate in the linear region therefore minimize the delay time. The gate signal of the power MOSFET may be generated by an op-amp. Let V_{in} be a negative voltage and initially assume that the MOSFET is off therefore the non-inverting terminal of the op-amp is at zero potential. The op-amp output is high therefore the NPN transistor is on and is a source of a large current since it is an emitter follower. This enables the gate-source capacitance C_{gs} to quickly charge upto the gate voltage required to turn-on the power MOSFET. Thus high speeds are achieved. When V_{in} becomes positive the output of op-amp becomes negative the PNP transistor turns-on and the gate-source capacitor quickly discharges through the PNP transistor. Thus the PNP transistor acts as a current sink and the MOSFET is quickly turned-off. The capacitor C helps in regulating the rate of rise and fall of the gate voltage thereby controlling the rate of rise and fall of MOSFET drain current. This can be explained as follows

- The drain-source voltage $V_{DS} = V_{DD} - I_D R_D$.
- If I_D increases V_{DS} reduces. Therefore the positive terminal of op-amp which is tied to the source terminal of the MOSFET feels this reduction and this reduction is transmitted to gate through the capacitor 'C' and the gate voltage reduces and the drain current is regulated by this reduction.

COMPARISON OF MOSFET WITH BJT

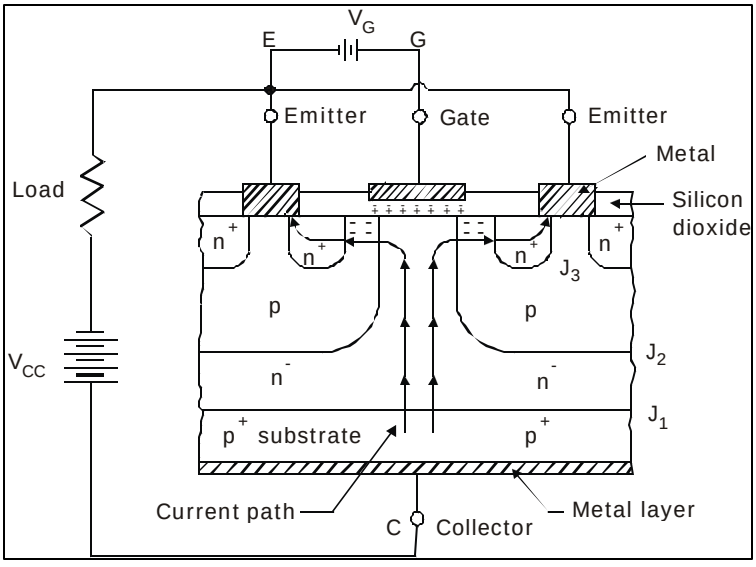
- Power MOSFETS have lower switching losses but its on-resistance and conduction losses are more. A BJT has higher switching loss bit lower conduction loss. So at high frequency applications power MOSFET is the obvious choice. But at lower operating frequencies BJT is superior.
- MOSFET has positive temperature coefficient for resistance. This makes parallel operation of MOSFET's easy. If a MOSFET shares increased current initially, it heats up faster, its resistance increases and this increased resistance causes this current to shift to other devices in parallel. A BJT is a negative temperature coefficient, so current shaving resistors are necessary during parallel operation of BJT's.
- In MOSFET secondary breakdown does not occur because it have positive temperature coefficient. But BJT exhibits negative temperature coefficient which results in secondary breakdown.
- Power MOSFET's in higher voltage ratings have more conduction losses.
- Power MOSFET's have lower ratings compared to BJT's . Power MOSFET's $\rightarrow$ 500V to 140A, BJT $\rightarrow$ 1200V, 800A.

MOSIGT OR IGBT



The metal oxide semiconductor insulated gate transistor or IGBT combines the advantages of BJT's and MOSFET's. Therefore an IGBT has high input impedance like a MOSFET and low-on state power loss as in a BJT. Further IGBT is free from second breakdown problem present in BJT.

IGBT BASIC STRUCTURE AND WORKING

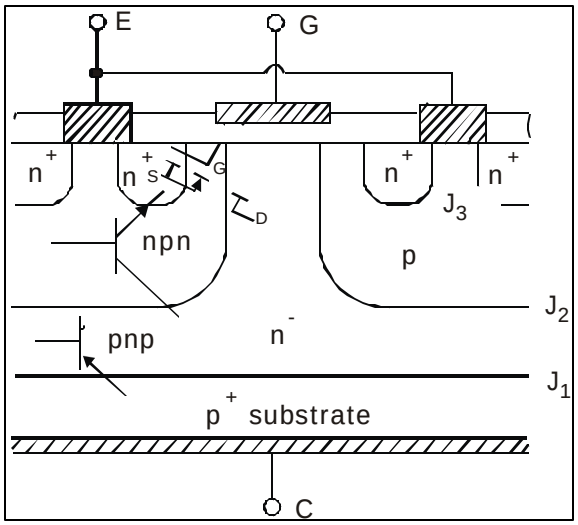


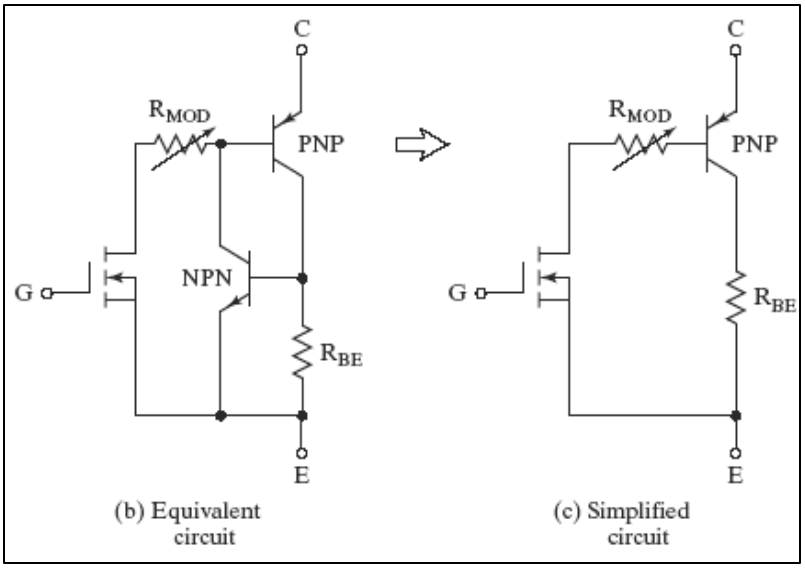
It is constructed virtually in the same manner as a power MOSFET. However, the substrate is now a p^+ layer called the collector.

When gate is positive with respect to positive with respect to emitter and with gate emitter voltage greater than V_{GSTH}, an n channel is formed as in case of power MOSFET. This n^- channel short circuits the n^- region with n^+ emitter regions.

An electron movement in the n^- channel in turn causes substantial hole injection from p^+ substrate layer into the epitaxially n^- layer. Eventually a forward current is established.

The three layers p^+, n^- and p constitute a pnp transistor with p^+ as emitter, n^- as base and p as collector. Also n^-, p and n^+ layers constitute a npn transistor. The MOSFET is formed with input gate, emitter as source and n^- region as drain. Equivalent circuit is as shown below.





Also p serves as collector for pnp device and also as base for npn transistor. The two pnp and npn is formed as shown.

When gate is applied $(V_{GS} > V_{GSth})$ MOSFET turns on. This gives the base drive to T_1. Therefore T_1 starts conducting. The collector of T_1 is base of T_2. Therefore regenerative action takes place and large number of carriers are injected into the n^- drift region. This reduces the ON-state loss of IGBT just like BJT.

When gate drive is removed IGBT is turn-off. When gate is removed the induced channel will vanish and internal MOSFET will turn-off. Therefore T_1 will turn-off it T_2 turns off.

Structure of IGBT is such that R_1 is very small. If R_1 small T_1 will not conduct therefore IGBT's are different from MOSFET's since resistance of drift region reduces when gate drive is applied due to p^+ injecting region. Therefore ON state IGBT is very small.

IGBT CHARACTERISTICS

STATIC CHARACTERISTICS

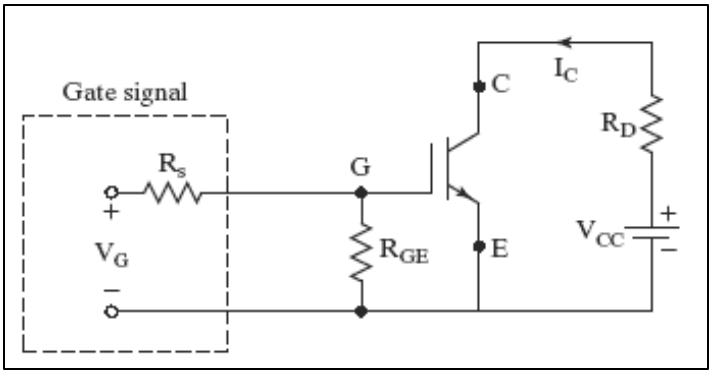


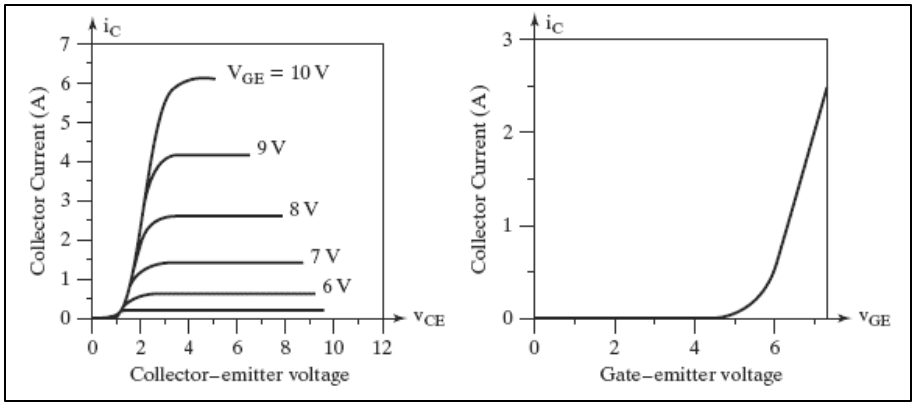
Fig. 9: IGBT bias circuit

Static V-I characteristics (I_C versus V_{CE})

Same as in BJT except control is by V_{GE}. Therefore IGBT is a voltage controlled device.

Transfer Characteristics (I_C versus V_{GE})

Identical to that of MOSFET. When $V_{GE} < V_{GET}$, IGBT is in off-state.



APPLICATIONS

Widely used in medium power applications such as DC and AC motor drives, UPS systems, Power supplies for solenoids, relays and contractors.

Though IGBT's are more expensive than BJT's, they have lower gate drive requirements, lower switching losses. The ratings up to 1200V, 500A.

SERIES AND PARALLEL OPERATION

Transistors may be operated in series to increase their voltage handling capability. It is very important that the series-connected transistors are turned on and off simultaneously. Other wise, the slowest device at turn-on and the fastest devices at turn-off will be subjected to the full voltage of the collector emitter circuit and the particular device may be destroyed due to high voltage. The devices should be matched for gain, transconductance, threshold voltage, on state voltage, turn-on time, and turn-off time. Even the gate or base drive characteristics should be identical.

Transistors are connected in parallel if one device cannot handle the load current demand. For equal current sharings, the transistors should be matched for gain, transconductance, saturation voltage, and turn-on time and turn-off time. But in practice, it is not always possible to meet these requirements. A reasonable amount of current sharing (45 to 55% with two transistors) can be obtained by connecting resistors in series with the emitter terminals as shown in the figure 10.

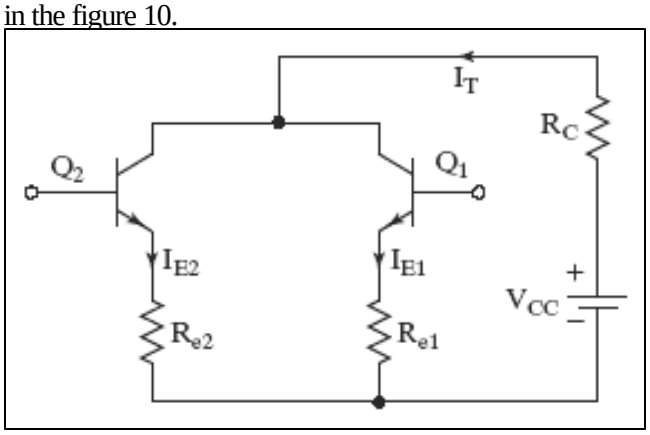


Fig. 10: Parallel connection of Transistors

The resistor will help current sharing under steady state conditions. Current sharing under dynamic conditions can be accomplished by connecting coupled inductors. If the current through Q_1 rises, the $l(di/dt)$ across L_1 increases, and a corresponding voltage of opposite polarity is induced across inductor L_2. The result is low impedance path, and the current is shifted to Q_2. The inductors would generate voltage spikes and they may be expensive and bulky, especially at high currents.

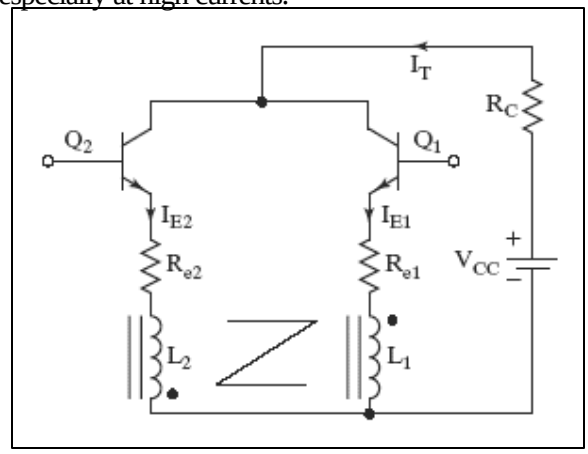


Fig. 11: Dynamic current sharing

BJTs have a negative temperature coefficient. During current sharing, if one BJT carries more current, its on-state resistance decreases and its current increases further, whereas MOSFETS have positive temperature coefficient and parallel operation is relatively easy. The MOSFET that initially draws higher current heats up faster and its on-state resistance increases, resulting in current shifting to the other devices. IGBTs require special care to match the characteristics due to the variations of the temperature coefficients with the collector current.

PROBLEM

1. Two MOSFETS which are connected in parallel carry a total current of $I_T = 20A$. The drain to source voltage of MOSFET M_1 is $V_{DS1} = 2.5V$ and that of MOSFET M_2 is $V_{DS2} = 3V$. Determine the drain current of each transistor and difference in current sharing it the current sharing series resistances are (a) $R_{s1} = 0.3\Omega$ and $R_{s2} = 0.2\Omega$, and (b) $R_{s1} = R_{s2} = 0.5\Omega$.

Solution

(a) $I_{D1} + I_{D2} = I_T \;\&\; V_{DS1} + I_{D1}R_{s1} = V_{DS2} + I_{D2}R_{s2} = R_{s2}(I_T - I_D)$

$$I_{D1} = \frac{V_{DS2} - V_{DS1} + I_T R_{s2}}{R_{s1} + R_{s2}}$$

$$I_{D1} = \frac{3 - 2.5 + 20 \times 0.2}{0.3 + 0.2} = 9A \quad or \quad 45\%$$

$$I_{D2} = 20 - 9 = 11A \quad or \quad 55\%$$

$$\Delta I = 55 - 45 = 10\%$$

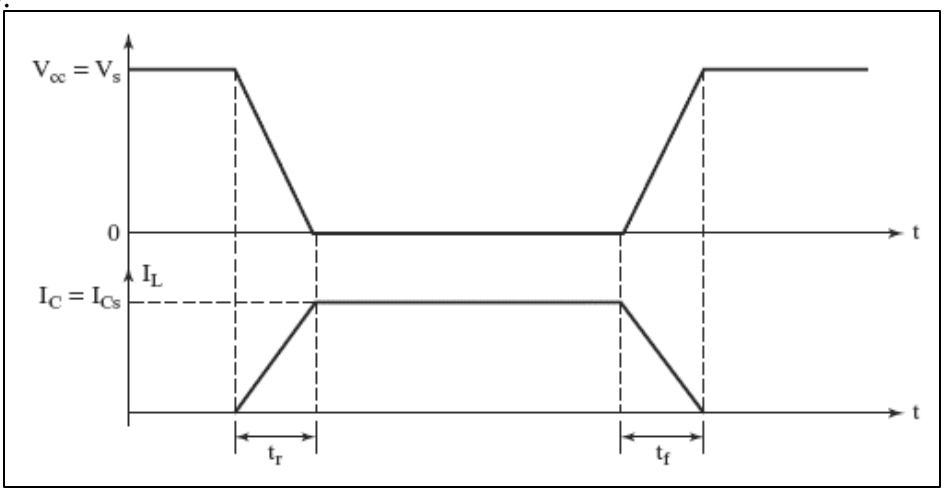
(b) $I_{D1} = \dfrac{3 - 2.5 + 20 \times 0.5}{0.5 + 0.5} = 10.5A \quad or \quad 52.5\%$

$I_{D2} = 20 - 10.5 = 9.5A \quad or \quad 47.5\%$

$\Delta I = 52.5 - 47.5 = 5\%$

di/dt AND dv/dt LIMITATIONS

Transistors require certain turn-on and turn-off times. Neglecting the delay time t_d and the storage time t_s, the typical voltage and current waveforms of a BJT switch is shown below.



During turn-on, the collector rise and the di/dt is

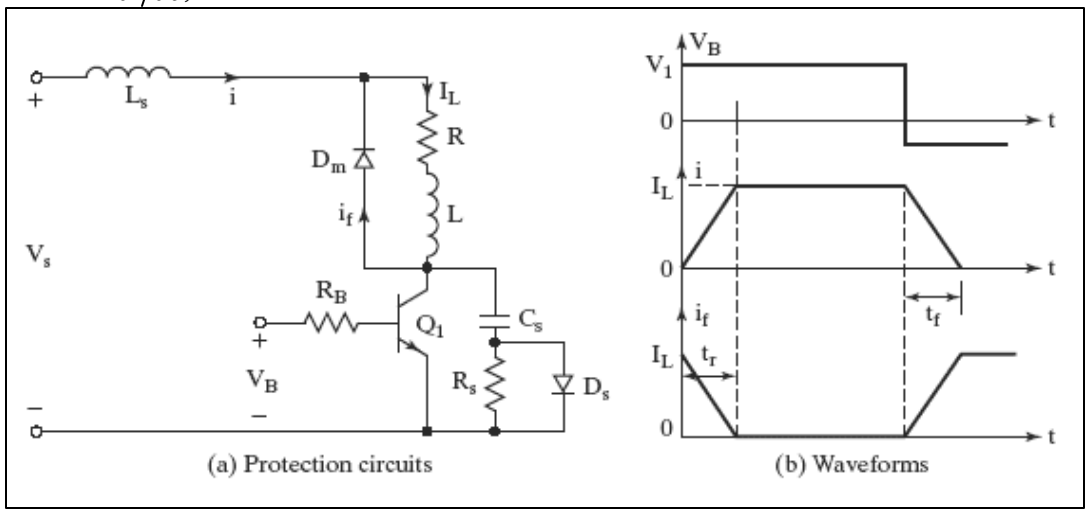
$$\frac{di}{dt} = \frac{I_L}{t_r} = \frac{I_{cs}}{t_r} \quad ...(1)$$

During turn off, the collector emitter voltage must rise in relation to the fall of the collector current, and is

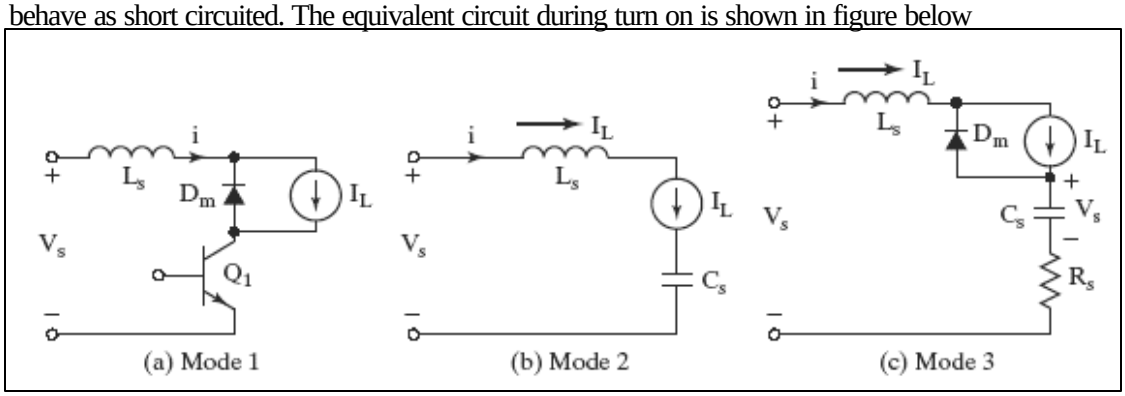
$$\frac{dv}{dt} = \frac{V_s}{t_f} = \frac{V_{cc}}{t_f} \quad ...(2)$$

The conditions di/dt and dv/dt in equation (1) and (2) are set by the transistor switching characteristics and must be satisfied during turn on and turn off. Protection circuits are normally required to keep the operating di/dt and dv/dt within the allowable

limits of transistor. A typical switch with di/dt and dv/dt protection is shown in figure (a), with operating wave forms in figure (b). The RC network across the transistor is known as the snubber circuit or snubber and limits the dv/dt. The inductor L_S, which limits the di/dt, is sometimes called series snubber.



Let us assume that under steady state conditions the load current I_L is free wheeling through diode D_m, which has negligible reverse reco`very time. When transistor Q_1 is turned on, the collector current rises and current of diode D_m falls, because D_m will behave as short circuited. The equivalent circuit during turn on is shown in figure below



The turn on di/dt is

$$\frac{di}{dt} = \frac{V_s}{L_s} \qquad ...(3)$$

Equating equations (1) and (3) gives the value of L_s

$$L_s = \frac{V_s t_r}{I_L} \qquad ...(4)$$

During turn off, the capacitor C_s will charge by the load current and the equivalent circuit is shown in figure (4). The capacitor voltage will appear across the transistor and the dv/dt is

$$\frac{dv}{dt} = \frac{I_L}{C_s} \qquad ...(5)$$

Equating equation (2) to equation (5) gives the required value of capacitance,

$$C_s = \frac{I_L t_f}{V_s} \qquad ...(6)$$

Once the capacitor is charge to V_s, the freewheeling diode will turn on. Due to the energy stored in L_s, there will be damped resonant circuit as shown in figure (5). The RLC circuit is normally made critically damped to avoid oscillations. For unity critical damping, $d = 1$, and equation $d = \frac{a}{w_0} = \frac{R}{2}\sqrt{\frac{C}{L}}$ yields

$$R_s = 2\sqrt{\frac{L_s}{C_s}}$$

The capacitor C_s has to discharge through the transistor and the increase the peak current rating of the transistor. The discharge through the transistor can be avoided by placing resistor R_s across C_s instead of placing R_s across D_s.

The discharge current is shown in figure below. When choosing the value of R_s, the discharge time, $R_s C_s = t_s$ should also be considered. A discharge time of one third the switching period, T_s is usually adequate.

$$3R_s C_s = T_s = \frac{1}{f_s}$$

$$R_s = \frac{1}{3 f_s C_s}$$

ISOLATION OF GATE AND BASE DRIVES

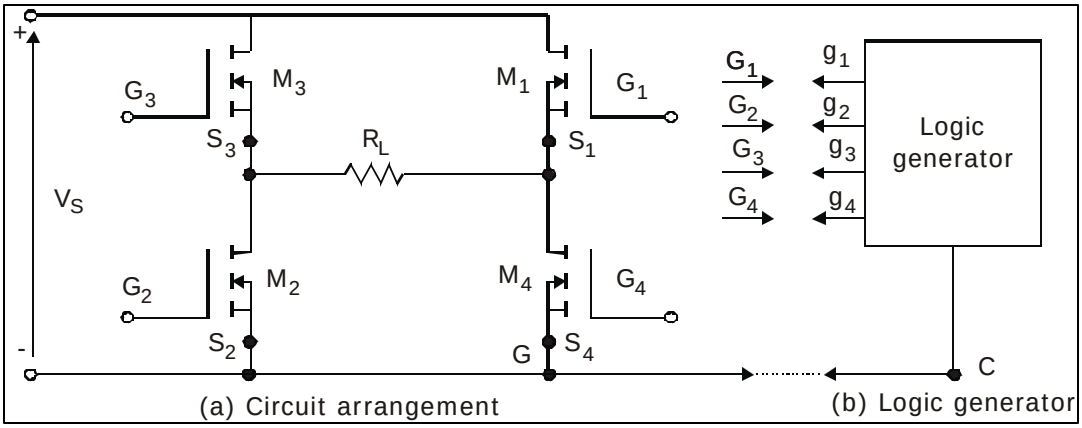
Necessity

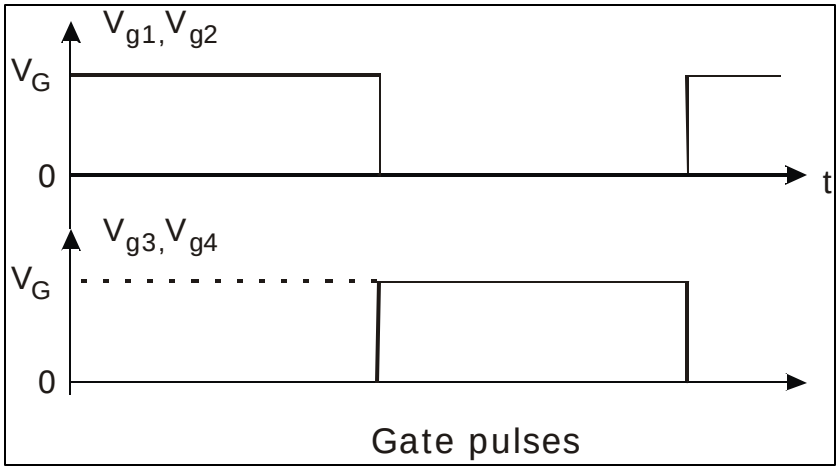
Driver circuits are operated at very low power levels. Normally the gating circuit are digital in nature which means the signal levels are 3 to 12 volts. The gate and base drives are connected to power devices which operate at high power levels.

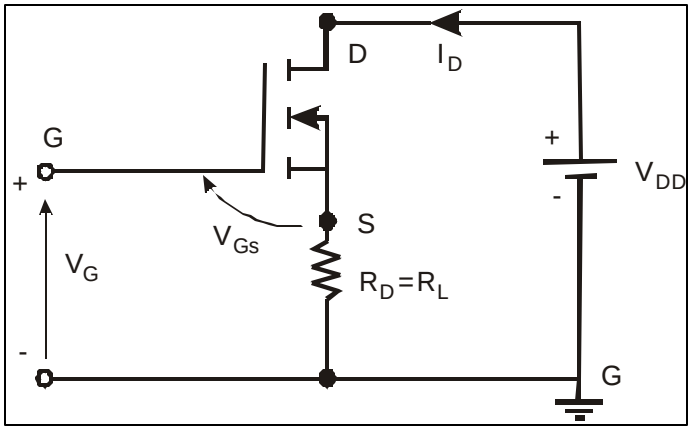
Illustration

The logic circuit generates four pulses; these pulses have common terminals. The terminal g, which has a voltage of V_G, with respect to terminal C, cannot be connected

directly to gate terminal G, therefore V_{g1} should be applied between G_1 & S_1 of transistor Q_1. Therefore there is need for isolation between logic circuit and power transistor.







$$V_{GS} = V_G - I_D R_D$$

There are two ways of floating or isolating control or gate signal with respect to ground.

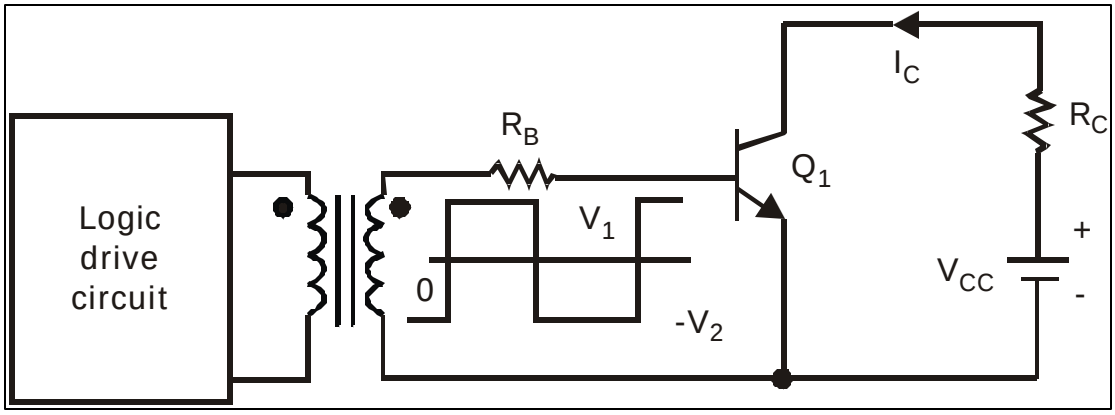
- Pulse transformers
- Optocouplers

PULSE TRANSFORMERS

Pulse transformers have one primary winding and can have one or more secondary windings.

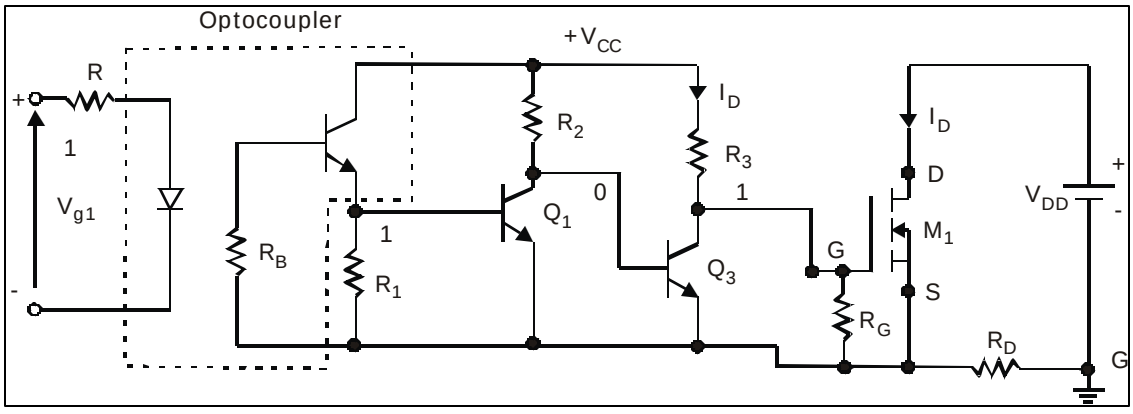
Multiple secondary windings allow simultaneous gating signals to series and parallel connected transistors. The transformer should have a very small leakage inductance and the rise time of output should be very small.

The transformer would saturate at low switching frequency and output would be distorted.



OPTOCOUPLERS

Optocouplers combine infrared LED and a silicon photo transistor. The input signal is applied to ILED and the output is taken from the photo transistor. The rise and fall times of photo transistor are very small with typical values of turn on time = $2.5ms$ and turn off of 300ns. This limits the high frequency applications. The photo transistor could be a darlington pair. The phototransistor require separate power supply and add to complexity and cost and weight of driver circuits.



THYRISTORS

A thyristor is the most important type of power semiconductor devices. They are extensively used in power electronic circuits. They are operated as bi-stable switches from non-conducting to conducting state.

A thyristor is a four layer, semiconductor of p-n-p-n structure with three pn junctions. It has three terminals, the anode, cathode and the gate.

The word thyristor is coined from thyratron and transistor. It was invented in the year 1957 at Bell Labs. The Different types of Thyristors are

- Silicon Controlled Rectifier (SCR).
- TRIAC
- DIAC
- Gate Turn Off Thyristor (GTO)

SILICON CONTROLLED RECTIFIER (SCR)

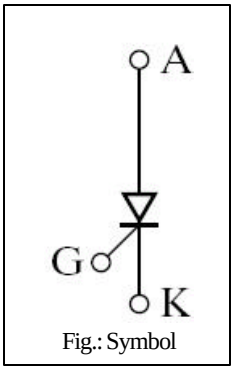


Fig.: Symbol

The SCR is a four layer three terminal device with junctions J_1, J_2, J_3 as shown. The construction of SCR shows that the gate terminal is kept nearer the cathode. The approximate thickness of each layer and doping densities are as indicated in the figure. In terms of their lateral dimensions Thyristors are the largest semiconductor devices made. A complete silicon wafer as large as ten centimeter in diameter may be used to make a single high power thyristor.

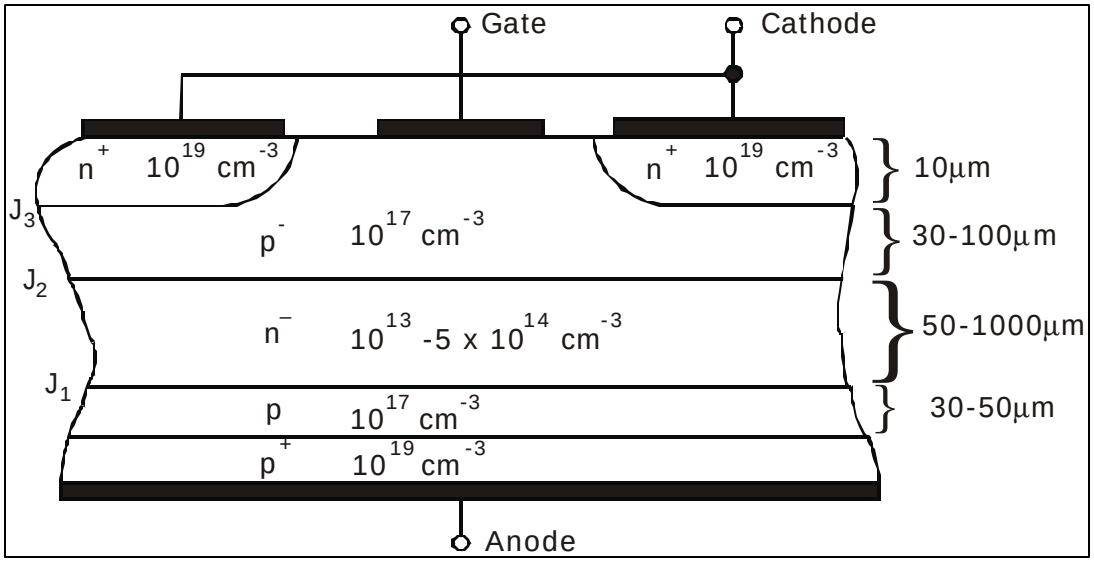


Fig.: Structure of a generic thyristor

QUALITATIVE ANALYSIS

When the anode is made positive with respect the cathode junctions $J_1 \& J_3$ are forward biased and junction J_2 is reverse biased. With anode to cathode voltage V_{AK} being small, only leakage current flows through the device. The SCR is then said to be in the forward blocking state. If V_{AK} is further increased to a large value, the reverse biased junction J_2 will breakdown due to avalanche effect resulting in a large current through the device. The voltage at which this phenomenon occurs is called the forward breakdown voltage V_{BO}. Since the other junctions $J_1 \& J_3$ are already forward biased, there will be free movement of carriers across all three junctions resulting in a large forward anode current. Once the SCR is switched on, the voltage drop across it is very small, typically 1 to 1.5V. The anode current is limited only by the external impedance present in the circuit.

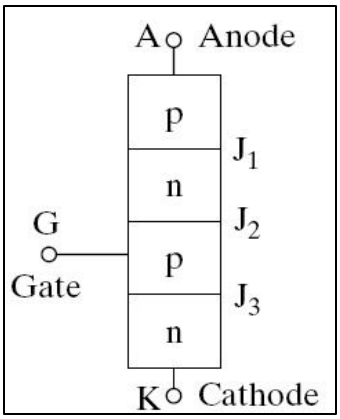


Fig.: Simplified model of a thyristor

Although an SCR can be turned on by increasing the forward voltage beyond V_{BO}, in practice, the forward voltage is maintained well below V_{BO} and the SCR is turned on by applying a positive voltage between gate and cathode. With the application of positive gate voltage, the leakage current through the junction J_2 is increased. This is because the resulting gate current consists mainly of electron flow from cathode to gate. Since the bottom end layer is heavily doped as compared to the p-layer, due to the applied voltage, some of these electrons reach junction J_2 and add to the minority carrier concentration in the p-layer. This raises the reverse leakage current and results in breakdown of junction J_2 even though the applied forward voltage is less than the breakdown voltage V_{BO}. With increase in gate current breakdown occurs earlier.

V-I CHARACTERISTICS

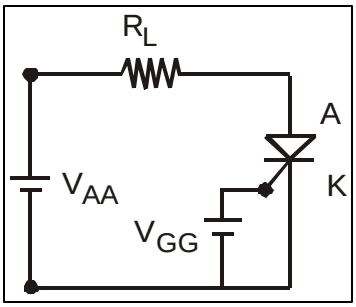


Fig. Circuit

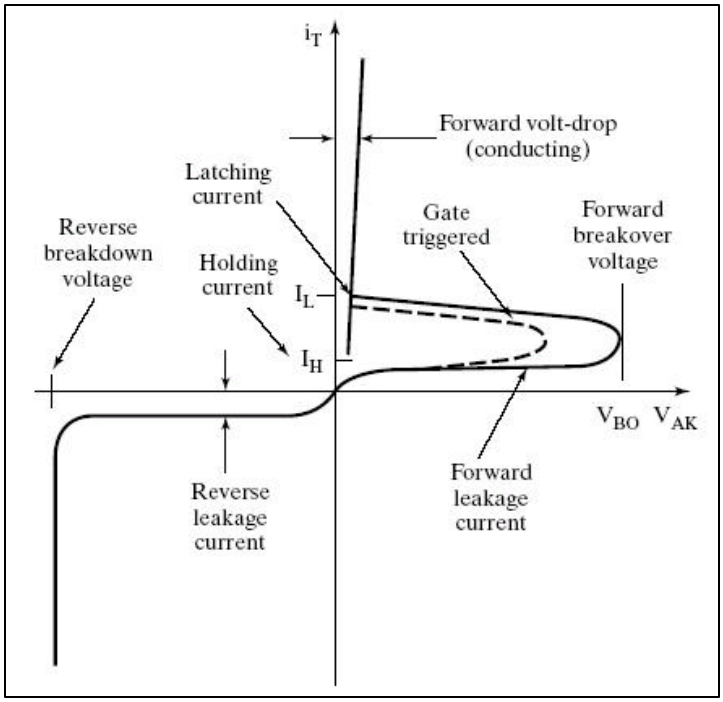


Fig: V-I Characteristics

A typical V-I characteristics of a thyristor is shown above. In the reverse direction the thyristor appears similar to a reverse biased diode which conducts very little current until avalanche breakdown occurs. In the forward direction the thyristor has two stable states or modes of operation that are connected together by an unstable mode that appears as a negative resistance on the V-I characteristics. The low current high voltage region is the forward blocking state or the off state and the low voltage high current mode is the on state. For the forward blocking state the quantity of interest is the forward blocking voltage V_{BO} which is defined for zero gate current. If a positive gate current is applied to a thyristor then the transition or break over to the on state will occur at smaller values of

anode to cathode voltage as shown. Although not indicated the gate current does not have to be a dc current but instead can be a pulse of current having some minimum time duration. This ability to switch the thyristor by means of a current pulse is the reason for wide spread applications of the device.

However once the thyristor is in the on state the gate cannot be used to turn the device off. The only way to turn off the thyristor is for the external circuit to force the current through the device to be less than the holding current for a minimum specified time period.

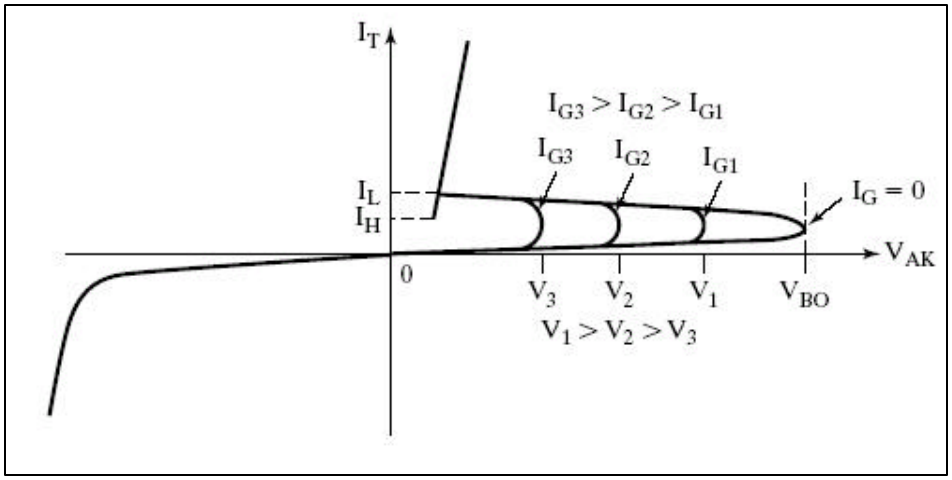


Fig.: Effects on gate current on forward blocking voltage

HOLDING CURRENT I_H

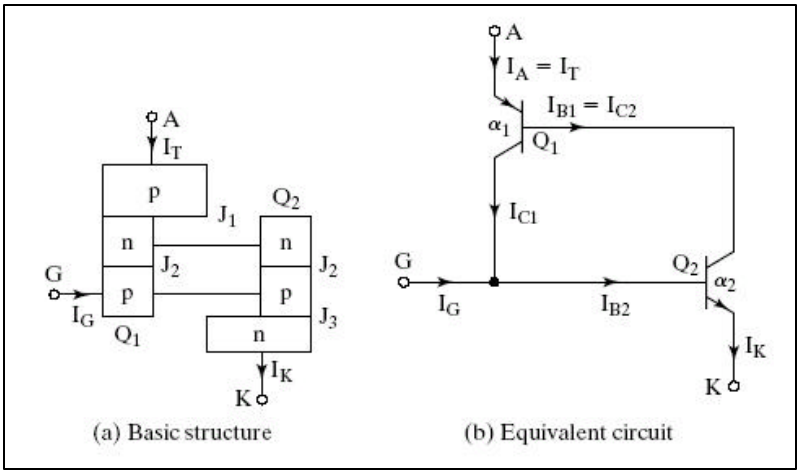
After an SCR has been switched to the on state a certain minimum value of anode current is required to maintain the thyristor in this low impedance state. If the anode current is reduced below the critical holding current value, the thyristor cannot maintain the current through it and reverts to its off state usually I_m is associated with turn off the device.

LATCHING CURRENT I_L

After the SCR has switched on, there is a minimum current required to sustain conduction. This current is called the latching current. I_L associated with turn on and is usually greater than holding current.

QUANTITATIVE ANALYSIS

TWO TRANSISTOR MODEL



The general transistor equations are,

$$I_C = b\, I_B + (1+ b)\, I_{CBO}$$
$$I_C = a\, I_E + I_{CBO}$$
$$I_E = I_C + I_B$$
$$I_B = I_E (1-a) - I_{CBO}$$

The SCR can be considered to be made up of two transistors as shown in above figure.

Considering PNP transistor of the equivalent circuit,

$$I_{E_1} = I_A, I_C = I_{C_1}, a = a_1, I_{CBO} = I_{CBO_1}, I_B = I_{B_1}$$
$$\therefore \qquad I_{B_1} = I_A (1-a_1) - I_{CBO_1} \qquad ---(1)$$

Considering NPN transistor of the equivalent circuit,

$$I_C = I_{C_2}, I_B = I_{B_2}, I_{E_2} = I_K = I_A + I_G$$
$$I_{C_2} = a_2 I_k + I_{CBO_2}$$
$$I_{C_2} = a_2 (I_A + I_G) + I_{CBO_2} \qquad ---(2)$$

From the equivalent circuit, we see that

$$\therefore \qquad I_{C_2} = I_{B_1}$$
$$\Rightarrow \qquad I_A = \frac{a_2 I_g + I_{CBO1} + I_{CBO2}}{1-(a_1 + a_2)}$$

Two transistors analog is valid only till SCR reaches ON state

Case 1: When $I_g = 0$,

$$I_A = \frac{I_{CBO_1} + I_{CBO_2}}{1-(a_1 + a_2)}$$

The gain a_1 of transistor T_1 varies with its emitter current $I_E = I_A$. Similarly varies with $I_E = I_A + I_g = I_K$. In this case, with $I_g = 0$, a_2 varies only with I_A. Initially when the applied forward voltage is small, $(a_1 + a_2) < 1$.

If however the reverse leakage current is increased by increasing the applied forward voltage, the gains of the transistor increase, resulting in $(a_1 + a_2) \to 1$.

From the equation, it is seen that when $(a_1 + a_2) = 1$, the anode current I_A tends towards ∞. This explains the increase in anode current for the break over voltage V_{B0}.

Case 2: With gate current I_g applied.

When sufficient gate drive is applied, we see that $I_{B_2} = I_g$ is established. This in turn results in a current through transistor T_2, this increases a_2 of T_2. But with the existence of $I_{C_2} = b_2 I_{b_2} = b_2 I_g$, a current through T, is established. Therefore, $I_{C_1} = b_1 I_{B_1} = b_1 b_2 I_{B_2} = b_1 b_2 I_g$. This current in turn is connected to the base of T_2. Thus the base drive of T_2 is increased which in turn increases the base drive of T_1, therefore regenerative feedback or positive feedback is established between the two transistors. This causes $(a_1 + a_2)$ to tend to unity therefore the anode current begins to grow towards a large value. This regeneration continues even if I_g is removed this characteristic of SCR makes it suitable for pulse triggering; SCR is also called a Lathing Device.

SWITCHING CHARACTERISTICS (DYNAMIC CHARACTERISTICS)

THYRISTOR TURN-ON CHARACTERISTICS

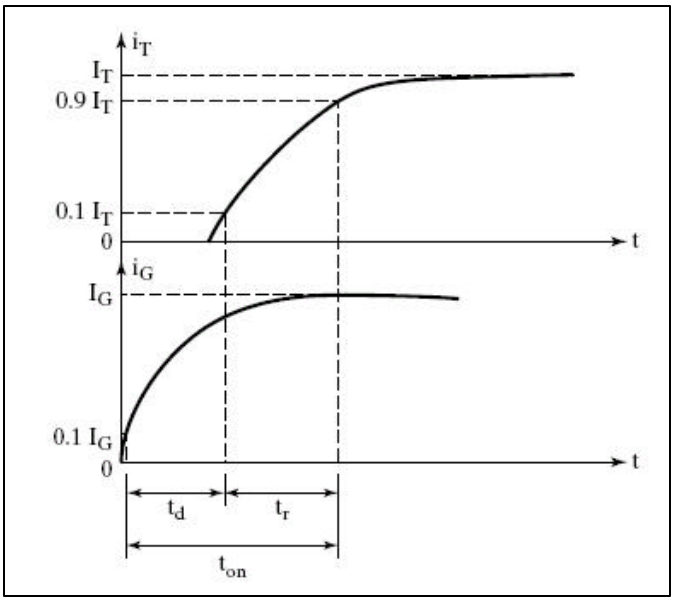
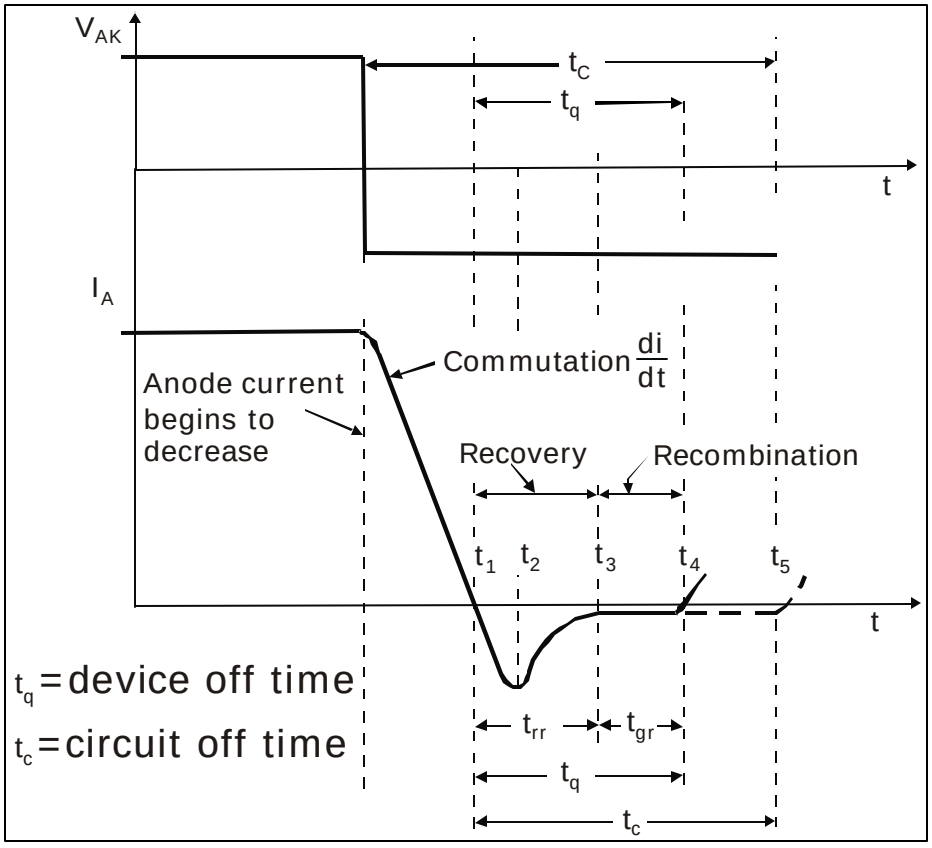


Fig.: Turn-on characteristics

When the SCR is turned on with the application of the gate signal, the SCR does not conduct fully at the instant of application of the gate trigger pulse. In the beginning, there is no appreciable increase in the SCR anode current, which is because, only a small portion of the silicon pellet in the immediate vicinity of the gate electrode starts conducting. The duration between 90% of the peak gate trigger pulse and the instant the forward voltage has fallen to 90% of its initial value is called the gate controlled / trigger delay time t_{gd}. It is also defined as the duration between 90% of the gate trigger pulse and the instant at which the anode current rises to 10% of its peak value. t_{gd} is usually in the range of 1μsec.

Once t_{gd} has lapsed, the current starts rising towards the peak value. The period during which the anode current rises from 10% to 90% of its peak value is called the rise time. It is also defined as the time for which the anode voltage falls from 90% to 10% of its peak value. The summation of t_{gd} and t_r gives the turn on time t_{on} of the thyristor.

THYRISTOR TURN OFF CHARACTERISTICS



When an SCR is turned on by the gate signal, the gate loses control over the device and the device can be brought back to the blocking state only by reducing the forward current to a level below that of the holding current. In AC circuits, however, the current goes through a natural zero value and the device will automatically switch off. But in DC circuits, where no neutral zero value of current exists, the forward current is reduced by applying a reverse voltage across anode and cathode and thus forcing the current through the SCR to zero.

As in the case of diodes, the SCR has a reverse recovery time t_{rr} which is due to charge storage in the junctions of the SCR. These excess carriers take some time for recombination resulting in the gate recovery time or reverse recombination time t_{gr}. Thus, the turn-off time t_q is the sum of the durations for which reverse recovery current flows after the application of reverse voltage and the time required for the recombination of all excess carriers present. At the end of the turn off time, a depletion layer develops across J_2 and the junction can now withstand the forward voltage. The turn off time is dependent on the anode current, the magnitude of reverse V_g applied ad the magnitude and rate of application of the forward voltage. The turn off time for converte grade SCR's is 50 to 100µsec and that for inverter grade SCR's is 10 to 20µsec.

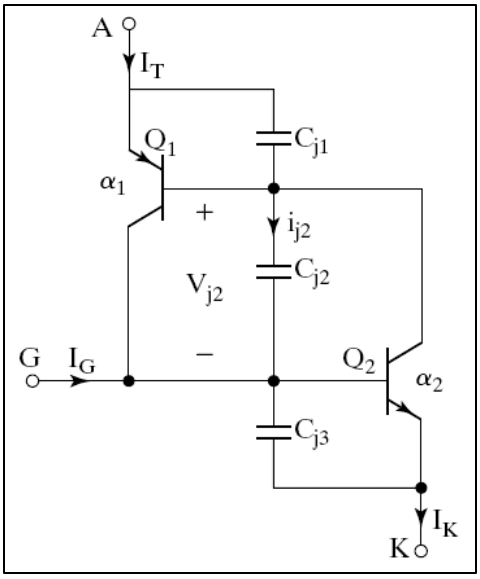
To ensure that SCR has successfully turned off , it is required that the circuit off time t_c be greater than SCR turn off time t_q .

THYRISTOR TURN ON

- **Thermal Turn on:** If the temperature of the thyristor is high, there will be an increase in charge carriers which would increase the leakage current. This would cause an increase in a_1 & a_2 and the thyristor may turn on. This type of turn on many cause thermal run away and is usually avoided.
- **Light**: If light be allowed to fall on the junctions of a thyristor, charge carrier concentration would increase which may turn on the SCR.
- **LASCR:** Light activated SCRs are turned on by allowing light to strike the silicon wafer.
- **High Voltage Triggering:** This is triggering without application of gate voltage with only application of a large voltage across the anode-cathode such that it is greater than the forward breakdown voltage V_{BO}. This type of turn on is destructive and should be avoided.
- **Gate Triggering:** Gate triggering is the method practically employed to turn-on the thyristor. Gate triggering will be discussed in detail later.
- $\frac{dv}{dt}$ **Triggering:** Under transient conditions, the capacitances of the p-n junction will influence the characteristics of a thyristor. If the thyristor is in the blocking state, a rapidly rising voltage applied across the device would cause a high current to flow through the device resulting in turn-on. If i_{j_2} is the current throught the junction j_2 and C_{j_2} is the junction capacitance and V_{j_2} is the voltage across j_2, then

$$i_{j_2} = \frac{dq_2}{dt} = \frac{d}{dt}\left(C_{j_2} V_{j_2}\right) = \frac{C_{j_2} dV_{J2}}{dt} + V_{j_2} \frac{dC_{j_2}}{dt}$$

From the above equation, we see that if $\frac{dv}{dt}$ is large, 1_{j_2} will be large. A high value of charging current may damage the thyristor and the device must be protected against high $\frac{dv}{dt}$. The manufacturers specify the allowable $\frac{dv}{dt}$.



THYRISTOR RATINGS

First Subscript	Second Subscript	Third Subscript
D → off state	W → working	M → Peak Value
T → ON state	R → Repetitive	
F → Forward	S →Surge or non-repetitive	
R → Reverse		

VOLTAGE RATINGS

V_{DWM} : This specifies the peak off state working forward voltage of the device. This specifies the maximum forward off state voltage which the thyristor can withstand during its working.

V_{DRM} : This is the peak repetitive off state forward voltage that the thyristor can block repeatedly in the forward direction (transient).

V_{DSM} : This is the peak off state surge / non-repetitive forward voltage that will occur across the thyristor.

V_{RWM} : This the peak reverse working voltage that the thyristor can withstand in the reverse direction.

V_{RRM} : It is the peak repetitive reverse voltage. It is defined as the maximum permissible instantaneous value of repetitive applied reverse voltage that the thyristor can block in reverse direction.

V_{RSM} : Peak surge reverse voltage. This rating occurs for transient conditions for a specified time duration.

V_T : On state voltage drop and is dependent on junction temperature.

V_{TM} : Peak on state voltage. This is specified for a particular anode current and junction temperature.

$\frac{dv}{dt}$ rating: This is the maximum rate of rise of anode voltage that the SCR has to withstand and which will not trigger the device without gate signal (refer $\frac{dv}{dt}$ triggering).

CURRENT RATING

$I_{Taverage}$: This is the on state average current which is specified at a particular temperature.

I_{TRMS} : This is the on-state RMS current.

Latching current, I_L : After the SCR has switched on, there is a minimum current required to sustain conduction. This current is called the latching current. I_L associated with turn on and is usually greater than holding current

Holding current, I_H : After an SCR has been switched to the on state a certain minimum value of anode current is required to maintain the thyristor in this low impedance state. If the anode current is reduced below the critical holding current value, the thyristor cannot maintain the current through it and reverts to its off state usually I_m is associated with turn off the device.

$\frac{di}{dt}$ rating: This is a non repetitive rate of rise of on-state current. This maximum value of rate of rise of current is which the thyristor can withstand without destruction. When thyristor is switched on, conduction starts at a place near the gate. This small area of

conduction spreads rapidly and if rate of rise of anode current $\frac{di}{dt}$ is large compared to the spreading velocity of carriers, local hotspots will be formed near the gate due to high current density. This causes the junction temperature to rise above the safe limit and the SCR may be damaged permanently. The $\frac{di}{dt}$ rating is specified in $A/m\sec$.

GATE SPECIFICATIONS

I_{GT} : This is the required gate current to trigger the SCR. This is usually specified as a DC value.

V_{GT} : This is the specified value of gate voltage to turn on the SCR (dc value).

V_{GD} : This is the value of gate voltage, to switch from off state to on state. A value below this will keep the SCR in off state.

Q_{RR} : Amount of charge carriers which have to be recovered during the turn off process.

R_{thjc} : Thermal resistance between junction and outer case of the device.

GATE TRIGGERING METHODS

Types

The different methods of gate triggering are the following

- R-triggering.
- RC triggering.
- UJT triggering.

RESISTANCE TRIGGERING

A simple resistance triggering circuit is as shown. The resistor R_1 limits the current through the gate of the SCR. R_2 is the variable resistance added to the circuit to achieve control over the triggering angle of SCR. Resistor 'R' is a stabilizing resistor. The diode D is required to ensure that no negative voltage reaches the gate of the SCR.

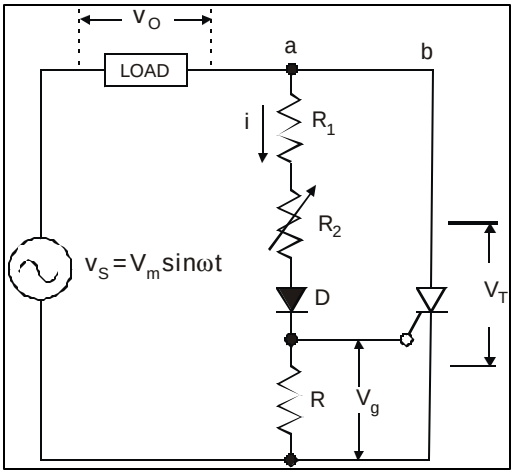


Fig.: Resistance firing circuit

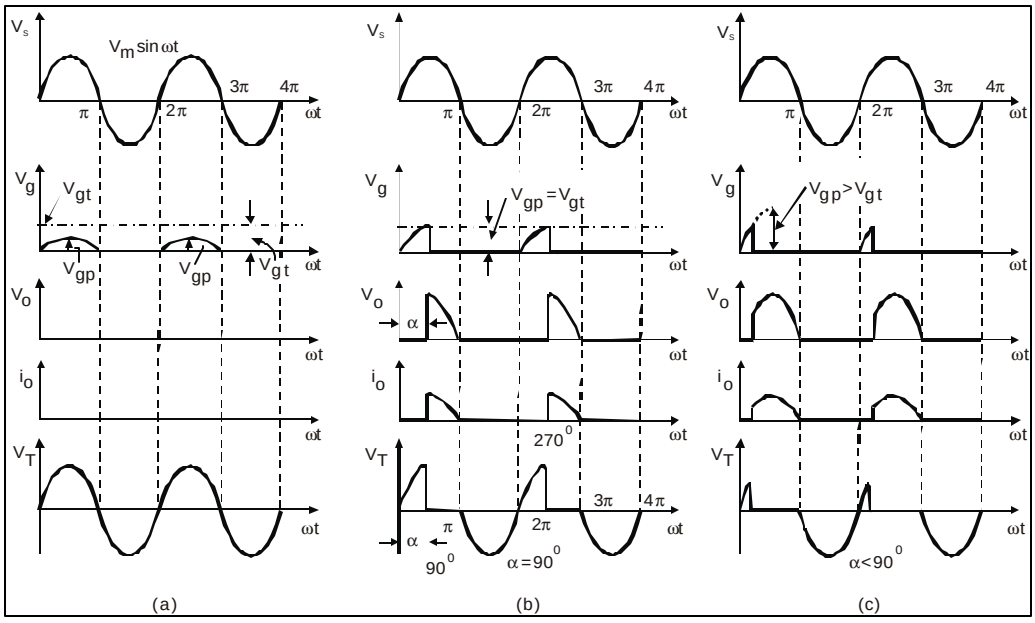


Fig.: Resistance firing of an SCR in half wave circuit with dc load

(a) No triggering of SCR (b) a **= 90^0 (c)** a **< 90^0**

Design

With $R_2 = 0$, we need to ensure that $\frac{V_m}{R_1} < I_{gm}$, where I_{gm} is the maximum or peak gate current of the SCR. Therefore $R_1 \geq \frac{V_m}{I_{gm}}$.

Also with $R_2 = 0$, we need to ensure that the voltage drop across resistor 'R' does not exceed V_{gm}, the maximum gate voltage

$$V_{gm} \geq \frac{V_m R}{R_1 + R}$$

$$\therefore \quad V_{gm} R_1 + V_{gm} R \geq V_m R$$

$$\therefore \quad V_{gm} R_1 \geq R\left(V_m - V_{gm}\right)$$

$$R \leq \frac{V_{gm} R_1}{V_m - V_{gm}}$$

OPERATION

Case 1: $V_{gp} < V_{gt}$

V_{gp}, the peak gate voltage is less then V_{gt} since R_2 is very large. Therefore, current 'I' flowing through the gate is very small. SCR will not turn on and therefore the load voltage is zero and v_{scr} is equal to V_s. This is because we are using only a resistive network. Therefore, output will be in phase with input.

Case 2: $V_{gp} = V_{gt}$, $R_2 \rightarrow$ optimum value.

When R_2 is set to an optimum value such that $V_{gp} = V_{gt}$, we see that the SCR is triggered at 90^0 (since V_{gp} reaches its peak at 90^0 only). The waveforms shows that the load voltage is zero till 90^0 and the voltage across the SCR is the same as input voltage till it is triggered at 90^0.

Case 3: $V_{gp} > V_{gt}$, $R_2 \rightarrow$ small value.

The triggering value V_{gt} is reached much earlier than 90^0. Hence the SCR turns on earlier than V_S reaches its peak value. The waveforms as shown with respect to $V_s = V_m \sin wt$.

At $\quad wt = a, V_S = V_{gt}, V_m = V_{gp} \left(\text{Q } V_{gt} = V_{gp} \sin a\right)$

Therefore $\quad a = \sin^{-1}\left(\frac{V_{gt}}{V_{gp}}\right)$

But $\quad V_{gp} = \frac{V_m R}{R_1 + R_2 + R}$

Therefore $\alpha = \sin^{-1}\left[\frac{V_{gt}\,(R_1 + R_2 + R)}{V_m R}\right]$

Since V_{gt}, R_1, R are constants α a R_2

RESISTANCE CAPACITANCE TRIGGERING

RC HALF WAVE

Capacitor 'C' in the circuit is connected to shift the phase of the gate voltage. D_1 is used to prevent negative voltage from reaching the gate cathode of SCR.

In the negative half cycle, the capacitor charges to the peak negative voltage of the supply $(-V_m)$ through the diode D_2. The capacitor maintains this voltage across it, till the supply voltage crosses zero. As the supply becomes positive, the capacitor charges through resistor 'R' from initial voltage of $-V_m$, to a positive value.

When the capacitor voltage is equal to the gate trigger voltage of the SCR, the SCR is fired and the capacitor voltage is clamped to a small positive value.

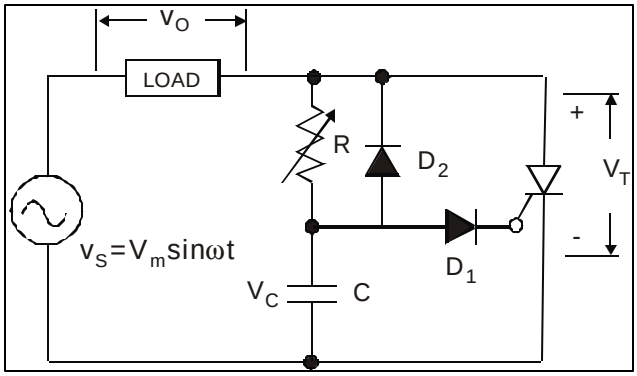


Fig.: RC half-wave trigger circuit

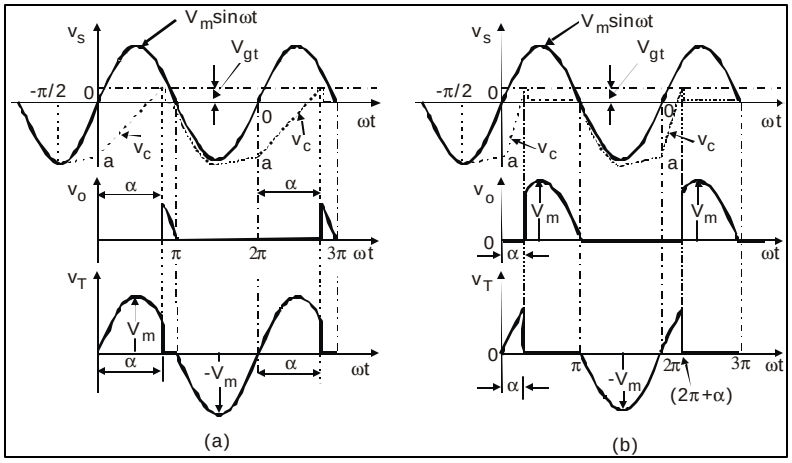


Fig.: Waveforms for RC half-wave trigger circuit

(a) High value of R **(b) Low value of R**

Case 1: R → Large.

When the resistor 'R' is large, the time taken for the capacitance to charge from $-V_m$ to V_{gt} is large, resulting in larger firing angle and lower load voltage.

Case 2: R → Small

When 'R' is set to a smaller value, the capacitor charges at a faster rate towards V_{gt} resulting in early triggering of SCR and hence V_L is more. When the SCR triggers, the voltage drop across it falls to 1 – 1.5V. This in turn lowers, the voltage across R & C. Low voltage across the SCR during conduction period keeps the capacitor discharge during the positive half cycle.

DESIGN EQUATION

From the circuit $V_C = V_{gt} + V_{d1}$. Considering the source voltage and the gate circuit, we can write $v_s = I_{gt} R + V_C$. SCR fires when $v_s \geq I_{gt} R + V_C$ that is $v_S \geq I_g R + V_{gt} + V_{d1}$. Therefore $R \leq \frac{v_s - V_{gt} - V_{d1}}{I_{gt}}$. The RC time constant for zero output voltage that is maximum firing angle for power frequencies is empirically gives as $RC \geq 1.3\left(\frac{T}{2}\right)$.

RC FULL WAVE

A simple circuit giving full wave output is shown in figure below. In this circuit the initial voltage from which the capacitor 'C' charges is essentially zero. The capacitor 'C' is reset to this voltage by the clamping action of the thyristor gate. For this reason the charging time constant RC must be chosen longer than for half wave RC circuit in order to delay the triggering. The RC value is empirically chosen as $RC \geq \frac{50T}{2}$. Also $R \leq \frac{v_s - V_{gt}}{I_{gt}}$.

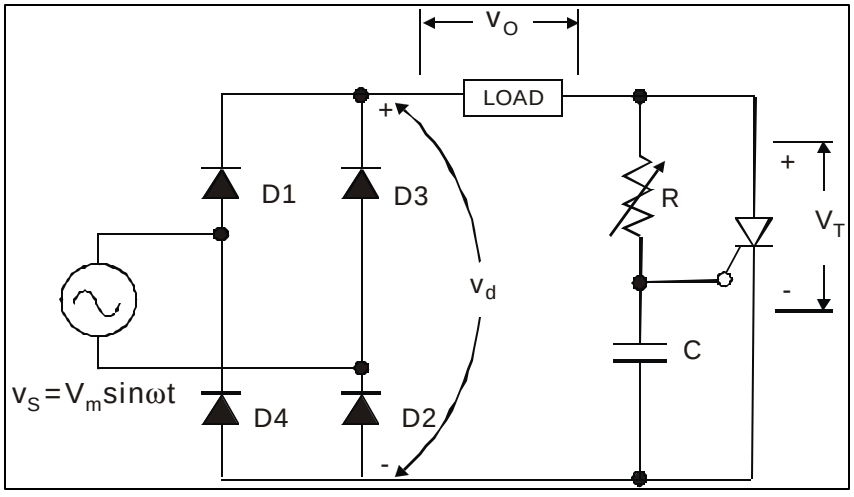


Fig: RC full-wave trigger circuit

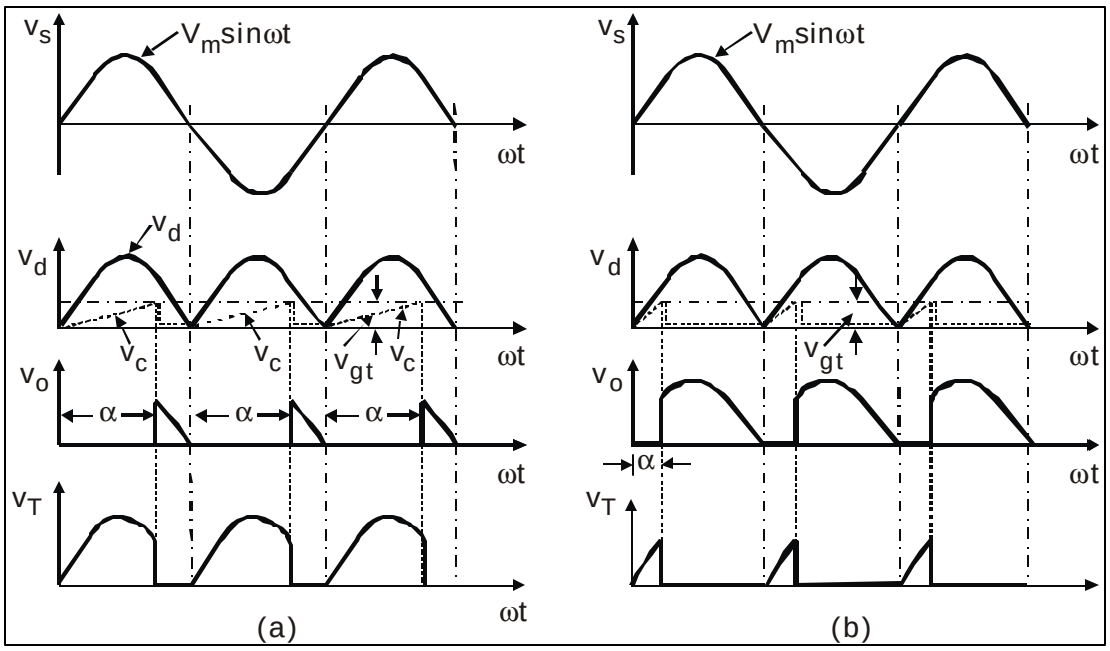


Fig: Wave-forms for RC full-wave trigger circuit

(a) High value of R **(b) Low value of R**

PROBLEM

1. Design a suitable RC triggering circuit for a thyristorised network operation on a 220V, 50Hz supply. The specifications of SCR are $V_{gt\min} = 5V$, $I_{gt\max} = 30mA$.

$$R = \frac{v_s - V_{gt} - V_D}{I_g} = 7143.3\Omega$$

Therefore $RC \geq 0.013$

$R \leq 7.143k\Omega$

$C \geq 1.8199mF$

UNI-JUNCTION TRANSISTOR (UJT)

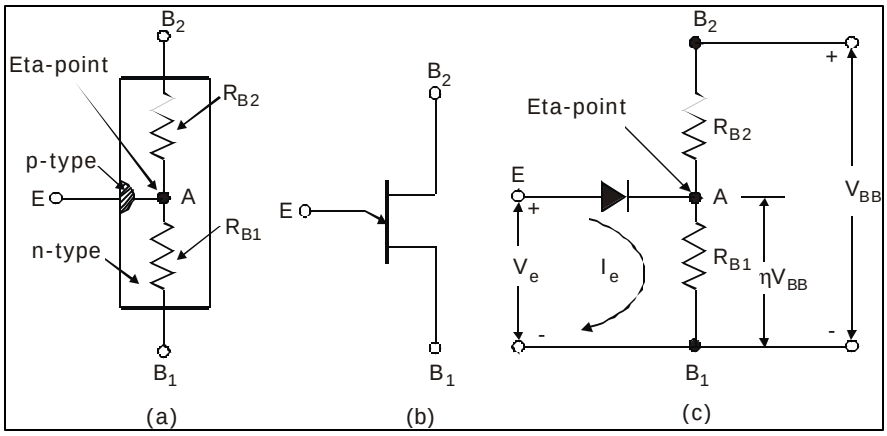


Fig.: (a) Basic structure of UJT (b) Symbolic representation

(c) Equivalent circuit

UJT is an n-type silicon bar in which p-type emitter is embedded. It has three terminals base1, base2 and emitter 'E'. Between B_1 and B_2 UJT behaves like ordinary resistor and the internal resistances are given as R_{B1} and R_{B2} with emitter open $R_{BB} = R_{B1} + R_{B2}$. Usually the p-region is heavily doped and n-region is lightly doped. The equivalent circuit of UJT is as shown. When V_{BB} is applied across B_1 and B_2, we find that potential at A is

$$V_{AB1} = \frac{V_{BB} R_{B1}}{R_{B1} + R_{B2}} = hV_{BB} \left[h = \frac{R_{B1}}{R_{B1} + R_{B2}} \right]$$

h is intrinsic stand off ratio of UJT and ranges between 0.51 and 0.82. Resistor R_{B2} is between 5 to 10KΩ.

OPERATION

When voltage V_{BB} is applied between emitter 'E' with base 1 B_1 as reference and the emitter voltage V_E is less than $(V_D + hV_{BE})$ the UJT does not conduct. $(V_D + hV_{BB})$ is designated as V_P which is the value of voltage required to turn on the UJT. Once V_E is equal to $V_P \equiv hV_{BE} + V_D$, then UJT is forward biased and it conducts.

The peak point is the point at which peak current I_P flows and the peak voltage V_P is across the UJT. After peak point the current increases but voltage across device drops, this is due to the fact that emitter starts to inject holes into the lower doped n-region. Since p-region is heavily doped compared to n-region. Also holes have a longer life time, therefore number of carriers in the base region increases rapidly. Thus potential at 'A' falls but current I_E increases rapidly. R_{B1} acts as a decreasing resistance.

The negative resistance region of UJT is between peak point and valley point. After valley point, the device acts as a normal diode since the base region is saturated and R_{B1} does not decrease again.

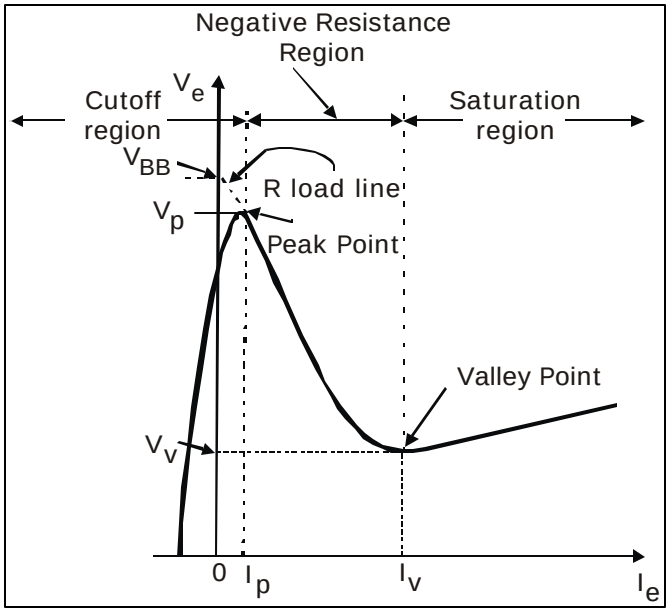


Fig.: V-I Characteristics of UJT

UJT RELAXATION OSCILLATOR

UJT is highly efficient switch. The switching times is in the range of nanoseconds. Since UJT exhibits negative resistance characteristics it can be used as relaxation oscillator. The circuit diagram is as shown with R_1 and R_2 being small compared to R_{B1} and R_{B2} of UJT.

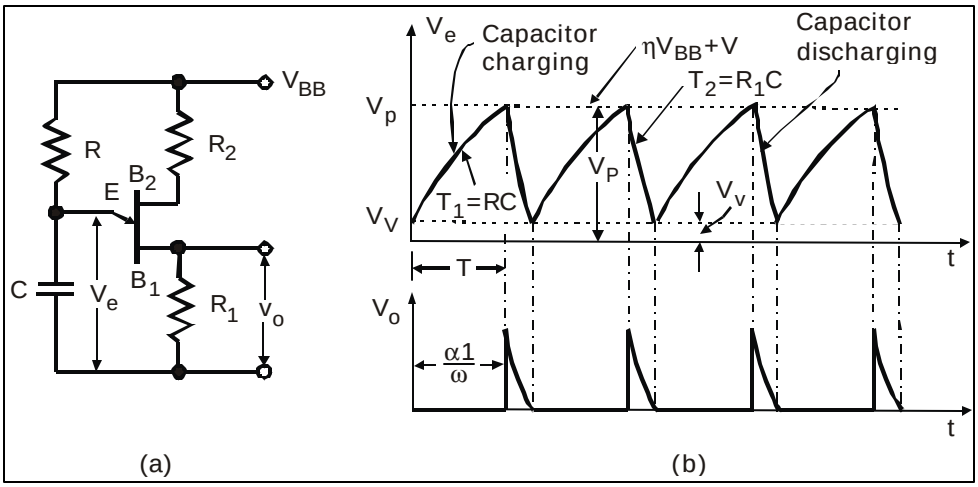


Fig.: UJT oscillator (a) Connection diagram and (b) Voltage waveforms

OPERATION

When V_{BB} is applied, capacitor 'C' begins to charge through resistor 'R' exponentially towards V_{BB}. During this charging emitter circuit of UJT is an open circuit. The rate of charging is $t_1 = RC$. When this capacitor voltage which is nothing but emitter voltage V_E reaches the peak point $V_P = hV_{BB} + V_D$, the emitter base junction is forward biased and UJT turns on. Capacitor 'C' rapidly discharges through load resistance R_1 with time constant $t_2 = R_1C\ (t_2 = t_1)$. When emitter voltage decreases to valley point V_v, UJT turns off. Once again the capacitor will charge towards V_{BB} and the cycle continues. The rate of charging of the capacitor will be determined by the resistor R in the circuit. If R is small the capacitor charges faster towards V_{BB} and thus reaches V_P faster and the SCR is triggered at a smaller firing angle. If R is large the capacitor takes a longer time to charge towards V_P the firing angle is delayed. The waveform for both cases is as shown below.

EXPRESSION FOR PERIOD OF OSCILLATION 'T'

The period of oscillation of the UJT can be derived based on the voltage across the capacitor. Here we assume that the period of charging of the capacitor is lot larger than than the discharging time.

Using initial and final value theorem for voltage across a capacitor, we get

$$V_C = V_{final} + \left(V_{initial} - V_{final}\right) e^{-t/RC}$$

$$t = T, V_C = V_P, V_{initial} = V_V, V_{final} = V_{BB}$$

Therefore $$V_P = V_{BB} + \left(V_V - V_{BB}\right) e^{-T/RC}$$

$$\Rightarrow \qquad T = RC \log_e \left(\frac{V_{BB} - V_V}{V_{BB} - V_P}\right)$$

If

$$V_V < V_{BB},$$

$$T = RC \ln \left(\frac{V_{BB}}{V_{BB} - V_P}\right)$$

$$= RC \ln \left[\frac{1}{1 - \frac{V_P}{V_{BB}}}\right]$$

But $$V_P = hV_{BB} + V_D$$

If $V_D = V_{BB}$ $V_P = hV_{BB}$

Therefore $T = RC \ln\left[\frac{1}{1-h}\right]$

DESIGN OF UJT OSCILLATOR

Resistor 'R' is limited to a value between 3 kilo ohms and 3 mega ohms. The upper limit on 'R' is set by the requirement that the load line formed by 'R' and V_{BB} intersects the device characteristics to the right of the peak point but to the left of valley point. If the load line fails to pass to the right of the peak point the UJT will not turn on, this condition will be satisfied if $V_{BB} - I_P R > V_P$, therefore $R < \frac{V_{BB} - V_P}{I_P}$.

At the valley point $I_E = I_V$ and $V_E = V_V$, so the condition for the lower limit on 'R' to ensure turn-off is $V_{BB} - I_V R < V_V$, therefore $R > \frac{V_{BB} - V_V}{I_V}$.

The recommended range of supply voltage is from 10 to 35V. the width of the triggering pulse $t_g = R_{B1}C$.

In general R_{B1} is limited to a value of 100 ohm and R_{B2} has a value of 100 ohm or greater and can be approximately determined as $R_{B2} = \frac{10^4}{hV_{BB}}$.

PROBLEM

1. A UJT is used to trigger the thyristor whose minimum gate triggering voltage is 6.2V, The UJT ratings are: $h = 0.66$, $I_p = 0.5mA$, $I_v = 3mA$, $R_{B1} + R_{B2} = 5k\Omega$, leakage current = 3.2mA, $V_p = 14v$ and $V_v = 1V$. Oscillator frequency is 2kHz and capacitor C = 0.04μF. Design the complete circuit.

Solution

$$T = R_C C \ln\left[\frac{1}{1-h}\right]$$

Here,

$T = \frac{1}{f} = \frac{1}{2\times10^3}$, since $f = 2kHz$ and putting other values,

$$\frac{1}{2\times10^3} = R_C \times 0.04\times10^{-6} \ln\left(\frac{1}{1-0.66}\right) = 11.6k\Omega$$

The peak voltage is given as, $V_p = hV_{BB} + V_D$

Let $V_D = 0.8$, then putting other values,

$$14 = 0.66V_{BB} + 0.8$$

$$V_{BB} = 20V$$

The value of R_2 is given by

$$R_2 = \frac{0.7\left(R_{B2} + R_{B1}\right)}{hV_{BB}}$$

$$R_2 = \frac{0.7\left(5\times10^3\right)}{0.66\times20}$$

$$\therefore R_2 = 265\Omega$$

Value of R_1 can be calculated by the equation

$$V_{BB} = I_{leakage}\left(R_1 + R_2 + R_{B1} + R_{B2}\right)$$

$$20 = 3.2\times10^{-3}\left(R_1 + 265 + 5000\right)$$

$$R_1 = 985\Omega$$

The value of $R_{c(\max)}$ is given by equation

$$R_{c(\max)} = \frac{V_{BB} - V_p}{I_p}$$

$$R_{c(\max)} = \frac{20 - 14}{0.5\times10^{-3}}$$

$$R_{c(\max)} = 12k\Omega$$

Similarly the value of $R_{c(\min)}$ is given by equation

$$R_{c(\min)} = \frac{V_{BB} - V_v}{I_v}$$

$$R_{c(\min)} = \frac{20 - 1}{3\times10^{-3}}$$

$$R_{c(\min)} = 6.33k\Omega$$

2. Design the UJT triggering circuit for SCR. Given $-V_{BB} = 20V$, $h = 0.6$, $I_p = 10mA$, $V_v = 2V$, $I_v = 10mA$. The frequency of oscillation is 100Hz. The triggering pulse width should be $50ms$.

Solution

The frequency f = 100Hz, Therefore $T = \frac{1}{f} = \frac{1}{100}$

From equation $T = R_c C \ln\left(\frac{1}{1-h}\right)$

Putting values in above equation,

$$\frac{1}{100} = R_c C \ln\left(\frac{1}{1-0.6}\right)$$

$$\therefore R_c C = 0.0109135$$

Let us select $C = 1mF$. Then R_c will be,

$$R_{c(\min)} = \frac{0.0109135}{1\times10^{-6}}$$

$$R_{c(\min)} = 10.91k\Omega .$$

The peak voltage is given as,

$$V_p = hV_{BB} + V_D$$

Let $V_D = 0.8$ and putting other values,

$$V_p = 0.6\times20 + 0.8 = 12.8V$$

The minimum value of R_c can be calculated from

$$R_{c(\min)} = \frac{V_{BB} - V_v}{I_v}$$

$$R_{c(\min)} = \frac{20-2}{10\times10^{-3}} = 1.8k\Omega$$

Value of R_2 can be calculated from

$$R_2 = \frac{10^4}{hV_{BB}}$$

$$R_2 = \frac{10^4}{0.6\times20} = 833.33\Omega$$

Here the pulse width is give, that is 50μs.

Hence, value of R_1 will be,

$$t_2 = R_1 C$$

The width $t_2 = 50m$ sec and $C = 1mF$, hence above equation becomes,

$$50\times10^{-6} = R_1\times1\times10^{-6}$$

$$\therefore R_1 = 50\Omega$$

Thus we obtained the values of components in UJT triggering circuit as,

$R_1 = 50\Omega$, $R_2 = 833.33\Omega$, $R_c = 10.91k\Omega$, $C = 1mF$.

SYNCHRONIZED UJT OSCILLATOR

A synchronized UJT triggering circuit is as shown in figure below. The diodes rectify the input ac to dc, resistor R_d lowers V_{dc} to a suitable value for the zener diode and UJT. The zener diode 'Z' functions to clip the rectified voltage to a standard level V_Z which remains constant except near $V_{dc} = 0$. This voltage V_Z is applied to the charging RC circuit. The capacitor 'C' charges at a rate determined by the RC time constant. When the capacitor reaches the peak point V_P the UJT starts conducting and capacitor discharges through the primary of the pulse transformer. As the current through the primary is in the from of a pulse the secondary windings have pulse voltages at the output. The pulses at the two secondaries feed SCRs in phase. As the zener voltage V_Z goes to zero at the end of each half cycle the synchronization of the trigger circuit with the supply voltage across the SCRs is archived, small variations in supply voltage and frequency are not going to effect the circuit operation. In case the resistor 'R' is reduced so that the capacitor voltage reaches UJT threshold voltage twice in each half cycle there will be two pulses in each half cycle with one pulse becoming redundant.

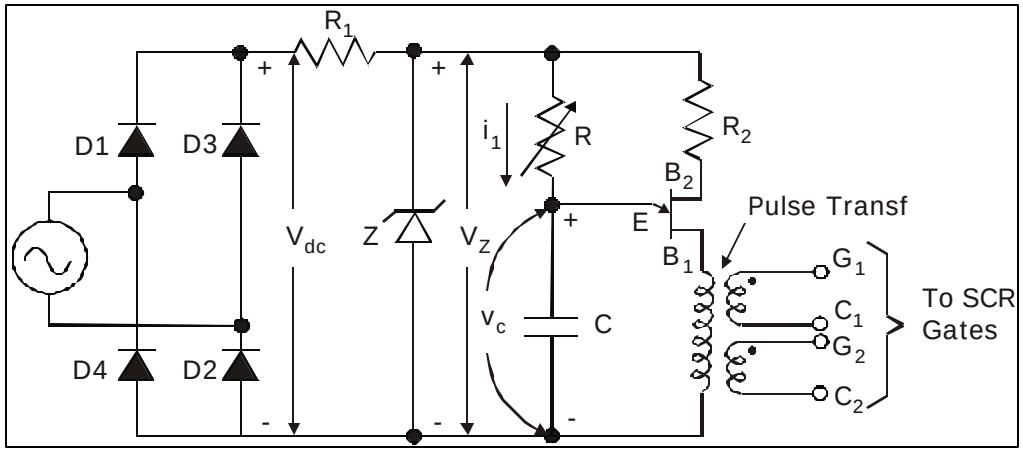


Fig.: Synchronized UJT trigger circuit

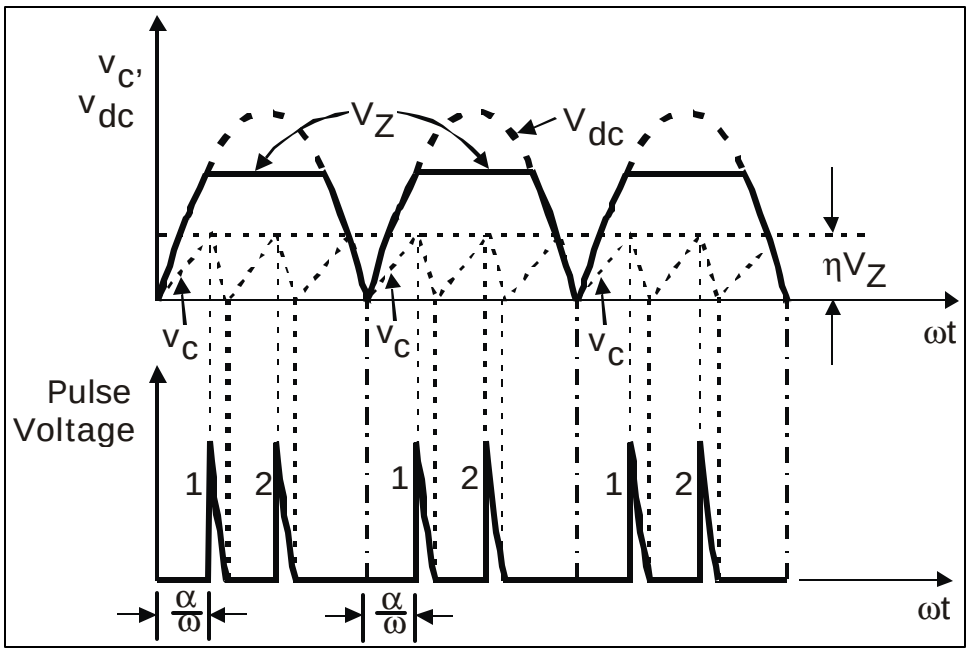


Fig.: Generation of output pulses for the synchronized UJT trigger circuit

DIGITAL FIRING CIRCUIT

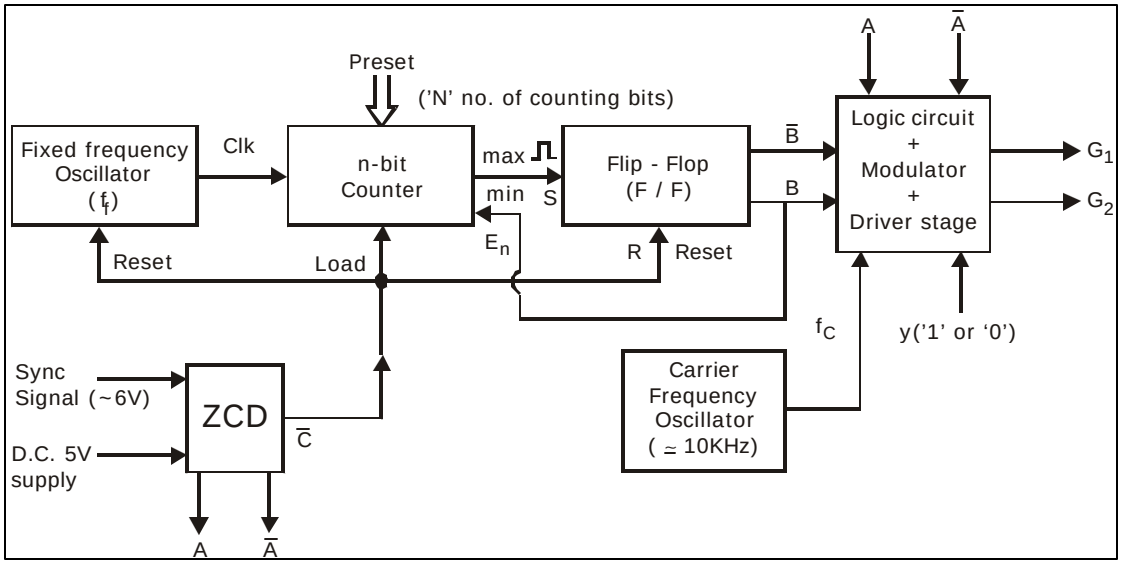


Fig.: Block diagram of digital firing circuit

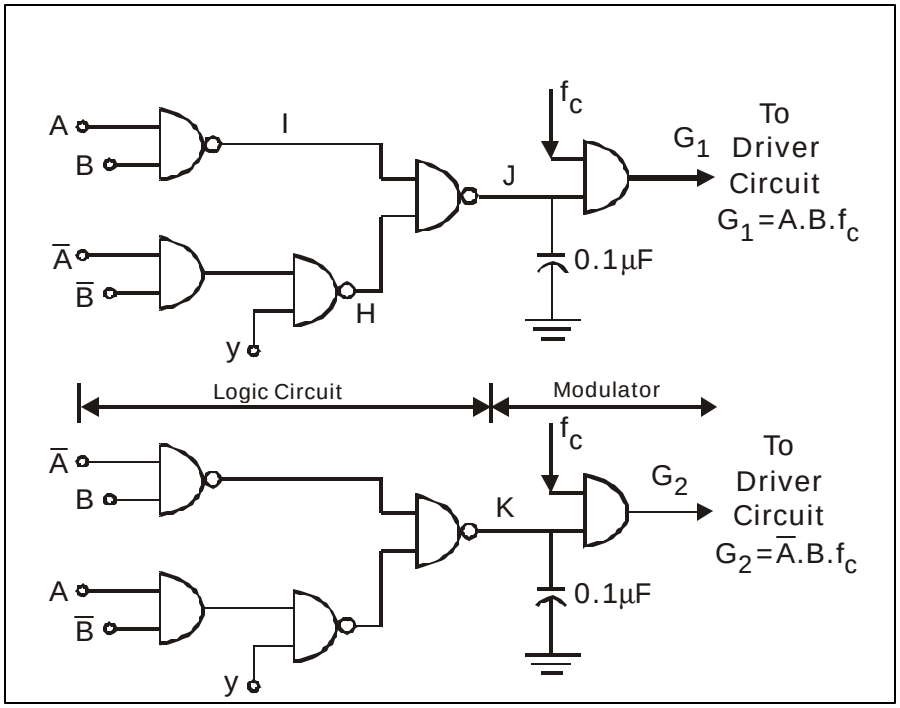


Fig.: Logic circuit, Carrier Modulator

The digital firing scheme is as shown in the above figure. It constitutes a pre-settable counter, oscillator, zero crossing detection, flip-flop and a logic control unit with NAND and AND function.

Oscillator: The oscillator generates the clock required for the counter. The frequency of the clock is say f_C. In order to cover the entire range of firing angle that is from 0^0 to 180^0, a n-bit counter is required for obtaining 2^n rectangular pulses in a half cycle of ac source. Therefore 4-bit counter is used, we obtain sixteen pulses in a half cycle of ac source.

Zero Crossing Detector: The zero crossing detector gives a short pulse whenever the input ac signal goes through zeroes. The ZCD output is used to reset the counter, oscillator and flip-flops for getting correct pulses at zero crossing point in each half cycle, a low voltage synchronized signal is used.

Counter: The counter is a pre-settable n-bit counter. It counts at the rate of f_C pulses/second. In order to cover the entire range of firing angle from 0 to 180^0 , the n-bit counter is required for obtaining 2^n rectangular pulses in a half cycle.

Example: If 4-bit counter is used there will be sixteen pulses / half cycle duration. The counter is used in the down counting mode. As soon as the synchronized signal crosses zero, the load and enable become high and low respectively and the counter starts counting the clock pulses in the down mode from the maximum value to the pre-set value 'N'. 'N' is the binary equivalent of the control signal. once the counter reaches the preset value 'N' counter overflow signal goes high. The counter overflow signal is processed to trigger the Thyristors. Thus by varying the preset input one can control the firing angle of Thyristors. The value of firing angle (a) can be calculated from the following equation

$$a = \left(\frac{2^n - N}{2^n}\right)180^0 = \left(1 - \frac{N}{16}\right)180^0 \left(\text{for } n = 4\right)$$

Modified R-S Flip-Flop: The reset input terminal of flip-flop is connected to the output of ZCD and set is connected to output of counter. The pulse goes low at each zero crossing of the ac signal. A low value of ZCD output resets the B-bar to 1 and B to 0.

A high output of the counter sets B-bar to 0 and B to 1. This state of the flip-flop is latched till the next zero crossing of the synchronized signal. The output terminal B of flip-flop is connected with enable pin of counter. A high at enable 'EN' of counter stops counting till the next zero crossing.

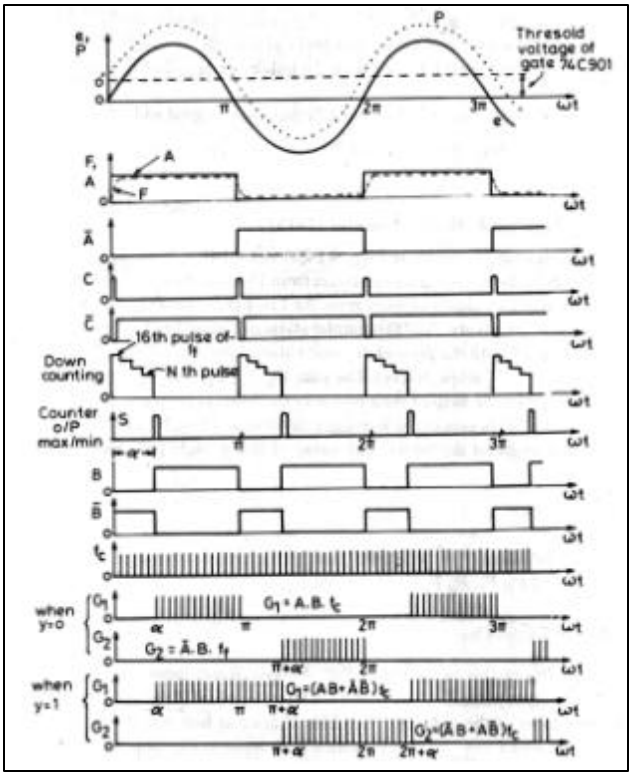
Input		***Output***		***Remarks***
R	***S***	***B***	***B-bar***	
1	***1***	***1***	***0***	
0	***1***	***1***	***0***	***Set***
0	***0***	***0***	***1***	***Reset***
1	***0***	***0***	***1***	***Last Stage***
1	***1***	***1***	***0***	

Truth Table of Modified R-S Flip-Flop

Logic Circuit, Modulation and Driver Stage: The output of the flip-flop and pulses A and A-bar of ZCD are applied to the logic circuit. The logic variable Y equal to zero or one enables to select the firing pulse duration from a to p or a

Overall Operation

The input sinusoidal signal is used to derive signals A and A-bar with the help of ZCD. The zero crossing detector along with a low voltage sync signal is used to generate pulses at the instant the input goes through zeroes. The signal C and C-bar are as shown. The signal C-bar is used to reset the fixed frequency oscillator, the flip flop and the n-bit counter. The fixed frequency oscillator determines the rate at which the counter must count. The counter is preset to a value N which is the decimal equivalent of the trigger angle. The counter starts to down count as soon as the C-bar connected to load pin is zero. Once the down count N is over the counter gives a overflow signal which is processed to be given to the Thyristors. This overflow signal is given to the Set input S of the modified R-S flip flop. If S=1 B goes high as given by the truth table and B –bar has to go low. B has been connected to the Enable pin of counter. Once B goes low the counter stops counting till the next zero crossing. The carrier oscillator generates pulses with a frequency of 10kHz for generating trigger pulses for the Thyristors. Depending upon the values of A, A-bar, B, B-bar and Y the logic circuit will generate triggering pulses for gate1 or gate 2 for Thyristors 1 and 2 respectively.



$\frac{dv}{dt}$ PROTECTION

The $\frac{dv}{dt}$ across the thyristor is limited by using snubber circuit as shown in figure (a) below. If switch S_1 is closed at $t = 0$, the rate of rise of voltage across the thyristor is limited by the capacitor C_S. When thyristor T_1 is turned on, the discharge current of the capacitor is limited by the resistor R_S as shown in figure (b) below.

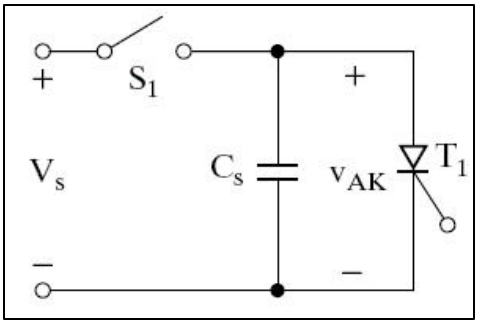


Fig. (a)

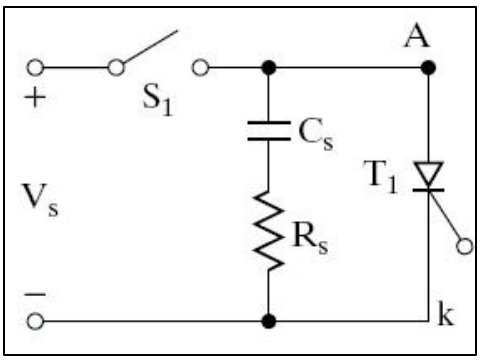


Fig. (b)

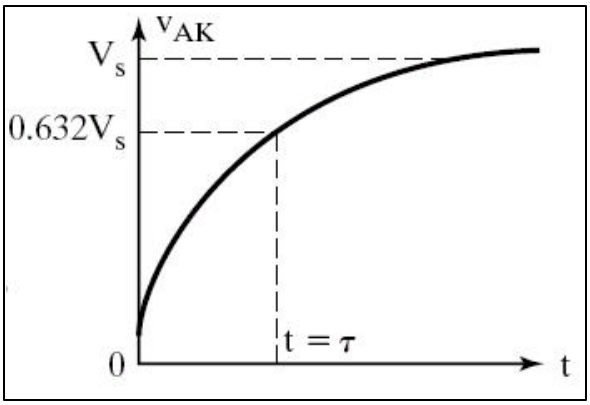


Fig. (c)

The voltage across the thyristor will rise exponentially as shown by fig (c) above. From fig. (b) above, circuit we have (for SCR off)

$$V_S = i(t)R_S + \frac{1}{C}\int i(t)\,dt + V_c(0)_{[for\ t=0]}.$$

Therefore $i(t) = \frac{V_S}{R_S}e^{-t/t_s}$, where $t_s = R_S C_S$

Also $V_T(t) = V_S - i(t)R_S$

$$V_T(t) = V_S - \frac{V_S}{R_S}e^{-t/t_s}R_S$$

Therefore $V_T(t) = V_S - V_S e^{-t/t_s} = V_S\left[1 - e^{-t/t_s}\right]$

At t = 0, $V_T(0) = 0$

At $t = t_s$, $V_T(t_s) = 0.632V_S$

Therefore $\frac{dv}{dt} = \frac{V_T(t_s) - V_T(0)}{t_s} = \frac{0.632V_S}{R_S C_S}$

And $R_S = \frac{V_S}{I_{TD}}$.

I_{TD} is the discharge current of the capacitor.

It is possible to use more than one resistor for $\frac{dv}{dt}$ and discharging as shown in the figure (d) below. The $\frac{dv}{dt}$ is limited by R_1 and C_S. $R_1 + R_2$ limits the discharging current such that $I_{TD} = \frac{V_S}{R_1 + R_2}$

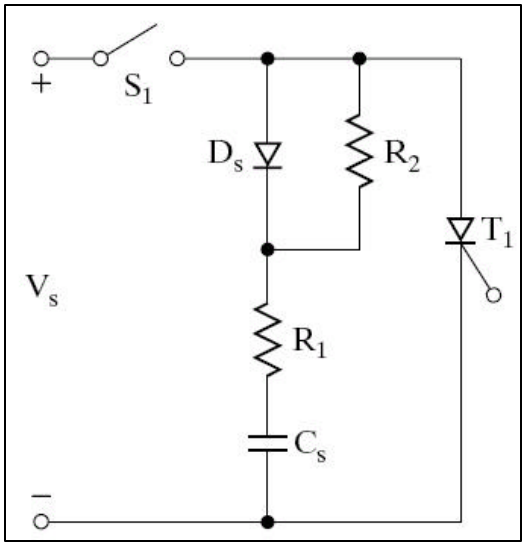


Fig. (d)

The load can form a series circuit with the snubber network as shown in figure (e) below. The damping ratio of this second order system consisting RLC network is given as,

$d = \frac{a}{w_0} = \frac{R_S + R}{2}\sqrt{\frac{C_S}{L_S + L}}$, where L_S is stray inductance and L, R is load inductance and resistance respectively.

To limit the peak overshoot applied across the thyristor, the damping ratio should be in the range of 0.5 to 1. If the load inductance is high, R_S can be high and C_S can be small to retain the desired value of damping ratio. A high value of R_S will reduce discharge current and a low value of C_S reduces snubber loss. The damping ratio is calculated for a particular circuit R_S and C_S can be found.

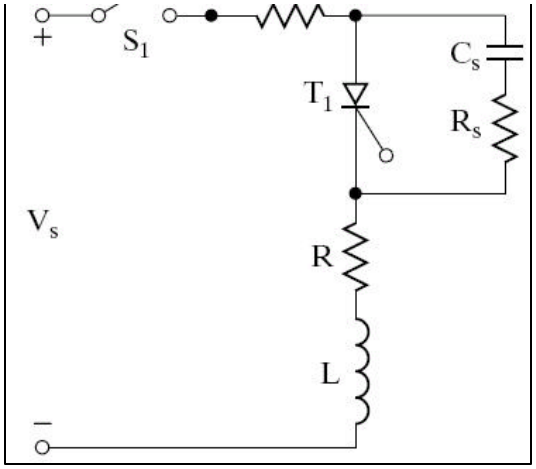
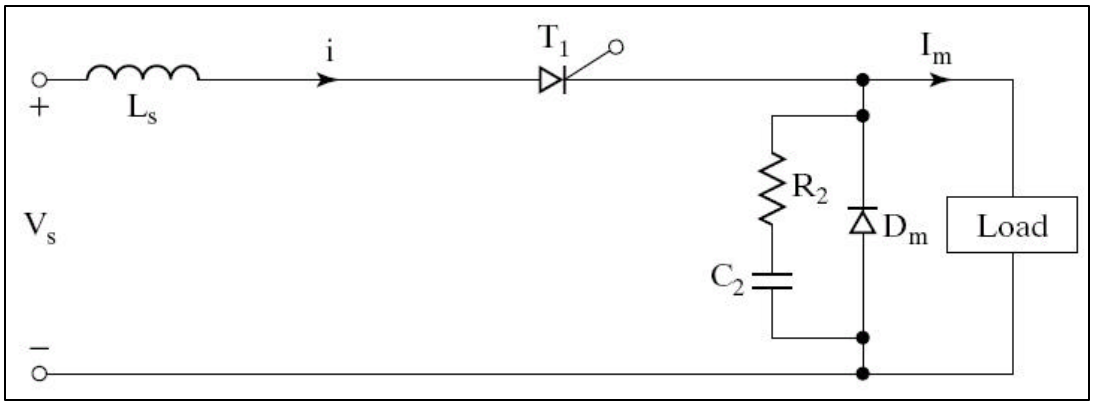


Fig. (e)

$\frac{di}{dt}$ PROTECTION



Practical devices must be protected against high $\frac{di}{dt}$. As an example let us consider the circuit shown above, under steady state operation D_m conducts when thyristor T_1 is off. If T_1 is fired when D_m is still conducting $\frac{di}{dt}$ can be very high and limited only by the stray inductance of the circuit. In practice the $\frac{di}{dt}$ is limited by adding a series inductor L_S as shown in the circuit above. Then the forward $\frac{di}{dt} = \frac{V_S}{L_S}$.

SERIES AND PARALLEL OPERATION

SCR ratings have improved considerably since its introduction in 1957. Presently, SCRs with voltage and current rating of 10kV and 3kA are available. However, for some industrial applications, the demand for voltage and current ratings is so high that a single SCR cannot fulfill such requirements. In such cases, SCRs are connected in series in order to meet the high voltage demand and in parallel for fulfilling high current demand.

The string efficiency that is a term used for measuring the degree of utilization of SCRs in a string.

$$\text{String efficiency} = \frac{\text{Actual voltage / current rating}}{(n_s, \text{ no. of SCRs}) \times \text{voltage / current rating of one SCR}}$$

Usually the above ratio is less than one. Since SCRs of same ratings and specifications do not have identical characteristics unequal voltage / current sharing is bound to occur for all SCRs in a string. Therefore the string efficiency can never be equal to one.

DERATING FACTOR (DRF)

The use of an extra unit will improve the reliability of a string. A measure of the reliability of the string is given by a factor called derating factor defined as

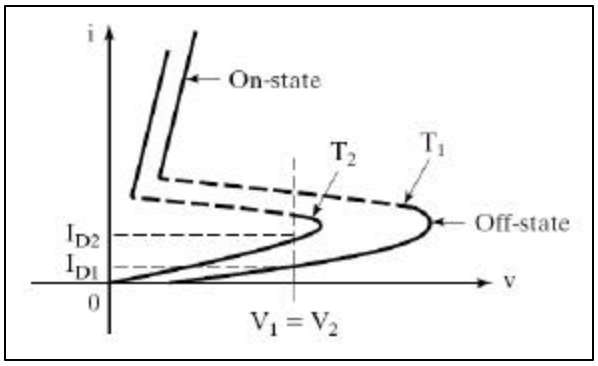
DRF = 1 - String efficiency

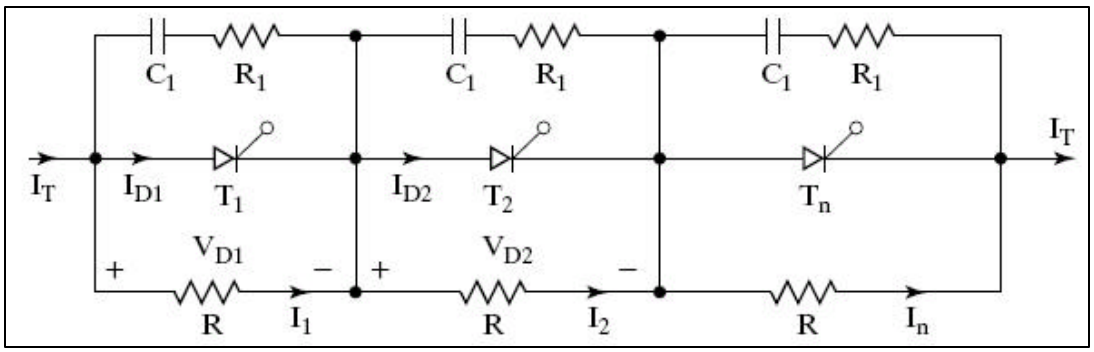
SERIES OPERATION OF SCRS

For high voltage applications two or more Thyristors can be connected in series to provide the required voltage rating. However due to production spread the characteristics of Thyristors of the same type are not identical.

STATIC EQUALIZATION

As seen from V-I characteristics, two identical Thyristors to be used in a string do not have the same off state current for same off-state voltages. If these SCRs are used in a string as such, unequal voltage distribution would occur. In order to overcome this, we could connect resistors across individual SCRs to meet the requirement of equal off state currents for the same off state voltage. But this is not practical therefore we use the same resistor 'R' across each SCR to get fairly uniform voltage distribution.





We see that, equal resistors 'R' are connected across individual SCR's which are connected in series. Let n_s be the number of SCRs connected. Let I_T be the total current that the string carries and individual SCRs have leakage currents $I_{D1}, I_{D2}.....,I_{Dn}$.

As seen from the V-I characteristics, even though the voltage across each SCR is the same, the leakage current in the off state differ. Let $I_{D1} < I_{D2}$. Since SCR1 has lower leakage current compared to other SCRs, it will block a higher voltage compared to other SCRs.

Let the leakage current of other SCRs, be such that $I_{D2} = I_{D3} = ..., I_{Dn}$. Therefore

$$I_{D1} = I_T - I_1 \qquad ....(1)$$

$$I_{D2} = I_T - I_2 \qquad ....(2)$$

If V_{D1} is the voltage across SCR1, then $V_{D1} = I_1 R$, and voltage across the rest of the SCRs is $(n_s - 1) I_2 R$.

Therefore total voltage across the string = $V_s = I_1 R + (n_s - 1) I_2 R$.

But from equation (2) $\qquad V_S = I_1 R + (n_s - 1)(I_T - I_{D2})$

But from equation (1) $\qquad I_T = I_{D1} + I_1$

Therefore $\qquad V_S = I_1 R + (n_s - 1)[I_{D1} + I_1 - I_{D2}] R$

$$V_S = V_{D1} + (n_s - 1) I_1 R + (n_s - 1)[I_{D1} - I_{D2}] R$$

But $\quad I_{D1} < I_{D2}, \ \therefore \quad V_S = V_{D1} + (n_s - 1) I_1 R - (n_s - 1)(I_{D2} - I_{D1}) R$

$I_{D2} - I_{D1} = \Delta I_D$ = difference between leakage currents of SCR1 and the rest of the SCRs.

Therefore $V_S = V_{D1} + (n_s - 1)V_{D1} - (n_S - 1)\Delta I_D R$

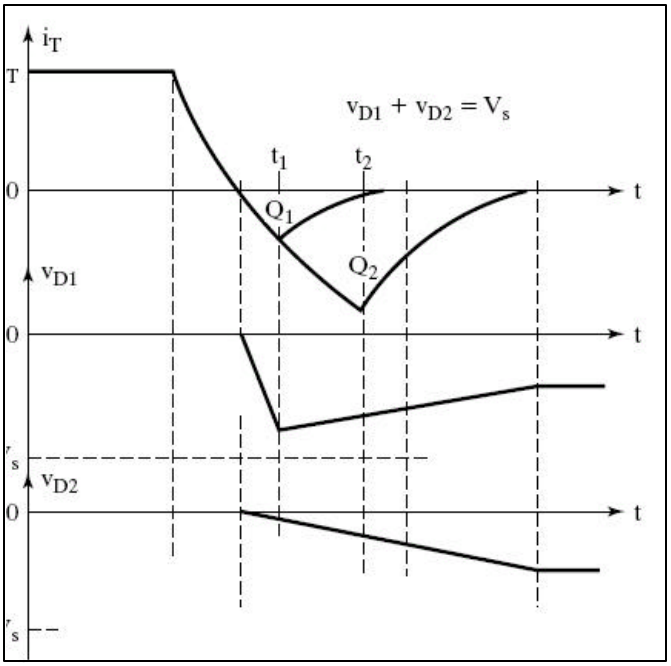
$$V_S = n_s V_{D1} - (n_s - 1)\Delta I_D R \qquad ...(3)$$

Also $$R = \frac{n_s V_{D1} - V_S}{(n_s - 1)\Delta I_D}$$

From equation (3), considering the worst case condition of $I_{D1} = 0$, $V_{D1(\max)} = \dfrac{V_S + (n_s - 1)\, R I_{D2}}{n_s}$

DYNAMIC EQUALIZATION

Under transient conditions, the voltage across individual SCRs in a string may not be distributed equally. The cause for this is the unequal junction capacitances of individual SCRs. During turn off the differences in stored charges causes differences in the reverse voltage sharing. The thyristor with the least recovered charge will face the highest transient voltage normally it is necessary to connect a capacitor C_1 across each thyristor as shown in the figure of series connected Thyristors.



DESIGN OF C

It is found that in series connected SCRs, voltage unbalance during turn off is more predominant than the turn on time. Therefore the design of 'C' is based on turn off characteristics.

Since SCR1 has recovered early, the voltage across capacitor 'C' is the difference between charge storage of SCR1 and SCR2 so the transient voltage across SCR1 is,

$\Delta V = \Delta I_D R = \frac{\Delta Q}{C}$, where Q_1 is the stored charge of T_1 and Q_2 is the stored charge of T_2 with $\Delta Q = Q_2 - Q_1$.

Assuming there are 'n_s' SCRs in the string, then $Q_2 = Q_3 .....Q_n$ and $Q_1 < Q_2$.

Voltage across SCR1 = $V_{D1} = \frac{V_S + (n_s - 1)\Delta I_D R}{n_s}$.

Substituting for $\Delta I_D R$, we have $V_{D1} = \frac{1}{n_s}\left[V_S + (n_s - 1)\frac{\Delta Q}{C_1}\right]$.

The worst case transient voltage sharing will occur when $Q_1 = 0$, and $\Delta Q = Q_2$ and $V_{DT(\max)}$ is given as

$$V_{D1(\max)} = \frac{1}{n_s}\left[V_S + (n_s - 1)\frac{Q_2}{C_1}\right]$$

Derating factor is given as $DRF = 1 - \frac{V_S}{n_s V_{D1(\max)}}$

PROBLEM

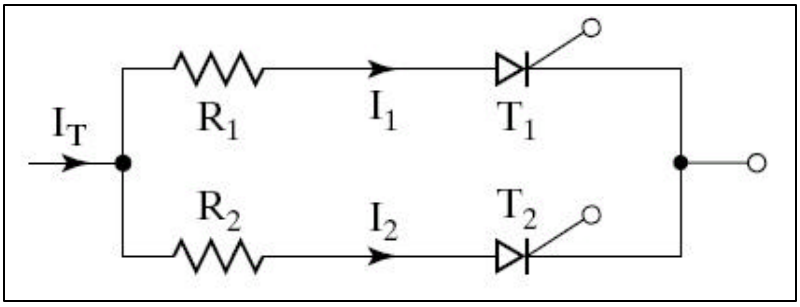
1. Ten thyrisors are used in a string to withstand a DC voltage of $V_S = 15kV$. The maximum leakage current and recovery charges of Thyristors are 10mA and 150μsec respectively. Each thyristor has a voltage sharing resistance of R=56kΩ and capacitance $C_1 = 0.5mF$. Determine
   a. Maximum steady state voltage sharing $V_{DS(\max)}$.
   b. Steady state voltage derating factor (DRF).
   c. Maximum transient voltage sharing.
   d. Transient voltage derating factor.

Solution

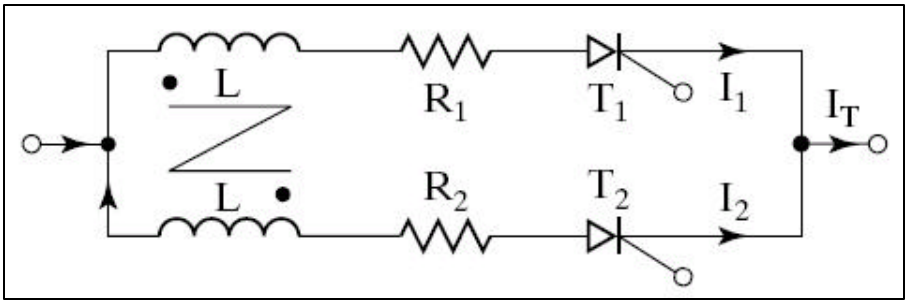
- $V_{DS(\max)} = \dfrac{V_S + (n_s - 1)\Delta I_D R}{n_s} = \left[\dfrac{V_S + (n_s - 1)}{n_s}.\dfrac{\Delta Q}{C}\right] = 2004V$
- $DRF = \dfrac{1 - V_S}{n_s V_{DT(\max)}} = 25.15\%$
- $DRF_{Transient} = 15.25\%$
- Transient voltage sharing = 1770V.

PARALLEL OPERATION OF SCRS.

Parallel operation is used whenever current required by the load is more than the capability of the single SCRs.



In parallel operation, if one SCR carriers more current than the other SCRs, it will result in a greater junction temperature which results in a decrease in the dynamic resistance which has a cumulative effect of increasing the current further. This may lead to the thermal runaway and finally damage the SCR. If one SCR is damaged, the load connected may also be damaged. When SCRs are operated in parallel, it should be ensured that they operated at the same temperature. This is done by mounting all the Thyristors on one common heat sink.



It is also important that for parallel connection, sharing of current is ensured. This could be done by connecting a small resistance in series. Unequal current distribution is overcome by magnetic coupling of parallel paths as shown. If current through T_1 increase, a voltage of opposite polarity will be induced in the windings of thyristor T_2 and impedance through paths of T_2 will be reduced, thereby increasing current flow through T_2.

THYRISTOR TYPES

Thyristors are manufactured almost exclusively by diffusion. The anode current requires a finite time to propagate to the whole area of the junction, from the point near the gate when the gate signal is initiated for turning on the thyristor. The manufacturers use various gate structures to control the di/dt, turn-on time, and turn-off time. Depending on the physical construction, and turn-on and turn-off behaviour, Thyristors can, broadly, be classified into nine categories.

- Phase-control Thyristors (SCR's).
- Fast-switching Thyristors (SCR's).
- Gate-turn-off Thyristors (GTOs).
- Bidirectional triode Thyristors (TRIACs).
- Reverse-conducting Thyristors (RCTs).
- Static induction Thyristors (SITHs).
- Light-activated silicon-controlled rectifiers (LASCRs).
- FET controlled Thyristors (FET-CTHs).
- MOS controlled Thyristors (MCTs).

PHASE-CONTROL THYRISTORS

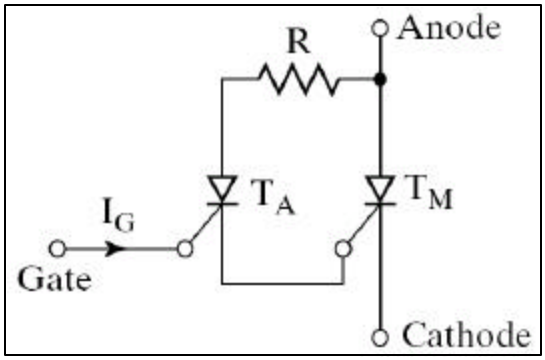


Fig.: Amplifying gate thyristor

This type of Thyristors generally operates at the line frequency and is turned off by natural commutation. The turn-off time t_q is of the order of 50 to 100μsec. This is most suited for low-speed switching applications and is also known as converter thyristor. Since a thyristor is basically silicon made controlled device, it is also known as silicon controlled rectifier (SCR).

The on-state voltage, V_T, varies typically from about 1.15V for 600V to 2.5V for 4000V devices; and for a 5000A 1200V thyristor it is typically 1.25V. The modern Thyristors use an amplifying gate, where an auxiliary thyristor T_A is gated on by a gate signal and then the amplified output of T_A is applied as a gate signal to the main thyristor T_M. This is shown in the figure below. The amplifying gate permits high dynamic characteristics

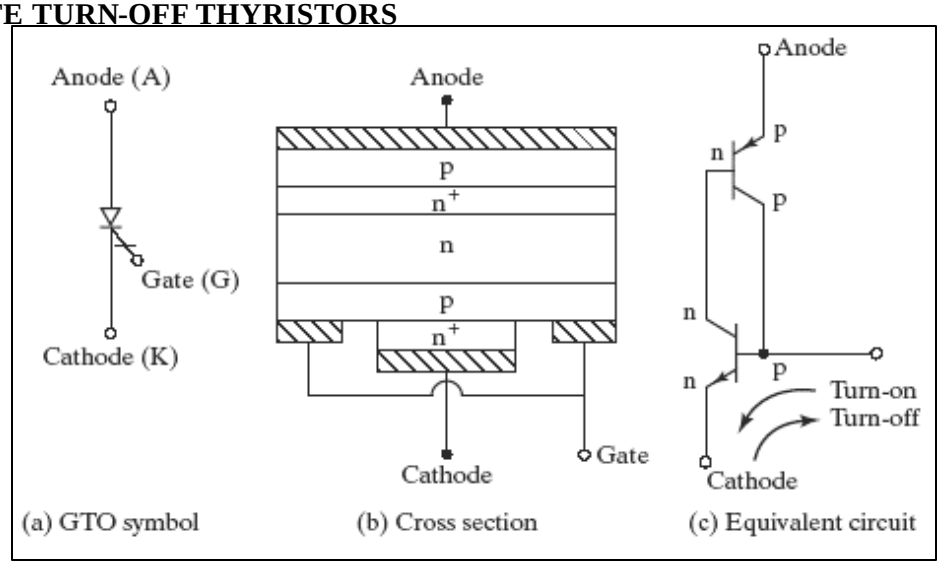
with typical dv/dt of 1000V/μsec and the di/dt of 500A/μsec and simplifies the circuit design by reducing or minimizing di/dt limiting inductor and dv/dt protection circuits.

FAST SWITCHING THYRISTORS

These are used in high-speed switching applications with forced commutation. They have fast turn-off time, generally in the rage 5 to 50μsec, depending on the voltage range. The on-state forward drop varies approximately as an inverse function of the turn-off time t_q. This type of thyristor is also known as inverter thyristor.

These Thyristors have high dv/dt of typically 1000 V/μsec & di/dt of 1000 A/μsec. The fast turn-off and high di/dt are very important to reduce the size and weight of commutating and or reactive circuit components. The on-state voltage of a 2200A, 1800V thyristor is typically 1.7V. Inverter Thyristors with a very limited reverse blocking capability, typically 10V and a very fast turn-off time between 3 and 5μsec are commonly known as asymmetrical Thyristors (ASCRs).

GATE TURN-OFF THYRISTORS



A gate-turn-off thyristor (GTO) like an SCR can be turned on by applying a positive gate signal. However, it can be turned off by a negative gate signal. A GTO is a latching device and can be built with current and voltage ratings similar to those of an SCR. A GTO is turned on by applying a short positive pulse and turned off by a short negative pulse to its gate. The GTOs have advantages over SCRs.

- Elimination of commutating components in forced commutation, resulting in reduction in cost, weight, and volume.
- Reduction in acoustic and electro-magnetic noise due to the elimination of commutation chokes.
- Faster turn-off permitting high switching frequencies and
- Improved efficiency of converters.

In low power applications GTOs have the following advantages over bipolar transistors.

- A higher blocking voltage capability.
- A high ratio of peak controllable current to average current.
- A high ratio of surge peak current to average current, typically 10:1.
- A high on-state gain (anode current/gate current), typically 600; and
- A pulsed gate signal of short duration.

Under surge conditions, a GTO goes into deeper saturation due to regenerative action. On the other hand, a bipolar transistor tends to come out of saturation.

A GTO has low gain during turn-off, typically 6, and requires a relatively high negative current pulse to turn off. It has higher on-state voltage than that of SCRs. The on-state voltage of typical 550A, 1200V GTO is typically 3.4V.

Controllable peak on-state current I_{TGQ} is the peak value of on-state current which can be turned off by gate control. The off state voltage is reapplied immediately after turn-off and the reapplied dv/dt is only limited by the snubber capacitance. Once a GTO is turned off, the load current I_L, which is diverted through and charges the snubber capacitor, determines the reapplied dv/dt.

$$\frac{dv}{dt} = \frac{I_L}{C_s}$$

Where C_s is the snubber capacitance

BIDIRECTIONAL TRIODE THYRISTORS

A TRIAC conducts in both directions unlike the SCR. Since it conducts in both directions, the terminals are named as MT1 and MT2 and the Gate. As seen from the diagram the gate 'G' is near terminal MT1. The cross hatched strip shows that 'G' is connected to n_3 as well as p_2. Similarly terminal MT1 is connected to p_2 as well as n_2 and terminal MT2 is connected to join p_1 and n_4.

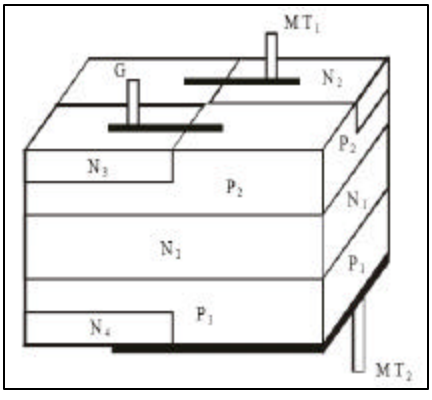


Fig.: Triac Structure

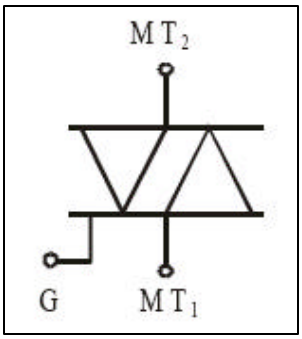


Fig.: Triac Symbol

With no signal to the gate the triac will block both half cycles of the applied AC voltage in case the peak value of this voltage is less than the breakover voltage in either direction. However the triac can be turned on by applying a positive voltage with respect to terminal MT1. For convenience sake MT1 is taken as the reference terminal. There are four modes of operation of the triac.

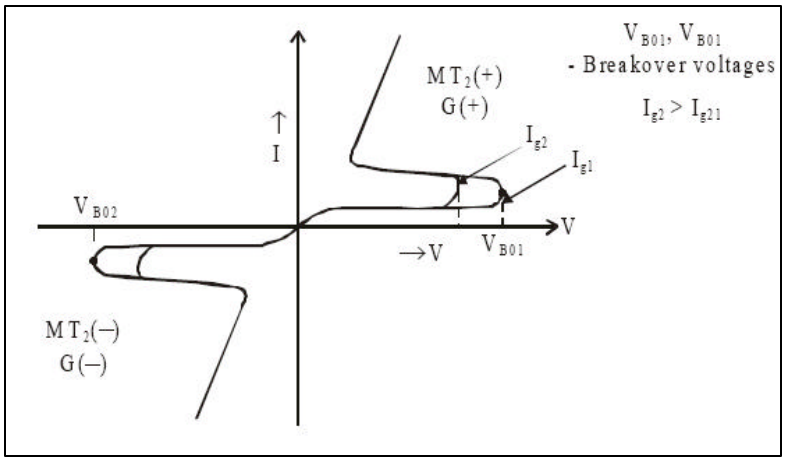
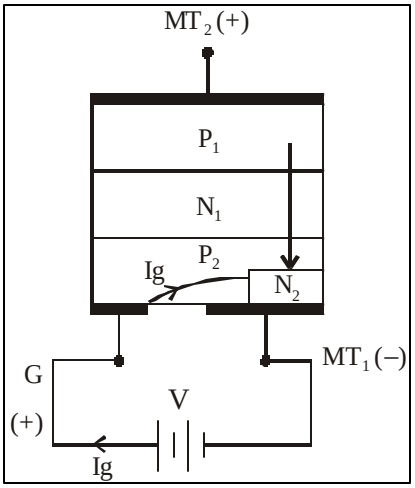


Fig.: V-I Characteristics of TRIAC

OPERATION

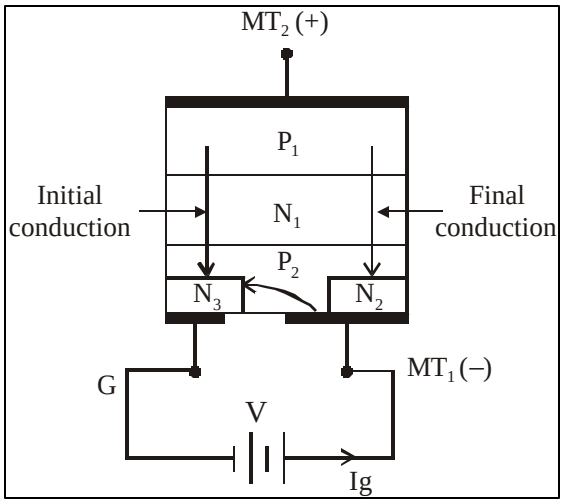
MODE (I): MT2 POSITIVE, GATE POSITIVE

When gate current is positive with respect to MT1, gate current mainly flows through p_2n_2 junction like in ordinary SCR. When the gate current has injected sufficient charge into the p_2 layer the traic starts conducting through $p_1n_1p_2n_2$ layers. This shows that when MT2 and gate are positive with respect to MT1 triac acts like a conventional thyristor. The quadrant of operation is the first quadrant.



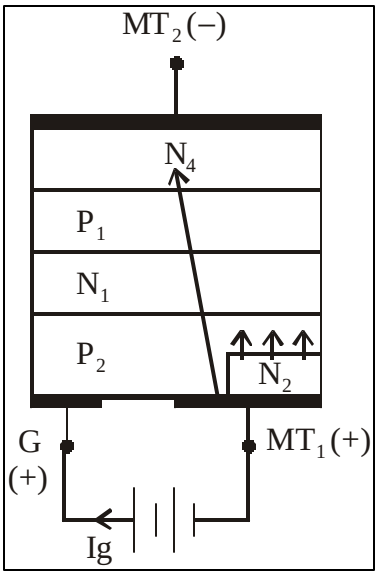
MODE (II): MT2 POSITIVE, GATE NEGATIVE

When gate terminal is negative with respect to MT1 gate current flows through p_2n_3 junction and forward biases this junction. As a result the triac starts conducting through $p_1n_1p_2n_3$ initially. With the conduction of $p_1n_1p_2n_3$ the voltage drop across this path falls but the potential of layer between p_2n_3 rises towards the anode potential of MT2. As the right hand portion of p_2 is clamped at cathode potential of MT1 a potential gradient exists across layer p_2. Its left hand side being at a higher potential than its right hand side a current is thus established in layer p_2 from left to right which forward bias the p_2n_2 junction and finally the main structure $p_1n_1p_2n_2$ begins to conduct. The structure of $p_1n_1p_2n_3$ may be regarded as an auxiliary SCR and the structure $p_1n_1p_2n_2$ as the main SCR. It can be stated that the anode current of the auxiliary SCR serves as the gate current of the main SCR. This mode of operation is less sensitive as compared to the previous mode since more gate current is required.



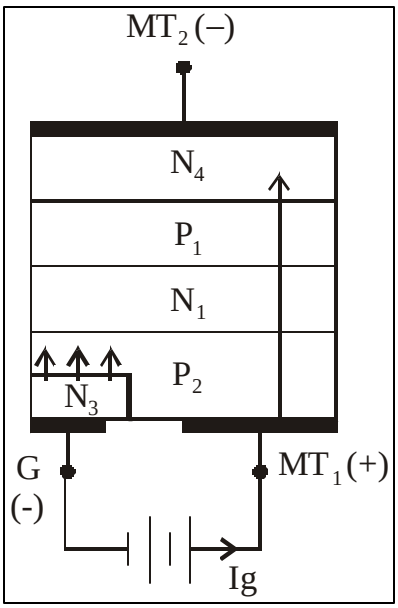
MODE (III): MT2 NEGATIVE, GATE POSITIVE

The gate current I_G forward bias p_2n_2 junction. Layer n_2 injects negative electrons $\left(e^{-}s\right)$ into the p_2 layer as shown . With n_2 layer acting as a remote gate the structure $p_2n_1p_1n_4$ eventually turns on. As usual the current after conduction is limited by the external load. Since in this mode the triac is turned on by a remote gate n_2, the device is less sensitive in the III quadrant with positive gate current.



MODE (IV): MT2 NEGATIVE, GATE NEGATIVE

In this mode the layer n_3 acts as a remote gate. The gate current forward bias the n_3p_2 junction. Finally the structure $p_2n_1p_1n_4$ is turned on. Though the triac is turned on by a remote gate n_3 yet the device is more sensitive in this mode.



CONCLUSION

We can conclude that the sensitivity of the triac is greatest in first quadrant and third quadrant. Thus the triac is rarely operated in the first quadrant with negative gate current and in the third quadrant with positive gate current.

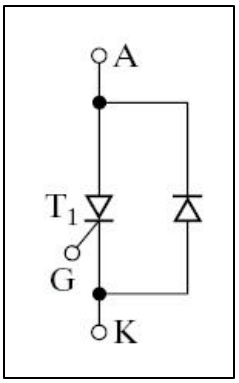
As the two conducting paths from MT1 to MT2 or from MT2 to MT1 interact with each other in the structure of the traic, voltage, current and frequency ratings are much lower as compared to conventional Thyristors. The maximum ratings are around 1200V, 300A.

APPLICATIONS

Triacs are used in heat control and for speed controls of small single phase series and induction motors.

REVERSE CONDUCTING THYRISTORS

In many choppers and inverter circuits, an antiparallel diode is connected across an SCR in order to allow a reverse current flow due to inductive load and to improve the turn-off requirement of commutation circuit. The diode clamps the reverse blocking voltage of the SCR to 1 or 2V under steady state conditions. However, under transient conditions, the reverse voltage may rise to 30V due to inducted voltage in the circuit stray inductance within the device.



An RCT is a compromise between the device characteristics and circuit requirement; and it may be considered as a thyristor with a built-in antiparallel diode. An RCT is also called an *asymmetrical thyristor* (ASCR). The forward blocking voltage varies from 400 to 2000V and the current rating goes up to 500A. The reverse blocking voltage is typically 30 to 40V. Since the ratio of forward current through the thyristor to the reverse current of diode is fixed for a given device, their applications will be limited to specific circuit designs.

STATIC INDUCTION THYRISTORS

The characteristics of SITH are similar to those of a MOSFET. A SITH is normally turned on by applying a positive gate voltage like normal Thyristors and is turned off by application of negative voltage to its gate. A SITH is a minority carrier device. As a result, SITH has low on-state resistance or voltage drop and it can be made with higher voltage and current ratings.

A SITH has fast switching speeds and high dv/dt and di/dt capabilities. The switching time is on the order of 1 to 6μsec. The voltage rating can go upto 2500V and the current rating is limited to 500A. This device is extremely process sensitive, and small perturbations in the manufacturing process would produce major changes in the device characteristics.

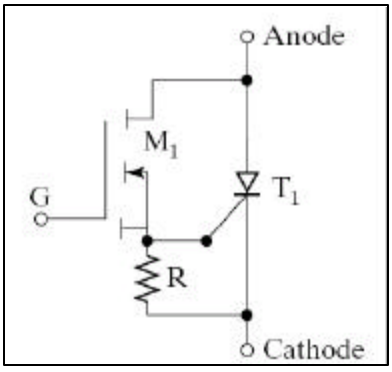
LIGHT-ACTIVATED SILICON CONTROLLED RECTIFIERS

This device is turned on by direct radiation on the silicon wafer with light. Electron-hole pairs which are created due to the radiation produce triggering current under the influence of electric field. The gate structure is designed to provide sufficient gate sensitivity for triggering from practical light source.

The LASACRs are used in high voltage and high current applications (e.g., high-voltage dc (HVDC) transmission and static reactive power or volt-ampere reactive (VAR) compensation). A LASCR offers complete electrical isolation between the light-triggering source and the switching device of power converter, which floats at a potential of as high as a few hundred kilovolts. The voltage rating of a LASCR could be as high as 4kV at 1500A with light-triggering power of less than 100mW. The typical di/dt is 250 A/μsec and the dv/dt could be as high as 2000 V/μsec.

FET CONTROLLED THYRISTORS

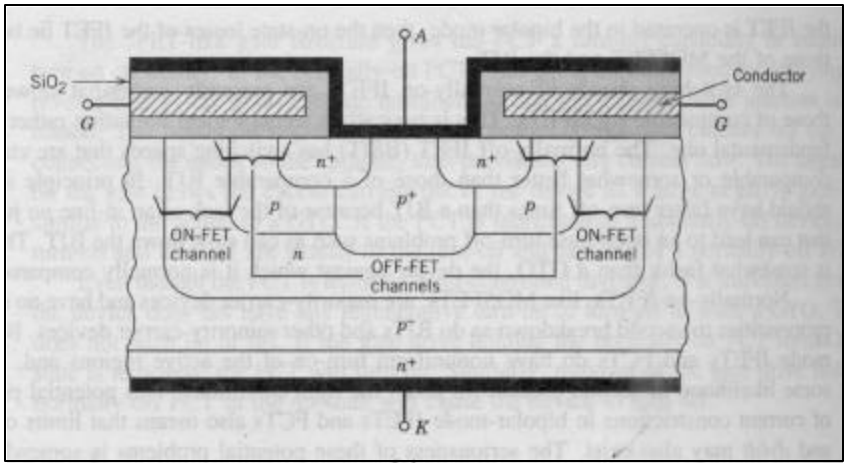
A FET-CTH device combines a MOSFET and a thyristor in parallel is as shown in figure. If a sufficient voltage is applied to the gate of the MOSFET, typically 3V, a triggering current for the thyristor is generated internally. It has a high switching speed, high di/dt and high dv/dt.



This device can be turned on like conventional Thyristors, but it can not be turned off by gate control. This would find applications where optical firing is to be used for providing electrical isolation between the input or control signal and the switching device of the power converter.

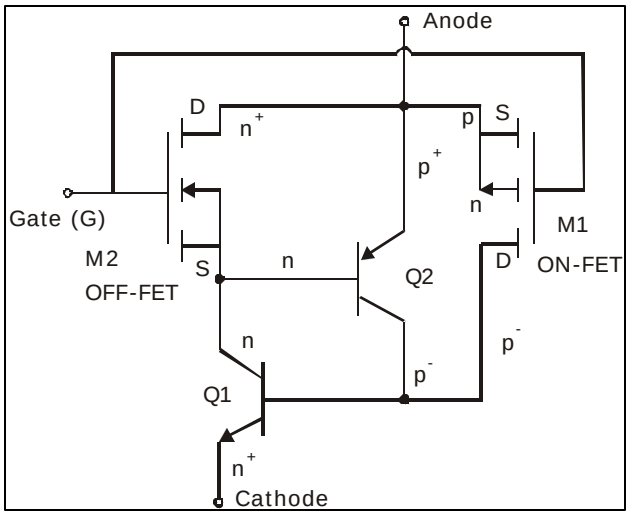
MOS-CONTROLLED THYRISTOR

A MOS controlled Thyristors or MCTs are a new devices that have recently become commercially available. It is basically a thyristor with two MOSFETs built in the gate structure. One MOSFET is for turning on the MCT and the other is to turn off the MCT. There are two types P-MCT and N-MCT. They have low on-state losses and large current capabilities of Thyristors with the advantages of MOSFET controlled turn-on and turn-off and relatively fast switching speeds.



The figure shows a single cell of MCT. Several thousands of such cells are fabricated integrally on the same silicon wafer and all cells are connected electrically in parallel. The thyristor portion of the device has the same structure as a conventional thyristor. The NPNP structure is represented by two transistors, one NPN and the other a PNP transistor. The MOS gate structure is represented a p-channel MOSFET M_1 which is the ON FET and n -channel MOSFET M_2 which is the OFF FET.

Operation



The equivalent circuit of a p-MCT is shown due to NPNP structure rather than PNPN structure of a normal SCR the anode serves as the reference terminal with respect to which all gate signals are applied. Let MCT be in its forward blocking state and a negative signal V_{GA} is applied. Then a p-channel is formed in the n-doped material of the p-channel MOSFET M_1 which causes holes to flow laterally from p^- layer to the p layer. This carrier movement causes transistor Q_1 to turn-on. This in turn turns ON transistor Q_2 since the collector of Q_1 is connected to the base of Q_2. Positive feedback and regeneration between the two transistors takes place just like in a conventional thyristor and hence MCT turns-on.

With the application of positive voltage applied between gate and anode an n-channel is formed in the p-region of the n-channel MOSFET M_2. Now current flow is established between the n and n^+ layer through the n-channel formed. Due to this the n-channel OFF FET shorts out the base emitter junction of the PNP transistor and thus Q_2 transistor is turned off. This results in MCT returning to its blocking state.

The MCT can be operated as a gate controlled device if its current is less than the peak controllable current. Attempting to turn off the MCT at currents higher than its rated controllable current may result in destroying the device. For higher values of current, the MCT has to be commutated off like a standard SCR. The gate pulse widths are not critical for smaller device currents. For larger currents, the width of the turn-off pulse should be larger. Moreover, the gate draws a peak current during turn-off. In many applications, including inverters and choppers, a continuous gate pulse over the entire on/off period is required to avoid state ambiguity.

An MCT has

- A low forward voltage drop during conduction.
- A fast turn-on time, typically 0.4μsec and a fast turn-off time, typically 1.25μsec for an MCT of 300A, 500V.
- Low switching losses.
- A low reverse voltage blocking capability and
- A high gate input impedance, which greatly simplifies the drive circuits. It can be effectively paralleled to switch high currents with only modest deratings of the per-device current rating. It cannot easily be driven from a pulse transformer if a continuous bias is required to avoid state ambiguity.