# Lecture 6 – 7

# Differential Amplifier

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## Outline

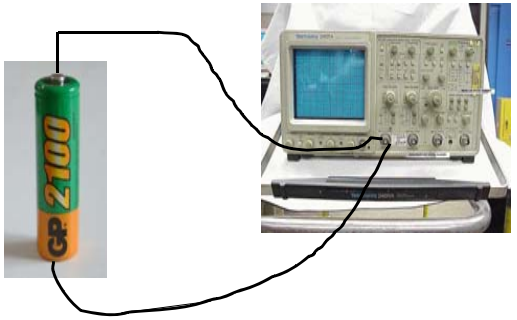
**Why differential amplifier?**

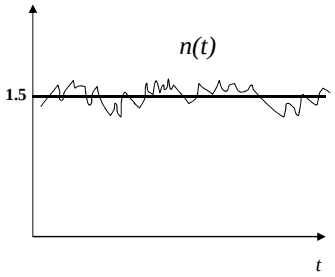
**Differential amplifier**

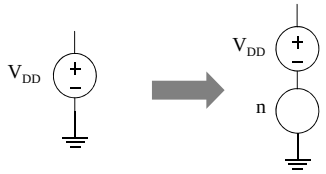
- **Large signal analysis**
- **Small signal analysis**
- **Gain**
- **CMRR**
- **Active load**



## Noise



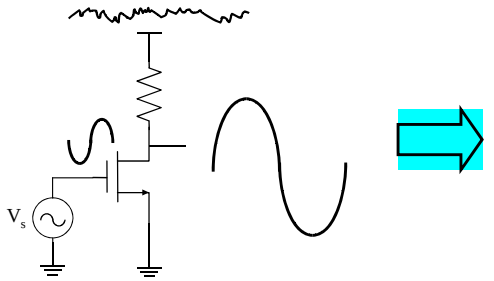




**Noise degrades information quality!**



## Noise in Single-Ended Systems

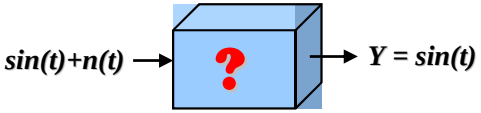



$v_o = sin(t) + n(t)$

$$\because V_o = \tilde{V}_{DD} - R_D I_D = V_{DD} + n(t) - R_D I_D$$
$$= V_{DD} + n(t) - R_D(g_m \cdot v_s)$$

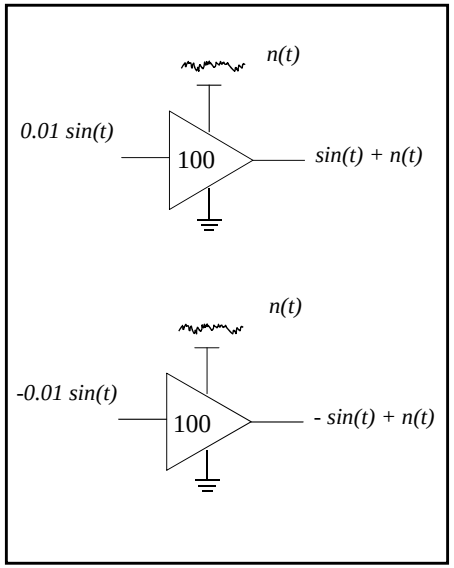
**How can we get rid of this noise?**

# Getting rid of noise



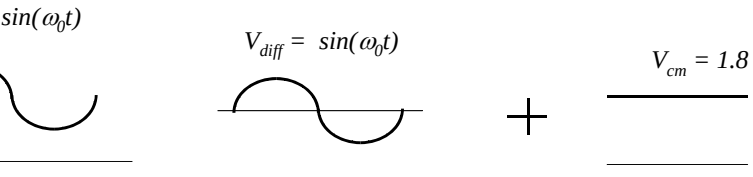

**Need to subtract n(t), but not the signal.**

$$\begin{array}{r|l} & Y_p = \ Y_{signal} + n(t) \\ - & Y_n = -\ Y_{signal} + n(t) \\ \hline & Y_p - Y_n = 2\,Y_{signal} \end{array}$$






# Differential Signaling




$$V_{signal} = V_{diff} + V_{cm}$$

$$V_{diff} = V_p - V_n$$

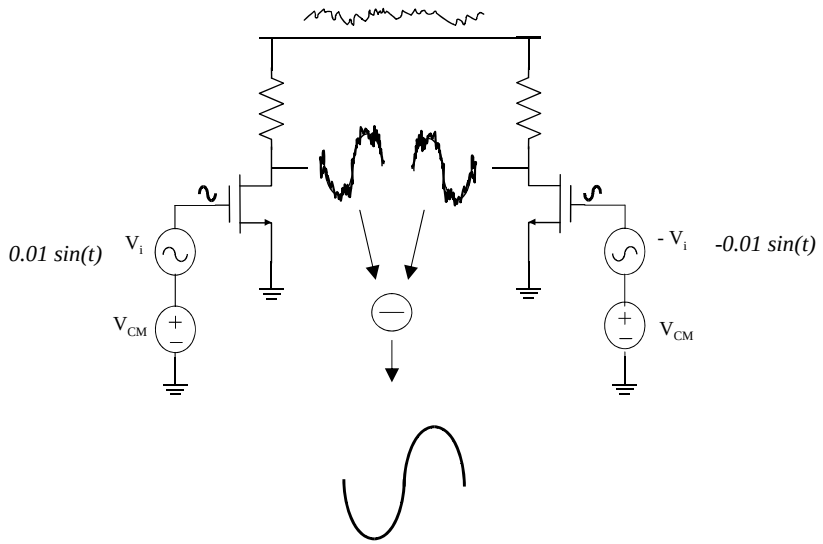
$$V_{CM} = 0.5(V_p + V_n)$$

$$V_p = \ 0.5\,V_{signal} + V_{cm}$$

$$V_n = -\,0.5\,V_{signal} + V_{cm}$$

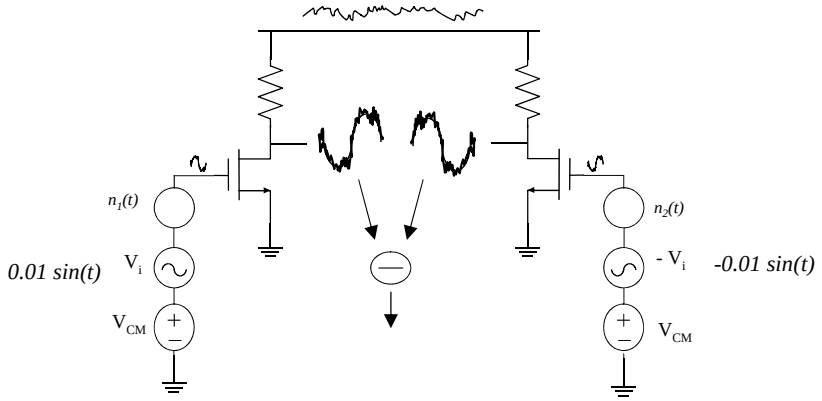


# Differential Signaling



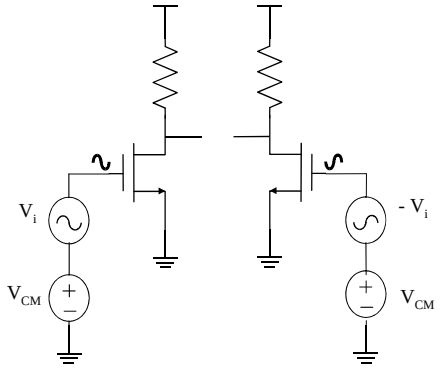



# How about non-common mode noise?




**Differential amplifier is ONLY immune to common-mode noise !**

# Differential Pair Configuration




**< Differential Gain >**

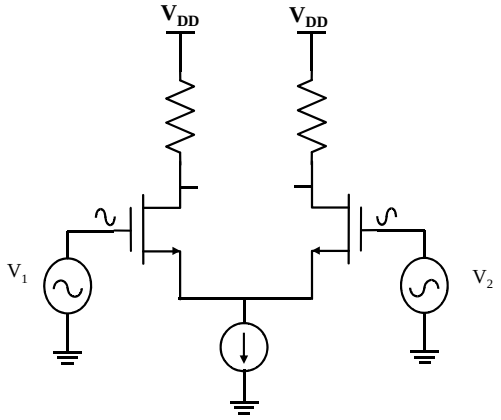
$$g_m R_D \propto \sqrt{I} \cdot R_D$$
$$\propto (V_{GS} - V_T) \cdot R_D$$
$$\propto (V_{CM} - V_T) \cdot R_D$$

**Gain is dependent on common mode voltage.**

**How do we make gain independent of common mode voltage ?**



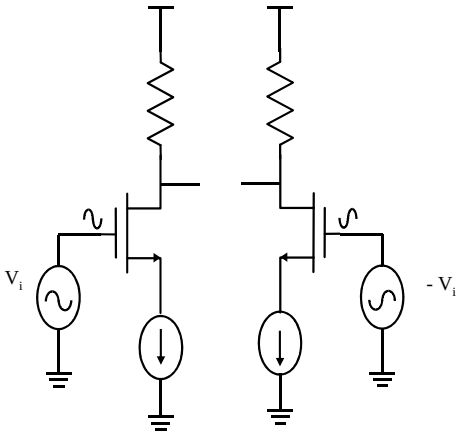
# Differential Pair Configuration




*Differential gain is independent of common mode voltage.*



# Differential Pair Configuration

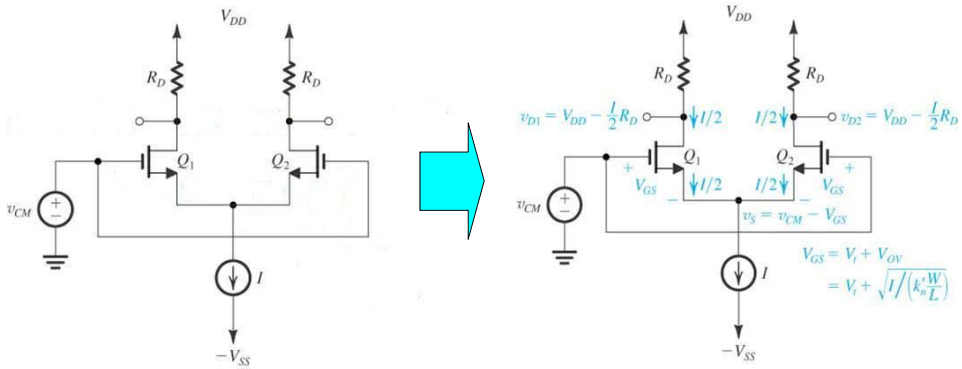



**What is the gain?**

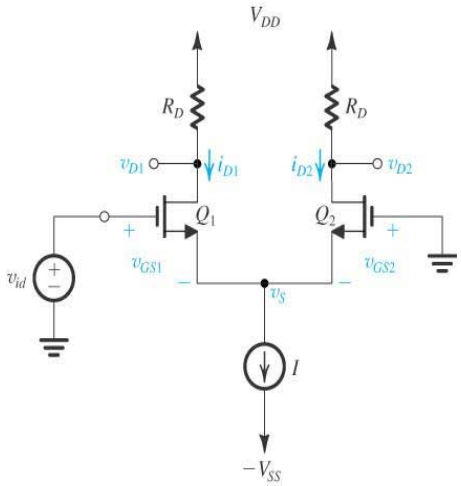
$-g_m R_D$ **?**



# Common-mode Input Voltage



# Differential Input Voltage




**With $v_{id}$ positive**

$v_{GS1} > v_{GS2}$, $i_{D1} > i_{D2}$, and $v_{D1} < v_{D2}$

$(v_{D2} - v_{D1})$ will be positive.

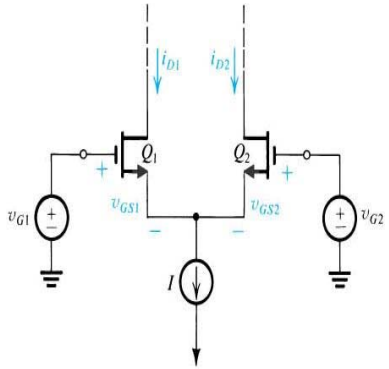
**With $v_{id}$ negative**

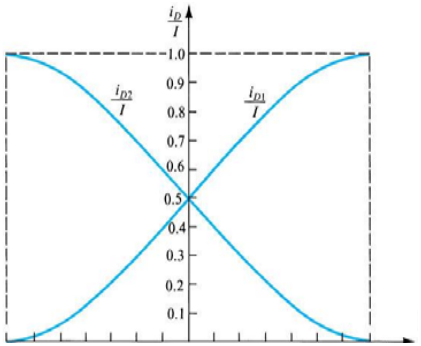
$v_{GS1} < v_{GS2}$, $i_{D1} < i_{D2}$, and $v_{D1} > v_{D2}$

$(v_{D2} - v_{D1})$ will be negative.



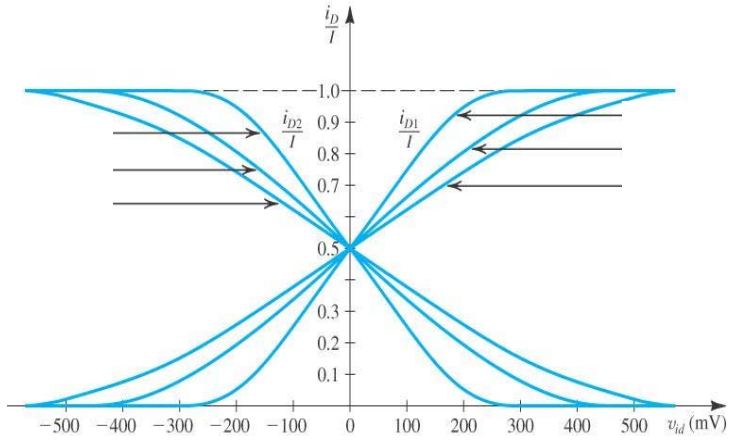
# Large Signal Operation





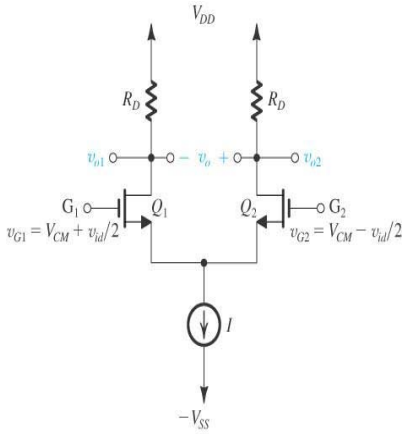

# Large Signal Operation

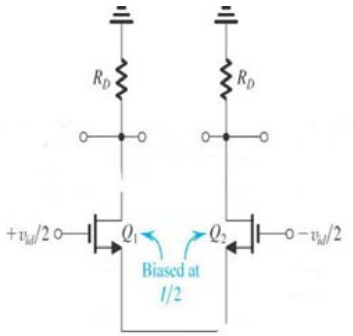



The linear range of operation of the MOS differential pair can be extended by reducing (W/L).

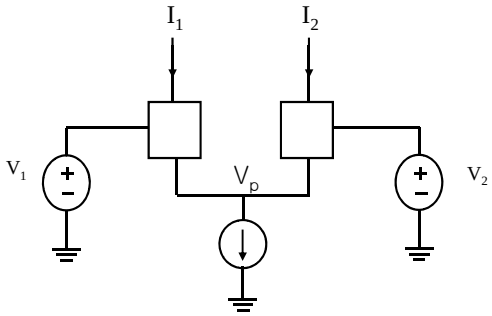


# Differential Gain in Small Signal Operation



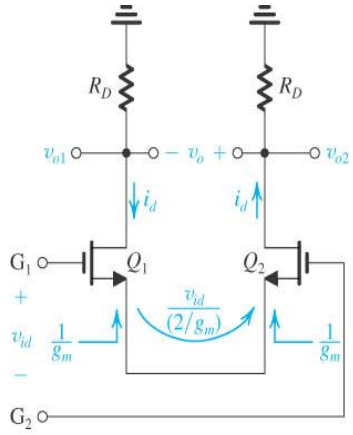
# Virtual Ground




For differential input, Vp does not change only if the circuit is **linear.**
(refer to Razavi pp. 114)



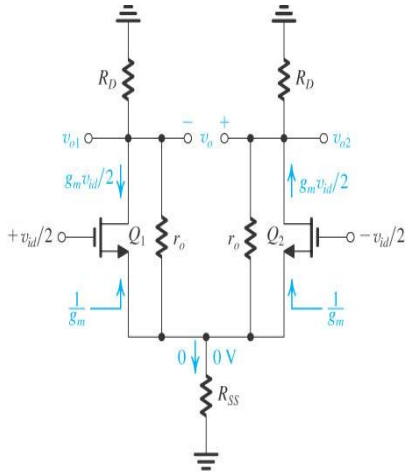
# Differential Gain in Small Signal Operation

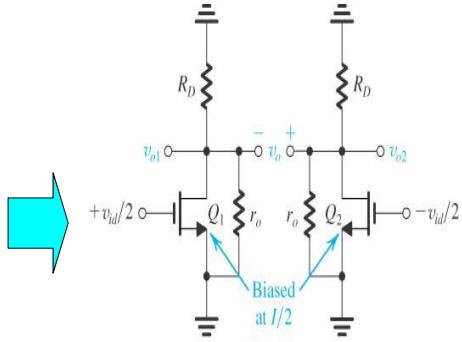



$$A_d = \frac{v_{o2} - v_{o1}}{v_{id}} = g_m R_D$$



# Differential Gain due to Output Resistance

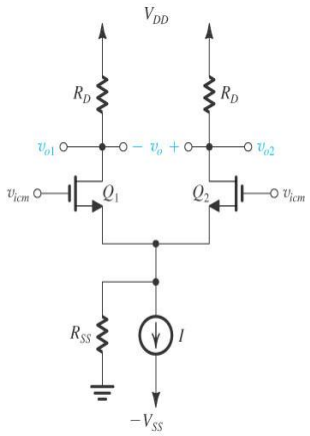


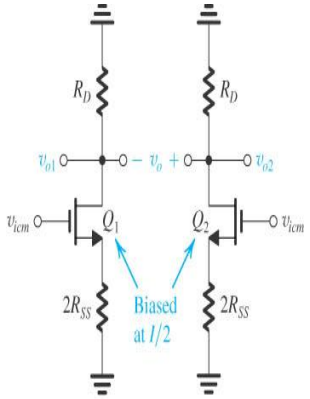




$$R_{out} \Rightarrow (R_D \,//\, r_O)$$



# Common-mode Gain

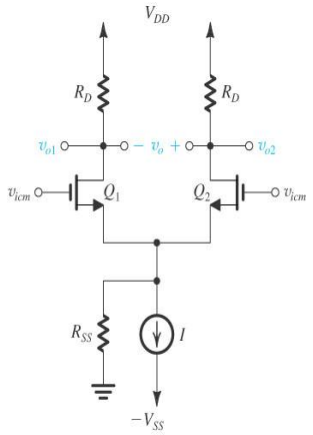



*Common-mode gain : differential & single-ended*

# Common-mode Rejection Ratio

$$CMRR = \left| \frac{A_d}{A_{CM}} \right|$$




CMRR can be considered as Signal-to-Noise Ratio!



# Input Offset Voltage

- Input offset voltage

  $V_{OS} = V_O/A_d$

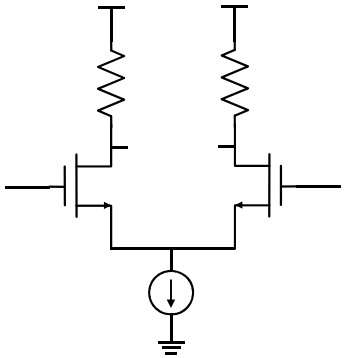
  (Vo: output voltage when Vin = 0)

- Mismatch



# Offset Voltage due to Mismatch

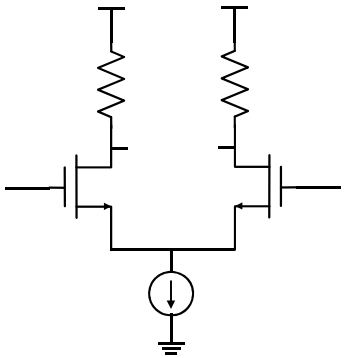
- Mismatch in R
- Mismatch in W/L



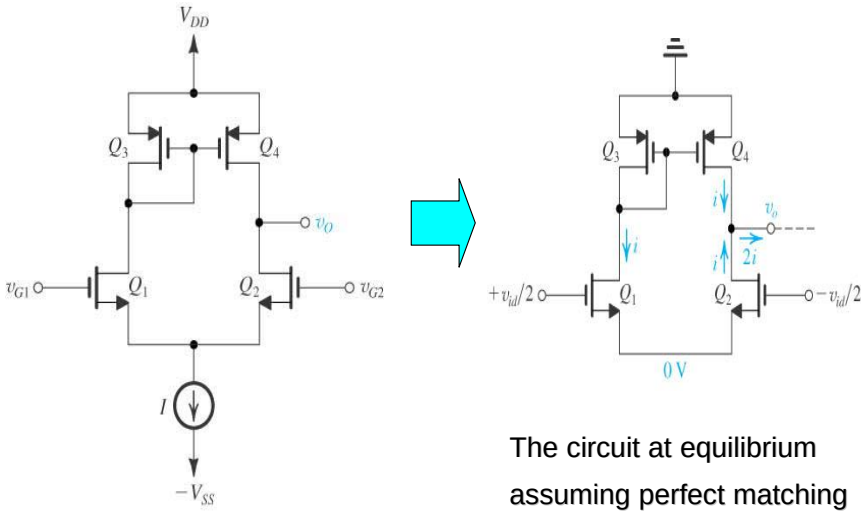


# Offset Voltage due to Mismatch

- Mismatch in Vth



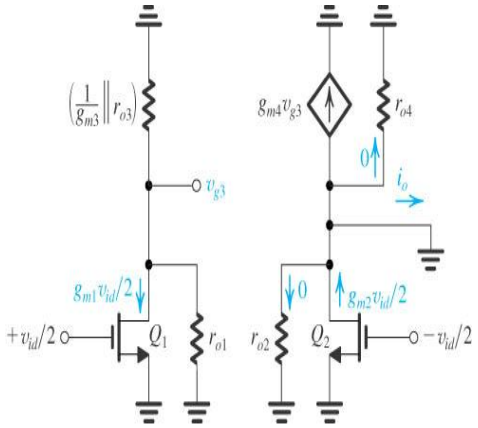
# Differential Amplifier with active load




The circuit at equilibrium assuming perfect matching

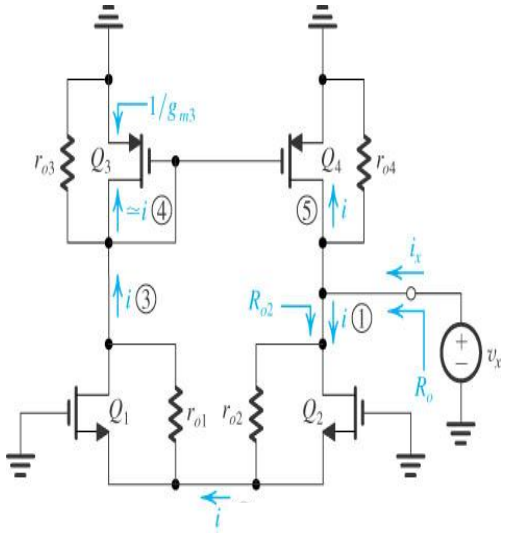


# Determining the Transconductance






# Determining the Output Resistance






# Common-mode Gain and CMRR