Class 13: Flip Flops

Topics:

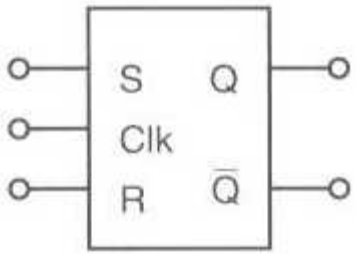
1. TOC
2. Introduction
3. Types of Flip Flops
4. Types of Flip Flops
5. D Flip Flop Operation
6. D Flip Flop Master Circuit
7. D Flip Flop Circuit
8. Tri-State Inverter
9. Flip-Flop Ideas
10. Flip-Flop Ideas

Class 13: Flip Flops

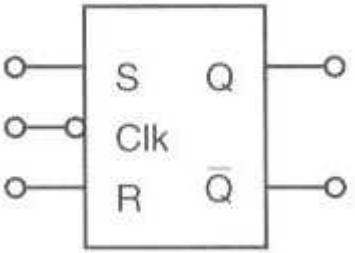
Introduction (Martin c.7)

Flip Flops basics:

- Storage elements for synchronous circuits (what is synchronous?)
- Break up any race conditions or oscillations, i.e., feedback loops around a cyclic logic circuit
- Inputs: normally have 1 or 2 input signals and a clock
- Outputs: differential outputs Q and Q'
    - output latched or stored on rising/falling edge of clock
    - output stable until next rising/falling edge of clock
- Can optionally have set and/or reset asynchronous inputs
    - regardless of state of the clock, the outputs will either be set to a 1 or reset to a 0
- Typical techniques
    - master_slave
    - edge_sensitive
- Typical configurations:
    - SR (set_reset)
    - D
    - JK
    - T (toggle)
- D FF is the most common for ICs



SR flip flop symbol
- changes on positive going clock edge



SR flip flop symbol
- changes on negative going clock edge

Class 13: Flip Flops

Types of Flip Flops (Martin c.7)

- D

Table 7.1 The Characteristic Table for a D Flip-flop

D	Q_{n+1}
0	0
1	1

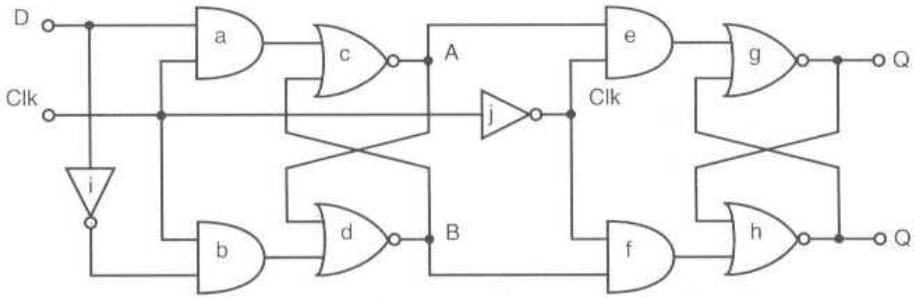


Figure 7.17 The logic diagram of a master–slave D flip-flop.

- SR

Table 7.2 The Characteristic Table of an SR Flip-flop

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	Indeterminate

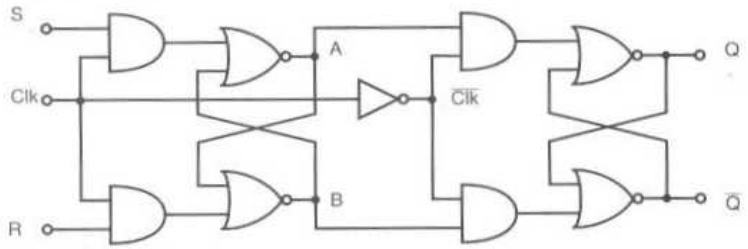
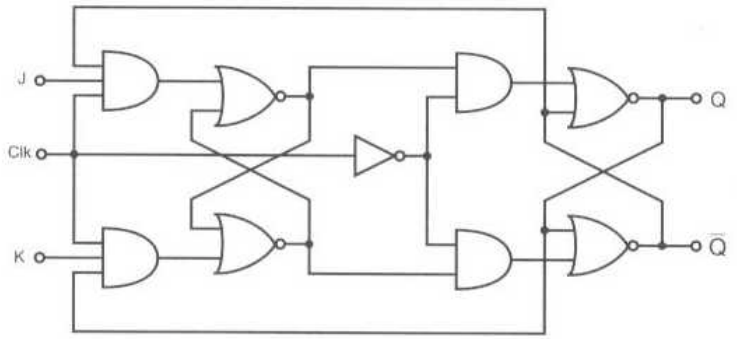


Figure 7.18 The logic diagram of a master–slave SR flip-flop.

- JK

Table 7.3 The Characteristic Table for a JK Flip-flop

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$



- T

Table 7.4 The Characteristic Table for a Toggle or T Flip-flop

T	Q_{n+1}
0	Q_{n+1}
1	$\overline{Q}_{n+1}$

realized by tying J and K together from a JK FF

Class 13: Flip Flops

Types of Flip Flops (Martin c.7)

•D

- •cascade of two latches with opposite clock phases
- •best choice (usually) for IC design
- •after FF is clocked, output is equal to the D value just before the clock changed

---

•SR

- •same as D FF if S=D and R=D'
- •can be set, reset, or remain in its previous state
- •intedeterminate state exists if S=R=high when CLK=low
- •major limitation is output can be affected by the input at any time the CLK is high, a.k.a., noise problem

---

•JK

- •often used for synchronous machines or counters
- •J=1, K=0 FF is set
- •J=0, K=1 FF is reset
- •J=0, K=0 No change
- •J=1, K=1 FF state toggles (difference between JK and SR, but same noise limitation)

•T

- •useful in counters

Class 13: Flip Flops

D Flip Flop Operation (Martin c.7)

Clk is ‘1’, implies master active, slave latched
B=D=1 since 1 or anything is 1 in ‘c’

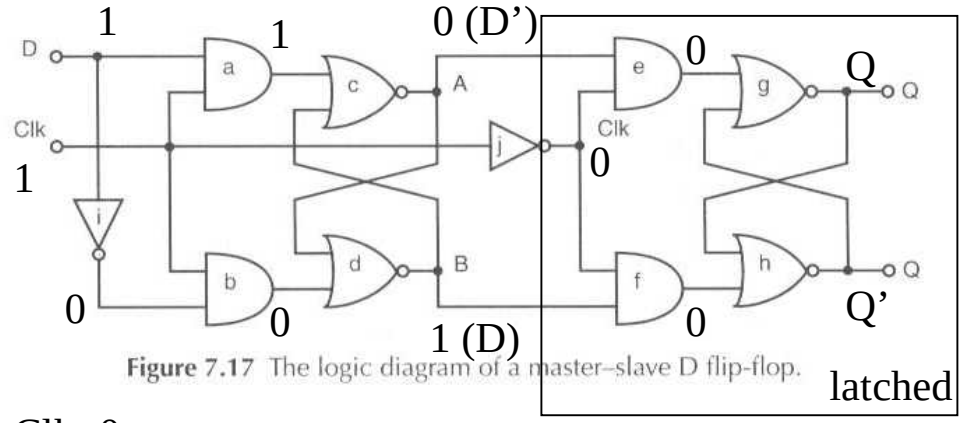


Figure 7.17 The logic diagram of a master–slave D flip-flop.

Clk is ‘1’, implies master active, slave latched
B=D=0 since 1 or anything is 1 in ‘d’

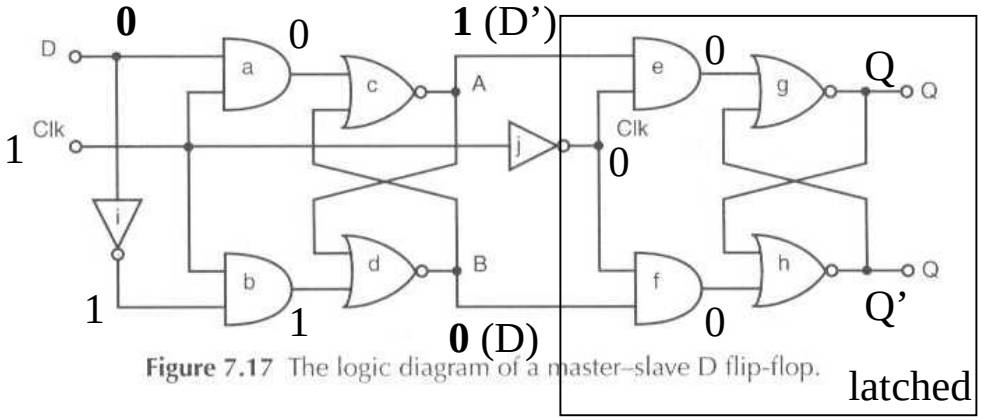


Figure 7.17 The logic diagram of a master–slave D flip-flop.

Clk=0

D=0

Clk is ‘0’, implies master latched, slave active
Q’=D’=0 since 1 or anything is 1 in ‘h’

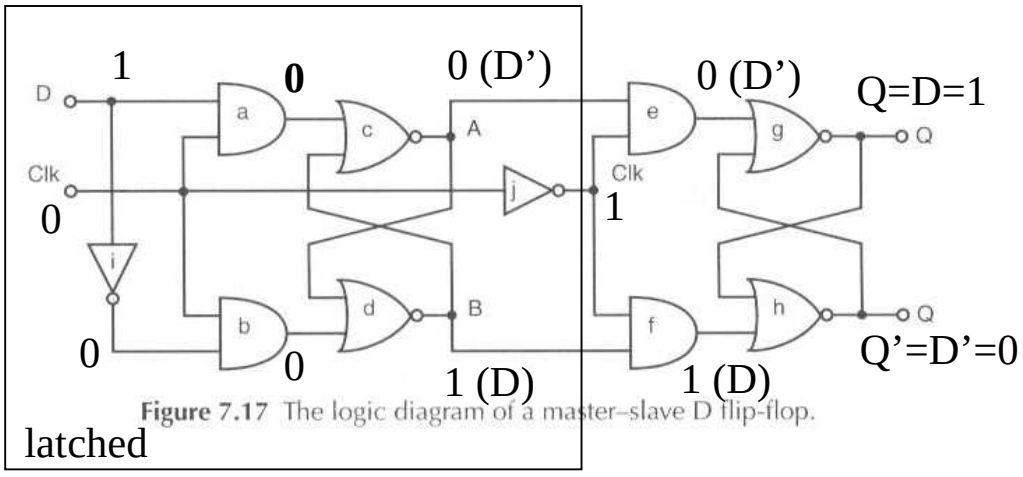


Figure 7.17 The logic diagram of a master–slave D flip-flop.

Clk is ‘0’, implies master latched, slave active
Q’=D’=0 since master disabled by ‘a’ and ‘b’

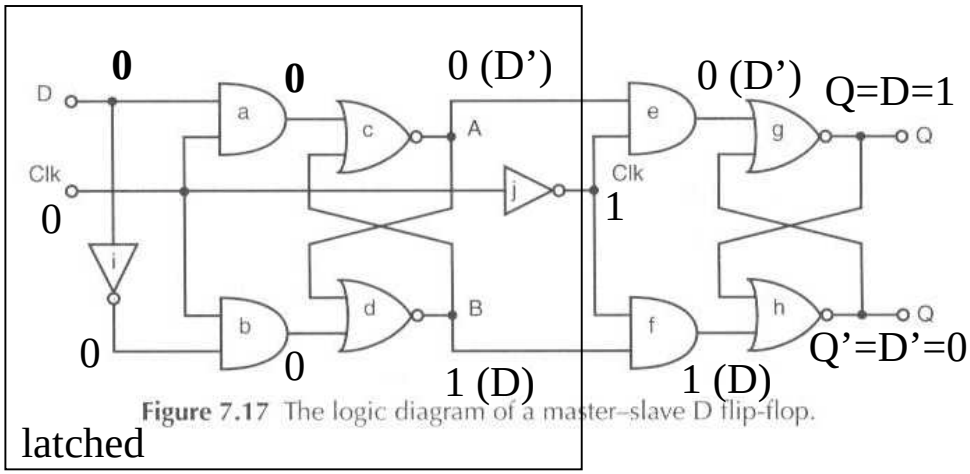


Figure 7.17 The logic diagram of a master–slave D flip-flop.

Class 13: Flip Flops

D Flip Flop Master Circuit (Martin c.7)

master

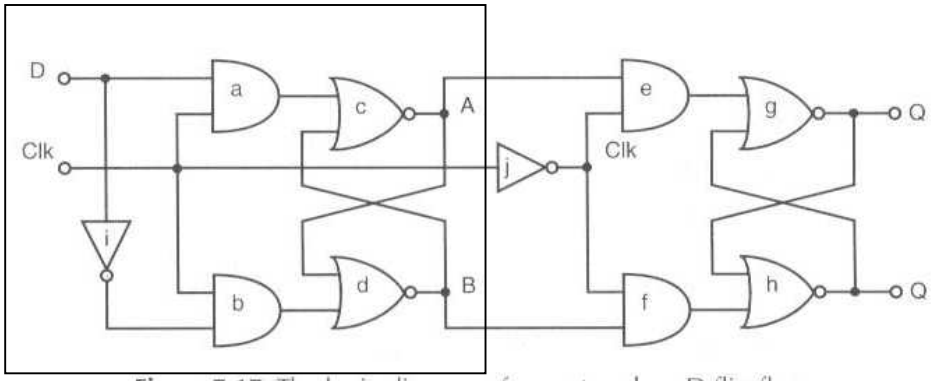
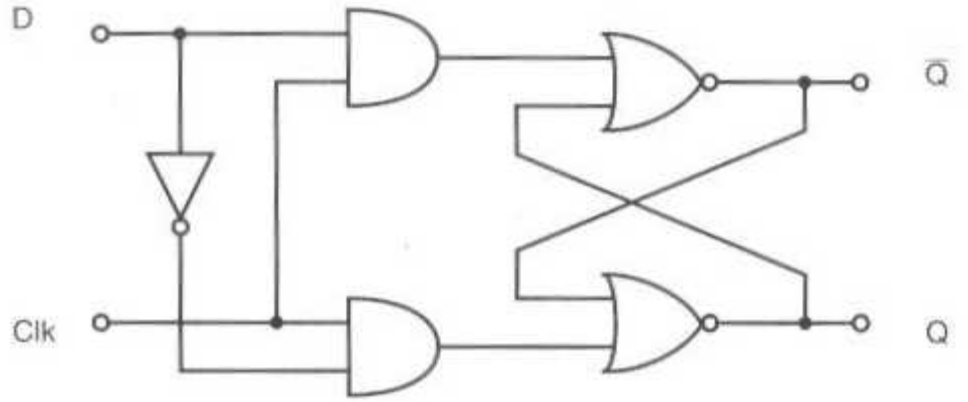
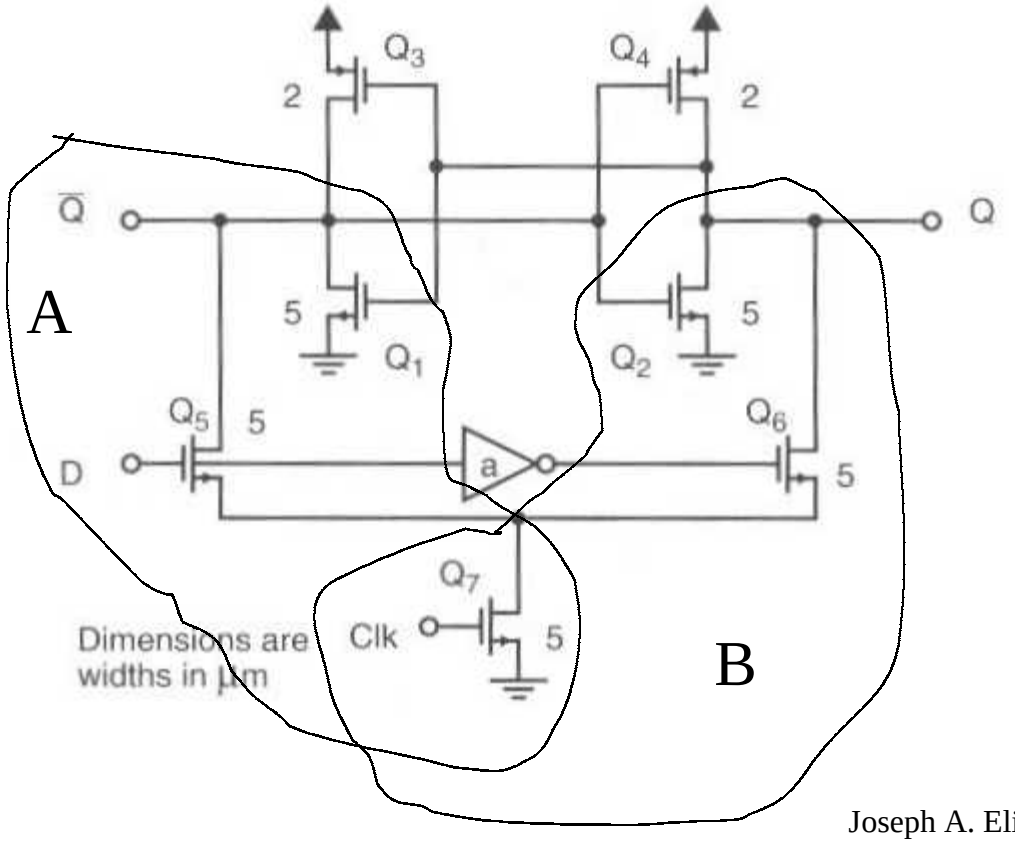
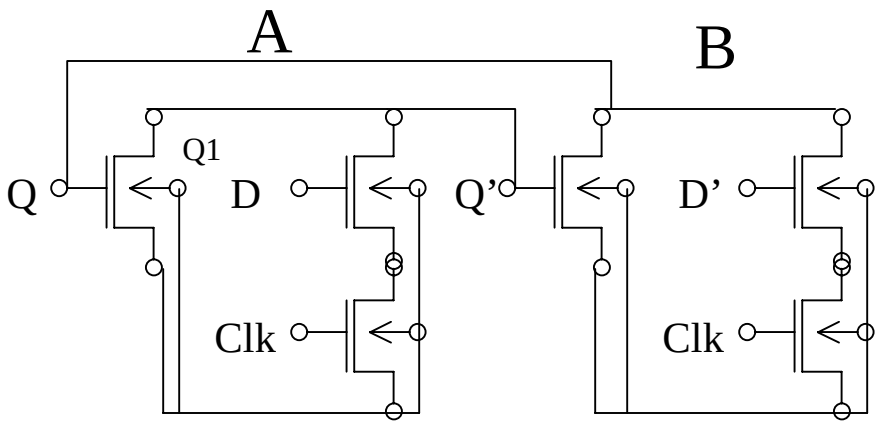


Figure 7.17 The logic diagram of a master–slave D flip-flop.







[Q + (D)(Clk)]'

[Q' + (D')(Clk)]'

Class 13: Flip Flops

D Flip Flop Circuit (Martin c.7)

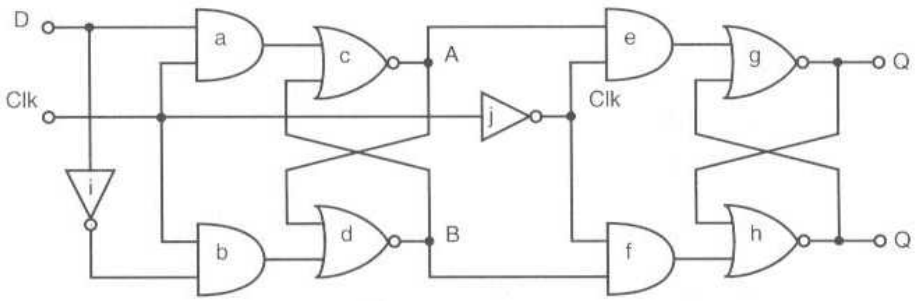
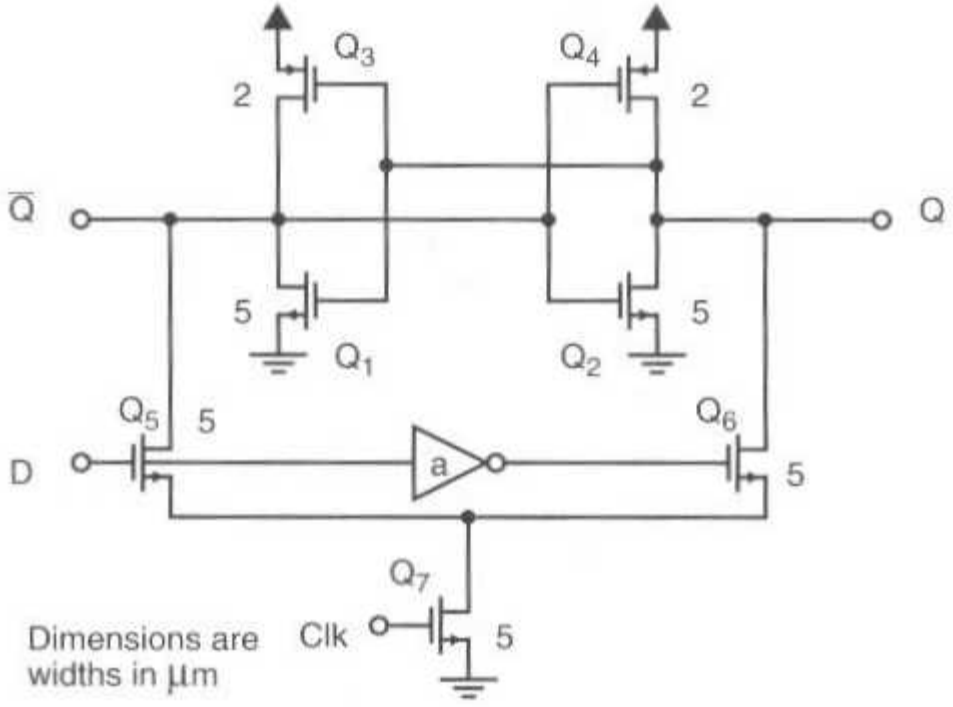
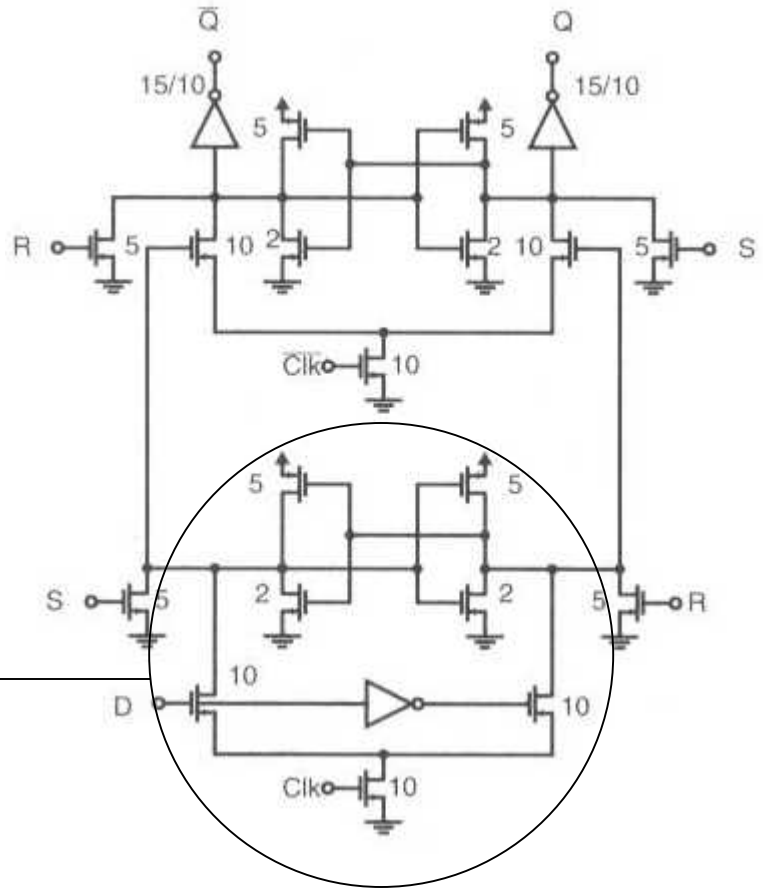


Figure 7.17 The logic diagram of a master–slave D flip-flop.

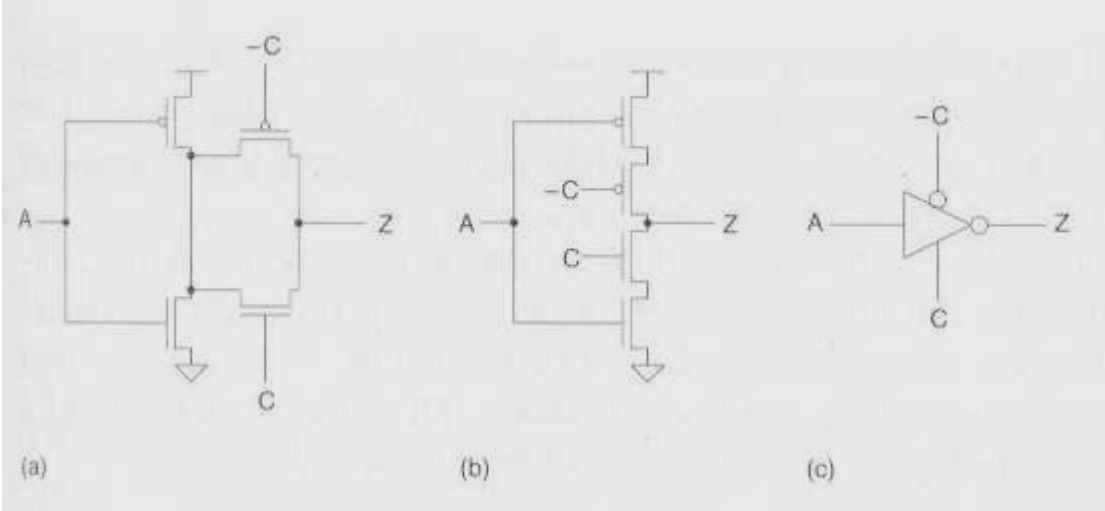




- S = 1 : Q = 0 immediately, Q' = S' after inv delay
- R = 1 : Q' = 1 immediately, Q = R' after inv delay

Class 13: Flip Flops

Tristate Inverter (Weste c.2)

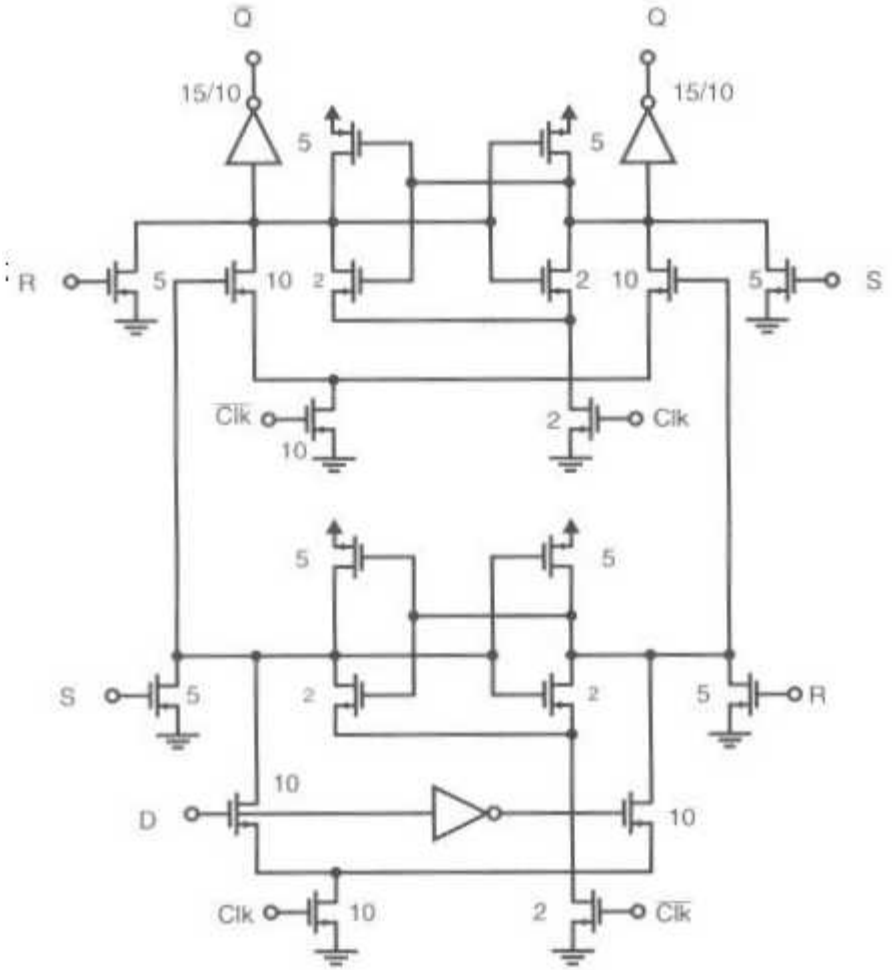


•Cascade of a transmission gate with an inverter
•C=0 –C=1: Z is tristated, i.e., A does not influence Z
•C=1 –C=0: Z = A’

Class 13: Flip Flops

Flip Flop Ideas (Martin c.7)

- Biphase D FF
- asynchronous Set and Reset
- Inverter Based



- Biphase D FF
- transmission gates used
- NOR based

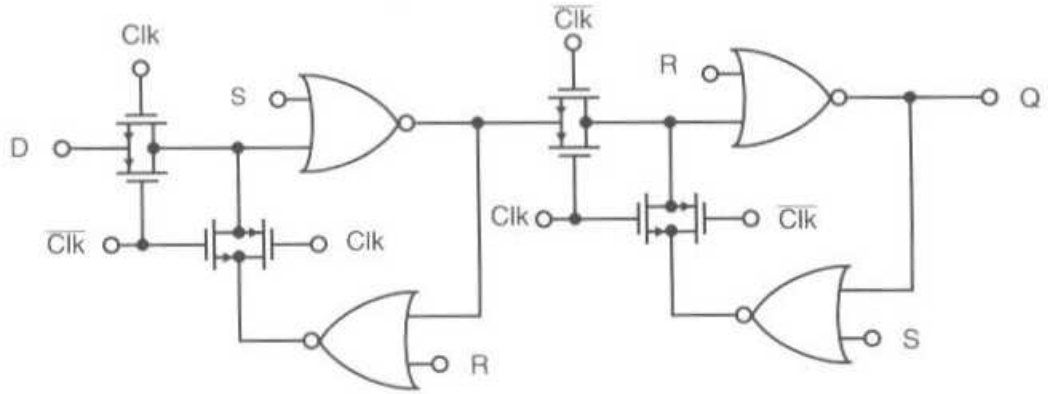
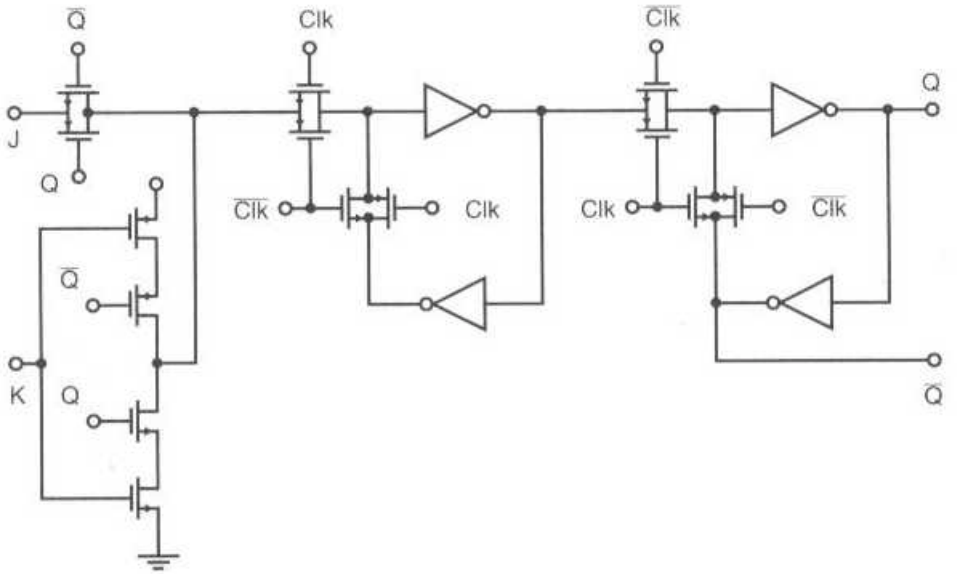


Figure 7.27 A transmission-gate-based master–slave D flip-flop.

Class 13: Flip Flops

Flip Flop Ideas (Martin c.7)

- Biphase JK FF
- transmission gates used
- Inverter based



Design Assignment

- Biphase D FF (clk, clk')
- buffer the D input with a tristate inverter
- Inverter based
- Asynchronous Reset
- hint: can optimize the layout by rearranging ckt

?