I B.Tech I Sem

BASIC ELECTRICAL AND ELECTRONICS ENGINEERING

Questions and Answers for Units III, IV & V

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Syllabus

UNIT I: ELECTRICAL and SINGLE PHASE AC CIRCUITS

Electrical Circuits - R-L-C Parameters, Voltage and Current Independent and Dependent Sources, Source Transformation – V–I relationship for Passive elements, Kirchoff's Laws, Network reduction techniques – series, parallel, series parallel, star–to-delta, delta-to-star transformation, Nodal Analysis.

Single Phase AC Circuits - R.M.S. and Average values, Form Factor, steady state analysis of series, Parallel and Series parallel Combinations of R, L and C with Sinusoidal excitation, concept of reactance, Impedance, Susceptance and Admittance – phase and phase difference, Concept of Power Factor, j-notation, complex and Polar forms of representation.

UNIT II: RESONANCE and NETWORK THEOREMS

Resonance – series resonance and parallel resonance circuits, concept of bandwidth and Q factor, Locus Diagrams for RL, RC and RLC Combinations for Various Parameters.

Network Theorems - Thevenin's, Norton's, Maximum Power Transfer, Superposition, Reciprocity, Tellegen's, Millman's and Compensation theorems for DC and AC excitations.

UNIT III: P-N JUNCTION DIODE & DIODE CIRCUITS

P-N Junction Diode - Diode equation, Energy Band diagram, Volt-Ampere characteristic, Temperature dependence, Ideal versus practical, Static and dynamic resistances, Equivalent circuit, Load line analysis, Diffusion and Transition Capacitances.

Rectifiers and Filters - The P-N junction as a rectifier - A Half Wave Rectifier, Ripple Factor, Full Wave Rectifier, Bridge Rectifier, Harmonic components in Rectifier Circuits, Filters – Inductor Filters, Capacitor Filters, L- section Filters, л- section Filters.

UNIT IV: BIPOLAR JUNCTION TRANSISTOR

Bipolar Junction Transistor (BJT) - Construction, Principle of Operation, Symbol, Amplifying Action, Common Emitter, Common Base and Common Collector configurations.

Transistor Biasing And Stabilization - Operating point, DC & AC load lines, Biasing - Fixed Bias, Emitter Feedback Bias, Collector to Emitter feedback bias, Voltage divider bias, Bias stability, Stabilization against variations in V_{BE} and I_{C0} , Bias Compensation using Diodes and Transistors.

Transistor Configurations - BJT modeling, Hybrid model, Determination of h-parameters from transistor characteristics, Analysis of CE, CB and CC configurations using h-parameters, Comparison of CE, CB and CC configurations.

UNIT V: JUNCTION FIELD EFFECT TRANSISTOR & SPECIAL PURPOSE DEVICES

Junction Field Effect Transistor - Construction, Principle of Operation, Symbol, Pinch-Off Voltage, Volt-Ampere Characteristic, Comparison of BJT and FET, Small Signal Model, Biasing FET.

Special Purpose Devices - Breakdown Mechanisms in Semi Conductor Diodes, Zener diode characteristics, Use of Zener diode as simple regulator, Principle of operation and Characteristics of Tunnel Diode (With help of Energy band diagram) and Varactor Diode, Principle of Operation of SCR.

TEXT BOOKS:

1. Electronic Devices and Circuits – R.L. Boylestad and Louis Nashelsky, PEI/PHI, 9th Ed, 2006.
2.Millman's Electronic Devices and Circuits – J.Millman and C.C.Halkias, Satyabratajit, TMH, 2/e, 1998.
3.Engineering circuit analysis- by William Hayt and Jack E. Kemmerly, Mc Graw Hill Company, 6th edition.

REFERANCE BOOKS:

1. Introduction to Electronic Devices and Circuits-Rober T. Paynter, Pearson Education.
2. Electronic Devices and Circuits -¬ K. Lal Kishore, B.S. Publications, 2nd Edition, 2005.
3. Linear circuit analysis (time domain phasor and Laplace transform approaches)- 2nd edition by Raymond A. DeCarlo and Pen-Min-Lin, Oxford University Press-2004.
4. Network Theory by N.C.Jagan & C.Lakshminarayana, B.S. Publications.

P-N Junction Diode & Diode Circuits

1. **Explain the formation of depletion region in an open circuited p-n junction with neat sketches.**

Ans:

- When two extrinsic semiconductors, one p-type and another n-type are joined, a p-n junction is formed.
- The holes from p-side and electrons from n-side which form majority carriers in their respective sections are diffused in either direction.
- At this stage p-side will loose its holes and hence a negative field exists towards left side of the junction.
- Similarly, n-side will loose its electrons and hence a positive field exists towards right side of the junction.
- The net result is that an electrical field exists across the junction. This field is known as potential barrier or contact potential.
- Potential barrier will be limited because the negative field on p- side and positive of n-side prevents further displacement of electrons and holes on either side respectively.
- The charge distribution is shown in figure.

Fig: Potential Distribution in p-n junction Diode

- The concentration of charge decrease as we move away from the junction. Because at the junction, holes and electrons are combined and become neutral.
- The junction is depleted of mobile charges. The region is called space charge region and its thickness is about few microns.
- The electric field intensity, which is the integral of density function ρ is shown in the figure.
- Contact potential as shown in the figure will be of the order of few tenths of volts. Its value of germanium is 0.2V and silicon is 0.6V.

2. **Draw the energy band diagram of p-n junction under open circuit conditions and explain.**

Ans:

- It is known that the Fermi level in n-type material lies just below the conduction band while in p-type material, it lies just above the valence band.
- When p-n junction is formed, the diffusion starts. The changes get adjusted so as to equalize the Fermi level in the two parts of p-n junction.
- This is similar to adjustment of water levels in two tanks of unequal level, when connected each other.
- The changes flow from p to n and n to p side till, the Fermi level on two sides get lined up.
- In n-type semi conductor , E_F is close to conduction band E_{cn} and it is close to valence band edge E_{VP} on p-side.
- So the conduction band edge of n-type semiconductor can't be at the same level as that of p-type semiconductor.
- Hence, as shown, the energy band diagram for p-n junction is where a shift in energy levels E_0 is indicated.

Fig:Energy Band Diagram for p-n Junction under open-circuit Conditions

we know that, for n-type, $E_F = E_{Cn} - kT \ln\left[\frac{N_C}{N_D}\right]$

$$E_{Cn} - E_F = kT \ln\left[\frac{N_C}{N_D}\right] \cdots\cdots\cdots\cdots\cdots\cdots (1)$$

for p-type, $E_F = E_{Vp} + kT \ln\left[\frac{N_V}{N_A}\right]$

$$E_F - E_{Vp} = kT \ln\left[\frac{N_V}{N_A}\right] \cdots\cdots\cdots\cdots\cdots\cdots (2)$$

Since, $n = p = n_i \; and \; np = n_i^2$

In N-type, $n_n \cong N_D$

$$n_n p_n \cong n_i^2$$

$$p_n = \frac{n_i^2}{N_D} \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (3)$$

In P-type $p_p \cong N_A$

$$n_p p_p \cong n_i^2$$

$$n_p = \frac{n_i^2}{N_A} \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (4)$$

From the energy band diagram

$$E_{Cn} - E_F = \frac{E_G}{2} - E_2 \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (5)$$

$$E_F - E_{Vp} = \frac{E_G}{2} - E_1 \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (6)$$

From equation (5)and equation (6), we get,

$$E_1 + E_2 = E_G - \left[E_{Cn} - E_{Vp}\right] \cdots\cdots\cdots\cdots\cdots\cdots\cdots (7)$$

Also from band structure, $E_0 = E_1 + E_2 \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (8)$

From equation (7) and equation (8), we get,

$$E_0 = E_G - \left[E_{Cn} - E_{Vp}\right] \cdots\cdots\cdots\cdots\cdots (9)$$

By adding equation (1) and (2), we get,

$$E_{Cn} - E_F + E_F - E_{Vp} = kT \ln\left[\frac{N_C}{N_D}\right] + kT \ln\left[\frac{N_V}{N_A}\right]$$

$$E_{Cn} - E_{Vp} = kT \ln\left[\frac{N_C}{N_D}\right] + kT \ln\left[\frac{N_V}{N_A}\right] \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (10)$$

Since, $np = e^{-(E_C - E_F)/kT} . N_C e^{-(E_F - E_V)/kT} . N_V$

$$n_i^2 = N_C\, N_V\, e^{-(E_C - E_V + E_F - E_F)/kT}$$

$$\frac{n_i^2}{(N_C N_V)} = e^{-(E_C - E_V)/kT}$$

$$\gg \qquad \frac{n_i^2}{(N_C N_V)} = e^{-\left(\frac{E_G}{kT}\right)} \qquad [\therefore\ E_C - E_V = E_G]$$

Taking ln on both sides we get,

$$\ln\left[\frac{n_i^2}{N_C\, N_V}\right] = -\left[\frac{E_G}{kT}\right]$$

$$kT \ln\left[\frac{N_C\, N_V}{n_i^2}\right] = E_G \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (11)$$

substituting the values of equation (10) and equation (11) in equation (9), we get,

$$E_0 = kT \ln\left[\frac{N_C\, N_V}{n_i^2}\right] - kT \ln\left[\frac{N_C}{N_D}\right] - kT \ln\left[\frac{N_V}{N_A}\right]$$

$$E_0 = kT \ln\left[\frac{N_C\, N_V}{n_i^2} \times \frac{N_D}{N_C} \times \frac{N_A}{N_V}\right]$$

$$E_0 = kT \ln\left[\frac{N_A N_D}{n_i^2}\right] \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (12)$$

Further for p-type, $p_{p_0} = N_A$, $n_{p0} = \frac{n_i^2}{N_A}$, $N_A = \frac{n_i^2}{n_{p0}}$

Further for N-type, $n_{n_0} = N_D$, $p_{n0} = \frac{n_i^2}{N_D}$, $N_D = \frac{n_i^2}{p_{n0}}$

Therefore $E_0 = kT \ln\left[\frac{n_{n0}}{n_{p0}}\right]$ and $E_0 = kT \ln\left[\frac{P_{p0}}{p_{n0}}\right]$

Where the subscript '0' indicate that the above relations are obtained under thermal conditions of equilibrium.

3. What do you understand by depletion region at pn junction? What is the effect of forward and reverse biasing of pn junction on the depletion region? Explain with necessary diagrams.

Ans: Depletion region: In a PN junction p-type consists of holes and n-type consists of electrons. Due to diffusion, the large number of holes from p-side diffuse to n-side and similarly, the large number of electrons from n-side diffuse to p-side.

Due to this displacement, p-side looses holes and forms a negative electric field to the left side of junction and n-side looses electrons and forms a positive electric field to the right side of the junction. Because of this large movement of holes and electrons, a barrier potential is developed across the junction. Finally, the holes will combine with free electrons and gets disappear leaving negative potential at p-side near the junction. Similarly the free electrons will combine with holes and gets disappear leaving positive potential at n-side near the junction. This region at the junction is known as depletion region.

The thickness of depletion region is the order of few microns. Where, 1 micron=10^{-4}cm.

Forward bias:

In forward bias, the thickness of depletion layer is very thin because p-type is connected to positive terminal and the n-type is connected to the negative terminal. This causes the holes and electrons to move freely across the junction, hence resulting in a large current.

Reverse bias:

In reverse bias, as the p-type is connected to the negative terminal and n-type is connected to the positive terminal, the force of attraction takes place, so the holes from p-side and the electrons from n-side moves away from the junction, thus increasing the width of depletion region. This results in a very little current, almost equal to zero. Therefore, in reverse bias the thickness of the depletion region is large.

4. Explain about various current components in a forward biased pn junction diode.

Ans:

- When a p-n junction is forward biased a large forward current flows, which is mainly due to majority carriers. The depletion region near the junction is very very small, under forward biased condition.
- In forward biased condition holes get diffused into n side from p side while electrons get diffused into p-side from n side.
- So on p-side, the current carried by electrons which is diffusion current due to minority carriers, decreases exponentially with respect to distance measured from the junction. This current due to electrons, on p-side which are minority carriers is denoted as I_{np}.
- Similarly holes from p side diffuse into n-side carry current which decreases exponentially with respect to distance measured from the junction. This current due to holes on n-side, which are minority carriers is denoted as I_{pn}.

Fig: Current componets

- If distance is denoted by then,
  $I_{np}(x)$ = Current due to electrons in p side as a function of x
  $I_{pn}(x)$ = Current due to holes in n side as a function of x
- At the junction i.e. at x = 0, electrons crossing from n side to p side constitute a current, $I_{np}(0)$ in the same direction as holes crossing the junction from p side to n side constitute a current , $I_{pn}(0)$. Hence the current at the junction is the total conventional current I flowing through the circuit.

$\therefore \quad I = I_{pn}(0) + I_{np}(0)$

- But as the entire circuit is a series circuit, the total current must be maintained at I, independent of x. This indicates that on p side there exists one more current component which is due to holes on p side which are majority carriers. It is denoted by $I_{pp}(x)$.
  $I_{pp}(x)$ = current due to holes in p side
- Similarly on n side, there exists, there exists one more current component which is due to electrons on n side, which are the majority carriers. It is denoted by $I_{nn}(x)$.
  $I_{nn}(x)$ = Current due to electrons in n side.
- On p side the total current is $I = I_{pp}(x) + I_{np}(x)$
- On n side the total current is $I = I_{nn}(x) + I_{pn}(x)$

5. Define law of junction. Explain about the term cut-in voltage associated with pn junction diode. How do you obtain cut-in voltage from forward V-I characteristics?

Ans: Law of Junction: This law states that for a forward biased junction diode the injected hole concentration $p_n(0)$ in the n-region increases over thermal equilibrium value P_{n_0}. It is given by,

$$p_n(0) = p_{n_0} e^{\frac{V}{V_T}}$$

Similarly for electron concentration, $$n_p(0) = n_{p_0} e^{\frac{V}{V_T}}$$

Cut-in voltage V_γ is the minimum bias voltage that should be applied across a diode for conduction to take place. The amount of current below V_γ is very small and above V_γ the current raises rapidly. Typically values of V_γ for germanium and silicon diodes are 0.2 V and 0.6V respectively.

The forward V-I characteristics of a junction diode are shown below.

Cut-in voltage can be obtained from the V-I characteristics by selecting a point on voltage axis where the current raises rapidly.

6. Explain the volt-ampere characteristics of PN diode.

Ans:

Fig: V-I Characteristics of a Diode

- ***In forward characteristics***, it is seen that initially forward current is small as long as the bias voltage is less than the barrier potential.
- At a certain voltage close to barrier potential, current increases rapidly.
- The voltage at which diode current starts increasing rapidly is called as cut-in voltage. It is denoted by V_γ.
- Below this voltage, current is less than 1% of maximum rated value of diode current.
- The cut-in voltage for germanium is about 0.2V while for silicon it is 0.6V.
- ***In* reverse *characteristics*** , reverse current increases initially as reverse voltage is increased. But after a certain voltage, the current remains constant equal to reverse saturation current I_0.
- The voltage at which breakdown occurs is called reverse breakdown voltage denoted as V_{BR}.
- Reverse current before the breakdown is very small and can be neglected practically.
- It is important to note that the breakdown voltage is much higher and practically diodes are not operated in the breakdown condition.

7. Explain the temperature dependence of V-I characteristics.

Ans: Dependency on V-I characteristics on temperature

The generation of electron hole pairs in semiconductors is increased due to the rise in temperature and which further leads to increase in their conductivity. Thus, the variation of current through the pn junction diode with temperature can be obtained using diode current equation i.e.,

$$I = I_0\left[e^{(V/\eta V_T)} - 1\right]$$

Where, I = Diode current

I_0 = Diode reverse saturation current

V = External applied voltage to the diode

η = Constant = 1 for germanium

= 2 for silicon

V_T = Thermal voltage = $\frac{T}{11600}$

T = Temperature of diode junction(^oK)

For the diodes both germanium and silicon, the reverse saturation current I_0 increases approximately 7 percent/^oC. The reverse saturation current approximately doubles for every 10^oC rise in temperature. Since $(1.07)^{10} \approx 2$. Thus current I increases, if the temperature is increased at fixed voltage. By only reducing V, we can bring back current I to its original value. In order to maintain a constant current I value, the value of $\frac{dV}{dT}$ is found to be $-2.5mV/^oC$ at room temperature for either germanium or silicon.

Basically, the value of cut-in voltage(or barrier voltage) is about 0.3V for germanium and 0.7 V for silicon. For both germanium and silicon diodes, the barrier voltage is decreased by $2mV/^oC$. This is due to dependency of barrier voltage on temperature. Mathematically,

$$I_{02} = I_{01} \times 2^{(T_2 - T_1)/10}$$

Where, I_{01} – Saturation current of the diode at temperature, T_1

I_{02} – Saturation current of the diode at temperature, T_2.

The effect of increased temperature on the pn junction diode characteristic curve is shown in figure. The maximum limit of temperature upto which a germanium and silicon diodes can used are 75° and 175°C respectively.

8. Explain about static and dynamic resistance in pn diode.

Ana: DC or Static Resistance

- The application of a dc voltage to a circuit containing a semiconductor diode will result in an operating point on the characteristic curve that will not change with time. The resistance of the diode at the operating point can be found simply by finding the Corresponding levels of V_D and I_D as shown in Fig.(1) and applying the following Equation:

$$R_D = \frac{V_D}{I_D}$$

- The dc resistance levels at the knee and below will be greater than the resistance levels obtained for the vertical rise section of the characteristics. The resistance levels in the reverse-bias region will naturally be quite high. Since ohmmeters typically employ a relatively constant-current source, the resistance determined will be at a preset current level (typically, a few mill amperes).

Figure(1): Determining the dc resistance of a diode at a particular operating point.

AC or Dynamic Resistance

- It is obvious from above equation that the dc resistance of a diode is independent of the shape of the characteristic in the region surrounding the point of interest. If a sinusoidal rather than dc input is applied, the situation will change completely. The varying input will move the instantaneous operating point up and down a region of the characteristics and thus defines a specific change in current and voltage. With no applied varying signal, the point of operation would be the *Q*-point determined by the applied dc levels as shown in fig(2).

Figure(2): determining the ac resistance at a *Q*-point

- A straight line drawn tangent to the curve through the *Q*-point as shown in Fig. 2 will define a particular change in voltage and current that can be used to determine the *ac* or *dynamic* resistance for this region of the diode characteristics. In equation form,

$$r_D = \frac{\Delta V_D}{\Delta I_D}$$

9. Derive an expression for transition capacitance.

Ans: Transition capacitance:

- Consider a reverse biased p-n junction diode as shown in figure.

Fig: Transition capacitance in reverse biased condition

- When a diode is reversed biased, reverse current flows due to minority carriers.
- The width of the depletion region increases as reverse bias voltage increases.
- As the charged particles move away from the junction there exists a change in charge with respect to the applied reverse voltage.
- So change in charge dQ with respect to the change in voltage dV is nothing but a capacitive effect.
- Such a capacitance which into the picture under reverse biased condition is called *Transition capacitance or space charge capacitance* denoted as C_T.

$$C_T = \left|\frac{dQ}{dV}\right|$$

Where, dQ is the increases in charge caused by a change dV in voltage.

Derivation of expression for C_T

- Consider a p-n junction diode, the two sides of which are not equally doped.
- Assume that p-side is lightly doped and n side is heavily doped.
- As depletion region penetrates lightly doped side, the most of depletion region is on p-side as it is lightly doped as shown in fig.

Fig: Unequally doped p-n junction diode

- It can be further assumed that concentration of acceptor impurity on p-side (N_A) is much less than the concentration of donor impurity on n-side(N_D)
- Hence the width of depletion region on n-side is negligible small compared to width of depletion region on p-side.
- Hence the entire depletion region can be assumed to be on the p-side only
- The relationship between potential and charge density is given by poisson's equation,

$$\frac{d^2V}{dx^2} = \frac{qN_A}{\varepsilon} \qquad \cdots\cdots\cdots\cdots (1)$$

Where x = the distance measured from the junction

ε = the permittivity of the semiconductor

Integrating equation (1) w.r.to x we get,

$$\int \frac{d^2V}{dx^2} dx = \int \frac{qN_A}{\varepsilon} dx$$

$$\therefore \frac{dV}{dx} = \frac{qN_A}{\varepsilon} x \qquad \cdots\cdots\cdots\cdots (2)$$

Assume constant of integration as zero.

Now $\frac{dV}{dx}$ is the electric field intensity over the range 0 to w over which depletion region is spreaded.

To get the potential, integrating equation (2) we get,

$$\int \frac{dV}{dx} dx = \int_0^w \frac{qN_A}{\varepsilon} x \, dx$$

$$\therefore V = \frac{qN_A}{\varepsilon} \frac{w^2}{2} \qquad \cdots\cdots\cdots\cdots\cdots (3)$$

At $x = w, V_R = V_B$ which is barrier potential

Now barrier potential is the difference between internally developed junction potential

And externally applied bias voltage.

$$\therefore V_B = V_J - V$$

Where V_B is barrier potential and V must be taken as negative for reverse bias.

Substituting in equation (3) we get,

$$V_B = \frac{qN_A}{\varepsilon} \frac{w^2}{2} \qquad \cdots\cdots\cdots (4)$$

From the above expression it can be observed that $w \propto \sqrt{V_B}$

The width of barrier i.e depletion layer increases with applied reverse bias.

Differentiating equation (4) w.r.to V_R,

$$1 = \frac{1}{2} \frac{qN_A}{\varepsilon} \left[\frac{dw}{dV_R}\right] 2w$$

$$\frac{dw}{dV_R} = \frac{\varepsilon}{qN_A w} \qquad \cdots\cdots (5)$$

If A is the area of cross section of the junction, then net charge Q in the distance w is

$$Q = no.of\ charged\ particles \times charge\ on\ each\ particle$$

$$= [N_A \times Volume\ ]q$$

$$= N_A AWq \qquad \cdots\cdots (6)$$

Differentiating equation (6) w.r.to V_R,

$$\frac{dQ}{dV_R} = N_A\, Aq \frac{dW}{dV_R}$$

$$= N_A\, Aq \frac{\varepsilon}{qN_A W}$$

$$C_T = \frac{\varepsilon A}{W}$$

10. Derive an expression for diffusion capacitance.

Diffusion Capacitance:

- When a p-n junction is forward biased, the depletion layer almost completely disappears.
- The electrons move and stored in p-region and holes stored in n-region.
- As applied voltage increases, the amount of charge stored on both sides of junction also increases.
- It is observed that the charge stored varies directly as the applied forward bias voltage.
- This effect is similar to a capacitor in which amount of charge stored varies with applied voltage.

$$C_T = \frac{dQ}{dV} = \frac{Rate\ of\ change\ of\ charge\ at\ junction}{Rate\ of\ change\ of\ applied\ forward\ voltage}$$

- The flow of charge Q results in a diode current I is given by

$$I = \frac{Q}{\tau}$$

$$Q = I \times \tau \qquad \cdots\cdots (1)$$

Where τ is average life time of charge carrier

The diode current equation $I = I_0\left[e^{V/\eta V_T} - 1\right]$

The charge $Q = \left[I_0\left[e^{V/\eta V_T} - 1\right]\right]\tau$

Differentiating above equation with respect to V

$$\frac{dQ}{dV} = \frac{\tau I_0}{\eta V_T}\left[e^{V/\eta V_T}\right] \qquad \cdots\cdots\cdots\cdots\cdots (2)$$

From diode current equation $I = I_0 e^{V/\eta V_T} - I_0$

$$I + I_0 = I_0 e^{V/\eta V_T} \qquad \cdots\cdots\cdots (3)$$

Substitute equation (3) in equation (2)

$$\frac{dQ}{dV} = \frac{\tau}{\eta V_T}(I + I_0)$$

$$\frac{dQ}{dV} \approx \frac{\tau I}{\eta V_T} \qquad since\ I \gg I_0$$

Diffusion capacitance, $C_D = \frac{\tau I}{\eta V_T}$

11. Explain in brief about diode equivalent circuit.

Ans: An equivalent circuit is combination of elements, inserted in the place of a device without changing behavior of system.

Different equivalent circuit models of diode are given below.

- Piece wise linear model
- Simplified model
- Ideal Diode model

Piece wise linear model: Figure shows the V-I characteristics of a diode in piece wise linear model. The slope of straight line represents the reciprocal of a diode resistance, when the diode is ON. Whenever the voltage across the diode reaches V_γ then the diode will be ON.

Fig: V-I Characteristics and its Equivalent Circuit of Piece Wise Linear Model

Simplified model: If we consider above piece wise linear model, the resistance r_d is practically smaller. So by removing the r_d, we get the diode equivalent in simplified model.

Fig: V-I Characteristics and its Equivalent Circuit of Simplified Model

Ideal Diode model: An ideal diode is the first and simplest approximation of a real diode. It has no forward voltage drop, no reverse current, and no breakdown. In fact, an ideal diode is only a theoretical approximation of a real diode. However, in a well defined circuit, a real diode behaves almost like an ideal diode because forward voltage across the diode is small as compared to the input and output voltages.

Fig: V-I Characteristics and its Equivalent Circuit of ideal Diode

12. Explain about Diode switching characteristics (Diode switching times).

Ans: When the bias of a diode is changed from forward to reverse or vice versa, the current takes definite time to reach a steady state value.

1) **Forward recovery time (t_{fr}):** It is defined as the time taken for the diode response to reach 90% from 10% of the final value. But usually this is very small and so is not of much importance. This is show in fig (a).

Fig(a): Rise time

2) **Reverse recovery time (t_{rr}):** It is defined as the time taken by the diode to return to the reverse state when the forward bias is suddenly changed to reverse bias. It is given by the sum of storage time and transition time.
3) **Storage time(t_s)and Transition time(t_t):** Suppose the input given to the circuit show in figure b(i). During 0 – t_1, the diode is forward biased. Forward resistance of the diode is small compared to R_L. Since all the voltage drop is across R_L itself, the voltage drop across the diode is small.

$$\therefore I_F = \frac{V_F}{R_L}$$

This is shown in fig b(ii) and voltage across the diode b(iii) up to t_1. Now when the forward voltage is suddenly reversed , at $t = t_1$, because of the Reverse recovery time, the diode current will not fall suddenly. Instead, it reverses its direction and $\approx \frac{V_R}{R_L}$ (R_L is small compared to reverse resistance of the diode). At $t = t_2$ the equilibrium level of the carrier density at the junction takes place. So the voltage across the diode falls slightly but not reverse and increase to V_R after time t_3. The current also decreases and reaches a value = reverse saturation current I_0.

Fig (b): Storage and Transition times

The interval time ($t_1 - t_2$) for the stored minority charge to become zero is called ***Storage time (t_s)***. The time ($t_2 - t_3$) when the diode has normally recovered and the reverse current reaches I_0 value is called ***Transition time t_t***.

13. Draw the block diagram of RPS. What are the important characteristics of a Rectifier circuit?

Ans:

- For the operation of most of the electronics devices and circuits, a d.c. source is required. So it is advantageous to convert domestic a.c. supply into d.c. voltages.
- The process of converting a.c. voltage into d.c. voltage is called as rectification. This is achieved with i) Step-down Transformer, ii) Rectifier, iii) Filter and iv) Voltage regulator circuits.
- These elements constitute d.c. regulated power supply shown in the figure below.

Fig. Block diagram of Regulated D.C. Power Supply

Stepdown Transformer: It steps down the high voltage A.C mains to low voltage A.C

Bridge Rectifier: It converts A.C to D.C but the D.C output is varying.

Filter: It will smooth the D.C from varying greatly to a small ripple.

Regulator: It eliminates the ripple by setting D.C output to a fixed voltage.

Characteristics of a Rectifier circuit

- The most important consideration in designing a rectifier is the unidirectional output voltage. Rectifier enable minimum operable DC voltage at the rated current.
- The regulations of rectifier circuit are also good i.e.,0.1%.
- The rectifier is protected in the event of short circuit on the load side.
- Over voltage protection is incorporated.
- The response of rectifier to the temperature changes is minimum.
- Transient response of this rectifier circuit is faster i.e., in µsec.

14. Draw the circuit diagram of a FWR, a) With centre tap connection and

b) Bridge connection and explain its operation.

Ans: FWR with centre tap connection

- A full-wave rectifier converts an ac voltage into a pulsating dc voltage using both half cycles of the applied ac voltage. In order to rectify both the half cycles of ac input, two diodes are used in this circuit. The diodes feed a common load R_L with the help of a center-tap transformer.
- A center-tap transformer is the one which produces two sinusoidal waveforms of same magnitude and frequency but out of phase with respect to the ground in the secondary winding of the transformer. The full wave rectifier is shown in the figure below.

- The individual diode currents and the load current waveforms are shown in figure below:

Fig. The input voltage, the individual diode currents and the load current waveforms.

Operation:

- During positive half of the input signal, anode of diode D_1 becomes positive and at the same time the anode of diode D_2 becomes negative. Hence D_1 conducts and D_2 does not conduct. The load current flows through D_1 and the voltage drop across R_L will be equal to the input voltage.
- During the negative half cycle of the input, the anode of D_1 becomes negative and the anode of D_2 becomes positive. Hence, D_1 does not conduct and D_2 conducts. The load current flows through D_2 and the voltage drop across R_L will be equal to the input voltage.
- It is noted that the load current flows in the both the half cycles of ac voltage and in the same direction through the load resistance.

Bridge rectifier

- The full-wave rectifier circuit requires a center tapped transformer where only one half of the total ac voltage of the transformer secondary winding is utilized to convert into dc output. The need of the center tapped transformer in a Full-wave rectifier is eliminated in the bridge rectifier. The bridge rectifier circuit has four diodes connected to form a bridge. The ac input voltage us applied to diagonally opposite ends of the bridge. The load resistance is connected between the other two ends of the bridge. The bridge rectifier circuit and its waveforms are shown in figure.

Fig. Bridge rectifier circuit and waveforms

Operation:

- For the positive half cycle of the input ac voltage diodes D_1 and D_3 conduct, whereas diodes D_2 and D_4 do not conduct. The conducting diodes will be in series through the load resistance R_L, so the load current flows through the R_L.
- During the negative half cycle of the input ac voltage diodes D_2 and D_4 conduct, whereas diodes D_1 and D_3 do not conduct. The conducting diodes D_2 and D_4 will be in series through the load resistance R_L and the current flows through the R_L, in the same direction as in the previous half cycle. Thus a bidirectional wave is converted into a unidirectional wave.

15. Define the terms as referred to FWR circuit.
(i) PIV
(ii) Average DC voltage
(iii) RMS current
(iv) Ripple factor

Ans: (i) PIV: Peak Inverse Voltage is the maximum possible voltage across a diode when it is reverse biased. Consider that diode D_1 is in the forward biased i.e., conducting and diode D_2 is reverse biased i.e., non-conducting. In this case a voltage V_m is developed across the load resistor R_L. Now the voltage across diode D_2 is the sum of the voltages across load resistor R_L and voltage across the lower half of transformer secondary V_m. Hence PIV of diode $D_2 = V_m + V_m = 2V_m$. Similarly PIV of diode D_1 is $2V_m$.

(ii) Average DC voltage: The dc output voltage is given by

$$V_{dc} = I_{dc} R_L = \frac{2I_m R_L}{\pi}$$

$$\frac{2}{\pi} \times \frac{V_m R_L}{R_f + R_L}$$

If $R_L >> R_f$ then $V_{dc} = \frac{2V_m}{\pi}$

(iii) R.M.S current:

$$I_{dc} = \frac{V_{dc}}{R_L} = \frac{2V_m}{\pi R_L} = \frac{2I_m}{\pi}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

(iv) Ripple Factor (γ) : It is defined as ration of R.M.S. value of a.c. component to the d.c. component in the output is known as "Ripple Factor".

The ripple factor, γ is given by $\gamma = \sqrt{\left[\frac{I_{rms}}{I_{dc}}\right]^2 - 1}$ or $\gamma = \sqrt{\left[\frac{V_{rms}}{V_{dc}}\right]^2 - 1}$

$$\gamma = \sqrt{\left[\frac{I_m}{\sqrt{2}} \times \frac{\pi}{2I_m}\right]^2 - 1}$$

$$= \sqrt{\left[\frac{\pi}{2\sqrt{2}}\right]^2 - 1}$$

$$\gamma = 0.48$$

16. Derive the expression for the ripple factor of HWR and FWR.

Ans: Ripple Factor (γ) **:** It is defined as ration of R.M.S. value of a.c. component to the d.c. component in the output is known as "Ripple Factor".

$$\gamma = \frac{V'rms}{V_{dc}}$$

$$V'rms = \sqrt{V_{rms}^2 - V_{dc}^2}$$

$$\gamma = \sqrt{\left[\frac{V_{rms}}{V_{dc}}\right]^2 - 1}$$

For Half wave rectifier, ripple factor $\gamma = \sqrt{\left[\frac{I_{rms}}{I_{dc}}\right]^2 - 1}$ or $\gamma = \sqrt{\left[\frac{V_{rms}}{V_{dc}}\right]^2 - 1}$

$$= \sqrt{\left[\frac{I_m/2}{I_m/\pi}\right]^2 - 1}$$

$$= \sqrt{\left[\frac{\pi}{2}\right]^2 - 1}$$

$$= 1.21$$

For Full wave rectifier, ripple factor $\gamma = \sqrt{\left[\frac{I_{rms}}{I_{dc}}\right]^2 - 1}$ or $\gamma = \sqrt{\left[\frac{V_{rms}}{V_{dc}}\right]^2 - 1}$

$$\gamma = \sqrt{\left[\frac{I_m}{\sqrt{2}} \times \frac{\pi}{2I_m}\right]^2 - 1}$$

$$= \sqrt{\left[\frac{\pi}{2\sqrt{2}}\right]^2 - 1}$$

$$\gamma = 0.48$$

17. Compare Rectifier circuits:

Ans:

S.No.	Parameter	Half wave	Full Wave	Bridge
1	Number of Diodes	1	2	4
2	Average dc current, I_{dc}	$\frac{I_m}{\pi}$	$\frac{2I_m}{\pi}$	$\frac{2I_m}{\pi}$
3	Average dc voltage, V_{dc}	$\frac{V_{sm}}{\pi}$	$\frac{2V_{sm}}{\pi}$	$\frac{2V_{sm}}{\pi}$
4	RMS current, I_{rms}	$\frac{I_m}{2}$	$\frac{I_m}{\sqrt{2}}$	$\frac{I_m}{\sqrt{2}}$
5	DC Power output, P_{dc}	$\frac{I_m^2 R_L}{\pi^2}$	$\frac{4I_m^2 R_L}{\pi^2}$	$\frac{4I_m^2 R_L}{\pi^2}$
6	AC Power input, P_{ac}	$\frac{I_m^2(R_L + R_f + R_s)}{4}$	$\frac{I_m^2(R_L + R_f + R_s)}{2}$	$\frac{I_m^2(R_L + 2R_f + R_s)}{2}$
7	Max. rectifier efficiency (η)	40.6%	81.2%	81.2%
8	Ripple factor (γ)	1.21	0.482	0.482
9	PIV	V_m	$2V_m$	$2V_m$
10	TUF	0.287	0.693	0.812
11	Max. load current (I_m)	$\frac{V_{sm}}{R_L + R_f + R_s}$	$\frac{V_{sm}}{R_L + R_f + R_s}$	$\frac{V_{sm}}{R_L + 2R_f + R_s}$

18. Explain the principle of operation of HWR with and without capacitor input filter and the waveforms.

Ans: A Half – wave rectifier is one which converts a.c. voltage into a pulsating voltage using only one half cycle of the applied a.c. voltage. The basic half-wave diode rectifier circuit along with its input and output waveforms is shown in figure below.

Fig. HWR without capacitor filter

The half-wave rectifier circuit shown in above figure consists of a resistive load; a rectifying element i.e., p-n junction diode and the source of a.c. voltage, all connected is series. The a.c. voltage is applied to the rectifier circuit using step-down transformer. The input to the rectifier circuit, $V = V_m \sin\omega t$ Where V_m is the peak value of secondary a.c. voltage.

Operation:

- For the positive half-cycle of input a.c. voltage, the diode D is forward biased and hence it conducts. Now a current flows in the circuit and there is a voltage drop across R_L. The waveform of the diode current (or) load current is shown in figure.
- For the negative half-cycle of input, the diode D is reverse biased and hence it does not conduct. Now no current flows in the circuit i.e., i=0 and Vo=0. Thus for the negative half-cycle no power is delivered to the load.

HWR with capacitor input filter:

Fig. HWR with capacitor filter.

The filter uses a single capacitor connected in parallel with the load R_L. In order to minimize the ripple in the output, the capacitor C used in the filter circuit is quite large of the order of tens of microfarads. The operation of the capacitor filter depends upon the fact that the capacitor stores energy during the conduction period and delivers this energy to the load during non-conduction period.

Operation:

- During, the positive quarter cycle of the ac input signal, the diode D is forward biased and hence it conducts. This quickly charges the capacitor C to peak value of input voltage V_m. Practically the capacitor charge (V_m-V_γ) due to diode forward voltage drop.
- When the input starts decreasing below its peak value, the capacitor remains charged at V_m and the ideal diode gets reverse biased. This is because the capacitor voltage which is cathode voltage of diode becomes more positive than anode.
- Therefore, during the entire negative half cycle and some part of the next positive half cycle, capacitor discharges through R_L. The discharging of capacitor is decided by R_LC, time constant which is very large and hence the capacitor discharge very little from Vm.
- In the next positive half cycle, when the input signal becomes more than the capacitor voltage, he diode becomes forward biased and charges the capacitor C back to V_m. The output waveform is shown in figure below:

Fig. HWR output with capacitor filter.

- The discharging if the capacitor is from A to B, the diode remains non-conducting. The diode conducts only from B to C and the capacitor charges.

19. Derive the ripple factor of capacitor filter. (or) For a FWR with shunt capacitance filter derive expression for ripple factor using approximate analysis.

Fig. Full-wave rectifier with capacitor filter

Operation:

- During the positive quarter cycle of the ac input signal, the diode D_1 is forward biased, the capacitor C gets charges through forward bias diode D_1 to the peak value of input voltage Vm.
- In the next quarter cycle from $\frac{л}{2}$ to л the capacitor starts discharging through R_L, because once the capacitor gets charges to V_m, the diode D_1 gets reverse biased and stops conducting, so during the period from $\frac{л}{2}$ to л the capacitor C supplies the load current.
- In the next quarter half cycle, that is, л to $\frac{3л}{2}$ of the rectified output voltage, if the input voltage exceeds the capacitor voltage, making D_2 forward biased, this charges the capacitor back In the next quarter half cycle, that is, from $\frac{3л}{2}$ to 2л , the diode gets reverse biased and the capacitor supplies the load current.In FWR, as the time required by the capacitor to charge is very small and it discharges very little due to large time constant, hence ripple in the output gets reduced considerably.
- The output waveform is shown in figure below:

Fig. FWR output with capacitor filter.

Expression for Ripple factor:

Let, T = time period of the ac input voltage
T/2= half of the time period
T_1 = time for which diode is conducting
T_2 = time for which diode is non-conducting
During time T_1, capacitor gets charged and this process is quick. During time T_2, capacitor gets discharged through R_L. As time constant R_L C is very large, discharging process is very slow and hence $T_2 >> T_1$.
Let V_r be the peak to peak value of ripple voltage, which is assumed to be triangular as shown in the figure below:

Fig. Triangular approximation of ripple

It is known mathematically that the rms value of such a triangular waveform is,

$$V_{rms} = \frac{V_r}{2\sqrt{3}}$$

During the time interval T_2, the capacitor C is discharging through the load resistance R_L.
The charge lost is, $Q = CV_r$ But $i = \frac{dQ}{dt}$

$$\therefore\ Q = \int_0^{T_2} i dt = I_{DC}T_2$$

As integration gives average (or) dc value, hence $I_{dc} . T_2 = C . V_r$

$$\therefore V_r = \frac{I_{dc}T_2}{C} \quad \text{but } T_1+T_2 = T/2$$

Normally, $T_2 >> T_1$, $\therefore\ T_1+T_2 \approx T_1 = T/2$ where T=1/f

$$\therefore\ V_r = \frac{I_{dc}}{C}\left(\frac{T}{2}\right) = \frac{I_{dc}T}{2C} = \frac{I_{dc}}{2fC}$$

But $I_{DC} = \frac{V_{DC}}{R_L}$, $\quad \therefore\ V_r = \frac{V_{DC}}{2fCR_L}$ = peak to peak ripple voltage

$$\text{Ripple factor} = \frac{V_{rms}}{V_{Dc}} = \frac{\frac{V_{DC}}{2fCR_L}}{2\sqrt{3}} \times \frac{1}{V_{DC}} \qquad [\therefore V_{rms} = \frac{V_r}{2\sqrt{3}}]$$

$$\therefore\ \text{Ripple factor} = \frac{1}{4\sqrt{3}fCR_L}$$

20. Draw the circuit diagram of FWR with inductor filter and explain its operation.

Ans: Full-wave rectifier with series inductor filter:

A FWR with series inductor filter is shown in figure.

FIG. FWR with series inductor filter.

- In the positive half cycle of the secondary voltage of the transformer, the diode D_1 is forward biased. Hence the current flows through D_1, L & R_L.
- While in the negative half cycle, the diode D_1 is reverse biased while diode D_2 is forware biased. Hence the current flows through D_2, L & R_L. Hence we get unidirectional current through R_L.
- Due to inductor L , which opposes change in current , it tries to make the output smooth by opposing the ripple content in the output.
- In order to determine the ripple and its relation to 'L' the current flowing through the FWR is represented by fourier series form.
- Fourier series for the load current for FWR as,

$$i_L = I_m\left[\frac{2}{\pi} - \frac{4}{3\pi}\cos 2\omega t - \frac{4}{15\pi}\cos 4\omega t - - - -\right]$$

Neglecting higher order harmonics we get,

$$i_L = \frac{2I_m}{\pi} - \frac{4I_m}{3\pi}\cos 2\omega t \text{ ---------- } (1)$$

Neglecting diode forward resistance and the choke resistance and transformer secondary resistance, we can write the dc component of current as

$$I_{DC} = \frac{2I_m}{\pi} = \frac{2V_m}{\pi R_L} \text{ ---------- } (2)$$

While the second harmonic component represents ac component or ripple present and can be written as

$$I_m = \frac{V_m}{Z} \text{ ---------- } (3)$$

Where $Z = R_L + J\,2X_L = \sqrt{R_L^2 + (2\omega L)^2} = \sqrt{R_L^2 + 4\omega^2 L^2}$

$$I_m = \frac{V_m}{\sqrt{R_L^2 + 4\omega^2 L^2}} \text{ ---------- } (4)$$

Substitute equation (4) in equation (1)

$$i_L = \frac{2I_m}{\pi} - \frac{4V_m \cos(2\omega t - \varphi)}{3\pi\sqrt{R_L^2 + 4\omega^2 L^2}} \text{ ---------- } (5)$$

i.e i_L = dc component + ac component

where φ is the angle by which the load current lags behind the voltage.

Expression for the ripple factor

Ripple factor $\gamma = \frac{I_{rms}}{I_{DC}}$ ---------- (6)

Where $I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{4V_m}{3\sqrt{2}\pi\sqrt{R_L^2+4\omega^2L^2}}$ and $I_{DC} = \frac{2V_m}{\pi R_L}$

Substitute above two equations in equation (6)

$$\text{Ripple factor } \gamma = \frac{\frac{4V_m}{3\sqrt{2}\pi\sqrt{R_L^2+4\omega^2L^2}}}{\frac{2V_m}{\pi R_L}} = \frac{2}{3\sqrt{2}} \times \frac{1}{\sqrt{1+\frac{4\omega^2L^2}{R_L^2}}}$$

Initially on no load condition, $R_L \rightarrow \infty$ and hence $\frac{4\omega^2L^2}{R_L^2} \rightarrow 0$

$$\gamma = \frac{2}{3\sqrt{2}} = 0.472$$

This is very close to normal FWR without filtering. So neglecting 1 we get

$$\text{Ripple factor } \gamma = \frac{2}{3\sqrt{2}} \times \frac{1}{\sqrt{\frac{4\omega^2L^2}{R_L^2}}}$$

$$\text{For FWR } \gamma = \frac{R_L}{3\sqrt{2}\omega L}$$

So as load changes, ripple changes which is inversely proportional to the value of the inductor.

21.Derive the expression for ripple factor for FWR with L-section filter. Explain the necessity of a bleeder resistor.

Ans:

- In inductor filter the ripple factor is directly proportional to load resistance and in capacitor filter the ripple factor is indirectly proportional to load resistance.
- If we combine the above two filters, then the ripple factor becomes almost independent of load resistance.

R_X ⟶ dc winding resistance of the choke, R_B ⟶ Bleeder resistance

Ripple factor derivation

- The analysis of the LC filter circuit is based on the following assumptions.
- $X_L >> R_X$, $X_L >> X_C$, $R >> X_C$, $R >> R_X$. where $R = R_B \parallel R_L$.
- Since the filter elements, L & C are having resonable large values, the reactances X_L of the inductance L at 2ω i.e. $X_L = 2\omega L$ is much larger than R_X.
- Also the reactance X_L is much larger than the reactance of C, X_C at 2ω as $X_C = \frac{1}{2\omega C}$

- The input voltage e_{in} , to the LC filter is the output voltage of the FWR using fourier series, the input voltage "e_{in}" can be written as

$$e_{in} = V_m\left[\frac{2}{\pi} - \frac{4}{3\pi}\cos 2\omega t - \frac{4}{15\pi}\cos 4\omega t - - - -\right]$$

The first term $\frac{2V_m}{л}$ indicates the DC output voltage of the rectifier. Remaining terms indicate ripples.

$$e_{in} \approx V_m\left[\frac{2}{\pi} - \frac{4}{3\pi}\cos 2\omega t\right]$$

$$V_{DC} = \frac{2V_m}{л}$$

The impedance Z_2 of the filter circuit for 2nd harmonic component of input , i.e. at 2ω will be

$$Z_2 = R_X + 2J\omega L + \left[\frac{1}{2J\omega C} \| R\right]$$

As per assumptions $|Z_2| = 2\omega L$

Second harmonic component of the current in the filter circuit will be

$$I_{2m} = \frac{\frac{4V_m}{3л}}{Z_2} \approx \frac{\frac{4V_m}{3л}}{2\omega L}$$

The second harmonic voltage across the load is

$$V_{2m} = I_{2m}\frac{1}{2\omega C} = \frac{\frac{4V_m}{3л}}{2\omega L} \times \frac{1}{2\omega C} = \frac{V_m}{3\pi\omega^2 LC}$$

$$\therefore V_{2rms} = \frac{V_{2m}}{\sqrt{2}} = \frac{V_m}{3\sqrt{2}\pi\omega^2 LC}$$

Ripple factor $\gamma = \frac{V_{2rms}}{V_{DC}} = \frac{V_m}{3\sqrt{2}\pi\omega^2 LC} \times \frac{\pi}{2V_m}$

Ripple factor $\gamma = \frac{1}{6\sqrt{2}\omega^2 LC}$

It is seen that the ripple factor for LC filter does't depend upon the load resistance unlike the capacitor filtor.

The necessity of Bleeder Resistance R_B:

- The basic requirement of this filter circuit is that the current through the choke must be continuous and not interrupted.
- An interrupted current through the choke may develop a large back emf which may be in excess of PIV rating of the diodes and or maximum voltage rating of the capacitor.
- Thus this back emf is harmful to the diodes and capacitor.
- To eliminate the back emf developed across the choke, the current through it must be maintained continuous.
- This is assured by connecting a bleeder resistance, R_B across the output.

22. Derive the ripple factor of л-filter with neat sketch. (or) Discuss a FWR with л-filter.

Ans:

Fig. Π-section Filter.

- It consists of an inductance L with a dc winding resistance as R_x and two capacitors C1 and C2. The filter circuit is fed from full wave rectifier. Generally two capacitors are selected equal.
- The rectifier output is given to the capacitor C_1. This capacitor offers very low reactance to the ac component but blocks dc component.
- Hence capacitor C_1 bypasses most of the ac component. The dc component then reaches to the choke L.
- The choke L offers very high reactance to dc. So it blocks ac component and does not allow it to reach to load while it allows dc component to pass through it.
- The capacitor C_2 now allows to pass remaining ac component and almost pure dc component reaches to the load.
- The circuit looks like a л, hence called л-Filter.

The output voltage is given by

$$V_{DC} = V_m - \frac{V_r}{2} - I_{DC}R_X$$

where V_r = peak to peak ripple voltage

R_X = DC resistance of choke

Now $V_r = \frac{I_{DC}}{2fc}$ for full wave

Ripple factor $\gamma = \frac{\sqrt{2}\ X_{C1}X_{c2}}{X_L R_L} = \frac{\sqrt{2}\left(\frac{1}{2\omega C_1}\right)\left(\frac{1}{2\omega C_2}\right)}{(2\omega L)R_L}$

$$\gamma = \frac{\sqrt{2}}{8\omega^3 L C_1 C_2 R_L}$$

if C_1 & C_2 are expressed in μF and frequency f is assumed to be 50Hz, then we get

$$\gamma \approx \frac{5700}{LC_1C_2R_L}$$

23. why do we need filters in a power supply, under what condition we shall prefer a capacitor filter?

Ans: The circuit which can be used to minimize the undesirable A.C in the output of a rectifier and leaving only the DC component to appear at the output is known as filter. In power supplies, the output of rectifier contains both AC and DC components. Thus, filters are used to remove unwanted ripple contents from this pulsating DC to get pure DC voltage. Even though, the output of a filter is not exactly a constant DC level. Thus, the output of a filter must be fed to a regulator which gives steady DC output.

The capacitive filter is an inexpensive filter for light loads which is connected directly across the load. The main function of capacitor is to allow AC component and block the DC component. Even though, it is a simple circuit to obtain pure DC voltage, but is inefficient due to the following reasons,

- The ripple factor is dependent on the load resistance , R_L.
- The output obtained using capacitor filter is not smooth as desired.
- The values of capacitor or load resistance must be fairly large to obtain a ripple voltage triangular waveform.

24. Compare all the filter circuits from the point of view of ripple factor.

Ans.

Capacitor Filter	**Inductor Filter**	**L – section or LC Filter**	**CLC or л Filter**
1.The circuit arrangement for capacitor filter is shown in figure.	1.The circuit arrangement for Inductor filter is shown in figure.	1.The circuit arrangement for L-section filter is shown in figure.	1.The circuit arrangement for CLC filter is shown in figure.
2. The expression for ripple factor is, $\gamma = \frac{1}{4\sqrt{3}f_C R_L}$ for FWR	2. The expression for ripple factor is, $\gamma = \frac{R_L}{3\sqrt{2}\omega L}$	2. The expression for ripple factor is, $\gamma = \frac{1}{6\sqrt{2}\omega^2 LC}$	2. The expression for ripple factor is, $\gamma = \frac{\sqrt{2}}{8\omega^2 LC_1C_2R_L}$
3. This filter is operated at large values of C and R_L because the ripple factor is very small at these values.	3. This filter is operated at small values of R_L because it gives a very less ripple factor and requires very high values of L (for less ripple factor) which increases the cost.	3. This filter does not depend on the value of load resistance R_L, it only depends on L and C values which are preferred to be high values for low RF.	3. This filter depends on load resistance R_L. This filter is generally preferred to operate at very high values of L, C_1 & C_2 . R_L for small RF value.
4. The ripple voltage depends on load current i.e., load resistance resistance.	4. The ripple voltage depends on load current.	4. The ripple voltage is independent of the load current.	4. The ripple voltage depends on load current i.e., load resistance.

Problems:

Problem 1

The mobility of free electrons and holes in pure germanium are 3800 and 1800 cm^2 /V-s respectively. The corresponding values for pure silicon are 1300 and 500 cm^2/V-s, respectively. Determine the values of intrinsic conductivity for both germanium and silicon. Assume $n_i = 2.5 \times 10^{13}$ cm^{-3} for germanium and $n_i = 1.5 \times 10^{10}$ cm^{-3} for silicon at room temperature.

Solution: (i) The intrinsic conductivity for germanium,

$$\sigma_i = qn_i(\mu_n + \mu_p)$$
$$= (1.6 \times 10^{-19})\ (2.5 \times 10^{13})\ (3800 + 1800)$$
$$= 0.0224 \text{ S/cm}$$

(ii) The intrinsic conductivity for silicon,

$$\sigma_i = qn_i\ (\mu_n + \mu_p)$$
$$= (1.6 \times 10^{-19})\ (1.5 \times 10^{10})\ (1300 + 500)$$
$$= 4.32 \times 10^{-6} \text{ S/cm}$$

Problem 2

In a P-type semiconductor, the Fermi level is 0.3 eV above the valance band at a room temperature of 300 °K. Determine the new position of the Fermi level for temperatures of (a) 350 °K and (b) 400 °K.

The Fermi level in a P-type material is given by

$$E_F = E_V + kT \ln \frac{N_V}{N_A}$$

Therefore, $(E_F - E_V) = kT \ln \frac{N_V}{N_A}$

At $T = 300$ °K, $0.3 = 300\ k \ln \frac{N_V}{N_A}$

(a) At $T = 350$ °K, $(E_{F1} - E_V) = 350k \ln \frac{N_V}{N_A}$

Hence, from the above equation

$$\frac{E_{F1} - E_V}{0.3} = \frac{350}{300}$$

Therefore, $E_{F1} - E_V = \frac{350}{300} \times 0.3 = 0.35$ eV

(b) At $T = 400$ °K, $(E_{F2} - E_V) = 400\ k \ln \frac{N_V}{N_A}$

Hence, from the above equation,

$$\frac{E_{F2} - E_V}{0.3} = \frac{400}{300}$$

Therefore, $E_{F2} - E_V = \frac{400}{300} \times 0.3 = 0.4$ eV

Problem 3

Find the concentration (densities) of holes and electrons in N-type Silicon at 300 °K, if the conductivity is 300 S/cm. Also find these values for P-type silicon. Given that for Silicon at 300 °K, $n_i = 1.5 \times 10^{10}/\text{cm}^3$, $\mu_n = 1300\ \text{cm}^2/\text{V-s}$ and $\mu_p = 500\ \text{cm}^2/\text{V-s}$.

Solution: (a) *Concentration in N-type Silicon*

The conductivity of an N-type Silicon is $\sigma = q\, n\, \mu_n$

Concentration of electrons, $n = \dfrac{\sigma}{q\mu_n}$

$$= \frac{300}{(1.6 \times 10^{-19})(1300)} = 1.442 \times 10^{18}\ \text{cm}^{-3}$$

Hence concentration of holes, $p = \dfrac{n_i^2}{n} = \dfrac{(1.5 \times 10^{10})^2}{1.442 \times 10^{18}} = 1.56 \times 10^2\ \text{cm}^{-3}$

(b) *Concentration in P-type silicon*

The conductivity of a P-type Silicon is $\sigma = qp\mu_p$

Hence, concentration of holes $\quad p = \dfrac{\sigma}{q\mu_p}$

$$= \frac{300}{(1.6 \times 10^{-19})(500)} = 3.75 \times 10^{18}\ \text{cm}^{-3}$$

and concentration of electrons, $\quad n = \dfrac{n_i^2}{p} = \dfrac{(1.5 \times 10^{10})^2}{3.75 \times 10^{18}} = 0.6 \times 10^2\ \text{cm}^{-3}$

Problem 4

(a) The resistivities of the P-region and N-region of a germanium diode are 6 Ω-cm and 4Ω-cm, respectively. Calculate the contact potential V_o and potential energy barrier E_o. (b) If the doping densities of both P and N-regions are doubled, determine V_o and E_o. Given that $q = 1.6 \times 10^{-19}$ C, $n_i = 2.5 \times 10^{13}/\text{cm}^3$, $\mu_p = 1800\ \text{cm}^2/\text{V-s}$, $\mu n = 3800\ \text{cm}^2/\text{V-s}$ and $V_T = 0.026$ V at 300 °K.

Solution: (a)Resistivity, $\quad \rho = \dfrac{1}{\sigma} = \dfrac{1}{N_A\, q\, \mu_p}\ 6\,\Omega - \text{cm}$

Therefore, $\quad N_A = \dfrac{1}{6q\mu_p} = \dfrac{1}{6 \times 1.6 \times 10^{-19} \times 1800} = 0.579 \times 10^{15}/\text{cm}^3$

Similarly, $\quad N_D = \dfrac{1}{4q\mu_n} = \dfrac{1}{4 \times 1.6 \times 10^{-19} \times 3800} = 0.579 \times 10^{15}/\text{cm}^3$

Therefore, $\quad V_o = V_T \ln \dfrac{N_D N_A}{n_i^2} = 0.026 \ln \dfrac{0.579 \times 0.411 \times 10^{30}}{(2.5 \times 10^{13})^2} = 0.1545$ V

Hence $\quad E_0 = 0.1545$ eV

(b) $V_o = 0.026 \ln \dfrac{2 \times 0.579 \times 10^{15} \times 2 \times 0.411 \times 10^{15}}{(2.5 \times 10^{13})^2} = 0.1906$ V

Therefore, $\quad E_0 = 0.1906$ eV

Problem5.

In the case of an open circuited p-n junction, the acceptor atom concentration is $2.5\times10^{16}/m^3$, donor atom concentration is $2.5\times10^{22}/m^3$ and intrinsic concentration is $2.5\times10^{19}/m^3$. Determine the value of the contact difference of potential.

Sol: $N_A = 2.5 \times 10^{16}/m^3$

$N_D = 2.5 \times 10^{22}/m^3$

$n_i = 2.5 \times 10^{19}/m^3$

Contact potential $V_J = V_T \ln\left[\frac{N_A N_D}{n_i^2}\right]$

Assume $V_T = 26mV$

$$V_J = 26 \times 10^{-3} \ln\left[\frac{2.5\times10^{16}\times2.5\times10^{22}}{(2.5\times10^{19})^2}\right]$$

$$= 0V$$

Problem6.

A diode operating at 300K at a forward voltage of 0.4V carriers a current of 10mA. When voltage is changed to 0.42V the current becomes thrice. Calculate the value of reverse leakage current and η for the diode(assume V_T = 26 mV).

Sol: Given data:

$T = 300^0K$

$V_1 = 0.4V$

$I_1 = 10mA$

$V_2 = 0.42V$

$I_2 = 30\ mA$ *(given the current becomes thrice)*

$V_T = 26mV$

To find: $I_0 = ?$ $\eta = ?$

The expression for diode current is given by

$$I = I_0\left[e^{V/\eta V_T} - 1\right]$$

For $V_1 = 0.4V$, $I_1 = 10mA$ *and* $V_T = 26mV$, *we get,*

$$10 \times 10^{-3} = I_0\left[e^{0.4/\eta\times26\times10^{-3}} - 1\right]$$

$$= I_0\left[e^{\frac{400}{26\eta}} - 1\right] \qquad since \quad e^{\frac{400}{26\eta}} >> 1$$

$$10 \times 10^{-3} = I_0\, e^{\frac{400}{26\eta}} \qquad \cdots\cdots\cdots \quad (1)$$

For V_2= 0.42V, I_2 = 30mA and V_T = 26mV, we get,

$$30 \times 10^{-3} = I_0\left[e^{0.42/\eta \times 26 \times 10^{-3}} - 1\right]$$

$$= I_0\left[e^{\frac{420}{26\eta}} - 1\right] \qquad since \quad e^{\frac{400}{26\eta}} >> 1$$

$$30 \times 10^{-3} = I_0 e^{\frac{420}{26\eta}} \qquad \cdots\cdots\cdots \quad (2)$$

Dividing equation (2) with equation (1), we get,

$$\frac{30\times10^{-3}}{10\times10^{-3}} = \frac{I_0 e^{\frac{420}{26\eta}}}{I_0\, e^{\frac{400}{26\eta}}}$$

$$3 = e^{\frac{20}{26\eta}}$$

$$3 = e^{\frac{10}{13\eta}}$$

$$\frac{10}{13\eta} = ln3 = 1.099$$

$$\therefore \eta = 0.7$$

Then , substituting the above η value in equation (1), we get,

$$10 \times 10^{-3} = I_0\, e^{\frac{400}{26\times0.7}}$$

$$\therefore I_0 = 2.85\, pAms$$

Problem7.

A pn junction diode has a reverse saturation current of 30 µA at a temperature of 125^0 C. At the same temperature, find the dynamic resistance for 0.2 V bias in forward and reverse direction.

Sol: Given data:

$$I_0 = 30\mu A$$

$$T = 125^0 C$$

$$V_f = 0.2\ (forward\ bias)$$

$$-V_f = -0.2\ (reverse\ bias)$$

To find:

r_f =?

r_r =?

Consider **η** =2 for silicon

We know that, $V_T = \frac{T}{11600} = \frac{398}{11600} = 34.3 \times 10^{-3} V \quad [since\ T = 125 + 273 = 398^0 K]$

Forward dynamic resistance $r_f = \frac{\eta V_T}{I_0 e^{V/\eta V_T}} = \frac{2\times34.3\times10^{-3}}{30\times10^{-6}\times e^{\frac{0.2}{2\times34.3\times10^{-3}}}} = 123.9\Omega$

Reverse dynamic resistance $r_r = \frac{\eta V_T}{I_0 e^{-V/\eta V_T}} = \frac{2\times34.3\times10^{-3}}{30\times10^{-6}\times e^{\frac{-0.2}{2\times34.3\times10^{-3}}}} = 42.18K\Omega$

Problem8.

A diode whose internal resistance is 20Ω is to supply power to a 100Ω load from 110V(rms) source pf supply. Calculate (a) peak load current (b) the dc load current (c) the ac load current (d) the percentage regulation from no load to full load.

Sol: Given a half-wave rectifier circuit R_f=20Ω, R_L=100Ω

Given an ac source with rms voltage of 110V, therefore the maximum amplitude of sinusoidal input is given by

$$V_m = \sqrt{2} \times V_{rms} = \sqrt{2} \times 100 = 155.56\ V$$

(a) peak load current: $I_m = \frac{V_m}{R_f+R_L}$

$$I_m = \frac{155.56}{120} = 1.29\ A$$

(b) the dc load current: $I_{dc} = \frac{I_m}{л} = 0.41\ A$

(c) the ac load current: $I_{rms} = \frac{I_m}{2} = 0.645\ A$

(d) $\mathbf{V_{NL}} = \frac{V_m}{\pi} = \frac{155.56}{\pi} = 49.51V$

$\mathbf{V_{FL}} = \frac{V_m}{\pi} - I_{dc}R_f = 41.26V$

% Regulation $= \frac{V_{NL}-V_{FL}}{V_{FL}} \times 100 = 19.97\%$

Problem9.

An a.c. supply of 230V is applied to a half-wave rectifier circuit through transformer of turns ration 5:1. Assume the diode is an ideal one. The load resistance is 300Ω.

Find (a) dc output voltage (b) PIV (c) maximum, and (d) average values of power delivered to the load.

Sol:

a) The transformer secondary voltage = 230/5 = 46V.

Maximum value of secondary voltage, $V_m = \sqrt{2} \times 46 = 65V$.

dc voltage = $V_{DC} = \frac{V_m}{л} = \frac{65}{\pi} = 20.7V$

b) PIV of a diode = $V_m = 65V$

c) Maximum value of load current $I_m = \frac{V_m}{R_L} = \frac{65}{300} = 0.217A$

Therefore, maximum value of power delivered to the load

$$P_m = I_m^2 \times R_L = (0.217)^2 \times 300 = 14.1W$$

d) The value of load current $I_{dc} = \frac{V_{dc}}{R_L} = \frac{20.7}{300} = 0.069A$

Therefore average power delivered to the load $P_{dc} = I_{dc}^2 \times R_L = (0.069)^2 \times 300$
$= 1.43W$

Problem10.

A Full-wave rectifier circuit uses two silicon diodes with a forward resistance of 20Ω each. A dc voltmeter connected across the load of 1kΩ reads 55.4volts. Calculate

i) I_{RMS},

ii) Average voltage across each diode,

iii) Ripple factor, and

iv) Transformer secondary voltage rating.

Sol:

Given $R_f = 20\Omega$, $R_L = 1K\Omega$, $V_{dc} = 55.4V$

For a FWR $V_{DC} = \frac{2V_m}{л}$ $\therefore V_m = \frac{55.4 \times \pi}{2} = 86.9V$

$$I_m = \frac{V_m}{R_f + R_L} = 0.08519A$$

i) $I_{rms} = \frac{I_m}{\sqrt{2}} = 0.06024A$

ii) $V = \frac{86.9}{2} = 43.45V$

iii) Ripple factor = $\gamma = \sqrt{\left[\frac{I_{rms}}{I_{dc}}\right]^2 - 1}$

$$I_{DC} = \frac{2I_m}{л} = 0.05423A$$

$$I_{rms} = \frac{I_m}{\sqrt{2}} = 0.06024A$$

$$\gamma = 0.48$$

iv) Transformer secondary voltage rating

$$V_{rms} = \frac{V_m}{\sqrt{2}} = \frac{86.9}{\sqrt{2}} = 61.49V$$

Problem11.

A 230V, 60Hz voltage is applied to the primary of a 5:1 step down, center tapped transformer used in the Full-wave rectifier having a load of 900Ω. If the diode resistance and the secondary coil resistance together has a resistance of 100Ω.

Determine:

i) dc voltage across the load,

ii) dc current flowing through the load,

iii) dc power delivered to the load, and

iv) ripple voltage and its frequency.

Sol: Given $V_{p(rms)} = 230V$

$$\frac{N_2}{N_1} = \frac{2V_{s(rms)}}{V_{p(rms)}}$$

$$\frac{1}{5} = \frac{2V_{s(rms)}}{230}$$

$$V_{s(rms)} = 23V(each\ half)$$

Given $R_L = 900\Omega$, $R_f + R_s = 100\Omega$

$$I_m = \frac{V_{sm}}{R_f+R_s+R_L} = \frac{\sqrt{2}\,V_{s(rms)}}{R_f+R_s+R_L} = \frac{\sqrt{2}\times 23}{900+100} = 0.03252A$$

$$I_{dc} = \frac{2I_m}{\pi} = \frac{2\times 0.03252}{\pi} = 0.0207A$$

i) $V_{dc} = I_{dc}R_L = 18.6365V$

ii) $I_{dc} = 0.0207V$

iii) $P_{dc} = I_{dc}^2 R_L\ or\ V_{dc}I_{dc} = 0.3857\ W$

iv) $PIV = 2V_{sm} = 65.0538V$

v) $Ripple\ factor = \frac{V_{r(rms)}}{V_{dc}} = 0.482$

$$Ripple\ Voltage = V_{r(rms)} = 0.482 \times 18.6365 = 8.9827V$$

Frequency of ripple=2f =2×60 = 120 Hz.

Problem12.

In a bridge rectifier the transformer is connected to 220V, 60Hz mains and the turns ratio of the step down transformer is 11:1. Assuming the diode to be ideal, find:

i) Idc

ii) voltage across the load

iii) PIV assume load resistance to be 1kΩ

Sol: $\frac{N_2}{N_1} = \frac{1}{11} = \frac{V_{s(rms)}}{220}$

$$V_{s(rms)} = \frac{220}{11} = 20V$$

$$V_{sm} = \sqrt{2}\ V_{s(rms)} = 28.2842V$$

i) $I_m = \frac{V_{sm}}{R_L} = \frac{28.2842}{1\times 10^3} = 28.2842mA$

$$\therefore I_{dc} = \frac{2I_m}{\pi} = 18mA$$

ii) $V_{dc} = I_{dc}R_L = 18 \times 10^{-3} \times 1 \times 10^3 = 18V$

iii) $PIV = V_{sm} = 28.2842V$

Problem13.

A 15-0-15 V (rms) ideal transformer is used with a full wave rectifier circuit with diodes having forward drop of 1V. The load is a resistance of 100Ω and a capacitor of 10000μF is used as a filter across the load resistance. Calculate the dc load current and the voltage.

Sol: $V_m = \sqrt{2}\, V_{s(rms)} = \sqrt{2} \times 15 = 21.2132V$

$R_L = 100\Omega, \quad diode\ drop = V_D = 1V, \quad C = 10000\mu F.$

$I_m = \frac{V_m - V_D}{R_L} = \frac{21.2132-1}{100} = 0.20213A$

$\therefore I_{rms} = \sqrt{2}\, I_m = 0.2858A$

$\therefore I_{dc} = \frac{2I_m}{\pi} = 0.1286A$

$V_{dc} = V_m - I_{dc}\left[\frac{1}{4fc}\right] - V_D = 20.1489V$

Problem14.

In a FWR circuit using an LC filter, L=10H, C=100μF and R_L=500Ω. Calculate I_{dc} , V_{dc} , ripple factor for an input of $v_i = 30\sin(100\pi t)V$.

Sol: $v_i = V_m \sin \omega t$

$V_{sm} = V_m = 30\ V$

$V_{dc} = \frac{2V_m}{\pi} = \frac{2\times 30}{\pi} = 19.0985V$

$I_{dc} = \frac{V_{dc}}{R_L} = \frac{19.0985}{500} = 38.19mA$

Ripple factor $\gamma = \frac{1}{6\sqrt{2}\omega^2 LC}$ $\quad where\ \omega = 100\pi$

$\gamma = 1.194 \times 10^{-3}$

BIPOLAR JUNCTION TRANSISTOR

1 Define a Transistor. Why transistor is considered as current control device? Explain.

Ans:

- Transistor means Transfer Resistor i.e., signals are transferred from low resistance circuit into high resistance circuit.
- It is a three terminal semiconductor device : Base, Emitter & Collector.
- It can be operated in three configurations: CB, CE & CC. According to configuration it can be used for voltage as well as current amplification.
- Basically, it is referred as Bipolar Junction Transistor (BJT), because the operation of transistor depends on the interaction of both majority and minority carriers.
- A BJT is formed by placing a P-type silicon layer in between two n-type semiconducting materials or by placing a n-type silicon layer in between two p-type semiconducting materials.

- The emitter terminal is heavily doped so that a large number of charge carriers are injected into the base.
- The base is very lightly doped and is very thin. It allows most of the charge carriers from emitter region to the collector region.
- The collector is moderately doped. Its main function is to collect the majority charge carriers coming from the emitter and passing through the base.

Why transistor is considered as current control device?

- Transistor is also called as current control device, since the output current is controlled by the input current.
- In order to realize such a device, we require a forward biased diode at the input port and a reverse biased diode at the output port.
- Also the reverse current of the output diode must be controlled by the forward current of the input diode.
- Since in the transistor we have two junctions in which one junction is forward biased and other junction is reverse biased.

- The forward biased junction injects holes from the p-side (if it is a PNP transistor) called emitter into the n-region called base which is taken as reference electrode. The reverse biased pn junction produces a minority carrier drift current and the output p-region which collects this current is called the collector.

- The emitter current injected into the base increases the minority carrier density in the base and augments the reverse minority carrier drift current flowing in the collector circuit.
- Thus the input emitter current controls the output collector current and the transistor behaves as a current controlled source or simply current control device.

2. With neat diagrams explain the working of npn and pnp transistor.
Ans: Working of a n-p-n transistor:

- The n-p-n transistor with base to emitter junction forward biased and collector base junction reverse biased is as shown in figure.
- As the base to emitter junction is forward biased the majority carriers emitted by the n-type emitter i.e., electrons have a tendency to flow towards the base which constitutes the emitter current I_E.
- As the base is p-type there is chance of recombination of electrons emitted by the emitter with the holes in the p-type base. But as the base is very thin and lightly doped only few electrons emitted by the n-type emitter less than 5% combines with the holes in the p-type base, the remaining more than 95% electrons emitted by the n-type emitter cross over into the collector region constitute the collector current.
  The current distributions are as shown in fig. $\mathbf{I_E = I_B + I_C}$

Working of a p-n-p transistor:

- The p-n-p transistor with base to emitter junction is forward biased and collector to base junction reverse biased is as show in figure.
- As the base to emitter junction is forward biased the majority carriers emitted by the p type emitter i.e., holes have a tendency to flow towards the base which constitutes the emitter current I_E.
- As the base is n-type there is a chance of recombination of holes emitted by the emitter with the electrons in the n-type base. But as the base us very thin and lightly doped only few electrons less than 5% combine with the holes emitted by the p-type emitter, the remaining 95% charge carriers cross over into the collector region to constitute the collector current.

  The current distributions are shown in figure. $\mathbf{I_E = I_B + I_C}$

3. Write short notes on emitter efficiency, Transport factor and large signal current gain.

Ans: Current components in a transistor:

- The figure below shows the various current components which flow across the forward biased emitter junction and reverse-biased collector junction in P-N-P transistor.

Figure. Current components in a transistor (PNP)

- The emitter current consists of the following two parts:

  1) Hole current I_{pE} constituted by holes (holes crossing from emitter into base).

  2) Electron current I_{nE} constituted by electrons (electrons crossing from base into the emitter).

  Therefore, Total emitter current $I_E = I_{pE}$ (majority)+ I_{nE} (Minority)

- The holes crossing the emitter base junction J_E and reaching the collector base junction J_C constitutes collector current I_{pC}. Not all the holes crossing the emitter base junction J_E reach collector base junction J_C because some of them combine with the electrons in the n-type base.
- Since base width is very small, most of the holes cross the collector base junction J_C and very few recombine, constituting the base current ($I_{pE} - I_{pC}$).
- When the emitter is open-circuited, I_E=0, and hence I_{pC}=0. Under this condition, the base and collector together current I_C equals the reverse saturation current I_{CO}, which consists of the following two parts: I_{PCO} caused by holes moving across I_C from N-region to P-region. In I_{nCO} caused by electrons moving across I_C from P-region to N-region. I_{CO} = I_{nCO} + I_{pCO}. In general, $I_C = I_{nC} + I_{pC}$. Thus for a P-N-P transistor, $\mathbf{I_E = I_B + I_C}$

1) **Emitter efficiency (γ) :** It is the ratio of current of injected carriers at emitter base junction to total emitter current.

$$\gamma = \frac{\text{current of injected carriers at } J_E}{\text{total emitter current}}$$

In case of pnp transistor, $\gamma = \frac{I_{pE}}{I_{pE}+I_{nE}} = \frac{I_{pE}}{I_E}$

In case of npn transistor, $\gamma = \frac{I_{nE}}{I_{pE}+I_{nE}} = \frac{I_{nE}}{I_E}$

Where, I_{pE} = Injected hole diffusion current at emitter junction.
I_{nE} = Injected electron diffusion current at emitter junction.

2) **Transport factor (β^*) :** It is the ratio of injected carrier current reaching at collector base junction J_C to injected carrier current at emitter base junction J_E.

$$\beta^* = \frac{\text{Injected carrier current reaching } J_C}{\text{Injected carrier current at } J_E}$$

In case of pnp transistor, $\beta^* = \frac{I_{pC}}{I_{pE}}$

In case of pnp transistor, $\beta^* = \frac{I_{nC}}{I_{nE}}$

3) **Large signal current gain(α) :** It is the ratio of the current due to injected carriers I_{pC} to the total emitter current I_E.

$$\alpha = \frac{I_{pC}}{I_E} = \frac{I_C - I_{co}}{I_E}$$

$$I_C = \alpha I_E + I_{CO}$$

4) **Relation between α, β & γ:** Multiplying and dividing equation $\alpha = \frac{I_{pC}}{I_E}$ with I_{pE} ,

$$\alpha = \frac{I_{pC}}{I_{pE}} \times \frac{I_{pE}}{I_E}$$

$$\alpha = \beta^* \gamma$$

4. What are the different configurations of BJT? Explain.

Ans: Transistor circuit configurations:

- Following are the three types of transistor circuit configurations:
  1) Common-Base (CB)
  2) Common-Emitter (CE)
  3) Common-Collector (CC)

- Here the term 'Common' is used to denote the transistor lead which is common to the input and output circuits. The common terminal is generally grounded.

Common Base (CB) Configuration:

- In this configuration input is applied between emitter and base and output is taken from the collector and base.
- Here, base of the transistor is common to both input and output circuits and hence the name common base configuration.

Here, $I_C = \alpha I_E + I_{CBO}$

Where I_{CBO} is reverse saturation current and it doubles for every 10^0 C rise in temperature. It is negligible small in most practical situations, we can approximately write:

$$I_C = \alpha I_E$$

$\alpha = \frac{I_C}{I_E}$ this is current amplification factor in CB configuration.

For a transistor, $I_E = I_B + I_C$

$$= I_B + \alpha I_E$$

$$I_B = I_E - \alpha I_E$$

$$I_B = I_E[1 - \alpha]$$

Common Emitter (CE) Configuration:

- In this configuration input is applied between base and emitter and output is taken from the collector and emitter.
- Here, emitter of the transistor is common to both input and output circuits and hence the name common emitter configuration.

We have seen $I_C = \alpha I_E + I_{CBO}$

$$I_C - I_{CBO} = \alpha I_E$$

Dividing by α $\frac{I_C}{\alpha} - \frac{I_{CBO}}{\alpha} = I_E$ since $I_E = I_B + I_C$

$$\frac{I_C}{\alpha} - \frac{I_{CBO}}{\alpha} = I_B + I_C$$

$$\frac{I_C}{\alpha} - I_C = I_B + \frac{I_{CBO}}{\alpha}$$

$$I_C\left[\frac{1}{\alpha} - 1\right] = I_B + \frac{I_{CBO}}{\alpha}$$

$$I_C\left[\frac{1-\alpha}{\alpha}\right] = I_B + \frac{I_{CBO}}{\alpha}$$

$$I_C = \left[\frac{\alpha}{1-\alpha}\right] I_B + \left[\frac{1}{1-\alpha}\right] I_{CBO}$$

Now we define new parameter $\beta = \frac{\alpha}{1-\alpha}$

β is always greater than 1

$I_C = \beta I_B + [1+\beta] I_{CBO}$ since $1 + \beta = \frac{1}{1-\alpha}$

The term $[1+\beta] I_{CBO}$ is the reverse leakage current in CE configuration. It is also defined as I_{CEO}

$$I_C = \beta I_B + I_{CEO}$$

Where I_{CEO} is collector emitter current when base is open. It is neglected in practical circuits.

$$I_C = \beta I_B$$

$\beta = \frac{I_C}{I_B}$ this is current amplification factor in CE configuration.

Common Collector (CC) Configuration:

- In this configuration input is applied between base and Collector and output is taken from the emitter and collector.
- Here, Collector of the transistor is common to both input and output circuits and hence the name common Collector configuration.

- The current gain of the circuit is defined as the ratio of output current to (I_E) to input current (I_B). It is designated as γ.

$$\gamma = \frac{I_E}{I_B} = \frac{I_E}{I_C} \times \frac{I_C}{I_B} = \frac{1}{\alpha}\beta$$

$$\gamma = \frac{I_E}{I_B} = \frac{\beta}{\alpha} = \frac{\beta}{\frac{\beta}{(1+\beta)}} = (1+\beta)$$

$$\therefore \quad \gamma = \frac{1}{1-\alpha} = 1 + \beta$$

It means that output current is (1+β) times the input current.

5. With necessary diagram explain the input and output characteristics of CE configuration.

Ans: Characteristics of Common-Emitter Circuit:

The circuit diagram for determining the static characteristic curves of the an N-P-N transistor in the common emitter configuration is shown in figure below.

Fig. Circuit to determine CE Static characteristics.

Input Characteristics:

- To determine the input characteristics, the collector to emitter voltage is kept constant at zero volts and base current is increased from zero in equal steps by increasing V_{BE} in the circuit.
- The value of V_{BE} is noted for each setting of I_B. This procedure is repeated for higher fixed values of V_{CE}, and the curves of I_B versus V_{BE} are drawn.
- The input characteristics thus obtained are shown in figure below.

Fig. CE Input Characteristics.

- When V_{CE}=0 , the emitter-base junction is forward biased and the junction behaves as a forward biased diode.
- When V_{CE} is increased, the width of the depletion region at the reverse biased collector-base junction will increase. Hence he effective width of the base will decrease. This effect causes a decrease in the base current I_B. Hence, to get the same value of I_B as that for V_{CE}=0, V_{BE} should be increased. Therefore, the curve shifts to the right as V_{CE} increases.

Output Characteristics:

- To determine the output characteristics, the base current I_B is kept constant at a suitable value by adjusting base-emitter voltage, V_{BE}. The magnitude of collector-emitter voltage V_{CE} is increased in suitable equal steps from zero and the collector current I_C is noted for each setting of V_{CE}.
- Now the curves of I_C versus V_{CE} are plotted for different constant values of I_B.
- The output characteristics thus obtained are shown in figure below.

Fig. CE Output characteristics

The output characteristics of common emitter configuration consist of three regions: Active, Saturation and Cut-off regions.

Active Region: The region where the curves are approximately horizontal is the "Active" region of the CE configuration. In the active region, the collector junction is reverse biased. As V_{CE} is increased, reverse bias increase. This causes depletion region to spread more in base than in collector, reducing the changes of recombination in the base. This increase the value of α_{dc} .

This Early effect causes collector current to rise more sharply with increasing V_{CE} in the active region of output characteristics of CE transistor.

Saturation Region: If V_{CE} is reduced to a small value such as 0.2V, then collector-base junction becomes forward biased, since the emitter-base junction is already forward biased by 0.7V. The input junction in CE configuration is base to emitter junction, which is always forward biased to operate transistor in active region. Thus input characteristics of CE configuration are similar to forward characteristics of p-n junction diode. When both the junctions are forwards

biased, the transistor operates in the saturation region, which is indicated on the output characteristics. The saturation value of V_{CE}, designated $V_{CE}(Sat)$, usually ranges between 0.1V to 0.3V.

Cut-Off Region: When the input base current is made equal to zero, the collector current is the reverse leakage current I_{CEO}. Accordingly, in order to cut off the transistor, it is not enough to reduce I_B=0. Instead, it is necessary to reverse bias the emitter junction slightly. We shall define cut off as the condition where the collector current is equal to the reverse saturation current I_{CO} and the emitter current is zero.

Transistor Parameters:

The slope of the CE characteristics will give the following four transistor parameters. Since these parameters have different dimensions, they are commonly known as Common emitter **hybrid parameters (or) h-parameters.**

i) Input Impedance (h_{ie}):

It is defined as the ratio of change in (input) base voltage to the change in (input) base current with the (output) collector voltage (V_{CE}), kept constant. Therefore,

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B} \ , \ V_{CE}\ constant$$

It is the slope of CB input characteristics I_B versus V_{BE}. The typical value of h_{ie} ranges from 500Ω to 2000Ω.

ii) Output Admittance (hoe):

It is defined as the ratio of change in the (output) collector current to the corresponding change in the (output) collector voltage. With the (input) base current I_B kept constant. Therefore,

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}} \ , \ I_B\ constant$$

It is the slope of CE output characteristics I_C versus V_{CE}.

The typical value of this parameter is of the order of 0.1 to 10μ mhos.

iii) Forward Current Gain (h_{fe}):

It is defined as a ratio of the change in the (output) collector current to the corresponding change in the (input) base current keeping the (output) collector voltage V_{CE} constant. Hence,

$$h_{fe} = \frac{\Delta I_C}{\Delta I_B} \ , \ V_{CE}\ constant$$

It is the slope of I_C versus I_B curve.

Its typical value varies from 20 to 200.

iv) Reverse Voltage Gain (h_{re}):

It is defined as a ratio of the change in the (input) base voltage and the corresponding change in (output) collector voltage with constant (input) base current, I_B.

Hence,

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}} \ , \ I_E\ constant$$

It is the slope of V_{BE} versus V_{CE} curve.

Its typical value is of the order of $10^{-5}\ to\ 10^{-4}$

6 With necessary diagram explain the input and output characteristics of CB configuration.

Ans: The circuit diagram for determining the static characteristic curves of an NPN transistor in the common base configuration is shown in fig. below.

Fig. Circuit to determine CB static characteristics.

Input Characteristics:

To determine the input characteristics, the collector-base voltage V_{CB} is kept constant at zero volts and the emitter current I_E is increased from zero in suitable equal steps by increasing V_{EB}. This is repeated for higher fixed values of V_{CB}. A curve is drawn between emitter current I_E and emitter-base voltage V_{EB} at constant collector-base voltage V_{CB}.

The input characteristics thus obtained are shown in figure below.

Fig. CB Input characteristics.

Early effect (or) Base – Width modulation:

As the collector voltage V_{CC} is made to increase the reverse bias, the space charge width between collector and base tends to increase, with the result that the effective width of the base decreases. This dependency of base-width on collector-to-emitter voltage is known as Early effect (or) Base-Width modulation.

Thus decrease in effective base width has following consequences:

- Due to Early effect, the base width reduces, there is a less chance of recombination of holes with electrons in base region and hence base current I_B decreases.
- As I_B decreases, the collector current I_C increases.
- As base width reduces the emitter current I_E increases for small emitter to base voltage.
- As collector current increases, common base current gain (α) increases.

Punch Through (or) Reach Through:

When reverse bias voltage increases more, the depletion region moves towards emitter junction and effective base width reduces to zero. This causes breakdown in the transistor. This condition is called "Punch Through" condition.

Output Characteristics:

To determine the output characteristics, the emitter current I_E is kept constant at a suitable value by adjusting the emitter-base voltage V_{EB}. Then V_{CB} is increased in suitable equal steps and the collector current I_C is noted for each value of I_E. Now the curves of I_C versus V_{CB} are plotted for constant values of I_E and the output characteristics thus obtained is shown in figure below.

Fig. CB Output characteristics

From the characteristics, it is seen that for a constant value of I_E, I_C is independent of V_{CB} and the curves are parallel to the axis of V_{CB}. Further, I_C flows even when V_{CB} is equal to zero. As the emitter-base junction is forward biased, the majority carriers, i.e., electrons, from the emitter are injected into the base region. Due to the action of the internal potential barrier at the reverse biased collector-base junction, they flow to the collector region and give rise to I_C even when V_{CB} is equal to zero.

Transistor Parameters:

The slope of the CB characteristics will give the following four transistor parameters. Since these parameters have different dimensions, they are commonly known as common base hybrid parameters (or) h-parameters.

i) Input Impedance (h_{ib}):

It is defined as the ratio of change in (input) emitter to base voltage to the change in (input) emitter current with the (output) collector to base voltage kept constant.

Therefore, $h_{ib} = \frac{\Delta V_{EB}}{\Delta I_E}, V_{CB}\ constant$

It is the slope of CB input characteristics curve.

The typical value of h_{ib} ranges from 20Ω to 50Ω.

ii) Output Admittance (h_{ob}):

It is defined as the ratio of change in the (output) collector current to the corresponding change in the (output) collector-base voltage, keeping the (input) emitter current I_E constant.

Therefore, $h_{ob} = \frac{\Delta I_C}{\Delta V_{CB}}, I_E\ constant$

It is the slope of CB output characteristics I_C versus V_{CB}.
The typical value of this parameter is of the order of 0.1 to 10μmhos.

iii) Forward Current Gain (h_{fb}):

It is defined as a ratio of the change in the (output) collector current to the corresponding change in the (input) emitter current keeping the (output) collector voltage V_{CB} constant.

Hence, $h_{fb} = \frac{\Delta I_C}{\Delta I_E}$, V_{CB} *constant*

It is the slope of I_C versus I_E curve. Its typical value varies from 0.9 to 1.0.

iv) Reverse Voltage Gain (h_{rb}):

It is defined as a ratio of the change in the (input) emitter voltage and the corresponding change in (output) collector voltage with constant (input) emitter current, I_E.

Hence, $h_{rb} = \frac{\Delta V_{EB}}{\Delta V_{CB}}$, I_E *constant*

It is the slope of V_{EB} versus V_{CB} curve. Its typical value is of the order of 10^{-5} to 10^{-4}

7. With necessary diagram explain the input and output characteristics of CC configuration.

Ans: Characteristics of common collector circuit:

The circuit diagram for determining the static characteristics of an N-P-N transistor in the common collector configuration is shown in fig. below.

Fig. Circuit to determine CC static characteristics.

Input Characteristics:

To determine the input characteristic, V_{EC} is kept at a suitable fixed value. The base collector voltage V_{BC} is increased in equal steps and the corresponding increase in I_B is noted. This is repeated for different fixed values of V_{EC}. Plots of V_{BC} versus I_B for different values of V_{EC} shown in figure are the input characteristics.

Fig. CC Input Characteristics.

Output Characteristics:

The output characteristics shown in figure below are the same as those of the common emitter configuration.

Fig. CC output characteristics.

8. Summarize the salient features of the characteristics of BJT operating in CE,CB and CC configurations.

Property	CB	CE	CC
Input Resistance	Low (About 100Ω)	Moderate (About 750Ω)	High (About 750kΩ)
Output Resistance	High (About 450kΩ)	Moderate (About 45kΩ)	Low (About 25Ω)
Current Gain	1	High	High
Voltage Gain	About 150	About 500	Less than 1
Phase Shift between input and output voltages	0° (or) 360°	180°	0° (or) 360°
Applications	For high frequency circuits	For Audio frequency circuits	For impedance matching

10 What is early effect? How does it modify the V-I characteristics of a BJT?

Ans: when the transistor is operated in active region the emitter junction is forward biased and collector junction is reverse biased. Thus the barrier width at emitter junction is negligible when compared with the space charge width W at collector junction.

The transition region at a junction is the region of uncovered charges on both sides of the junction at the positions occupied by the impurity atoms. As the voltage applied across the junction increases, the transition region penetrates deeper into the collector and base. Because neutrality of charge must be maintained, the number of uncovered charges on each side remains equal. Since the doping in the base is substantially smaller than that of the collector, the penetration of the transition region into the base is much larger than into the collector. Hence, the collector depletion region is neglected and all the immobile charges are indicated in the base region.

If the metallurgical base width is W_B, then the effective electrical base width is $W'_B = W_B - W$. Thus, the modulation the effective base width by the collector voltage is known as the Early effect. The decrease in W'_B with increasing reverse collector voltage has three consequences. Firstly, there is less chance for recombination within the base region. Hence α increases with increasing $|V_{CB}|$. Secondly, the concentration gradient of minority carriers p_n is increased within the base. Finally, for extremely large voltages, W'_B may be reduced to zero, causing voltage breakdown in the transistor.

11. How Transistor acts as an amplifier

Ans.

- A load resistor R_L is connected in series with the collector supply voltage V_{CC} of CB transistor configuration as shown in figure.

CB transistor configuration

- A small change in the input voltage between emitter and base, say ΔV_i , causes a relatively larger change in emitter current, say ΔI_E.
- A fraction of this change in current is collected and passed through R_L and is denoted by symbol α'.
- Therefore the corresponding change in voltage across the load resistor R_L due to this current is $\Delta V_0 = \alpha' R_L \, \Delta I_E$
- Here , the voltage amplification $A_v = \frac{\Delta V_0}{\Delta V_i}$ is greater than unity and thus the transistor acts as an amplifier.

11 Derive an Eber's moll equation for a transistor.

Ans: The Eber's moll model is an ideal model for a bipolar transistor, which can be used in the forward active mode of operation, in the reverse active mode, in saturation and in cutoff. This model is the predecessor of today's compute simulation models and contains only the ideal diode currents.

Fig: Eber's Moll Model

Figure shows the Eber's Moll model for a transistor, which consists of two diodes and two current sources. The two diodes represent the base-emitter and base-collector diodes. The current sources quantify the transport of minority carriers through the base region. These current sources depend on the current through each diode. The parameters I_{EO}, I_{CO}, α_F *and* α_R are the saturation currents of the base-emitter and base-collector and the forward and reverse transport factors.

Using the parameters identified in figure, we can obtained the relation between the emitter, base and collector currents to the forward and reverse currents and transport factors as follows.

By applying the KCL at collector node of figure, we get,

$$I_C + \alpha_F I_E = I$$

$$\Rightarrow \quad I_C = -\alpha_F I_E + I$$

$$\Rightarrow \quad I_C = -\alpha_F I_E + I_0\left[e^{\frac{V_{CB}}{V_T}} - 1\right]$$

Where, I = diode current

I_0 = Magnitude of reverse saturation current.

But, $I_0 = -I_{C0}$

Then, the expression for collector current becomes as,

$$I_C = -\alpha_F I_E - I_{CO}\left[e^{\frac{V_{CB}}{V_T}} - 1\right] \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (1)$$

Similarly, in the inverted mode of operation, by applying the KCL at emitter node of figure, we get,

$$I_E + \alpha_R I_C = I'$$

$$\Rightarrow \quad I_E = -\alpha_R I_C + I'$$

$$\Rightarrow \quad I_E = -\alpha_R I_C + I_0\left[e^{\frac{V_{EB}}{V_T}} - 1\right]$$

But, $I_0 = -I_{EO}$

Then, the expression for emitter current becomes as,

$$I_E = -\alpha_R I_C - I_{EO}\left[e^{\frac{V_{EB}}{V_T}} - 1\right] \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (2)$$

And the Eber's Moll parameters are related by the following equation,

$$I_{EO}\alpha_F = I_{CO}\alpha_R \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (3)$$

This relation is also referred as the reciprocity relation and can be derived by examining the minority carrier current through the base. For the specific case, where the base-emitter and base-collector voltage are the same and the base doping is uniform, there can be no minority carrier diffusion in the base so that,

$$I_F(V_{EB})\alpha_F = I_R(V_{CB} = V_{EB})\alpha_R \cdots\cdots\cdots\cdots\cdots\cdots\cdots (4)$$

Using above expression, we can obtain the reciprocity relation. The forward and reverse bias transport factors are obtained by measuring the current gain in the forward or normal active and reverse or inverted active mode of operation. The saturation currents I_{EO} and I_{CO} are obtained by measuring the base-emitter (or base-collector) diode current while shorting the base-collector (or base-emitter) diode.

If $\alpha_F = \alpha_R = 0$, then the dependent current sources in figure may be removed. All the minority carriers will recombine in the base, if the width of the base is made much larger than the diffusion length of minority carriers in the base. Due to the above process, no minority carrier will be available to reach the collector. Thus, the transistor action ceases due to the zero amplification factor. Therefore, it's simply impossible to construct a transistor by placing two isolated diodes back to back.

12 Define α_{dc} and β_{dc} of a transistor. Derive the relation between them and write any two applications of transistor.

Ans: α_{dc} : The relation between I_E and I_C due to majority carriers is related by α, in a DC mode. α_{dc} is defined by the following formula,

$$\alpha_{dc} = \frac{\Delta I_C}{\Delta I_E}$$

Where, ΔI_C and ΔI_E are the change in collector and emitter currents at the point of operation. α ranges from 0.90 to 0.998. Since α is defined for the majority carriers, we have,

$$\Delta I_C = \alpha\Delta I_E + \Delta I_B$$

$\boldsymbol{\beta_{dc}}$**:** The relation between collector current I_C and base current I_B in a DC mode is defined as,

$$\beta_{dc} = \frac{\Delta I_C}{\Delta I_B}$$

ΔI_C and ΔI_B are calculated at a particular operating point on the characteristic curves.

Relationship between $\boldsymbol{\alpha_{dc}}$ $\boldsymbol{and}$ $\boldsymbol{\beta_{dc}}$

A simple relation exists between β and α. This can be derived as follows,

$$\beta = \frac{\Delta I_C}{\Delta I_B} \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (1)$$

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (2)$$

Now $\quad I_E = I_B + I_C$

$$\Delta I_E = \Delta I_B + \Delta I_C$$

$$\Rightarrow \quad \Delta I_B = \Delta I_E - \Delta I_C$$

Substituting the value of ΔI_B in equation (1), we get,

$$\beta = \frac{\Delta I_C}{\Delta I_E - \Delta I_C} \cdots\cdots\cdots\cdots\cdots\cdots (3)$$

Dividing the numerator and denominator of RHS of equation (3) by ΔI_E, we get,

$$\beta = \frac{\Delta I_C / \Delta I_E}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}} = \frac{\alpha}{1-\alpha} \qquad \left[since \;\; \alpha = \frac{\Delta I_C}{\Delta I_E} \right]$$

$$\therefore \beta = \frac{\alpha}{1-\alpha}$$

It is clear that as α approaches unity, β approaches infinity. In other words, the current gain in CE configuration is very high. Because of this reason, this circuit arrangement is used in about 90 to 95 percent of all transistor applications.

Application of transistor:

- Used in amplifier circuits
- Used in oscillator circuits
- Used as a switch in digital circuits
- It finds many applications in computers, satellites and modern communication systems.

13. What is the use of biasing? Draw the DC equivalent model.

Ans: TRANSISTOR BIASING

The basic function transistor is to do amplification. The process of raising the strength of a weak signal without any change in its shape is known as faithful amplification. For faithful amplification, the following three conditions must be satisfied:

i) The emitter-base junction should be forward biased,

ii) The collector-base junction should be reverse biased.

iii) Three should be proper zero signal collector current.

The proper flow of zero signal collector current (proper operating point of a transistor) and the maintenance of proper collector-emitter voltage during the passage of signal is known as 'transistor biasing'.

When a transistor is not properly biased, it work inefficiently and produces distortion in the output signal. Hence a transistor is to be biased correctly. A transistor is biased either with the help of battery (or) associating a circuit with the transistor. The latter method is generally employed. The circuit used with the transistor is known as biasing circuit.

In order to produce distortion-free output in amplifier circuits, the supply voltages and resistances in the circuit must be suitably chose. These voltages and resistances establish a set of d.c. voltage V_{CEQ} and current I_{CQ} to operate the transistor in the active region. These voltages and currents are called quiescent values which determine the operating point (or) Q-Point for the transistor.

The process of giving proper supply voltages and resistances for obtaining the desired Q Point is called biasing.

DC Load Line:

Consider common emitter configuration circuit shown in figure below:

In transistor circuit analysis generally it is required to determine the value of I_C for any desired value of V_{CE}. From the load line method, we can determine the value of I_C for any desired value of V_{CE}. The output characteristics of CE configuration is shown in figure below:

By applying KVL to the collector circuit

$$-V_C + I_C R_C + V_{CE} = 0$$

$$\Rightarrow V_{CC} = I_C R_C + V_{CE}$$
$$\Rightarrow V_{CE} = V_{CC} - I_C R_C$$

If the bias voltage V_{BB} is such that the transistor is not conducting then I_C=0 and V_{CE}= V_{CC}.

Therefore, when I_C=0, V_{CE}= V_{CC} this point is plotted on the output characteristics as point A.

If V_{CE}=0 then

$$0 = V_{CC} - I_C R_C$$

$$\Rightarrow I_C = \frac{V_{CC}}{R_C}$$

Therefore, V_{CE}=0, $I_C = \frac{V_{CC}}{R_C}$ this point is plotted on the output characteristics as point B.

The line drawn through these points is straight line 'd.c load line'.

The d.c. load line is plot of I_C versus V_{CE} for a given value of R_C and a given level of V_{CC}. Hence from the load line we can determine the I_C for any desired value of V_{CE}.

Operating Point (or) Quiescent Point:

In designing a circuit, a point on the load line is selected as the dc bias point (or) quiescent point. The Q-Point specifies the collector current I_C and collector to emitter voltage V_{CE} that exists when no input signal is applied. The dc bias point (or) quiescent point is the point on the load line which represents the current in a transistor and the voltage across it when no signal is applied. The zero signal values of I_C ad V_{CE} are known as the operating point.

Biasing:

The process of giving proper supply voltages and resistances for obtaining the desired Q point is called 'biasing'.

14. Explain the criteria for fixing operating point. (or) Explain the reasons for keeping the operating point of a transistor as fixed.

Ans:

- The operating point can be selected at three different positions on dc load line: near saturation region, near cut-off region or at the center, i.e. in the active region.
- The selection of operating point will depend on its application. When transistor is used as an amplifier, the Q point should be selected at the center of the dc load line to prevent any possible distortion in the amplified output signal. This is well-understood by going through following cases.
- **Case 1:** Biasing circuit is designed to fix a Q-point at point P, as shown in fig.(a). point P is very near to the saturation region. The collector current is clipped at the positive half cycle. So, even though base current varies sinusoid ally, collector current is not a useful sinusoidal waveform. i.e. distortion is present at the output. Therefore, point P is not a suitable operating point.

Fig(a). Operating point near saturation region gives clipping at the positive peak.

- **Case 2:** In fig.(b) shows biasing circuit is designed to fix a Q point at point R is very near to the cut-off region. The collector current is clipped at the negative half cycle. So, point R is also not a suitable operating point.

Fig.(b) Operating point near cut-off region given clipping at the negative peak.

- **Case 3:** Biasing circuit is designed to fix a Q-point at point Q as shown in fig.(c). The output signal is sinusoidal waveform without any distortion. Thus point Q is the best operating point.

Fig(c). Operating point at the centre of active region is most suitable.

- A good amplifier amplifies signals without introducing distortion. Thus always the operating point is chosen as the mid point of the DC load line.

Stabilization:

The maintenance of operating point stable is known as *'Stabilization'*. There are two factors which are responsible for shifting the operating point. They are:

i) The transistor parameters are temperature dependent.

ii) When a transistor is replaced by another of same type, there is a wide spread in the values of transistor parameters.

So, stabilization of the operating point is necessary due to the following reasons:

a) Temperature dependence of I_C.

b) Individual variations and

c) Thermal runaway.

Temperature dependence of I_C:

The instability of I_C is principally caused by the following three sources:

i) The I_{CO} doubles for every 10^oC rise in temperature.

ii) Increase of β with increase of temperature.

iii) The V_{BE} decreases about 2.5mV per ^oC increase in temperature.

Individual variations:

When a transistor is replaced by another transistor of the same type, the values of β and V_{BE} are not exactly the same. Hence the operating point is changed. So it is necessary to stabilize the operating point irrespective of individual variations in transistors parameters.

Thermal Runaway:

Depending upon the construction of a transistor, the collector junction can withstand maximum temperature. The range of temperature lies between 60° C to 100° C for 'Ge' transistor and 150 ^oC to 225° C for 'Si' transistor. If the temperature increases beyond this range then the transistor

burns out. The increase in the collector junction temperature is due to thermal runaway. When a collector current flows in a transistor, it is heated i.e., its temperature increases. If no stabilization is done, the collector leakage current also increases. This further increases the transistor temperature. Consequently, there is a further increase in collector leakage current. The action becomes cumulative and the transistor may ultimately burn out. The self-destruction of an unstabilized transistor is known as thermal runaway.

The following two techniques are used for stabilization.

1) Stabilization techniques:

The technique consists in the use of a resistive biasing circuit which permits such a variation of base current I_B as to maintain I_C almost constant in spite of I_{CO}, β and V_{BE}.

2) Compensation techniques:

In this technique, temperature sensitive devices such as diodes, thermistors and sensistors etc., are used. Such devices produce compensating voltages and current in such a way that the operating points maintained stable.

Stability factors:

Since there are three variables which are temperature dependent, we can define three stability factors as below:

i) S: The stability factor 'S' is defined as the ration of change of collector current I_C with respect to the reverse saturation current I_{CO}, keeping β and V_{BE} constant.

i.e., $$S = \frac{\partial I_C}{\partial I_{CO}} \approx \left.\frac{\partial I_C}{\partial I_{CO}}\right|_{V_{BE},\ \beta \text{ constant}}$$

ii) **S':** The stability factor S' is defined as the rate of change of I_C with respect to V_{BE}, keeping I_{CO} and β constant i.e.,

$$S' = \frac{\partial I_C}{\partial V_{BE}} \approx \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\ \beta \text{ constant}}$$

iii) **S'':** The stability factor S'' is defined as the rate of change of I_C with respect to β, keeping I_{CO} and V_{BE} constant i.e.,

$$S' = \frac{\partial I_C}{\partial \beta} \approx \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CO},\ V_{BE} \text{ constant}}$$

Ideally, stability factor should be perfectly zero to keep operating point stable.
Practically, stability factor should have the value as minimum as possible.

Derivation of Stability Factor (S):

For a common emitter configuration collector current is given as,

$$I_C = \beta I_B + I_{CEO}$$
$$\Rightarrow I_C = \beta I_B + (1+\beta) I_{CO} \qquad \text{..... (1)}$$

Differentiating equation (1) w.r.t. I_C keeping β constant, we get

$$1 = \beta \frac{\partial I_B}{\partial I_C} + (1+\beta)\frac{\partial I_{CO}}{\partial I_C}$$

$$\Rightarrow 1 - \beta \frac{\partial I_B}{\partial I_C} = (1+\beta)\frac{\partial I_{CO}}{\partial I_C}$$

$$\Rightarrow \frac{\partial I_C}{\partial I_{CO}} = \frac{1+\beta}{1-\beta\frac{\partial I_B}{\partial I_C}}$$

$$\Rightarrow S = \frac{1+\beta}{1-\beta\frac{\partial I_B}{\partial I_C}} \qquad \text{..... (2)}$$

To obtain S' and S'':
In standard equation of I_C, replace I_B in terms of V_{BE} to get S'.
Differentiating equation of I_C w.r.t. β after replacing I_B in terms of V_{BE} to get S''.

15. List out the different types of biasing methods. Explain about collector to base bias circuit.
Ans: Methods of Biasing:
Some of the methods used for providing bias for a transistor are as follows:
1) Fixed bias (or) base resistor method.
2) Collector to base bias (or) biasing with feedback resistor.
3) Voltage divider bias.

Collector to Base bias (or) Biasing with feedback resistor:
A CE amplifier using collector to base bias circuit is shown in the figure. In this method, the biasing resistor is connected between the collector and the base of the transistor.

Fig. Collector–to–Base bias circuit.

Circuit Analysis:
Base Circuit:

Consider the base-emitter circuit, applying the KVL to the circuit we get,

$$V_{CC} - \left(I_B + I_C\right) R_C - I_B R_B - V_{BE} = 0$$

$$\Rightarrow V_{CC} = I_B \left(R_C + R_B\right) + I_C R_C + V_{BE}$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_C + R_B} \qquad \text{..... (1)}$$

But $I_C = \beta I_B$

$$\therefore I_C = \frac{\beta\left(V_{CC} - I_C R_C - V_{BE}\right)}{R_C + R_B} \qquad \text{..... (2)}$$

Collector circuit:
Consider the collector-emitter circuit, applying the KVL to the circuit we get

$$-V_{CC} + \left(I_B + I_C\right) R_C + V_{CE} = 0$$

$$\Rightarrow V_{CE} = V_{CC} - \left(I_C + I_B\right) R_C \qquad \text{..... (3)}$$

Stability factor S:
The stability factor S is given by,

$$S = \frac{1+\beta}{1-\beta\dfrac{\partial I_B}{\partial I_C}}$$

We have $I_B = \dfrac{V_{CC} - V_{BE} - I_C R_C}{R_B + R_C}$ = constant

Differentiating the above equation w.r.t. I_C we get

$$\frac{\partial I_B}{\partial I_C} = -\frac{R_C}{R_C + R_B}$$

$$\therefore S = \frac{1+\beta}{1+\beta\dfrac{R_C}{R_C + R_B}} \qquad \text{..... (4)}$$

The stability factor S is smaller than the value obtained by fixed bias circuit. Also 'S' can be made smaller by making R_B small (or) R_C large.
Stability factor S':

We have $I_C = \dfrac{\beta\left(V_{CC} - V_{BE} - I_C R_C\right)}{R_C + R_B}$

Differentiating the above equation w.r.t. I_C,

We get $$1 = -\frac{\beta}{R_B + R_C}\frac{\partial V_{BE}}{\partial I_C} - \beta\frac{R_C}{R_B + R_C}$$

$$1+\beta\frac{R_C}{R_B+R_C}=-\frac{\beta}{R_B+R_C}\frac{\partial V_{BE}}{\partial I_C}$$

$$\frac{R_C+R_B+\beta R_C}{R_C+R_B}=-\frac{\beta}{R_C+R_B}\frac{\partial V_{BE}}{\partial I_C}$$

$$\Rightarrow S^{'}=-\frac{\beta}{R_B+(1+\beta)R_C} \qquad \text{..... (5)}$$

Stability factor S":

We have $I_C=\dfrac{\beta\left(V_{CC}-V_{BE}-I_C R_C\right)}{R_C+R_B}$

Differentiating the above equation w.r.t. β,

We get $$\frac{\partial I_C}{\partial\beta}=\frac{V_{CC}-V_{BE}}{R_C+R_B}-\frac{R_C}{R_C+R_B}\left[I_C+\beta\frac{\partial I_C}{\partial\beta}\right]$$

$$\Rightarrow\frac{\partial I_C}{\partial\beta}\left[1+\beta\frac{R_C}{R_C+R_B}\right]=\frac{V_{CC}-V_{BE}-I_C R_C}{R_C+R_B}$$

$$\Rightarrow\frac{\partial I_C}{\partial\beta}\left[R_B(1+\beta)R_C\right]=V_{CC}-V_{BE}-I_C R_C$$

$$\Rightarrow S^{''}=\frac{V_{CC}-V_{BE}-I_C R_C}{R_B+(1+\beta)R_C}$$

$$\Rightarrow S^{''}=\frac{I_C\left(R_C+R_B\right)}{R_B+(1+\beta)R_C} \qquad \text{..... (6)}$$

17. Draw a BJT fixed bias circuit and derive the expression for the stability factor 'S'.

1). Fixed bias (or) base resistor method:
A CE amplifier used fixed bias circuit is shown in figure below:

Fig. Fixed bias circuit.

In this method, a high resistance R_B is connected between positive terminal of supply V_{CC} and base of the transistor. Here the required zero signal base current flows through R_B and is provided by V_{CC}.

In figure, the base-emitter junction is forward biased because the base is positive w.r.t. emitter. By a proper selection of R_B, the required zero signal base current (and hence $I_C=\beta I_B$) can be made to flow.

Circuit Analysis:
Base Circuit:
Consider the base-emitter circuit loop of the above figure.
Writing KVL to the loop, we obtain

$$-V_{CC} + I_B R_B + V_{BE} = 0$$

$$\Rightarrow V_{CC} = I_B R_B + V_{BE}$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

But $I_C = \beta I_B + I_{CEO}$

As I_{CEO} is very small, $I_C \approx \beta I_B$

$$\therefore I_C = \beta\left(\frac{V_{CC} - V_{BE}}{R_B}\right)$$

$\Rightarrow$ β, V_{CC}, V_{BE} are constant for a transistor $\therefore$ I_C depends on R_B.

Choose suitable value of R_B to get constant I_C in active region.

$$\therefore R_B = \frac{(V_{CC} - V_{BE})\beta}{I_C} \quad \text{(or)} \quad R_B = \frac{\beta V_{CC}}{I_C} \qquad (\because V_{BE} << V_{CC})$$

Collector Circuit:

Consider the collector-emitter circuit loop of the circuit.
Writing KVL to the collector circuit, we get

$$-V_{CC} + I_B R_B + V_{CE} = 0$$

$$\Rightarrow V_{CE} = V_{CC} - I_C R_C$$

Stability factor S:

The stability factor S is given by, $$S = \frac{1+\beta}{1-\beta\frac{\partial I_B}{\partial I_C}}$$

We have $I_B = \frac{V_{CC} - V_{BE}}{R_B}$ = constant $\therefore \frac{\partial I_B}{\partial I_C} = 0$

$$\therefore S = 1 + \beta$$

If β=100 then S=101. This shows that I_C changes 101 times as much as any changes in I_{CO}. Thus I_C is dependent upon I_{CO} and temperature.

The value of S is high and has very poor stability.

Stability factor S':

We have $I_C = \beta I_B + (1+\beta) I_{CO}$

But $I_B = \frac{V_{CC} - V_{BE}}{R_B}$

$$\therefore I_C = \beta\left(\frac{V_{CC} - V_{BE}}{R_B}\right) + (1+\beta) I_{CO}$$

Differentiating the above equation w.r.t. I_C,

We get $$1 = -\frac{\beta}{R_B}\frac{\partial V_{BE}}{\partial I_C}$$

$$\Rightarrow S' = -\frac{\beta}{R_B}$$

Stability factor S'':

We have $I_C = \beta I_B + (1+\beta) I_{CO}$

Differentiating the above equation w.r.t. β,

We get $\frac{\partial I_C}{\partial \beta} = I_B + I_{CO}$

$\Rightarrow S'' = \frac{I_C}{\beta}$ ($\because I_{CO}$ is very small & $I_B = \frac{I_C}{\beta}$)

Advantages of fixed bias circuit:

1. This is a simple circuit which uses very few components.
2. The operating point can be fixed anywhere in the active region of the characteristics by simply changing the values of R_B. Thus, it provides maximum flexibility in the design.

Disadvantages of fixed bias circuit:

1. With the rise in temperature the operating point if not stable.
2. When the transistor is replaced by another with different value of β, the operating point with shift i.e., the stabilization of operating point is very poor in fixed bias circuit.

Because of these disadvantages, fixed bias circuit required some modifications. In the modified circuit, R_B is connected between collector and base. Hence the circuit is called 'collector to base' bias circuit.

16. Draw the circuit diagram of a self bias BJT circuit and how to determine the values of R_1 and R_2.

Voltage Divider Bias (Or) Self-Bias (Or) Emitter Bias:

The voltage divider bias circuit is shown in figure.

Fig: Voltage devider bias circuit

In this method, the biasing is provided by three resistors R_1, R_2 and R_E. The resistors R_1 and R_2 acts as a potential divider giving a fixed voltage to the base. If collector current increases due to change in temperature (or) change in β, the emitter current I_E also increases and the voltage drop across R_E increases, reducing the voltage difference between base and emitter (V_{BE}).

Due to reduction in V_{BE}, base current I_B and hence collector current I_C is also reduces. Therefore, we can say that negative feedback exists in the emitter bias circuit. This reduction in collector current I_C components for the original change in I_C.

Circuit Analysis:

Let current flows through R_1. As the base current I_B is very small, the current flowing through R_2 can also be taken as I.

The calculation of collector current I_C is as follows:

The current 'I' flowing through R_1 (or) R_2 is given by

$$I = \frac{V_{CC}}{R_1 + R_2} \quad \text{..... (1)}$$

The voltage V_2 developed across R_2 is given by,

$$V_2 = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2 \quad \text{..... (2)}$$

Base Circuit:

Applying KVL to the base circuit, we have

$$V_2 = V_{BE} + V_E = V_{BE} + I_E R_E \qquad \Rightarrow V_2 = V_{BE} + I_C R_E \qquad (\because I_E \approx I_C)$$

$$\therefore I_C = \frac{V_2 - V_{BE}}{R_E} \quad \text{..... (3)}$$

Hence I_C is almost independent of transistor parameters and hence good stabilization is ensured.

Collector Circuit:

Applying KVL to the collector circuit, we have

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E \qquad \Rightarrow V_{CC} = I_C R_C + V_{CE} + I_C R_E \qquad (\because I_E \approx I_C)$$

$$\Rightarrow V_{CE} = V_{CC} - I_C (R_C + R_E) \quad \text{..... (4)}$$

Circuit analysis using Thevenin's Theorem:

The Thevenin equivalent circuit of voltage-divider bias is as shown below:

Fig. Simplified equivalent circuit.

From above figure we have,

$$V_2 = V_{Th} = \left(\frac{R_2}{R_1 + R_2} \right) V_{CC} \qquad \text{..... (5)}$$

$$R_{Th} = R_1 \square R_2 = \frac{R_1 R_2}{R_1 + R_2} \qquad \text{..... (6)}$$

Applying KVL to the base-emitter circuit, we have

$$V_{Th} = I_B R_{Th} + V_{BE} + \left(I_B + I_C \right) R_E \qquad \text{..... (7)}$$

Applying KVL to the collector-emitter circuit, we have

$$V_{CE} = V_{CC} - I_C \left(R_C + R_E \right) \qquad \left(\because I_C >> I_B \right) \text{.....(8)}$$

From equation (8), we have

$$\therefore I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E}$$

Substituting this value of I_C in equation (7), we have

$$V_{Th} = I_B R_{Th} + V_{BE} + R_E \left[I_B + \frac{V_{CC} - V_{CE}}{R_C + R_E} \right]$$

$$V_{Th} = I_B R_{Th} + V_{BE} + R_E I_B + \frac{R_E V_{CC}}{R_C + R_E} - \frac{R_E V_{CE}}{R_C + R_E}$$

From equation (9) we can calculate the value of collector voltage V_{CE} for each value of I_B.

Stability factor (S):

For determining stability factor 'S' for voltage divider bias, consider the Thevenin's equivalent circuit. Hence, Thevenin's equivalent voltage V_{th} is given by

$$V_{Th} = \frac{R_2}{R_1 + R_2} V_{CC}$$

and the R1 and R2 are replaced by R_B which is the parallel combination of R_1 and R_2.

$$\therefore R_B = \frac{R_1 R_2}{R_1 + R_2}$$

Applying KVL to the base circuit, we get

$$V_{Th} = I_B R_B + V_{BE} + \left(I_B + I_C \right) R_E$$

Differentiating w.r.t. I_C and considering V_{BE} to be independent of I_C we get,

$$0 = \frac{\partial I_B}{\partial I_C} \times R_B + \frac{\partial I_B}{\partial I_C} \left(R_E \right) + R_E$$

$$\therefore \frac{\partial I_B}{\partial I_C} \left(R_E + R_B \right) = -R_E \qquad \therefore \frac{\partial I_B}{\partial I_C} = \frac{-R_E}{R_E + R_B}$$

We have already seen the generalized expression for stability factor 'S' given by

$$S = \frac{1 + \beta}{1 - \beta \frac{\partial I_B}{\partial I_C}}$$

Substituting value of $\frac{\partial I_B}{\partial I_C}$ in the above equation, we get

$$\therefore S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E+R_B}\right)}$$

$$\Rightarrow S = \frac{(1+\beta)(R_E+R_B)}{R_B+R_E+\beta R_E} = \frac{(1+\beta)(R_E+R_B)}{R_B+(1+\beta)R_E}$$

$$S = (1+\beta)\left(\frac{1+\frac{R_B}{R_E}}{1+\beta+\frac{R_B}{R_E}}\right)$$

The ratio $\frac{R_B}{R_E}$ controls value of stability factor 'S'.

If $\frac{R_B}{R_E} << 1$ then above equation reduces to $S = (1+\beta)\left(\frac{1}{1+\beta}\right) = 1$

Practically $\frac{R_B}{R_E} \neq 0$ But to have better stability factor 'S', we have to keep ration $\frac{R_B}{R_E}$ as small as possible.

Stability factor 'S' for voltage divider bias (or) self bias is less as compared to other biasing circuits studied. So, this circuit is most commonly used.

Stability factor (S'):
Stability factor S' is given by

$$S' = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\ \beta \text{ constant}}$$

It is the variation of I_C with V_{BE} when I_{CO} and β are considered constant.

We know that, $I_C = \beta I_B + (1+\beta) I_{CO}$

$$I_B = \frac{I_C - (1+\beta) I_{CO}}{\beta}$$

and $V_{Th} = I_B R_B + V_{BE} + (I_B + I_C) R_E$

$$V_{BE} = V_{Th} - (R_E + R_B) I_B - R_E I_C$$

By substituting I_B in the above equation, we get

$$V_{BE} = V_{Th} - (R_E + R_B)\left(\frac{I_C - (1+\beta) I_{CO}}{\beta}\right) - R_E I_C$$

$$= V_{Th} - \frac{(R_E + R_B) I_C}{\beta} + \frac{(R_E + R_B)(1+\beta) I_{CO}}{\beta} - R_E I_C$$

$$\Rightarrow V_{BE} = V_{Th} - \frac{\left[(1+\beta) R_E + R_B\right] I_C}{\beta} + \frac{(R_E + R_B)(1+\beta) I_{CO}}{\beta}$$

Differentiating the above equation w.r.t V_{BE} with I_{CO} and β constant, we get

$$1 = 0 - \left[\frac{R_B + (1+\beta) R_E}{\beta}\right]\frac{\partial I_C}{\partial V_{BE}} + 0$$

$$\Rightarrow \frac{\partial I_C}{\partial V_{BE}} = \frac{-\beta}{R_B + (1+\beta) R_E}$$

$$\therefore S' = \frac{-\beta}{R_B + (1+\beta) R_E}$$

Stability Factor S'':

Stability factor S'' is given by $S'' = \left.\frac{\partial I_C}{\partial \beta}\right|$ I_{CO}, V_{BE} constant

We have, $$V_{BE} = V_{Th} - \frac{\left[R_B + (1+\beta) R_E\right] I_C}{\beta} + \left[\frac{(R_E + R_B)(1+\beta)}{\beta}\right] I_{CO}$$

$$= V_{Th} - \frac{\left[R_B + (1+\beta) R_E\right] I_C}{\beta} + V'$$

where $V' = \left[\frac{(R_E + R_B)(1+\beta)}{\beta}\right] I_{CO} = (R_E + R_B) I_{CO}$ $\quad (\because \beta >> 1)$

Therefore, we write the above equation in terms of I_C, we get

$$I_C = \frac{\beta\left[V_{Th} + V' - V_{BE}\right]}{R_B + R_E(1+\beta)}$$

Differentiating above equation w.r.t. taking V' independent of β, we get,

$$\frac{\partial I_C}{\partial \beta} = \frac{R_B + R_E(1+\beta)\left(V_{Th} + V' - V_{BE}\right) - \beta\left[V_{Th} + V' - V_{BE}\right]R_E}{\left[R_B + R_E(1+\beta)\right]^2}$$

Multiplying numerator and denominator by (1+β) we get,

$$\frac{\partial I_C}{\partial \beta} = \frac{(1+\beta)\left(R_B + R_E\right)\left(V_{Th} + V' - V_{BE}\right)}{(1+\beta)\left[R_B + R_E(1+\beta)\right]\left[R_B + R_E(1+\beta)\right]}$$

$$= \frac{S\left(V_{Th} + V' - V_{BE}\right)}{(1+\beta)\left[R_B + R_E(1+\beta)\right]} \qquad \left\{\because S = \frac{(1+\beta)\left(R_B + R_E\right)}{\left[R_B + R_E(1+\beta)\right]}\right\}$$

Multiplying numerator and denominator by β, we get

$$\frac{\partial I_C}{\partial \beta} = \frac{\beta\left(V_{Th} + V' - V_{BE}\right)S}{\beta(1+\beta)\left[R_B + R_E(1+\beta)\right]} = \frac{I_C S}{\beta(1+\beta)}$$

$$\left(\because I_C = \frac{\beta\left(V_{Th} + V' - V_{BE}\right)}{\left[R_B + R_E(1+\beta)\right]}\right) \qquad \therefore S'' = \frac{\partial I_C}{\partial \beta} = \frac{I_C S}{\beta(1+\beta)} \text{ where } S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_E + R_B}\right)}$$

18. What are the compensation techniques used for V_{BE} and I_{CO}? Explain with the help of suitable circuits.

Ans: The stabilization techniques refer to the use of resistive biasing circuits which permit I_B to vary so as to keep I_C relatively constant. On the other hand, compensation techniques refer to the use of temperature sensitive devices such as diodes, transistors, thermistors, sensistors etc., to compensate for the variation in currents. Sometimes for excellent bias and thermal stabilization, both stabilization as well as compensation techniques are used.

The following are some compensation techniques:

1) Diode compensation for instability due to V_{BE} variation.
2) Diode compensation for instability due to I_{CO} variation.
3) Thermistor compensation.
4) Sensistor compensation.

1) Diode compensation for instability due to V_{BE} variation:

For germanium transistor, changes in I_{CO} with temperature contribute more serious problem than for silicon transistor. On the other hand, in a silicon transistor, the changes of V_{BE} with temperature possesses significantly to the changes in I_C. A diode may be used as compensation element for variation in V_{BE} (or) I_{CO}. The figure below shows the circuit of self bias stabilization technique with a diode compensation for V_{BE}. The Thevenin's equivalent circuit is shown in figure.

Fig. Self bias with stabilization and compensation Fig. Thevenin's equivalent circuit

The diode D used here is of the same material and type as the transistor. Hence the voltage V_D across the diode has same temperature coefficient (-2.5mV/^{o}C) as V_{BE} of the transistor. The diode D is forward biased by the source V_{DD} and resistor R_D.

Applying KVL to the base circuit, we get

$$-V_{th} + I_B R_{th} + V_{BE} + I_E R_E - V_D = 0$$

$$\Rightarrow \quad V_{th} - V_{BE} + V_D = I_B R_{th} + R_E(I_E + I_C) \cdots\cdots\cdots (1)$$

But $\quad I_C = \beta I_B + (1+\beta) I_{CO} \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots \quad (2)$

From equation (1), we get

$$V_{th} - V_{BE} + V_D = R_E I_C + (R_{th} + R_E) I_B$$

Substituting value of I_B from equation (2), we get

$$V_{th} - V_{BE} + V_D = R_E I_C + (R_{th} + R_E)\left[\frac{I_C - (1+\beta) I_{CO}}{\beta}\right]$$

$$\Rightarrow \quad \beta(V_{th} - V_{BE} + V_D) = \beta R_E I_C + (R_{th} + R_E) I_C - (1+\beta) I_{CO}(R_{th} + R_E)$$

$$\Rightarrow \quad \beta(V_{th} - V_{BE} + V_D) = (1+\beta) I_{CO}\,(R_{th} + R_E) = I_C(R_{th} + (1+\beta) R_E)$$

$$\Rightarrow \quad I_C = \frac{\beta(V_{th} - V_{BE} + V_D) = (1+\beta) I_{CO}\,(R_{th} + R_E)}{R_{th} + (1+\beta) R_E} \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (3)$$

Since variation in V_{BE} with temperature is the same as the variation in V_D with temperature, hence the quantity (V_{BE}-V_D) remains constant in equation (3). So the current I_C remains constant in spite of the variation in V_{BE}.

2) Diode compensation for instability due to I_{CO} variation:

Consider the transistor amplifier circuit with diode D used for compensation of variation in I_{CO}. The diode D and the transistor are of the same type and same material.

In this circuit diode is kept in reverse biased condition. The reverse saturation current I_O of the diode will increase with temperature at the same as the transistor collector saturation current I_{CO}.

From figure $I = \frac{V_{CC}-V_{BE}}{R} \approx \frac{V_{cc}}{R} = constant$

The diode D is reverse biased by V_{BE}. So the current through D is the reverse saturation current I_O. Now base current $I_B = I - I_O$

But $I_C = \beta I_B + (1+\beta) I_{CO}$

$\Rightarrow \quad I_C = \beta(I - I_O) + (1+\beta) I_{CO}$

If $\beta \gg 1, I_C \approx \beta I - \beta I_O + \beta I_{CO}$

In the above expression, I is almost constant and if I_O of diode D and I_{CO} of transistor track each other over the operating temperature range, then I_C remains constant.

19. Explain bias compensation using Thermistor and Sensistors.

Ans: Thermistor Compensation:

This method of transistor compensation uses temperature sensitive resistive elements, thermistor rather than diodes (or) transistors: It has a negative temperature coefficient, its resistance decreases exponentially with increasing temperature as shown in the figure.

Slope of this curve = $\frac{\partial R_T}{\partial T}$

$\frac{\partial R_T}{\partial T}$ is the temperature coefficient for thermistor, and the slope is negative. So we can say that thermistor has negative temperature coefficient of resistance.

Figure below shows thermistor compensation technique. As shown in figure, R_2 is replaced by thermistor R_T in self bias circuit.

Fig. Thermistor compensation technique.

With increase in temperature, R_T decreases. Hence voltage drop across it also decreases. This voltage drop is nothing but the voltage at the base with respect to ground. Hence, V_{BE} decreases which reduces I_B. This behavior will tend to offset the increase in collector current with temperature.

We know that $I_C = \beta I_B + (1 + \beta) I_{CO}$

In this equation, there is increase in I_{CBO} and decreases in I_B which keeps I_C almost constant.Consider another thermistor compensation technique shown in figure. Here, thermistor is connected between emitter and V_{CC} to minimize the increase in collector current due to change in I_{CO}, V_{BE} (or) β with temperature.

Fig. Thermistor compensation technique.

I_C increase with temperature and R_T decreases with increase in temperature. Therefore, current flowing through R_E increases, which increases the voltage drop across it. Emitter to Base junction is forward biased. But due to increase in voltage drop across R_E, emitter is made more positive, which reduces the forward bias voltage V_{BE}. Hence, base current reduces. I_C is given by, $I_C = \beta I_B + (1 + \beta) I_{CO}$

As I_{CBO} increases with temperature, I_B decreases and hence I_C remain fairly constant.

Sensistor Compensation:

This method of transistor compensation uses sensistor, which is temperature sensitive resistive element. Sensistor has a positive temperature coefficient, i.e., its resistance increases exponentially with increasing temperature.

Slope of this curve = $\frac{\partial R_T}{\partial T}$

$\frac{\partial R_T}{\partial T}$ is the temperature coefficient for Sensistor, and the slope is positive. So we can say that sensistor has positive temperature coefficient of resistance. As shown in figure R_1 is replaced by sensistor R_T in self bias circuit. As temperature increases, R_T increases which decreases the current flowing through it. Hence current through R_2 decreases which reduces the voltage drop across it.

Fig. Sensistor compensation technique.

As voltage drop across R_2 decreases, I_B decreases. It means, when I_{CBO} increases with increase in temperature, I_B reduces due to variation in V_{BE}, maintaining I_C fairly constant.

20. Explain in detail about themal runaway and thermal resistance.

Ans: Thermal Runaway:

The collector current for the CE circuit is given by $I_C = \beta I_B + (1 + \beta) I_{CO}$ The three variables in the equation, β, I_B and I_{CO} increase with rise in temperature. In particular, the reverse saturation current (or) leakage current I_{CO} changes greatly with temperature. Specifically, it doubles for every ^{10oC} rise in temperature. The collector current I_C causes the collector-base junction temperature to rise which, in turn, increase I_{CO}, as a result I_C increase still further, which will further rise the temperature at the collector-base junction. This process is cumulative and it is referred to as self heating. The excess heat produced at the collector-base junction may even burn and destroy the transistor. This situation is called "Thermal Runaway" of the transistor.

Thermal Resistance:

Transistor is a temperature dependent device. In order to keep the temperature within the limits, the heat generated must be dissipated to the surroundings. Most of the heat within the transistor is produced at the collector junction. If the temperature exceeds the permissible limit,the junction is destroyed. For Silicon transistor, the temperature is in the range 150° C to 225° C. For Germanium, it is between 60° C to 100° C.

Let T_A ^oC be the ambient temperature i.e., the temperature of surroundings air around transistor and T_J ^oC, the temperature of collector-base junction of the transistor.

Let P_D be the power in watt dissipated at the collector junction. The steady state temperature rise at the collector junction is proportional to the power dissipated at the junction. It is given by

$$\partial T = T_J - T_A = \theta P_D$$

Where θ = constant of proportionality. Which is referred to as thermal resistance.

$$\theta = \frac{T_J - T_A}{P_D}$$

The unit of θ, the thermal resistance, is ^oC/watt.

The typical values of θ for various transistors vary from 0.2 ^oC/watt for a high power transistor to 1000 ^oC/watt for a low power transistor.

21. what is the condition for thermal stability?

Ans: Condition for thermal stability:

To avoid thermal runaway the required condition is that, the rate at which heat is released at the collector junction must not exceed the rate at which the heat can be dissipated under steady state condition.

$$\text{i.e., } \frac{dP_C}{dT_J} < \frac{dP_D}{dT_J} \qquad \cdots\cdots \quad (1)$$

we know that, the steady state temperature rise at the collector junction is proportional to the power dissipated at the junction.

$$\text{i.e., } \Delta T = T_J - T_A = \theta P_D$$

where,

$T_J = junction\ temperature(^0C)$

$T_A = Ambient\ temperature(^0C)$

$P_D = Dissipated\ power\ at\ the\ collector\ junction(watts)$

$\theta = Thermal\ resistance$

$$T_J - T_A = \theta P_D$$

Differentiate with respect to T_J, we get,

$\Rightarrow \quad 1 = \theta \frac{dP_D}{dT_J}$

$\Rightarrow \quad \frac{dP_D}{dT_J} = \frac{1}{\theta} \qquad \cdots\cdots \quad (2)$

Then, from equation (1), we have,

$\frac{dP_D}{dT_J} < \frac{1}{\theta}$ is the condition which must be satisfied to prevent thermal run away.

Thus, the transistor cannot runaway below a specified ambient temperature under any biasing condition.

21. Explain thermal instability. What are the factors affecting the stability factor?

Ans: Thermal instability:

The collector current for CE configuration is given by,

$$I_C = \beta I_B + (1 + \beta) I_{CO}$$

$$I_C = \frac{I_{CO}}{1-\alpha} + \frac{\alpha I_B}{1-\alpha}$$

i.e., change in temperature also effects the operating point i.e., I_{CO} doubles for every 10^0C rise in temperature.

The collector current causes the collector junction to rise its temperature. Hence, I_{CO} increases simultaneously and I_C also increases. This in turn increases the temperature and so I_{CO} still increases and then I_C. So, the transistor output characteristics will shift upwards. Then, the operating point changes. So, in certain cases, even if the operating point is fixed in the middle of active region, because of change in temperature, the operating point will be shifted to the saturation region.

The factors that affect the stability of Q point are

1) I_{CO}:

- The flow of current in circuit produces heat at the junctions. This heat increases the temperature at the junctions. We know that reverse saturation current I_{CO} increases with increasing temperature. Its value doubles for every 10^0C rise in temperature.
- Since $I_C = \beta I_B + (1 + \beta) I_{CO}$
  The increase in I_{CO} increase the collector current I_C
- The increase in I_C further raises the temperature at the junction and the same cycle repeats.
- This excessive increase in I_C shifts the Q point into the saturation region, changing the operating condition set by biasing circuit.
- The excess heat produced at the collector base junction may even burn and destroy the transistor. This situation is called ***thermal runaway***.

2) V_{BE}:

- V_{BE} changes with temperature at the rate of 2.5mV/ ^{0}C
- As I_B depends on V_{BE} and I_C depends on I_B $[since\ I_C = \beta I_B]$, I_C depends on V_{BE}.
- Thus I_C changes with temperature due to change in V_{BE}. The change in collector current I_C change the operating point.

3) β:

- Since $I_C = \beta I_B$, as β varies, I_C also varies. The change in I_C change the operating point.

22. Give the advantages of h-parameter analysis.

Ans: Analyzing the transistor circuits using h-parameters has the following advantages.

- The radio frequencies up to which, h-parameters are real numbers.
- h- parameters are very easy to measure.
- Using the transistor static characteristic curves, h-parameters can be found.
- In circuit analysis and design, these parameters are very convenient to use.
- h- parameters in one configuration can be easily converted into other configuration.
- These parameters are readily supplied by manufactures.

24. Analyze a single stage transistor amplifier using h-parameters.

Ans: Figure shows a single stage transistor amplifier with external load, signal source and proper biasing.

Fig: Basic amplifier circuit

Fig: h-parameter equivalent circuit of the single stage transistor amplifier circuit.

Current Gain (or) Current Amplification, A_I

From output circuit $I_2 = h_f I_1 + h_O V_2$

But $V_2 = I_L Z_L = -I_2 Z_L$

$$\therefore I_2 = h_f I_1 - I_2 Z_L h_O$$

$$I_2 + I_2 Z_L h_O = h_f I_1$$

$$I_2(1 + Z_L h_O) = h_f I_1$$

$$A_I = -\frac{I_2}{I_1} = \frac{-h_f}{1+Z_L h_O}$$

$$A_I = \frac{-h_f}{1+h_O Z_L}$$

Input Impedance (Z_i):

In the circuit, Rs is the signal source resistance. The impedance seen when looking into the amplifier terminals (1, 1') is the amplifier input impedance Z_i , i.e.,

$$Z_i = \frac{V_1}{I_1} = \frac{h_f I_1 + h_r V_2}{I_1} = h_f + \frac{h_r V_2}{I_1}$$

Substituting $V_2 = -I_2 Z_L = A_I I_1 Z_L$

$$Z_i = h_i + h_r A_I z_L$$

Substituting for A_I

$$Z_i = h_f - \frac{h_f h_r Z_L}{1+h_o Z_L}$$

$$= h_i - \frac{h_f h_r}{Z_L\left[\frac{1}{Z_L}+h_O\right]} Z_L$$

Taking the load admittance as $Y_L = \frac{1}{Z_L}$

$$\therefore Z_i = h_i - \frac{h_f h_r}{Y_L + h_O}$$

Voltage Gain (or) Voltage Amplification factor (Av):

The ratio of the output voltage V_2 to the input voltage V_i gives the voltage gain of the transistor. i.e.,

$$A_V = \frac{V_2}{V_1}$$

Substituting $V_2 = -I_2 Z_L = A_I I_1 Z_L$

$$A_V = \frac{A_I I_1 Z_L}{V_1} = \frac{A_I Z_L}{Z_i}$$

$$A_V = \frac{A_I Z_L}{Z_i}$$

Output Admittance (Y_O):

By definition, Y_O is obtained by setting V_1 to zero, Z_L to infinity and by driving the output terminals from a generator V_2. . If the current drawn from V_2 is I_2, then

$$Y_0 = \frac{I_2}{V_2} = with\ V_1 = 0\ \&\ R_L = \infty$$

From the circuit, $I_2 = h_f I_1 + h_O V_2$

Dividing by V_2, $\frac{I_2}{V_2} = h_f \frac{I_1}{V_2} + h_O$

From the circuit $V_1 = h_f I_1 + h_r V_2$

Dividing by V_2, & taking $V_1 = 0$

$$0 = h_f \frac{I_1}{V_2} + h_r$$

$$\Rightarrow \frac{I_1}{V_2} = \frac{-h_r}{h_f}$$

Using this equation in the above we get,

$$\frac{I_2}{V_2} = h_f \left(\frac{-h_r}{h_f}\right) + h_O$$

$$\therefore Y_O = h_o - \frac{h_f h_r}{h_i}$$

Voltage Amplification (A_{VS}) taking into account the resistance (R_S) of the source:

The overall voltage gain A_{VS} is given by

$$A_{vs} = \frac{V_2}{V_s} = \frac{V_2}{V_1} \times \frac{V_1}{V_s} = A_V \times \frac{V_1}{V_s}$$

$$V_1 = \frac{V_s Z_i}{Z_i + R_s}$$

$$\frac{V_1}{V_s} = \frac{Z_i}{Z_i + R_s} \; then \; A_{vs} = \frac{A_v Z_i}{Z_i + R_s}$$

Substituting $A_v = \frac{A_I Z_L}{Z_i + R_s}$

Note that if $R_s = 0, then \; A_{vs} = \frac{A_I Z_L}{Z_i + R_s} = A_v$. Hence, A_V is the voltage gain with an ideal voltage source (with Rs=0). In practice, A_{VS} is more meaningful than A_V because source resistance has an appreciable effect on the overall amplification.

Current amplification (A_{IS}) taking into account the source resistance:

The equivalent input circuit using Norton's equivalent circuit for the source, for the calculation of A_{IS} is shown in fig. below.

Overall current gain, $A_{IS} = \frac{-I_2}{I_s} = \frac{-I_2}{I_1} \times \frac{I_1}{I_s} = A_I \times \frac{I_1}{I_s}$

$$I_1 = I_s \times \frac{R_s}{R_s + Z_i}$$

$$\frac{I_1}{I_s} = \frac{R_s}{R_s + Z_i}$$

If $R_S = \infty$, then $A_{IS} = A_I$. Hence, A_I is the current gain with an ideal current source (one with infinite source resistance).

But , $A_{vs} = \frac{A_I Z_L}{Z_i + R_s} \cdot \frac{R_s}{R_s}$

$$\Rightarrow \; A_{vs} = \frac{A_{IS} Z_L}{R_s}$$

Operating Power Gain:

Average power delivered to the load is $P_2 = |V_2||I_L|cos\theta$, where θ is the phase angle between V_2 and I_L. Assume that Z_L is resistive i.e., $Z_L = R_L$. Since h-parameters are real at low frequencies, the power delivered to the load is $P_2 = V_2 I_L = -V_2 I_2$, since the input power $P_1 = V_1 I_1$, the operating power gain A_p of the transistor is defined as

$$A_P = \frac{P_2}{P_1} = \frac{-V_2 I_2}{V_1 I_1} = A_v A_I$$

$$A_P = A_I A_I \frac{R_L}{R_i}$$

$$\therefore A_P = A_I^2 \frac{R_L}{R_i}$$

Input impedance taking into account the source resistance (R_S):

$$Z_{is} = \frac{V_s}{I_s} = R_s + Z_I$$

$$\therefore Z_{is} = R_s + h_i + h_r A_I Z_L$$

Output impedance taking into account the source resistance (R_S):

By definition, Y_O is obtained by setting V_S to zero, Z_L to infinitely and by driving the output terminals from a generator V_2.

If the current drawn from V_2 is I_2, then $Y_0 = \frac{I_2}{V_2}$ $with\ V_s = 0\ \&\ R_L = \infty$

from the circuit, $I_2 = h_f I_1 + h_O V_2$

Dividing V_2, $\frac{I_2}{V_2} = h_f \frac{I_1}{V_2} + h_O$

With $V_s = 0$, by applying KVL input circuit,

$$R_s I_1 + h_i I_1 + h_r V_2 = 0$$

$$I_1(R_s + h_i) + h_r V_2 = 0$$

$$\therefore \frac{I_1}{V_2} = \frac{-h_r}{R_s + h_f}$$

Using this in the above equation, we get

$$\frac{I_2}{V_2} = h_f \left[\frac{-h_r}{R_s + h_i}\right] + h_O$$

$$\therefore Y_0 = h_0 - \frac{h_f h_r}{R_s + h_i}$$

Problems:

Problems1.

In a common-base connection, the emitter current I_E is 6.28 mA and the collector current I_C is 6.20 mA. Determine the common-base d.c. current gain.

Solution:

Given: $I_E = 6.28$ mA and $I_C = 6.20$ mA

We know that common-base d.c. current gain,

$$\alpha = \frac{I_C}{I_E} = \frac{6.20 \times 10^{-3}}{6.28 \times 10^{-3}} = 0.987$$

Problem2.

The transistor has $I_E = 10$ mA and $\alpha = 0.98$. Determine the values of I_C and I_B.

Solution:

Given: $I_E = 10$ mA and $\alpha = 0.98$

The common-base d.c. current gain, $\alpha = \frac{I_C}{I_E}$

i.e. $0.98 = \frac{I_C}{10}$

Therefore $I_C = 0.98 \times 10 = 9.8$ mA

The emitter current $I_E = I_B + I_C$

i.e. $10 = I_B + 9.8$

Therefore, $I_B = 0.2$ mA

Problem3.

A transistor has $\beta = 100$. If the collector current is 40 mA, find the value of emitter current.

Solution:

Given: $\beta = 100$ and $I_C = 40$ mA

$$\beta = 100 = \frac{I_C}{I_B} = \frac{40}{I_B}$$

Therefore, $I_B = 40/100 = 0.4$ mA and

$$I_E = I_B + I_C = (0.4 + 40) \times 10^{-3} = 40.4 \text{ mA}$$

Problem4.

A transistor has $I_B = 100\ \mu A$ and $I_C = 2$ mA. Find (a) β of the transistor, (b) α of the transistor, (c) emitter current I_E, (d) if I_B changes by + 25 μA and I_C changes by + 0.6 mA, find the new value of β.

Solution:

Given: $I_B = 100\ \mu A = 100 \times 10^{-6}$ A and $I_C = 2$ mA $= 2 \times 10^{-3}$ A.

(a) **To find β of the transistor**

$$\beta = \frac{I_C}{I_B} = \frac{2 \times 10^{-3}}{100 \times 10^{-6}} = 20$$

(b) **To find α of the transistor**

$$\alpha = \frac{\beta}{\beta + 1} = \frac{20}{1 + 20} = 0.952$$

(c) **To find emitter current, I_E**

$$I_E = I_B + I_C = 100 \times 10^{-6} + 2 \times 10^{-3}\ \text{A}$$
$$= (0.01 + 2) \times 10^{-3} = 2.01 \times 10^{-3}\ \text{A} = 2.01\ \text{mA}$$

(d) **To find the new value of β when** $\Delta I_B = 25\ \mu A$ and $\Delta I_C = 0.6$ mA

Therefore,

$$I_B = (100 + 25)\ \mu A = 125\ \mu A$$
$$I_C = (2 + 0.6)\ \text{mA} = 2.6\ \text{mA}$$

New value of β of the transistor,

$$\beta = \frac{I_C}{I_B} = \frac{2.6 \times 10^{-3}}{125 \times 10^{-6}} = 20.8$$

Problem5.

For a transistor circuit having $\alpha = 0.98$, $I_{CBO} = I_{CO} = 5\ \mu A$ and $I_B = 100\ \mu A$, find I_C and I_E.

Solution:

Given: $\alpha = 0.98$, $I_{CBO} = I_{CO} = 5\ \mu A$ and $I_B = 100\ \mu A$

The collector current is

$$I_C = \frac{\alpha \cdot I_B}{1 - \alpha} + \frac{I_{CO}}{1 - \alpha} = \frac{0.98 \times 100 \times 10^{-6}}{1 - 0.98} + \frac{5 \times 10^{-6}}{1 - 0.98} = 5.15\ \text{mA}$$

The emitter current is

$$I_E = I_B + I_C = 100 \times 10^{-6} + 5.15 \times 10^{-3} = 5.25\ \text{mA}$$

Problem6.

Determine I_C, I_E and α for a transistor circuit having $I_B = 15\ \mu A$ and $\beta = 150$.

Solution:

The collector current, $I_C = \beta I_B = 150 \times 15 \times 10^{-6} = 2.25$ mA

The emitter current, $I_E = I_C + I_B = 2.25 \times 10^{-3} + 15 \times 10^{-6} = 2.265$ mA

Common-base current gain, $\alpha = \dfrac{\beta}{1+\beta} = \dfrac{150}{151} = 0.9934$

Problem7.

Determine the base, collector and emitter currents and V_{CE} for a CE circuit shown in Fig. For $V_{CC} = 10$ V, $V_{BB} = 4$ V, $R_B = 200$ kΩ, $R_C = 2$kΩ, V_{BE} (on) = 0.7 V, $\beta = 200$.

Solution:

Referring to Fig. 6.18, the base current is

$$I_B = \frac{V_{BB} - V_{BE}(on)}{R_B} = \frac{4 - 0.7}{200 \times 10^3} = 16.5\ \mu A$$

The collector current is

$$I_C = \beta I_B = 200 \times 16.5 \times 10^{-6} = 3.3 \text{ mA}$$

The emitter current is

$$I_E = I_C + I_B = 3.3 \times 10^{-3} + 16.5 \times 10^{-6} = 3.3165 \text{ mA}$$

Therefore, $V_{CE} = V_{CC} - I_C R_C = 10 - 3.3 \times 10^{-3} \times 2 \times 10^3 = 3.4$ V

Problem8.

Calculate the values of I_C and I_E for a transistor with $\alpha_{d.c.} = 0.99$ and $I_{CBO} = 5\ \mu A$. I_B is measured as $20\ \mu A$.

Solution:

Given, $\alpha_{d.c.} = 0.99$, $I_{CBO} = 5\ \mu A$ and $I_B = 20\ \mu A$

$$I_C = \frac{\alpha_{d.c.} I_B}{1-\alpha_{d.c.}} + \frac{I_{CBO}}{1-\alpha_{d.c.}} = \frac{0.99 \times 20 \times 10^{-6}}{1-0.99} + \frac{5 \times 10^{-6}}{1-0.99} = 2.48\ mA$$

Therefore, $$I_E = I_B + I_C = 20 \times 10^{-6} + 2.48 \times 10^{-3} = 2.5\ mA$$

Problem9.

The reverse leakage current of the transistor when connected in CB configuration is $0.2\ \mu A$ and it is $18\ \mu A$ when the same transistor is connected in CE configuration. Calculate $\alpha_{d.c.}$ and $\beta_{d.c.}$ of the transistor.

Solution:

The leakage current $I_{CBO} = 0.2\ \mu A$

$I_{CEO} = 18\ \mu A$

Assume that $I_B = 30\ mA$

$I_E = I_B + I_C$

$I_C = I_E - I_B = \beta I_B + (1+\beta)\, I_{CBO}$

We know that $$I_{CEO} = \frac{I_{CBO}}{1-\alpha} = (1+\beta) I_{CBO}$$

$$\beta = \frac{I_{CEO}}{I_{CBO}} - 1 = \frac{18}{0.2} - 1 = 89$$

$$I_c = \beta I_B + (1+\beta) I_{CBO}$$
$$= 89\,(30 \times 10^{-3}) + (1+89)\,(0.2 \times 10^{-6})$$
$$= 2.67\ A$$

$$\alpha_{d.c.} = 1 - \frac{I_{CBO}}{I_{CEO}} = 1 - \frac{0.2 \times 10^{-6}}{18 \times 10^{-6}} = 0.988$$

$$\beta_{d.c.} = \frac{I_C - I_{CBO}}{I_B - I_{CEO}}$$
$$= \frac{2.67 - 0.2 \times 10^{-6}}{30 \times 10^{-3} - 18 \times 10^{-6}} = 89$$

Problem10.

For the transistor amplifier shown in Fig. 6.23(a), $V_{CC} = 12$ V, $R_1 = 8$ kΩ, $R_2 = 4$ kΩ, $R_C = 1$ kΩ, $R_E = 1$ kΩ and $R_L = 1.5$ kΩ. Assume $V_{BE} = 0.7$ V. (i) Draw the d.c. load line, (ii) determine the operating point, and (iii) draw the a.c. load line.

Solution:

(i) *DC load line:*

Referring to Fig. 6.23(a), we have $V_{CC} = V_{CE} + I_C (R_C + R_E)$.

To draw the d.c. load line, we need two end points, viz. maximum V_{CE} point (at $I_C = 0$) and maximum I_C point (at $V_{CE} = 0$).

Maximum $V_{CE} = V_{CC} = 12$ V, which locates the point B ($0B = 12$ V) of the d.c. load line.

$$\text{Maximum} \qquad I_C = \frac{V_{CC}}{R_C + R_E} = \frac{12}{(1+1)\times 10^3} = 6 \text{ mA}$$

Fig. 6.23

This locates the point A ($0A$ = 6 mA) of the d.c. load line. Figure 6.23(b) shows the d.c. load line AB, with (12 V, 6 mA).

(ii) *Operating point Q*

The voltage across R_2 is $V_2 = \dfrac{R_2}{R_1 + R_2} V_{CC}$

Therefore,
$$V_2 = \frac{4 \times 10^3}{12 \times 10^3} \times 12 = 4 \text{ V}$$
$$V_2 = V_{BE} + I_E R_E$$

Therefore,
$$I_E = \frac{V_2 - V_{BE}}{R_E} = \frac{4 - 0.7}{1 \times 10^3} = 3.3 \text{ mA}$$
$$I_C \approx I_E = 3.3 \text{ mA}$$
$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$
$$= 12 - 3.3 \times 10^{-3} \times 2 \times 10^3 = 5.4 \text{ V}$$

Therefore, the operating point Q is at 5.4 V and 3.3 mA, which is shown on the d.c. load line.

(iii) *AC load line*

To draw the a.c. load line, we need two end points, viz. maximum V_{CE} and maximum I_C when signal is applied.

AC load,
$$R_{\text{a.c.}} = R_C \parallel R_L = \frac{1 \times 1.5}{2.5} = 0.6 \text{ k}\Omega$$

Therefore, maximum V_{CE}
$$= V_{CEQ} + I_{CQ} R_{\text{a.c.}}$$
$$= 5.4 + 3.3 \times 10^{-3} \times 0.6 \times 10^3 = 7.38 \text{ V}$$

This locates the point C ($0C$ = 6.24 V) on the V_{CE} axis.

$$\text{Maximum } I_C = I_{CQ} + \frac{V_{CEQ}}{R_{\text{a.c.}}}$$

$$= 3.3 \times 10^{-3} + \frac{5.4}{0.6 \times 10^3} = 12.3 \text{ mA}$$

This locates the point D ($0D$ = 12.3 mA) on the I_C axis. By joining points C and D, a.c. load line CD is constructed.

Problem11.

Design the circuit shown in Fig. 6.24, given Q-point values are to be I_{CQ} = 1 mA and V_{CEQ} = 6 V. Assume that V_{CC} = 10 V, β = 100 and V_{BE} (*on*) = 0.7 V.

Solution: The collector resistance is

$$R_C = \frac{V_{CC} - V_{CEQ}}{I_{CQ}} = \frac{10-6}{1\times10^{-3}} = 4\ \text{k}\Omega$$

Fig. 6.24

The base current is

$$I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{1\times10^{-3}}{100} = 10\ \mu\text{A}$$

The base resistance is

$$R_B = \frac{V_{CC} - V_{BE}\ (on)}{I_{BQ}} = \frac{10-0.7}{10\times10^{-6}} = 0.93\ \text{M}\Omega$$

Problem12.

Figure below shows a silicon transistor with β=100 and biased by base resistor method. Determine the operating point.

Solution:

Given V_{CC}=10V, V_{BE}=0.7V (Silicon transistor), β=100, R_B=930KΩ.

Applying KVL to base-emitter loop,

$$V_{CC} - V_{BE} = I_B R_B \Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$I_C = \beta I_B = \beta\left(\frac{V_{CC}-V_{BE}}{R_B}\right) = 100\left(\frac{10-0.7}{930\times10^3}\right) = 1mA$$

Applying KVL to collector-emitter loop,

$$V_{CC} - V_{CE} = I_C R_C \Rightarrow V_{CE} = V_{CC} - I_C R_C$$

$$\Rightarrow V_{CE} = 10 - \left(1\times10^{-3}\times4\times10^3\right) = 6V$$

∴ Operating point is (6V, 1mA)

2. For the following circuit shown in figure below, find the operating point.

Solution:

KVL to base- emitter loop is

$$-V_{CC} + I_B R_B + V_{BE} + \left(I_C + I_B\right) R_E = 0$$

$$I_B R_B + \beta I_B R_E + I_B R_B = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_E}$$

$$\therefore I_B = \frac{20 - 0.7}{(430 + 51) \times 10^3} = 40.1 \mu A$$

$$I_C = \beta I_B = 2.01 mA$$

KVL to collector- emitter loop is

$$-V_{CC} + I_C R_C + V_{CE} + I_C R_E = 0$$

$$\Rightarrow V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$V_{CE} = 20 - 2.01 \times 10^{-3} (2+1) \times 10^3 \quad = 20 - 6.03 = \mathbf{13.97V}$$

$\therefore$ Operating point is **Q (13.97V, 2.01mA)**

Problem13.

An N-P-N transistor with β=50 is used in a CE circuit with V_{CC}=10V, R_C=2KΩ. The bias is obtained by connecting a 100KΩ resistance from collector to base. Assume V_{BE}=0.7V. Find

i) the quiescent point and

ii) Stability factor 'S'

Solution:

i) Applying KVL to the base circuit,

$$V_{CC} = (I_B + I_C)R_C + I_B R_B + V_{BE}$$
$$\Rightarrow V_{CC} = I_B(R_C + R_B) + I_C R_C + V_{BE}$$

$$\therefore I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_C + R_B} \qquad \therefore I_C = \frac{\beta(V_{CC} - V_{BE} - I_C R_C)}{R_C + R_B}$$

$$\therefore I_C = \frac{50(10 - 0.7 - 2\times10^{-3} I_C)}{102\times10^3} \qquad \Rightarrow I_C = 2.3mA$$

Applying KVL to Collector Circuit

$$V_{CC} = (I_B + I_C)R_C + V_{CE} \qquad \therefore V_{CE} = V_{CC} - (I_B + I_C)R_C$$

$$= 10 - (46\times10^{-6} + 2.3\times10^{-3})\times 2\times10^3$$

$$\Rightarrow V_{CE} = 5.308V$$ ∴ The quiescent point is **(5.308V, 2.3mA)**

ii) Stability factor, S:

$$S = \frac{1+\beta}{1+\beta\dfrac{R_C}{R_C + R_B}}$$

$$\Rightarrow S = \frac{51}{1+50\left(\dfrac{20\times10^3}{102\times10^3}\right)} = 25.75$$

Problem14.

A transistor with β=45 is used with collector to base resistor R_B biasing with quiescent value of 5V for V_{CE}. If V_{CC}=24V, R_C=10kΩ, R_E=270Ω, find the value of R_B.

Solution:
Applying KVL to collector and emitter loop, we have

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\Rightarrow V_{CC} - V_{CE} = I_C R_C + \left(I_C + I_B\right) R_E$$

$$\Rightarrow V_{CC} - V_{CE} = \left[\beta R_C + (1+\beta) R_E\right] I_B$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{\beta R_C + (1+\beta) R_E} = \frac{24-5}{45\times 10 + 50\times 0.27}$$

$$= 0.041 \text{ mA}$$

Further, $V_{CC} - I_C R_C - I_B R_B - V_{BE} - I_E R_E = 0$

$$\Rightarrow V_{CC} - V_{BE} = R_C \beta I_B + I_B R_B + (1+\beta) R_E I_B$$

$$\Rightarrow 24 - 0.7 = I_B\left[45\times 10 + R_B + 50\times 0.27\right] \qquad \Rightarrow 23.3 = 0.041\left[450 + R_B + 12.42\right]$$

$$\therefore R_B = 105.87\, K\Omega$$

Problem15.
For the circuit shown in figure, determine the value of I_C and V_{CE}. Assume V_{BE}=0.7V and β=100

Solution:

$$V_B = \frac{R_1}{R_1 + R_2} V_{CC} = \frac{5\times 10^3}{10\times 10^3 + 5\times 10^3} \times 10 = 3.33V$$

We know that $V_E = V_B - V_{BE} = 3.33 - 0.7 = 2.63V$

and $I_E = \frac{V_E}{R_E} = \frac{2.63V}{500} = 5.26mA$

We know that $I_B = \frac{I_E}{1+\beta} = \frac{2.63\times10^{-3}}{101} = 52.08\mu A$

and $I_C = \beta I_B = 100\times52.08\times10^{-6}$ = **5.208mA**

Applying KVL to the collector circuit we get

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\Rightarrow V_{CE} = V_{CC} - I_C R_C - I_E R_E \qquad = 10 - 5.208\times10^{-3}\times1\times10^{3} - 5.26\times10^{-3}\times500$$

$$\Rightarrow V_{CE} = 2.162V$$

JUNCTION FIELD EFFECT TRANSISTOR AND SPECIAL PURPOSE DEVICES

1. Draw the structure of an N- channel JFET and explain its principle of operation. Why is the name field effect used for the device.

Ans. Structure and symbol of n-channel JFET:

The structure and symbol of n-channel JFET are shown in figure below

(a) Structure of N- channel JFET (b) Symbol

The electrons enter the channel through the terminal called 'source' and leave through the terminal called 'drain'. The terminals taken out from heavily doped electrodes of p-type material are called 'gates'. Usually, these electrodes are connected together and only one terminal is taken out, which is called 'gate.

Construction of N-Channel JFET:

It consists of a N-type bar which is made of Silicon. Ohmic contacts (terminals), made at the two ends of the bar, are called Source and Drain.

Source (S) : This terminal is connected to the negative pole of the battery. Electronics which are the majority carriers in the N-type bar enter the bar through this terminal.

Drain (D) : This terminal is connected to the positive pole of the battery. The majority carriers leave the bar through this terminal.

Gate (G) : Heavily doped P-type silicon is diffused on both sides of the N-type silicon bar by which PN junctions are formed. These layers are joined together are called Gate(G).

Channel : The region BC of the N-type bar between the depletion regions is called the Channel. Majority carriers move from the source to drain when a potential difference VDS is applied between the source and drain.

Operation of N-Channel JFET:

The operation of N-Channel JFET can be understood with the help of figure below.

Fig. Operation of FET.

Before considering the operation, let us consider that how the depletion layers are formed. Let us first suppose that the gate has been reverse-biased by gate battery V_{GG} and the drain battery V_{DD} is not connected.

When V_{GS}=0 and V_{DS}=0:

When no voltage is applied between drain and source, and gate and source, the thickness of the depletion regions round the P-N junction is uniform as shown in figure below.

When V_{DS}=0 and V_{GS} is decreased from zero:

In this case, the P-N junctions are reverse-biased and hence the thickness of the depletion region increases. As V_{GS} is decreased from zero, the reverse bias voltage across the P-N junction is increased and hence, the thickness of the depletion region in the channel increases until the two depletion regions make contact with each other. In this condition, the channel is said to be cut-off. The value of V_{GS} which is required to cut-off the channel is called the cut-off voltage V_C.

When V_{GS}=0 and V_{DS} is increased from zero:

Drain is positive with respect to the source. Now the majority carriers (electrons) flow through the N-Channel from source to drain. Therefore the conventional current I_D flows from drain to source. The magnitude of the current will depend upon the following factors:

1. The conductivity of the channel.
2. The length of the channel.
3. The cross sectional area 'A' of the channel.
4. The magnitude of the applied voltage V_{DS}.

Thus the channel acts as a resistor of resistance 'R' is given by, $R = \frac{\rho L}{A}$

$$I_D = \frac{V_{DS}}{R} = \frac{AV_{DS}}{\rho L}$$

Where 'ρ' is the resistivity of the channel. As V_{DS} increases, the reverse voltage across the P-N junction increase and hence the thickness of the depletion region also increases. Therefore, the channel is wedge shaped as shown in fig. below.

As V_{DS} is increase, at a certain value V_P of V_{DS}, the cross sectional area of the channel becomes minimum. At this voltage, the channel is said to be pinched off and the drain voltage V_P is called the pinch-off voltage.

As a result of the decreasing cross-section of the channel with the increase of V_{DS}, the following results are obtained.

2. Draw the static characteristics curves of an n-channel JFET and explain the different portions of the characteristics. Define the pinch-off voltage and indicate its location on drain characteristics.

Ans.

Fig. Drain characteristics.

i) As V_{DS} is increased from zero, I_D increases linearly along OP, this region from V_{DS}=0 to V_{DS}=V_P is called the ohmic region. In this region, the FET acts as a voltage variable resistor (VVR) or voltage dependent resistor (VDR).

ii) When V_{DS}=V_P, I_D becomes maximum. When V_{DS} is increased beyond V_P, the length of the pinch-off (or) saturation region increases. Hence, there is no further increase of I_D.

iii) At a certain voltage corresponding to the point B, I_D suddenly increases. This effect is due to the Avalanche multiplication of electrons caused by breaking of covalent bonds of silicon atoms in the depletion region between the gate and the drain. The drain voltage at which the breakdown occurs is denoted by BV_{DGO}.

When V_{GS} is negative and V_{DS} is increased:

When the gate is maintained at a negative voltage less than the negative cut-off voltage, the reverse voltage across the junction is further increased. Hence for a negative value of V_{GS}, the curve of I_D versus V_{DS} is similar to that for V_{GS}=0, but the values of V_P and BV_{DGO} are lower. The drain current I_D is controlled by the electric field that extends into the channel due to reverse biased voltage applied to the gate, hence, this device has been given the name Field Effect Transistor.

3. Why FET is called unipolar device and is called as voltage operated device? What are the important characteristics of FET?

Ans. A device in which the flow of current through the conducting region is controlled by an electric field is called as FET. The conduction current flows only due to majority carriers. Thus, FET is called as unipolar device.

FET is also called as voltage controlled device because the voltage at the input terminal controls the output current.

Important characteristics of FET

- The flow of current in the conduction region is only due to majority carriers.
- The conduction is through an N-type or p-type semiconductor material due to the absence of junctions.
- FET has very high input impedance of the order 100MΩ.
- FET has lower output impedance.
- FET is a voltage controlled device.
- FET amplifiers have low gain bandwidth product due to the junction capacitive effects.
- FET has higher switching speeds and cut-off frequencies.
- FET has negative temperature coefficient at high current levels.

4. Write about the broad classification of FET.

Ans. Based on the construction, the FET can be classified into two types as:

a) Junction Field Effect Transistor (JFET)

b) Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

Depending upon the majority carriers, JFET has been classified into two types, namely,

(1) N-Channel JFET with electrons as the majority carriers, and

(2) P-Channel JFET with holes as the majority carriers.

The broad classification of FETs is shown in following figure.

5. why we call FET as a voltage controlled device?

Ans: For a Junction Field Effect Transistor under certain operating conditions, the resistance of the drain-source channel is a function of the gate-source voltage alone and behave as an almost pure ohmic resistor. Maximum drain-source current I_{DSS} and minimum resistance will exist when the gate-source voltage is equal to zero volts (i.e., V_{GS}=0). If the gate voltage is increased (i.e., negatively for N-channel JFETs and positively for P-channel JFETs), the resistance will also increase. When the drain current is reduced to a point where the FET is no longer conductive, the maximum resistance is reached. The voltage at this point is represented as $V_{GS}=V_{GS(OFF)}$.

By changing the voltage applied on the FET's gate pin, the resistance offered by the FET's channel changes and different currents are drawn from the circuit for different values of resistance. Thus, the load current (drain-source current) of a FET is controlled by the voltage applied on the gate pin. Hence, FETs are acts as voltage controlled device.

6. Draw the structure of P – channel JFET and its symbol.

Ans

Structure and Symbol of P-Channel JFET:

The structure and symbol of P-Channel JFET is shown in the figure. The device could be made of P type bar with two N-type gates as shown in the figure. Then this will be P-Channel JFET is similar; the only difference being that in N-Channel JFET the current is carried by the electrons while in P Channel JFET, it is carried by holes.

7. Define JFET Parameters

i) DC drain resistance
ii) AC drain resistance
iii) Transconductance
iv) Amplification factor

Ans: i) DC drain resistance, r_d

It is defined as the ratio of drain to source voltage to drain current by keeping the gate to source voltage constant. The DC drain resistance is given by

$$R_D = \frac{V_{DS}}{I_D}\Big|_{V_{Gs}=Constant}$$

ii) AC drain resistance, r_d

It is defined as the ratio of change in drain to source voltage to the change in drain current at a constant gate to source voltage.

$$r_D = \frac{\Delta V_{DS}}{\Delta I_D}\Big|_{V_{Gs}=Constant}$$

iii) Transconductance

It is defined as the rate of change of drain current with change in gate to source voltage by keeping the drain to source voltage constant. It is denoted by 'g_m'.

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}\Big|_{V_{DS}=Constant}$$

Its units are ampere per volt or mS (milli Siemen). It is also called as mutual conductance.

Fig. Transfer characteristics

Figure shows the graph of I_D versus V_{GS}, from this a relation for g_m can be deduced as,

$$g_m = g_{mo}[1 - \frac{V_{GS}}{V_p}]$$

Where g_{mo} = value of g_m at V_{GS}= 0, is $\frac{-2I_{DSS}}{V_p}$

V_p = Pinchoff voltage.

IV) Amplification Factor, μ

It is defined as the ratio of change in drain to source voltage to change in gate to source voltage keeping the drain current constant.

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}\Big|_{I_D=Constant}$$

The above expression can also be written as,

$$\mu = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\mu = r_D \times g_m$$

where, μ is a unitless quantity.

$r_D = \frac{\Delta V_{DS}}{\Delta I_D}$ = Drain resistance

$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$ = Transconductance

8. What are the differences between BJT and FET?

Ans.

S.NO	Parameter	BJT	FET
1	**Control element**	Current controlled device. Input current I_B controls output current I_C.	Voltage controlled device. Input voltage V_{GS} controls drain current I_D.
2	**Device type**	Current flows due to both, majority and minority carriers and hence **bipolar device**.	Current flows due to only majority carriers and hence **unipolar device**.
3	**Types**	npn and pnp	n-channel and p-channel.
4	**Symbols**	npn pnp	n-channel p-channel
5	**Configurations**	CE, CB, CC	CS, CG, CD
6	**Input resistance**	Less compare to JFET	High compare to BJT.
7	**Size**	Bigger than JFET	Smaller in construction than BJT, thus making them useful in integrated circuits(IC).
8	**Sensitivity**	Higher sensitivity to changes in the applied signals.	Less sensitivity to changes in the applied voltage.
9	**Thermal stability**	Less	More
10	**Thermal runaway**	Exists in BJT, because of cumulative effect of increase in I_C with temperature, resulting increase in temperature in the device.	Does not exist in JFET, because drain resistance r_d increases with temperature, which reduces I_D, reducing the I_D and hence the temperature of the device.
11	**Relation between input and output**	Linear	Non-linear
12	**Ratio of o/p to i/p**	$\beta = \frac{I_C}{I_B}$	$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$
13	**Thermal noise**	More in BJT as more charge carriers cross junctions.	Much lower in JFET as very few charge carriers cross the junction.
14	**Gain bandwidth production**	High	Low

9. Explain how FET acts as a Voltage Variable Resistor?

Ans. FET as a Voltage –Variable Resistor (VVR):

FET is operated in the constant current portion of its output characteristics for the linear applications .In the region before pinch off , where V_{DS} is small the drain to source resistance r_d can be controlled by the bias voltage V_{GS}. The FET is useful as a voltage variable resistor (VVR) or Voltage Dependent resistor(VDR).

In JFET, the drain source conductance $g_d = I_D/V_{DS}$ for small values of V_{DS}, which may be expressed as

$$g_d = g_{do}\left[1-\left(\frac{V_{GS}}{V_P}\right)^{\frac{1}{2}}\right]$$

where g_{do} is the value of drain conductance when the bias voltage V_{GS} is zero.

The variation of the r_d with V_{GS} can be closely approximated by the empirical expression,

$$r_d = \frac{r_0}{1-KV_{GS}}$$

Where r_0 = drain resistance at zero gate bias, and K=a constant, dependent upon FET type.

Thus, small signal FET drain resistance r_d varies with applied gate voltage V_{GS} and FET act like a VARIABLE PASSIVE RESISTOR.

10. what are the biasing schemes available to achieve the required bias in a JFET? Explain any one of the biasing schemes.

Ans: The biasing schemes available to achieve the required bias in JFET are as follows,

i). Fixed bias
ii). Self bias
iii). Voltage divider bias

Fixed bias: The fixed bias circuits are shown in figure.

a)Fixed bias of JFET

b) dc analysis of fixed bias

For the dc analysis assume the capacitors are acts as open circuited and it acts as short circuit for ac analysis.

For the dc analysis assume $I_G \approx 0$. And $V_{RG} = I_G \cdot R_G = 0$ V.

The zero volt drop across R_G permits replacing R_G by a short circuit equivalent. Thus the figure (a) can be redrawn (b).

Applying KVL to the input circuit

$$-V_{GG} - V_{GS} = 0 \text{ or } V_{GS} = -V_{GG} \text{ ---------- (1)}$$

If V_{GG} is fixed then V_{GS} is also fixed in magnitude resulting in fixed bias configuration. The dc levels of voltage V_{GS} and current I_D can be determined as follows.

The drain to source voltage of the can be determined by applying KVL to the output circuit as follows $V_{DS} + I_D R_D = V_{DD}$

Or $V_{DS} = V_{DD} - I_D R_D$ ---------- (2)

We know $V_{DS} = V_D - V_S$ if $V_S = 0$

$V_D = V_{DS}$

Hence from equation (2) we get $I_{DQ} = \frac{V_{DD} - V_D}{R_D}$

In addition $V_{GS} = V_G - V_S$ then $V_{GQ} = V_{GS}$

The graphical analysis of FET biasing as follows

Transfer characteristics of JFET

To locate the operating point, the fixed level of V_{GS} (for fixed bias we provide $V_{GS} = V_{GG}$) has been superimposed on the transfer characteristics (as vertical line). The point where the curves intersect is the commonly referred as Q point. The level of I_D at Q point can be determined from the vertical axis.

11. Explain how do you set a Q-point in a self biased JFET.

Ans:

The self bias configuration of JFET is shown in Figure 10(a). It eliminates the need for two dc supplies. The controlling gate to source voltage V_{GS} is determined by the voltage across the resistor R_S connected in the source terminal.

For the dc analysis the capacitors can be replaced by "open circuits" and the resistor R_G replaced by a short circuit equivalent since $I_G = 0$. The modified circuit shown in Figure 10(b)

The voltage across R_S is $V_{RS} = I_S R_S = I_D R_S$.

Apply the KVL to the closed loop of Figure 10(b)

$$V_{GS} + V_{RS} = 0$$

$$V_{GS} = -V_{RS} = -I_D R_S \qquad (1)$$

In this case V_{GS} is a function of the output current I_D and not fixed in magnitude like fixed bias configuration. The equation (1) and Shockkly equation relates the same two variables I_D and V_{GS}, permitting either a mathematical or graphical solution. The mathematical analysis can be obtained as follows, Shockkly's equation is given by

Figure 10 (a) JFET self bias configuration

Figure 10(b) DC analysis of the self bias configuration

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 = I_{DSS}\left(1-\frac{-I_D R_S}{V_P}\right)^2 = I_{DSS}\left(1+\frac{I_D R_S}{V_P}\right)^2 \qquad (2)$$

The equation (2) can be squared and rearranged as $I_D^2 + K_1 I_D + K_2 = 0$

The quadratic equation can then be solved for the appropriate solution for I_D.

The dc levels of other quantities are determined as follows. Apply KVL to the output circuit.

$$V_{DD} = I_D R_D + I_S R_S + V_{DS} \quad \text{or } V_{DS} = V_{DD} - I_S R_S - I_D R_D$$

but we know $I_D = I_S$ hence

$$V_{DS} = V_{DD} - I_D (R_S + R_D) \quad \text{or } I_D = \frac{V_{DD} - V_{DS}}{(R_S + R_D)}$$

In addition $V_G = 0$ and $V_{DS} = V_D - V_S$

or $V_D = V_{DS} + V_S = V_{DS} + I_D R_S = V_{DD} - I_S R_S - I_D R_D + I_D R_S = V_{DD} - I_D R_D$

thus $V_D = V_{DD} - I_D R_D = V_{DD} - V_{RD}$

In the graphical approach first establish the transfer characteristics of JFET as shown in figure 10(c). The equation (1) line two points are determined by assuming if $I_D = 0$ then $V_{GS} = 0$ (point A) and other point is at $V_{GS} = -I_D R_D$ (Point B). This line will intersect the transfer characteristics of the JFET. This intersecting point is known as "Q point". The values V_{GSQ} and I_Q are measured from the graph from their respective axis.

The biasing of the device should offer some degree of stability to changes in the transistor parameters. Particularly the values of I_{DSS} and V_P. The values can vary as a result of variations in the resistivity of the channel and the thickness of the channel. To obtain the better stability the amplitude of signal being processed is not too large then this change may not be acceptable. But whether maximum amplitude is required then variation I_D and V_{GS} could result in distortion. Thus stability is reduced. To obtain better stability of 'Q' point, voltage divider bias is used.

Figure 10(c) Determining 'Q' point for self bias of JFET

12. Draw and explain a voltage divider bias JFET circuit.
Ans:

The voltage divider bias arrangement is shown in figure 11(a). The basic construction is exactly the same as BJT, but the dc analysis of each is quite different. $I_G = 0$ for FET amplifiers, but the magnitude of I_B for common emitter BJT amplifiers can affect the dc levels of current and voltage in both the input and output circuits. In BJT I_B provides, the link between input and output circuits, similarly V_{GS} will do the same for the FET configuration.

Figure 11(a) Voltage divider bias arrangement

Figure 11(b) DC analysis of voltage divider bias arrangement

For the dc analysis note that, all the capacitors have been replaced by an open circuit. Since $I_G = 0$, it requires that $I_{R1} = I_{R2}$ (refer figure 11(b)) and the resistors R_1 and R_2 can be used to determine level of V_G. Using the potential divider rule V_G can be determined as follows

$$V_G = \frac{V_{DD}R_2}{R_1 + R_2}$$

Apply KVL to the input circuit we get,

$$V_G - V_{GS} - V_{RS} = 0 \quad \text{or} \quad V_{GS} = V_G - V_{RS} = V_G - I_D R_S \quad (1)$$

This result is an equation that continues to include the same two variables appearing in Shockley's equation. "V_{GS} and I_D". The equation (1) is a straight line equation. To plot the straight line in transfer characteristics substitute $I_D = 0$ in eqn (1) for finding the value of V_{GS}

$$V_{GS} = V_G\big|_{\text{if } I_D=0}$$

and to solve I_D substitute $V_{GS} = 0$ in eqn (1)

$$V_{GS} = V_G - I_D R_S$$

$$0 = V_G - I_D R_S \quad \text{or} \quad V_G = I_D R_S$$

or

$$I_D = \frac{V_G}{R_S}\bigg|_{\text{if } V_{GS}=0}$$

The above two points permit the drawing of a straight line to represent equation (1). The intersection of the straight line with the transfer curve in the region to the left of the vertical axis will define the operating point and the corresponding levels of I_D and V_{GS}.

Once the quiescent values are determined, the other values of the circuit are determined as follows.

Apply KVL to the output circuit.

$$V_{DD} = V_{DS} + I_D R_D + I_S R_S$$

We know $I_S \simeq I_D$ hence $V_{DD} = V_{DS} + I_D (R_S + R_D)$

or $$V_{DS} = V_{DD} - I_D (R_S + R_D)$$

$$V_{DS} = V_D - V_S \text{ or } V_D = V_{DS} + V_S$$

Substitute the value of V_{DS} in the above equation

We get $$V_D = V_{DS} + V_S = V_{DD} - I_D R_S - I_D R_D + I_S R_S$$

$$V_D = V_{DD} - I_D R_D$$

$$V_S + ISRS = I_D R_D$$

and $$I_{R1} = I_{R2} = \frac{V_{DD}}{R_1 + R_2}$$

This biasing techniques provides better stability than other methods.

Figure 11 (c) Determination of 'Q' point

13. Compare N-channel with P-Channel FET's and What are the applications of JFET?
Ans:

1. In an N-channel JFET the current carriers are electrons, whereas the current carriers are holes in a P-channel JFET.
2. Mobility of electrons is large in N-channel JFET, mobility of holes is poor in P-channel JFET.
3. The input noise is less in N-channel JFET than that of P-channel JFET.
4. The transconductance is larger in N-channel JFET than that of P-channel JFET.

Applications of JFET

1. FET is used as a buffer in measuring instruments, receivers since it has high input impedance and low output impedance.
2. FET's are used in Radio Frequency amplifiers in FM (Frequency Mode) tuners and communication equipment for the low noise level.
3. Since the input capacitance is low, FET's are used in cascade amplifiers in measuring and test equipments.
4. Since the device is voltage controlled, it is used as voltage variable resistor in operational amplifiers and tone controls
5. FET's are used in mixer circuits in FM and TV receivers, and communication equipments because inter modulation distortion is low.
6. It is used in oscillator circuits because frequency drift is low.
7. As the coupling capacitor is small, FET's are used in low frequency amplifiers in hearing aids and inductive transducers.
8. FET's are used in digital circuits in computers, LSD and a memory circuit because of it is small size.

14. Explain about breakdown mechanisms in semiconductor diodes.

A: **Avalanche breakdown**

- Though reverse current is not dependent on reverse voltage, if reverse voltage is increased, at a particular value, velocity of minority carriers increases.
- Due to kinetic energy associated with the minority carriers, more minority carriers are generated when there is collision of minority carriers with the atoms.
- The collision makes the electrons to break the covalent bonds.
- These electrons are available as minority carriers and get accelerated due to high reverse voltage.
- They again collide with another atoms to generate more minority carriers. This is called ***carrier multiplication***.
- Finally large number of minority carriers move across the junction, breaking the p-n junction.
- These large number of minority carriers give rise to a very high reverse current.
- This effect is called ***avalanche effect*** and the mechanism of destroying the junction is called reverse breakdown of a p-n junction.
- The voltage at which breakdown of a p-n junction occurs is called ***reverse breakdown voltage.***

Zener breakdown

- When a p-n junction is heavily doped the depletion region is very narrow. So under reverse bias conditions, the electric field across the depletion layer is very intense.
- Such an intense field is enough to pull the electrons out of the valance bands of the stable atoms.
- So this is not due to the collision of carriers with atoms.
- Such a creation of free electrons is called zener effect.
- These minority carriers constitute very large current and mechanism is called zener breakdown.

15 Explain about Zener diode and its characteristics. How it works as a voltage regulator.

A **Zener diode**

- The diodes designed to work in breakdown region are called zener diode.
- It is heavily doped than ordinary diode.
- Operates in reverse breakdown region.
- It can be used as voltage regulator.
- When biased in the forward direction it behaves just like a normal signal diode passing the rated current, but when a reverse voltage is applied to it the reverse saturation current remains fairly constant over a wide range of voltages.
- The reverse voltage increases until the diodes breakdown voltage VB is reached at which point a process called *Avalanche Breakdown* occurs in the depletion layer and the current flowing through the zener diode increases dramatically to the maximum circuit value (which is usually limited by a series resistor). This breakdown voltage point is called the "zener voltage" for zener diodes.

- The point at which current flows can be very accurately controlled (to less than 1% tolerance) in the doping stage of the diodes construction giving the diode a specific *zener breakdown voltage*, (Vz) ranging from a few volts up to a few hundred volts.
- This zener breakdown voltage on the I-V curve is almost a vertical straight line.
- The **Zener Diode** is used in its "reverse bias" or reverse breakdown mode, i.e. the diodes anode connects to the negative supply.
- From the I-V characteristics curve above, we can see that the zener diode has a region in its reverse bias characteristics of almost a constant negative voltage regardless of the value of the current flowing through the diode and remains nearly constant even with large changes in current as long as the zener diodes current remains between the breakdown current I_Z(min) and the maximum current rating I_Z(max).

- **Zener Diode Regulator**
- This ability to control itself can be used to great effect to regulate or stabilise a voltage source against supply or load variations.
- The fact that the voltage across the diode in the breakdown region is almost constant turns out to be an important application of the zener diode as a voltage regulator.
- The function of a regulator is to provide a constant output voltage to a load connected in parallel with it in spite of the ripples in the supply voltage or the variation in the load current and the zener diode will continue to regulate the voltage until the diodes current falls below the minimum I_Z(min) value in the reverse breakdown region.

- A zener diode is always operated in its reverse biased condition.
- A voltage regulator circuit can be designed using a zener diode to maintain a constant DC output voltage across the load in spite of variations in the input voltage or changes in the load current.
- The zener voltage regulator consists of a current limiting resistor RS connected in series with the input voltage VS with the zener diode connected in parallel with the load RL in this reverse biased condition.
- The stabilized output voltage is always selected to be the same as the breakdown voltage V_Z of the diode.

16. Explain about tunnel diode and its V-I characteristics with the help of energy band diagrams

A **Tunnel diode**

AC equivalent ckt

- A normal pn-junction has an impurity concentration of about 1 part in 10^8. With this amount of doping, the width of depletion layer, which constitutes the potential barrier of the junction, is of the order of 5 microns (5x10-4 cm).
- If the concentration of impurity atoms is greatly increased, say 1 part in 103 the device characteristics are completely changed. The new diode was announced in 1958 by Leo Esaki. This diode is called 'Tunnel diode' or 'Esaki diode'.
- The barrier potential V_B is related with the width of the depletion region with the following equation.

$$V_B = \frac{q N_A}{2 \in} . \omega^2 \qquad \Rightarrow \omega^2 = \frac{2 V_B \in}{q N_A}.$$

- From the above equation the width of the barrier varies inversely as the square root of impurity concentration.
- As the depletion width decreases there is a large probability that an electron will penetrate through the barrier. This quantum mechanical behavior is referred to as tunneling and hence these high impurity density pn-junction devices are called Tunnel diodes. This phenomenon is called as 'tunneling'.

The volt-ampere characteristic:

If a reverse bias voltage is applied to the tunnel diode, the height of the barrier is increased above the open-circuit value E_O. Hence the n-side levels must shift downward with respect to the p-side levels as shown in the figure below.

Fig. Under applied reverse bias

We now observe that there are some energy states in the valance band of the p-side which lie at the same level as allowed empty states in the conduction band of the n-side. Hence these electrons will tunnel from the p to the n-side, giving rise to a reverse diode current. As the magnitude of the reverse bias increase, causing the reverse current to increase.

Consider if a forward bias is applied to the diode so that the potential barrier is decreased below Eo. Hence the n-side levels must shift upward with respect to those on the p-side.
The energy band diagrams for a heavily doped under forward bias conditions are shown in figure below.

Fig. As the bias is increased, the band structure changes progressively from (a) to (d).

From fig (a) we can observe that the electrons will tunnel from the n to the p material giving rise to the forward current. As the forward bias is increased further, the maximum number of electrons can leave from occupied states on the right side of the junction, and tunnel through the barrier to the empty states on the left side of the junction giving rise to the peak current Ip. If still more forward bias is applied, fig© is obtained and the tunneling current decreases. Finally if the forward bias is larger there is no9 empty allowed states on one side of the junction at the same energy as occupied states on the other side, the tunneling current must drop to zero. The V-I characteristics of tunnel diode is shown in fig.

Fig.-I Characteristics of a tunnel diode.

The tunnel diode exhibits a negative resistance characteristics between peak current Ip and valley current Iv. The tunnel diode is excellent conductor in the reverse bias conditions. By applying small forward bias voltage to the tunnel diode the current increases and reaches to the maximum level. The maximum for small forward bias voltage is called as 'peak current (Ip)'.The corresponding voltage to the peak current is called 'peak voltage (Vp)'.

If forward bias voltage is increased beyond the peak voltage the current starts decreasing and reaches to the maximum level. This minimum value of the current is called as "valley current (Iv)". The corresponding voltage to the valley current is called as "valley voltage (Vv)". If forward bias voltage is increased beyond valley voltage it exhibits the same characteristics as ordinary diode.

Applications of Tunnel diode:

1. It is used as a very high speed switch, since tunneling takes place at the speed of light.
2. It is used as a high frequency oscillator.

17. Explain the principle of varactor diode and list out the applications.

Ans

- Also called Varicap, epicap, voltage variable capacitance(VVC), tuning diodes.
- It can be operated under reverse biased condition.
- We know that the transition capacitance c(t) is given by c(t)= εA/W
- As the transition capacitance varies with the applied voltage, it can be used as a voltage variable capacitance in many applications.

The voltage- variable nature of transition capacitance of reverse-biased pn- junction may be utilized in several applications such as

1) In voltage tuning of an LC resonant.
2) Self balancing bridge circuits.
3) In parametric amplifiers etc.
4) FM radio and TV receivers, AFC circuits.
5) Used in adjustable band pass filters.

- Varactor diode symbol and circuit models are shown below.

Rs: Body series resistance.

C(t): Barrier capacitance.

R_r : Reverse diode resistance.

Typically, at a reverse bias of 4v,

C(t)= 20pF, R(s)=8.5 ohms, R(r)>1M (usually neglected).

18. Explain the working principle of SCR with suitable diagrams.
Ans:

SCR(Silicon Controlled Rectifier)

- It is an unidirectional device like diode, it allows to flow current in only one direction. But unlike diode, it has a built in features to switch ON and OFF.
- It is a 4 layer pnpn device where p & n layers are alternatively arranged. The outer layers are heavily doped.
- It has 3 terminals anode, cathode, gate and 3 p-n junctions called J_1, J_2 and J_3.
- The switching of SCR is controlled by the additional input called gate.

(a) Basic Structure (b) Circuit symbol

Fig, Basic structure and circuit symbol of SCR.

Operation of SCR:
The operation of SCR is divided into two categories,

i) When gate is open:
Consider that the anode is positive with respect to cathode and gate is open. The junctions J1 and J3 are forward biased and junctions J2 is reverse biased. There is depletion region around J2 and only leakage current flows which is negligibly small. Practically the SCR is said to be 'OFF'. This is called forward blocking state of SCR and voltage applied to anode and cathode with anode positive is called *forward voltage.* This is shown in figure (a) below.

With gate open, if cathode is made positive with respect to anode, the junctions J1, J3 become reverse biased and J2 forward biased. Still the current flowing is leakage current, which can be neglected as it is very small. The voltage applied to make cathode positive is called reverse voltage and SCR is said to be in reverse blocking state. This is shown in the figure (b) below.

(a) J_1, J_3 Reverse biased.
J_2 Forward biased.

Fig. Operation of SCR when gate is open (a), (b).

2. When gate is closed:

Consider that the voltage is applied between gate and cathode when the SCR is in forward blocking state. The gate is made positive with respect to the cathode. The electrons from n-type cathode, which are majority in number, cross the junction J3 to reach to positive of battery.

While holes from p-type move towards the negative of battery. This constitutes the gate current. This current increases the anode current as some of the electrons cross junction J2. As anode current increases, more electrons cross the junction J2 and the anode current further increases. Due to regenerative action, within short time, the junction J2 breaks and SCR conducts heavily. The connections are shown in the figure. The resistance R is required to limit the current.

Once the SCR conducts, the gate loses its control.

Fig. Operation of SCR when gate is closed.

Characteristics of SCR:

The characteristics are divided into two sections:

i) Forward characteristics

ii) Reverse characteristics

i) Forward characteristics:

It shows a forward blocking region, when I_G=0. It also shows that when forward voltage increases up to V_{BO}, the SCR turns ON and high current results. It also shows that, if gate bias is used then as gate current increases, less voltage is required to turn ON the SCR.

If the forward current falls below the level of the holding current I_H, then depletion region begins to develop around J_2 and device goes into the forward blocking region.

When SCR is turned on from OFF state, the resulting forward current is called *latching current* I_L. The latching current is slightly higher than the holding current.

ii) Reverse characteristics:

If the anode to cathode voltage is reversed, then the device enters into the reverse blocking region. The current is negligibly small and practically neglected.

If the reverse voltage is increases, similar to the diode, at a particular value avalanche breakdown occurs and a large current flows through the device. This is called reverse breakdown and the voltage at which this happens is called reverse breakdown voltage

Fig. Characteristics of SCR.

Two Transistor Analogy:

The easiest way to understand how SCR works it ot visualize it separately into two halves, as shown in the figure. The left half is a p-n-p transistor and right half is n-p-n transistor. This is also called two transistor model of SCR.

The collector current of T1 becomes base current of T2 and collector current of T2 becomes base current of T1.

Fig, Two transistor model of SCR.

Problems

Problem1

When a reverse gate voltage of 12 V is applied to JFET, the gate current is 1 nA. Determine the resistance between gate and source.

Solution: $V_{GS} = 12$ V, $I_G = 10^{-9}$ A.

Therefore, gate-to-source resistance $= \dfrac{V_{GS}}{I_G} = \dfrac{12}{10^{-9}} = 12{,}000\ \text{M}\Omega$

Problem2

When the reverse gate voltage of JFET changes from 4.0 to 3.9 V, the drain current changes from 1.3 to 1.6 mA. Find the value of transconductance.

Solution: $\Delta V_{GS} = 4.0 - 3.9 = 0.1$ V

$\Delta I_D = 1.6 - 1.3 = 0.3$ mA

Therefore, transconductance, $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}} = \dfrac{0.3 \times 10^{-3}}{0.1} = 3$ m mho .

Problem3

A FET has a driven current of 4 mA. If $D_{SS} = 8$ mA and $V_{GS(off)} = -6$ V. Find the values of V_{GS} and V_P.

Solution:

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

$$4 = 8\left[1 + \frac{V_{GS}}{6}\right]^2$$

$$1 + \frac{V_{GS}}{6} = \sqrt{\frac{4}{8}} = \frac{1}{\sqrt{2}} = 0.707$$

Therefore, $V_{GS} = -1.76$ V

$V_P = |V_{GS(off)}| = 6$V

Problem4

An N-channel JFET has $I_{DSS} = 8$ mA and $V_p = -5$ V. Determine the minimum value of V_{DS} for pinch-off region and the drain current I_{DS}, for $V_{GS} = -2$ V in the pinch-off region.

Solution: The minimum value of V_{DS} for pinch-off to occur for $V_{GS} = -2$ V is

$$V_{DSmin} = V_{GS} - V_P = -2 - (-5) = 3\text{V}$$

$$I_{DS} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$= 8 \times 10^{-3}\,[1 - (-2)/(-5)]^2 = 2.88 \text{ mA}$$

Problem5

A FET has a drain current of 4mA. If I_{DSS} = 8mA and V_{GS} off = -6V. Find values of V_{GS} and V_P.

Given IDS = 4 mA
IDSS = 8mA
V_{GSoff} = - 6V.
Ans: (i) VP = V_{GSoff} = -6V = 6V.

(ii) $I_{DS} = I_{DSS}\left[1-\frac{V_{GS}}{V_p}\right]^2$

$4\times10^{-3}=8\times10^{-3}\left[1-\frac{V_{GS}}{6}\right]^2$

$\frac{1}{2} = \left[1-\frac{V_{GS}}{6}\right]^2$

V_{GS}= 6 0.293 1.758 Volts

Problem6.

The readings obtained from a JFET are as follows: -

Drain to source voltage (volts) = 5 12 12
Gate to source voltage (volts) = 0 0 -0.25
Drain current Id (mA) = 8 8.2 7.5
Determine (i) AC drain resistance (ii) TransConductance (iii) Amplification Factor

SOL:

(i) **Ac Drain Resistance** = $r_D = \frac{\Delta V_{DS}}{\Delta I_D}\Big|_{V_{Gs}=Constant}$

$= \frac{12-5\ (\text{Volts})}{8.2-8(\ \text{mA})} = \frac{7}{0.2\times10^{-3}} = 35\ \text{K}\Omega.$

(ii) **Transconductance** = $\frac{\Delta I_D}{\Delta V_{GS}}\Big|_{V_{DS}=Constant} = \frac{8.2-7.5}{0-(-0.25)} = \frac{0.7\text{mA}}{0.25} = 2.8\text{m}\mho$

(iii) **Amplification Factor,** $\mu = r_D \times g_m$ = 2.8 x 10^{-3} x 35x 10^3 = 98

BEE Regular

SET - 1	GR 11	CODE: GR11A05

I B. Tech I Semester Examinations, February, 2012

BASIC ELECTRICAL & ELECTRONICS ENGINEERING

(Common to EEE, ECE, CSE,BME,IT)

Time: 3 hours **Max Marks: 75**

Answer any FIVE questions

All questions carry equal marks

*****

1.(a) Explain the Following terms **[8]**

(i) Independent source & Dependent source

(ii) KVL & KCL

(iii) Source Transformation

(iv) Passive Element

(b) A 60 Hz, Voltage of 110 V(rms) is impressed on a 150 ohms resistance **[7]**

(i) Write the time equation for the voltage and resulting current.

(ii) Show the voltage and current on a time diagram

(iii) Show the voltage and current on a phasor diagram

2.(a) A Series RLC circuit has R=5 ohms, L=40 mH, C=1 μ Farads. Calculate **[8]**

(i) Q of the circuit

(ii) Band Width

(iii) Resonance frequency

(iv) Half power frequencies.

(b) State the Thevenin's theorem. Obtain the Thevenin's equivalent circuit across A and B for the circuit shown in ***Fig.1*** **[7]**

Fig. 1

SET - 1	GR 11	CODE: GR11A05

3.(a) Explain the Diode specifications and Give the equivalent circuits of [8]
(i) Ideal Diode
(ii) Simplified Diode
(iii) Piece wise linear model.

(b) A half-Wave rectifier is fed by 220 v, 50 Hz via a step down transformer of turns ratio 11:1. Find (i) Output DC (ii) Peak Inverse Voltage. [7]

4.(a) Sketch and explain input and output characteristics of common emitter (CE) configuration of Bipolar transistor. [8]

(b) What is meant by Bias Stabilization? Derive an expression for stability factor. [7]

5.(a) How does FET behave [8]
(i) For small drain source voltages (ii) For large drain source voltages .

(b) Draw the characteristic curves of Zener diodes and explain their salient features [7]
.

6.(a) Explain star- delta transformation used for analysing electrical circuit. [8]

(b) Explain Tellegen's theorem with suitable example. [7]

7.(a) What is ripple factor? Arrive at an expression for the ripple factor of a full-wave rectifier with π section filter [8]

(b) Explain the principle of varicap diode and list out the applications. [7]

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Note: Second Semester Class Work Start From 13-02-2012(Monday)

BEE Supply 09-07-12

SET - 1 | GR 11 | CODE: GR11A1005

I B. Tech I Semester Examinations, June / July, 2012
BASIC ELECTRICAL & ELECTRONICS ENGINEERING
(Common to BME, EEE, ECE, CSE, IT)

Time: 3 hours | Max Marks: 75

Answer any FIVE questions

All questions carry equal marks

*****

1 a) State and explain with suitable examples Kirchhoff's current law and voltage law. 8 Marks

b) Find the branch currents I_1, I_2, I_3 using mesh analysis for the circuit shown in the figure 7 Marks

2 a) State and explain Thevenin's theorem 8 Marks

b) Find the Norton's equivalent circuit across a and b for the circuit shown in the figure 7 Marks

3 a) Draw the circuit of a single phase bridge rectifier. Explain how it converts a.c to d.c. 8 Marks

b) Derive an expression for ripple factor of a bridge rectifier with resistive load. 7 Marks

SET - 1 | GR 11 | CODE: GR11A1005

4 a) Explain by drawing relevant circuits the types of bias for BJT amplifiers. 8 Marks

b) Find the stability factor for the circuit shown in the figure 7 Marks

5 a) Draw the output and transfer characteristics of a JFET and explain how you will find μ, r_p, and g_m, from these characteristics. 8 Marks

b) The readings obtained from an experiment of a JFET are as follows: 7 Marks

Drain to source voltage	5	12	12
Gate to source voltage	0	0	-0.25
Drain current	8	8.2	7.5

6 a) Define the terms : i) Power Factor, ii) Impedance, iii) Admittance, iv) Phasor 8 Marks

b) Obtain the power supplied by the source for circuit shown in the figure 7 Marks

7 a) Explain with suitable circuits how a zener diode works as a voltage regulator 8 Marks

b) Compare BJT and JFET 7 Marks

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Regular

SET - 2 | GR 11 | CODE: GR11A1005

I B.Tech I Semester Examinations, January / February - 2013

Basic Electrical and Electronics Engineering

(Common to EEE, ECE, CSE, IT, BME)

Time: 3 hours **Max Marks: 75**

Answer any FIVE questions
All questions carry equal marks
*****

1 a) Determine the voltage Vab across the terminals a,b of the network shown in fig 1(a). **8 Marks**

fig 1(a)

b) Find current through capacitor ic(t) in the circuit shown in the fig 1(b). Assume circuit is not energized at t=0˙ **7 Marks**

fig 1(b)

2 a) **Answer the following** **8 Marks**

(i)Define antiresonant frequency of a parallel tuned circuit and quality factor of an inductor in terms of energy.

(ii) A circuit having a resistance of 5Ω, an inductance of 0.4H and a variable capacitance in series is connected across a 230V, 50Hz supply. *Determine (a) the value of capacitance; (b) the voltage across inductance and capacitance and (c) Q-factor of the circuit.*

b) State Tellegen's theorem and comment. Calculate the load current I in the circuit shown in the fig 2(b) by using Millman's theorem. **7 Marks**

fig2(b)

3 a) With the help of energy diagrams, explain the formation of PN junction and depletion region. **8 Marks**

b) Determine the ripple factor for filtered bridge rectifier with a load as shown in the fig 3(b). **7 Marks**

4 a) Explain with mathematical equations, how a transistor acts as an amplifier. The transistor shown in fig 4(a) has the following ratings: $P_{D(max)}$=800mW ; $V_{CE(max)}$=15V; $I_{C(max)}$=100mA. Determine the maximum value to which Vcc can be adjusted without exceeding a rating. Which rating would be exceeded first? **8 Marks**

b) Draw the circuit diagram of collector to base feedback bias arrangement and analyse. Calculate the Q-point values (I_c, V_{CE}) for the circuit shown below in fig 4(b). **7 Marks**

5 a) For JFET in fig 5(a), Vp = 4V = pinchoff voltage and I_{DSS}=12mA. Determine the maximum value of V_{DD} required to put the device in the constant current area of operation. Given $V_{GS(off)}$= -4V. **8 Marks**

fig 5(a)

b) Explain the V-I characteristic of a tunnel diode with the help of energy band diagrams. **7 Marks**

6 a) Find the equivalent resistance between the terminals 1 and 2 of the network shown in fig 6(a). **8 Marks**

fig 6(a)

b) Derive expressions for diffusion and transition capacitances of a BJT **7 Marks**

7 a) Define h-parameters for CC configuration of a BJT. Derive expressions for R_i , A_I , A_v and R_o in terms of CE h-parameters. **8 Marks**

b) Explain with constructional details, the operation and V-I characteristic of a Varactor diode. Mention its applications. **7 Marks**

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