BG96 Reference Design

LTE Module Series

Rev. BG96_Reference_Design_Rev.B

Date: 2017-05-05

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About the Document

History

Revision	Date	Author	Description
A	2017-02-09	Lyndon LIU/ Lorry XU	Initial
B	2017-05-05	Lyndon LIU	1. Added the design of I2S, I2C and UART3/SPI interfaces in Sheet 1. 2. Modified the circuit design of USB_BOOT in Sheet 1. 3. Added power supply design for audio codec circuits in Sheet 2. 4. Modified the block diagram of DC-DC Application in Sheet 2. 5. Modified the circuit design of STATUS in Sheet 2. 6. Added UART3 level translator circuit (Transistor Solution) in Sheet 4. 7. Added the design of SPI and GPIO interfaces in Sheet 6. 8. Added audio codec design circuit in Sheet 7.

Contents

1 Reference Design

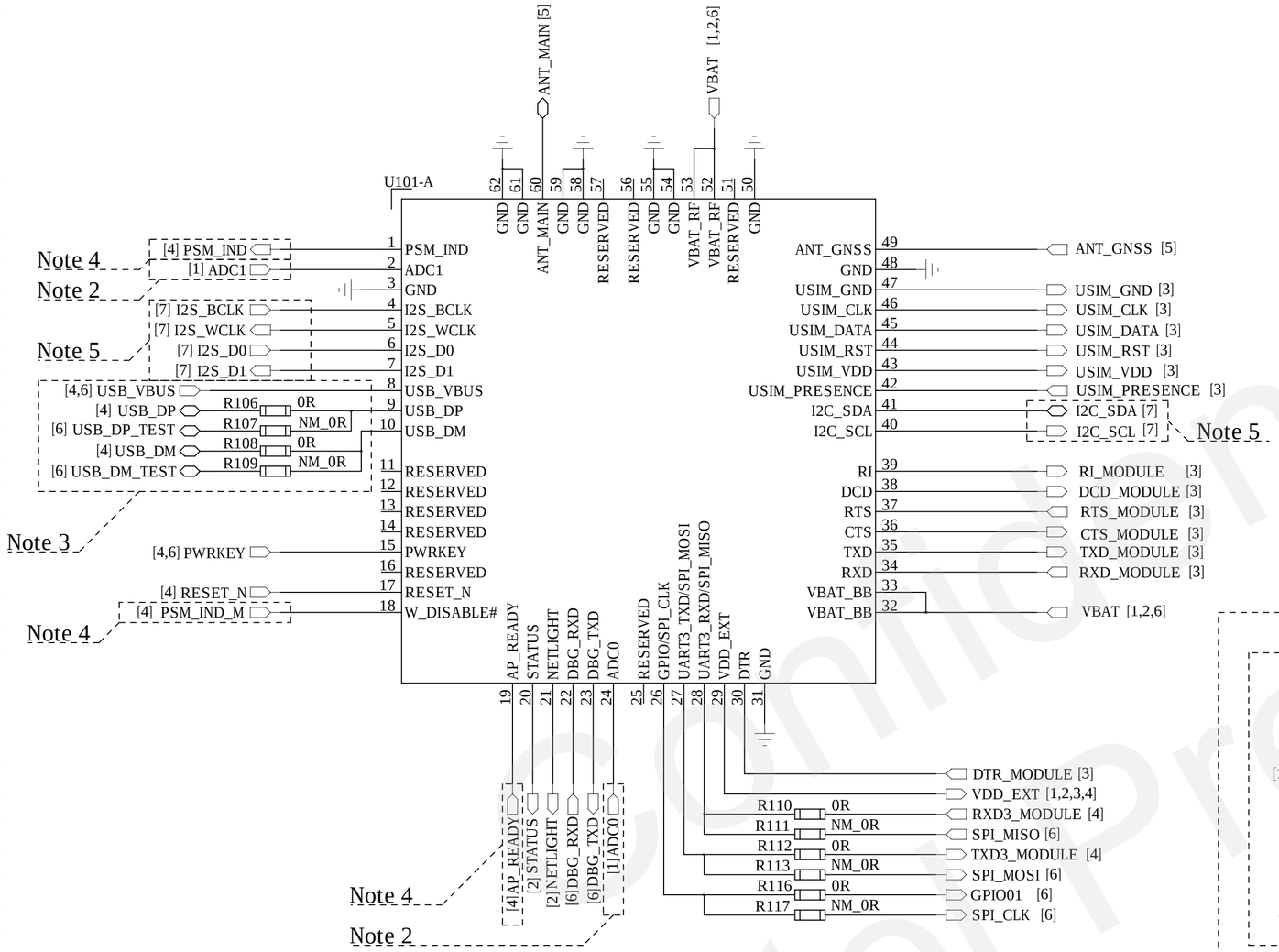
1.1. Introduction

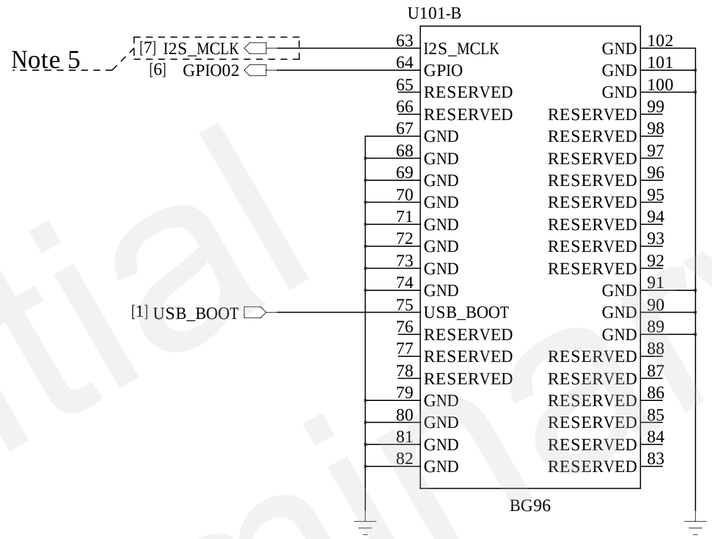
This document provides the reference design for Quectel BG96 module.

1.2. Schematics

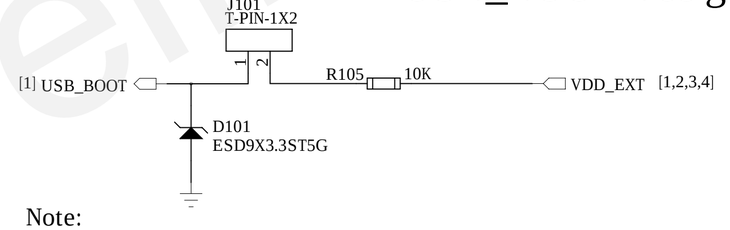
The schematics illustrated in the following pages are provided for your reference only.

Module Interface



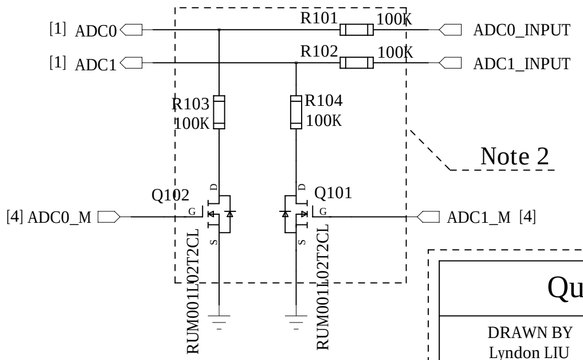


USB_BOOT Design



Note:
When USB_BOOT is at high level, the module will be forced to be in download mode.

ADC Design



Notes:
1. Keep all RESERVED and unused pins unconnected, and all GND pins should be connected to ground.
2. ADC pin can not be directly connected to the power supply and must not exceed the voltage range.
   Power saving can be realized through using ADCx_M signal to control ADC sampling.
3. It is recommended to reserve the test points for upgrading the firmware over USB interface and minimize the stub length of USB test signals.
4. The funcitons of PSM_IND, W_DISABLE# and AP_READY pins are under development.
5. I2S and I2C funtions are used together for Audio Codec design.
   I2S function is under developing by Qualcomm.
6. The STATUS is an open drain output pin, and its drive current is less than 1mA.
7. The pins 26~28 are multi-funtion pins. They can be configured as UART3 or SPI function.

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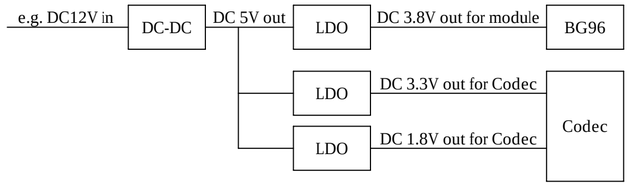
Power Supply Design

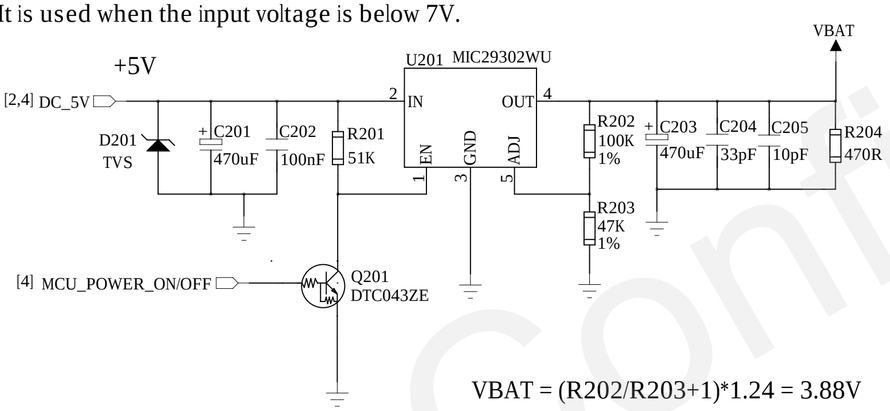
DC-DC Application

It is used when the input voltage is above 7V. First use a DC-DC converter to convert the high input voltage into a 5V output, and then the LDO will generate a 3.8V typical voltage for the module.



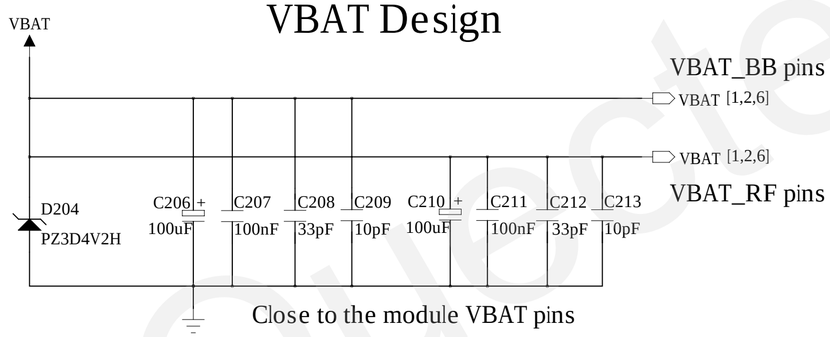
LDO Design

It is used when the input voltage is below 7V.



VBAT = (R202/R203+1)*1.24 = 3.88V

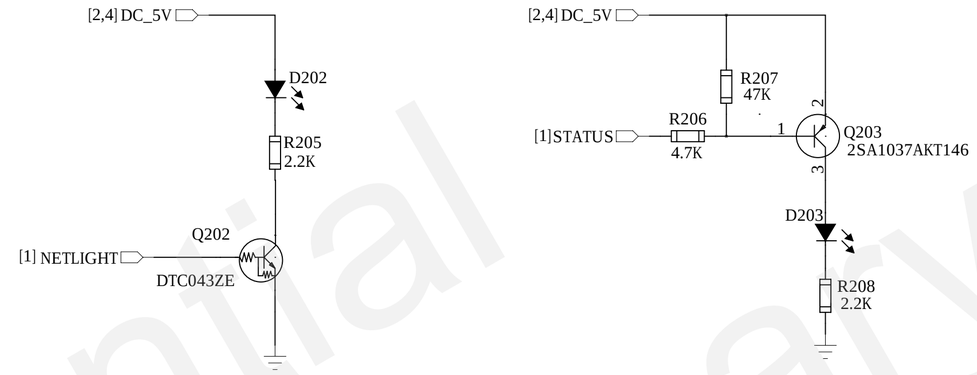
VBAT Design



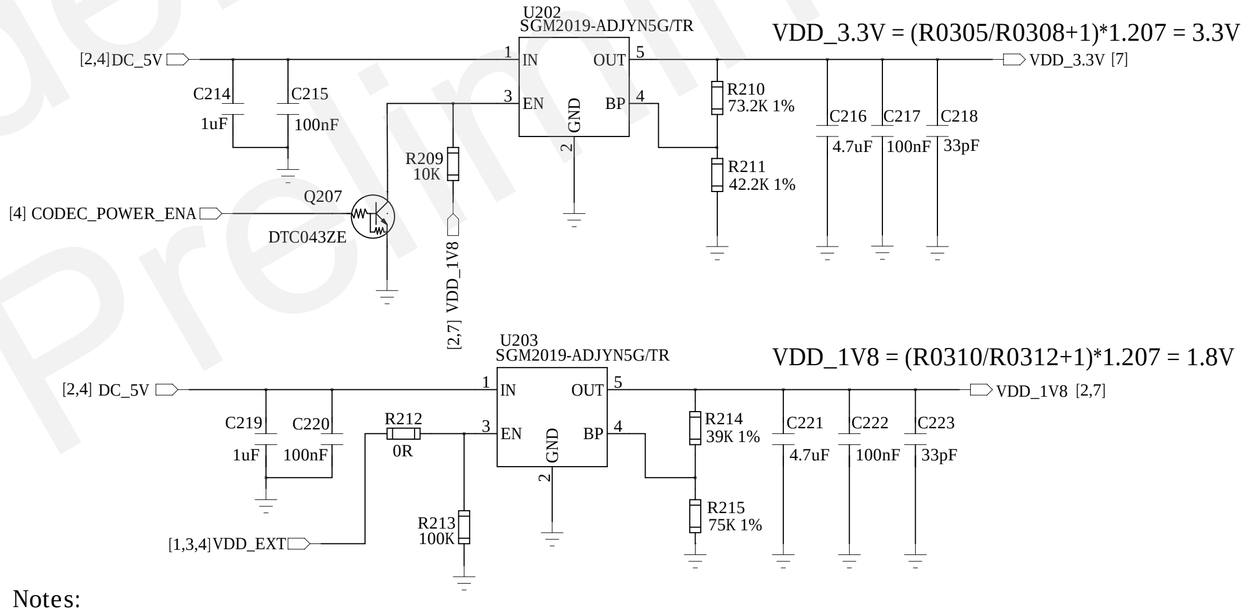
Close to the module VBAT pins

Note:
VBAT should be routed in star mode to VBAT_BB and VBAT_RF pins.

Indicators



Power Supply for Audio Codec



Notes:

1. CODEC_POWER_ENA must be at low level in order to ensure the normal output voltage of VDD_3.3V. If VDD_3.3V power supply needs to be switched off, please keep CODEC_POWER_ENA at high level.
2. To ensure that ALC5616 works normally, please follow the power ON and OFF sequences of its power supply.
   Power ON Sequence: power on VDD_1V8 first, and then VDD_3V3.
   Power OFF Sequence: power off VDD_3V3 first, and then VDD_1V8.

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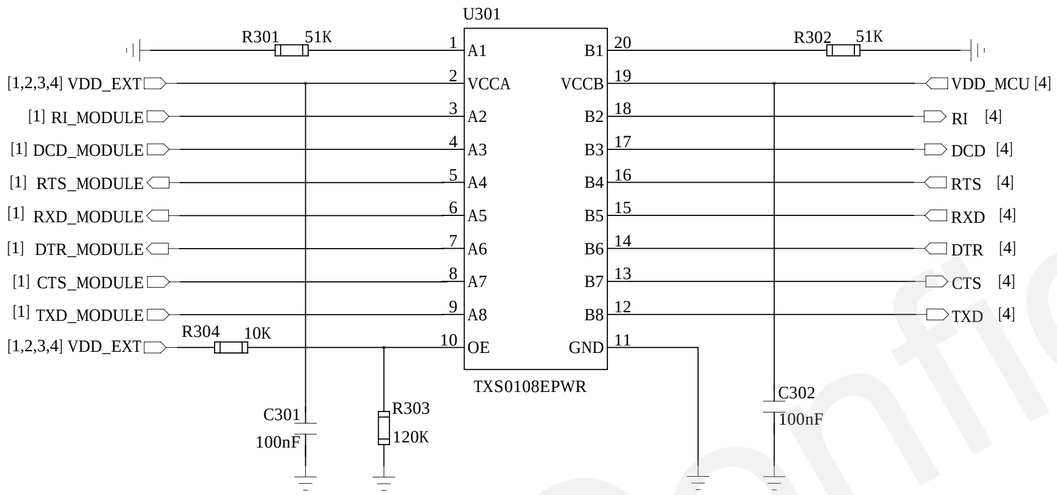
UART and (U)SIM Designs

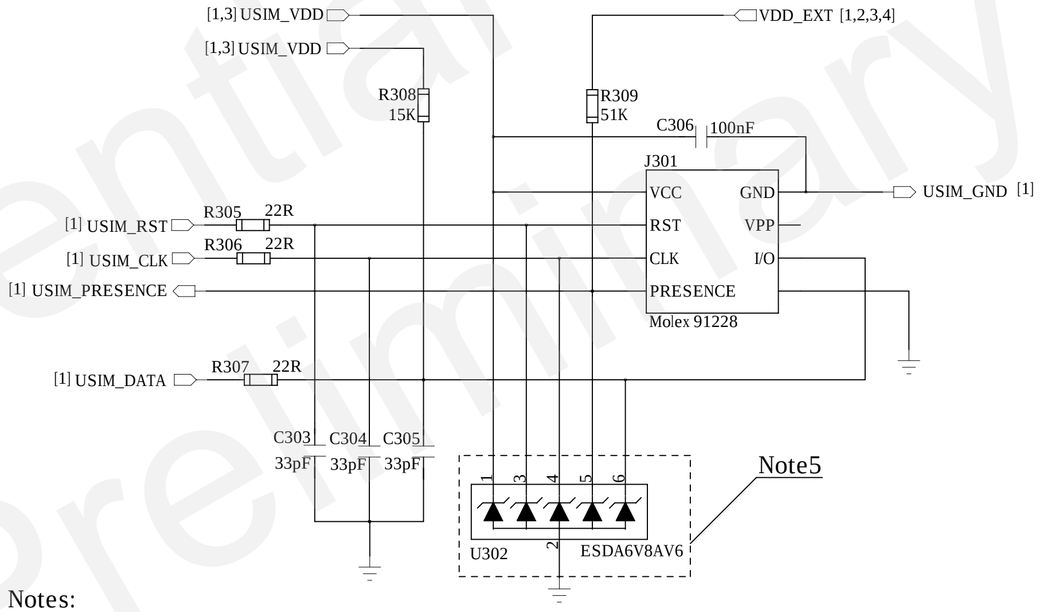
UART Level Translator



Notes:

1. TXS0108EPWR is used to realize the voltage level translation between BG96 and MCU.
2. This circuit is available for BG96 UART voltage level translation design.
3. VCCA should not exceed VCCB. For more information about TXS0108EPWR, please refer to the datasheet from TI website.
4. DTR is pulled up by software. Driving DTR to low level wakes up the module.

(U)SIM Design



Notes:

1. R305~R307 are applied to suppress the EMI spurious transmission and enhance the ESD protection.
2. R308 can improve anti-jamming capability of the (U)SIM circuit.
3. BG96 supports (U)SIM card hot-plugging, which can be implemented through USIM_PRESENCE pin. The circuit above is designed for low-level detection.
4. The value of C306 should be less than 1uF.
5. Parasitic capacitance of the ESD array should not exceed 50pF.

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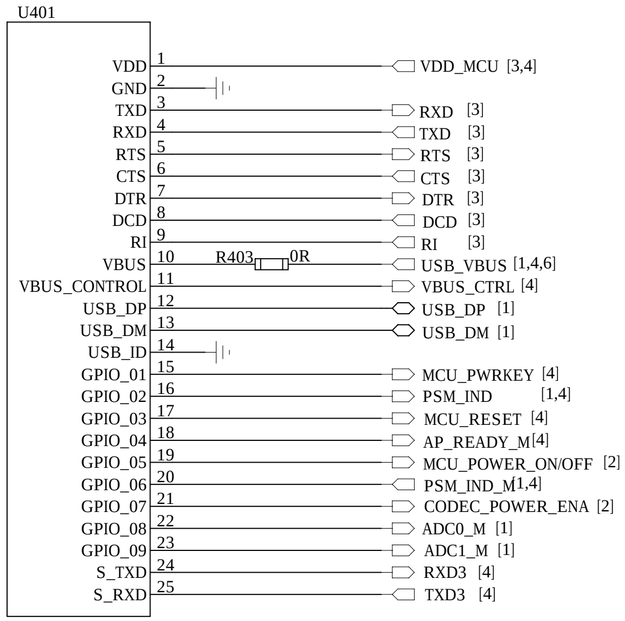
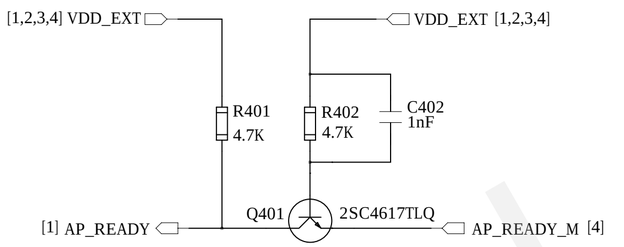
MCU Interface

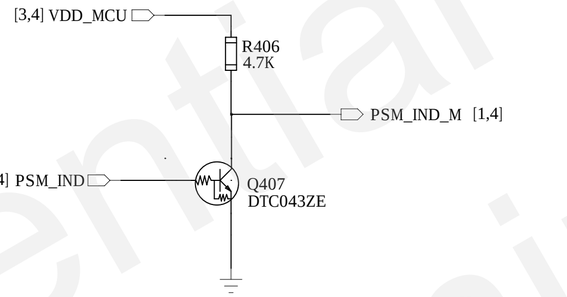


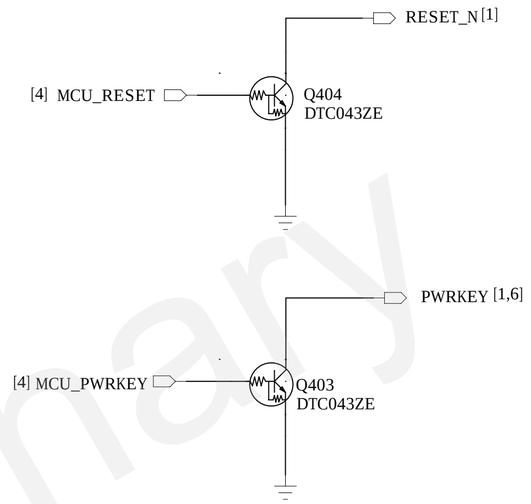
Notes:

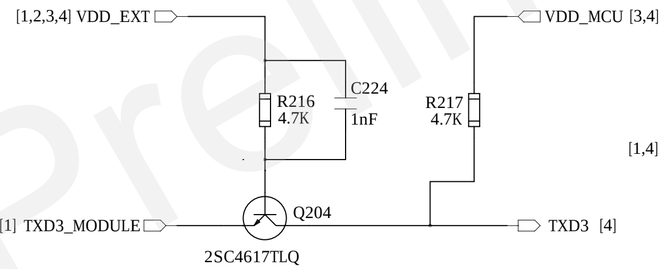
1. U401 represents customer's MCU.
2. Pay attention to the UART connection of RTS/CTS.
3. BG96 can only work as a USB device and supports FS/HS mode.
   To communicate with USB interface, MCU needs to support USB host or OTG function.
   The USB interface is primarily used for AT command communication, data transmission, software debugging and firmware upgrade.
   The USB_VBUS pin of UG96 is used for USB detection, and VBUS_CTRL powers on and off VBUS.

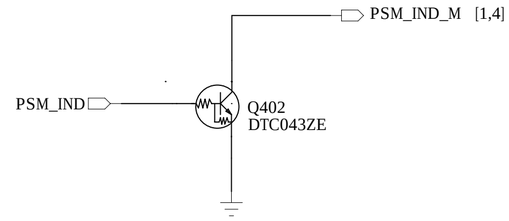
VBUS_CTRL = High level, Q408 is turned on.

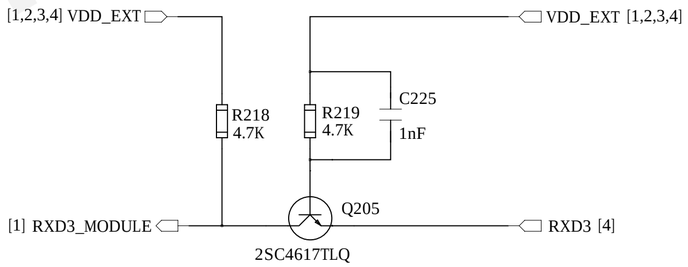












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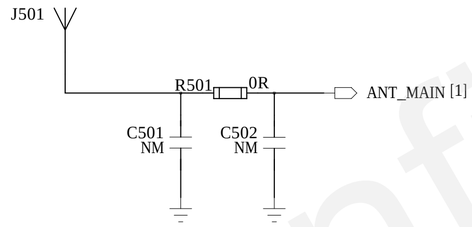
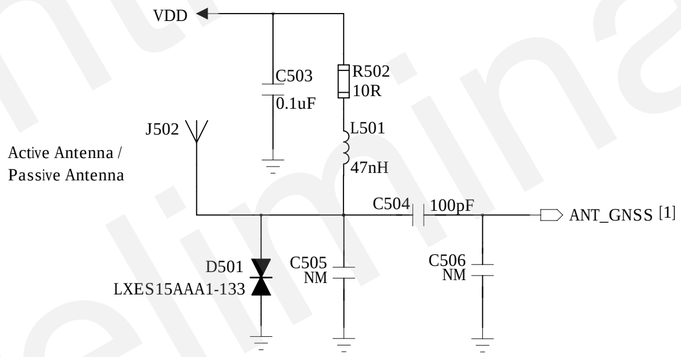
RF and GNSS Design

Main Antenna Interface



GNSS Antenna Interface



Notes:

1. The main antenna circuit is recommended to use a PI type circuit, which is convenient for subsequent debugging.
2. An external LDO can be selected to supply power according to the active antenna requirement.
3. If the module is designed with a passive antenna, then R502 and L501 are not needed.
4. ESD protection devices should be added to the GNSS antenna interface, and the parasitic capacitance should be less than 0.05pF.

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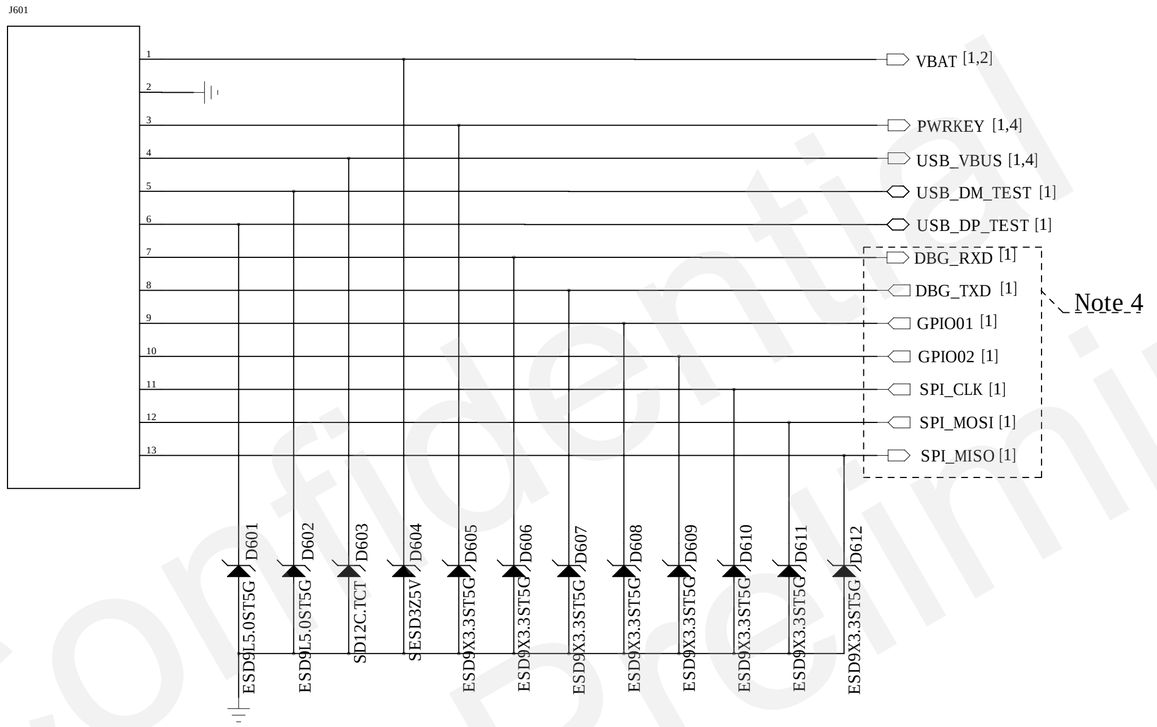
Test Points

Reserved Test Points



Notes:

1. Both USB and UART2 interfaces are reserved for software debugging.
2. USB interface also can be used to upgrade firmware.
3. Keep USB test points as close as possible to USB pins.
   Junction capacitance of ESD protection components on USB data lines might influence the signal. Please pay attention to it. Typically, the capacitance should be less than 1pF.
4. The voltage level of UART2, GPIO and SPI interfaces is 1.8V.
   Do not connect them directly to a 3.3V level.

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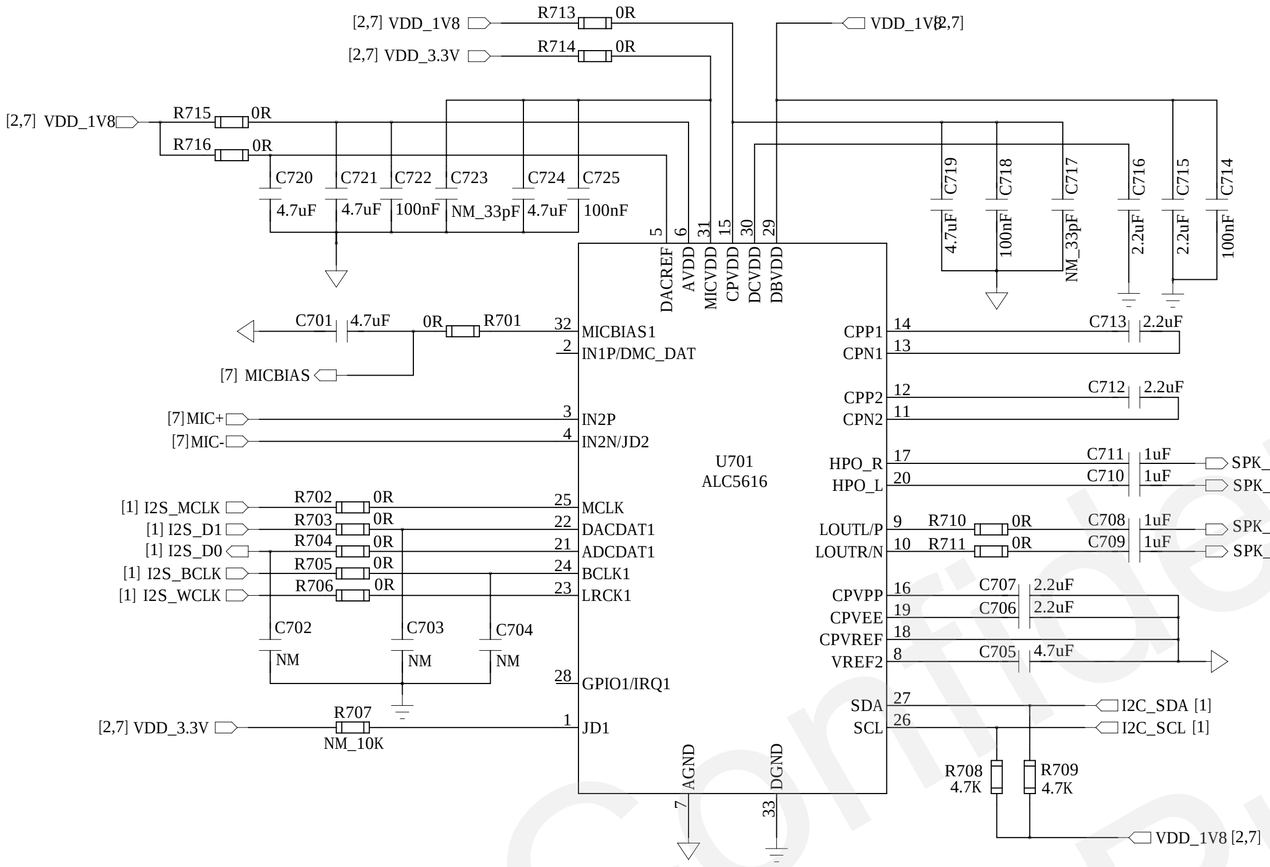
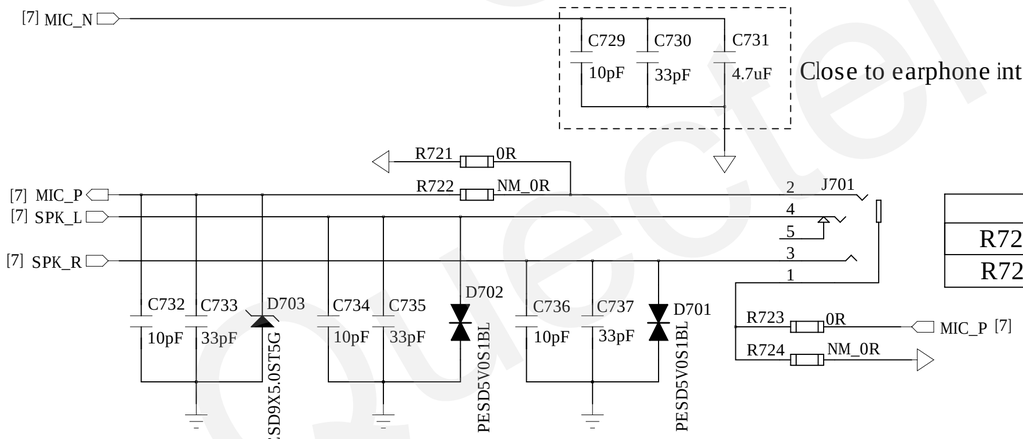
Audio Design



Notes:

1. The analog ground and digital ground of audio codec must be separated first and then connected together at a distant end, so as to avoid noise interference to analog ground.
2. To ensure that ALC5616 works normally, please follow the power ON and OFF sequences of its power supply.
   Power ON Sequence: power on DBVDD/AVDD/DACREF/CPVDD first, and then MICVDD.
   Power OFF Sequence: power off MICVDD first, and then DBVDD/AVDD/DACREF/CPVDD.
3. For more details, please refer to ALC5616 datasheet.

Audio - Earphone Application

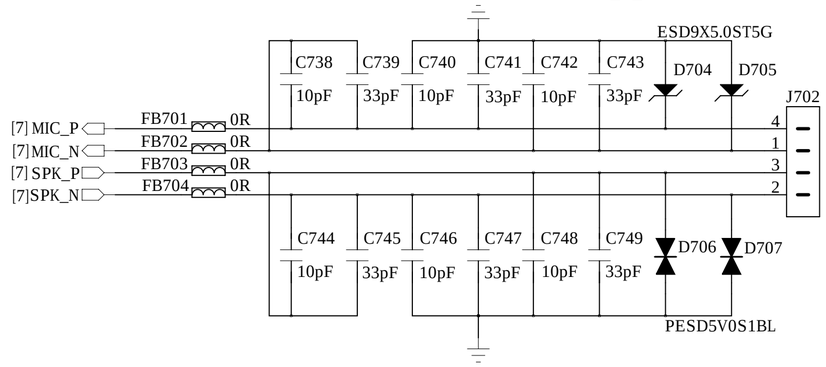


	CTIA	OMTP
R722/R724	NM	M
R721/R723	M	NM

Notes:

1. The analog output only drives earphone and headset. For larger power loads such as speakers, the design needs to incease the audio power amplifier.
2. The maximum capacitive loading for SPK is 330 pF and that for MIC is 250 pF.

Audio - Handset Application



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