# 声明

本 PDF 为个人翻译，准确行不能保证，建议参照原版进行学习

本人博文地址：https://me.csdn.net/weixin_44048162

Github 地址 ：https://github.com/843862803

使用的翻译软件为巽二博主所写

博主博文地址：https://me.csdn.net/m0_37868504

在不收取其他人费用的前提下，可以自由传播！

本文最后几页无法翻译，请见谅

因使用拆分后的文件进行翻译，文章索引可能无法使用。

# MSP432P401R，MSP432P401M SimpleLink™混合信号微控制器

## 1设备概述

### 1.1特点

•核心 – 带浮动的ARM®32位Cortex®-M4F CPU-
Point Unit and Memory Protection Unit
– 频率高达48 MHz –
ULPBench™基准测试：
– 192.3 ULPMark™-CP
– 绩效基准：
– 3.41 CoreMark/MHz
– 1.22 DMIPS/MHz (Dhrystone 2.1)

- Advanced Low-Power Analog Features
  - 14-Bit 1-MSPS SAR ADC With 13.2 ENOB
    具有过采样，差分和单端输入的原生和能力达到16 ENOB
  - Internal Voltage Reference With 10-ppm/°C Typical Stability
  - Two Analog Comparators
- Memories
  - Up to 256KB of Flash Main Memory (Organized Into Two Banks Enabling Simultaneous Read/Execute During Erase)
  - 16KB of Flash Information Memory (Used for BSL, TLV, and Flash Mailbox)
  - Up to 64KB of SRAM (Including 6KB of Backup Memory)
  - 32KB of ROM With MSP432™ Peripheral Driver Libraries
- Ultra-Low-Power Operating Modes
  - Active: 80 µA/MHz
  - Low-Frequency Active: 83 µA at 128 kHz
  - LPM3 (With RTC): 660 nA
  - LPM3.5 (With RTC): 630 nA
  - LPM4: 500 nA
  - LPM4.5: 25 nA
- Development Kits and Software (See *Tools and Software*)
  - MSP-EXP432P401R LaunchPad™ Development Kit
  - MSP-TS432PZ100 100-Pin Target Board
  - SimpleLink™ MSP432 Software Development Kit (SDK)
- Operating Characteristics
  - Wide Supply Voltage Range: 1.62 V to 3.7 V
  - Temperature Range (Ambient): –40°C to 85°C
- Flexible Clocking Features
  - Tunable Internal DCO (up to 48 MHz)
  - 32.768 kHz Low-Frequency Crystal Support (LFXT)
  - High-Frequency Crystal Support (HFXT) up to 48 MHz
  - Low-Frequency Internal Reference Oscillator (REFO)
  - Very Low-Power Low-Frequency Internal Oscillator (VLO)
  - Module Oscillator (MODOSC)
  - System Oscillator (SYSOSC)

•代码安全功能 – JTAG和SWD锁定 – IP保护（最多四个安全Flash区域，每个具有可配置的起始地址和大小）

- Enhanced System Features
  - Programmable Supervision and Monitoring of Supply Voltage
  - Multiple-Class Resets for Better Control of Application and Debug
  - 8-Channel DMA
  - RTC With Calendar and Alarm Functions
- Timing and Control
  - Up to Four 16-Bit Timers, Each With up to Five Capture, Compare, PWM Capability
  - Two 32-Bit Timers, Each With Interrupt Generation Capability
- Serial Communication
  - Up to Four eUSCI_A Modules
    - UART With Automatic Baud-Rate Detection
    - IrDA Encode and Decode
    - SPI (up to 16 Mbps)
  - Up to Four eUSCI_B Modules
    - $I^2C$ (With Multiple-Slave Addressing)
    - SPI (up to 16 Mbps)
- Flexible I/O Features
  - Ultra-Low-Leakage I/Os (±20 nA Maximum)
  - All I/Os With Capacitive-Touch Capability
  - Up to 48 I/Os With Interrupt and Wake-up Capability
  - Up to 24 I/Os With Port Mapping Capability
  - Eight I/Os With Glitch Filtering Capability

- Encryption and Data Integrity Accelerators
  - 128-, 192-, or 256-Bit AES Encryption and Decryption Accelerator
  - 32-Bit Hardware CRC Engine
- JTAG and Debug Support
  - 4-Pin JTAG and 2-Pin SWD Debug Interfaces
  - Serial Wire Trace
  - Power Debug and Profiling of Applications

## 1.2申请

- Industrial and Automation
  - Glass Breakage Detectors
  - Smart Thermostats
  - Access Panels
  - Gas Monitors
  - Field Transmitters
  - Process Automation
  - Home Automation
- Metering
  - Flow Meters
  - Electric Meters
  - Communication Modules
- Test and Measurement
  - Digital Multimeters
  - Wireless Digital Multimeters
  - Contactless and Hand-Held Digital Meters
- Health and Fitness
  - Watches
  - Activity Monitors
  - Fitness Accessories
  - Blood Glucose Meters
- Consumer Electronics
  - Mobile Devices
  - Sensor Hubs

## 1.3说明

SimpleLink
MSP432P401x微控制器（MCU）是经过优化的无线主机MCU，集成了14位模数转换器（ADC），最高可达16 ENOB，可提供超低功耗性能，包括80 µA/MHz有功功率和660具有FPU和DSP扩展的待机电源nA。作为优化的无线主机MCU，MSP432P401x允许开发人员为基于SimpleLink无线连接解决方　　案的应用添加高精度模拟和存储器扩展。

MSP432P401x器件是SimpleLink微控制器（MCU）平台的一部分，该平台由Wi-Fi®，Bluetooth®低功耗，Sub-1 GHz和主机MCU组成。所有这些都与一个核心软件开发工具包（SDK）和丰富的工具集共享一个易于使用的通用开发环境。通过SimpleLink平台的一次性集成，您可以将产品组合中的任意设备组合添加到设计中。SimpleLink平台的最终目标是在您的设计要求发生变化时实现100％的代码重用。有关更多信息，请访问www.ti.com/simplelink。

MSP432P401x器件由全面的工具，软件，文档，培训和支持生态系统提供支持，可帮助您快速开始开发。MSP-EXP432P401R
LaunchPad开发套件或MSP-TS432PZ100目标插座板（带有额外的MCU样本）以及免费的SimpleLink MSP432 SDK是您入门所需的全部内容。

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE(2) |
|---|---|---|
| MSP432P401RIPZ<br>MSP432P401MIPZ | LQFP (100) | 14 mm × 14 mm |
| MSP432P401RIZXH<br>MSP432P401MIZXH | NFBGA (80) | 5 mm × 5 mm |
| MSP432P401RIRGC<br>MSP432P401MIRGC | VQFN (64) | 9 mm × 9 mm |

（1）有关所有可用器件的最新部件，封装和订购信息，请参见第9节中的封装选项附录，或参见TI网站。

（2）此处显示的尺寸为近似值。有关公差的封装尺寸，请参见第9节中的机械数据。

# 1.4功能框图

图1-1显示了MSP432P401R和MSP432P401M器件的功能框图。

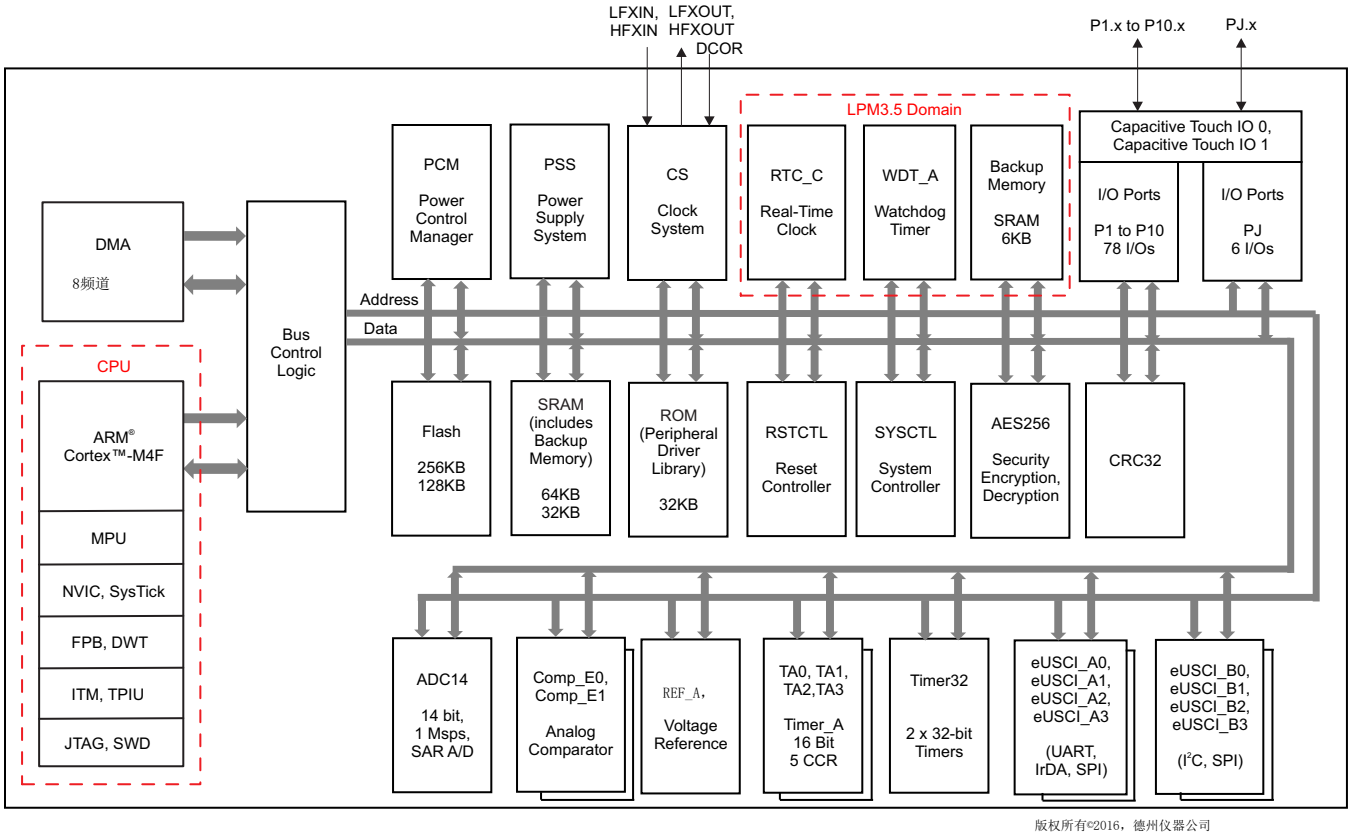





图1-1。 MSP432P401R，MSP432P401M功能框图

CPU和设备中的所有外围设备通过公共AHB矩阵相互交互。

在某些情况下，AHB端口和外围设备之间存在桥接。从存储器映射的角度来看，这些桥对应用是透明的，因此未在框图中示出。

# Table of Contents

# 2修订历史

注意：以前版本的页码可能与当前版本中的页码不同。

## 2016年7月26日至2017年3月7日期间的变更

# 3器件比较

表3-1总结了MSP432P401x微控制器的功能。

**Table 3-1. Device Comparison(1)**

| DEVICE | FLASH (KB) | SRAM (KB) | ADC14 (Channels) | COMP_E0 (Channels) | COMP_E1 (Channels) | Timer_A(2) | eUSCI | | 20-mA DRIVE I/O | TOTAL I/Os | PACKAGE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | CHANNEL A: UART, IrDA, SPI | CHANNEL B: SPI, I2C | | | |
| MSP432P401RIPZ | 256 | 64 | 24 ext，2 int | 8 | 8 | 5,5,5,4 | 4 | 4 | 4 | 84 | 100 PZ |
| MSP432P401MIPZ | 128 | 32 | 24分机，2 int | 8 | 8 | 5,5,5,4 | 4 | 4 | 4 | 84 | 100 PZ |
| MSP432P401RIZXH | 256 | 64 | 16分机，2分6 | 8 | 5,5,5 | 3 | 4 | 4 | 64 | 80 | ZXH |
| MSP432P401MIZXH | 128 | 32 | 16分机，2 int | 6 | 8 | 5,5,5 | 3 | 4 | 4 | 64 | 80 ZXH |
| MSP432P401RIRGC | 256 | 64 | 12 ext，2 int | 2 | 4 | 5,5 | 5 | 3 | 3 | 4 | 48 64 RGC |
| MSP432P401MIRGC | 128 | 32 | 12 ext，2 int | 2 | 4 | 5,5 | 5 | 3 | 3 | 4 | 48 64 RGC |

（1）有关所有可用器件的最新部件、封装和订购信息，请参见第9节中的封装选项附录，或访问TI网站www.ti.com。

（2）序列中的每个数字代表Timer_A的实例化，其中包含相关数量的捕获/比较寄存器和PWM输出发生器。例如，数字序列3,5表示Timer_A的两个实例，第一实例具有3，第二实例分别具有5个捕获/比较寄存器和PWM输出发生器。

## 3.1相关产品

有关此系列产品或相关产品中其他设备的信息，请参阅以下链接。

**Products for TI Microcontrollers** Low-power and high-performance MCUs, with wired and wireless 连接选项。

**Products for SimpleLink MSP432 MCUs** SimpleLink MSP432 MCUs with an ultra-low-power ARM Cortex-M4内核针对物联网传感器节点应用进行了优化。该系列采用集成的14位ADC，可在不牺牲功率的情况下采集和处理高精度信号，是TI SimpleLink无线连接解决方 案的最佳主机MCU。

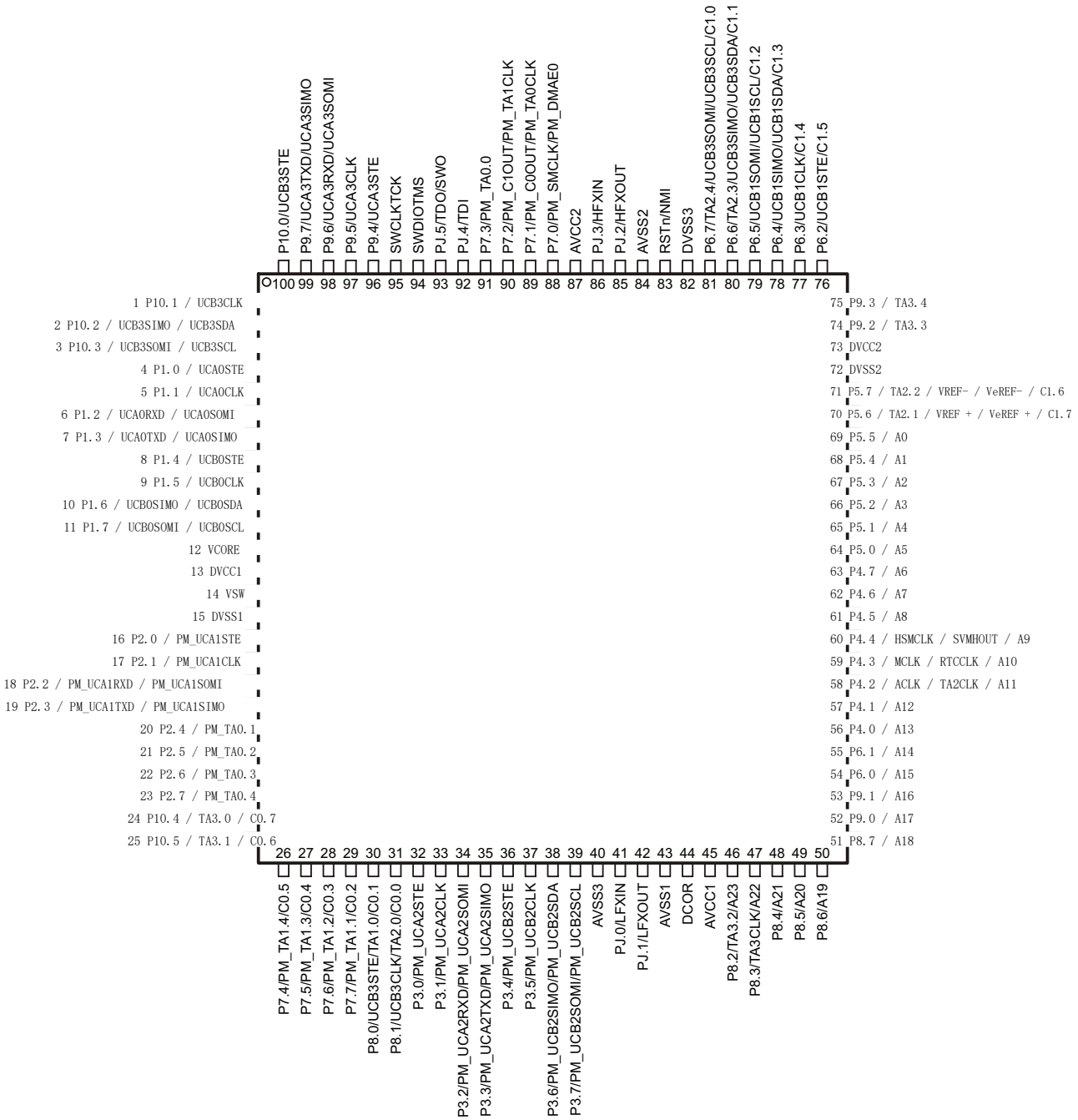
**Companion Products for MSP432P401R** Review products that are frequently purchased or used with 这个产品。

**Reference Designs for MSP432P401R** The TI Designs Reference Design Library is a robust reference 跨越模拟，嵌入式处理器和连接的设计库。
TI专家创建的TI设计包括原理图或方框图，BOM和设计文件，可帮助您快速启动系统设计，从而加快产品上市速度。在ti.com/tidesigns上搜索和下载设计。

# 4终端配置和功能

## 4.1引脚图

图4-1显示了100引脚PZ封装的引脚排列。




A. 端口P2，P3和P7上的辅助数字功能是完全可映射的。此引脚分布仅显示默认映射。有关详细信息，请参见第6.9.2节。

B. 在这些数字I / O上实现毛刺滤波器：P1.0，P1.4，P1.5，P3.0，P3.4，P3.5，P6.6，P6.7。

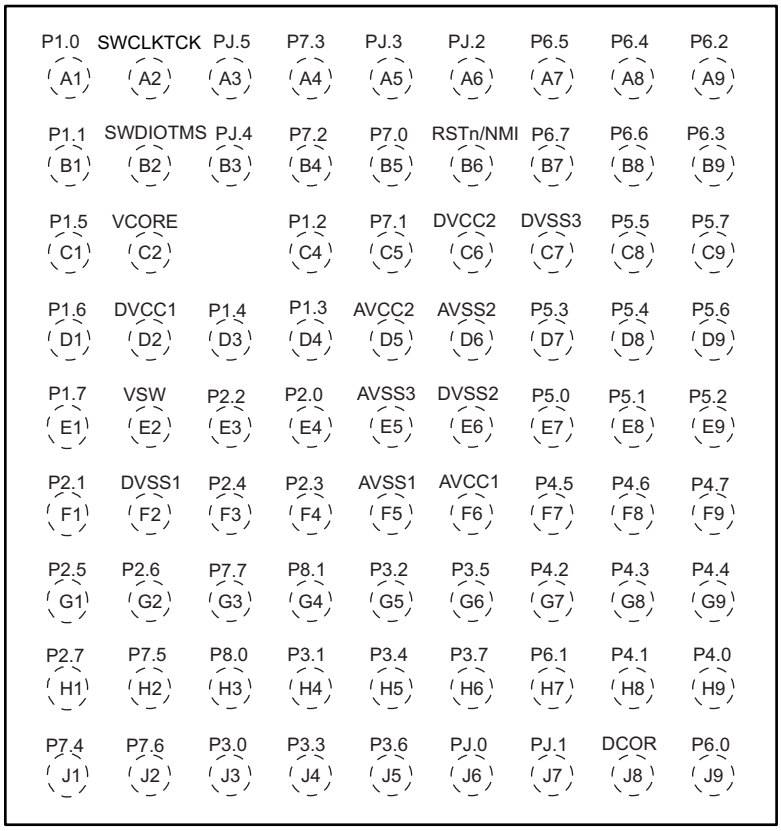
C. UART BSL引脚：P1.2 – BSLRXD，P1.3 – BSLTXD

D. SPI BSL引脚：P1.4 – BSLSTE，P1.5 – BSLCLK，P1.6 – BSLSIMO，P1.7 – BSLSOMI

E. $I^2C$ BSL pins: P3.6 - BSLSDA, P7.7 - BSLSCL

图4-1。 100针PZ封装（俯视图）

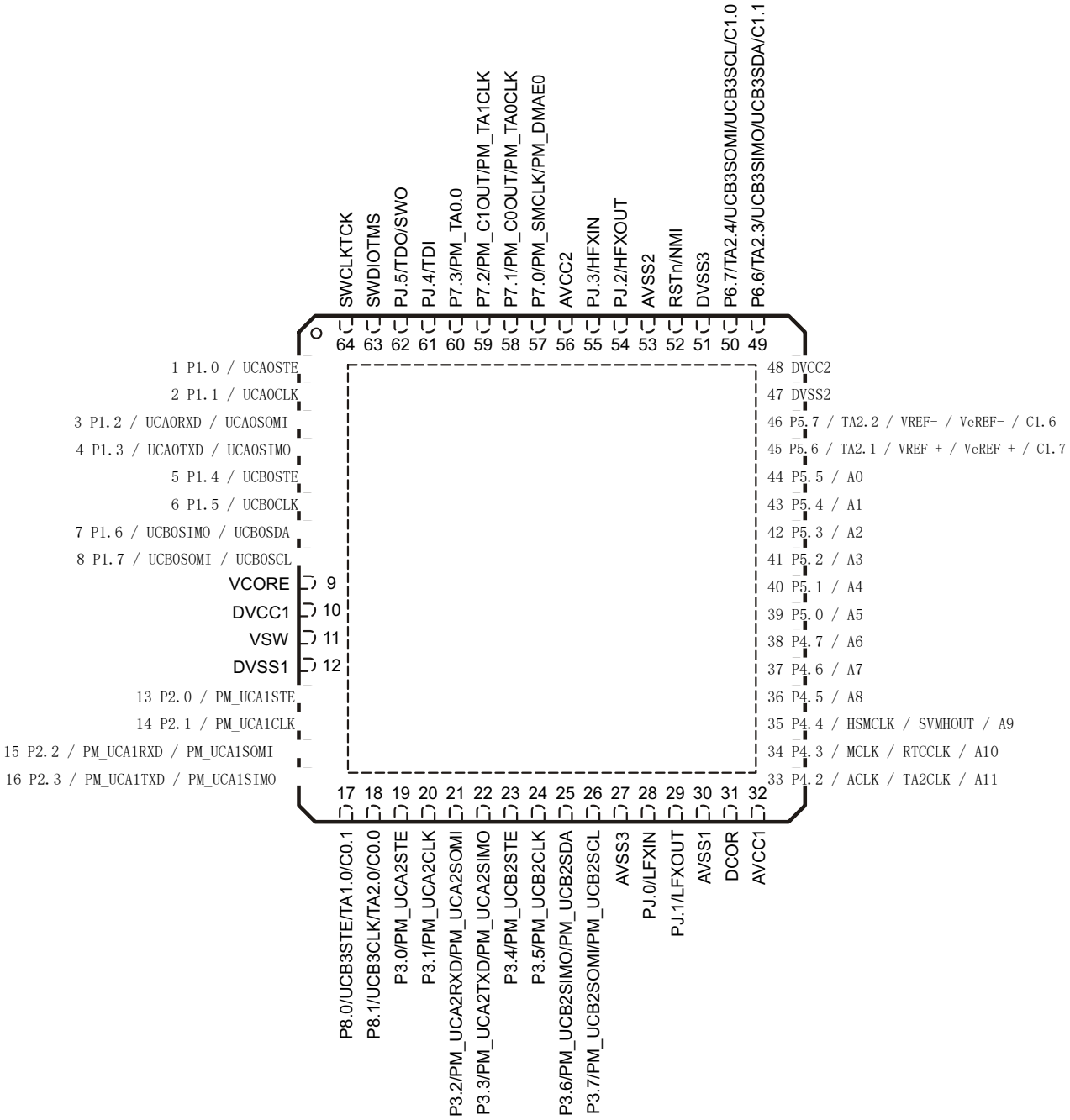
图4-2显示了80引脚ZXH封装的引脚排列。




A. 在这些数字I / O上实现毛刺滤波器：P1.0，P1.4，P1.5，P3.0，P3.4，P3.5，P6.6，P6.7。
B. UART BSL引脚：P1.2 - BSLRXD，P1.3 - BSLTXD
C. SPI BSL引脚：P1.4 - BSLSTE，P1.5 - BSLCLK，P1.6 - BSLSIMO，P1.7 - BSLSOMI
D. $I^2C$ BSL pins: P3.6 - BSLSDA, P3.7 - BSLSCL

图4-2。 80针ZXH封装（俯视图）

图4-3显示了64引脚RGC封装的引脚排列。




A. 端口P2，P3和P7上的辅助数字功能是完全可映射的。此引脚分布仅显示默认映射。有关详细信息，请参见第6.9.2节。

B. 在这些数字I / O上实现毛刺滤波器：P1.0，P1.4，P1.5，P3.0，P3.4，P3.5，P6.6，P6.7。

C. TI建议将QFN封装上的导热垫连接到DVSS。

D. UART BSL引脚：P1.2 – BSLRXD，P1.3 – BSLTXD

E. SPI BSL引脚：P1.4 – BSLSTE，P1.5 – BSLCLK，P1.6 – BSLSIMO，P1.7 – BSLSOMI

F. $I^2C$ BSL pins: P3.6 - BSLSDA, P7.7 - BSLSCL

图4-3。 64引脚RGC封装（俯视图）

## 4.2引脚属性

表4-1描述了引脚的属性。

**Table 4-1. Pin Attributes**

| PIN NO.(1) | | | SIGNAL NAME(2) (3) | SIGNAL TYPE(4) | BUFFER TYPE(5) | POWER SOURCE(6) | RESET STATE AFTER POR(7) |
|---|---|---|---|---|---|---|---|
| PZ | ZXH | RGC | | | | | |
| 1 | N / A | N / A. | P10.1 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | UCB3CLK | I/O | LVCMOS | DVCC | N/A |
| 2 | N / A | N / A. | P10.2 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | UCB3SIMO | I/O | LVCMOS | DVCC | N/A |
| | | | UCB3SDA | I/O | LVCMOS | DVCC | N/A |
| 3 | N / A | N / A. | P10.3 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | UCB3SOMI | I/O | LVCMOS | DVCC | N/A |
| | | | UCB3SCL | I/O | LVCMOS | DVCC | N/A |
| 4 | A1 | 1 | P1.0 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | UCA0STE | I/O | LVCMOS | DVCC | N/A |
| 5 | B1 | 2 | P1.1 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | UCA0CLK | I/O | LVCMOS | DVCC | N/A |
| 6 | C4 | 3 | P1.2 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | UCA0RXD | I | LVCMOS | DVCC | N/A |
| | | | UCA0SOMI | I/O | LVCMOS | DVCC | N/A |
| 7 | D4 | 4 | P1.3 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | UCA0TXD | O | LVCMOS | DVCC | N/A |
| | | | UCA0SIMO | I/O | LVCMOS | DVCC | N/A |
| 8 | D3 | 5 | P1.4 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | UCB0STE | I/O | LVCMOS | DVCC | N/A |
| 9 | C1 | 6 | P1.5 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | UCB0CLK | I/O | LVCMOS | DVCC | N/A |
| 10 | D1 | 7 | P1.6 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | UCB0SIMO | I/O | LVCMOS | DVCC | N/A |
| | | | UCB0SDA | I/O | LVCMOS | DVCC | N/A |
| 11 | E1 | 8 | P1.7 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | UCB0SOMI | I/O | LVCMOS | DVCC | N/A |
| | | | UCB0SCL | I/O | LVCMOS | DVCC | N/A |
| 12 | C2 | 9 | VCORE | – 电源 | DVCC | N / A. | |
| 13 | D2 | 10 | DVCC1 | – 电源 | 不适用 | N / A. | |
| 14 | E2 | 11 | VSW | – 电源 | 不适用 | N / A. | |
| 15 | F2 | 12 | DVSS1 | – 电源 | N / A | N / A. | |
| 16 | E4 | 13 | P2.0 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | PM_UCA1STE | I/O | LVCMOS | DVCC | N/A |

(1) N/A = not available on this package
（2）（RD）表示该引脚的复位默认信号名称。
（3）要确定每个引脚的引脚复用编码，请参见第6.12节“输入/输出图”。
(4) Signal Types: I = Input, O = Output, I/O = Input or Output, P = power
(5) Buffer Types: see Table 4-3 for details
（6）此表中所示的电源是I / O电源，可能与模块电源不同。
（7）复位状态：OFF
=施密特触发和上拉或下拉（如果可用）禁用的高阻抗PD
=启用下拉的高阻抗输入PU =启用上拉的高阻抗输入N / A =不适用

**Table 4-1. Pin Attributes (continued)**

| PIN NO.(1) | | | SIGNAL NAME(2) (3) | SIGNAL TYPE(4) | BUFFER TYPE(5) | POWER SOURCE(6) | RESET STATE AFTER POR(7) |
|---|---|---|---|---|---|---|---|
| PZ | ZXH | RGC | | | | | |
| 17 | F1 | 14 | P2.1 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | PM_UCA1CLK | I/O | LVCMOS | DVCC | N/A |
| 18 | E3 | 15 | P2.2 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | PM_UCA1RXD | I | LVCMOS | DVCC | N/A |
| | | | PM_UCA1SOMI | I/O | LVCMOS | DVCC | N/A |
| 19 | F4 | 16 | P2.3 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | PM_UCA1TXD | O | LVCMOS | DVCC | N/A |
| | | | PM_UCA1SIMO | I/O | LVCMOS | DVCC | N/A |
| 20 | F3 | 不适用 | P2.4 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | PM_TA0.1 | I/O | LVCMOS | DVCC | N/A |
| 21 | G1 | N / A. | P2.5 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | PM_TA0.2 | I/O | LVCMOS | DVCC | N/A |
| 22 | G2 | N / A. | P2.6 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | PM_TA0.3 | I/O | LVCMOS | DVCC | N/A |
| 23 | H1 | N / A. | P2.7 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | PM_TA0.4 | I/O | LVCMOS | DVCC | N/A |
| 24 | N / A | N / A. | P10.4 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | TA3.0 | I/O | LVCMOS | DVCC | N/A |
| | | | C0.7 | I | Analog | DVCC | N/A |
| 25 | N / A | N / A. | P10.5 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | TA3.1 | I/O | LVCMOS | DVCC | N/A |
| | | | C0.6 | I | Analog | DVCC | N/A |
| 26 | J1 | N / A. | P7.4 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | PM_TA1.4 | I/O | LVCMOS | DVCC | N/A |
| | | | C0.5 | I | Analog | DVCC | N/A |
| 27 | H2 | N / A. | P7.5 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | PM_TA1.3 | I/O | LVCMOS | DVCC | N/A |
| | | | C0.4 | I | Analog | DVCC | N/A |
| 28 | J2 | N / A. | P7.6 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | PM_TA1.2 | I/O | LVCMOS | DVCC | N/A |
| | | | C0.3 | I | Analog | DVCC | N/A |
| 29 | G3 | N / A. | P7.7 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | PM_TA1.1 | I/O | LVCMOS | DVCC | N/A |
| | | | C0.2 | I | Analog | DVCC | N/A |
| 30 | H3 | 17 | P8.0 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | UCB3STE | I/O | LVCMOS | DVCC | N/A |
| | | | TA1.0 | I/O | LVCMOS | DVCC | N/A |
| | | | C0.1 | I | Analog | DVCC | N/A |
| 31 | G4 | 18 | P8.1 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | UCB3CLK | I/O | LVCMOS | DVCC | N/A |
| | | | TA2.0 | I/O | LVCMOS | DVCC | N/A |
| | | | C0.0 | I | Analog | DVCC | N/A |
| 32 | J3 | 19 | P3.0 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | PM_UCA2STE | I/O | LVCMOS | DVCC | N/A |
| 33 | H4 | 20 | P3.1 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | PM_UCA2CLK | I/O | LVCMOS | DVCC | N/A |

**Table 4-1. Pin Attributes (continued)**

| PIN NO.(1) | | | SIGNAL NAME(2) (3) | SIGNAL TYPE(4) | BUFFER TYPE(5) | POWER SOURCE(6) | RESET STATE AFTER POR(7) |
|---|---|---|---|---|---|---|---|
| PZ | ZXH | RGC | | | | | |
| 34 | G5 | 21 | P3.2 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | PM_UCA2RXD | I | LVCMOS | DVCC | N/A |
| | | | PM_UCA2SOMI | I/O | LVCMOS | DVCC | N/A |
| 35 | J4 | 22 | P3.3 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | PM_UCA2TXD | O | LVCMOS | DVCC | N/A |
| | | | PM_UCA2SIMO | I/O | LVCMOS | DVCC | N/A |
| 36 | H5 | 23 | P3.4 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | PM_UCB2STE | I/O | LVCMOS | DVCC | N/A |
| 37 | G6 | 24 | P3.5 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | PM_UCB2CLK | I/O | LVCMOS | DVCC | N/A |
| 38 | J5 | 25 | P3.6 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | PM_UCB2SIMO | I/O | LVCMOS | DVCC | N/A |
| | | | PM_UCB2SDA | I/O | LVCMOS | DVCC | N/A |
| 39 | H6 | 26 | P3.7 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | PM_UCB2SOMI | I/O | LVCMOS | DVCC | N/A |
| | | | PM_UCB2SCL | I | LVCMOS | DVCC | N/A |
| 40 | E5 | 27 | AVSS3 | – | 电源 | 不适用 | 不适用 |
| 41 | J6 | 28 | PJ.0 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | LFXIN | I | Analog | DVCC | N/A |
| 42 | J7 | 29 | PJ.1 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | LFXOUT | O | Analog | DVCC | N/A |
| 43 | F5 | 30 | AVSS1 | – | 电源 | 不适用 | 不适用 |
| 44 | J8 | 31 | DCOR | – | 模拟 | N / A | N / A. |
| 45 | F6 | 32 | AVCC1 | – | 电源 | N / A | N / A. |
| 46 | N / A | N / A. | P8.2 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | TA3.2 | I/O | LVCMOS | DVCC | N/A |
| | | | A23 | I | Analog | DVCC | N/A |
| 47 | N / A | N / A. | P8.3 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | TA3CLK | I | LVCMOS | DVCC | N/A |
| | | | A22 | I | Analog | DVCC | N/A |
| 48 | N / A | N / A. | P8.4 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | A21 | I | Analog | DVCC | N/A |
| 49 | N / A | N / A. | P8.5 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | A20 | I | Analog | DVCC | N/A |
| 50 | N / A | N / A. | P8.6 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | A19 | I | Analog | DVCC | N/A |
| 51 | N / A | N / A. | P8.7 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | A18 | I | Analog | DVCC | N/A |
| 52 | N / A | N / A. | P9.0 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | A17 | I | Analog | DVCC | N/A |
| 53 | N / A | N / A. | P9.1 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | A16 | I | Analog | DVCC | N/A |
| 54 | J9 | N / A. | P6.0 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | A15 | I | Analog | DVCC | N/A |
| 55 | H7 | N / A. | P6.1 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | A14 | I | Analog | DVCC | N/A |

**Table 4-1. Pin Attributes (continued)**

| PIN NO.(1) | | | SIGNAL NAME(2) (3) | SIGNAL TYPE(4) | BUFFER TYPE(5) | POWER SOURCE(6) | RESET STATE AFTER POR(7) |
|---|---|---|---|---|---|---|---|
| PZ | ZXH | RGC | | | | | |
| 56 | H9 | N / A. | P4.0 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | A13 | I | Analog | DVCC | N/A |
| 57 | H8 | N / A. | P4.1 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | A12 | I | Analog | DVCC | N/A |
| 58 | G7 | 33 | P4.2 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | ACLK | O | LVCMOS | DVCC | N/A |
| | | | TA2CLK | I | LVCMOS | DVCC | N/A |
| | | | A11 | I | Analog | DVCC | N/A |
| 59 | G8 | 34 | P4.3 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | MCLK | O | LVCMOS | DVCC | N/A |
| | | | RTCCLK | O | LVCMOS | DVCC | N/A |
| | | | A10 | I | Analog | DVCC | N/A |
| 60 | G9 | 35 | P4.4 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | HSMCLK | O | LVCMOS | DVCC | N/A |
| | | | SVMHOUT | O | LVCMOS | DVCC | N/A |
| | | | A9 | I | Analog | DVCC | N/A |
| 61 | F7 | 36 | P4.5 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | A8 | I | Analog | DVCC | N/A |
| 62 | F8 | 37 | P4.6 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | A7 | I | Analog | DVCC | N/A |
| 63 | F9 | 38 | P4.7 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | A6 | I | Analog | DVCC | N/A |
| 64 | E7 | 39 | P5.0 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | A5 | I | Analog | DVCC | N/A |
| 65 | E8 | 40 | P5.1 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | A4 | I | Analog | DVCC | N/A |
| 66 | E9 | 41 | P5.2 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | A3 | I | Analog | DVCC | N/A |
| 67 | D7 | 42 | P5.3 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | A2 | I | Analog | DVCC | N/A |
| 68 | D8 | 43 | P5.4 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | A1 | I | Analog | DVCC | N/A |
| 69 | C8 | 44 | P5.5 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | A0 | I | Analog | DVCC | N/A |
| 70 | D9 | 45 | P5.6 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | TA2.1 | I/O | LVCMOS | DVCC | N/A |
| | | | VREF+ | O | Analog | DVCC | N/A |
| | | | VeREF+ | I | Analog | DVCC | N/A |
| | | | C1.7 | I | Analog | DVCC | N/A |
| 71 | C9 | 46 | P5.7 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | TA2.2 | I/O | LVCMOS | DVCC | N/A |
| | | | VREF- | O | Analog | DVCC | N/A |
| | | | VeREF- | I | Analog | DVCC | N/A |
| | | | C1.6 | I | Analog | DVCC | N/A |
| 72 | E6 | 47 DVSS2 | – 电源不适用不适用 | | | | |
| 73 | C6 | 48 DVCC2 | – 电源N / A N / A. | | | | |

**Table 4-1. Pin Attributes (continued)**

| PIN NO.(1) | | | SIGNAL NAME(2) (3) | SIGNAL TYPE(4) | BUFFER TYPE(5) | POWER SOURCE(6) | RESET STATE AFTER POR(7) |
|---|---|---|---|---|---|---|---|
| PZ | ZXH | RGC | | | | | |
| 74 | N / A | N / A. | P9.2 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | TA3.3 | I/O | LVCMOS | DVCC | N/A |
| 75 | N / A | N / A. | P9.3 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | TA3.4 | I/O | LVCMOS | DVCC | N/A |
| 76 | A9 | N / A. | P6.2 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | UCB1STE | I/O | LVCMOS | DVCC | N/A |
| | | | C1.5 | I | Analog | DVCC | N/A |
| 77 | B9 | 不适用 | P6.3 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | UCB1CLK | I/O | LVCMOS | DVCC | N/A |
| | | | C1.4 | I | Analog | DVCC | N/A |
| 78 | A8 | N / A. | P6.4 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | UCB1SIMO | I/O | LVCMOS | DVCC | N/A |
| | | | UCB1SDA | I/O | LVCMOS | DVCC | N/A |
| | | | C1.3 | I | Analog | DVCC | N/A |
| 79 | A7 | 不适用 | P6.5 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | UCB1SOMI | I/O | LVCMOS | DVCC | N/A |
| | | | UCB1SCL | I/O | LVCMOS | DVCC | N/A |
| | | | C1.2 | I | Analog | DVCC | N/A |
| 80 | B8 | 49 | P6.6 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | TA2.3 | I/O | LVCMOS | DVCC | N/A |
| | | | UCB3SIMO | I/O | LVCMOS | DVCC | N/A |
| | | | UCB3SDA | I/O | LVCMOS | DVCC | N/A |
| | | | C1.1 | I | Analog | DVCC | N/A |
| 81 | B7 | 50 | P6.7 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | TA2.4 | I/O | LVCMOS | DVCC | N/A |
| | | | UCB3SOMI | I/O | LVCMOS | DVCC | N/A |
| | | | UCB3SCL | I/O | LVCMOS | DVCC | N/A |
| | | | C1.0 | I | Analog | DVCC | N/A |
| 82 | C7 | 51 DVSS3 | – 电源不适用不适用 | | | | |
| 83 | B6 | 52 | RSTn (RD) | I | LVCMOS | DVCC | PU |
| | | | NMI | I | LVCMOS | DVCC | N/A |
| 84 | D6 | 53 AVSS2 | – 电源不适用不适用 | | | | |
| 85 | A6 | 54 | PJ.2 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | HFXOUT | O | Analog | DVCC | N/A |
| 86 | A5 | 55 | PJ.3 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | HFXIN | I | Analog | DVCC | N/A |
| 87 | D5 | 56 AVCC2 | – 电源N / A N / A. | | | | |
| 88 | B5 | 57 | P7.0 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | PM_SMCLK | O | LVCMOS | DVCC | N/A |
| | | | PM_DMAE0 | I | LVCMOS | DVCC | N/A |
| 89 | C5 | 58 | P7.1 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | PM_C0OUT | O | LVCMOS | DVCC | N/A |
| | | | PM_TA0CLK | I | LVCMOS | DVCC | N/A |
| 90 | B4 | 59 | P7.2 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | PM_C1OUT | O | LVCMOS | DVCC | N/A |
| | | | PM_TA1CLK | I | LVCMOS | DVCC | N/A |

**Table 4-1. Pin Attributes (continued)**

| PIN NO.(1) | | | SIGNAL NAME(2) (3) | SIGNAL TYPE(4) | BUFFER TYPE(5) | POWER SOURCE(6) | RESET STATE AFTER POR(7) |
|---|---|---|---|---|---|---|---|
| PZ | ZXH | RGC | | | | | |
| 91 | A4 | 60 | P7.3 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | PM_TA0.0 | I/O | LVCMOS | DVCC | N/A |
| 92 | B3 | 61 | PJ.4 | I/O | LVCMOS | DVCC | N/A |
| | | | TDI (RD) | I | LVCMOS | DVCC | PU |
| 93 | A3 | 62 | PJ.5 | I/O | LVCMOS | DVCC | N/A |
| | | | TDO (RD) | O | LVCMOS | DVCC | N/A |
| | | | SWO | O | LVCMOS | DVCC | N/A |
| 94 | B2 | 63 | SWDIOTMS | I / O | LVCMOS | DVCC | PU |
| 95 | A2 | 64 | SWCLKTCK | I | LVCMOS | DVCC | PD |
| 96 | N / A | N / A. | P9.4 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | UCA3STE | I/O | LVCMOS | DVCC | N/A |
| 97 | N / A | N / A. | P9.5 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | UCA3CLK | I/O | LVCMOS | DVCC | N/A |
| 98 | N / A | N / A. | P9.6 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | UCA3RXD | I | LVCMOS | DVCC | N/A |
| | | | UCA3SOMI | I/O | LVCMOS | DVCC | N/A |
| 99 | N / A | N / A. | P9.7 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | UCA3TXD | O | LVCMOS | DVCC | N/A |
| | | | UCA3SIMO | I/O | LVCMOS | DVCC | N/A |
| 100 | N / A | N / A. | P10.0 (RD) | I/O | LVCMOS | DVCC | OFF |
| | | | UCB3STE | I/O | LVCMOS | DVCC | N/A |
| N/A | N/A | Pad | QFN Pad | – | – | N/A | – |

## 4.3信号描述

表4-2描述了所有器件型号和封装选项的信号。

**Table 4-2. Signal Descriptions**

| FUNCTION | SIGNAL NAME | SIGNAL NO.(1) | | | SIGNAL TYPE(2) | DESCRIPTION |
|---|---|---|---|---|---|---|
| | | PZ | ZXH | RGC | | |
| ADC | A0 | 69 | C8 | 44 | I | ADC analog input A0 |
| | A1 | 68 | D8 | 43 | I | ADC analog input A1 |
| | A2 | 67 | D7 | 42 | I | ADC analog input A2 |
| | A3 | 66 | E9 | 41 | I | ADC analog input A3 |
| | A4 | 65 | E8 | 40 | I | ADC analog input A4 |
| | A5 | 64 | E7 | 39 | I | ADC analog input A5 |
| | A6 | 63 | F9 | 38 | I | ADC analog input A6 |
| | A7 | 62 | F8 | 37 | I | ADC analog input A7 |
| | A8 | 61 | F7 | 36 | I | ADC analog input A8 |
| | A9 | 60 | G9 | 35 | I | ADC analog input A9 |
| | A10 | 59 | G8 | 34 | I | ADC analog input A10 |
| | A11 | 58 | G7 | 33 | I | ADC analog input A11 |
| | A12 | 57 | H8 | N/A | I | ADC analog input A12 |
| | A13 | 56 | H9 | N/A | I | ADC analog input A13 |
| | A14 | 55 | H7 | N/A | I | ADC analog input A14 |
| | A15 | 54 | J9 | N/A | I | ADC analog input A15 |
| | A16 | 53 | N/A | N/A | I | ADC analog input A16 |
| | A17 | 52 | N/A | N/A | I | ADC analog input A17 |
| | A18 | 51 | N/A | N/A | I | ADC analog input A18 |
| | A19 | 50 | N/A | N/A | I | ADC analog input A19 |
| | A20 | 49 | N/A | N/A | I | ADC analog input A20 |
| | A21 | 48 | N/A | N/A | I | ADC analog input A21 |
| | A22 | 47 | N/A | N/A | I | ADC analog input A22 |
| | A23 | 46 | N/A | N/A | I | ADC analog input A23 |
| Clock | ACLK | 58 | G7 | 33 | O | ACLK clock output |
| | DCOR 44 J8 31 – DCO外部电阻引脚 | | | | | |
| | HFXIN 86 A5 55 I用于高频晶体振荡器HFXT的输入 | | | | | |
| | HFXOUT 85 A6 54 O高频晶体振荡器HFXT的输出 | | | | | |
| | HSMCLK | 60 | G9 | 35 | O | HSMCLK clock output |
| | LFXIN 41 J6 28 I用于低频晶体振荡器LFXT的输入 | | | | | |
| | LFXOUT 42 J7 29 O低频晶体振荡器LFXT的输出 | | | | | |
| | MCLK | 59 | G8 | 34 | O | MCLK clock output |

(1) N/A = not available
(2) I = input, O = output

表4-2。信号描述（续）

| FUNCTION | SIGNAL NAME | SIGNAL NO.(1) | | | SIGNAL TYPE(2) | DESCRIPTION |
|---|---|---|---|---|---|---|
| | | PZ | ZXH | RGC | | |
| Comparator | C0.0 | 31 | G4 | 18 | I | Comparator_E0 input 0 |
| | C0.1 | 30 | H3 | 17 | I | Comparator_E0 input 1 |
| | C0.2 | 29 | G3 | N/A | I | Comparator_E0 input 2 |
| | C0.3 | 28 | J2 | N/A | I | Comparator_E0 input 3 |
| | C0.4 | 27 | H2 | N/A | I | Comparator_E0 input 4 |
| | C0.5 | 26 | J1 | N/A | I | Comparator_E0 input 5 |
| | C0.6 | 25 | N/A | N/A | I | Comparator_E0 input 6 |
| | C0.7 | 24 | N/A | N/A | I | Comparator_E0 input 7 |
| | C1.0 | 81 | B7 | 50 | I | Comparator_E1 input 0 |
| | C1.1 | 80 | B8 | 49 | I | Comparator_E1 input 1 |
| | C1.2 | 79 | A7 | N/A | I | Comparator_E1 input 2 |
| | C1.3 | 78 | A8 | N/A | I | Comparator_E1 input 3 |
| | C1.4 | 77 | B9 | N/A | I | Comparator_E1 input 4 |
| | C1.5 | 76 | A9 | N/A | I | Comparator_E1 input 5 |
| | C1.6 | 71 | C9 | 46 | I | Comparator_E1 input 6 |
| | C1.7 | 70 | D9 | 45 | I | Comparator_E1 input 7 |
| Debug | SWCLKTCK | 95 | A2 | 64 | I | Serial wire clock input (SWCLK)/JTAG clock input (TCK) |
| | SWDIOTMS | 94 | B2 | 63 | I/O | Serial wire data input/output (SWDIO)/JTAG test mode select (TMS) |
| | SWO | 93 | A3 | 62 | O | Serial wire trace output |
| | TDI | 92 | B3 | 61 | I | JTAG test data input |
| | TDO | 93 | A3 | 62 | O | JTAG test data output |
| GPIO | P1.0 | 4 | A1 | 1 | I/O | General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability |
| | P1.1 | 5 | B1 | 2 | I/O | General-purpose digital I/O with port interrupt and wake-up capability |
| | P1.2 | 6 | C4 | 3 | I/O | General-purpose digital I/O with port interrupt and wake-up capability |
| | P1.3 | 7 | D4 | 4 | I/O | General-purpose digital I/O with port interrupt and wake-up capability |
| | P1.4 | 8 | D3 | 5 | I/O | General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability |
| | P1.5 | 9 | C1 | 6 | I/O | General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability |
| | P1.6 | 10 | D1 | 7 | I/O | General-purpose digital I/O with port interrupt and wake-up capability |
| | P1.7 | 11 | E1 | 8 | I/O | General-purpose digital I/O with port interrupt and wake-up capability |

表4-2。信号描述（续）

| FUNCTION | SIGNAL NAME | SIGNAL NO.(1) | | | SIGNAL TYPE(2) | DESCRIPTION |
|---|---|---|---|---|---|---|
| | | PZ | ZXH | RGC | | |
| GPIO (continued) | P2.0 | 16 | E4 | 13 | I/O | 具有端口中断和唤醒功能的通用数字I / O，具有可重配置端口映射辅助功能。该I / O可配置为高驱动器运行，最高可达20 mA驱动器。 |
| | P2.1 | 17 | F1 | 14 | I/O | 具有端口中断和唤醒功能的通用数字I / O，具有可重配置端口映射辅助功能。该I / O可配置为高驱动器运行，最高可达20 mA驱动器。 |
| | P2.2 | 18 | E3 | 15 | I/O | 具有端口中断和唤醒功能的通用数字I / O，具有可重配置端口映射辅助功能。该I / O可配置为高驱动器运行，最高可达20 mA驱动器。 |
| | P2.3 | 19 | F4 | 16 | I/O | 具有端口中断和唤醒功能的通用数字I / O，具有可重配置端口映射辅助功能。该I / O可配置为高驱动器运行，最高可达20 mA驱动器。 |
| | P2.4 | 20 | F3 | N/A | I/O | 具有端口中断和唤醒功能的通用数字I / O，具有可重配置端口映射辅助功能 |
| | P2.5 | 21 | G1 | N/A | I/O | 具有端口中断和唤醒功能的通用数字I / O，具有可重配置端口映射辅助功能 |
| | P2.6 | 22 | G2 | N/A | I/O | 具有端口中断和唤醒功能的通用数字I / O，具有可重配置端口映射辅助功能 |
| | P2.7 | 23 | H1 | N/A | I/O | 具有端口中断和唤醒功能的通用数字I / O，具有可重配置端口映射辅助功能 |
| | P3.0 | 32 | J3 | 19 | I/O | 具有端口中断，唤醒和毛刺过滤功能的通用数字I / O，以及具有可重配置端口映射辅助功能的通用数字I / O. |
| | P3.1 | 33 | H4 | 20 | I/O | 具有端口中断和唤醒功能的通用数字I / O，具有可重配置端口映射辅助功能 |
| | P3.2 | 34 | G5 | 21 | I/O | 具有端口中断和唤醒功能的通用数字I / O，具有可重配置端口映射辅助功能 |
| | P3.3 | 35 | J4 | 22 | I/O | 具有端口中断和唤醒功能的通用数字I / O，具有可重配置端口映射辅助功能 |
| | P3.4 | 36 | H5 | 23 | I/O | 具有端口中断，唤醒和毛刺过滤功能的通用数字I / O，以及具有可重配置端口映射辅助功能的通用数字I / O. |
| | P3.5 | 37 | G6 | 24 | I/O | 具有端口中断，唤醒和毛刺过滤功能的通用数字I / O，以及具有可重配置端口映射辅助功能的通用数字I / O. |
| | P3.6 | 38 | J5 | 25 | I/O | 具有端口中断和唤醒功能的通用数字I / O，具有可重配置端口映射辅助功能 |
| | P3.7 | 39 | H6 | 26 | I/O | 具有端口中断和唤醒功能的通用数字I / O，具有可重配置端口映射辅助功能 |

表4-2。信号描述（续）

| FUNCTION | SIGNAL NAME | SIGNAL NO.(1) | | | SIGNAL TYPE(2) | DESCRIPTION |
|---|---|---|---|---|---|---|
| | | PZ | ZXH | RGC | | |
| GPIO (continued) | P4.0 | 56 | H9 | N/A | I/O | General-purpose digital I/O with port interrupt and wake-up capability |
| | P4.1 | 57 | H8 | N/A | I/O | General-purpose digital I/O with port interrupt and wake-up capability |
| | P4.2 | 58 | G7 | 33 | I/O | General-purpose digital I/O with port interrupt and wake-up capability |
| | P4.3 | 59 | G8 | 34 | I/O | General-purpose digital I/O with port interrupt and wake-up capability |
| | P4.4 | 60 | G9 | 35 | I/O | General-purpose digital I/O with port interrupt and wake-up capability |
| | P4.5 | 61 | F7 | 36 | I/O | General-purpose digital I/O with port interrupt and wake-up capability |
| | P4.6 | 62 | F8 | 37 | I/O | General-purpose digital I/O with port interrupt and wake-up capability |
| | P4.7 | 63 | F9 | 38 | I/O | General-purpose digital I/O with port interrupt and wake-up capability |
| | P5.0 | 64 | E7 | 39 | I/O | General-purpose digital I/O with port interrupt and wake-up capability |
| | P5.1 | 65 | E8 | 40 | I/O | General-purpose digital I/O with port interrupt and wake-up capability |
| | P5.2 | 66 | E9 | 41 | I/O | General-purpose digital I/O with port interrupt and wake-up capability |
| | P5.3 | 67 | D7 | 42 | I/O | General-purpose digital I/O with port interrupt and wake-up capability |
| | P5.4 | 68 | D8 | 43 | I/O | General-purpose digital I/O with port interrupt and wake-up capability |
| | P5.5 | 69 | C8 | 44 | I/O | General-purpose digital I/O with port interrupt and wake-up capability |
| | P5.6 | 70 | D9 | 45 | I/O | General-purpose digital I/O with port interrupt and wake-up capability |
| | P5.7 | 71 | C9 | 46 | I/O | General-purpose digital I/O with port interrupt and wake-up capability |
| | P6.0 | 54 | J9 | N/A | I/O | General-purpose digital I/O with port interrupt and wake-up capability |
| | P6.1 | 55 | H7 | N/A | I/O | General-purpose digital I/O with port interrupt and wake-up capability |
| | P6.2 | 76 | A9 | N/A | I/O | General-purpose digital I/O with port interrupt and wake-up capability |
| | P6.3 | 77 | B9 | N/A | I/O | General-purpose digital I/O with port interrupt and wake-up capability |
| | P6.4 | 78 | A8 | N/A | I/O | General-purpose digital I/O with port interrupt and wake-up capability |
| | P6.5 | 79 | A7 | N/A | I/O | General-purpose digital I/O with port interrupt and wake-up capability |
| | P6.6 | 80 | B8 | 49 | I/O | General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability |
| | P6.7 | 81 | B7 | 50 | I/O | General-purpose digital I/O with port interrupt, wake-up, and glitch filtering capability |

表4-2。信号描述（续）

| FUNCTION | SIGNAL NAME | SIGNAL NO.(1) | | | SIGNAL TYPE(2) | DESCRIPTION |
|---|---|---|---|---|---|---|
| | | PZ | ZXH | RGC | | |
| GPIO (continued) | P7.0 | 88 | B5 | 57 | I/O | General-purpose digital I/O with reconfigurable port mapping secondary function (RD) |
| | P7.1 | 89 | C5 | 58 | I/O | General-purpose digital I/O with reconfigurable port mapping secondary function (RD) |
| | P7.2 | 90 | B4 | 59 | I/O | General-purpose digital I/O with reconfigurable port mapping secondary function (RD) |
| | P7.3 | 91 | A4 | 60 | I/O | General-purpose digital I/O with reconfigurable port mapping secondary function (RD) |
| | P7.4 | 26 | J1 | N/A | I/O | General-purpose digital I/O with reconfigurable port mapping secondary function (RD) |
| | P7.5 | 27 | H2 | N/A | I/O | General-purpose digital I/O with reconfigurable port mapping secondary function (RD) |
| | P7.6 | 28 | J2 | N/A | I/O | General-purpose digital I/O with reconfigurable port mapping secondary function (RD) |
| | P7.7 | 29 | G3 | N/A | I/O | General-purpose digital I/O with reconfigurable port mapping secondary function (RD) |
| | P8.0 30 H3 17 I / O通用数字I / O. | | | | | |
| | P8.1 31 G4 18 I / O通用数字I / O. | | | | | |
| | P8.2 46 N / A N / A I / O通用数字I / O. | | | | | |
| | P8.3 47 N / A N / A I / O通用数字I / O. | | | | | |
| | P8.4 48 N / A N / A I / O通用数字I / O. | | | | | |
| | P8.5 49 N / A N / A I / O通用数字I / O. | | | | | |
| | P8.6 50 N / A N / A I / O通用数字I / O. | | | | | |
| | P8.7 51 N / A N / A I / O通用数字I / O. | | | | | |
| | P9.0 52 N / A N / A I / O通用数字I / O. | | | | | |
| | P9.1 53 N / A N / A I / O通用数字I / O. | | | | | |
| | P9.2 74 N / A N / A I / O通用数字I / O. | | | | | |
| | P9.3 75 N / A N / A I / O通用数字I / O. | | | | | |
| | P9.4 96 N / A N / A I / O通用数字I / O. | | | | | |
| | P9.5 97 N / A N / A I / O通用数字I / O. | | | | | |
| | P9.6 98 N / A N / A I / O通用数字I / O. | | | | | |
| | P9.7 99 N / A N / A I / O通用数字I / O. | | | | | |
| | P10.0 100 N / A N / A I / O通用数字I / O. | | | | | |
| | P10.1 1 N / A N / A I / O通用数字I / O. | | | | | |
| | P10.2 2 N / A N / A I / O通用数字I / O. | | | | | |
| | P10.3 3 N / A N / A I / O通用数字I / O. | | | | | |
| | P10.4 24 N / A N / A I / O通用数字I / O. | | | | | |
| | P10.5 25 N / A N / A I / O通用数字I / O. | | | | | |
| | PJ.0 41 J6 28 I / O通用数字I / O. | | | | | |
| | PJ.1 42 J7 29 I / O通用数字I / O. | | | | | |
| | PJ.2 85 A6 54 I / O通用数字I / O. | | | | | |
| | PJ.3 86 A5 55 I / O通用数字I / O. | | | | | |
| | PJ.4 92 B3 61 I / O通用数字I / O. | | | | | |
| | PJ.5 93 A3 62 I / O通用数字I / O. | | | | | |

表4-2。信号描述（续）

| FUNCTION | SIGNAL NAME | SIGNAL NO.(1) | | | SIGNAL TYPE(2) | DESCRIPTION |
|---|---|---|---|---|---|---|
| | | PZ | ZXH | RGC | | |
| $I^2C$ | UCB0SCL | 11 | E1 | 8 | I/O | $I^2C$ clock – eUSCI_B0 $I^2C$ mode |
| | UCB0SDA | 10 | D1 | 7 | I/O | $I^2C$ data – eUSCI_B0 $I^2C$ mode |
| | UCB1SCL | 79 | A7 | N/A | I/O | $I^2C$ clock – eUSCI_B1 $I^2C$ mode |
| | UCB1SDA | 78 | A8 | N/A | I/O | $I^2C$ data – eUSCI_B1 $I^2C$ mode |
| | UCB3SCL | 3 | N/A | N/A | I/O | $I^2C$ clock – eUSCI_B3 $I^2C$ mode |
| | UCB3SCL | 81 | B7 | 50 | I/O | $I^2C$ clock – eUSCI_B3 $I^2C$ mode |
| | UCB3SDA | 2 | N/A | N/A | I/O | $I^2C$ data – eUSCI_B3 $I^2C$ mode |
| | UCB3SDA | 80 | B8 | 49 | I/O | $I^2C$ data – eUSCI_B3 $I^2C$ mode |

表4-2。信号描述（续）

| FUNCTION | SIGNAL NAME | SIGNAL NO.(1) | | | SIGNAL TYPE(2) | DESCRIPTION |
|---|---|---|---|---|---|---|
| | | PZ | ZXH | RGC | | |
| Port Mapper | PM_C0OUT 89 C5 58 O默认映射：Comparator E0输出 | | | | | |
| | PM_C1OUT 90 B4 59 O默认映射：Comparator E1输出 | | | | | |
| | PM_DMAE0 88 B5 57 I默认映射：DMA外部触发输入 | | | | | |
| | PM_SMCLK 88 B5 57 O默认映射：SMCLK时钟输出 | | | | | |
| | PM_TA0.0 | 91 | A4 | 60 | I/O | Default mapping: TA0 CCR0 capture: CCI0A input, compare: Out0 |
| | PM_TA0.1 | 20 | F3 | N/A | I/O | Default mapping: TA0 CCR1 capture: CCI1A input, compare: Out1 |
| | PM_TA0.2 | 21 | G1 | N/A | I/O | Default mapping: TA0 CCR2 capture: CCI2A input, compare: Out2 |
| | PM_TA0.3 | 22 | G2 | N/A | I/O | Default mapping: TA0 CCR3 capture: CCI3A input, compare: Out3 |
| | PM_TA0.4 | 23 | H1 | N/A | I/O | Default mapping: TA0 CCR4 capture: CCI4A input, compare: Out4 |
| | PM_TA0CLK 89 C5 58 I默认映射：TA0输入时钟 | | | | | |
| | PM_TA1.2 | 28 | J2 | N/A | I/O | Default mapping: TA1 CCR2 capture: CCI2A input, compare: Out2 |
| | PM_TA1.3 | 27 | H2 | N/A | I/O | Default mapping: TA1 CCR3 capture: CCI3A input, compare: Out3 |
| | PM_TA1.4 | 26 | J1 | N/A | I/O | Default mapping: TA1 CCR4 capture: CCI4A input, compare: Out4 |
| | PM_TA1CLK 90 B4 59 I默认映射：TA1输入时钟 | | | | | |
| | PM_UCA1CLK | 17 | F1 | 14 | I/O | 默认映射：时钟信号输入 - eUSCI_A1 SPI从机模式时钟信号输出 - eUSCI_A1 SPI主机模式 |
| | PM_UCA1RXD | 18 | E3 | 15 | I | Default mapping: Receive data – eUSCI_A1 UART mode |
| | PM_UCA1SIMO | 19 | F4 | 16 | I/O | Default mapping: Slave in, master out – eUSCI_A1 SPI mode |
| | PM_UCA1SOMI | 18 | E3 | 15 | I/O | Default mapping: Slave out, master in – eUSCI_A1 SPI mode |
| | PM_UCA1STE | 16 | E4 | 13 | I/O | Default mapping: Slave transmit enable – eUSCI_A1 SPI mode |
| | PM_UCA1TXD | 19 | F4 | 16 | O | Default mapping: Transmit data – eUSCI_A1 UART mode |
| | PM_UCA2CLK | 33 | H4 | 20 | I/O | 默认映射：时钟信号输入 - eUSCI_A2 SPI从机模式时钟信号输出 - eUSCI_A2 SPI主机模式 |
| | PM_UCA2RXD | 34 | G5 | 21 | I | Default mapping: Receive data – eUSCI_A2 UART mode |
| | PM_UCA2SIMO | 35 | J4 | 22 | I/O | Default mapping: Slave in, master out – eUSCI_A2 SPI mode |
| | PM_UCA2SOMI | 34 | G5 | 21 | I/O | Default mapping: Slave out, master in – eUSCI_A2 SPI mode |
| | PM_UCA2STE | 32 | J3 | 19 | I/O | Default mapping: Slave transmit enable – eUSCI_A2 SPI mode |
| | PM_UCA2TXD | 35 | J4 | 22 | O | Default mapping: Transmit data – eUSCI_A2 UART mode |

表4-2。信号描述（续）

| FUNCTION | SIGNAL NAME | SIGNAL NO.(1) | | | SIGNAL TYPE(2) | DESCRIPTION |
|---|---|---|---|---|---|---|
| | | PZ | ZXH | RGC | | |
| Port Mapper (continued) | PM_UCB2CLK | 37 | G6 | 24 | I/O | 默认映射：时钟信号输入 – eUSCI_B2 SPI从模式时钟信号输出 – eUSCI_B2 SPI主模式 |
| | PM_UCB2SCL | 39 | H6 | 26 | I | Default mapping: I2C clock – eUSCI_B2 I2C mode |
| | PM_UCB2SDA | 38 | J5 | 25 | I/O | Default mapping: I2C data – eUSCI_B2 I2C mode |
| | PM_UCB2SIMO | 38 | J5 | 25 | I/O | Default mapping: Slave in, master out – eUSCI_B2 SPI mode |
| | PM_UCB2SOMI | 39 | H6 | 26 | I/O | Default mapping: Slave out, master in – eUSCI_B2 SPI mode |
| | PM_UCB2STE | 36 | H5 | 23 | I/O | Default mapping: Slave transmit enable – eUSCI_B2 SPI mode |
| Power | AVCC1 | 45 | F6 | 32 | – | Analog power supply |
| | AVCC2 | 87 | D5 | 56 | – | Analog power supply |
| | AVSS1 | 43 | F5 | 30 | – | Analog ground supply |
| | AVSS2 | 84 | D6 | 53 | – | Analog ground supply |
| | AVSS3 | 40 | E5 | 27 | – | Analog ground supply |
| | DVCC1 | 13 | D2 | 10 | – | Digital power supply |
| | DVCC2 | 73 | C6 | 48 | – | Digital power supply |
| | DVSS1 | 15 | F2 | 12 | – | Digital ground supply |
| | DVSS2 | 72 | E6 | 47 | – | Digital ground supply |
| | DVSS3 82 C7 51 – 必须接地 | | | | | |
| | VCORE(3) | 12 | C2 | 9 | – | Regulated core power supply (internal use only, no external current loading) |
| | VSW 14 E2 11 – DC-DC转换器开关输出 | | | | | |
| RTC RTCCLK 59 G8 34 O RTC C时钟校准输出 | | | | | | |
| Reference | VREF + 70 D9 45 O内部共用参考电压正极 | | | | | |
| | VREF- 71 C9 46 O内部共用参考电压负端 | | | | | |
| | VeREF + 70 D9 45 I ADC外部参考电压的正极 | | | | | |
| | VeREF- | 71 | C9 | 46 | I | Negative terminal of external reference voltage to ADC (recommended to connect to onboard ground) |

（3）VCORE仅供内部使用。无需外部电流负载。 VCORE只应连接到推荐的电容值CVCORE。

表4-2。信号描述（续）

| FUNCTION | SIGNAL NAME | SIGNAL NO.(1) | | | SIGNAL TYPE(2) | DESCRIPTION |
|---|---|---|---|---|---|---|
| | | PZ | ZXH | RGC | | |
| SPI | UCA0CLK | 5 | B1 | 2 | I/O | Clock signal input – eUSCI_A0 SPI slave mode<br>Clock signal output – eUSCI_A0 SPI master mode |
| | UCA0SIMO 7 D4 4 I / O从机输入，主机输出 – eUSCI A0 SPI模式 | | | | | |
| | UCA0SOMI 6 C4 3 I / O从机输出，主机输入 – eUSCI_A0 SPI模式 | | | | | |
| | UCA0STE 4 A1 1 I / O从发送使能 – eUSCI_A0 SPI模式 | | | | | |
| | UCA3CLK | 97 | N/A | N/A | I/O | Clock signal input – eUSCI_A3 SPI slave mode<br>Clock signal output – eUSCI_A3 SPI master mode |
| | UCA3SIMO 99 N / A N / A I / O从机输入，主机输出 – eUSCI A3 SPI模式 | | | | | |
| | UCA3SOMI 98 N / A N / A I / O从机输出，主机输入 – eUSCI A3 SPI模式 | | | | | |
| | UCA3STE 96 N / A N / A I / O从发送使能 – eUSCI_A3 SPI模式 | | | | | |
| | UCB0CLK | 9 | C1 | 6 | I/O | Clock signal input – eUSCI_B0 SPI slave mode<br>Clock signal output – eUSCI_B0 SPI master mode |
| | UCB0SIMO 10 D1 7 I / O从机输入，主机输出 – eUSCI B0 SPI模式 | | | | | |
| | UCB0SOMI 11 E1 8 I / O从机输出，主机输入 – eUSCI B0 SPI模式 | | | | | |
| | UCB0STE 8 D3 5 I / O从发送使能 – eUSCI B0 SPI模式 | | | | | |
| | UCB1CLK | 77 | B9 | N/A | I/O | Clock signal input – eUSCI_B1 SPI slave mode<br>Clock signal output – eUSCI_B1 SPI master mode |
| | UCB1SIMO 78 A8 N / A I / O从机输入，主机输出 – eUSCI_B1 SPI模式 | | | | | |
| | UCB1SOMI 79 A7 N / A I / O从机输出，主机输入 – eUSCI B1 SPI模式 | | | | | |
| | UCB1STE 76 A9 N / A I / O从发送使能 – eUSCI B1 SPI模式 | | | | | |
| | UCB3CLK | 1 | N/A | N/A | I/O | Clock signal input – eUSCI_B3 SPI slave mode<br>Clock signal output – eUSCI_B3 SPI master mode |
| | UCB3CLK | 31 | G4 | 18 | I/O | Clock signal input – eUSCI_B3 SPI slave mode<br>Clock signal output – eUSCI_B3 SPI master mode |
| | UCB3SIMO 2 N / A N / A I / O从机输入，主机输出 – eUSCI_B3 SPI模式 | | | | | |
| | UCB3SIMO 80 B8 49 I / O从机输入，主机输出 – eUSCI B3 SPI模式 | | | | | |
| | UCB3SOMI 3 N / A N / A I / O从机输出，主机输入 – eUSCI B3 SPI模式 | | | | | |
| | UCB3SOMI 81 B7 50 I / O从机输出，主机输入 – eUSCI B3 SPI模式 | | | | | |
| | UCB3STE 30 H3 17 I / O从机发送使能 – eUSCI_B3 SPI模式 | | | | | |
| | UCB3STE 100 N / A N / A I / O从发送使能 – eUSCI_B3 SPI模式 | | | | | |
| System | NMI 83 B6 52 I外部不可屏蔽中断 | | | | | |
| | RSTn 83 B6 52 I外部复位（低电平有效） | | | | | |
| | SVMHOUT | 60 | G9 | 35 | O | SVMH output |
| 散热QFN焊盘N / A N / A焊盘 – QFN封装外露散热焊盘。 TI建议连接到VSS。 | | | | | | |

表4-2。信号描述（续）

| FUNCTION | SIGNAL NAME | SIGNAL NO.(1) | | | SIGNAL TYPE(2) | DESCRIPTION |
|---|---|---|---|---|---|---|
| | | PZ | ZXH | RGC | | |
| Timer | PM_TA1.1 | 29 | G3 | N/A | I/O | Default mapping: TA1 CCR1 capture: CCI1A input, compare: Out1 |
| | TA1.0 30 H3 17 I / O TA1 CCR0捕获：CCI0A输入，比较：Out0 | | | | | |
| | TA2.0 31 G4 18 I / O TA2 CCR0捕获：CCI0A输入，比较：Out0 | | | | | |
| | TA2.1 70 D9 45 I / O TA2 CCR1捕获：CCI1A输入，比较：Out1 | | | | | |
| | TA2.2 71 C9 46 I / O TA2 CCR2捕获：CCI2A输入，比较：Out2 | | | | | |
| | TA2.3 80 B8 49 I / O TA2 CCR3捕获：CCI3A输入，比较：Out3 | | | | | |
| | TA2.4 81 B7 50 I / O TA2 CCR4捕获：CCI4A输入，比较：Out4 | | | | | |
| | TA2CLK | 58 | G7 | 33 | I | TA2 input clock |
| | TA3.0 24 N / A N / A I / O TA3 CCR0捕获：CCI0A输入，比较：Out0 | | | | | |
| | TA3.1 25 N / A N / A I / O TA3 CCR1捕获：CCI1A输入，比较：Out1 | | | | | |
| | TA3.2 46 N / A N / A I / O TA3 CCR2捕获：CCI2A输入，比较：Out2 | | | | | |
| | TA3.3 74 N / A N / A I / O TA3 CCR3捕获：CCI3A输入，比较：Out3 | | | | | |
| | TA3.4 75 N / A N / A I / O TA3 CCR4捕获：CCI4A输入，比较：Out4 | | | | | |
| | TA3CLK | 47 | N/A | N/A | I | TA3 input clock |
| UART | UCA0RXD 6 C4 3 I接收数据 - eUSCI_A0 UART模式 | | | | | |
| | UCA0TXD 7 D4 4 O发送数据 - eUSCI_A0 UART模式 | | | | | |
| | UCA3RXD 98 N / A N / A I接收数据 - eUSCI_A3 UART模式 | | | | | |
| | UCA3TXD 99 N / A N / A O发送数据 - eUSCI_A3 UART模式 | | | | | |

## 4.4引脚复用

这些器件的引脚多路复用由寄存器设置和工作模式控制（例如，如果器件处于测试模式）。有关每个引脚的设置和多路复用端口的图表的详细信息，请参见第6.12节。

## 4.5缓冲类型

表4-3描述了表4-1中引用的缓冲区类型。

**Table 4-3. Buffer Type**

| BUFFER TYPE (STANDARD) | NOMINAL VOLTAGE | HYSTERESIS | PU OR PD | NOMINAL PU OR PD STRENGTH (µA) | OUTPUT DRIVE STRENGTH (mA) | OTHER CHARACTERISTICS |
|---|---|---|---|---|---|---|
| Analog(1) | 3.0 V | N | N/A | N/A | N/A | See analog modules in *Specifications* for details |
| HVCMOS | 13.0 V | Y | N/A | N/A | See *Typical Characteristics* | |
| LVCMOS | 3.0 V | Y(2) | Programmable | See *General-Purpose I/Os* | See *Typical Characteristics* | |
| Power (DVCC)(3) | 3.0 V | N | N/A | N/A | N/A | SVSMH enables hysteresis on DVCC |
| Power (AVCC)(3) | 3.0 V | N | N/A | N/A | N/A | |
| Power (DVSS and AVSS)(3) | 0 V | N | N/A | N/A | N/A | |

（1）这是一个开关，而不是一个缓冲区。
(2) Only for input pins
（3）这是电源输入，而不是缓冲器。

## 4.6未使用引脚的连接

表4-4列出了所有未使用引脚的正确终止。

**Table 4-4. Connection for Unused Pins(1)**

| PIN | POTENTIAL | COMMENT |
|---|---|---|
| AVCC | $DV_{CC}$ | |
| AVSS | $DV_{SS}$ | |
| Px.0至Px.7打开设置为端口功能，输出方向，并在PC板上保持未连接状态 | | |
| RSTn / NMI DVCC或VCC47kΩ上拉，1.1 nF下拉。 | | |
| PJ.4 / TDI开路JTAG TDI引脚与通用I / O功能（PJ.4）共用。如果不使用，该引脚应设置为端口功能，输出方向。当用作JTAG TDI引脚时，它应保持打开状态。 | | |
| PJ.5/TDO/SWO | $DV_{CC}$ or $V_{CC}$ | JTAG TDO / SWO引脚与通用I / O功能（PJ.5）共用。如果不使用，该引脚应设置为端口功能，输出方向。当用作JTAG TDO / SWO引脚时，应从外部下拉。 |
| SWDIOTMS DVCC或VCC该引脚应从外部上拉。 | | |
| SWCLKTCK DVSS或VSS该引脚应从外部下拉。 | | |

（1）对于具有与通用I / O共用的辅助功能的任何未使用引脚，请遵循Px.0至Px.7引脚的指导原则。

# 5规格

## 5.1 Absolute Maximum Ratings(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | MIN | MAX | UNIT |
|---|---|---|---|
| 在DVCC和AVCC引脚上施加的电压为VSS −0.3 4.17 V. DVCC和AVCC引脚之间的电压差（2）±0.3 V. | | | |
| Voltage applied to any pin(3) | –0.3 | $V_{CC}$ + 0.3 V (4.17 V MAX) | V |
| Diode current at any device pin | | ±2 | mA |
| Storage temperature, $T_{stg}$ (4) | –40 | 125 | °C |
| Maximum junction temperature, $T_J$ | | 95 | °C |

（1）超出绝对最大额定值下列出的应力可能会对器件造成永久性损坏。这些仅是应力额定值，并不暗示器件在这些或任何其他条件下的功能操作超出了推荐工作条件下指出的条件。长时间暴露在绝对最大额定条件下可能会影响器件的可靠性。
（2）DVCC和AVCC之间的电压差超过规定的限值可能导致设备故障。
（3）所有电压均以VSS为参考。
（4）根据当前的JEDEC J-STD-020规范，在板焊期间可能会施加更高的温度，峰值回流温度不高于运输箱或卷轴上设备标签上的分类。

## 5.2 ESD评级

| | | VALUE | UNIT |
|---|---|---|---|
| $V_{(ESD)}$ Electrostatic discharge | 人体模型（HBM），符合ANSI / ESDA / JEDEC JS-001（1）（2）±1000 | | V |
| | 充电器件型号（CDM），符合JEDEC规范JESD22-C101（3）±250 | | |

（1）JEDEC文件JEP 155规定，500 V HBM可通过标准ESD控制过程实现安全制造。列为±1000 V的引脚实际上可能具有更高的性能。
（2）除DVSS3外的所有引脚均通过HBM至±1000 V. DVSS3引脚用于TI内部测试。将DVSS3引脚连接到客户应用板上的电源地。
（3）JEDEC文件JEP 157规定250V CDM允许使用标准ESD控制过程进行安全制造。列为±250 V的引脚实际上可能具有更高的性能。

## 5.3推荐的操作条件

典型数据基于VCC = 3.0 V，TA = 25° C（除非另有说明）

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range at all DVCC and AVCC pins (1) (2) (3) | At power-up (with internal $V_{CC}$ supervision) | 1.71 | | 3.7 | V |
| | | Normal operation with internal $V_{CC}$ supervision | 1.71 | | 3.7 | |
| | | Normal operation without internal $V_{CC}$ supervision | 1.62 | | 3.7 | |
| 所有DVSS和AVSS引脚上的VSS电源电压为0 V. | | | | | | |
| $I_{INRUSH}$ | Inrush current into the $V_{CC}$ pins(4) | | | | 100 | mA |
| $f_{MCLK}$ | Frequency of the CPU and AHB clock in the system(5) | | 0 | | 48 | MHz |
| TA运行的自由空气温度-40 85° C TJ工作结温-40 85° C | | | | | | |

（1）TI建议从同一电源为AVCC和DVCC供电。在上电和运行期间，AVCC和DVCC之间的最大差值为±0.1 V. 有关去耦电容器建议，请参见第5.4节。
（2）电源电压的变化不得超过1 V / ms。即使在推荐的电源电压范围内，更快的更改也可能导致VCCDET触发复位。
（3）模块可能具有不同的电源电压范围规格。请参见本数据手册中相应模块的规范。
（4）不包括I / O电流（由应用要求驱动）
（5）工作频率可能要求以等待状态访问闪存。更多详细信息，请参见第5.8节。

## 5.4 Recommended External Components(1) (2) (3)

| | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $C_{DVCC}$ | Capacitor on DVCC pin | For DC-DC operation(4) | 3.3 | 4.7 | | µF |
| | | For LDO-only operation | 3.3 | 4.7 | | |
| $C_{VCORE}$ | Capacitor on VCORE pin | For DC-DC operation, including capacitor tolerance | 1.54 | 4.7 | 9 | µF |
| | | For LDO-only operation, including capacitor tolerance | 70 | 100 | 9000 | nF |
| $C_{AVCC}$ | Capacitor on AVCC pin | | 3.3 | 4.7 | | µF |
| LVSS和VCORE引脚之间的LVSW电感用于DC-DC 3.3 4.713 µH<br>RLVSW-DCR允许用于LVSW 150350mΩ的DCR | | | | | | |
| $I_{SAT-LVSW}$ | $L_{VSW}$ saturation current | | 700 | | | mA |

（1）为获得最佳性能，请选择组件值以匹配表中给出的典型值。
（2）有关元件选择、放置以及相关PCB设计指南的更多详细信息，请参见板上指南部分。
（3）选择元件时应考虑电容和电感值的容差，以确保不超过MIN和MAX限值。
（4）CDVCC不应小于CVCORE。

# 5.5运行模式VCC范围

over operating free-air temperature (unless otherwise noted)

| 参数操作模式测试条件MIN MAX单位 | | | | | |
|---|---|---|---|---|---|
| $V_{CC\_LDO}$ (1) (2) | AM_LDO_VCORE0<br>AM_LF_VCORE0<br>LPM0_LDO_VCORE0<br>LPM0_LF_VCORE0<br>LPM3_VCORE0<br>LPM4_VCORE0<br>LPM3.5<br>AM_LDO_VCORE1<br>AM_LF_VCORE1<br>LPM0_LDO_VCORE1<br>LPM0_LF_VCORE1<br>LPM3_VCORE1<br>LPM4_VCORE1 | LDO active, SVSMH disabled | 1.62 | 3.7 | V |
| | | LDO active, SVSMH enabled | 1.71 | 3.7 | |
| $V_{CC\_DCDC\_DF0}$ | AM_DCDC_VCORE0<br>LPM0_DCDC_VCORE0<br>AM_DCDC_VCORE1<br>LPM0_DCDC_VCORE1 | DC-DC active, DC-DC operation not forced (DCDC_FORCE = 0), SVSMH enabled or disabled(3) | 2.0 | 3.7 | V |
| $V_{CC\_DCDC\_DF1}$ | AM_DCDC_VCORE0<br>LPM0_DCDC_VCORE0<br>AM_DCDC_VCORE1<br>LPM0_DCDC_VCORE1 | DC-DC active, DC-DC operation forced (DCDC_FORCE = 1), SVSMH enabled or disabled | 1.8 | 3.7 | V |
| $V_{CC\_VCORE\_OFF}$ (4) | LPM4.5 | LDO disabled, SVSMH disabled | 1.62 | 3.7 | V |
| | | LDO disabled, SVSMH enabled | 1.71 | 3.7 | |

（1）仅存在于活动模式和LPM0模式下保持活动状态。
（2）低频有源、低频LPM0、LPM3、LPM4和LPM3.5模式仅基于LDO。
（3）当VCC低于规定的MIN值时，只要VCC下降速度低于可靠检测的速率，DC-DC操作就会自动切换到LDO。有关详细信息，请参阅表5-19。
（4）LPM4.5模式下的核心电压关闭。

## 5.6 Operating Mode CPU Frequency Ranges(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | OPERATING MODE | DESCRIPTION | $f_{MCLK}$ | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $f_{AM\_LDO\_VCORE0}$ | AM_LDO_VCORE0 | Normal performance mode with LDO as the active regulator | 0 | 24 | MHz |
| $f_{AM\_LDO\_VCORE1}$ | AM_LDO_VCORE1 | High performance mode with LDO as the active regulator | 0 | 48 | MHz |
| $f_{AM\_DCDC\_VCORE0}$ | AM_DCDC_VCORE0 | Normal performance mode with DC-DC as the active regulator | 0 | 24 | MHz |
| $f_{AM\_DCDC\_VCORE1}$ | AM_DCDC_VCORE1 | High performance mode with DC-DC as the active regulator | 0 | 48 | MHz |
| $f_{AM\_LF\_VCORE0}$ | AM_LF_VCORE0 | Low-frequency mode with LDO as the active regulator | 0 | 128 | kHz |
| $f_{AM\_LF\_VCORE1}$ | AM_LF_VCORE1 | Low-frequency mode with LDO as the active regulator | 0 | 128 | kHz |

（1）DMA可以与CPU相同的频率运行。

# 5.7工作模式外围频率范围

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数操作模式描述MIN MAX单元 | | | | | |
|---|---|---|---|---|---|
| $f_{AM\_LPM0\_VCORE0}$ | AM_LDO_VCORE0 | 基于LDO或DC-DC的有源或LPM0模式的外设频率范围，适用于VCORE0 0 12 MHz | | | |
| | AM_DCDC_VCORE0 | | | | |
| | LPM0_LDO_VCORE0 | | | | |
| | LPM0_DCDC_VCORE0 | | | | |
| $f_{AM\_LPM0\_VCORE1}$ | AM_LDO_VCORE1 | 基于LDO或DC-DC的有源或LPM0模式的外设频率范围，适用于VCORE1 0 24 MHz | | | |
| | AM_DCDC_VCORE1 | | | | |
| | LPM0_LDO_VCORE1 | | | | |
| | LPM0_DCDC_VCORE1 | | | | |
| $f_{AM\_LPM0\_LF}$ | AM_LF_VCORE0 | VCORE0和VCORE1的低频有效或低频LPM0模式下的外设频率范围 | 0 | 128 | kHz |
| | AM_LF_VCORE1 | | | | |
| | LPM0_LF_VCORE0 | | | | |
| | LPM0_LF_VCORE1 | | | | |
| $f_{LPM3}$(1) | LPM3_VCORE0 | Peripheral frequency in LPM3 mode for VCORE0 and VCORE1 | 0 | 32.768 | kHz |
| | LPM3_VCORE1 | | | | |
| $f_{LPM3.5}$(1) | LPM3.5 | Peripheral frequency in LPM3.5 mode | 0 | 32.768 | kHz |

（1）只有RTC和WDT可以激活。

## 5.8操作模式执行频率与闪存等待状态要求

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | NUMBER OF FLASH WAIT STATES | FLASH READ MODE | MAXIMUM SUPPORTED MCLK FREQUENCY(1) (2) | | UNIT |
|---|---|---|---|---|---|
| | | | AM_LDO_VCORE0, AM_DCDC_VCORE0 | AM_LDO_VCORE1, AM_DCDC_VCORE1 | |
| $f_{MAX\_NRM\_FLWAIT0}$ | 0 | Normal read mode | 16 | 24 | MHz |
| $f_{MAX\_NRM\_FLWAIT1}$ | 1 | Normal read mode | 24 | 48 | MHz |
| $f_{MAX\_ORM\_FLWAIT0}$ | 0 | Other read modes(3) | 8 | 12 | MHz |
| $f_{MAX\_ORM\_FLWAIT1}$ | 1 | Other read modes(3) | 16 | 24 | MHz |
| $f_{MAX\_ORM\_FLWAIT2}$ | 2 | Other read modes(3) | 24 | 36 | MHz |
| $f_{MAX\_ORM\_FLWAIT3}$ | 3 | Other read modes(3) | 24 | 48 | MHz |

（1）违反给定等待状态配置的最大频率限制会导致不确定数据或从闪存中取出指令。

（2）在低频有效模式下，始终可以在零等待状态下访问闪存，因为最大MCLK频率限制为128 kHz。

（3）其他读取模式是指读取裕度0，读取裕度1，程序验证和擦除验证。

## 5.9器件复位期间的电流消耗

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1) (2) (3)

| PARAMETER | | $V_{CC}$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{RESET}$ | Current during device reset | 2.2 V | | 510 | | µA |
| | | 3.0 V | | 600 | 850 | |

（1）器件通过RSTn / NMI引脚保持复位状态。

（2）电流测量到VCC

（3）所有其他输入引脚连接到0 V或VCC。输出不会提供或同步任何电流。

## 5.10基于LDO的有源模式下的电流消耗 – Dhrystone 2.1程序

over recommended operating free-air temperature (unless otherwise noted)(1) (2) (3) (4) (5)

| PARAMETER | EXECUTION MEMORY | $V_{CC}$ | MCLK = 1 MHz | | MCLK = 8 MHz | | MCLK = 16 MHz | | MCLK = 24 MHz | | MCLK = 32 MHz | | MCLK = 40 MHz | | MCLK = 48 MHz | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{AM\_LDO\_VCORE0,Flash}$(6) (7) (8) | Flash | 3.0 V | 490 | 625 | 1500 | 1700 | 2650 | 2950 | 3580 | 3900 | | | | | | | µA |
| $I_{AM\_LDO\_VCORE1,Flash}$(6) (7) (8) | Flash | 3.0 V | 510 | 685 | 1650 | 1900 | 2970 | 3300 | 4260 | 4700 | 5300 | 5800 | 6500 | 7100 | 7700 | 8400 | µA |
| $I_{AM\_LDO\_VCORE0,SRAM}$(9) | SRAM | 3.0 V | 435 | 565 | 1070 | 1240 | 1800 | 2010 | 2530 | 2800 | | | | | | | µA |
| $I_{AM\_LDO\_VCORE1,SRAM}$(9) | SRAM | 3.0 V | 450 | 620 | 1160 | 1370 | 1980 | 2250 | 2800 | 3120 | 3650 | 4020 | 4470 | 4900 | 5280 | 5760 | µA |

（1）由DCO采购的MCLK。

（2）电流测量到VCC

（3）所有其他输入引脚连接到0 V或VCC。输出不会提供或同步任何电流。

（4）所有SRAM库保持活动状态。

（5）所有外围设备都处于非活动状态。

（6）执行Dhrystone 2.1程序的设备。从flash执行代码。 SRAM中的堆栈和数据。

（7）闪存配置为支持在给定频率和核心电压电平下操作所需的最小等待状态。

（8）使能Flash指令和数据缓冲区（BUFI = BUFD = 1）。

（9）执行Dhrystone 2.1程序的设备。从SRAM执行代码。 SRAM中的堆栈和数据。

## 5.11基于DC-DC的有源模式下的电流消耗 – Dhrystone 2.1程序

over recommended operating free-air temperature (unless otherwise noted)(1) (2) (3) (4) (5)

| PARAMETER | EXECUTION MEMORY | $V_{CC}$ | MCLK = 1 MHz | | MCLK = 8 MHz | | MCLK = 16 MHz | | MCLK = 24 MHz | | MCLK = 32 MHz | | MCLK = 40 MHz | | MCLK = 48 MHz | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{AM\_DCDC\_VCORE0,Flash}$ (6) (7) (8) | Flash | 3.0 V | 400 | 475 | 925 | 1050 | 1530 | 1720 | 2060 | 2300 | | | | | | | µA |
| $I_{AM\_DCDC\_VCORE1,Flash}$ (6) (7) (8) | Flash | 3.0 V | 430 | 550 | 1100 | 1280 | 1880 | 2140 | 2650 | 3000 | 3290 | 3700 | 4020 | 4500 | 4720 | 5300 | µA |
| $I_{AM\_DCDC\_VCORE0,SRAM}$ (9) | SRAM | 3.0 V | 370 | 450 | 680 | 780 | 1040 | 1180 | 1410 | 1600 | | | | | | | µA |
| $I_{AM\_DCDC\_VCORE1,SRAM}$ (9) | SRAM | 3.0 V | 390 | 510 | 790 | 940 | 1250 | 1440 | 1720 | 1960 | 2200 | 2480 | 2670 | 3000 | 3050 | 3420 | µA |

（1）由DCO采购的MCLK。
（2）电流测量到VCC
（3）所有其他输入引脚连接到0 V或VCC。输出不会提供或同步任何电流。
（4）所有SRAM组都有效。
（5）所有外围设备都处于非活动状态。
（6）执行Dhrystone 2.1程序的设备。从flash执行代码。 SRAM中的堆栈和数据。
（7）闪存配置为支持在给定频率和核心电压电平下操作所需的最小等待状态。
（8）使能Flash指令和数据缓冲区（RUFT = RUFD = 1）。
（9）执行Dhrystone 2.1程序的设备。从SRAM执行代码。 SRAM中的堆栈和数据。

## 5.12低频有源模式下的电流消耗 – Dhrystone 2.1程序

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2) (3) (4) (5)

| PARAMETER | EXECUTION MEMORY | $V_{CC}$ | –40°C | | 25°C | | 60°C | | 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{AM\_LF\_VCORE0,\ Flash}$ (6) (7) (8) | Flash | 2.2 V | 75 | 80 | 95 | 115 | | | | | µA |
| | | 3.0 V | 78 | 83 | 100 | 98 | 118 | 200 | | | |
| $I_{AM\_LF\_VCORE1,\ Flash}$ (6) (7) (8) | Flash | 2.2 V | 78 | 85 | 105 | 125 | | | | | µA |
| | | 3.0 V | 81 | 88 | 110 | 108 | 128 | 245 | | | |
| $I_{AM\_LF\_VCORE0,\ SRAM}$ (9) | SRAM | 2.2 V | 68 | 73 | 90 | 105 | | | | | µA |
| | | 3.0 V | 71 | 76 | 92 | 93 | 108 | 190 | | | |
| $I_{AM\_LF\_VCORE1,\ SRAM}$ (9) | SRAM | 2.2 V | 70 | 77 | 98 | 117 | | | | | µA |
| | | 3.0 V | 73 | 90 | 102 | 101 | 120 | 235 | | | |

（1）电流测量到VCC
（2）所有其他输入引脚连接到0 V或VCC。输出不会提供或同步任何电流。
(3) MCLK, HSMCLK, and SMCLK sourced by REFO at 128 kHz
（4）所有外围设备都处于非活动状态。
（5）SRAM存储区0和1启用从闪存执行，SRAM存储区0到3启用从SRAM执行。
（6）Flash配置为0等待状态。
（7）执行Dhrystone 2.1程序的设备。从flash执行代码。 SRAM中的堆栈和数据。
（8）使能Flash指令和数据缓冲区（RUFT = RUFD = 1）。
（9）执行Dhrystone 2.1程序的设备。从SRAM执行代码。 SRAM中的堆栈和数据。

## 5.13 CoreMark程序的有源模式电流的典型特性

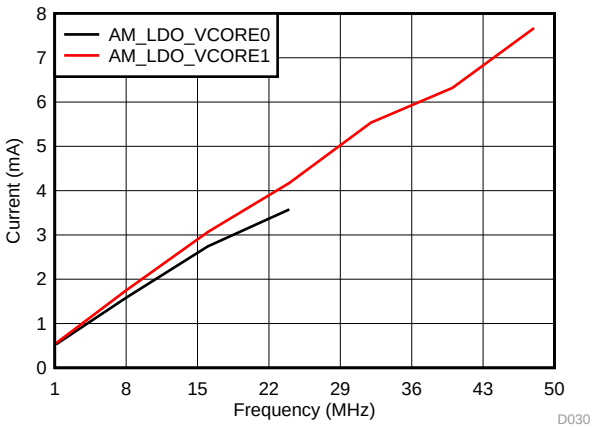



图5-1。频率与电流消耗

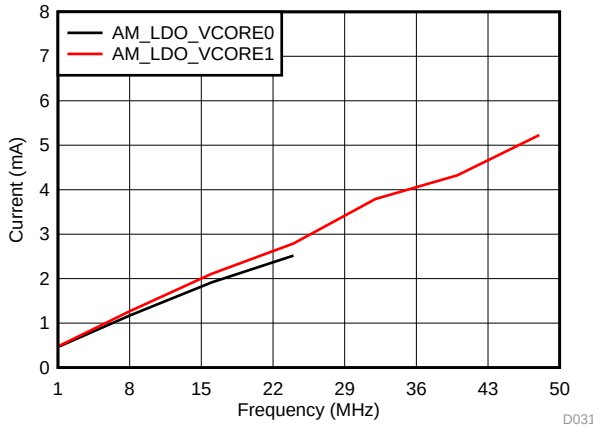



图5-2。频率与电流消耗

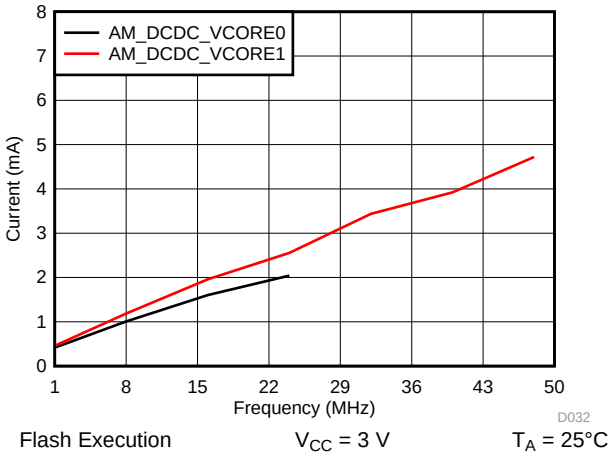



图5-3。频率与电流消耗

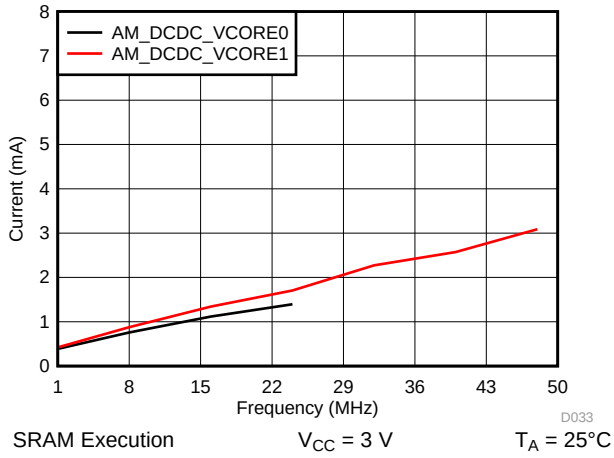
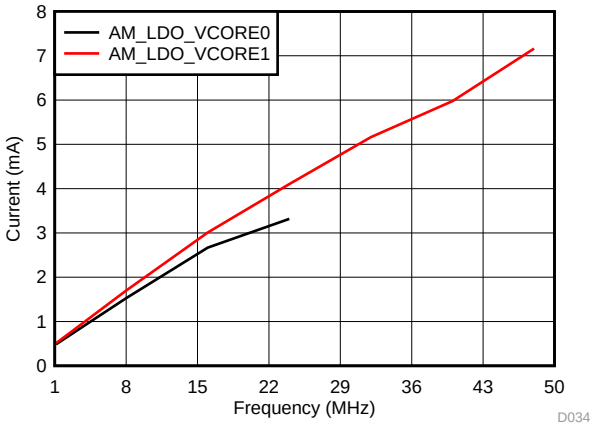


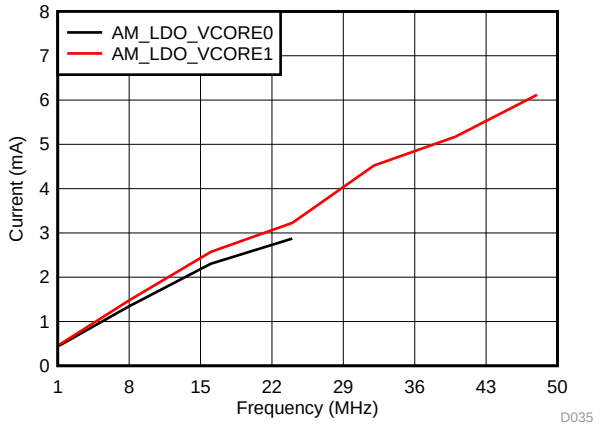

图5-4。频率与电流消耗

# 5.14素数程序的有源模式电流的典型特性



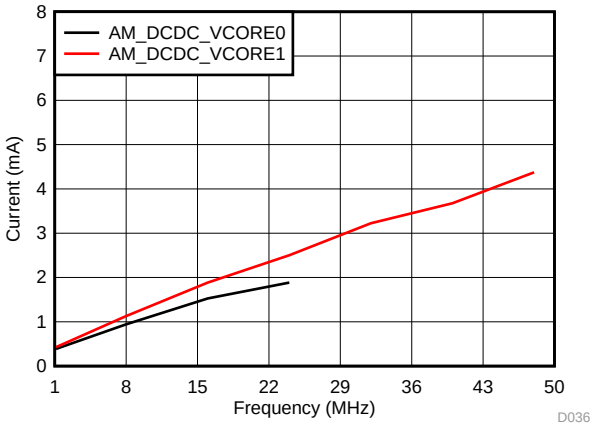

Flash Execution $V_{CC}$ = 3 V $T_A$ = 25°C

图5-5。频率与电流消耗



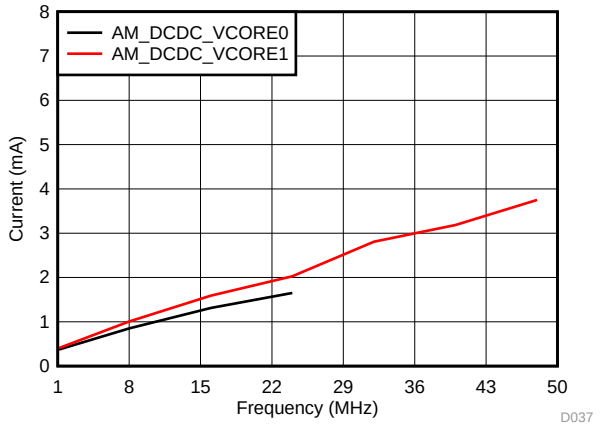

SRAM Execution $V_{CC}$ = 3 V $T_A$ = 25°C

图5-6。频率与电流消耗




Flash Execution $V_{CC}$ = 3 V $T_A$ = 25°C

图5-7。频率与电流消耗




SRAM Execution $V_{CC}$ = 3 V $T_A$ = 25°C

图5-8。频率与电流消耗

## 5.15 Fibonacci程序的有源模式电流的典型特性

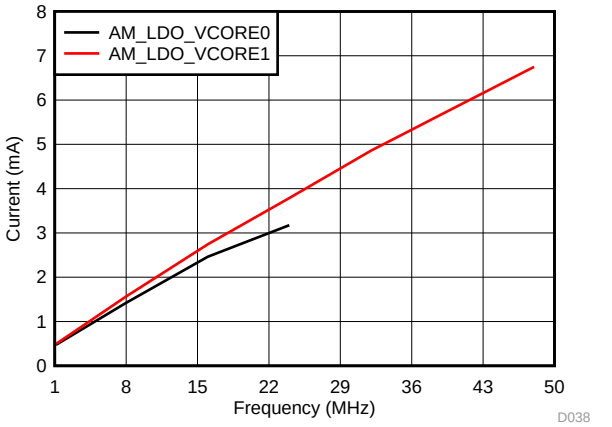



图5-9。频率与电流消耗

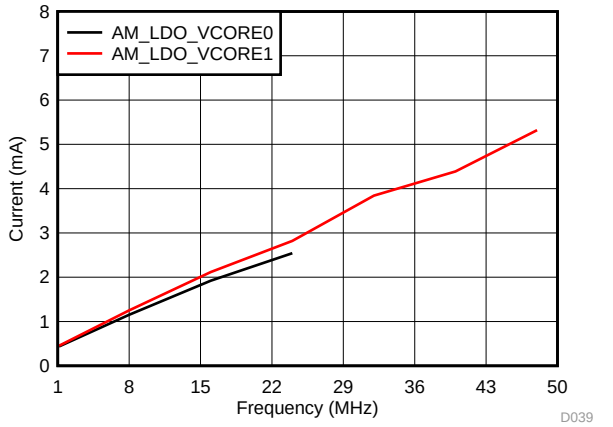



图5-10。频率与电流消耗

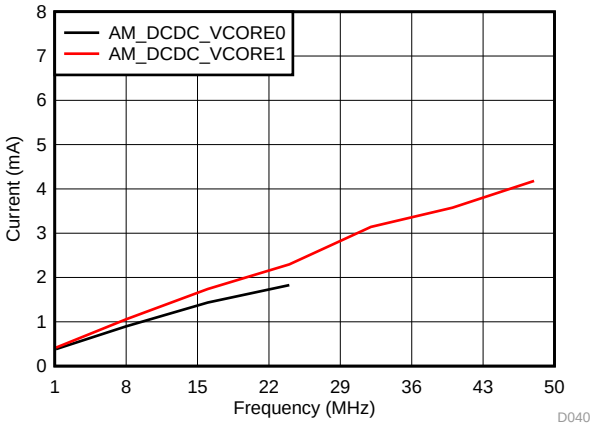



图5-11。频率与电流消耗

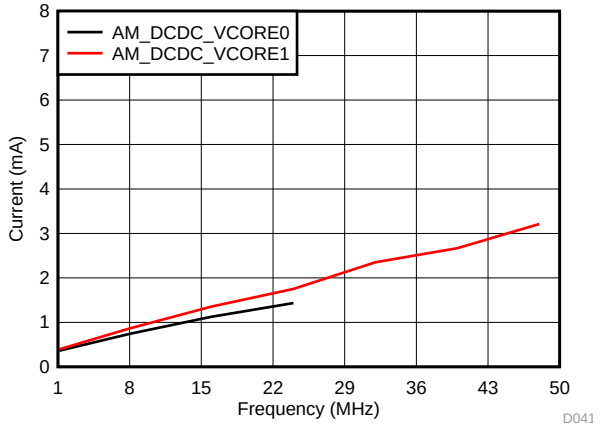
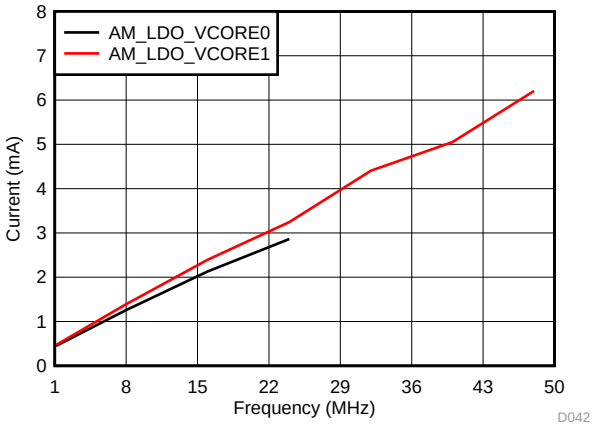


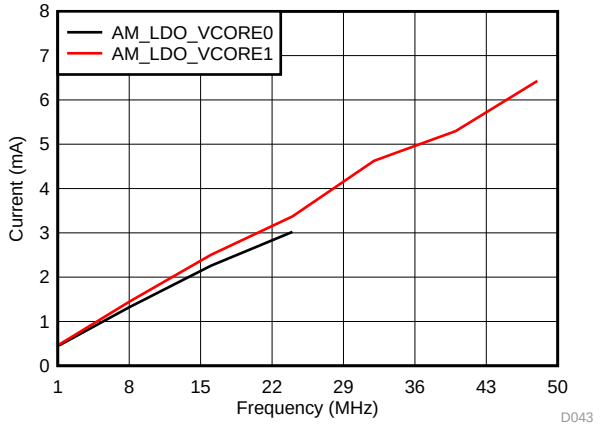

图5-12。频率与电流消耗

# 5.16 While（1）程序的有源模式电流的典型特性



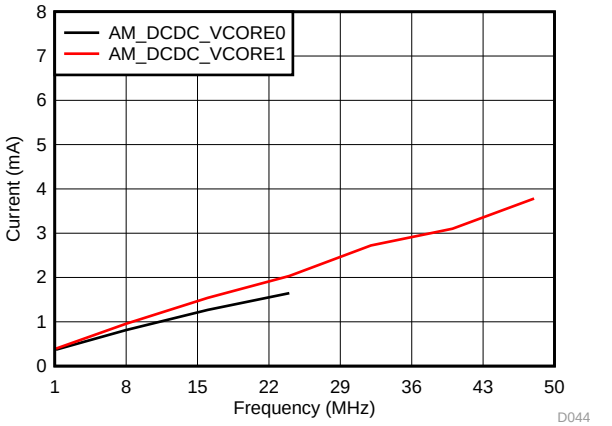

Flash Execution $V_{CC}$ = 3 V $T_A$ = 25°C

图5-13。频率与电流消耗



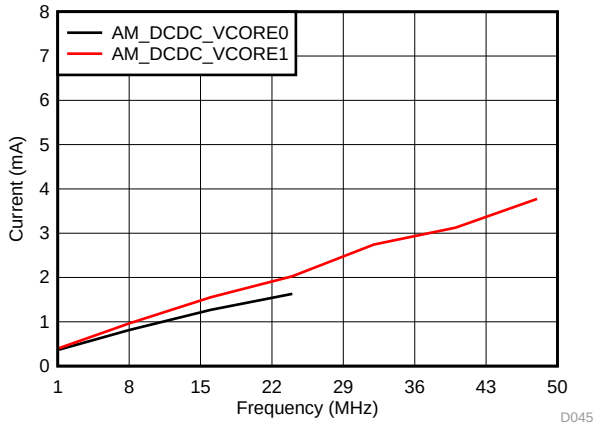

SRAM Execution $V_{CC}$ = 3 V $T_A$ = 25°C

图5-14。频率与电流消耗




Flash Execution $V_{CC}$ = 3 V $T_A$ = 25°C

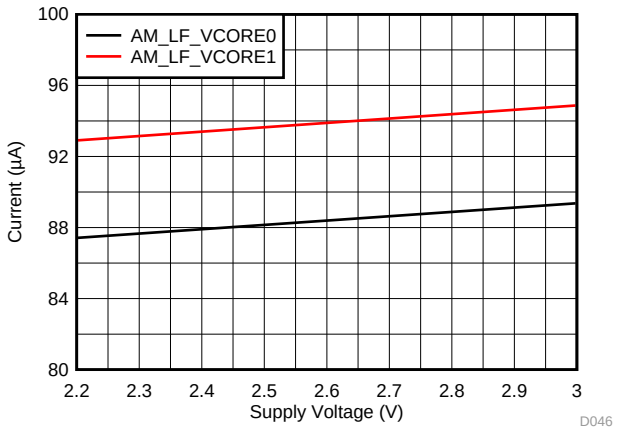
图5-15。频率与电流消耗




SRAM Execution $V_{CC}$ = 3 V $T_A$ = 25°C

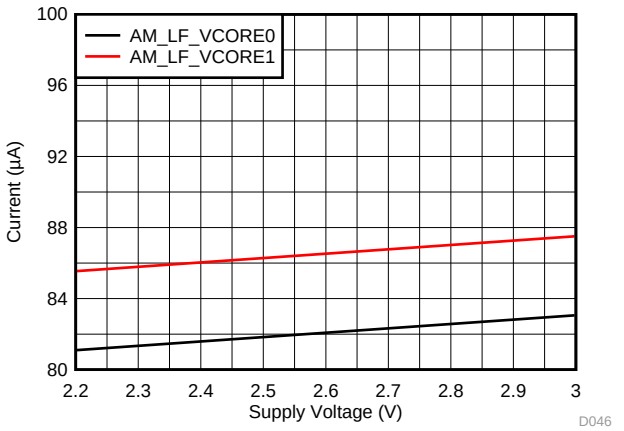
图5-16。频率与电流消耗

## 5.17 CoreMark程序的低频有源模式电流的典型特性




Flash Execution $T_A$ = 25°C MCLK = 128 kHz

图5-17。电源电压与电流消耗




SRAM Execution $T_A$ = 25°C MCLK = 128 kHz

图5-18。电源电压与电流消耗

## 5.18基于LDO的LPM0模式下的电流消耗

over recommended operating free-air temperature (unless otherwise noted)(1) (2) (3) (4) (5) (6)

| PARAMETER | $V_{CC}$ | MCLK = 1 MHz | | MCLK = 8 MHz | | MCLK = 16 MHz | | MCLK = 24 MHz | | MCLK = 32 MHz | | MCLK = 40 MHz | | MCLK = 48 MHz | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM0\_LDO\_VCORE0}$ | 2.2 V | 355 | 485 | 465 | 605 | 590 | 735 | 710 | 860 | | | | | | | µA |
| | 3.0 V | 355 | 485 | 465 | 605 | 590 | 735 | 710 | 860 | | | | | | | |
| $I_{LPM0\_LDO\_VCORE1}$ | 2.2 V | 365 | 530 | 495 | 665 | 640 | 820 | 775 | 970 | 965 | 1160 | 1130 | 1330 | 1235 | 1450 | µA |
| | 3.0 V | 365 | 530 | 495 | 665 | 640 | 820 | 775 | 970 | 965 | 1160 | 1130 | 1330 | 1230 | 1450 | |

（1）由DCO采购的MCLK。
（2）电流测量到VCC
（3）所有其他输入引脚连接到0 V或VCC。输出不会提供或同步任何电流。
（4）CPU关闭。无法访问闪存和SRAM。
（5）所有SRAM组都有效。
（6）所有外围设备都处于非活动状态。

## 5.19基于DC-DC的LPM0模式下的电流消耗

over recommended operating free-air temperature (unless otherwise noted)(1) (2) (3) (4) (5) (6)

| PARAMETER | $V_{CC}$ | MCLK = 1 MHz | | MCLK = 8 MHz | | MCLK = 16 MHz | | MCLK = 24 MHz | | MCLK = 32 MHz | | MCLK = 40 MHz | | MCLK = 48 MHz | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM0\_DCDC\_VCORE0}$ | 2.2 V | 330 | 425 | 400 | 510 | 485 | 600 | 570 | 690 | | | | | | | µA |
| | 3.0 V | 325 | 400 | 380 | 460 | 440 | 530 | 510 | 610 | | | | | | | |
| $I_{LPM0\_DCDC\_VCORE1}$ | 2.2 V | 350 | 485 | 445 | 590 | 555 | 710 | 660 | 820 | 810 | 970 | 935 | 1110 | 1020 | 1200 | µA |
| | 3.0 V | 345 | 450 | 420 | 530 | 500 | 620 | 585 | 720 | 700 | 830 | 800 | 940 | 870 | 1020 | |

（1）由DCO采购的MCLK。
（2）电流测量到VCC
（3）所有其他输入引脚连接到0 V或VCC。输出不会提供或同步任何电流。
（4）CPU关闭。无法访问闪存和SRAM。
（5）所有SRAM组都有效。
（6）所有外围设备都处于非活动状态。

## 5.20低频LPM0模式下的电流消耗

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2) (3) (4) (5) (6)

| PARAMETER | $V_{CC}$ | –40°C | | 25°C | | 60°C | | 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM0\_LF\_VCORE0}$ | 2.2 V | 58 | 63 | 78 | 94 | | | | | µA |
| | 3.0 V | 61 | 66 | 82 | 81 | 97 | 180 | | | |
| $I_{LPM0\_LF\_VCORE1}$ | 2.2 V | 60 | 66 | 84 | 104 | | | | | µA |
| | 3.0 V | 63 | 69 | 90 | 87 | 107 | 220 | | | |

（1）电流测量到VCC
（2）所有其他输入引脚连接到0 V或VCC。输出不会提供或同步任何电流。
（3）由REFO以128 kHz提供的MCLK，HSMCLK和SMCLK。
（4）所有外围设备都处于非活动状态。
（5）SRAM的Bank 0保持活动状态。其余的银行都倒闭了。
（6）CPU关闭。无法访问闪存和SRAM。

## 5.21 LPM3，LPM4模式下的电流消耗

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2) (3) (4) (5) (6)

| PARAMETER | $V_{CC}$ | –40°C | | 25°C | | 60°C | | 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM3\_VCORE0\_RTCLF}$ (7) (8) | 2.2 V | 0.52 | | 0.64 | | 1.11 | | 2.43 | | µA |
| | 3.0 V | 0.54 | 0.66 | 0.85 | 1.13 | 2.46 | 5 | | | |
| $I_{LPM3\_VCORE0\_RTCREFO}$ (9) (8) | 2.2 V | 0.85 | | 1.07 | | 1.55 | | 2.89 | | µA |
| | 3.0 V | 0.95 | 1.16 | 1.35 | 1.64 | 2.98 | 5.6 | | | |
| $I_{LPM3\_VCORE1\_RTCLF}$ (7) (8) | 2.2 V | 0.72 | | 0.93 | | 1.47 | | 2.95 | | µA |
| | 3.0 V | 0.75 | 0.95 | 1.35 | 1.5 | 2.98 | 6 | | | |
| $I_{LPM3\_VCORE1\_RTCREFO}$ (9) (8) | 2.2 V | 1.04 | | 1.3 | | 1.87 | | 3.34 | | µA |
| | 3.0 V | 1.14 | 1.4 | 1.7 | 1.96 | 3.44 | 6.5 | | | |
| $I_{LPM4\_VCORE0}$ (10) | 2.2 V | 0.37 | | 0.48 | | 0.92 | | 2.19 | | µA |
| | 3.0 V | 0.4 | 0.5 | 0.65 | 0.94 | 2.2 | 4.8 | | | |
| $I_{LPM4\_VCORE1}$ (10) | 2.2 V | 0.54 | | 0.7 | | 1.2 | | 2.58 | | µA |
| | 3.0 V | 0.56 | 0.72 | 0.98 | 1.23 | 2.6 | 5.6 | | | |

（1）电流测量到VCC。
（2）所有其他输入引脚连接到0 V或VCC。输出不会提供或同步任何电流。
（3）CPU关闭，闪存灯关机。
（4）SRAM的Bank 0保留，所有其他bank都断电。
（5）有关为保留启用的每个额外Bank的额外电流消耗的详细信息，请参阅表5-47。
（6）SVSMH被禁用。
（7）由LFXT采购的RTC。 LF晶体的有效负载电容为3.7 pF。
（8）WDT模块被禁用。
（9）由REFO采购的RTC。
（10）禁用RTC和WDT模块。

## 5.22 LPM3.5，LPM4.5模式下的电流消耗

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

| PARAMETER | $V_{CC}$ | –40°C | | 25°C | | 60°C | | 85°C | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | TYP | MAX | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM3.5\_RTCLF}$ (3) (4) (5) (6) (7) | 2.2 V | 0.48 | | 0.6 | | 1.07 | | 2.36 | | µA |
| | 3.0 V | 0.5 | 0.63 | 0.81 | 1.1 | 2.38 | 4.9 | | | |
| $I_{LPM3.5\_RTCREFO}$ (3) (4) (8) (6) (7) | 2.2 V | 0.82 | | 1.03 | | 1.52 | | 2.81 | | µA |
| | 3.0 V | 0.92 | 1.12 | 1.3 | 1.61 | 2.9 | 5.5 | | | |
| $I_{LPM4.5}$ (9) (7) | 2.2 V | 10 | | 20 | | 45 | | 125 | | nA |
| | 3.0 V | 15 | 25 | 35 | 50 | 150 | 300 | | | |

（1）电流测量到VCC。
（2）所有其他输入引脚连接到0 V或VCC。输出不会提供或同步任何电流。
（3）CPU和闪存断电。
（4）SRAM的Bank 0保留，所有其他bank断电。
（5）由LFXT采购的RTC。 LF晶体的有效负载电容为3.7 pF。
（6）WDT模块被禁用。
（7）SVSMH被禁用。
（8）REFO采购的RTC。
（9）无核心电压。 CPU，闪存和所有SRAM组都断电。

## 5.23数字外设的电流消耗

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

| PARAMETER | TEST CONDITIONS | TYP | MAX | UNIT |
|---|---|---|---|---|
| ITIMER_A Timer_A配置为PWM定时器，占空比为50%，转换为50 µA/ MHz | | | | |
| $I_{TIMER32}$ | Timer32 enabled | 3.5 | | µA/MHz |
| IUART eUSCI A配置为UART模式6.5 µA/ MHz<br>ISPI eUSCI_A配置为SPI主模式5 µA/ MHz | | | | |
| $I_{I2C}$ | eUSCI_B configured in $I^2C$ master mode | 5 | | µA/MHz |
| IWDT A WDT A配置为间隔定时器模式6 µA/ MHz<br>IRTC_C RTC_C使能并来自32-kHz LFXT 100 nA | | | | |
| $I_{AES256}$ | AES256 active | 19 | | µA/MHz |
| $I_{CRC32}$ | CRC32 active | 2 | | µA/MHz |

(1) Measured with VCORE = 1.2 V

## 5.24热阻特性

| THERMAL METRICS(1) | | PACKAGE | VALUE(2) | UNIT |
|---|---|---|---|---|
| $R\theta_{JA}$ | Junction-to-ambient thermal resistance, still air(3) | LQFP-100 (PZ) | 50.9 | °C/W |
| $R\theta_{JC(TOP)}$ | Junction-to-case (top) thermal resistance(4) | | 9.7 | °C/W |
| $R\theta_{JB}$ | Junction-to-board thermal resistance(5) | | 27.2 | °C/W |
| $\Psi_{JB}$ | Junction-to-board thermal characterization parameter | | 26.9 | °C/W |
| $\Psi_{JT}$ | Junction-to-top thermal characterization parameter | | 0.2 | °C/W |
| $R\theta_{JC(BOTTOM)}$ | Junction-to-case (bottom) thermal resistance(6) | | N/A | °C/W |
| $R\theta_{JA}$ | Junction-to-ambient thermal resistance, still air(3) | NFBGA-80 (ZXH) | 58.1 | °C/W |
| $R\theta_{JC(TOP)}$ | Junction-to-case (top) thermal resistance(4) | | 26.1 | °C/W |
| $R\theta_{JB}$ | Junction-to-board thermal resistance(5) | | 22.6 | °C/W |
| $\Psi_{JB}$ | Junction-to-board thermal characterization parameter | | 22.0 | °C/W |
| $\Psi_{JT}$ | Junction-to-top thermal characterization parameter | | 0.5 | °C/W |
| $R\theta_{JC(BOTTOM)}$ | Junction-to-case (bottom) thermal resistance(6) | | N/A | °C/W |
| $R\theta_{JA}$ | Junction-to-ambient thermal resistance, still air(3) | VQFN-64 (RGC) | 29.4 | °C/W |
| $R\theta_{JC(TOP)}$ | Junction-to-case (top) thermal resistance(4) | | 14.8 | °C/W |
| $R\theta_{JB}$ | Junction-to-board thermal resistance(5) | | 8.3 | °C/W |
| $\Psi_{JB}$ | Junction-to-board thermal characterization parameter | | 8.2 | °C/W |
| $\Psi_{JT}$ | Junction-to-top thermal characterization parameter | | 0.2 | °C/W |
| $R\theta_{JC(BOTTOM)}$ | Junction-to-case (bottom) thermal resistance(6) | | 1.0 | °C/W |

（1）有关传统和新热指标的更多信息，请参阅半导体和IC封装热指标。

(2) N/A = not applicable

（3）在JESD51-2a中描述的环境中，在JESD51-7中规定的JEDEC标准High-K板的模拟中获得自然对流下的结至环境热阻。

（4）通过在封装顶部模拟冷板测试获得结至壳体（顶部）热阻。没有特定的JEDEC标准测试，但可以在ANSI SEMI标准G30-88中找到详细描述。

（5）如JESD51-8中所述，通过在具有环形冷板夹具的环境中模拟以控制PCB温度来获得结到板的热阻。

（6）通过在暴露的（电源）焊盘上模拟冷板测试来获得结至壳体（底部）热阻。没有特定的JEDEC标准测试，但可以在ANSI SEMI标准G30-88中找到详细描述。

# 5.25定时和开关特性

## 5.25.1复位时序

表5-1列出了从不同类型的重置中恢复的延迟。

**Table 5-1. Reset Recovery Latencies**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{SOFT}$ | Latency from release of soft reset to first CPU instruction fetch | | 5 | | MCLK cycles |
| $t_{HARD}$ | Latency from release of hard reset to release of soft reset | | 25 | | MCLK cycles |
| $t_{POR}$ | Latency from release of device POR to release of hard reset | | 15 | 25 | µs |
| $t_{COLDPWR,100\ nF}$ | Latency from a cold power-up condition to release of device POR, $C_{VCORE}$ = 100 nF | | 300 | 400 | µs |
| $t_{COLDPWR,4.7\ µF}$ | Latency from a cold power-up condition to release of device POR, $C_{VCORE}$ = 4.7 µF | | 400 | 500 | µs |

(1) See Section 6.8.1 for details on the various classes of resets on the device

表5-2列出了从RSTn引脚上施加的外部复位恢复的延迟。

表5-2。外部重置恢复延迟（1）

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|
| $t_{AM\_RSTn}$ | External reset applied when device is in LDO or DC-DC based active modes, MCLK = 1 to 48 MHz | | 5 | ms |
| $t_{AMLF\_RSTn,\ 128\ kHz}$ | External reset applied when device is in low-frequency active modes, MCLK = 128 kHz | | 5.5 | ms |
| $t_{AMLF\_RSTn,\ 32\ kHz}$ | External reset applied when device is in low-frequency active modes, MCLK = 32.768 kHz | | 6.5 | ms |
| $t_{LPM0\_RSTn}$ | External reset applied when device is in LDO or DC-DC based LPM0 modes, MCLK = 1 to 48 MHz | | 5 | ms |
| $t_{LPM0LF\_RSTn,\ 128\ kHz}$ | External reset applied when device is in low-frequency LPM0 modes, MCLK = 128 kHz | | 5.5 | ms |
| $t_{LPM0LF\_RSTn,\ 32\ kHz}$ | External reset applied when device is in low-frequency LPM0 modes, MCLK = 32.768 kHz | | 6.5 | ms |
| $t_{LPM3\_LPM4\_RSTn}$ | External reset applied when device is in LPM3 or LPM4 modes, MCLK = 24 or 48 MHz while entering LPM3 or LPM4 modes | | 5 | ms |
| $t_{LPMx.5\_RSTn}$ | External reset applied when device is in LPM3.5 or LPM4.5 modes | | 5 | ms |

（1）在RSTn引脚上施加外部复位，并且从外部复位的释放到用户应用代码的启动来测量延迟。

## 5.25.2模式转换时序

表5-3列出了在不同活动模式之间切换所需的延迟。

表5-3。活动模式转换延迟

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | ORIGINAL OPERATING MODE | FINAL OPERATING MODE | TEST CONDITIONS | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{OFF\_AMLDO0}$ | Power Off | AM_LDO_VCORE0 | From $V_{CC}$ reaching 1.71 V to start of user application code | | 6 | ms |
| $t_{AMLDO0\_AMLDO1}$ | AM_LDO_VCORE0 | AM_LDO_VCORE1 | Transition from AM_LDO_VCORE0 to AM_LDO_VCORE1 MCLK frequency = 24 MHz | 300 | 350 | µs |
| $t_{AMLDO1\_AMLDO0}$ | AM_LDO_VCORE1 | AM_LDO_VCORE0 | Transition from AM_LDO_VCORE1 to AM_LDO_VCORE0 MCLK frequency = 24 MHz | 4 | 5 | µs |
| $t_{AMLDO0\_AMDCDC0}$ | AM_LDO_VCORE0 | AM_DCDC_VCORE0 | Transition from AM_LDO_VCORE0 to AM_DCDC_VCORE0 MCLK frequency = 24 MHz | 20 | 30 | µs |
| $t_{AMDCDC0\_AMLDO0}$ | AM_DCDC_VCORE0 | AM_LDO_VCORE0 | Transition from AM_DCDC_VCORE0 to AM_LDO_VCORE0 MCLK frequency = 24 MHz | 10 | 15 | µs |
| $t_{AMLDO1\_AMDCDC1}$ | AM_LDO_VCORE1 | AM_DCDC_VCORE1 | Transition from AM_LDO_VCORE1 to AM_DCDC_VCORE1 MCLK frequency = 48 MHz | 20 | 30 | µs |
| $t_{AMDCDC1\_AMLDO1}$ | AM_DCDC_VCORE1 | AM_LDO_VCORE1 | Transition from AM_DCDC_VCORE1 to AM_LDO_VCORE1 MCLK frequency = 48 MHz | 10 | 15 | µs |
| $t_{AMLDO0\_AMLF0}$ | AM_LDO_VCORE0 | AM_LF_VCORE0 | Transition from AM_LDO_VCORE0 to AM_LF_VCORE0 SELM = 2, REFO frequency = 128 kHz | 90 | 100 | µs |
| $t_{AMLF0\_AMLDO0}$ | AM_LF_VCORE0 | AM_LDO_VCORE0 | Transition from AM_LF_VCORE0 to AM_LDO_VCORE0 SELM = 2, REFO frequency = 128 kHz | 50 | 60 | µs |
| $t_{AMLDO1\_AMLF1}$ | AM_LDO_VCORE1 | AM_LF_VCORE1 | Transition from AM_LDO_VCORE1 to AM_LF_VCORE1 SELM = 2, REFO frequency = 128 kHz | 90 | 100 | µs |
| $t_{AMLF1\_AMLDO1}$ | AM_LF_VCORE1 | AM_LDO_VCORE1 | Transition from AM_LF_VCORE1 to AM_LDO_VCORE1 SELM = 2, REFO frequency = 128 kHz | 50 | 60 | µs |

表5-4列出了在不同的活动模式和LPM0模式之间切换所需的延迟。

表5-4。 LPM0模式转换延迟

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | ORIGINAL OPERATING MODE | FINAL OPERATING MODE | TEST CONDITIONS | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{AMLDOx\_LPM0LDOx}$ (1) | AM_LDO_VCOREx | LPM0_LDO_VCOREx | Transition from AM_LDO_VCORE0 or AM_LDO_VCORE1 to LPM0_LDO_VCORE0 or LPM0_LDO_VCORE1 | 1 | | MCLK cycles |
| $t_{LPM0LDOx\_AMLDOx}$ (2) | LPM0_LDO_VCOREx | AM_LDO_VCOREx | Transition from LPM0_LDO_VCORE0 or LPM0_LDO_VCORE1 to AM_LDO_VCORE0 or AM_LDO_VCORE1 through I/O interrupt | 3 | 4 | MCLK cycles |
| $t_{AMDCDCx\_LPM0DCDCx}$ (1) | AM_DCDC_VCOREx | LPM0_DCDC_VCOREx | Transition from AM_DCDC_VCORE0 or AM_DCDC_VCORE1 to LPM0_DCDC_VCORE0 or LPM0_DCDC_VCORE1 | 1 | | MCLK cycles |
| $t_{LPM0DCDCx\_AMDCDCx}$ (2) | LPM0_DCDC_VCOREx | AM_DCDC_VCOREx | Transition from LPM0_DCDC_VCORE0 or LPM0_DCDC_VCORE1 to AM_DCDC_VCORE0 or AM_DCDC_VCORE1 through I/O interrupt | 3 | 4 | MCLK cycles |
| $t_{AMLFx\_LPM0LFx}$ (1) | AM_LF_VCOREx | LPM0_LF_VCOREx | Transition from AM_LF_VCORE0 or AM_LF_VCORE1 to LPM0_LF_VCORE0 or LPM0_LF_VCORE1 | 1 | | MCLK cycles |
| $t_{LPM0LFx\_AMLFx}$ (2) | LPM0_LF_VCOREx | AM_LF_VCOREx | Transition from LPM0_LF_VCORE0 or LPM0_LF_VCORE1 to AM_LF_VCORE0 or AM_LF_VCORE1 through I/O interrupt | 3 | 4 | MCLK cycles |

（1）这是CPU执行WFI指令到CPU输出外断言SLEEPING信号之间的延迟。
（2）这是I / O中断事件与CPU输出时SLEEPING信号无效之间的延迟。

表5-5列出了在不同的活动模式和LPM3或LPM4模式之间切换所需的延迟。

表5-5。 LPM3，LPM4模式转换延迟

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | ORIGINAL OPERATING MODE | FINAL OPERATING MODE | TEST CONDITIONS | | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{AMLDO0\_LPMx0}$ (1) | AM_LDO_VCORE0 | LPM3_LPM4_VCORE0 | Transition from AM_LDO_VCORE0 to LPM3 or LPM4 at VCORE0 | SELM = 3. DCO frequency = 24 MHz | 22 | 24 | µs |
| $t_{LPMx0\_AMLDO0\_NORIO}$ (2) | LPM3_LPM4_VCORE0 | AM_LDO_VCORE0 | Transition from LPM3 or LPM4 at VCORE0 to AM_LDO_VCORE0 through wake-up event from nonglitch filter type I/O | SELM = 3. DCO frequency = 24 MHz | 8 | 9 | µs |
| $t_{LPMx0\_AMLDO0\_GFLTIO}$ (2) | LPM3_LPM4_VCORE0 | AM_LDO_VCORE0 | Transition from LPM3 or LPM4 at VCORE0 to AM_LDO_VCORE0 through wake-up event from glitch filter type I/O, GLTFLT_EN = 1 | SELM = 3. DCO frequency = 24 MHz | 9 | 10 | µs |
| $t_{AMLDO1\_LPMx1}$ (1) | AM_LDO_VCORE1 | LPM3_LPM4_VCORE1 | Transition from AM_LDO_VCORE1 to LPM3 or LPM4 at VCORE1 | SELM = 3. DCO frequency = 48 MHz | 21 | 23 | µs |
| $t_{LPMx1\_AMLDO1\_NORIO}$ (2) | LPM3_LPM4_VCORE1 | AM_LDO_VCORE1 | Transition from LPM3 or LPM4 at VCORE1 to AM_LDO_VCORE1 through wake-up event from nonglitch filter type I/O | SELM = 3. DCO frequency = 48 MHz | 7.5 | 8 | µs |
| $t_{LPMx1\_AMLDO1\_GFLTIO}$ (2) | LPM3_LPM4_VCORE1 | AM_LDO_VCORE1 | Transition from LPM3 or LPM4 at VCORE1 to AM_LDO_VCORE1 through wake-up event from glitch filter type I/O, GLTFLT_EN = 1 | SELM = 3. DCO frequency = 48 MHz | 8 | 9 | µs |
| $t_{AMLFx\_LPMx\_128k}$ (1) | AM_LF_VCOREx | LPM3_LPM4_VCOREx | Transition from AM_LF_VCORE0 or AM_LF_VCORE1 to LPM3 or LPM4 at VCORE0/1 | SELM = 2. REFO frequency = 128 kHz | 240 | 260 | µs |
| $t_{AMLFx\_LPMx\_32k}$ (1) | AM_LF_VCOREx | LPM3_LPM4_VCOREx | Transition from AM_LF_VCORE0 or AM_LF_VCORE1 to LPM3 or LPM4 at VCORE0/1 | SELM = 0. LFXT frequency = 32.768 kHz | 880 | 900 | µs |
| $t_{LPMx\_AMLFx\_NORIO\_128k}$ (2) | LPM3_LPM4_VCOREx | AM_LF_VCOREx | Transition from LPM3 or LPM4 at VCORE0/1 to AM_LF_VCORE0 or AM_LF_VCORE1 through wake-up event from nonglitch filter type I/O | SELM = 2. REFO frequency = 128 kHz | 45 | 50 | µs |
| $t_{LPMx\_AMLFx\_NORIO\_32k}$ (2) | LPM3_LPM4_VCOREx | AM_LF_VCOREx | Transition from LPM3 or LPM4 at VCORE0/1 to AM_LF_VCORE0 or AM_LF_VCORE1 through wake-up event from nonglitch filter type I/O | SELM = 0. LFXT frequency = 32.768 kHz | 150 | 170 | µs |

（1）这是从CPU到LPM3或LPM4条目执行WFI指令的延迟

（2）这是从I / O唤醒事件到器件引脚MCLK时钟启动的延迟。

表5-6列出了更改为LPM3.5和LPM4.5模式所需的延迟。

表5-6。 LPM3.5，LPM4.5模式转换延迟

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | ORIGINAL OPERATING MODE | FINAL OPERATING MODE | TEST CONDITIONS | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{AMLDOx\_LPM3.5}$ (1) | AM_LDO_VCOREx | LPM3.5 | Transition from AM_LDO_VCORE0 or AM_LDO_VCORE1 to LPM3.5 | 25 | 30 | µs |
| $t_{AMDCDCx\_LPM3.5}$ (1) | AM_DCDC_VCOREx | LPM3.5 | Transition from AM_DCDC_VCORE0 or AM_DCDC_VCORE1 to LPM3.5 | 35 | 50 | µs |
| $t_{AMLFx\_LPM3.5}$ (1) | AM_LF_VCOREx | LPM3.5 | Transition from AM_LF_VCORE0 or AM_LF_VCORE1 to LPM3.5 | 225 | 250 | µs |
| $t_{AMLDOx\_LPM4.5}$ (2) | AM_LDO_VCOREx | LPM4.5 | Transition from AM_LDO_VCORE0 or AM_LDO_VCORE1 to LPM4.5 | 25 | 30 | µs |
| $t_{AMDCDCx\_LPM4.5}$ (2) | AM_DCDC_VCOREx | LPM4.5 | Transition from AM_DCDC_VCORE0 or AM_DCDC_VCORE1 to LPM4.5 | 35 | 50 | µs |
| $t_{AMLFx\_LPM4.5}$ (2) | AM_LF_VCOREx | LPM4.5 | Transition from AM_LF_VCORE0 or AM_LF_VCORE1 to LPM4.5 | 250 | 270 | µs |
| $t_{LPM3.5\_AMLDO0}$ (3) | LPM3.5 | AM_LDO_VCORE0 | Transition from LPM3.5 to AM_LDO_VCORE0 | 0.7 | 0.8 | ms |
| $t_{LPM4.5\_AMLDO0\_SVSMON,\ 100\ nF}$ (3) | LPM4.5 | AM_LDO_VCORE0 | Transition from LPM4.5 to AM_LDO_VCORE0, SVSMH enabled while in LPM4.5, $C_{VCORE}$ = 100 nF | 0.8 | 0.9 | ms |
| $t_{LPM4.5\_AMLDO0\_SVSMON,\ 4.7\ µF}$ (3) | LPM4.5 | AM_LDO_VCORE0 | Transition from LPM4.5 to AM_LDO_VCORE0, SVSMH enabled while in LPM4.5, $C_{VCORE}$ = 4.7 µF | 0.9 | 1 | ms |
| $t_{LPM4.5\_AMLDO0\_SVSMOFF,\ 100\ nF}$ (3) | LPM4.5 | AM_LDO_VCORE0 | Transition from LPM4.5 to AM_LDO_VCORE0, SVSMH disabled while in LPM4.5, $C_{VCORE}$ = 100 nF | 1 | 1.1 | ms |
| $t_{LPM4.5\_AMLDO0\_SVSMOFF,\ 4.7\ µF}$ (3) | LPM4.5 | AM_LDO_VCORE0 | Transition from LPM4.5 to AM_LDO_VCORE0, SVSMH disabled while in LPM4.5, $C_{VCORE}$ = 4.7 µF | 1.1 | 1.2 | ms |

（1）这是从CPU到LPM3.5模式进入的WFI指令执行的延迟。
（2）这是从CPU执行WFI指令到LPM4.5模式进入的延迟。
（3）这是从I / O唤醒事件到用户应用程序代码启动的延迟。

## 5.25.3时钟规范

表5-7列出了低频晶体振荡器LFXT的输入要求。

表5-7。低频晶体振荡器，LFXT，推荐工作条件

over operating free-air temperature range (unless otherwise noted)

| 参数测试条件MIN TYP MAX UNIT | | | | | | |
|---|---|---|---|---|---|---|
| ESR晶体等效串联电阻fOSC = 32.768 kHz 16 4065kΩ | | | | | | |
| $C_{LFXT}$ | Capacitance from LFXT input to ground and from LFXT output to ground(1) | | 7.4 | 12 | 24 | pF |
| CSHUNT晶体分流电容0.6 0.8 1.6 pF | | | | | | |
| Cm晶体运动电容1 2 10 fF | | | | | | |

（1）不包括板寄生虫。封装和电路板为CLFXT增加了额外的电容。

表5-8列出了低频晶体振荡器LFXT的特性。

表5-8。 LFXT低频晶体振荡器

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数测试条件VCC MIN TYP MAX UNIT | | | | | | |
|---|---|---|---|---|---|---|
| $I_{VCC,LFXT}$ | Current consumption(1) | $f_{OSC}$ = 32.768 kHz, LFXTBYPASS = 0, LFXTDRIVE = {0}, $C_{L,eff}$ = 3.7 pF, Typical ESR and $C_{SHUNT}$ | 3.0 V | | 100 | nA |
| | | $f_{OSC}$ = 32.768 kHz, LFXTBYPASS = 0, LFXTDRIVE = {1}, $C_{L,eff}$ = 6 pF, Typical ESR and $C_{SHUNT}$ | | | 120 | |
| | | $f_{OSC}$ = 32.768 kHz, LFXTBYPASS = 0, LFXTDRIVE = {2}, $C_{L,eff}$ = 9 pF, Typical ESR and $C_{SHUNT}$ | | | 150 | |
| | | $f_{OSC}$ = 32.768 kHz, LFXTBYPASS = 0, LFXTDRIVE = {3}, $C_{L,eff}$ = 12 pF, Typical ESR and $C_{SHUNT}$ | | | 170 | |
| $f_{LFXT}$ | LFXT oscillator crystal frequency | LFXTBYPASS = 0(2) | | | 32.768 | kHz |
| $DC_{LFXT}$ | LFXT oscillator duty cycle | $f_{LFXT}$ = 32.768 kHz(2) | | 30% | 70% | |
| $f_{LFXT,SW}$ | LFXT oscillator logic-level square-wave input frequency | LFXTBYPASS = 1(3) (4) | | 10 | 32.768 50 | kHz |
| DCLFXT, SW | LFXT oscillator logic-level square-wave input duty cycle | LFXTBYPASS = 1 | | 30% | 70% | |
| $OA_{LFXT}$ | Oscillation allowance for LF crystals(5) | LFXTBYPASS = 0, LFXTDRIVE = {1}, $f_{LFXT}$ = 32.768 kHz, $C_{L,eff}$ = 6 pF | | 200 | 240 | kΩ |
| | | LFXTBYPASS = 0, LFXTDRIVE = {3}, $f_{LFXT}$ = 32.768 kHz, $C_{L,eff}$ = 12 pF | | 300 | 340 | |

（1）AVCC和DVCC电源的总电流测量值。

（2）以ACLK引脚测量。

（3）当LFXTBYPASS置位时，LFXT电路自动断电。输入信号是数字方波，参数在本数据手册的施密特触发器输入部分中定义。占空比要求由DCLFXT，SW定义。

（4）不能超过整个设备的最大工作频率。

（5）振荡余量基于推荐晶体的安全系数5。振荡容限是LFXTDRIVE设置和有效负载的函数。通常，可以根据以下指南实现可比较的振荡器容差，但应根据为应用选择的实际晶体进行评估：•对于LFXTDRIVE = {0}，CL，eff = 3.7 pF。

- •对于LFXTDRIVE = {1}，6pF≤CL，eff≤9pF。
- •对于LFXTDRIVE = {2}，6pF≤CL，eff≤10pF。
- •对于LFXTDRIVE = {3}，6pF≤CL，eff≤12pF。

表5-8。低频晶体振荡器，LFXT（续）

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数测试条件VCC | | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $C_{LFXIN}$ | Integrated load capacitance at LFXIN terminal(6) (7) | | | | 2 | | pF |
| $C_{LFXOUT}$ | Integrated load capacitance at LFXOUT terminal(6) (7) | | | | 2 | | pF |
| $t_{START,LFXT}$ | Start-up time(8) | $f_{OSC}$ = 32.768 kHz, LFXTBYPASS = 0, LFXTDRIVE = {0}, $C_{L,eff}$ = 3.7 pF, Typical ESR and $C_{SHUNT}$, FCNTLF_EN = 0(2) | 3.0 V | | 1.1 | | s |
| | | $f_{OSC}$ = 32.768 kHz, LFXTBYPASS = 0, LFXTDRIVE = {3}, $C_{L,eff}$ = 12 pF, Typical ESR and $C_{SHUNT}$, FCNTLF_EN = 0(2) | | | 1.3 | | |
| $f_{Fault,LFXT}$ | Oscillator fault frequency(9) (10) | | | 1 | | 3 | kHz |

（6）这表示分别存在于LFXIN和LFXOUT端子的所有寄生电容，包括寄生键和封装电容。有效负载电容CL，eff可以计算为CIN x COUT /（CIN + COUT），其中CIN和COUT分别是LFXIN和LFXOUT端子的总电容。

（7）两个端子都需要外部电容，以满足晶体制造商规定的有效负载电容。支持的推荐有效负载电容值为3.7 pF，6 pF，9 pF和12 pF。最大分流电容为1.6 pF。由于PCB增加了额外的电容，因此还必须考虑整体电容。TI建议验证是否满足所选晶振的推荐有效负载电容。

（8）不包括可编程启动计数器

（9）高于MAX规范的频率不设置故障标志。

MIN和MAX规范之间的频率可以设置标志，静态条件或者在故障状态下将设置故障标志。

（10）用逻辑电平输入频率测量，但也适用于晶体操作。

表5-9列出了高频晶体振荡器HFXT的输入要求。

表5-9。高频晶体振荡器，HFXT，推荐工作条件

over operating free-air temperature range (unless otherwise noted)

| 参数测试条件MIN | | | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| ESR | Crystal equivalent series resistance | $f_{OSC}$ = 1 MHz to ≤4 MHz | 75 | 150 | Ω |
| | | $f_{OSC}$ = >4 MHz to ≤8 MHz | 75 | 150 | |
| | | $f_{OSC}$ = >8 MHz to ≤16 MHz | 40 | 80 | |
| | | $f_{OSC}$ = >16 MHz to ≤24 MHz | 30 | 60 | |
| | | $f_{OSC}$ = >24 MHz to ≤32 MHz | 20 | 40 | |
| | | $f_{OSC}$ = >32 MHz to ≤48 MHz | 15 | 30 | |
| $C_{HFXT}$ | Capacitance from HFXT input to ground and from HFXT output to ground | $f_{OSC}$ = 1 MHz to 48 MHz | 28 | 32 36 | pF |

CSHUNT晶体并联电容fOSC = 1 MHz至48 MHz 1 3 7 pF

Cm晶体运动电容fOSC = 1 MHz至48 MHz 3 7 30 fF

表5-10列出了高频晶体振荡器HFXT的特性。

表5-10。高频晶体振荡器，HFXT

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数测试条件VCC | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| $I_{DVCC,HFXT}$ HFXT oscillator crystal current HF mode at typical ESR | $f_{OSC}$ = 1 MHz, HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 0, $C_{L,eff}$ = 16 pF, Typical ESR and $C_{SHUNT}$ | 3.0 V | | 40 | µA |
| | $f_{OSC}$ = 4 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 0, $C_{L,eff}$ = 16 pF, Typical ESR and $C_{SHUNT}$ | | | 60 | |
| | $f_{OSC}$ = 8 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 1, $C_{L,eff}$ = 16 pF, Typical ESR and $C_{SHUNT}$ | | | 100 | |
| | $f_{OSC}$ = 16 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 2, $C_{L,eff}$ = 16 pF, Typical ESR and $C_{SHUNT}$ | | | 180 | |
| | $f_{OSC}$ = 24 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 3, $C_{L,eff}$ = 16 pF, Typical ESR and $C_{SHUNT}$ | | | 260 | |
| | $f_{OSC}$ = 32 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 4, $C_{L,eff}$ = 16 pF, Typical ESR and $C_{SHUNT}$ | | | 320 | |
| | $f_{OSC}$ = 40 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 5, $C_{L,eff}$ = 16 pF, Typical ESR and $C_{SHUNT}$ | | | 480 | |
| | $f_{OSC}$ = 48 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 6, $C_{L,eff}$ = 16 pF, Typical ESR and $C_{SHUNT}$ | | | 550 | |
| $f_{HFXT}$ HFXT oscillator crystal frequency, crystal mode | HFXTBYPASS = 0, HFFREQ = 0 (1) | | 1 | 4 | MHz |
| | HFXTBYPASS = 0, HFFREQ = 1 (1) | | 4.01 | 8 | |
| | HFXTBYPASS = 0, HFFREQ = 2 (1) | | 8.01 | 16 | |
| | HFXTBYPASS = 0, HFFREQ = 3 (1) | | 16.01 | 24 | |
| | HFXTBYPASS = 0, HFFREQ = 4 (1) | | 24.01 | 32 | |
| | HFXTBYPASS = 0, HFFREQ = 5 (1) | | 32.01 | 40 | |
| | HFXTBYPASS = 0, HFFREQ = 6 (1) | | 40.01 | 48 | |
| $DC_{HFXT}$ HFXT oscillator duty cycle | Measured at MCLK or HSMCLK, $f_{HFXT}$ = 1 MHz to 48 MHz | | 40% | 50% 60% | |
| $f_{HFXT,SW}$ HFXT oscillator logic-level square-wave input frequency, bypass mode | HFXTBYPASS = 1 (1)(2) | | 0.8 | 48 | MHz |
| $DC_{HFXT, SW}$ HFXT oscillator logic-level square-wave input duty cycle | HFXTBYPASS = 1，外部时钟用作MCLK或HSMCLK的直接源，没有分频器（DIVM = 0或DIVHS = 0）。 | | 45% | 55% | |
| | HFXTBYPASS = 1，外部时钟用作MCLK或HSMCLK的直接源，带有分频器（DIVM> 0或DIVHS> 0）或不用作MCLK或HSMCLK的直接源。 | | 40% | 60% | |

（1）不能超过整个设备的最大工作频率

（2）当设置HFXTBYPASS时，HFXT电路自动断电。输入信号是数字方波，参数在本数据手册的施密特触发器输入部分中定义。占空比要求由DCHFXT，SW定义。

表5-10。高频晶体振荡器，HFXT（续）

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数测试条件VCC | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| $OA_{HFXT}$ Oscillation allowance for HFXT crystals(3) | HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 0, $f_{HFXT,HF}$ = 1 MHz, $C_{L,eff}$ = 16 pF | | 1225 | 5000 | Ω |
| | HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 0, $f_{HFXT,HF}$ = 4 MHz, $C_{L,eff}$ = 16 pF | | 640 | 1250 | |
| | HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 1, $f_{HFXT,HF}$ = 8 MHz, $C_{L,eff}$ = 16 pF | | 360 | 750 | |
| | HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 2, $f_{HFXT,HF}$ = 16 MHz, $C_{L,eff}$ = 16 pF | | 200 | 425 | |
| | HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 3, $f_{HFXT,HF}$ = 24 MHz, $C_{L,eff}$ = 16 pF | | 135 | 275 | |
| | HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 4, $f_{HFXT,HF}$ = 32 MHz, $C_{L,eff}$ = 16 pF | | 110 | 225 | |
| | HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 5 $f_{HFXT,HF}$ = 40 MHz, $C_{L,eff}$ = 16 pF | | 105 | 160 | |
| | HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 6, $f_{HFXT,HF}$ = 48 MHz, $C_{L,eff}$ = 16 pF | | 80 | 140 | |

（3）振荡余量基于推荐晶体的安全系数5。

## 表5-10。高频晶体振荡器，HFXT（续）

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数测试条件VCC | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| $t_{START,HFXT}$ Start-up time(4) | $f_{OSC}$ = 1 MHz, HFXTBYPASS = 0, HFXTDRIVE = 0, HFFREQ = 0, $C_{L,eff}$ = 16 pF, Typical ESR and $C_{SHUNT}$, FCNTHF_EN = 0 | 3.0 V | | 4 | ms |
| | $f_{OSC}$ = 4 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 0, $C_{L,eff}$ = 16 pF, Typical ESR and $C_{SHUNT}$, FCNTHF_EN = 0 | | | 1.8 | |
| | $f_{OSC}$ = 8 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 1, $C_{L,eff}$ = 16 pF, Typical ESR and $C_{SHUNT}$, FCNTHF_EN = 0 | | | 0.7 | |
| | $f_{OSC}$ = 16 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 2, $C_{L,eff}$ = 16 pF, Typical ESR and $C_{SHUNT}$, FCNTHF_EN = 0 | | | 0.6 | |
| | $f_{OSC}$ = 24 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 3, $C_{L,eff}$ = 16 pF, Typical ESR and $C_{SHUNT}$, FCNTHF_EN = 0 | | | 450 | µs |
| | $f_{OSC}$ = 32 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 4, $C_{L,eff}$ = 16 pF, Typical ESR and $C_{SHUNT}$, FCNTHF_EN = 0 | | | 300 | |
| | $f_{OSC}$ = 40 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 5, $C_{L,eff}$ = 16 pF, Typical ESR and $C_{SHUNT}$, FCNTHF_EN = 0 | | | 250 | |
| | $f_{OSC}$ = 48 MHz, HFXTBYPASS = 0, HFXTDRIVE = 1, HFFREQ = 6, $C_{L,eff}$ = 16 pF, Typical ESR and $C_{SHUNT}$, FCNTHF_EN = 0 | | | 250 | |
| $C_{HFXIN}$ Integrated load capacitance at HFXIN terminal(5) (6) | | | | 2 | pF |
| $C_{HFXOUT}$ Integrated load capacitance at HFXOUT terminal(5) (6) | | | | 2 | pF |
| $f_{Fault,HFXT}$ Oscillator fault frequency(7) (8) | | | 400 | 700 | kHz |

（4）不包括可编程启动计数器

（5）这代表分别存在于HFXIN和HFXOUT端子的所有寄生电容，包括寄生键和封装电容。有效负载电容CL，eff可以计算为CIN x COUT /（CIN + COUT），其中CIN和COUT分别是HFXIN和HFXOUT端子的总电容。

（6）两个端子都需要外部电容，以满足晶体制造商规定的有效负载电容。支持的推荐有效负载电容值为14 pF，16 pF和18 pF。最大分流电容为7 pF。由于PCB增加了额外的电容，因此还必须考虑整体电容。TI建议验证是否满足所选晶振的推荐有效负载电容。

（7）高于MAX规范的频率不设置故障标志。 MIN和MAX之间的频率可能会设置标志。静态条件或卡在故障条件下将设置标志。

（8）用逻辑电平输入频率测量，但也适用于晶体操作。

表5-11列出了DCO的特性。

**Table 5-11. DCO**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | 参数测试条件VCC，TA | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{RSEL0\_CTR}$ | DCO center frequency accuracy for range 0 with calibrated factory settings | Internal resistor mode, DCORSEL = 0, DCOTUNE = 0 | | 1.443 | 1.5 | 1.557 | MHz |
| | | External resistor mode, DCORSEL = 0, DCOTUNE = 0 | | 1.482 | 1.5 | 1.518 | |
| $f_{RSEL1\_CTR}$ | DCO center frequency accuracy for range 1 with calibrated factory settings | Internal resistor mode, DCORSEL = 1, DCOTUNE = 0 | | 2.885 | 3 | 3.115 | MHz |
| | | External resistor mode, DCORSEL = 1, DCOTUNE = 0 | | 2.964 | 3 | 3.036 | |
| $f_{RSEL2\_CTR}$ | DCO center frequency accuracy for range 2 with calibrated factory settings | Internal resistor mode, DCORSEL = 2, DCOTUNE = 0 | | 5.77 | 6 | 6.23 | MHz |
| | | External resistor mode, DCORSEL = 2, DCOTUNE = 0 | | 5.928 | 6 | 6.072 | |
| $f_{RSEL3\_CTR}$ | DCO center frequency accuracy for range 3 with calibrated factory settings | Internal resistor mode, DCORSEL = 3, DCOTUNE = 0 | | 11.541 | 12 | 12.459 | MHz |
| | | External resistor mode, DCORSEL = 3, DCOTUNE = 0 | | 11.856 | 12 | 12.144 | |
| $f_{RSEL4\_CTR}$ | DCO center frequency accuracy for range 4 with calibrated factory settings | Internal resistor mode, DCORSEL = 4, DCOTUNE = 0 | | 23.082 | 24 | 24.918 | MHz |
| | | External resistor mode, DCORSEL = 4, DCOTUNE = 0 | | 23.712 | 24 | 24.288 | |
| $f_{RSEL5\_CTR}$ | DCO center frequency accuracy for range 5 with calibrated factory settings | Internal resistor mode, DCORSEL = 5, DCOTUNE = 0 | | 46.164 | 48 | 49.836 | MHz |
| | | External resistor mode, DCORSEL = 5, DCOTUNE = 0 | | 47.424 | 48 | 48.576 | |
| $df_{DCO}/dT$ | DCO frequency drift with temperature(1) | Internal resistor mode, At fixed voltage | 1.62 V to 3.7 V | | | 250 | ppm/°C |
| | | External resistor mode(2) At fixed voltage | 1.62 V to 3.7 V | | | 40 | |
| $df_{DCO}/dV_{CC}$ | DCO frequency voltage drift with voltage(3) | At fixed temperature, applicable for both DCO Internal and External resistor modes | –40°C to 85 °C | | | 0.1 | %/V |
| $f_{RSEL0}$ | DCO frequency range 0 | DCORSEL = 0 DCO internal or external resistor mode | 3.0 V，25℃ | 0.98 | 2.26 | MHz | |
| $f_{RSEL1}$ | DCO frequency range 1 | DCORSEL = 1 DCO internal or external resistor mode | 3.0 V，25℃ | 1.96 | 4.51 | MHz | |
| $f_{RSEL2}$ | DCO frequency range 2 | DCORSEL = 2 DCO internal or external resistor mode | 3.0 V，25℃ | 3.92 | 9.02 | MHz | |
| $f_{RSEL3}$ | DCO frequency range 3 | DCORSEL = 3 DCO internal or external resistor mode | 3.0 V，25℃ | 7.84 | 18.04 | MHz | |
| $f_{RSEL4}$ | DCO frequency range 4 | DCORSEL = 4 DCO internal or external resistor mode | 3.0 V，25℃ | 15.68 | 36.07 | MHz | |
| $f_{RSEL5}$ | DCO frequency range 5 | DCORSEL = 5 DCO internal or external resistor mode | 3.0 V，25℃ | 31.36 | 52 | MHz | |
| $f_{DCO\_DC}$ | Duty cycle | | | 47% | 50% | 53% | |

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
（2）不包括外部电阻的温度系数。
DCOR引脚的外部电阻推荐值：91kΩ，0.1%，±25 ppm /℃。
(3) Calculated using the box method: (MAX(1.62 V to 3.7 V) – MIN(1.62 V to 3.7 V)) / MIN(1.62 V to 3.7 V) / (3.7 V – 1.62 V)

**Table 5-11. DCO (continued)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数测试条件VCC，TA | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{DCO\_JITTER}$ | DCO period jitter | DCORSEL = 5, DCOTUNE = 0 | | 50 | 90 | ps |
| | | DCORSEL = 4, DCOTUNE = 0 | | 80 | 120 | |
| | | DCORSEL = 3, DCOTUNE = 0 | | 115 | 170 | |
| | | DCORSEL = 2, DCOTUNE = 0 | | 160 | 240 | |
| | | DCORSEL = 1, DCOTUNE = 0 | | 225 | 340 | |
| | | DCORSEL = 0, DCOTUNE = 0 | | 450 | 550 | |
| TDCO_STEP步长DCO的步长。 0.2% | | | | | | |
| $t_{DCO\_SETTLE\_RANGE}$ | DCO settling from worst case DCORSELn to DCORSELm | DCO settled to within 1.5% of steady state frequency | | | 10 | µs |
| $t_{DCO\_SETTLE\_TUNE}$ | DCO settling worst case DCOTUNEn to DCOTUNEm within any DCORSEL setting | DCO settled to within 1.5% of steady state frequency | | | 10 | µs |
| $t_{START}$ | DCO start-up time(4) | DCO settled to within 0.5% of steady state frequency | | 5 | | µs |

（4）DCO外部电阻引脚（DCOR）的最大寄生电容不应超过5 pF，以确保指定的DCO启动时间。

表5-12列出了DCO的总体容差。

**Table 5-12. DCO Overall Tolerance**

over operating free-air temperature range (unless otherwise noted)

| RESISTOR OPTION | TEMPERATURE CHANGE | TEMPERATURE DRIFT (%) | VOLTAGE CHANGE | VOLTAGE DRIFT (%) | OVERALL DRIFT (%) | OVERALL ACCURACY (%) |
|---|---|---|---|---|---|---|
| Internal resistor | –40°C to 85 °C | ±3.125 | 1.62 V to 3.7 V | ±0.2 | ±3.325 | ±3.825 |
| | 0°C | 0 | 1.62 V to 3.7 V | ±0.2 | ±0.2 | ±0.7 |
| | –40°C to 85 °C | ±3.125 | 0 V | 0 | ±3.125 | ±3.625 |
| External resistor with 25-ppm TCR | –40°C to 85 °C | ±0.5 | 1.62 V to 3.7 V | ±0.2 | ±0.7 | ±1.2 |
| | 0°C | 0 | 1.62 V to 3.7 V | ±0.2 | ±0.2 | ±0.7 |
| | –40°C to 85 °C | ±0.5 | 0 V | 0 | ±0.5 | ±1 |

表5-13列出了内部超低功耗低频振荡器（VLO）的特性。

表5-13。内部超低功耗低频振荡器（VLO）

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数测试条件 | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{VLO}$ | Current consumption(1) | | | 50 | | nA |
| $f_{VLO}$ | VLO frequency | | 6 | 9.4 | 14 | kHz |
| $df_{VLO}/d_T$ | VLO frequency temperature drift(2) | | | 0.1 | | %/°C |
| $df_{VLO}/dV_{CC}$ | VLO frequency supply voltage drift(3) | | | 0.2 | | %/V |
| $DC_{VLO}$ | Duty cycle | | 40% | 50% | 60% | |

(1) Current measured on DVCC supply
(2) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(3) Calculated using the box method: (MAX(1.62 V to 3.7 V) – MIN(1.62 V to 3.7 V)) / MIN(1.62 V to 3.7 V) / (3.7 V – 1.62 V)

表5-14列出了32.768 kHz模式下内部参考低频振荡器（REFO）的特性。

表5-14。 32.768 kHz模式下的内部参考低频振荡器（REFO）（1）

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数测试条件 | | | VCC | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{REFO}$ | REFO current consumption(2) | | | | 0.6 | | µA |
| $f_{REFO}$ | REFO frequency calibrated | | | | 32.768 | | kHz |
| | REFO absolute tolerance calibrated | $T_A$ = –40°C to 85°C | | | | ±3% | |
| | | $T_A$ = 25°C | 3 V | | | ±1.5% | |
| $df_{REFO}/d_T$ | REFO frequency temperature drift(3) | | | | 0.012 | | %/°C |
| $df_{REFO}/dV_{CC}$ | REFO frequency supply voltage drift(4) | | | | 0.2 | | %/V |
| $DC_{REFO}$ | REFO duty cycle | | | 40% | 50% | 60% | |

（1）REFO配置为32.768-kHz模式，REFOFSEL = 0。
（2）AVCC和DVCC电源的总电流测量值。
(3) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(4) Calculated using the box method: (MAX(1.62 V to 3.7 V) – MIN(1.62 V to 3.7 V)) / MIN(1.62 V to 3.7 V) / (3.7 V – 1.62 V)

表5-15列出了128 kHz模式下内部参考低频振荡器（REFO）的特性。

表5-15。 128 kHz模式下的内部参考低频振荡器（REFO）（1）

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数测试条件 | | | VCC | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| REFO | REFO current consumption(2) | | | | 1 | | µA |
| $f_{REFO}$ | REFO frequency calibrated | | | | 128 | | kHz |
| | REFO absolute tolerance calibrated | $T_A$ = –40°C to 85°C | | | | ±6% | |
| | | $T_A$ = 25°C | 3 V | | | ±1.5% | |
| $df_{REFO}/d_T$ | REFO frequency temperature drift(3) | | | | 0.018 | | %/°C |
| $df_{REFO}/dV_{CC}$ | REFO frequency supply voltage drift(4) | | | | 0.4 | | %/V |
| $DC_{REFO}$ | REFO duty cycle | | | 40% | 50% | 60% | |

（1）REFO配置为128-kHz模式，REFOFSEL = 1。
（2）AVCC和DVCC电源的总电流测量值。
(3) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(4) Calculated using the box method: (MAX(1.62 V to 3.7 V) – MIN(1.62 V to 3.7 V)) / MIN(1.62 V to 3.7 V) / (3.7 V – 1.62 V)

表5-16列出了模块振荡器（MODOSC）的特性。

**Table 5-16. Module Oscillator (MODOSC)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | 参数测试条件VCC | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $I_{MODOSC}$ | Current consumption(1) | | | 50 | μA |
| $f_{MODOSC}$ | MODOSC frequency | 23 | 25 | 27 | MHz |
| $df_{MODOSC}/dT$ | MODOSC frequency temperature drift(2) | | 0.02 | | %/℃ |
| $df_{MODOSC}/dVCC$ | MODOSC frequency supply voltage drift(3) | | 0.3 | | %/V |
| $DC_{MODOSC}$ | Duty cycle | 40% | 50% | 60% | |

（1）AVCC和DVCC电源的总电流测量值。
(2) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(3) Calculated using the box method: (MAX(1.62 V to 3.7 V) – MIN(1.62 V to 3.7 V)) / MIN(1.62 V to 3.7 V) / (3.7 V – 1.62 V)

表5-17列出了系统振荡器（SYSOSC）的特性。

**Table 5-17. System Oscillator (SYSOSC)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | 参数测试条件VCC | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $I_{SYSOSC}$ | Current consumption(1) | | 30 | | μA |
| $f_{SYSOSC}$ | SYSOSC frequency | 4.25 | 5.0 | 5.75 | MHz |
| $df_{SYSOSC}/dT$ | SYSOSC frequency temperature drift(2) | | 0.03 | | %/℃ |
| $df_{SYSOSC}/dVCC$ | SYSOSC frequency supply voltage drift(3) | | 0.5 | | %/V |
| $DC_{SYSOSC}$ | Duty cycle | 40% | 50% | 60% | |

（1）AVCC电源测量的电流。
(2) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(3) Calculated using the box method: (MAX(1.62 V to 3.7 V) – MIN(1.62 V to 3.7 V)) / MIN(1.62 V to 3.7 V) / (3.7 V – 1.62 V)

## 5.25.4供电系统

表5-18列出了LDO VCORE稳压器的特性。

表5-18。 VCORE稳压器（LDO）特性

| | 参数测试条件MIN TYP MAX UNIT | | | | | |
|---|---|---|---|---|---|---|
| $V_{CORE0-HP}$ | Static VCORE voltage Level 0 in active and LPM0 modes | Device power modes AM_LDO_VCORE0, LPM0_LDO_VCORE0 | 1.12 | 1.2 | 1.28 | V |
| $V_{CORE1-HP}$ | Static VCORE voltage Level 1 in active and LPM0 modes | Device power modes AM_LDO_VCORE1, LPM0_LDO_VCORE1 | 1.31 | 1.4 | 1.49 | V |
| $V_{CORE0-LF}$ | Static VCORE voltage Level 0 in low-frequency active and low frequency LPM0 modes | 器件功耗模式AM_LF_VCORE0 1.12 1.2 1.28 V. | | | | |
| $V_{CORE1-LF}$ | Static VCORE voltage Level 1 in low-frequency active and low frequency LPM0 modes | 器件功耗模式AM_LF_VCORE1 1.31 1.4 1.49 V. | | | | |
| $V_{CORE0-LPM34}$ | Static VCORE voltage Level 0 in LPM3 and LPM4 modes | Device power modes LPM3, LPM4 | 1.08 | 1.2 | 1.32 | V |
| $V_{CORE1-LPM34}$ | Static VCORE voltage Level 1 in LPM3 and LPM4 modes | Device power modes LPM3, LPM4 | 1.27 | 1.4 | 1.53 | V |
| $V_{CORE0-LPM35}$ | Static VCORE voltage Level 0 in LPM3.5 mode | Device power mode LPM3.5 | 1.08 | 1.2 | 1.32 | V |
| IINRUSH-ST启动时的浪涌电流设备上电200 mA | | | | | | |
| $I_{PEAK-LDO}$ | Peak current drawn by LDO from $DV_{CC}$ | | | | 350 | mA |
| $I_{SC-coreLDO}$ | Short circuit current limit for core LDO | Measured when output is shorted to ground | | | 300 | mA |

表5-19列出了DC-DC VCORE稳压器的特性。

表5-19。 VCORE稳压器（DC-DC）特性

| | 参数测试条件MIN TYP MAX UNIT | | | | | |
|---|---|---|---|---|---|---|
| $DV_{CC-DCDC}$ | Allowed $DV_{CC}$ range for DC-DC operation | DCDC_FORCE = 1 | 1.8 | | 3.7 | V |
| $V_{DCDC\_SO}$ (1) | DC-DC to LDO switch over voltage | $dDV_{CC}/dt$ = 1 V/ms, DCDC_FORCE = 0 | 1.8 | | 2.0 | V |
| $V_{CORE0-DCDC}$ | Static VCORE voltage Level 0 in DC-DC high-performance modes | Device power modes AM_DCDC_VCORE0, LPM0_DCDC_VCORE0 | 1.12 | 1.2 | 1.28 | V |
| $V_{CORE1-DCDC}$ | Static VCORE voltage Level 1 in DC-DC high-performance modes | Device power modes AM_DCDC_VCORE1, LPM0_DCDC_VCORE1 | 1.31 | 1.4 | 1.49 | V |
| $I_{PEAK-DCDC}$ | Peak current drawn by DC-DC from DVCC | | | | 300 | mA |
| $I_{SC-DCDC}$ | Short circuit current limit for DC-DC | Measured when output is shorted to ground | | | 500 | mA |

（1）当DVCC低于此电压时，稳压器内部从DC-DC切换到LDO。

表5-20列出了VCCDET特性。

**Table 5-20. PSS, VCCDET**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | 参数测试条件MIN TYP MAX UNIT | | | | | |
|---|---|---|---|---|---|---|
| $V_{VCC\_VCCDET-}$ | VCCDET power-down level - trip point with falling $V_{CC}$ | $dDV_{CC}/d_t$ < 3 V/s (1) | 0.64 | 1.12 | 1.55 | V |
| $V_{VCC\_VCCDET+}$ | VCCDET power-up level - trip point with rising $V_{CC}$ | $dDV_{CC}/d_t$ < 3 V/s (1) | 0.70 | 1.18 | 1.59 | V |
| VVCC_VCC_hys VCCDET迟滞30 65 100 mV | | | | | | |

（1）用缓慢变化的电源测量VCCDET电平。更快的斜坡可能导致不同的水平。

表5-21列出了SVSMH特性。

**Table 5-21. PSS, SVSMH**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | 参数测试条件MIN TYP MAX UNIT | | | | | |
|---|---|---|---|---|---|---|
| $I_{SVSMH}$ | $SVSM_H$ current consumption, low-power mode | SVSMHOFF = 0, SVSMHLP = 1 | | 200 | 400 | nA |
| | $SVSM_H$ current consumption, high-performance mode | SVSMHOFF = 0, SVSMHLP = 0 | | 7 | 10 | µA |
| $V_{SVSMH-,HP}$ | $SVSM_H$ threshold level during high-performance mode (falling $DV_{CC}$) | SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 0, DC ($dDV_{CC}/dt$ < 1V/s) | 1.59 | 1.64 | 1.71 | V |
| | | SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 1, DC ($dDV_{CC}/dt$ < 1V/s) | 1.59 | 1.64 | 1.71 | |
| | | SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 2, DC ($dDV_{CC}/dt$ < 1V/s) | 1.59 | 1.64 | 1.71 | |
| | | SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 3, DC ($dDV_{CC}/dt$ < 1V/s) | 2.0 | 2.06 | 2.12 | |
| | | SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 4, DC ($dDV_{CC}/dt$ < 1V/s) | 2.2 | 2.26 | 2.32 | |
| | | SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 5, DC ($dDV_{CC}/dt$ < 1V/s) | 2.4 | 2.47 | 2.54 | |
| | | SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 6, DC ($dDV_{CC}/dt$ < 1V/s) | 2.7 | 2.79 | 2.88 | |
| | | SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 7, DC ($dDV_{CC}/dt$ < 1V/s) | 2.9 | 3.0 | 3.1 | |
| $V_{SVSMH+,HP}$ | $SVSM_H$ threshold level; High Performance Mode [rising $DV_{CC}$] | SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 0, DC ($dDV_{CC}/dt$ < 1V/s) | 1.6 | 1.66 | 1.71 | V |
| | | SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 1, DC ($dDV_{CC}/dt$ < 1V/s) | 1.6 | 1.66 | 1.71 | |
| | | SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 2, DC ($dDV_{CC}/dt$ < 1V/s) | 1.6 | 1.66 | 1.71 | |
| | | SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 3, DC ($dDV_{CC}/dt$ < 1V/s) | 2.02 | 2.07 | 2.14 | |
| | | SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 4, DC ($dDV_{CC}/dt$ < 1V/s) | 2.22 | 2.27 | 2.34 | |
| | | SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 5, DC ($dDV_{CC}/dt$ < 1V/s) | 2.42 | 2.48 | 2.56 | |
| | | SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 6, DC ($dDV_{CC}/dt$ < 1V/s) | 2.72 | 2.8 | 2.9 | |
| | | SVSMHOFF = 0, SVSMHLP = 0, SVSMHTH = 7, DC ($dDV_{CC}/dt$ < 1V/s) | 2.92 | 3.01 | 3.12 | |

**Table 5-21. PSS, SVSMH (continued)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数测试条件MIN TYP MAX UNIT | | | | | | |
|---|---|---|---|---|---|---|
| $V_{SVSMH-,LP}$ | $SVSM_H$ threshold level; Low Power Mode [falling $DV_{CC}$] | SVSMHOFF = 0, SVSMHLP = 1, SVSMHTH = 0, DC ($dDV_{CC}/dt$ < 1V/s) | 1.55 | 1.62 | 1.71 | V |
| | | SVSMHOFF = 0, SVSMHLP = 1, SVSMHTH = 1, DC ($dDV_{CC}/dt$ < 1V/s) | 1.55 | 1.62 | 1.71 | |
| | | SVSMHOFF = 0, SVSMHLP = 1, SVSMHTH = 2, DC ($dDV_{CC}/dt$ < 1V/s) | 1.55 | 1.62 | 1.71 | |
| | | SVSMHOFF = 0, SVSMHLP = 1, SVSMHTH = 3, DC ($dDV_{CC}/dt$ < 1V/s) | 2.0 | 2.09 | 2.18 | |
| | | SVSMHOFF = 0, SVSMHLP = 1, SVSMHTH = 4, DC ($dDV_{CC}/dt$ < 1V/s) | 2.2 | 2.3 | 2.4 | |
| | | SVSMHOFF = 0, SVSMHLP = 1, SVSMHTH = 5, DC ($dDV_{CC}/dt$ < 1V/s) | 2.4 | 2.51 | 2.62 | |
| | | SVSMHOFF = 0, SVSMHLP = 1, SVSMHTH = 6, DC ($dDV_{CC}/dt$ < 1V/s) | 2.7 | 2.83 | 2.94 | |
| | | SVSMHOFF = 0, SVSMHLP = 1, SVSMHTH = 7, DC ($dDV_{CC}/dt$ < 1V/s) | 2.87 | 3.0 | 3.13 | |
| $V_{SVSMH\_hys}$ | $SVSM_H$ hysteresis | | | 15 | 30 | mV |
| $t_{PD,SVSMH}$ | $SVS_H$ propagation delay, high-performance mode | SVSMHOFF = 0, SVSMHLP = 0, very fast $dV_{DVCC}/dt$ | | 3 | 10 | µs |
| | $SVS_H$ propagation delay, low-power mode | SVSMHOFF = 0, SVSMHLP = 1, very fast $dV_{DVCC}/dt$ | | 25 | 100 | |
| $t_{(SVSMH)}$ | $SVSM_H$ on or off delay time | SVSMHOFF = 1 → 0, SVSMHLP = 0 (1) | | 17 | 40 | µs |

（1）如果SVSMH在激活模式下保持禁用并在进入设备的低功耗模式（LPM3，LPM4，LPM3.5或LPM4.5）之前启用，则应注意自启用后已经过了足够的时间在进入器件低功耗模式之前模块的功能，以允许按SVSMH开启或关闭延迟时间规范成功唤醒SVSMH模块。否则，SVSMH可能会跳闸，导致器件复位并从低功耗模式唤醒。

5.25.5数字I / O.

表5-22列出了数字输入的特性。

表5-22。数字输入（适用于普通和高驱动I / O）

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数测试条件VCC | | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| VIT +正向输入阈值电压 | | | 2.2 V | 0.99 | 1.65 | | V |
| | | | 3 V | 1,35 | 2.25 | | |
| VIT-负输入阈值电压 | | | 2.2 V | 0.55 | 1.21 | | V |
| | | | 3 V | 0,75 | 1.65 | | |
| Vhys输入电压滞后（VIT + – VIT-） | | | 2.2 V | 0.32 | 0.84 | | V |
| | | | 3 V | 0,4 | 1.0 | | |
| $R_{Pull}$ | Pullup or pulldown resistor | For pullup: $V_{IN} = V_{SS}$, For pulldown: $V_{IN} = V_{CC}$ | | 20 | 30 | 40 | kΩ |
| CI，dig输入电容，仅数字端口引脚VIN = VSS或VCC | | | | | 3 | | pF |
| $C_{I,ana}$ | Input capacitance, port pins shared with analog functions | $V_{IN} = V_{SS}$ or $V_{CC}$ | | | 5 | | pF |
| $I_{lkg,ndio}$ | Normal I/O high-impedance input leakage current | See (1)(2) | 2.2 V, 3 V | | | ±20 | nA |
| $I_{lkg,hdio}$ | High-drive I/O high-impedance input leakage current | See (1)(2) | 2.2 V, 3 V | | | ±20 | nA |
| $t_{int}$ | External interrupt timing (external trigger pulse duration to set interrupt flag) | Ports with interrupt capability and without glitch filter (3) | 2.2 V, 3 V | 20 | | | ns |
| | | Ports with interrupt capability and with glitch filter but glitch filter disabled (GLTFLT_EN = 0) (3) | 2.2 V, 3 V | 20 | | | ns |
| | | Ports with interrupt capability and with glitch filter, glitch filter enabled (GLTFTL_EN = 1) (4) | 2.2 V, 3 V | 0.25 | | 1 | µs |
| $t_{RST}$ | External reset pulse duration on RSTn pin(5) | | 2.2 V, 3 V | 1 | | | µs |

（1）除非另有说明，否则输入漏电流是在VSS或VCC施加到相应引脚的情况下测量的

（2）数字端口引脚的输入泄漏是单独测量的。选择端口引脚用于输入，并禁用上拉/下拉电阻。

（3）每次满足最小中断脉冲持续时间色调时，外部信号设置中断标志。它可以由短于色调的触发信号设置。

（4）总是过滤小于MIN值的触发脉冲持续时间，并且总是通过大于MAX值的触发脉冲持续时间。如果持续时间在MIN和MAX值之间，则可以过滤或不过滤触发脉冲。

（5）如果RSTn / NMI引脚配置为NMI，则不适用。

表5-23列出了正常驱动数字输出的特性。典型特征图见图5-19至图5-22。

**Table 5-23. Digital Outputs, Normal I/Os**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数 | 测试条件 | VCC | MIN | MAX | 单元 |
|---|---|---|---|---|---|
| $V_{OH}$ High-level output voltage | $I_{(OHmax)}$ = –1 mA(1) | 2.2 V | $V_{CC}$ – 0.25 | $V_{CC}$ | V |
| | $I_{(OHmax)}$ = –3 mA(2) | | $V_{CC}$ – 0.60 | $V_{CC}$ | |
| | $I_{(OHmax)}$ = –2 mA(1) | 3.0 V | $V_{CC}$ – 0.25 | $V_{CC}$ | |
| | $I_{(OHmax)}$ = –6 mA(2) | | $V_{CC}$ – 0.60 | $V_{CC}$ | |
| $V_{OL}$ Low-level output voltage | $I_{(OLmax)}$ = 1 mA(1) | 2.2 V | $V_{SS}$ | $V_{SS}$ + 0.25 | V |
| | $I_{(OLmax)}$ = 3 mA(2) | | $V_{SS}$ | $V_{SS}$ + 0.60 | |
| | $I_{(OLmax)}$ = 2 mA(1) | 3.0 V | $V_{SS}$ | $V_{SS}$ + 0.25 | |
| | $I_{(OLmax)}$ = 6 mA(2) | | $V_{SS}$ | $V_{SS}$ + 0.60 | |
| $f_{Px.y}$ Port output frequency (with RC load)(3) | VCORE = 1.4 V, $C_L$ = 20 pF, $R_L$ (4) (5) | 1.62 V | | 24 | MHz |
| | | 2.2 V | | 24 | |
| | | 3.0 V | | 24 | |
| $d_{Px.y}$ Port output duty cycle (with RC Load) | VCORE = 1.4 V, $C_L$ = 20 pF, $R_L$ (4) (5) | 1.62 V | 40% | 60% | |
| | | 2.2 V | 40% | 60% | |
| | | 3.0 V | 45% | 55% | |
| $f_{Port\_CLK}$ Clock output frequency(3) | VCORE = 1.4 V, $C_L$ = 20 pF(5) | 1.62 V | | 24 | MHz |
| | | 2.2 V | | 24 | |
| | | 3.0 V | | 24 | |
| $d_{Port\_CLK}$ Clock output duty cycle | VCORE = 1.4 V, $C_L$ = 20 pF(5) | 1.62 V | 40% | 60% | |
| | | 2.2 V | 40% | 60% | |
| | | 3.0 V | 45% | 55% | |
| $t_{rise,dig}$ Port output rise time, digital only port pins | $C_L$ = 20 pF (6) | 1.62 V | | 8 | ns |
| | | 2.2 V | | 5 | |
| | | 3.0 V | | 3 | |
| $t_{fall,dig}$ Port output fall time, digital only port pins | $C_L$ = 20 pF (7) | 1.62 V | | 8 | ns |
| | | 2.2 V | | 5 | |
| | | 3.0 V | | 3 | |
| $t_{rise,ana}$ Port output rise time, port pins with shared analog functions | $C_L$ = 20 pF (6) | 1.62 V | | 8 | ns |
| | | 2.2 V | | 5 | |
| | | 3.0 V | | 3 | |
| $t_{fall,ana}$ Port output fall time, port pins with shared analog functions | $C_L$ = 20 pF (7) | 1.62 V | | 8 | ns |
| | | 2.2 V | | 5 | |
| | | 3.0 V | | 3 | |

（1）所有输出组合的最大总电流I（OHmax）和I（OLmax）不应超过±48 mA，以保持规定的最大电压降。

（2）所有输出组合的最大总电流I（OHmax）和I（OLmax）不应超过±100 mA，以保持规定的最大电压降。

（3）端口可以输出至少达到规定限值的频率 – 它可能支持更高的频率。

（4）在VCC和VSS之间使用2×R1和R1 =3.2kΩ的电阻分压器作为负载。输出连接到分频器的中心抽头。 CL = 20 pF连接到VSS的输出。

（5）输出电压在指定的切换频率下达到至少20%和80%VCC。

（6）在VCC的20%至VCC的80%之间测量。

（7）在VCC的80%至VCC的20%之间测量。

表5-24列出了高驱动数字输出的特性。典型特征图见图5-23至图5-26。

表5-24。数字输出，高驱动I / O.

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数 | 测试条件 | VCC | MIN | MAX | 单元 |
|---|---|---|---|---|---|
| $V_{OH}$ High-level output voltage | $I_{(OHmax)}$ = –5 mA(1) | 2.2 V | $V_{CC}$ – 0.25 | $V_{CC}$ | V |
| | $I_{(OHmax)}$ = –15 mA(2) | | $V_{CC}$ – 0.60 | $V_{CC}$ | |
| | $I_{(OHmax)}$ = –10 mA(1) | 3.0 V | $V_{CC}$ – 0.25 | $V_{CC}$ | |
| | $I_{(OHmax)}$ = –20 mA(2) | | $V_{CC}$ – 0.50 | $V_{CC}$ | |
| $V_{OL}$ Low-level output voltage | $I_{(OLmax)}$ = 5 mA(1) | 2.2 V | $V_{SS}$ | $V_{SS}$ + 0.25 | V |
| | $I_{(OLmax)}$ = 15 mA(2) | | $V_{SS}$ | $V_{SS}$ + 0.60 | |
| | $I_{(OLmax)}$ = 10 mA(1) | 3.0 V | $V_{SS}$ | $V_{SS}$ + 0.25 | |
| | $I_{(OLmax)}$ = 20 mA(2) | | $V_{SS}$ | $V_{SS}$ + 0.50 | |
| $f_{Px.y}$ Port output frequency (with RC load)(3) | VCORE = 1.4 V, $C_L$ = 80 pF, $R_L$ (4) (5) | 1.62 V | 24 | | MHz |
| | | 2.2 V | 24 | | |
| | | 3.0 V | 24 | | |
| $d_{Px.y}$ Port output duty cycle (with RC Load) | VCORE = 1.4 V, $C_L$ = 80 pF, $R_L$ (4) (5) | 1.62 V | 45% | 55% | |
| | | 2.2 V | 45% | 55% | |
| | | 3.0 V | 45% | 55% | |
| $f_{Port\_CLK}$ Clock output frequency(3) | VCORE = 1.4 V, $C_L$ = 80 pF(5) | 1.62 V | 24 | | MHz |
| | | 2.2 V | 24 | | |
| | | 3.0 V | 24 | | |
| $d_{Port\_CLK}$ Clock output duty cycle | VCORE = 1.4 V, $C_L$ = 80 pF(5) | 1.62 V | 45% | 55% | |
| | | 2.2 V | 45% | 55% | |
| | | 3.0 V | 45% | 55% | |
| $t_{rise}$ Port output rise time | $C_L$ = 80 pF (6) | 1.62 V | 8 | | ns |
| | | 2.2 V | | 5 | |
| | | 3.0 V | 3 | | |
| $t_{fall}$ Port output fall time | $C_L$ = 80 pF (7) | 1.62 V | 8 | | ns |
| | | 2.2 V | | 5 | |
| | | 3.0 V | 3 | | |

（1）所有输出组合的最大总电流I（OHmax）和I（OLmax）不应超过±48 mA，以保持规定的最大电压降。

（2）所有输出组合的最大总电流I（OHmax）和I（OLmax）不应超过±100 mA，以保持规定的最大电压降。

（3）端口可以输出至少达到规定限值的频率，并且可能支持更高的频率。

（4）在VCC和VSS之间使用2×R1和R1 =3.2kΩ的电阻分压器作为负载。输出连接到分频器的中心抽头。 CL = 80 pF连接到VSS的输出。

（5）输出电压在指定的切换频率下达到至少20%和80%VCC。

（6）在VCC的20%至VCC的80%之间测量。

（7）在VCC的80%至VCC的20%之间测量。

表5-25列出了引脚振荡器端口的频率。典型特征图见图5-27和图5-28。

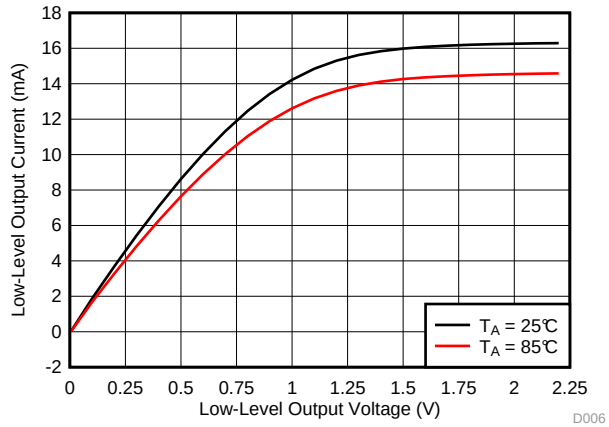
表5-25。引脚振荡器频率，端口Px

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数 | 测试条件 | VCC | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $fo_{Px.y}$ Pin-oscillator frequency | Px.y, $C_L$ = 10 pF(1) | 3.0 V | | | 1900 | kHz |
| | Px.y, $C_L$ = 20 pF(1) | 3.0 V | | | 1150 | kHz |

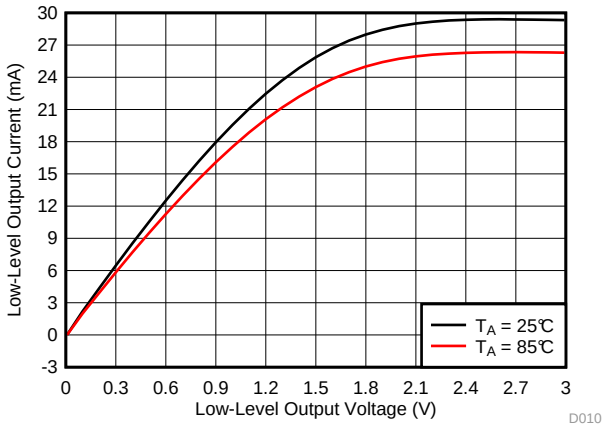
（1）CL是从输出端连接到VSS的外部负载电容，包括所有寄生效应，如PCB走线。

## 5.25.5.1典型特性，正常驱动I / O输出，3.0 V和2.2 V



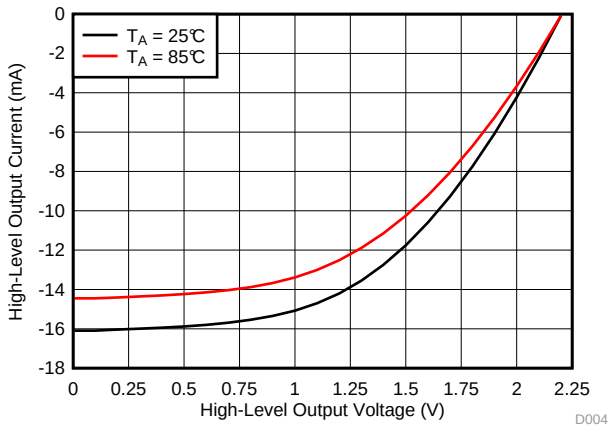

$V_{CC}$ = 2.2 V P7.0

**Figure 5-19. Low-Level Output Voltage vs Low-Level Output Current**



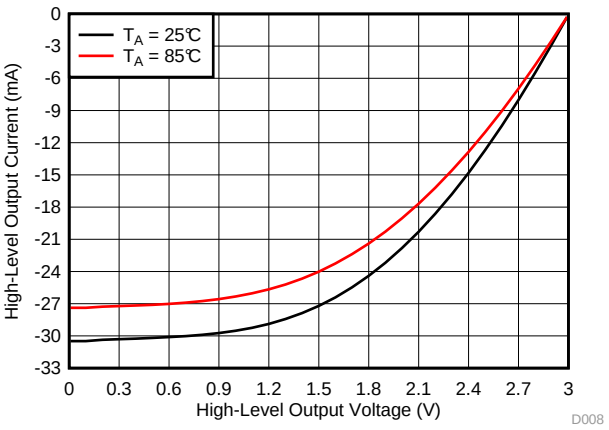

$V_{CC}$ = 3.0 V P7.0

**Figure 5-20. Low-Level Output Voltage vs Low-Level Output Current**




$V_{CC}$ = 2.2 V P7.0

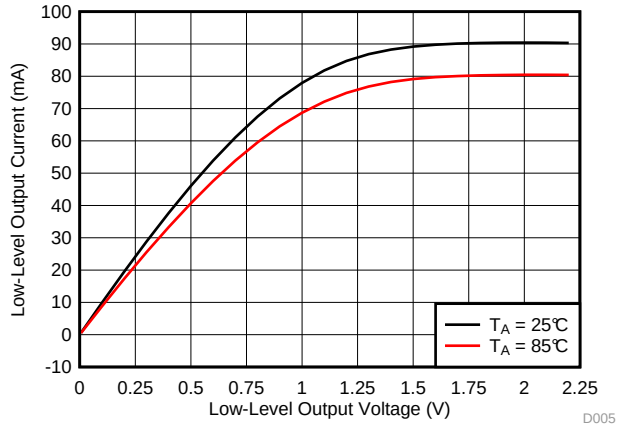
图5-21。高电平输出电压vs.
**High-Level Output Current**




$V_{CC}$ = 3.0 V P7.0

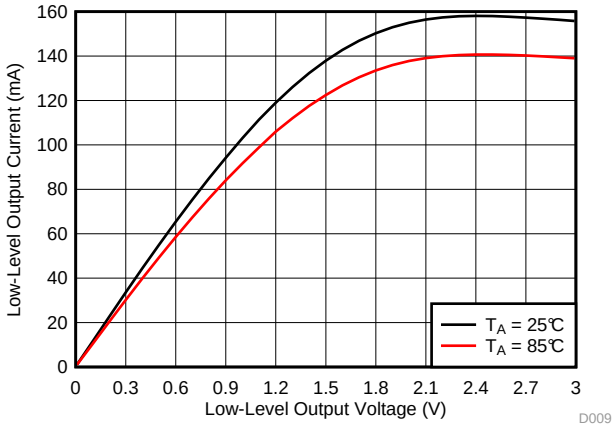
图5-22。高电平输出电压vs.
**High-Level Output Current**

## 5.25.5.2典型特性，3.0 V和2.2 V的高驱动I / O输出



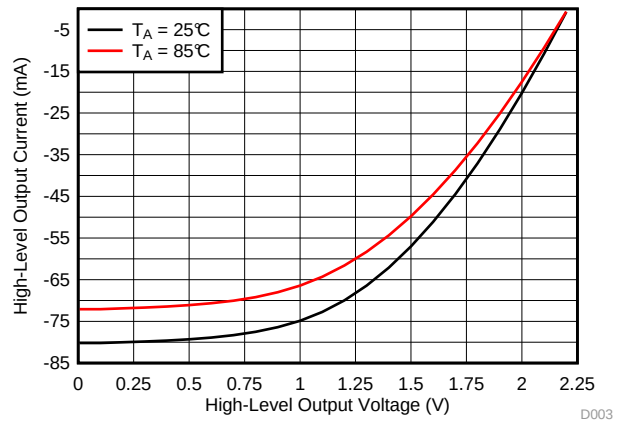

$V_{CC}$ = 2.2 V P2.1

**Figure 5-23. Low-Level Output Voltage vs Low-Level Output Current**



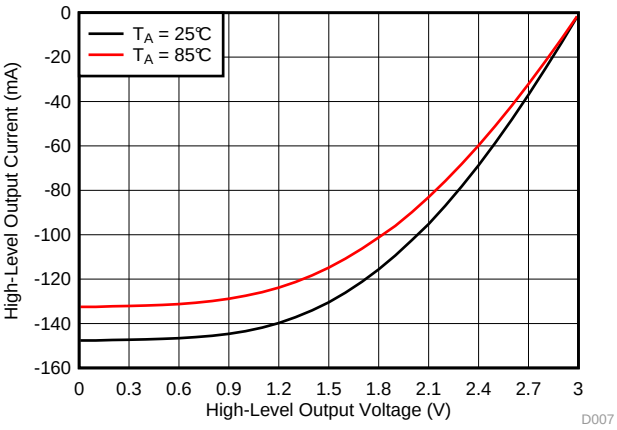

$V_{CC}$ = 3.0 V P2.1

**Figure 5-24. Low-Level Output Voltage vs Low-Level Output Current**




$V_{CC}$ = 2.2 V P2.1

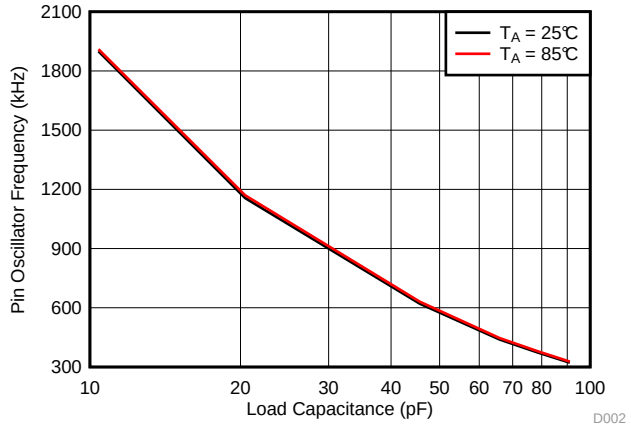
图5-25。高电平输出电压vs.
High-Level Output Current




$V_{CC}$ = 3.0 V P2.1

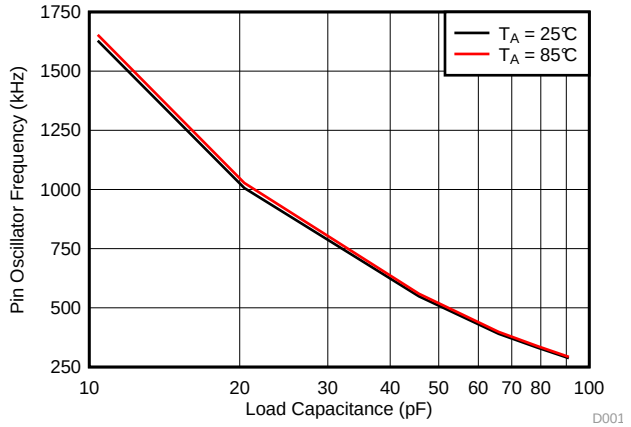
图5-26。高电平输出电压vs.
High-Level Output Current

## 5.25.5.3典型特性，引脚振荡器频率




One output active at a time $V_{CC}$ = 3.0 V

图5-27。负载电容与引脚振荡器频率




One output active at a time $V_{CC}$ = 2.2 V

图5-28。负载电容与引脚振荡器频率

### 5.25.6 14-Bit ADC

表5-26列出了ADC的电源和输入范围条件。

表5-26。 14位ADC，电源和输入范围条件

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | 参数测试条件VCC | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $AV_{CC}$ | Analog supply voltage | AVCC and DVCC are connected together, AVSS and DVSS are connected together, V(AVSS) = V(DVSS) = 0 V, ADC14PWRMD = 2 | | 1.62 | 3.7 | V |
| $AV_{CC}$ | Analog supply voltage | AVCC and DVCC are connected together, AVSS and DVSS are connected together, V(AVSS) = V(DVSS) = 0 V, ADC14PWRMD = 0 | | 1.8 | 3.7 | V |
| V(Ax) | Analog input voltage range(1) | All ADC analog input pins Ax | | 0 | AVCC | V |
| VCM输入共模范围所有ADC模拟输入引脚Ax（ADC14DIF = 1）0 | | | | | VREF | V |
| $I_{(ADC14)}$ single-ended mode | Operating supply current into AVCC and DVCC terminals(2) | $f_{ADC14CLK}$ = 25 MHz, 1 Msps (ADC14PWRMD = 0), ADC14ON = 1, ADC14DIF = 0, ADC14VRSEL = 0xE, REFON = 0, ADC14SHT0x = 0x0, ADC14SHT1x = 0x0 | 3.0 V | 490 | 640 | µA |
| | | | 2.2 V | 450 | 580 | |
| | | $f_{ADC14CLK}$ = 5 MHz, 200 ksps (ADC14PWRMD = 2), ADC14ON = 1, ADC14DIF = 0, ADC14VRSEL = 0xE, REFON = 0, ADC14SHT0x = 0x0, ADC14SHT1x = 0x0 | 3.0 V | 215 | 270 | |
| | | | 2.2 V | 210 | 260 | |
| $I_{(ADC14)}$ differential mode | Operating supply current into AVCC and DVCC terminals(2) | $f_{ADC14CLK}$ = 25 MHz, 1 Msps (ADC14PWRMD = 0), ADC14ON = 1, ADC14DIF = 1, ADC14VRSEL = 0xE, REFON = 0, ADC14SHT0x = 0x0, ADC14SHT1x = 0x0 | 3.0 V | 690 | 875 | µA |
| | | | 2.2 V | 620 | 785 | |
| | | $f_{ADC14CLK}$ = 5 MHz, 200 ksps (ADC14PWRMD = 2), ADC14ON = 1, ADC14DIF = 1, ADC14VRSEL = 0xE, REFON = 0, ADC14SHT0x = 0x0, ADC14SHT1x = 0x0 | 3.0 V | 275 | 335 | |
| | | | 2.2 V | 260 | 320 | |
| $C_I$ | Input capacitance into a single terminal(3) | | | 12 | 15 | pF |
| RI输入MUX导通电阻0V≤V（Ax）≤AVCC | | | 1.8 V至 3.7 V | 0.135 | 1 | kΩ |
| | | | 1.62 V至 <1.8 V | 0.15 | 1.5 | |

（1）模拟输入电压范围必须在所选参考电压范围VR+至VR–内，才能获得有效的转换结果。
（2）内部参考电源电流不包含在电流消耗参数I（ADC14）中。
（3）仅表示ADC开关电容。有关内部寄生引脚电容，请参阅数字输入电气规范。

表5-27列出了ADC的时序参数。

表5-27。 14位ADC，时序参数

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数 | 测试条件 | VCC | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{ADC14CLK}$ ADC clock frequency(1) | ADC14PWRMD = 0 | 1.8 V to 3.7 V | 0.128 | | 25 | MHz |
| | ADC14PWRMD = 2 | 1.62 V至3.7 V | 0.128 | | 5.75 | |
| $N_{CONVERT}$ Clock cycles for conversion | ADC14RES = 11 | | | | 16 | cycles |
| | ADC14RES = 10 | | | | 14 | |
| | ADC14RES = 01 | | | | 11 | |
| | ADC14RES = 00 | | | | 9 | |
| $t_{ADC14ON}$ Turnon settling time of ADC | See (2) | | | | 1.5 | µs |
| $t_{Sample}$ Sampling time(3) (4) | $R_S$ = 200 Ω, $C_{pext}$ = 10 pF, $R_I$ = 1 kΩ, $C_I$ = 15 pF, $C_{pint}$ = 5 pF | | 0.215 | | | µs |

（1）MODOSC可用于1 Msps、SYSOSC可用于ADC的200 ksps采样率操作。
（2）条件是在tADC14ON小于±1 LSB之后转换中的错误开始。参考和输入信号已经确定。
（3）采样时间应至少为4×（1 / fADC14CLK）。
（4）tsample≥（n + 1）×ln（2）×[（RS + RI）×CI + RS×（Cpext + Cpint）]，其中n = ADC分辨率= 14，RS =外部源电阻，Cpext =外部寄生电容。

表5-28列出了ADC的线性度参数。

表5-28。 14位ADC，线性度参数（1）（2）

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数 | 测试条件 | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Resolution | | | 14 | | bits |
| EI积分线性误差（INL） | ±2.3 LSB | | | | |
| $E_D$ Differential linearity error (DNL) | | –0.99 | | 1 | LSB |
| $E_O$ Offset error | ADC14VRSEL = 0xE, 0xF | | ±0.2 | ±1 | mV |
| | ADC14VRSEL = 0x1 | | ±1.2 | ±2 | |
| $E_G$ Gain error | ADC14VRSEL = 0xE | | ±2 | ±4 | LSB |
| | ADC14VRSEL = 0xF | | ±20 | ±60 | |
| | ADC14VRSEL = 0x1 | | ±50 | ±180 | |
| $E_T$ Total unadjusted error | ADC14VRSEL = 0xE | | ±4 | ±15 | LSB |
| | ADC14VRSEL = 0xF | | ±22 | ±62 | |
| | ADC14VRSEL = 0x1 | | ±55 | ±185 | |

（1）为满足规定的精度，必须使用1.45 V的最小参考电压。低至1.2 V的参考电压可用于1 Msps采样率，同时降低精度要求。
（2）对于ADC14VRSEL = 0xE，应将VeREF-引脚连接到板载地。

表5-29列出了ADC的动态参数。

表5-29。 14位ADC，动态参数（1）

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | 参数测试条件MIN TYP MAX UNIT | | | | | |
|---|---|---|---|---|---|---|
| SINAD(2) | Signal-to-noise and distortion | 1 Msps, ADC14DIF = 0, ADC14VRSEL = 0xE, 2.5-V reference, 20-kHz input sine, LDO based operation | 71 | 73 | | dB |
| | | 1 Msps, ADC14DIF = 0, ADC14VRSEL = 0xE, 2.5-V reference, 20-kHz input sine, DC-DC based operation | 62 | 70 | | |
| | | 1 Msps, ADC14DIF = 1, ADC14VRSEL = 0xE, 2.5-V reference, 20-kHz input sine | 79 | 81 | | |
| ENOB(2) | Effective number of bits | 1 Msps, ADC14DIF = 0, ADC14VRSEL = 0xE, 2.5-V reference, 20-kHz input sine, LDO based operation | 11.5 | 11.8 | | bit |
| | | 1 Msps, ADC14DIF = 0, ADC14VRSEL = 0xE, 2.5-V reference, 20-kHz input sine, DC-DC based operation | 10 | 11.3 | | |
| | | 1 Msps, ADC14DIF = 1, ADC14VRSEL = 0xE, 2.5-V reference, 20-kHz input sine | 12.8 | 13.2 | | |
| CMRR_DC | Common-mode rejection ratio, DC | 共模输入信号在DC时为0至VREF pp，ADC14DIF = 1 70 85 dB | | | | |
| CMRR_AC | Common-mode rejection ratio, AC | 共模输入信号= 0至VREF pp，1 MHz，ADC14DIF = 1 55 65 dB | | | | |
| PSRR_DC | Power supply rejection ratio, DC | $AV_{CC}$ = $AV_{CC\ (min)}$ to $AV_{CC(max)}$, ADC14DIF = 0, ADC14VRSEL = 0xE | | 1 | 2.5 | mV/V |
| | | $AV_{CC}$ = $AV_{CC\ (min)}$ to $AV_{CC(max)}$, ADC14DIF = 1, ADC14VRSEL = 0xE | | 50 | 150 | µV/V |
| PSRR_AC | Power supply rejection ratio, AC | $dAV_{CC}$ = 0.1 V at 1 kHz, ADC14DIF = 0, ADC14VRSEL = 0xE | | 1 | | mV/V |
| | | $dAV_{CC}$ = 0.1 V at 1 kHz, ADC14DIF = 1, ADC14VRSEL = 0xE | | 50 | | µV/V |

（1）对于ADC14VRSEL = 0xE，应将VeREF-引脚连接到板载地。
（2）来自HFXT振荡器的ADC时钟。

表5-30列出了温度传感器和内置V1 / 2的特性。

表5-30。 14位ADC，温度传感器和内置V1 / 2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数 | 测试条件 | VCC | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{SENSOR}$ | See (1) (2) | ADC14ON = 1, ADC14TCMAP = 1, $T_A$ = 0°C | | 685 | | mV |
| $TC_{SENSOR}$ | See (2) | ADC14ON = 1, ADC14TCMAP = 1 | | 1.9 | | mV/°C |
| $t_{SENSOR}$ (sample) | Sample time required if ADCTCMAP = 1 and channel (MAX – 1) is selected(3) | ADC14ON = 1, ADC14TCMAP = 1, Error of conversion result ≤ 1 LSB | | 5 | | µs |
| $V_{1/2}$ | AVCC voltage divider for ADC14BATMAP = 1 on MAX input channel | ADC14ON = 1, ADC14BATMAP = 1 | | 48% | 50% 52% | |
| $t_{V\ 1/2}$ (sample) | Sample time required if ADC14BATMAP = 1 and channel MAX is selected(4) | ADC14ON = 1, ADC14BMAP = 1 | | 1 | | µs |

（1）温度传感器偏移可高达±35° C。 TI建议采用单点校准，以最大限度地减少内置温度传感器的失调误差。

（2）对于每个可用的参考电压电平，TLV结构包含30° C±3° C和85° C±3° C的校准值。传感器电压可以计算为VSENSE = TCSENSOR×（温度，° C）+ VSENSOR，其中可以根据校准值计算TCSENSOR和VSENSOR以获得更高的精度。

（3）传感器的典型等效阻抗为250kΩ。 所需的采样时间包括传感器开启时间tSENSOR（on）。

（4）导通时间tV1 / 2（on）包含在采样时间tV 1/2（样本）中。不需要按时额外。

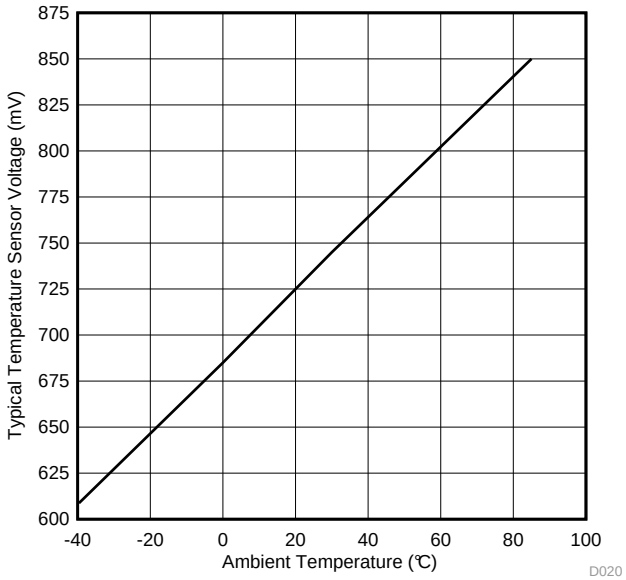



图5-29。典型温度传感器电压

表5-31列出了ADC内部参考缓冲器的特性。

表5-31。 14位ADC，内部参考缓冲器

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数测试条件 | | | VCC | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{REF+}$ | Operating supply current into AVCC terminal(1) | ADC ON, REFOUT = 0, ADC14PWRMD = 0, REFVSEL = {0, 1, 3} | 3 V | | 600 | 800 | µA |
| | | ADC ON, REFOUT = 0, ADC14PWRMD = 2, REFVSEL = {0, 1, 3} | | | 200 | 300 | |
| | | ADC ON, REFOUT = 1, ADC14PWRMD = 2, REFVSEL = {0, 1, 3} | | | 650 | 850 | |
| $t_{on}$ | Turnon time | | 3 V | | | 5 | µs |

（1）内部参考电流通过端子AVCC提供。

表5-32列出了ADC外部参考的特性。

表5-32。 14位ADC，外部参考

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

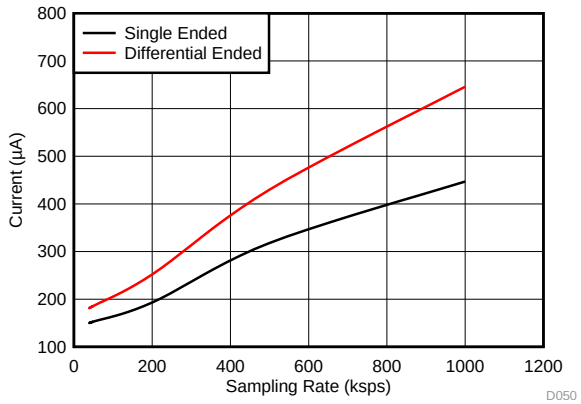
| 参数测试条件 | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{eREF+}$ | Positive external reference voltage input(1) | | 1.45 | | $AV_{CC}$ | V |
| $V_{eREF-}$ | Negative external reference voltage input | | | | 0 | V |
| ($V_{eREF+}$ - $V_{eREF-}$) | Differential external reference voltage input(1) | | 1.45 | | $AV_{CC}$ | V |
| IVeREF + IVeREF− | Static input current in single-ended input mode | 1.45 V ≤ $V_{eREF+}$≤ $V_{AVCC}$, $V_{eREF-}$ = 0 V, $f_{ADC14CLK}$ = 25 MHz, ADC14SHT0x = 0x1, ADC14SHT1x = 0x1, ADC14DIF = 0 | | | ±75 | µA |
| | | 1.45 V ≤ $V_{eREF+}$≤ $V_{AVCC}$, $V_{eREF-}$ = 0 V, $f_{ADC14CLK}$ = 5 MHz, ADC14SHT0x = 0x1, ADC14SHT1x = 0x1, ADC14DIF = 0 | | | ±15 | |
| IVeREF + IVeREF− | 差分输入模式下的静态输入电流 | 1.45 V ≤ $V_{eREF+}$≤ $V_{AVCC}$, $V_{eREF-}$ = 0 V, $f_{ADC14CLK}$ = 25 MHz, ADC14SHT0x = 0x1, ADC14SHT1x = 0x1, ADC14DIF = 1 | | | ±150 | µA |
| | | 1.45 V ≤ $V_{eREF+}$≤ $V_{AVCC}$, $V_{eREF-}$ = 0 V $f_{ADC14CLK}$ = 5 MHz, ADC14SHT0x = 0x1, ADC14SHT1x = 0x1, ADC14DIF = 1 | | | ±30 | |
| $C_{VeREF+}$ | Capacitance at VeREF+ terminal | See (2) | 5 | | | µF |

（1）对于1 Msps采样率，可以应用低至1.2 V的较低参考电压，同时降低线性度参数的精度要求。

（2）如果用于ADC14，则应将两个去耦电容（5 µF和50 nF）连接到VeREF+端子，以去耦外部参考源所需的动态电流。另请参阅MSP432P4xx SimpleLink™微控制器技术参考手册。

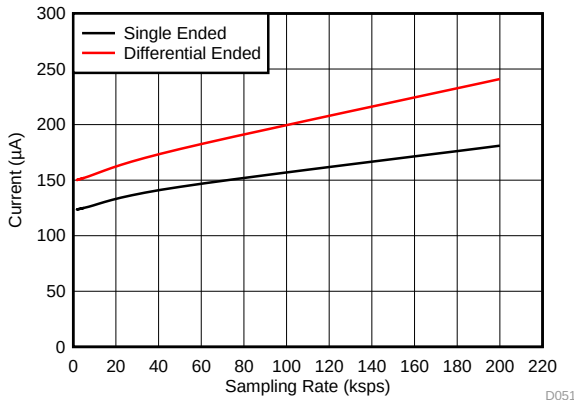
## 5.25.6.1 ADC的典型特性

typical characteristics at 3 V, 25°C, and 1-Msps sampling rate of ADC (unless otherwise specified)



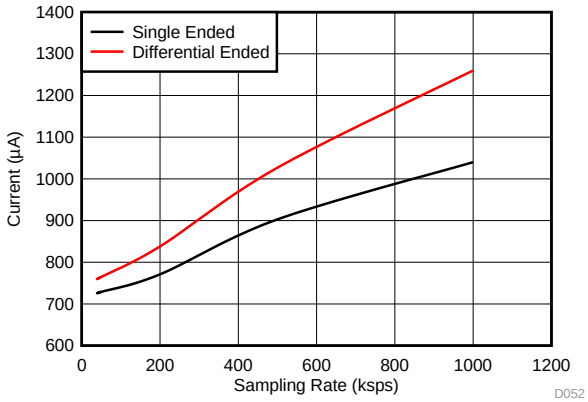

VRSEL = 14 VREF = 2.5 V
Resolution = 14 Bit ADC14PWRMD = 0

**Figure 5-30. Current vs Sampling Rate**



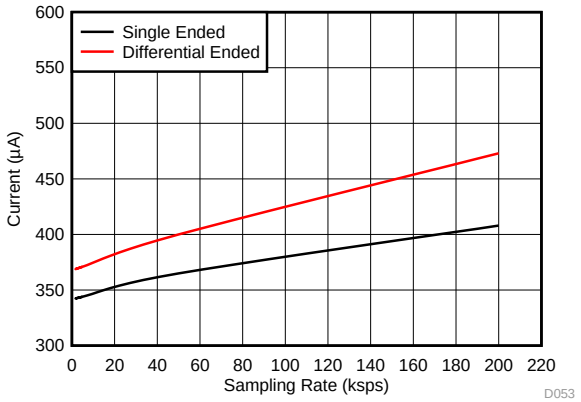

VRSEL = 14 VREF = 2.5 V
Resolution = 12 Bit ADC14PWRMD = 2

**Figure 5-31. Current vs Sampling Rate**



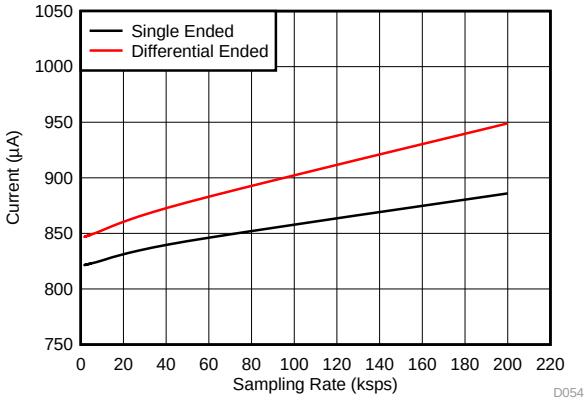

VRSEL = 1 VREF = 2.5 V
REFOUT = 0 ADC14PWRMD = 0
Resolution = 14 Bit

**Figure 5-32. Current vs Sampling Rate**



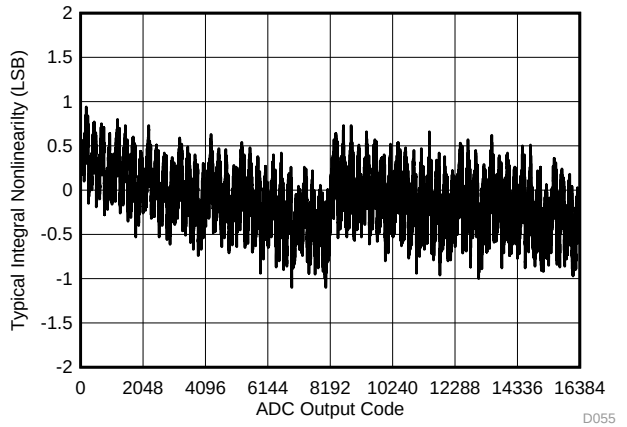

VRSEL = 1 VREF = 2.5 V
REFOUT = 0 ADC14PWRMD = 2
Resolution = 12 Bit

**Figure 5-33. Current vs Sampling Rate**




VRSEL = 1 VREF = 2.5 V
REFOUT = 1 ADC14PWRMD = 2
Resolution = 12 Bit

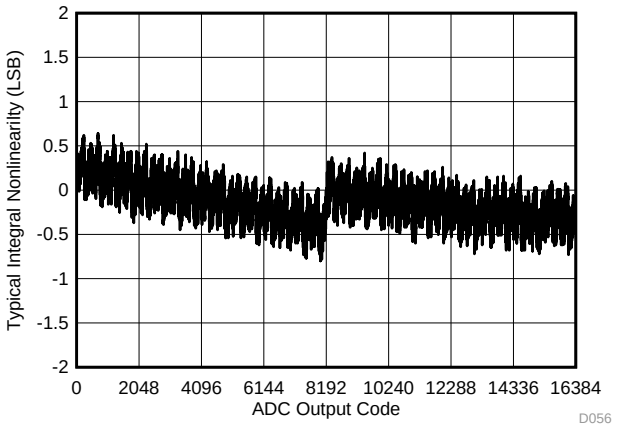
**Figure 5-34. Current vs Sampling Rate**




VRSEL = 1 VREF = 2.5 V

Input Mode = Single Ended

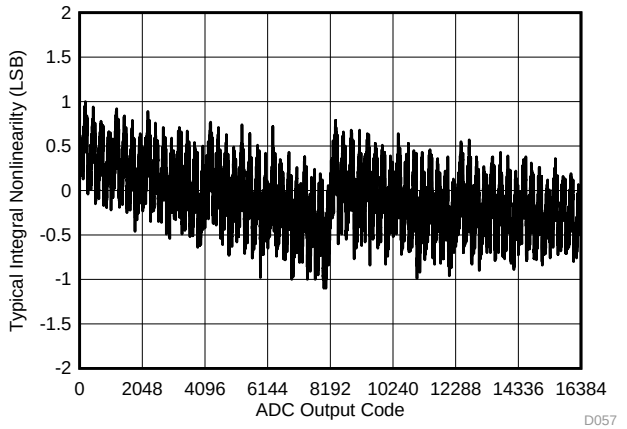
**Figure 5-35. INL vs ADC Output Code**




VRSEL = 1 VREF = 2.5 V

Input Mode = Differential

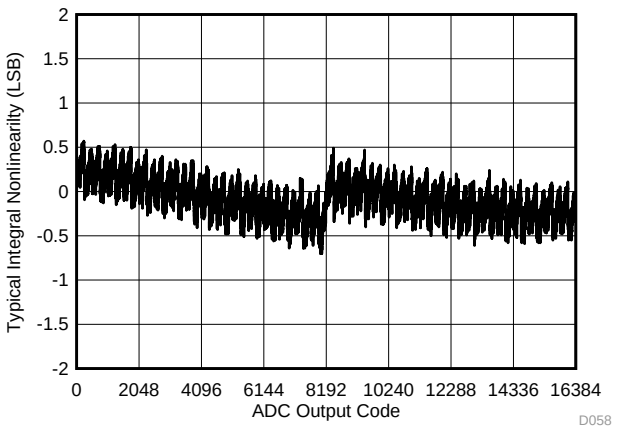
**Figure 5-36. INL vs ADC Output Code**




VRSEL = 14 VREF = 2.5 V

Input Mode = Single Ended

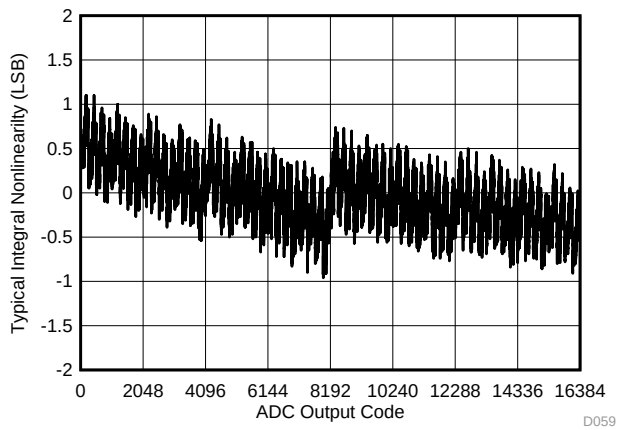
**Figure 5-37. INL vs ADC Output Code**




VRSEL = 14 VREF = 2.5 V

Input Mode = Differential

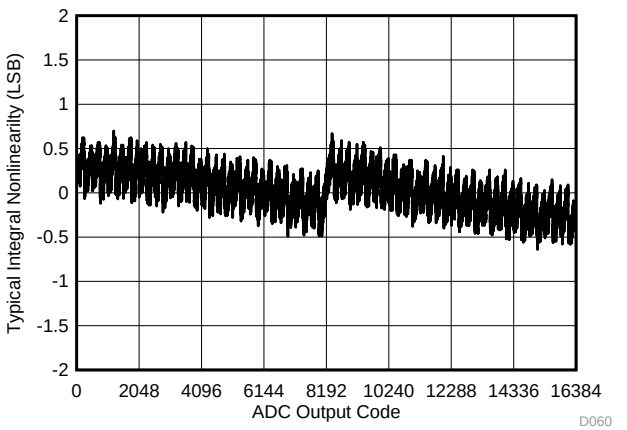
**Figure 5-38. INL vs ADC Output Code**




VRSEL = 15 VREF = 2.5 V

Input Mode = Single Ended

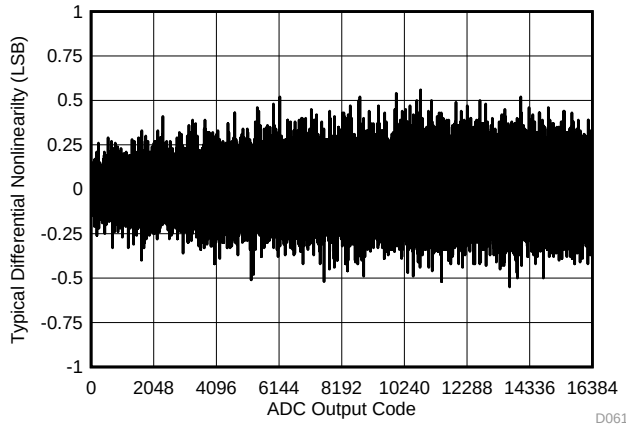
**Figure 5-39. INL vs ADC Output Code**




VRSEL = 15 VREF = 2.5 V

Input Mode = Differential

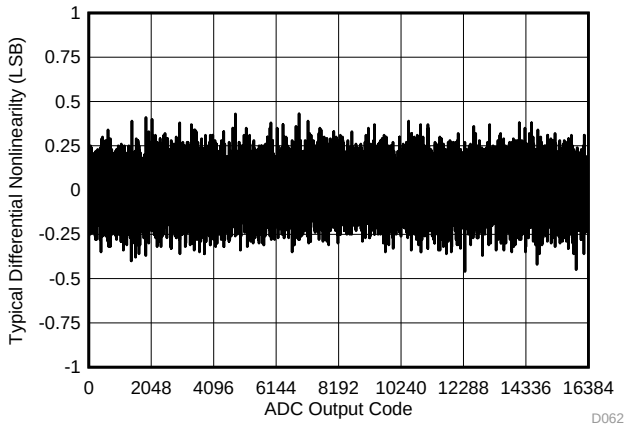
**Figure 5-40. INL vs ADC Output Code**




VRSEL = 1 VREF = 2.5 V

Input Mode = Single Ended

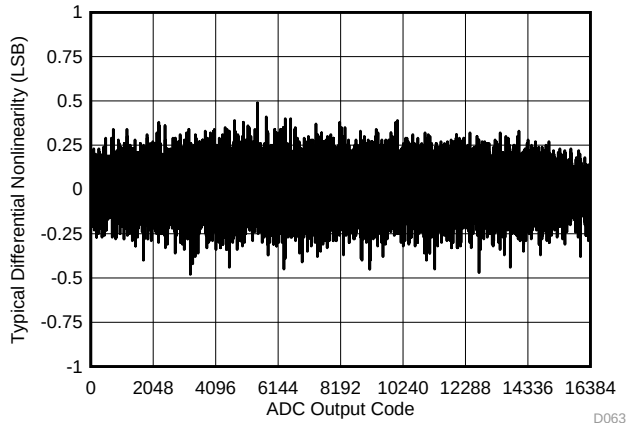
**Figure 5-41. DNL vs ADC Output Code**




VRSEL = 1 VREF = 2.5 V

Input Mode = Differential

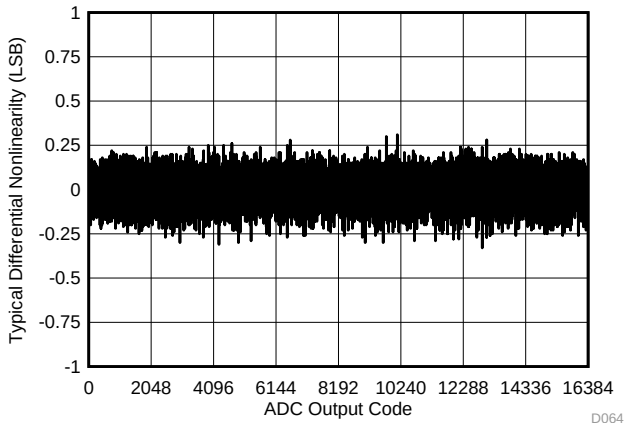
**Figure 5-42. DNL vs ADC Output Code**




VRSEL = 14 VREF = 2.5 V

Input Mode = Single Ended

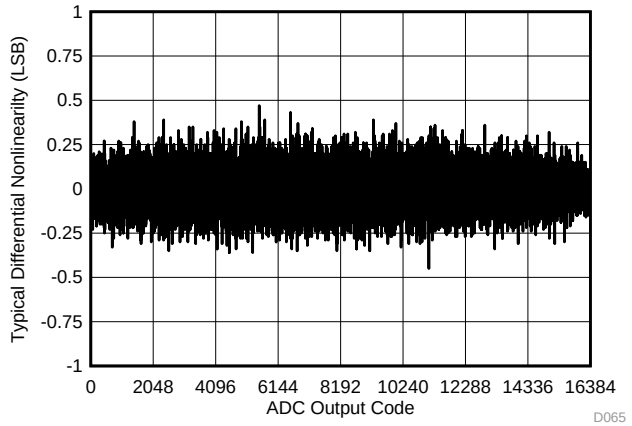
**Figure 5-43. DNL vs ADC Output Code**




VRSEL = 14 VREF = 2.5 V

Input Mode = Differential

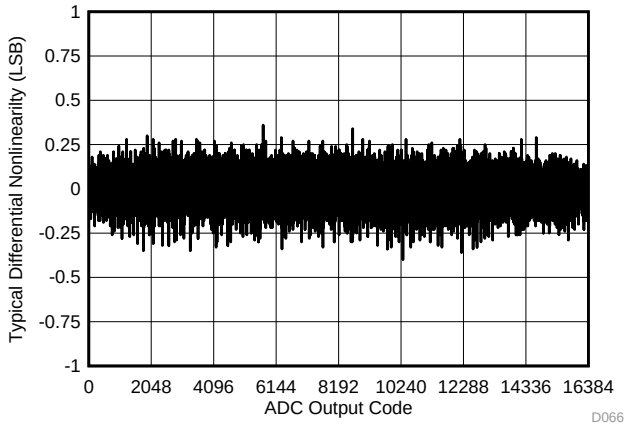
**Figure 5-44. DNL vs ADC Output Code**




VRSEL = 15 VREF = 2.5 V

Input Mode = Single Ended

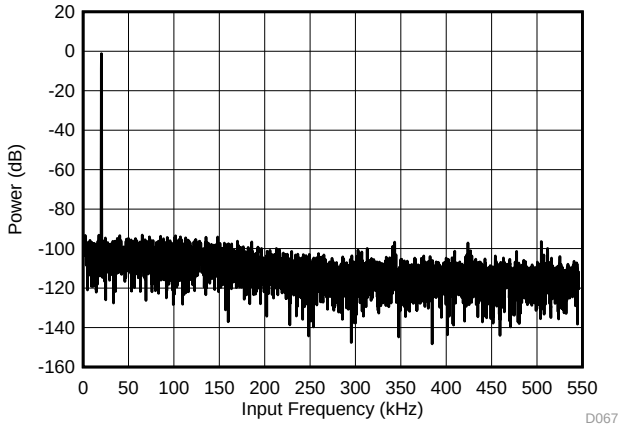
**Figure 5-45. DNL vs ADC Output Code**




VRSEL = 15 VREF = 2.5 V

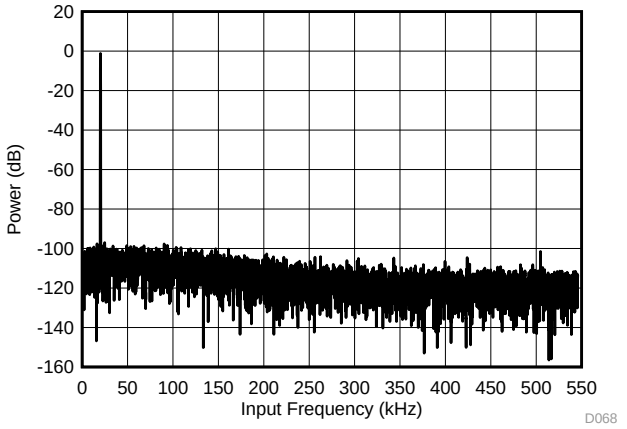
Input Mode = Differential

**Figure 5-46. DNL vs ADC Output Code**



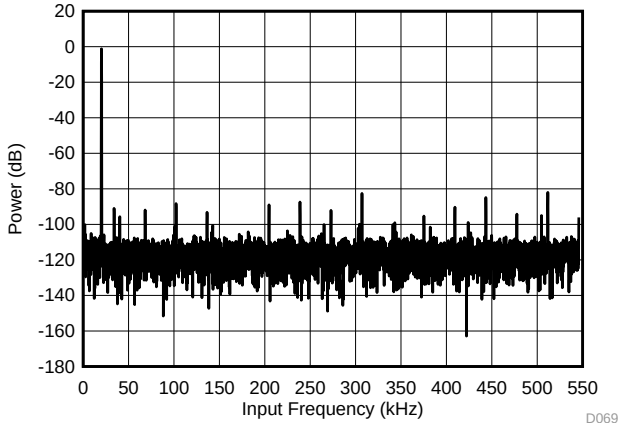

$f_{in}$ = 20 kHz | VRSEL = 1
VREF = 2.5 V | SINAD = 69 dB
THD = -86 dB | Input Mode = Single Ended

**Figure 5-47. Power vs Input Frequency**



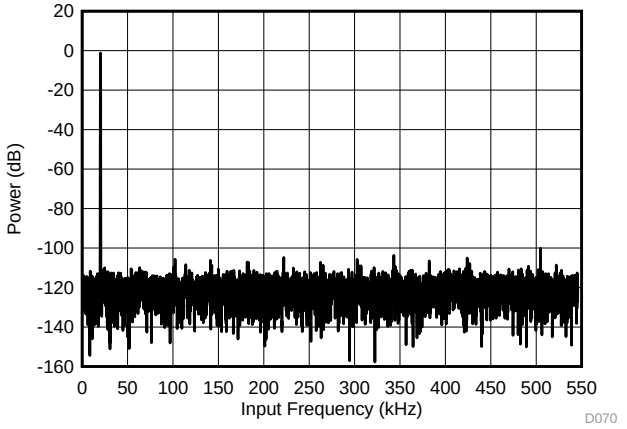

$f_{in}$ = 20 kHz | VRSEL = 1
VREF = 2.5 V | SINAD = 74 dB
THD = -91 dB | Input Mode = Differential

**Figure 5-48. Power vs Input Frequency**



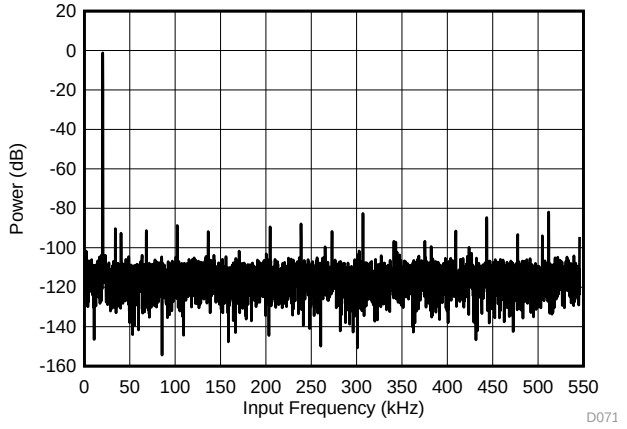

$f_{in}$ = 20 kHz | VRSEL = 14
VREF = 2.5 V | SINAD = 73 dB
THD = -92 dB | Input Mode = Single Ended

**Figure 5-49. Power vs Input Frequency**



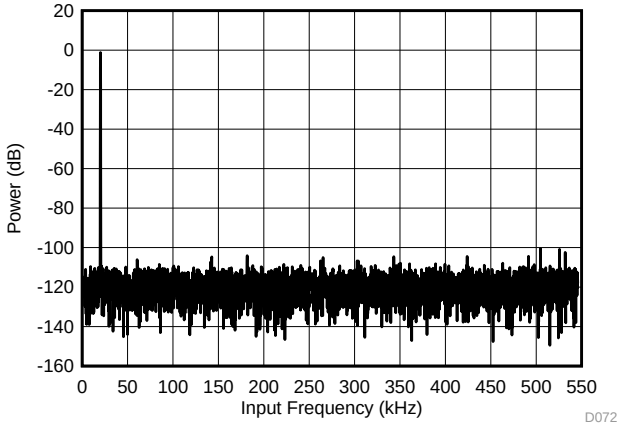

$f_{in}$ = 20 kHz | VRSEL = 14
VREF = 2.5 V | SINAD = 82 dB
THD = -100 dB | Input Mode = Differential

**Figure 5-50. Power vs Input Frequency**



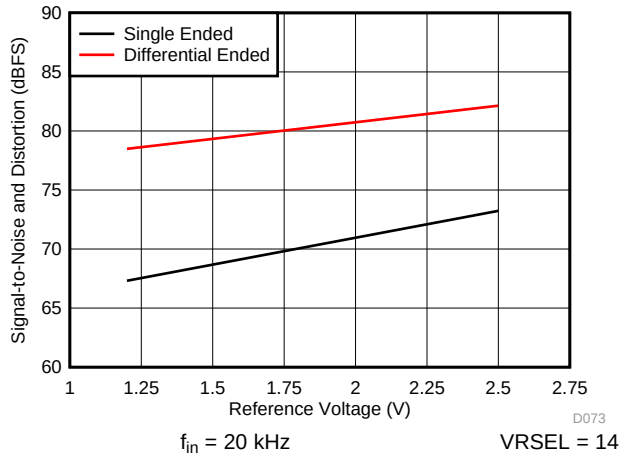

$f_{in}$ = 20 kHz | VRSEL = 15
VREF = 2.5 V | SINAD = 72 dB
THD = -90 dB | Input Mode = Single Ended

**Figure 5-51. Power vs Input Frequency**



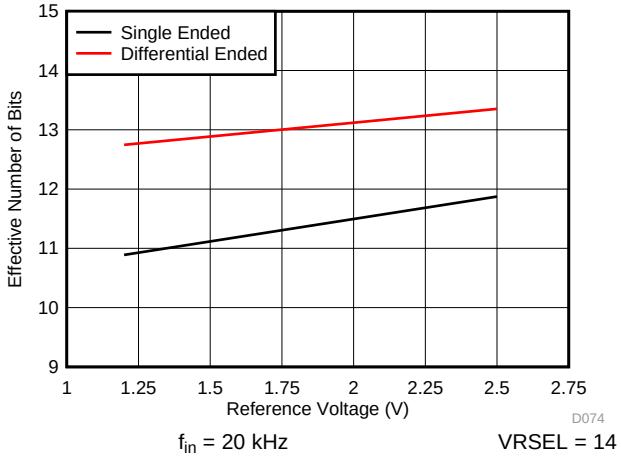

$f_{in}$ = 20 kHz | VRSEL = 15
VREF = 2.5 V | SINAD = 80 dB
THD = -100 dB | Input Mode = Differential

**Figure 5-52. Power vs Input Frequency**



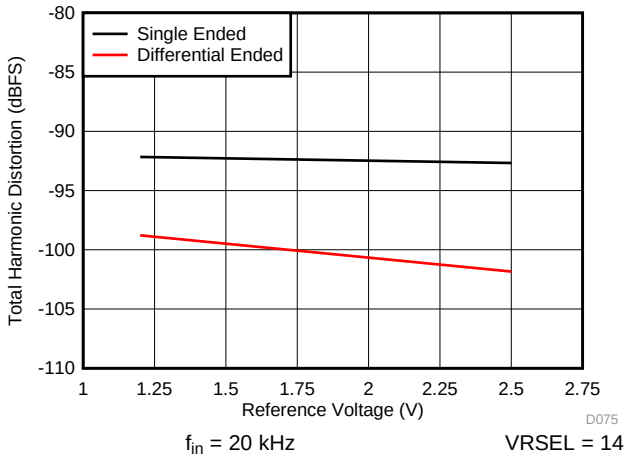

$f_{in}$ = 20 kHz VRSEL = 14

**Figure 5-53. SINAD vs Reference Voltage**



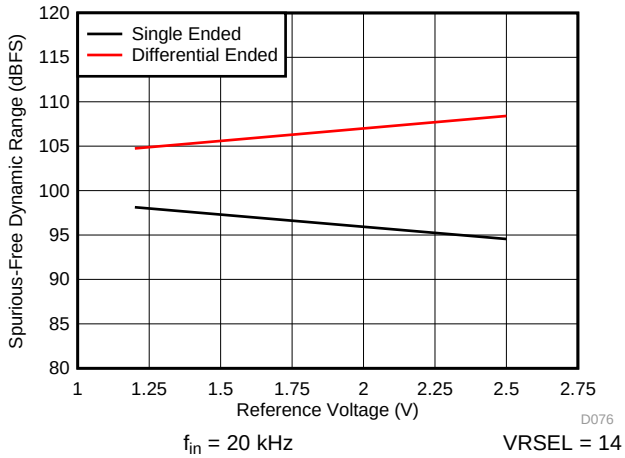

$f_{in}$ = 20 kHz VRSEL = 14

**Figure 5-54. ENOB vs Reference Voltage**



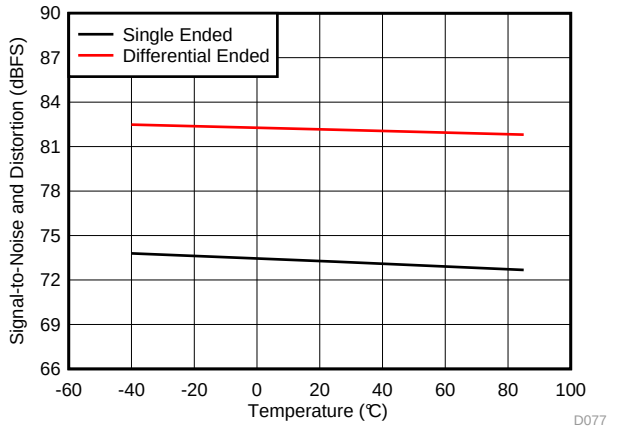

$f_{in}$ = 20 kHz VRSEL = 14

**Figure 5-55. THD vs Reference Voltage**



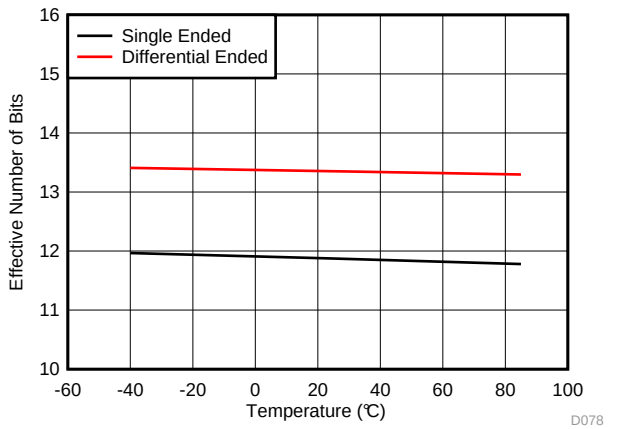

$f_{in}$ = 20 kHz VRSEL = 14

**Figure 5-56. SFDR vs Reference Voltage**



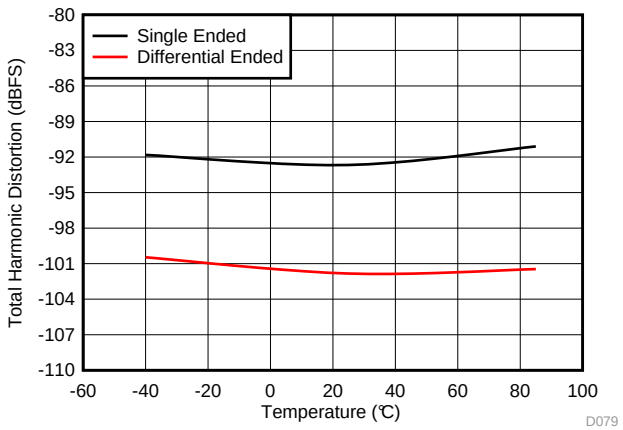

$f_{in}$ = 20 kHz VRSEL = 14 VREF = 2.5 V

**Figure 5-57. SINAD vs Temperature**



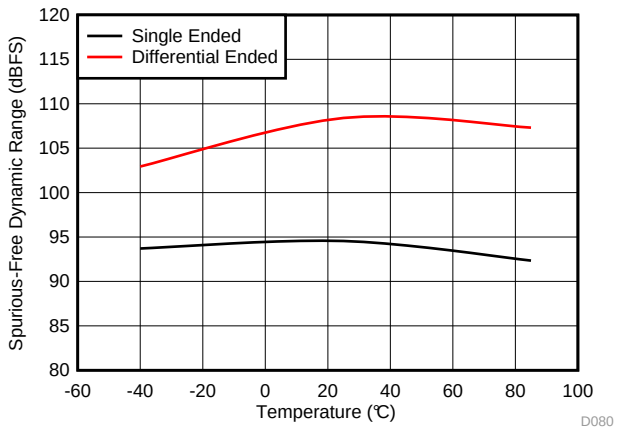

$f_{in}$ = 20 kHz VRSEL = 14 VREF = 2.5 V

**Figure 5-58. ENOB vs Temperature**



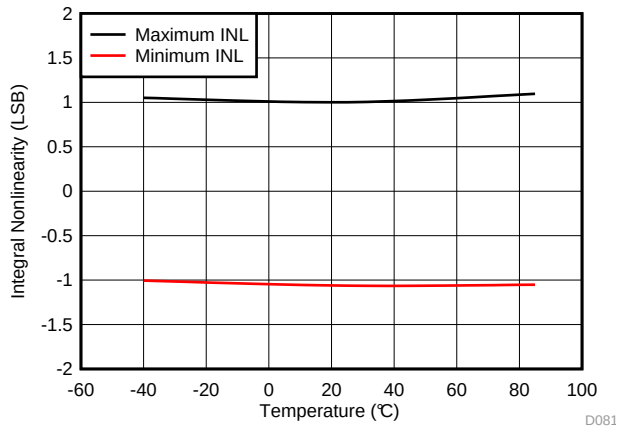

$f_{in}$ = 20 kHz VRSEL = 14 VREF = 2.5 V

**Figure 5-59. THD vs Temperature**



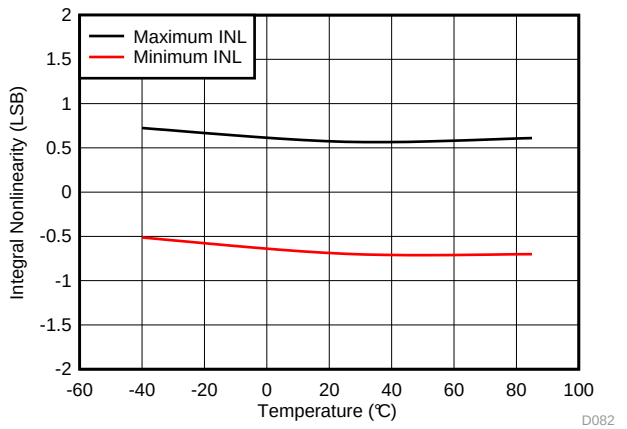

$f_{in}$ = 20 kHz VRSEL = 14 VREF = 2.5 V

**Figure 5-60. SFDR vs Temperature**



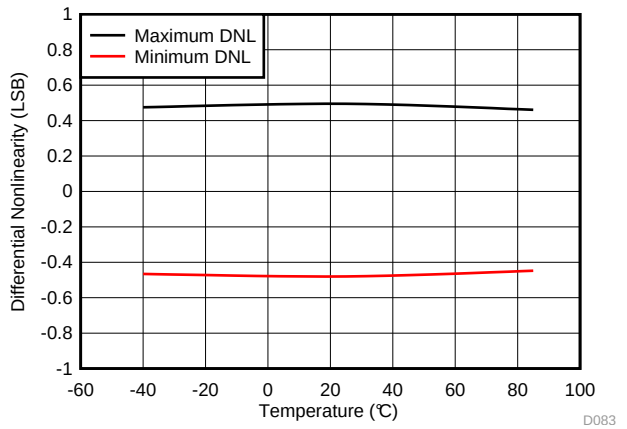

VRSEL = 14 VREF = 2.5 V
Input Mode = Single Ended

**Figure 5-61. INL vs Temperature**



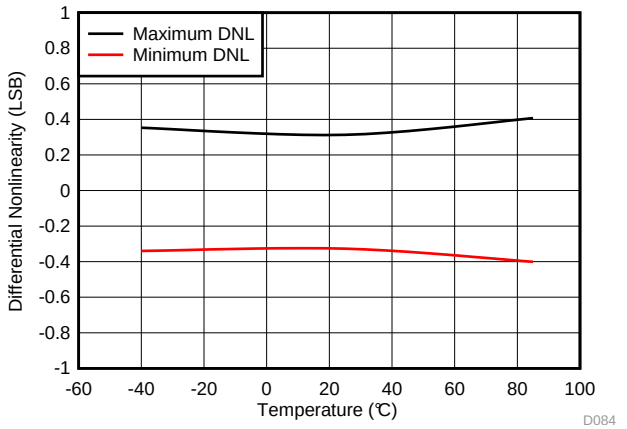

VRSEL = 14 VREF = 2.5 V
Input Mode = Differential

**Figure 5-62. INL vs Temperature**



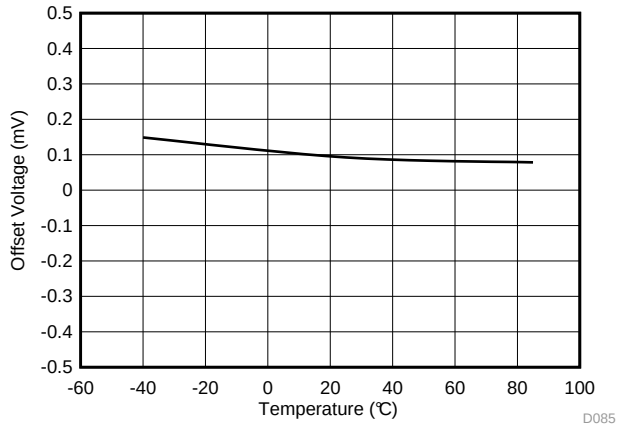

VRSEL = 14 VREF = 2.5 V
Input Mode = Single Ended

**Figure 5-63. DNL vs Temperature**




VRSEL = 14 VREF = 2.5 V
Input Mode = Differential

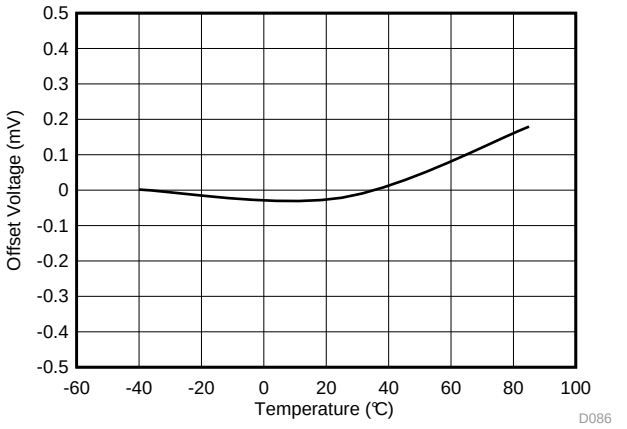
**Figure 5-64. DNL vs Temperature**




VRSEL = 14 VREF = 2.5 V

Input Mode = Single Ended

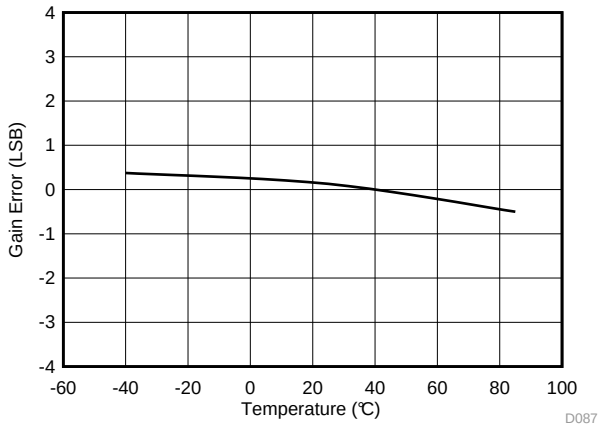
图5-65。偏移电压与温度的关系




VRSEL = 14 VREF = 2.5 V

Input Mode = Differential

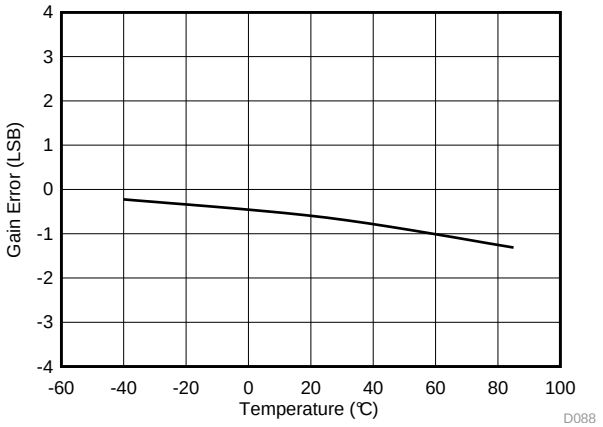
图5-66。偏移电压与温度的关系




VRSEL = 14 VREF = 2.5 V

Input Mode = Single Ended

**Figure 5-67. Gain Error vs Temperature**




VRSEL = 14 VREF = 2.5 V

Input Mode = Differential

**Figure 5-68. Gain Error vs Temperature**

## 5.25.7 REF_A

表5-33列出了REF_A内置参考的特性。

表5-33。 REF_A，内置参考（LDO操作）

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数 | 测试条件 | VCC | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{REF+}$ | Positive built-in reference voltage output | REFVSEL = {0}表示1.2 V，REFON = 1 | 1.62 V | 1.2±1% | | |
| | | REFVSEL = {1}表示1.45 V，REFON = 1 | 1.75 V | 1.45±1% | | |
| | | REFVSEL = {3}表示2.5 V，REFON = 1 | 2.8 V | 2.5±1% | | |
| $AV_{CC(min)}$ | AVCC minimum voltage, Positive built-in reference active | REFVSEL = {0} for 1.2 V | | 1.62 | | V |
| | | REFVSEL = {1} for 1.45 V | | 1.75 | | |
| | | REFVSEL = {3} for 2.5 V | | 2.8 | | |
| $I_{REF+}$ | Operating supply current into AVCC terminal(1) | REFON = 1 | 3 V | | 15 | 20 | µA |
| $I_{O(VREF+)}$ | VREF maximum load current, VREF+ terminal | REFVSEL = {0, 1, 3}, $AV_{CC}$ = $AV_{CC\ (min)}$ for each reference level, REFON = REFOUT = 1 | | –1000 | | +10 | µA |
| $I_{L(VREF+)}$ | Load-current regulation, VREF+ terminal | REFVSEL = {0, 1, 3}, I(VREF+) = +10 µA or –1000 µA, $AV_{CC}$ = $AV_{CC\ (min)}$ for each reference level, REFON = REFOUT = 1 | | | | 2500 | µV/mA |
| $C_{VREF±}$ | Capacitance at VREF+, VREF- terminals | REFON = REFOUT = 1 | | 0 | | 100 | pF |
| $PSRR\_DC_{REFOUT0}$ | Power supply rejection ratio (DC) after ADC buffer | 每个参考电平AVCC = AVCC（min），REFVSEL = {0,1,3}，REFON = 1，REFOUT = 0 | | | 50 | 350 | µV/V |
| $PSRR\_DC_{REFOUT1}$ | Power supply rejection ratio (DC) after ADC buffer | 每个参考电平AVCC = AVCC（min），REFVSEL = {0,1,3}，REFON = 1，REFOUT = 1 | | | 50 | 250 | µV/V |
| $PSRR\_AC_{REFOUT0}$ | Power supply rejection ratio (AC) after ADC buffer | 每个参考电平AVCC = AVCC（min），1 kHz时dAVCC = 0.1 V，REFVSEL = {0,1,3}，REFON = 1，REFOUT = 0 | | | 2 | 10 | mV/V |
| $PSRR\_AC_{REFOUT1}$ | Power supply rejection ratio (AC) after ADC buffer | 每个参考电平AVCC = AVCC（min），1 kHz时dAVCC = 0.1 V，REFVSEL = {0,1,3}，REFON = 1，REFOUT = 1 | | | 2 | 5 | mV/V |
| $TC_{REF+}$ (2) | Temperature coefficient of built-in reference | REFVSEL = {0, 1, 3}, REFON = 1, $T_A$ = –40°C to 85°C | | | 10 | 25 | ppm/°C |
| $t_{SETTLE}$ | Settling time of reference voltage(3) | $AV_{CC}$ = $AV_{CC\ (min)}$ to $AV_{CC(max)}$ REFVSEL = {0, 1, 3}, REFON = 0 → 1 | | | 70 | 80 | µs |

（1）内部参考电流由端子AVCC提供。

（2）使用盒法计算：（MAX（-40° C至85° C） - MIN（-40° C至85° C））/ MIN（-40° C至85° C）/（85° C - （ - 40° C））。

（3）条件是在tSETTLE小于±0.5 LSB后ADC转换中的错误开始。

## 5.25.8 Comparator_E

表5-34列出了比较器的特性。

**Table 5-34. Comparator_E**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数测试条件VCC | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | 1.62 | 3.7 | V |
| $I_{AVCC\_COMP}$ | Comparator operating supply current into AVCC, Excludes reference resistor ladder | CEPWRMD = 00, CEON = 1, CERSx = 00 (fast) | 2.2 V, 3 V | 10 | 15 | µA |
| | | CEPWRMD = 01, CEON = 1, CERSx = 00 (medium) | 2.2 V, 3 V | 8 | 10 | |
| | | CEPWRMD = 10, CEON = 1, CERSx = 00 (slow), $T_A$ = 30°C | 2.2 V, 3 V | | 0.5 | |
| | | CEPWRMD = 10, CEON = 1, CERSx = 00 (slow), $T_A$ = 85°C | 2.2 V, 3 V | | 0.5 | |
| $I_{AVCC\_REF}$ | Quiescent current of resistor ladder into AVCC, Includes REF_A module current | CEREFACC = 0, CEREFLx = 01, CERSx = 10, REFON = 0, CEON = 0 | 2.2 V, 3 V | 25 | 35 | µA |
| | | CEREFACC = 1, CEREFLx = 01, CERSx = 10, REFON = 0, CEON = 0 | 2.2 V, 3 V | 10 | 15 | |
| $V_{REF}$ | Reference voltage level | CERSx = 11, CEREFLx = 01, CEREFACC = 0 | 1.62 V | 1.17 | 1.2 | 1.23 | V |
| | | CERSx = 11, CEREFLx = 10, CEREFACC = 0 | 2.2 V | 1.95 | 2.0 | 2.05 | |
| | | CERSx = 11, CEREFLx = 11, CEREFACC = 0 | 2.7 V | 2.40 | 2.5 | 2.60 | |
| | | CERSx = 11, CEREFLx = 01, CEREFACC = 1 | 1.62 V | 1.15 | 1.2 | 1.23 | |
| | | CERSx = 11, CEREFLx = 10, CEREFACC = 1 | 2.2 V | 1.92 | 2.0 | 2.05 | |
| | | CERSx = 11, CEREFLx = 11, CEREFACC = 1 | 2.7 V | 2.4 | 2.5 | 2.6 | |
| $V_{IC}$ | Common mode input range | | | 0 | | VCC–1 | V |
| $V_{OFFSET}$ | Input offset voltage | CEPWRMD = 00 | | –10 | | +10 | mV |
| | | CEPWRMD = 01 | | –20 | | +20 | |
| | | CEPWRMD = 10 | | –20 | | +20 | |
| $C_{IN}$ | Input capacitance | CEPWRMD = 00 or CEPWRMD = 01 | | | 8 | | pF |
| | | CEPWRMD = 10 | | | 8 | | |
| $R_{SIN}$ | Series input resistance | On (switch closed) | | | 2 | 4 | kΩ |
| | | Off (switch open) | | 50 | | | MΩ |
| $t_{PD}$ | Propagation delay, response time | CEPWRMD = 00, CEF = 0, Overdrive ≥ 20 mV | | | 330 | 550 | ns |
| | | CEPWRMD = 01, CEF = 0, Overdrive ≥ 20 mV | | | 410 | 650 | |
| | | CEPWRMD = 10, CEF = 0, Overdrive ≥ 20 mV | | | | 30 | µs |
| $t_{PD,filter}$ | Propagation delay with filter active | CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 00 | | | 0.6 | 0.9 | µs |
| | | CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 01 | | | 1.1 | 1.6 | |
| | | CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 10 | | | 2 | 3 | |
| | | CEPWRMD = 00 or 01, CEF = 1, Overdrive ≥ 20 mV, CEFDLY = 11 | | | 4 | 6 | |

**Table 5-34. Comparator_E (continued)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数测试条件VCC | | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{EN\_CMP}$ | Comparator enable time | CEON = 0 to 1, CEPWRMD = 00, VIN+, VIN- from pins, Overdrive ≥ 20 mV | | | 0.8 | 1 | µs |
| | | CEON = 0 to 1, CEPWRMD = 01, VIN+, VIN- from pins, Overdrive ≥ 20 mV | | | 0.9 | 1.2 | |
| | | CEON = 0 to 1, CEPWRMD = 10, VIN+, VIN- from pins, Overdrive ≥ 20 mV | | | 15 | 25 | |
| $t_{EN\_CMP\_VREF}$ | Comparator and reference ladder and reference voltage enable time | CEON = 0 to 1, CEPWRMD = 00, CEREFLx = 10, CERSx = 11, REFON = 0, Overdrive ≥ 20 mV | | | 90 | 120 | µs |
| | | CEON = 0 to 1, CEPWRMD = 01, CEREFLx = 10, CERSx = 11, REFON = 0, Overdrive ≥ 20 mV | | | 90 | 120 | |
| | | CEON = 0 to 1, CEPWRMD = 10, CEREFLx = 10, CERSx = 11, REFON = 0, Overdrive ≥ 20 mV | | | 90 | 120 | |
| | | CEON = 0 to 1, CEPWRMD = 00, CEREFLx = 10, CERSx = 10, REFON = 0, CEREF0/1 = 0x0F, Overdrive ≥ 20 mV | | | 90 | 180 | |
| | | CEON = 0 to 1, CEPWRMD = 01, CEREFLx = 10, CERSx = 10, REFON = 0, CEREF0/1 = 0x0F, Overdrive ≥ 20 mV | | | 90 | 180 | |
| | | CEON = 0 to 1, CEPWRMD = 10, CEREFLx = 10, CERSx = 10, REFON = 0, CEREF0/1 = 0x0F, Overdrive ≥ 20 mV | | | 90 | 180 | |
| $t_{EN\_CMP\_RL}$ | Comparator and reference ladder enable time | CEON = 0 to 1, CEPWRMD = 00, CEREFLx = 10, CERSx = 10, REFON = 1, CEREF0/1 = 0x0F, Overdrive ≥ 20 mV | | | 1.5 | 2 | µs |
| | | CEON = 0 to 1, CEPWRMD = 01, CEREFLx = 10, CERSx = 10, REFON = 1, CEREF0/1 = 0x0F, Overdrive ≥ 20 mV | | | 1.5 | 2 | |
| | | CEON = 0 to 1, CEPWRMD = 10, CEREFLx = 10, CERSx = 10, REFON = 1, CEREF0/1 = 0x0F, Overdrive ≥ 20 mV | | | 15 | 25 | |
| $V_{CMP\_REF}$ | Reference voltage for a given tap | VIN = reference into resistor ladder, n = 0 to 31 | | VIN × (n + 0.9) / 32 | VIN × (n + 1) / 32 | VIN × (n + 1.1) / 32 | V |

### 5.25.9 eUSCI

表5-35列出了UART模式下eUSCI支持的时钟频率。

表5-35。 eUSCI（UART模式）时钟频率

| 参数 | 测试条件 | VCORE | MIN | TYP | MAX | 单元 |
|---|---|---|---|---|---|---|
| $f_{eUSCI}$ eUSCI input clock frequency | Internal: SMCLK, External: UCLK, Duty cycle = 50% ±10% | 1.2 V | | | 12 | MHz |
| | | 1.4 V | | | 24 | |
| $f_{BITCLK}$ BITCLK clock frequency (equals baud rate in MBaud) | | 1.2 V | | | 5 | MHz |
| | | 1.4 V | | | 7 | |

表5-36列出了UART模式下eUSCI的特性。

表5-36。 eUSCI（UART模式）开关特性

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数 | 测试条件 | VCC | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_t$ UART receive deglitch time(1) | UCGLITx = 0 | | | 5 | 20 | ns |
| | UCGLITx = 1 | | | 20 | 60 | |
| | UCGLITx = 2 | | | 30 | 100 | |
| | UCGLITx = 3 | | | 50 | 150 | |

（1）抑制短于UART接收去毛刺时间的UART接收输入（UCxRX）上的脉冲。因此，选定的抗尖峰脉冲时间可以限制最大可用波特率。为确保正确识别脉冲，其持续时间应超过抗尖峰脉冲时间的最大规格。

表5-37列出了SPI主模式下eUSCI支持的时钟频率。

表5-37。 eUSCI（SPI主模式）时钟频率

| 参数 | 条件 | VCC | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{eUSCI}$ eUSCI input clock frequency | SMCLK, Duty cycle = 50% ±10% | VCORE = 1.2 V | | | 12 | MHz |
| | | VCORE = 1.4 V | | | 24 | |

表5-38列出了SPI主模式下eUSCI的特性。

**Table 5-38. eUSCI (SPI Master Mode)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

| 参数测试条件VCORE VCC MIN MAX单元 | | | | | | |
|---|---|---|---|---|---|---|
| $t_{STE,LEAD}$ | STE lead time, STE active to clock | UCSTEM = 1, UCMODEx = 01 or 10 | | | 1 | UCxCLK cycles |
| $t_{STE,LAG}$ | STE lag time, Last clock to STE inactive | UCSTEM = 1, UCMODEx = 01 or 10 | | | 1 | UCxCLK cycles |
| $t_{STE,ACC}$ | STE access time, STE active to SIMO data out | UCSTEM = 0, UCMODEx = 01 or 10 | | 1.62 V | 30 | ns |
| | | | | 3.7 V | 20 | |
| $t_{STE,DIS}$ | STE disable time, STE inactive to SIMO high impedance | UCSTEM = 0, UCMODEx = 01 or 10 | | 1.62 V | 20 | ns |
| | | | | 3.7 V | 15 | |
| $t_{SU,MI}$ | SOMI input data setup time | | 1.2 V | 1.62 V | 45 | ns |
| | | | 1.4 V | 3.7 V | 30 | |
| $t_{HD,MI}$ | SOMI input data hold time | | | 1.62 V | 0 | ns |
| | | | | 3.7 V | 0 | |
| $t_{VALID,MO}$ | SIMO output data valid time(2) | UCLK edge to SIMO valid, $C_L$ = 20 pF | | 1.62 V | 14 | ns |
| | | | | 3.7 V | 7 | |
| $t_{HD,MO}$ | SIMO output data hold time(3) | $C_L$ = 20 pF | | 1.62 V | 0 | ns |
| | | | | 3.7 V | 0 | |

（1）fUCxCLK = 1 /（2tLO / HI），tLO / HI = MAX（tVALID，MO（eUSCI）+ tSU，SI（从机），tSU，MI（eUSCI）+ tVALID，SO（从机））对于从机参数tSU，SI（从站）和tVALID，SO（从站），请参见所连接从站的SPI参数。

（2）指定在输出改变UCLK时钟沿之后将下一个有效数据驱动到SIMO输出的时间。请参见图5-69和图5-70中的时序图。

（3）指定输出改变UCLK时钟沿后SIMO输出上的数据有效的时间。负值表示在UCLK上观察到输出更改时钟沿之前，SIMO输出上的数据可能无效。请参见图569和图5-70中的时序图。

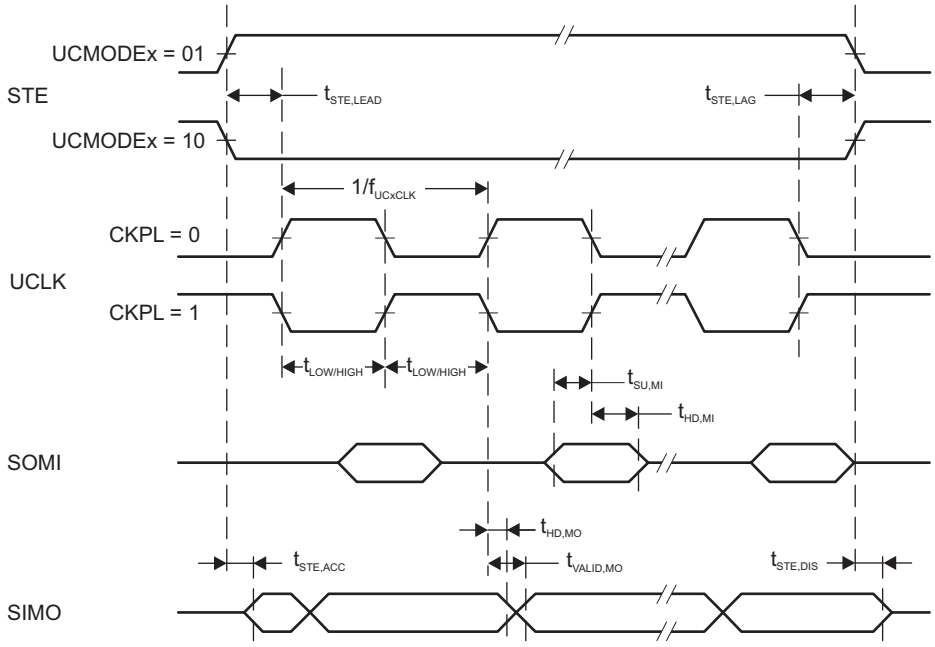



**Figure 5-69. SPI Master Mode, CKPH = 0**

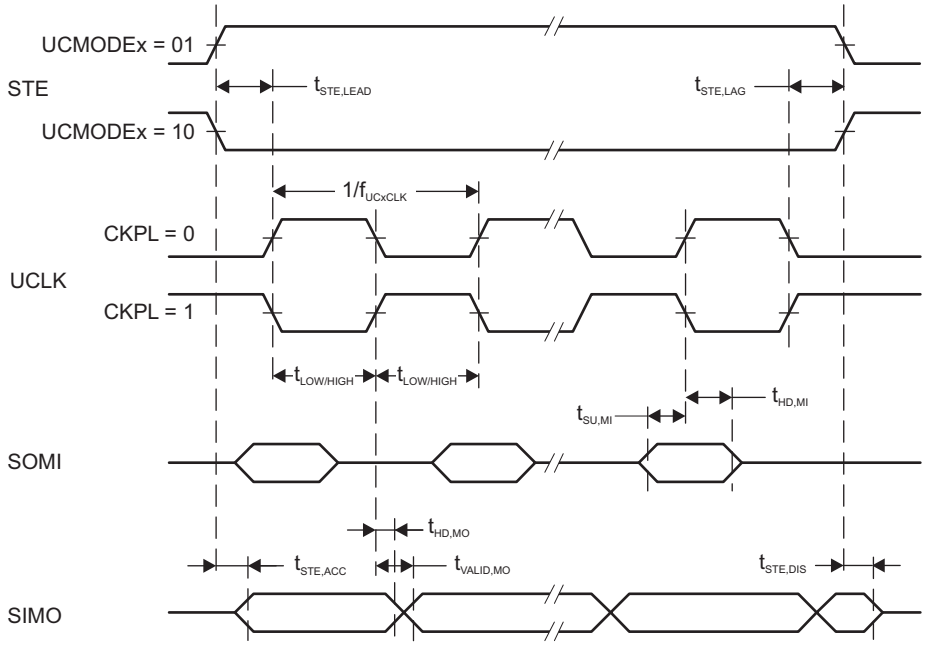



**Figure 5-70. SPI Master Mode, CKPH = 1**

表5-39列出了SPI从模式下eUSCI的特性。

**Table 5-39. eUSCI (SPI Slave Mode)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

| | | 参数测试条件VCC | MIN | MAX | 单元 |
|---|---|---|---|---|---|
| $t_{STE,LEAD}$ | STE lead time, STE active to clock | | 1.62 V | 45 | ns |
| | | | 3.7 V | 20 | |
| $t_{STE,LAG}$ | STE lag time, Last clock to STE inactive | | 1.62 V | 1 | ns |
| | | | 3.7 V | 1 | |
| $t_{STE,ACC}$ | STE access time, STE active to SOMI data out | | 1.62 V | 25 | ns |
| | | | 3.7 V | 15 | |
| $t_{STE,DIS}$ | STE disable time, STE inactive to SOMI high impedance | | 1.62 V | 18 | ns |
| | | | 3.7 V | 14 | |
| $t_{SU,SI}$ | SIMO input data setup time | | 1.62 V | 3 | ns |
| | | | 3.7 V | 2 | |
| $t_{HD,SI}$ | SIMO input data hold time | | 1.62 V | 0 | ns |
| | | | 3.7 V | 0 | |
| $t_{VALID,SO}$ | SOMI output data valid time(2) | UCLK edge to SOMI valid, $C_L$ = 20 pF | 1.62 V | 35 | ns |
| | | | 3.7 V | 18 | |
| $t_{HD,SO}$ | SOMI output data hold time(3) | $C_L$ = 20 pF | 1.62 V | 10 | ns |
| | | | 3.7 V | 6 | |

（1）fUCxCLK = 1 /（2tLO / HI），tLO /HI≥MAX（tVALID，MO（主站）+ tSU，SI（eUSCI），tSU，MI（主站）+ tVALID，SO（eUSCI））用于主站参数tSU，MI（主站）和tVALID，MO（主站），请参见附加主站的SPI参数。

（2）指定输出更改UCLK时钟沿后，将下一个有效数据驱动到SOMI输出的时间。请参见图5-71和图5-72中的时序图。

（3）指定输出改变UCLK时钟沿后SOMI输出上的数据有效的时间。请参见图5-71和图5-72中的时序图。

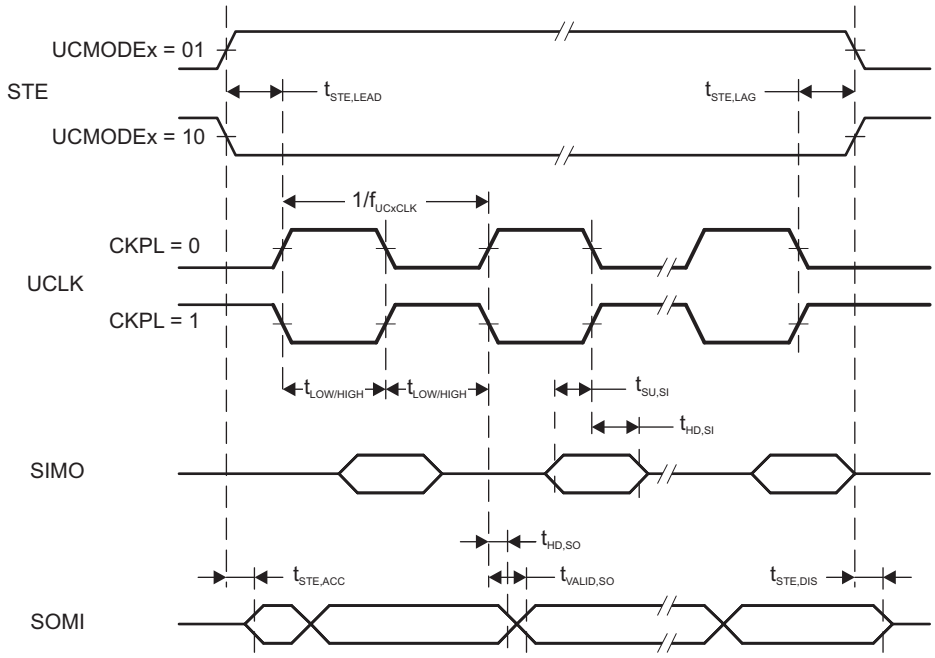



**Figure 5-71. SPI Slave Mode, CKPH = 0**

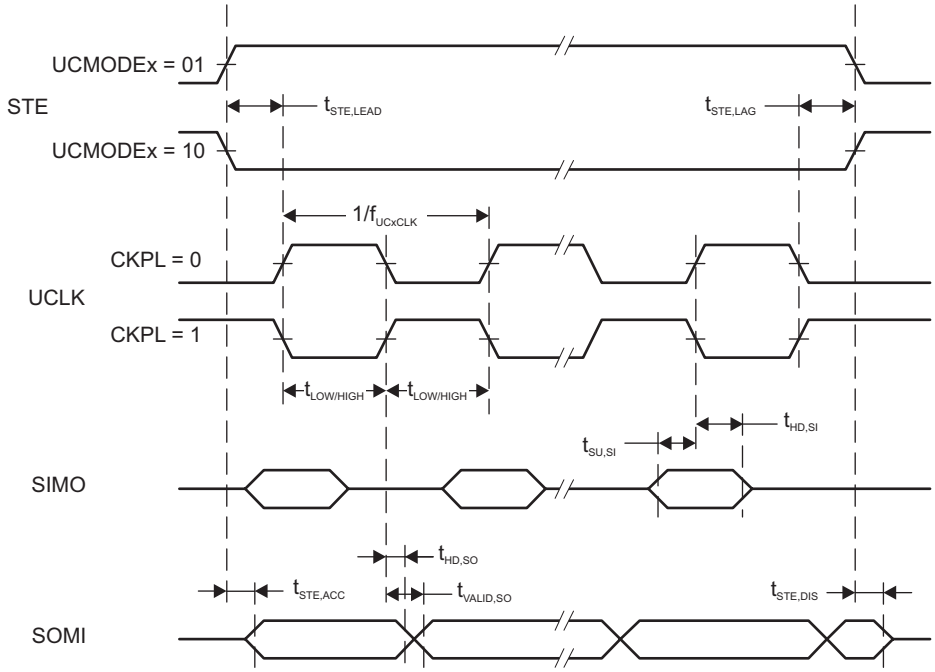



**Figure 5-72. SPI Slave Mode, CKPH = 1**

表5-40列出了I2C模式下eUSCI支持的时钟频率。

表5-40。 eUSCI（I2C模式）时钟频率

| 参数测试条件VCORE | VCC | MIN | MAX单元 | | | |
|---|---|---|---|---|---|---|
| $f_{eUSCI}$ | eUSCI input clock frequency | Internal: SMCLK, External: UCLK, Duty cycle = 50% ±10% | 1.2 V | 12 | | MHz |
| | | | 1.4 V | 24 | | |
| $f_{SCL}$ | SCL clock frequency | | | | 1 | MHz |

表5-41列出了I2C模式下eUSCI的特性。

**Table 5-41. eUSCI ($I^2C$ Mode)**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 5-73)

| 参数测试条件 | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{HD,STA}$ | Hold time (repeated) START | $f_{SCL}$ = 100 kHz | 5.5 | | µs |
| | | $f_{SCL}$ = 400 kHz | 1.5 | | |
| | | $f_{SCL}$ = 1 MHz | 0.6 | | |
| $t_{SU,STA}$ | Setup time for a repeated START | $f_{SCL}$ = 100 kHz | 5.5 | | µs |
| | | $f_{SCL}$ = 400 kHz | 1.5 | | |
| | | $f_{SCL}$ = 1 MHz | 0.6 | | |
| $t_{HD,DAT}$ | Data hold time | $f_{SCL}$ = 100 kHz | 80 | | ns |
| | | $f_{SCL}$ = 400 kHz | 80 | | |
| | | $f_{SCL}$ = 1 MHz | 80 | | |
| $t_{SU,DAT}$ | Data setup time | $f_{SCL}$ = 100 kHz | 5.5 | | µs |
| | | $f_{SCL}$ = 400 kHz | 1.5 | | |
| | | $f_{SCL}$ = 1 MHz | 0.6 | | |
| $t_{SU,STO}$ | Setup time for STOP | $f_{SCL}$ = 100 kHz | 5.5 | | µs |
| | | $f_{SCL}$ = 400 kHz | 1.5 | | |
| | | $f_{SCL}$ = 1 MHz | 0.6 | | |
| $t_{SP}$ | Pulse duration of spikes suppressed by input filter | UCGLITx = 0 | 50 | 120 | ns |
| | | UCGLITx = 1 | 25 | 60 | |
| | | UCGLITx = 2 | 10 | 35 | |
| | | UCGLITx = 3 | 5 | 20 | |
| $t_{TIMEOUT}$ | Clock low time-out | UCCLTOx = 1 | 27 | | ms |
| | | UCCLTOx = 2 | 30 | | |
| | | UCCLTOx = 3 | 33 | | |

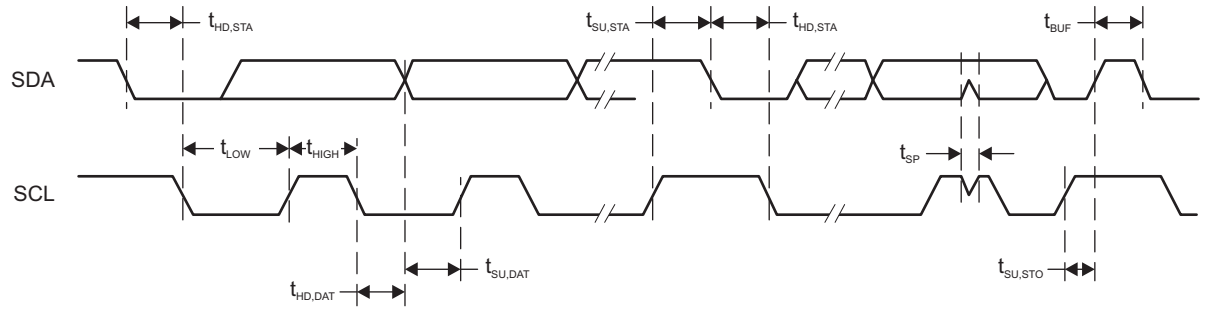



**Figure 5-73. $I^2C$ Mode Timing**

## 5.25.10定时器

表5-42列出了Timer_A的特性。

**Table 5-42. Timer_A**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数测试条件VCORE VCC MIN MAX单元 | | | | | | |
|---|---|---|---|---|---|---|
| $f_{TA}$ | Timer_A input clock frequency | Internal: SMCLK<br>External: TACLK<br>Duty cycle = 50% ±10% | 1.2 V 12 | | | MHz |
| | | | 1.4 V 24 | | | |
| $t_{TA,cap}$ | Timer_A capture timing | All capture inputs,<br>Minimum pulse duration required for capture | | | 20 | ns |

表5-43列出了Timer32的特性。

**Table 5-43. Timer32**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数测试条件VCORE VCC MIN MAX单元 | | | | | | |
|---|---|---|---|---|---|---|
| $f_{T32}$ | Timer32 operating clock frequency(1) | | 1.2 V | | 24 | MHz |
| | | | 1.4 V 48 | | | |

（1）Timer32与Cortex-M4 CPU在同一时钟运行。

## 5.25.11记忆

表5-44列出了闪存的一般特性。

**Table 5-44. Flash Memory**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| DVCCPGM / ERS用于编程或擦除的电源电压1.62 3.7 V. | | | | |
| IPGM / ERS，PEAK编程期间来自DVCC的峰值电源电流或擦除10 mA | | | | |
| $N_{Endurance}$ | Program or erase endurance(1) | 20000 | | cycles |
| $t_{Retention}$ | Data retention duration | 20 | | years |

（1）位的编程或擦除周期定义为位从1变为0到1的位。

表5-45列出了使用MSP432外设驱动程序库的闪存操作的特性。

表5-45。使用MSP432外设驱动程序库的闪存操作（1）

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数测试条件MIN TYP MAX UNIT | | | | | |
|---|---|---|---|---|---|
| $t_{PGM\_API,\ Word}$ | Program time for 32-bit data using ROM_FlashCtl_programMemory() API | VCORE = 1.4 V, MCLK = 48 MHz | 40 | 275 | µs |
| $t_{PGM\_API,\ Sector}$ | 使用ROM_FlashCtl_programMemory（）API编程4KB数据（一个扇区）的时间 | VCORE = 1.4 V, MCLK = 48 MHz | 4.5 | 71 | ms |
| $t_{ERS\_API,\ Sector}$ | Sector erase time using ROM_FlashCtl_eraseSector() API | VCORE = 1.4 V, MCLK = 48 MHz, Number of erase or program cycles <1k | 9 | 309(2) | ms |
| | | VCORE = 1.4 V, MCLK = 48 MHz, Number of erase or program cycles >1k and <20k | 9 | 3035(2) | |
| $t_{ERS\_API,\ Mass-Erase}$ | Mass erase time using ROM_FlashCtl_performMassErase() API | VCORE = 1.4 V, MCLK = 48 MHz, Number of erase or program cycles <1k, MSP432P401R devices with 256KB of flash memory | 12 | 19800(3) | ms |
| | | VCORE = 1.4 V, MCLK = 48 MHz, Number of erase or program cycles <1k, MSP432P401M devices with 128KB of flash memory | 12 | 9900(3) | ms |
| $I_{AVGPGM\_API}$ | Average supply current from DVCC during program using ROM_FlashCtl_programMemory() API | VCORE = 1.2 V, MCLK = 3 MHz | 5 | 7 | mA |
| $I_{AVGERS\_API}$ | Average supply current from DVCC during erase using ROM_FlashCtl_eraseSector() API | VCORE = 1.2 V, MCLK = 3 MHz | 2 | 3 | mA |

（1）从ROM执行的MSP432外设驱动程序库。

（2）理论上，通过将典型值乘以NMAX_ERS来计算特定擦除或程序耐久性的最大值。

（3）理论上，通过将特定擦除或程序耐久性的典型值乘以NMAX_ERS和闪存主存储器中的扇区总数来计算最大值。

表5-46列出了闪存独立操作的特性。

**Table 5-46. Flash Stand-Alone Operations**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数测试条件MIN TYP MAX UNIT | | | | | |
|---|---|---|---|---|---|
| $t_{PGM, Immediate}$ | Program time for one 32-bit data using immediate write mode | VER_PRE = 0, VER_PST = 1 | 40 | | µs |
| | | VER_PRE = 1, VER_PST = 1 | 60 | | |
| $t_{PGM, Full-word}$ | Program time for one 128-bit word using full word write mode | VER_PRE = 0, VER_PST = 1 | 40 | | µs |
| | | VER_PRE = 1, VER_PST = 1 | 60 | | |
| $t_{PGM, Burst}$ | Program time for 4×128-bit burst using burst write mode | AUTO_PRE = 0, AUTO_PST = 1 | 65 | | µs |
| | | AUTO_PRE = 1, AUTO_PST = 1 | 85 | | |
| $t_{ERS}$ | Time for sector erase or mass erase | | 9 | | ms |
| $N_{MAX\_PGM}$ | Maximum number of pulses to complete program operation | | 5 | | |
| $N_{MAX\_ERS}$ | Maximum number of pulses to complete erase operation | Number of erase or program cycles <1k | 34 | | |
| | | Number of erase or program cycles >1k and <20k | 334 | | |

表5-47列出了SRAM的特性。

**Table 5-47. SRAM**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| 参数测试条件MIN TYP MAX UNIT | | | | | |
|---|---|---|---|---|---|
| ISRAM_EN启用时，一个SRAM bank的电流消耗 | | VCORE = 1.2 V | 100 | 3500 | nA |
| | | VCORE = 1.4 V | 300 | 5500 | |
| ISRAM_RET保留时的一个SRAM bank的电流消耗 | | VCORE = 1.2 V | 30 | 1250 | nA |
| | | VCORE = 1.4 V | 35 | 1200 | |
| $t_{SRAM\_EN, one}$ | Time taken to enable one SRAM bank | | 4 | 5 | µs |
| $t_{SRAM\_DIS, one}$ | Time taken to disable one SRAM bank | | 4 | 5 | µs |
| $t_{SRAM\_EN, all}$ | Time taken to enable all SRAM banks except Bank 0 | | 7 | 8 | µs |
| $t_{SRAM\_DIS, all}$ | Time taken to disable all SRAM banks except Bank 0 | | 4 | 5 | µs |

## 5.25.12仿真和调试

表5-48列出了JTAG接口的特性。

**Table 5-48. JTAG**

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{TCK}$ | TCK clock frequency | 0 | | 10 | MHz |
| $t_{TCK}$ | TCK clock period | 100 | | | ns |
| $t_{TCK\_LOW}$ | TCK clock low time | | $t_{TCK}/2$ | | ns |
| $t_{TCK\_HIGH}$ | TCK clock high time | | $t_{TCK}/2$ | | ns |
| $t_{TCK\_RISE}$ | TCK rise time | 0 | | 10 | ns |
| $t_{TCK\_FALL}$ | TCK fall time | 0 | | 10 | ns |
| $t_{TMS\_SU}$ | TMS setup time to TCK rise | 30 | | | ns |
| $t_{TMS\_HLD}$ | TMS hold time from TCK rise | 9 | | | ns |
| $t_{TDI\_SU}$ | TDI setup time to TCK rise | 20 | | | ns |
| $t_{TDI\_HLD}$ | TDI hold time from TCK rise | 7 | | | ns |
| $t_{TDO\_ZDV}$ | TCK fall to data valid from high impedance | | 9 | 44 | ns |
| $t_{TDO\_DV}$ | TCK fall to data valid from data valid | | 9 | 44 | ns |
| $t_{TDO\_DVZ}$ | TCK fall to high impedance from data valid | | 8 | 38 | ns |

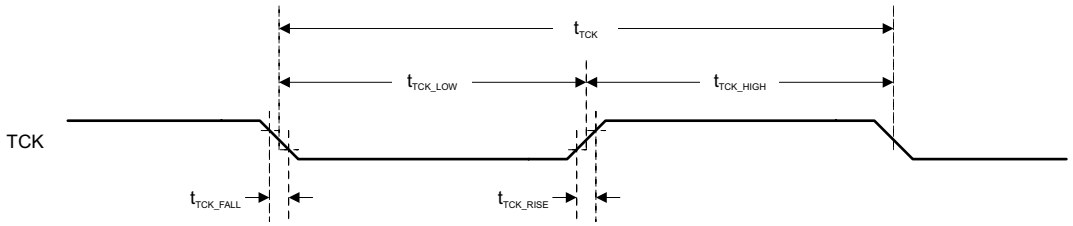



图5-74。 JTAG测试时钟输入时序

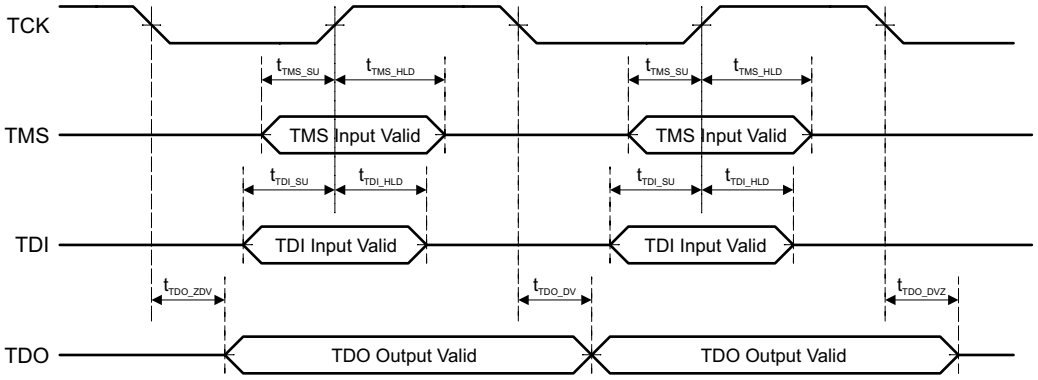



图5-75。 JTAG测试访问端口（TAP）时序

# 6详细说明

## 6.1概述

MSP432P401x微控制器是TI MSP430低功耗DNA，高级混合信号功能以及ARM 32位Cortex-M4 RISC引擎处理能力的理想组合。微控制器附带了捆绑的驱动程序库，并与ARM生态系统的标准组件兼容。

## 6.2处理器和执行功能

Cortex-M4处理器提供高性能低成本平台，可满足最小内存实现，减少引脚数和低功耗的系统要求，同时提供出色的计算性能和对中断的出色系统响应。
Thumb®-2混合16位和32位处理器指令集可提供32位ARM内核所需的高性能，其内存尺寸通常与8位和16位器件相关（通常在微控制器级应用程序所需的几千字节内存范围。

在MSP432P401x MCU中，Cortex-M4处理器可以运行高达48 MHz，为目标应用类别提供高性能，同时保持超低有源功耗。

### 6.2.1浮点单元

MSP432P401x MCU上的Cortex-M4处理器包括一个紧耦合浮点单元（FPU）。
FPU是符合IEEE
754标准的单精度浮点模块，支持加，减，乘，除，累加和平方根运算。它还提供定点和浮点数据格式与浮点常量指令之间的转换。

### 6.2.2记忆保护单元

MSP432P401x
MCU上的Cortex-M4处理器包括一个紧耦合的存储器保护单元（MPU），最多可支持八个保护区域。应用程序可以使用MPU来强制执行内存权限规则，这些规则可以将进程彼此隔离或强制执行内存访问规则。这些功能通常是操作系统处理目的所必需的。

### 6.2.3嵌套向量中断控制器（NVIC）

NVIC支持多达64个中断，具有8级中断优先级。 Cortex-M4
NVIC架构允许低延迟，高效的中断和事件处理，以及与设备级功率控制策略的无缝集成。

### 6.2.4 SysTick

Cortex-M4包括一个集成系统定时器SysTick，它提供一个简单的24位，清除写入，递减，零包装计数器和灵活的控制机制。计数器可以以多种不同的方式使用，并且通常用于操作系统相关目的或作为通用警报机制。

### 6.2.5调试和跟踪功能

Cortex-M4处理器实现了完整的硬件调试解决方案，通过传统的4引脚JTAG端口或2引脚串行线调试（SWD）端口提供处理器和存储器的高系统可视性，这是微控制器和其他产品的理想选择。小包装设备。
SWJ-DP接口将SWD和JTAG调试端口组合到一个模块中，可根据应用需求在2引脚和4引脚工作模式之间进行无缝切换。

对于系统跟踪，处理器集成了仪表跟踪宏单元（ITM）以及数据监视点和分析单元。为了实现简单且经济高效的系统跟踪事件分析，串行线查看器（SWV）可以通过单个引脚导出软件生成的消息流，数据跟踪和分析信息。

**NOTE**

有关Cortex-M4
CPU的程序员模型以及第6.2节中提到的相关外设的详细规范和信息，请参阅www.arm.com上的相应参考手册。

## 6.3存储器映射

该设备支持4GB地址空间，分为8个512MB区域（见图6-1）。

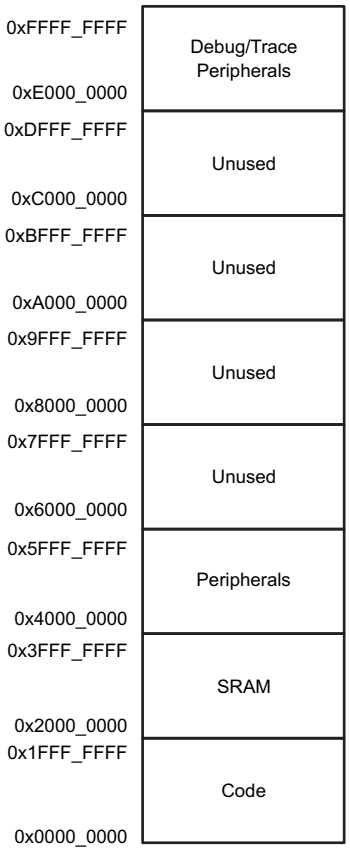



**Figure 6-1. Device Memory Zones**

### 6.3.1码区存储器映射

从0x0000_0000到0x1FFF_FFFF的区域被定义为Code区域，可通过Cortex-M4处理器的ICODE和DCODE总线以及系统DMA访问。该区域映射闪存，ROM和内部SRAM（允许从SRAM进行最佳的单周期执行）。

图6-2显示了Code区域的MSP432P401x特定存储器映射，对用户代码可见。

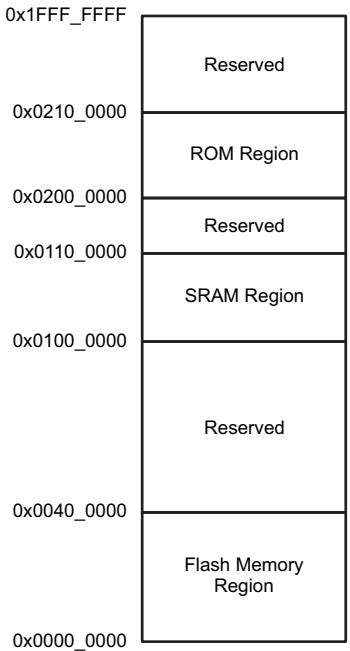



**Figure 6-2. Code Zone Memory Map**

### 6.3.1.1闪存区域

从0x0000_0000到0x003F_FFFF的4MB区域被定义为闪存区域。该区域进一步划分为不同类型的闪存区域，详见6.4.1节。

### 6.3.1.2 SRAM区域

从0x0100_0000到0x010F_FFFF的1MB区域被定义为SRAM区域。该区域也在器件的SRAM区域中别名，从而允许有效访问SRAM，用于指令读取和数据读取。更多详细信息，请参见第6.4.2节。

### 6.3.1.3 ROM区域

从0x0200_0000到0x020F_FFFF的1MB区域被定义为ROM区域。有关ROM的详细信息，请参见第6.4.3节。

## 6.3.2 SRAM区域存储器映射

器件的SRAM区位于0x2000_0000到0x3FFF_FFFF的地址范围内。图6-3显示了该区域的划分方式。

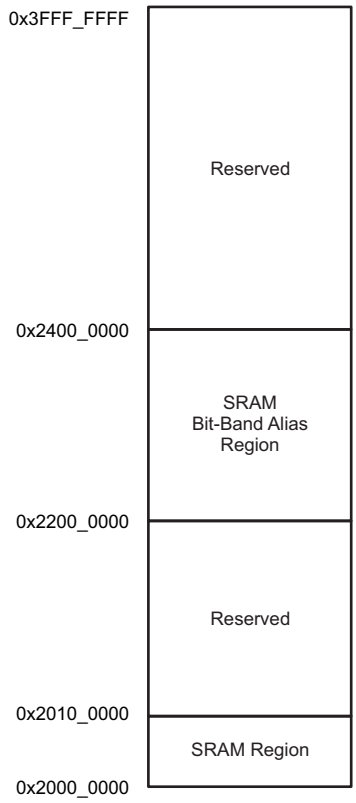



**Figure 6-3. SRAM Zone Memory Map**

### 6.3.2.1 SRAM区域

从0x2000_0000到0x200F_FFFF的1MB区域被定义为SRAM区域。在该区域中可访问的SRAM也在器件的代码区中别名，从而允许有效访问SRAM，用于指令提取和数据读取。有关SRAM的详细信息，请参见第6.4.2节。

### 6.3.2.2 SRAM位带别名区域

从0x2200_0000到0x23FF_FFFF的32MB区域形成1-MB SRAM区域的位带别名区域。位带是Cortex-M4处理器的一项功能，允许应用程序在整个SRAM空间中设置或清除各个位，而无需使用处理器的流水线带宽来执行独占的读 - 修改 - 写序列。

## 6.3.3外围区域存储器映射

器件的外围区域位于0x4000_0000到0x5FFF_FFFF的地址范围内。图6-4显示了该范围如何进一步划分。

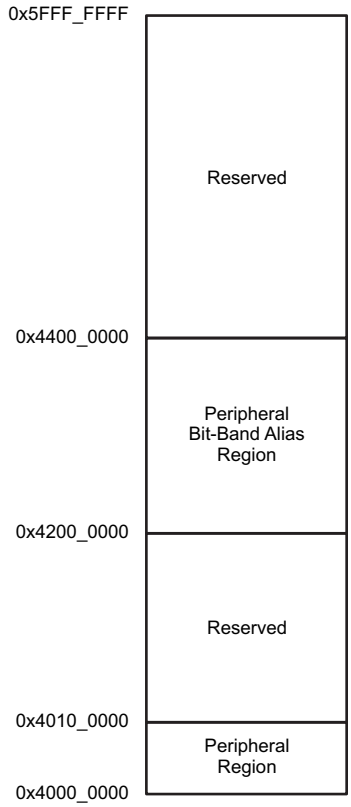



**Figure 6-4. Peripheral Zone Memory Map**

### 6.3.3.1 周边区域

从0x4000_0000到0x400F_FFFF的1MB区域专用于系统和应用程序控制设备的外围设备。在MSP432P401x MCU上，该区域共有128KB专用于外设，其余则保留。表6-1列出了此128 KB空间内的外设分配。

请注意，所有外围设备可能并非在该系列的所有设备中都可用（详情请参阅REMARKS列）。如果某个外设被列为特定设备的N / A，则将相应的地址空间视为保留。

**NOTE**

标记为16位的外设应通过字节或半字大小读或写来访问。对这些外设的任何32位访问都会导致总线错误响应。

**Table 6-1. Peripheral Address Offsets**

| ADDRESS RANGE | PERIPHERAL | TABLE | REMARKS |
|---|---|---|---|
| 0x4000_0000–0x4000_03FF | Timer_A0 | Table 6-2 | 16-bit peripheral |
| 0x4000_0400–0x4000_07FF | Timer_A1 | Table 6-3 | 16-bit peripheral |
| 0x4000_0800–0x4000_0BFF | Timer_A2 | Table 6-4 | 16-bit peripheral |
| 0x4000_0C00–0x4000_0FFF | Timer_A3 | Table 6-5 | 16-bit peripheral |
| 0x4000_1000–0x4000_13FF | eUSCI_A0 | Table 6-6 | 16-bit peripheral |
| 0x4000_1400–0x4000_17FF | eUSCI_A1 | Table 6-7 | 16-bit peripheral |
| 0x4000_1800–0x4000_1BFF | eUSCI_A2 | Table 6-8 | 16-bit peripheral |
| 0x4000_1C00–0x4000_1FFF | eUSCI_A3 | Table 6-9 | 16-bit peripheral |
| 0x4000_2000–0x4000_23FF | eUSCI_B0 | Table 6-10 | 16-bit peripheral |
| 0x4000_2400–0x4000_27FF | eUSCI_B1 | Table 6-11 | 16-bit peripheral |

表6-1。外设地址偏移（续）

| ADDRESS RANGE | PERIPHERAL | TABLE | REMARKS |
|---|---|---|---|
| 0x4000_2800–0x4000_2BFF | eUSCI_B2 | Table 6-12 | 16-bit peripheral |
| 0x4000_2C00–0x4000_2FFF | eUSCI_B3 | Table 6-13 | 16-bit peripheral |
| 0x4000_3000–0x4000_33FF | REF_A | Table 6-14 | 16-bit peripheral |
| 0x4000_3400–0x4000_37FF | COMP_E0 | Table 6-15 | 16-bit peripheral |
| 0x4000_3800–0x4000_3BFF | COMP_E1 | Table 6-16 | 16-bit peripheral |
| 0x4000_3C00–0x4000_3FFF | AES256 | Table 6-17 | 16-bit peripheral |
| 0x4000_4000–0x4000_43FF | CRC32 | Table 6-18 | 16-bit peripheral |
| 0x4000_4400–0x4000_47FF | RTC_C | Table 6-19 | 16-bit peripheral |
| 0x4000_4800–0x4000_4BFF | WDT_A | Table 6-20 | 16-bit peripheral |
| 0x4000_4C00–0x4000_4FFF | Port Module | Table 6-21 | 16-bit peripheral |
| 0x4000_5000–0x4000_53FF | Port Mapping Controller | Table 6-22 | 16-bit peripheral |
| 0x4000_5400–0x4000_57FF | Capacitive Touch I/O 0 | Table 6-23 | 16-bit peripheral |
| 0x4000_5800–0x4000_5BFF | Capacitive Touch I/O 1 | Table 6-24 | 16-bit peripheral |
| 0x4000_5C00–0x4000_8FFF | Reserved | | Read only, always reads 0h |
| 0x4000_9000–0x4000_BFFF | Reserved | | Read only, always reads 0h |
| 0x4000_C000–0x4000_CFFF | Timer32 | Table 6-25 | |
| 0x4000_D000–0x4000_DFFF | Reserved | | Read only, always reads 0h |
| 0x4000_E000–0x4000_FFFF | DMA | Table 6-26 | |
| 0x4001_0000–0x4001_03FF | PCM | Table 6-27 | |
| 0x4001_0400–0x4001_07FF | CS | Table 6-28 | |
| 0x4001_0800–0x4001_0FFF | PSS | Table 6-29 | |
| 0x4001_1000–0x4001_17FF | FLCTL | Table 6-30 | |
| 0x4001_1800–0x4001_1BFF | Reserved | | Read only, always reads 0h |
| 0x4001_1C00–0x4001_1FFF | Reserved | | Read only, always reads 0h |
| 0x4001_2000–0x4001_23FF | ADC14 | Table 6-31 | |
| 0x4001_2400–0x4001_FFFF | Reserved | | Read only, always reads 0h |

表6-2。 Timer_A0寄存器（基址：0x4000_0000）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| Timer_A0 Control | TA0CTL | 00h |
| Timer_A0捕捉/比较控制0 TA0CCTL0 02h | | |
| Timer_A0捕捉/比较控制1 TA0CCTL1 04h | | |
| Timer_A0捕捉/比较控制2 TA0CCTL2 06h | | |
| Timer_A0捕捉/比较控制3 TA0CCTL3 08h | | |
| Timer_A0捕捉/比较控制4 TA0CCTL4 0Ah | | |
| Timer_A0 Counter | TA0R | 10h |
| Timer_A0 Capture/Compare 0 | TA0CCR0 | 12h |
| Timer_A0 Capture/Compare 1 | TA0CCR1 | 14h |
| Timer_A0 Capture/Compare 2 | TA0CCR2 | 16h |
| Timer_A0 Capture/Compare 3 | TA0CCR3 | 18h |
| Timer_A0 Capture/Compare 4 | TA0CCR4 | 1Ah |
| Timer_A0 Interrupt Vector | TA0IV | 2Eh |
| Timer_A0 Expansion 0 | TA0EX0 | 20h |

表6-3。 Timer_A1寄存器（基址：0x4000_0400）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| Timer_A1 Control | TA1CTL | 00h |
| Timer_A1捕捉/比较控制0 TA1CCTL0 02h | | |
| Timer_A1捕捉/比较控制1 TA1CCTL1 04h | | |
| Timer_A1捕捉/比较控制2 TA1CCTL2 06h | | |
| Timer_A1捕捉/比较控制3 TA1CCTL3 08h | | |
| Timer_A1捕捉/比较控制4 TA1CCTL4 0Ah | | |
| Timer_A1 Counter | TA1R | 10h |
| Timer_A1 Capture/Compare 0 | TA1CCR0 | 12h |
| Timer_A1 Capture/Compare 1 | TA1CCR1 | 14h |
| Timer_A1 Capture/Compare 2 | TA1CCR2 | 16h |
| Timer_A1 Capture/Compare 3 | TA1CCR3 | 18h |
| Timer_A1 Capture/Compare 4 | TA1CCR4 | 1Ah |
| Timer_A1 Interrupt Vector | TA1IV | 2Eh |
| Timer_A1 Expansion 0 | TA1EX0 | 20h |

表6-4。 Timer_A2寄存器（基址：0x4000_0800）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| Timer_A2 Control | TA2CTL | 00h |
| Timer_A2捕捉/比较控制0 TA2CCTL0 02h | | |
| Timer_A2捕捉/比较控制1 TA2CCTL1 04h | | |
| Timer_A2捕捉/比较控制2 TA2CCTL2 06h | | |
| Timer_A2捕捉/比较控制3 TA2CCTL3 08h | | |
| Timer_A2捕捉/比较控制4 TA2CCTL4 0Ah | | |
| Timer_A2 Counter | TA2R | 10h |
| Timer_A2 Capture/Compare 0 | TA2CCR0 | 12h |
| Timer_A2 Capture/Compare 1 | TA2CCR1 | 14h |
| Timer_A2 Capture/Compare 2 | TA2CCR2 | 16h |
| Timer_A2 Capture/Compare 3 | TA2CCR3 | 18h |
| Timer_A2 Capture/Compare 4 | TA2CCR4 | 1Ah |
| Timer_A2 Interrupt Vector | TA2IV | 2Eh |
| Timer_A2 Expansion 0 | TA2EX0 | 20h |

表6-5。 Timer_A3寄存器（基址：0x4000_0C00）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| Timer_A3 Control | TA3CTL | 00h |
| Timer_A3捕捉/比较控制0 TA3CCTL0 02h | | |
| Timer_A3捕捉/比较控制1 TA3CCTL1 04h | | |
| Timer_A3捕捉/比较控制2 TA3CCTL2 06h | | |
| Timer_A3捕捉/比较控制3 TA3CCTL3 08h | | |
| Timer_A3捕捉/比较控制4 TA3CCTL4 0Ah | | |
| Timer_A3 Counter | TA3R | 10h |
| Timer_A3 Capture/Compare 0 | TA3CCR0 | 12h |
| Timer_A3 Capture/Compare 1 | TA3CCR1 | 14h |
| Timer_A3 Capture/Compare 2 | TA3CCR2 | 16h |
| Timer_A3 Capture/Compare 3 | TA3CCR3 | 18h |
| Timer_A3 Capture/Compare 4 | TA3CCR4 | 1Ah |
| Timer_A3 Interrupt Vector | TA3IV | 2Eh |

表6-5。 Timer_A3寄存器（基址：0x4000_0C00）（续）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| Timer_A3 Expansion 0 | TA3EX0 | 20h |

表6-6。 eUSCI_A0寄存器（基址：0x4000_1000）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| eUSCI_A0 Control Word 0 | UCA0CTLW0 | 00h |
| eUSCI_A0 Control Word 1 | UCA0CTLW1 | 02h |
| eUSCI_A0 Baud Rate Control | UCA0BRW | 06h |
| eUSCI_A0 Modulation Control | UCA0MCTLW | 08h |
| eUSCI_A0 Status | UCA0STATW | 0Ah |
| eUSCI_A0 Receive Buffer | UCA0RXBUF | 0Ch |
| eUSCI_A0 Transmit Buffer | UCA0TXBUF | 0Eh |
| eUSCI_A0 Auto Baud Rate Control | UCA0ABCTL | 10h |
| eUSCI_A0 IrDA Control | UCA0IRCTL | 12h |
| eUSCI_A0 Interrupt Enable | UCA0IE | 1Ah |
| eUSCI_A0 Interrupt Flag | UCA0IFG | 1Ch |
| eUSCI_A0 Interrupt Vector | UCA0IV | 1Eh |

表6-7。 eUSCI_A1寄存器（基地址：0x4000_1400）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| eUSCI_A1 Control Word 0 | UCA1CTLW0 | 00h |
| eUSCI_A1 Control Word 1 | UCA1CTLW1 | 02h |
| eUSCI_A1 Baud Rate Control | UCA1BRW | 06h |
| eUSCI_A1 Modulation Control | UCA1MCTLW | 08h |
| eUSCI_A1 Status | UCA1STATW | 0Ah |
| eUSCI_A1 Receive Buffer | UCA1RXBUF | 0Ch |
| eUSCI_A1 Transmit Buffer | UCA1TXBUF | 0Eh |
| eUSCI_A1 Auto Baud Rate Control | UCA1ABCTL | 10h |
| eUSCI_A1 IrDA Control | UCA1IRCTL | 12h |
| eUSCI_A1 Interrupt Enable | UCA1IE | 1Ah |
| eUSCI_A1 Interrupt Flag | UCA1IFG | 1Ch |
| eUSCI_A1 Interrupt Vector | UCA1IV | 1Eh |

表6-8。 eUSCI_A2寄存器（基地址：0x4000_1800）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| eUSCI_A2 Control Word 0 | UCA2CTLW0 | 00h |
| eUSCI_A2 Control Word 1 | UCA2CTLW1 | 02h |
| eUSCI_A2 Baud Rate Control | UCA2BRW | 06h |
| eUSCI_A2 Modulation Control | UCA2MCTLW | 08h |
| eUSCI_A2 Status | UCA2STATW | 0Ah |
| eUSCI_A2 Receive Buffer | UCA2RXBUF | 0Ch |
| eUSCI_A2 Transmit Buffer | UCA2TXBUF | 0Eh |
| eUSCI_A2 Auto Baud Rate Control | UCA2ABCTL | 10h |
| eUSCI_A2 IrDA Control | UCA2IRCTL | 12h |
| eUSCI_A2 Interrupt Enable | UCA2IE | 1Ah |
| eUSCI_A2 Interrupt Flag | UCA2IFG | 1Ch |
| eUSCI_A2 Interrupt Vector | UCA2IV | 1Eh |

表6-9。 eUSCI_A3寄存器（基址：0x4000_1C00）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| eUSCI_A3 Control Word 0 | UCA3CTLW0 | 00h |
| eUSCI_A3 Control Word 1 | UCA3CTLW1 | 02h |
| eUSCI_A3 Baud Rate Control | UCA3BRW | 06h |
| eUSCI_A3 Modulation Control | UCA3MCTLW | 08h |
| eUSCI_A3 Status | UCA3STATW | 0Ah |
| eUSCI_A3 Receive Buffer | UCA3RXBUF | 0Ch |
| eUSCI_A3 Transmit Buffer | UCA3TXBUF | 0Eh |
| eUSCI_A3 Auto Baud Rate Control | UCA3ABCTL | 10h |
| eUSCI_A3 IrDA Control | UCA3IRCTL | 12h |
| eUSCI_A3 Interrupt Enable | UCA3IE | 1Ah |
| eUSCI_A3 Interrupt Flag | UCA3IFG | 1Ch |
| eUSCI_A3 Interrupt Vector | UCA3IV | 1Eh |

表6-10。 eUSCI_B0寄存器（基地址：0x4000_2000）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| eUSCI_B0 Control Word 0 | UCB0CTLW0 | 00h |
| eUSCI_B0 Control Word 1 | UCB0CTLW1 | 02h |
| eUSCI_B0 Bit Rate Control Word | UCB0BRW | 06h |
| eUSCI_B0 Status Word | UCB0STATW | 08h |
| eUSCI_B0 Byte Counter Threshold | UCB0TBCNT | 0Ah |
| eUSCI_B0 Receive Buffer | UCB0RXBUF | 0Ch |
| eUSCI_B0 Transmit Buffer | UCB0TXBUF | 0Eh |
| eUSCI_B0 I2C Own Address 0 | UCB0I2COA0 | 14h |
| eUSCI_B0 I2C Own Address 1 | UCB0I2COA1 | 16h |
| eUSCI_B0 I2C Own Address 2 | UCB0I2COA2 | 18h |
| eUSCI_B0 I2C Own Address 3 | UCB0I2COA3 | 1Ah |
| eUSCI_B0 Received Address | UCB0ADDRX | 1Ch |
| eUSCI_B0 Address Mask | UCB0ADDMASK | 1Eh |
| eUSCI_B0 I2C Slave Address | UCB0I2CSA | 20h |
| eUSCI_B0 Interrupt Enable | UCB0IE | 2Ah |
| eUSCI_B0 Interrupt Flag | UCB0IFG | 2Ch |
| eUSCI_B0 Interrupt Vector | UCB0IV | 2Eh |

表6-11。 eUSCI_B1寄存器（基地址：0x4000_2400）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| eUSCI_B1 Control Word 0 | UCB1CTLW0 | 00h |
| eUSCI_B1 Control Word 1 | UCB1CTLW1 | 02h |
| eUSCI_B1 Bit Rate Control Word | UCB1BRW | 06h |
| eUSCI_B1 Status Word | UCB1STATW | 08h |
| eUSCI_B1 Byte Counter Threshold | UCB1TBCNT | 0Ah |
| eUSCI_B1 Receive Buffer | UCB1RXBUF | 0Ch |
| eUSCI_B1 Transmit Buffer | UCB1TXBUF | 0Eh |
| eUSCI_B1 I2C Own Address 0 | UCB1I2COA0 | 14h |
| eUSCI_B1 I2C Own Address 1 | UCB1I2COA1 | 16h |
| eUSCI_B1 I2C Own Address 2 | UCB1I2COA2 | 18h |
| eUSCI_B1 I2C Own Address 3 | UCB1I2COA3 | 1Ah |
| eUSCI_B1 Received Address | UCB1ADDRX | 1Ch |

表6-11。 eUSCI_B1寄存器（基地址：0x4000_2400）（续）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| eUSCI_B1 Address Mask | UCB1ADDMASK | 1Eh |
| eUSCI_B1 I2C Slave Address | UCB1I2CSA | 20h |
| eUSCI_B1 Interrupt Enable | UCB1IE | 2Ah |
| eUSCI_B1 Interrupt Flag | UCB1IFG | 2Ch |
| eUSCI_B1 Interrupt Vector | UCB1IV | 2Eh |

表6-12。 eUSCI_B2寄存器（基地址：0x4000_2800）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| eUSCI_B2 Control Word 0 | UCB2CTLW0 | 00h |
| eUSCI_B2 Control Word 1 | UCB2CTLW1 | 02h |
| eUSCI_B2 Bit Rate Control Word | UCB2BRW | 06h |
| eUSCI_B2 Status Word | UCB2STATW | 08h |
| eUSCI_B2 Byte Counter Threshold | UCB2TBCNT | 0Ah |
| eUSCI_B2 Receive Buffer | UCB2RXBUF | 0Ch |
| eUSCI_B2 Transmit Buffer | UCB2TXBUF | 0Eh |
| eUSCI_B2 I2C Own Address 0 | UCB2I2COA0 | 14h |
| eUSCI_B2 I2C Own Address 1 | UCB2I2COA1 | 16h |
| eUSCI_B2 I2C Own Address 2 | UCB2I2COA2 | 18h |
| eUSCI_B2 I2C Own Address 3 | UCB2I2COA3 | 1Ah |
| eUSCI_B2 Received Address | UCB2ADDRX | 1Ch |
| eUSCI_B2 Address Mask | UCB2ADDMASK | 1Eh |
| eUSCI_B2 I2C Slave Address | UCB2I2CSA | 20h |
| eUSCI_B2 Interrupt Enable | UCB2IE | 2Ah |
| eUSCI_B2 Interrupt Flag | UCB2IFG | 2Ch |
| eUSCI_B2 Interrupt Vector | UCB2IV | 2Eh |

表6-13。 eUSCI_B3寄存器（基地址：0x4000_2C00）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| eUSCI_B3 Control Word 0 | UCB3CTLW0 | 00h |
| eUSCI_B3 Control Word 1 | UCB3CTLW1 | 02h |
| eUSCI_B3 Bit Rate Control Word | UCB3BRW | 06h |
| eUSCI_B3 Status Word | UCB3STATW | 08h |
| eUSCI_B3 Byte Counter Threshold | UCB3TBCNT | 0Ah |
| eUSCI_B3 Receive Buffer | UCB3RXBUF | 0Ch |
| eUSCI_B3 Transmit Buffer | UCB3TXBUF | 0Eh |
| eUSCI_B3 I2C Own Address 0 | UCB3I2COA0 | 14h |
| eUSCI_B3 I2C Own Address 1 | UCB3I2COA1 | 16h |
| eUSCI_B3 I2C Own Address 2 | UCB3I2COA2 | 18h |
| eUSCI_B3 I2C Own Address 3 | UCB3I2COA3 | 1Ah |
| eUSCI_B3 Received Address | UCB3ADDRX | 1Ch |
| eUSCI_B3 Address Mask | UCB3ADDMASK | 1Eh |
| eUSCI_B3 I2C Slave Address | UCB3I2CSA | 20h |
| eUSCI_B3 Interrupt Enable | UCB3IE | 2Ah |
| eUSCI_B3 Interrupt Flag | UCB3IFG | 2Ch |
| eUSCI_B3 Interrupt Vector | UCB3IV | 2Eh |

表6-14。 REF_A寄存器（基址：0x4000_3000）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| REF_A Control 0 | REFCTL0 | 00h |

表6-15。 COMP_E0寄存器（基址：0x4000_3400）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| Comparator_E0 Control 0 | CE0CTL0 | 00h |
| Comparator_E0 Control 1 | CE0CTL1 | 02h |
| Comparator_E0 Control 2 | CE0CTL2 | 04h |
| Comparator_E0 Control 3 | CE0CTL3 | 06h |
| Comparator_E0 Interrupt | CE0INT | 0Ch |
| Comparator_E0中断向量字CE0IV 0Eh | | |

表6-16。 COMP_E1寄存器（基址：0x4000_3800）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| Comparator_E1 Control 0 | CE1CTL0 | 00h |
| Comparator_E1 Control 1 | CE1CTL1 | 02h |
| Comparator_E1 Control 2 | CE1CTL2 | 04h |
| Comparator_E1 Control 3 | CE1CTL3 | 06h |
| Comparator_E1 Interrupt | CE1INT | 0Ch |
| Comparator_E1中断向量字CE1IV 0Eh | | |

表6-17。 AES256寄存器（基址：0x4000_3C00）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| AES Accelerator Control 0 | AESACTL0 | 00h |
| AES Accelerator Control 1 | AESACTL1 | 02h |
| AES Accelerator Status | AESASTAT | 04h |
| AES Accelerator Key | AESAKEY | 06h |
| AES Accelerator Data In | AESADIN | 08h |
| AES Accelerator Data Out | AESADOUT | 0Ah |
| AES加速器在AESAXDIN 0Ch中进行异或数据 | | |
| AES加速器异或数据输入（无触发）AESAXIN 0Eh | | |

表6-18。 CRC32寄存器（基址：0x4000_4000）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| CRC32 Data Input Low | CRC32DI | 000h |
| CRC32 Data In Reverse Low | CRC32DIRB | 004h |
| CRC32初始化和结果低CRC32INIRES_LO 008h | | |
| CRC32初始化和结果高CRC32INIRES_HI 00Ah | | |
| CRC32结果反向低CRC32RESR_LO 00Ch | | |
| CRC32结果反转高CRC32RESR_HI 00Eh | | |
| CRC16 Data Input Low | CRC16DI | 010h |
| CRC16 Data In Reverse Low | CRC16DIRB | 014h |
| CRC16初始化和结果CRC16INIRES 018h | | |
| CRC16 Result Reverse | CRC16RESR | 01Eh |

表6-19。 RTC_C寄存器（基址：0x4000_4400）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| Real-Time Clock Control 0 | RTCCTL0 | 00h |
| 实时时钟控制1,3 RTCCTL13 02h | | |
| 实时时钟偏移校准RTCOCAL 04h | | |
| 实时时钟温度补偿RTCTCMP 06h | | |
| 实时预分频定时器0控制RTCPS0CTL 08h | | |
| 实时预分频定时器1控制RTCPS1CTL 0Ah | | |
| 实时预分频定时器0,1计数器RTCPS 0Ch | | |
| 实时时钟中断向量RTCIV 0Eh | | |
| 实时时钟秒，分钟RTCTIM0 10h | | |
| 实时时钟小时，星期几RTCTIM1 12h | | |
| Real-Time Clock Date | RTCDATE | 14h |
| Real-Time Clock Year | RTCYEAR | 16h |
| 实时时钟分钟，小时报警RTCAMINHR 18h | | |
| 实时时钟星期几，月份报警RTCADOWDAY 1Ah | | |
| Binary-to-BCD Conversion | RTCBIN2BCD | 1Ch |
| BCD-to-Binary Conversion | RTCBCD2BIN | 1Eh |

表6-20。 WDT_A寄存器（基址：0x4000_4800）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| Watchdog Timer Control | WDTCTL | 0Ch |

表6-21。端口寄存器（基址：0x4000_4C00）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| Port 1 Input | P1IN | 000h |
| Port 2 Input | P2IN | 001h |
| Port 1 Output | P1OUT | 002h |
| Port 2 Output | P2OUT | 003h |
| Port 1 Direction | P1DIR | 004h |
| Port 2 Direction | P2DIR | 005h |
| Port 1 Resistor Enable | P1REN | 006h |
| Port 2 Resistor Enable | P2REN | 007h |
| Port 2 Drive Strength | P2DS | 009h |
| Port 1 Select 0 | P1SEL0 | 00Ah |
| Port 2 Select 0 | P2SEL0 | 00Bh |
| Port 1 Select 1 | P1SEL1 | 00Ch |
| Port 2 Select 1 | P2SEL1 | 00Dh |
| Port 1 Interrupt Vector | P1IV | 00Eh |
| Port 1 Complement Selection | P1SELC | 016h |
| Port 2 Complement Selection | P2SELC | 017h |
| Port 1 Interrupt Edge Select | P1IES | 018h |
| Port 2 Interrupt Edge Select | P2IES | 019h |
| Port 1 Interrupt Enable | P1IE | 01Ah |
| Port 2 Interrupt Enable | P2IE | 01Bh |
| Port 1 Interrupt Flag | P1IFG | 01Ch |
| Port 2 Interrupt Flag | P2IFG | 01Dh |
| Port 2 Interrupt Vector | P2IV | 01Eh |
| Port 3 Input | P3IN | 020h |

表6-21。端口寄存器（基址：0x4000_4C00）（续）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| Port 4 Input | P4IN | 021h |
| Port 3 Output | P3OUT | 022h |
| Port 4 Output | P4OUT | 023h |
| Port 3 Direction | P3DIR | 024h |
| Port 4 Direction | P4DIR | 025h |
| Port 3 Resistor Enable | P3REN | 026h |
| Port 4 Resistor Enable | P4REN | 027h |
| Port 3 Select 0 | P3SEL0 | 02Ah |
| Port 4 Select 0 | P4SEL0 | 02Bh |
| Port 3 Select 1 | P3SEL1 | 02Ch |
| Port 4 Select 1 | P4SEL1 | 02Dh |
| Port 3 Interrupt Vector | P3IV | 02Eh |
| Port 3 Complement Selection | P3SELC | 036h |
| Port 4 Complement Selection | P4SELC | 037h |
| Port 3 Interrupt Edge Select | P3IES | 038h |
| Port 4 Interrupt Edge Select | P4IES | 039h |
| Port 3 Interrupt Enable | P3IE | 03Ah |
| Port 4 Interrupt Enable | P4IE | 03Bh |
| Port 3 Interrupt Flag | P3IFG | 03Ch |
| Port 4 Interrupt Flag | P4IFG | 03Dh |
| Port 4 Interrupt Vector | P4IV | 03Eh |
| Port 5 Input | P5IN | 040h |
| Port 6 Input | P6IN | 041h |
| Port 5 Output | P5OUT | 042h |
| Port 6 Output | P6OUT | 043h |
| Port 5 Direction | P5DIR | 044h |
| Port 6 Direction | P6DIR | 045h |
| Port 5 Resistor Enable | P5REN | 046h |
| Port 6 Resistor Enable | P6REN | 047h |
| Port 5 Select 0 | P5SEL0 | 04Ah |
| Port 6 Select 0 | P6SEL0 | 04Bh |
| Port 5 Select 1 | P5SEL1 | 04Ch |
| Port 6 Select 1 | P6SEL1 | 04Dh |
| Port 5 Interrupt Vector | P5IV | 04Eh |
| Port 5 Complement Selection | P5SELC | 056h |
| Port 6 Complement Selection | P6SELC | 057h |
| Port 5 Interrupt Edge Select | P5IES | 058h |
| Port 6 Interrupt Edge Select | P6IES | 059h |
| Port 5 Interrupt Enable | P5IE | 05Ah |
| Port 6 Interrupt Enable | P6IE | 05Bh |
| Port 5 Interrupt Flag | P5IFG | 05Ch |
| Port 6 Interrupt Flag | P6IFG | 05Dh |
| Port 6 Interrupt Vector | P6IV | 05Eh |
| Port 7 Input | P7IN | 060h |
| Port 8 Input | P8IN | 061h |
| Port 7 Output | P7OUT | 062h |
| Port 8 Output | P8OUT | 063h |

表6-21。端口寄存器（基址：0x4000_4C00）（续）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| Port 7 Direction | P7DIR | 064h |
| Port 8 Direction | P8DIR | 065h |
| Port 7 Resistor Enable | P7REN | 066h |
| Port 8 Resistor Enable | P8REN | 067h |
| Port 7 Select 0 | P7SEL0 | 06Ah |
| Port 8 Select 0 | P8SEL0 | 06Bh |
| Port 7 Select 1 | P7SEL1 | 06Ch |
| Port 8 Select 1 | P8SEL1 | 06Dh |
| Port 7 Interrupt Vector | P7IV | 06Eh |
| Port 7 Complement Selection | P7SELC | 076h |
| Port 8 Complement Selection | P8SELC | 077h |
| Port 7 Interrupt Edge Select | P7IES | 078h |
| Port 8 Interrupt Edge Select | P8IES | 079h |
| Port 7 Interrupt Enable | P7IE | 07Ah |
| Port 8 Interrupt Enable | P8IE | 07Bh |
| Port 7 Interrupt Flag | P7IFG | 07Ch |
| Port 8 Interrupt Flag | P8IFG | 07Dh |
| Port 8 Interrupt Vector | P8IV | 07Eh |
| Port 9 Input | P9IN | 080h |
| Port 10 Input | P10IN | 081h |
| Port 9 Output | P9OUT | 082h |
| Port 10 Output | P10OUT | 083h |
| Port 9 Direction | P9DIR | 084h |
| Port 10 Direction | P10DIR | 085h |
| Port 9 Resistor Enable | P9REN | 086h |
| Port 10 Resistor Enable | P10REN | 087h |
| Port 9 Select 0 | P9SEL0 | 08Ah |
| Port 10 Select 0 | P10SEL0 | 08Bh |
| Port 9 Select 1 | P9SEL1 | 08Ch |
| Port 10 Select 1 | P10SEL1 | 08Dh |
| Port 9 Interrupt Vector | P9IV | 08Eh |
| Port 9 Complement Selection | P9SELC | 096h |
| 端口10补码选择P10SELC 097h | | |
| Port 9 Interrupt Edge Select | P9IES | 098h |
| 端口10中断边沿选择P10IES 099h | | |
| Port 9 Interrupt Enable | P9IE | 09Ah |
| Port 10 Interrupt Enable | P10IE | 09Bh |
| Port 9 Interrupt Flag | P9IFG | 09Ch |
| Port 10 Interrupt Flag | P10IFG | 09Dh |
| Port 10 Interrupt Vector | P10IV | 09Eh |
| Port J Input | PJIN | 120h |
| Port J Output | PJOUT | 122h |
| Port J Direction | PJDIR | 124h |
| Port J Resistor Enable | PJREN | 126h |
| Port J Select 0 | PJSEL0 | 12Ah |
| Port J Select 1 | PJSEL1 | 12Ch |
| Port J Complement Select | PJSELC | 136h |

表6-22。 PMAP寄存器（基址：0x4000_5000）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| Port Mapping Key | PMAPKEYID | 00h |
| Port Mapping Control | PMAPCTL | 02h |
| Port Mapping P2.0 | P2MAP0 | 10h |
| Port Mapping P2.1 | P2MAP1 | 11h |
| Port Mapping P2.2 | P2MAP2 | 12h |
| Port Mapping P2.3 | P2MAP3 | 13h |
| Port Mapping P2.4 | P2MAP4 | 14h |
| Port Mapping P2.5 | P2MAP5 | 15h |
| Port Mapping P2.6 | P2MAP6 | 16h |
| Port Mapping P2.7 | P2MAP7 | 17h |
| Port Mapping P3.0 | P3MAP0 | 18h |
| Port Mapping P3.1 | P3MAP1 | 19h |
| Port Mapping P3.2 | P3MAP2 | 1Ah |
| Port Mapping P3.3 | P3MAP3 | 1Bh |
| Port Mapping P3.4 | P3MAP4 | 1Ch |
| Port Mapping P3.5 | P3MAP5 | 1Dh |
| Port Mapping P3.6 | P3MAP6 | 1Eh |
| Port Mapping P3.7 | P3MAP7 | 1Fh |
| Port Mapping P7.0 | P7MAP0 | 38h |
| Port Mapping P7.1 | P7MAP1 | 39h |
| Port Mapping P7.2 | P7MAP2 | 3Ah |
| Port Mapping P7.3 | P7MAP3 | 3Bh |
| Port Mapping P7.4 | P7MAP4 | 3Ch |
| Port Mapping P7.5 | P7MAP5 | 3Dh |
| Port Mapping P7.6 | P7MAP6 | 3Eh |
| Port Mapping P7.7 | P7MAP7 | 3Fh |

表6-23。电容触摸I / O 0寄存器（基址：0x4000_5400）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| 电容触摸I / O 0控制CAPTIO0CTL 0Eh | | |

表6-24。电容触摸I / O 1寄存器（基址：0x4000_5800）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| 电容触摸I / O 1控制CAPTIO1CTL 0Eh | | |

表6-25。 Timer32寄存器（基址：0x4000_C000）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| Timer 1 Load | T32LOAD1 | 00h |
| Timer 1 Current Value | T32VALUE1 | 04h |
| Timer 1 Timer Control | T32CONTROL1 | 08h |
| Timer 1 Interrupt Clear | T32INTCLR1 | 0Ch |
| Timer 1 Raw Interrupt Status | T32RIS1 | 10h |
| Timer 1 Interrupt Status | T32MIS1 | 14h |
| Timer 1 Background Load | T32BGLOAD1 | 18h |
| Timer 2 Load | T32LOAD2 | 20h |
| Timer 2 Current Value | T32VALUE2 | 24h |

表6-25。 Timer32寄存器（基址：0x4000_C000）（续）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| Timer 2 Timer Control | T32CONTROL2 | 28h |
| Timer 2 Interrupt Clear | T32INTCLR2 | 2Ch |
| Timer 2 Raw Interrupt Status | T32RIS2 | 30h |
| Timer 2 Interrupt Status | T32MIS2 | 34h |
| Timer 2 Background Load | T32BGLOAD2 | 38h |

表6-26。 DMA寄存器（基址：0x4000_E000）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| 设备配置状态DMA_DEVICE_CFG_000h | | |
| 软件通道触发DMA_SW_CHTRIG_004h | | |
| 通道0源配置DMA_CH0_SRCCFG_010h | | |
| 通道1源配置DMA_CH1_SRCCFG_014h | | |
| 通道2源配置DMA_CH2_SRCCFG_018h | | |
| 通道3源配置DMA_CH3_SRCCFG_01Ch | | |
| 通道4源配置DMA_CH4_SRCCFG_020h | | |
| 通道5源配置DMA_CH5_SRCCFG_024h | | |
| 通道6源配置DMA_CH6_SRCCFG_028h | | |
| 通道7源配置DMA_CH7_SRCCFG_02Ch | | |
| 中断1源通道配置DMA_INT1_SRCCFG_100h | | |
| 中断2源通道配置DMA_INT2_SRCCFG_104h | | |
| 中断3源通道配置DMA_INT3_SRCCFG_108h | | |
| 中断0源通道标志DMA_INT0_SRCFLG_110h | | |
| 中断0源通道清除标志DMA_INT0_CLRFLG_114h | | |
| Status | DMA_STAT | 1000h |
| Configuration | DMA_CFG | 1004h |
| 通道控制数据库指针DMA_CTLBASE_1008h | | |
| 通道备用控制数据库指针DMA_ALTBASE_100Ch | | |
| 通道等待请求状态DMA_WAITSTAT_1010h | | |
| Channel Software Request | DMA_SWREQ | 1014h |
| Channel_Useburst设置DMA_USEBURSTSET_1018h | | |
| Channel_Useburst清除DMA_USEBURSTCLR_101Ch | | |
| 通道请求掩码设置DMA_REQMASKSET_1020h | | |
| 通道请求掩码清除DMA_REQMASKCLR_1024h | | |
| Channel Enable Set | DMA_ENASET | 1028h |
| Channel Enable Clear | DMA_ENACLR | 102Ch |
| 通道主备用集DMA_ALTSET_1030h | | |
| Channel_Primary-Alternate_Clear_DMA_ALTCLR_1034h | | |
| Channel Priority Set | DMA_PRIOSET | 1038h |
| Channel Priority Clear | DMA_PRIOCLR | 103Ch |
| Bus Error Clear | DMA_ERRCLR | 104Ch |

表6-27。 PCM寄存器（基址：0x4001_0000）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| Control 0 | PCMCTL0 | 00h |
| Control 1 | PCMCTL1 | 04h |
| Interrupt Enable | PCMIE | 08h |
| Interrupt Flag | PCMIFG | 0Ch |

表6-27。 PCM寄存器（基址：0x4001_0000）（续）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| Clear Interrupt Flag | PCMCLRIFG | 10h |

表6-28。 CS寄存器（基址：0x4001_0400）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| Key | CSKEY | 00h |
| Control 0 | CSCTL0 | 04h |
| Control 1 | CSCTL1 | 08h |
| Control 2 | CSCTL2 | 0Ch |
| Control 3 | CSCTL3 | 10h |
| Clock Enable | CSCLKEN | 30h |
| Status | CSSTAT | 34h |
| Interrupt Enable | CSIE | 40h |
| Interrupt Flag | CSIFG | 48h |
| Clear Interrupt Flag | CSCLRIFG | 50h |
| Set Interrupt Flag | CSSETIFG | 58h |
| DCO外部电阻校准0 CSDCOERCAL0 60h | | |
| DCO外部电阻校准1 CSDCOERCAL1 64h | | |

表6-29。 PSS寄存器（基地址：0x4001_0800）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| Key | PSSKEY | 00h |
| Control 0 | PSSCTL0 | 04h |
| Interrupt Enable | PSSIE | 34h |
| Interrupt Flag | PSSIFG | 38h |
| Clear Interrupt Flag | PSSCLRIFG | 3Ch |

表6-30。 FLCTL寄存器（基址：0x4001_1000）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| Power Status | FLCTL_POWER_STAT | 000h |
| Bank 0读取控制FLCTL_BANK0_RDCTL 010h | | |
| Bank 1读取控制FLCTL_BANK1_RDCTL 014h | | |
| 读取突发/比较控制和状态FLCTL_RDBRST_CTLSTAT 020h | | |
| 读取突发/比较起始地址FLCTL_RDBRST_STARTADDR 024h | | |
| 读取突发/比较长度FLCTL_RDBRST_LEN 028h | | |
| 读取突发/比较失败地址FLCTL_RDBRST_FAILADDR 03Ch | | |
| 读取突发/比较失败计数FLCTL_RDBRST_FAILCNT 040h | | |
| 程序控制和状态FLCTL_PRG_CTLSTAT 050h | | |
| 程序突发控制和状态FLCTL_PRGBRST_CTLSTAT 054h | | |
| 程序突发起始地址FLCTL_PRGBRST_STARTADDR 058h | | |
| 程序突发数据0_0 FLCTL_PRGBRST_DATA0_0 060h | | |
| 程序突发数据0_1 FLCTL_PRGBRST_DATA0_1 064h | | |
| 程序突发数据0_2 FLCTL_PRGBRST_DATA0_2 068h | | |
| 程序突发数据0_3 FLCTL_PRGBRST_DATA0_3 06Ch | | |
| 程序突发数据1_0 FLCTL_PRGBRST_DATA1_0 070h | | |
| 程序突发数据1_1 FLCTL_PRGBRST_DATA1_1 074h | | |
| 程序突发数据1_2 FLCTL_PRGBRST_DATA1_2 078h | | |

表6-30。 FLCTL寄存器（基址：0x4001_1000）（续）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| 程序突发数据1_3 FLCTL_PRGBRST_DATA1_3 07Ch | | |
| 程序突发数据2_0 FLCTL_PRGBRST_DATA2_0 080h | | |
| 程序突发数据2_1 FLCTL_PRGBRST_DATA2_1 084h | | |
| 程序突发数据2_2 FLCTL_PRGBRST_DATA2_2 088h | | |
| 程序突发数据2_3 FLCTL_PRGBRST_DATA2_3 08Ch | | |
| 程序突发数据3_0 FLCTL_PRGBRST_DATA3_0 090h | | |
| 程序突发数据3_1 FLCTL_PRGBRST_DATA3_1 094h | | |
| 程序突发数据3_2 FLCTL_PRGBRST_DATA3_2 098h | | |
| 程序突发数据3_3 FLCTL_PRGBRST_DATA3_3 09Ch | | |
| 擦除控制和状态FLCTL_ERASE_CTLSTAT 0A0h | | |
| 擦除扇区地址FLCTL_ERASE_SECTADDR 0A4h | | |
| 信息存储区0写/擦除保护FLCTL_BANK0_INFO_WEPROT 0B0h | | |
| 主存储器组0写/擦除保护FLCTL_BANK0_MAIN_WEPROT 0B4h | | |
| 信息存储区1写/擦除保护FLCTL_BANK1_INFO_WEPROT 0C0h | | |
| 主存储器组1写/擦除保护FLCTL_BANK1_MAIN_WEPROT 0C4h | | |
| 基准控制和状态FLCTL_BMRK_CTLSTAT 0D0h | | |
| 基准指令获取计数FLCTL_BMRK_IFETCH 0D4h | | |
| 基准数据读取计数FLCTL_BMRK_DREAD 0D8h | | |
| 基准计数比较FLCTL_BMRK_CMP 0DCh | | |
| Interrupt Flag | FLCTL_IFG | 0F0h |
| Interrupt Enable | FLCTL_IE | 0F4h |
| Clear Interrupt Flag | FLCTL_CLRIFG | 0F8h |
| Set Interrupt Flag | FLCTL_SETIFG | 0FCh |
| 读取时序控制FLCTL_READ_TIMCTL 100h | | |
| 读保证金计时控制FLCTL_READMARGIN_TIMCTL 104h | | |
| 程序验证时序控制FLCTL_PRGVER_TIMCTL 108h | | |
| 擦除验证时序控制FLCTL_ERSVER_TIMCTL 10Ch | | |
| 程序时序控制FLCTL_PROGRAM_TIMCTL 114h | | |
| 擦除时序控制FLCTL_ERASE_TIMCTL 118h | | |
| 质量擦除定时控制FLCTL_MASSERASE_TIMCTL 11Ch | | |
| 突发程序时序控制FLCTL_BURSTPRG_TIMCTL 120h | | |

表6-31。 ADC14寄存器（基址：0x4001_2000）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| Control 0 | ADC14CTL0 | 00h |
| Control 1 | ADC14CTL1 | 04h |
| 窗口比较器低阈值0 ADC14LO0 08h | | |
| 窗口比较器高阈值0 ADC14HI0 0Ch | | |
| 窗口比较器低阈值1 ADC14LO1 10h | | |
| 窗口比较器高阈值1 ADC14HI1 14h | | |
| Memory Control 0 | ADC14MCTL0 | 18h |
| Memory Control 1 | ADC14MCTL1 | 1Ch |
| Memory Control 2 | ADC14MCTL2 | 20h |
| Memory Control 3 | ADC14MCTL3 | 24h |
| Memory Control 4 | ADC14MCTL4 | 28h |
| Memory Control 5 | ADC14MCTL5 | 2Ch |
| Memory Control 6 | ADC14MCTL6 | 30h |

表6-31。 ADC14寄存器（基址：0x4001_2000）（续）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| Memory Control 7 | ADC14MCTL7 | 34h |
| Memory Control 8 | ADC14MCTL8 | 38h |
| Memory Control 9 | ADC14MCTL9 | 3Ch |
| Memory Control 10 | ADC14MCTL10 | 40h |
| Memory Control 11 | ADC14MCTL11 | 44h |
| Memory Control 12 | ADC14MCTL12 | 48h |
| Memory Control 13 | ADC14MCTL13 | 4Ch |
| Memory Control 14 | ADC14MCTL14 | 50h |
| Memory Control 15 | ADC14MCTL15 | 54h |
| Memory Control 16 | ADC14MCTL16 | 58h |
| Memory Control 17 | ADC14MCTL17 | 5Ch |
| Memory Control 18 | ADC14MCTL18 | 60h |
| Memory Control 19 | ADC14MCTL19 | 64h |
| Memory Control 20 | ADC14MCTL20 | 68h |
| Memory Control 21 | ADC14MCTL21 | 6Ch |
| Memory Control 22 | ADC14MCTL22 | 70h |
| Memory Control 23 | ADC14MCTL23 | 74h |
| Memory Control 24 | ADC14MCTL24 | 78h |
| Memory Control 25 | ADC14MCTL25 | 7Ch |
| Memory Control 26 | ADC14MCTL26 | 80h |
| Memory Control 27 | ADC14MCTL27 | 84h |
| Memory Control 28 | ADC14MCTL28 | 88h |
| Memory Control 29 | ADC14MCTL29 | 8Ch |
| Memory Control 30 | ADC14MCTL30 | 90h |
| Memory Control 31 | ADC14MCTL31 | 94h |
| Memory 0 | ADC14MEM0 | 98h |
| Memory 1 | ADC14MEM1 | 9Ch |
| Memory 2 | ADC14MEM2 | A0h |
| Memory 3 | ADC14MEM3 | A4h |
| Memory 4 | ADC14MEM4 | A8h |
| Memory 5 | ADC14MEM5 | ACh |
| Memory 6 | ADC14MEM6 | B0h |
| Memory 7 | ADC14MEM7 | B4h |
| Memory 8 | ADC14MEM8 | B8h |
| Memory 9 | ADC14MEM9 | BCh |
| Memory 10 | ADC14MEM10 | C0h |
| Memory 11 | ADC14MEM11 | C4h |
| Memory 12 | ADC14MEM12 | C8h |
| Memory 13 | ADC14MEM13 | CCh |
| Memory 14 | ADC14MEM14 | D0h |
| Memory 15 | ADC14MEM15 | D4h |
| Memory 16 | ADC14MEM16 | D8h |
| Memory 17 | ADC14MEM17 | DCh |
| Memory 18 | ADC14MEM18 | E0h |
| Memory 19 | ADC14MEM19 | E4h |
| Memory 20 | ADC14MEM20 | E8h |
| Memory 21 | ADC14MEM21 | ECh |

表6-31。 ADC14寄存器（基址：0x4001_2000）（续）

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| Memory 22 | ADC14MEM22 | F0h |
| Memory 23 | ADC14MEM23 | F4h |
| Memory 24 | ADC14MEM24 | F8h |
| Memory 25 | ADC14MEM25 | FCh |
| Memory 26 | ADC14MEM26 | 100 |
| Memory 27 | ADC14MEM27 | 104 |
| Memory 28 | ADC14MEM28 | 108 |
| Memory 29 | ADC14MEM29 | 10C |
| Memory 30 | ADC14MEM30 | 110h |
| Memory 31 | ADC14MEM31 | 114h |
| Interrupt Enable 0 | ADC14IER0 | 13Ch |
| Interrupt Enable 1 | ADC14IER1 | 140h |
| Interrupt Flag 0 | ADC14IFGR0 | 144h |
| Interrupt Flag 1 | ADC14IFGR1 | 148h |
| 清除中断标志0 ADC14CLRIFGR0 14Ch | | |
| 清除中断标志1 ADC14CLRIFGR1 150h | | |
| Interrupt Vector | ADC14IV | 154h |

## 6.3.3.2外围位带别名区域

从0x4200_0000到0x43FF_FFFF的32MB区域形成1MB外围区域的位带别名区域。位带是Cortex-M4处理器的一项功能，允许应用程序在整个外设存储空间中设置或清除各个位，而无需使用处理器的流水线带宽来执行独占的读 - 修改 - 写序列。

**NOTE**

仅通过字节或半字访问来访问16位外设的限制也适用于这些外设的相应位带区域。换句话说，对这些外设的位带别名区域的写入必须仅以字节或半字访问的形式。

## 6.3.4调试和跟踪外围区域

该区域映射Cortex-M4的内部和外部PPB区域（见表6-32）。以下外围设备映射到此区域：

- Core and System debug control registers (internal PPB)
- NVIC and other registers in the System Control space of the Cortex-M4 (internal PPB)
- FPB, DWT, ITM (internal PPB)
- TPIU, Debug ROM table (external PPB)
- Reset Controller (external PPB)
- System Controller (external PPB)

**Table 6-32. Debug Zone Memory Map**

| 地址范围 | 模块或外围 | 备注 |
|---|---|---|
| 0xE000_0000–0xE000_0FFF | ITM | Internal PPB |
| 0xE000_1000–0xE000_1FFF | DWT | Internal PPB |
| 0xE000_2000–0xE000_2FFF | FPB | Internal PPB |
| 0xE000_3000–0xE000_DFFF | Reserved | Internal PPB |
| 0xE000_E000–0xE000_EFFF | Cortex-M4 System Control Space | Internal PPB |
| 0xE000_F000–0xE003_FFFF | Reserved | Internal PPB |
| 0xE004_0000–0xE004_0FFF | TPIU | External PPB |
| 0xE004_1000–0xE004_1FFF | Reserved | External PPB |
| 0xE004_2000–0xE004_23FF | Reset Controller (see Table 6-33) | External PPB |
| 0xE004_2400–0xE004_2FFF | Reserved | External PPB |
| 0xE004_3000–0xE004_33FF | System Controller (see Table 6-34) | External PPB |
| 0xE004_3400–0xE004_3FFF | Reserved | External PPB |
| 0xE004_4000–0xE004_43FF | System Controller | External PPB |
| 0xE004_4400–0xE00F_EFFF | Reserved | External PPB |
| 0xE00F_F000–0xE00F_FFFF | ROM Table (External PPB) | External PPB |
| 0xE010_0000–0xFFFF_FFFF | Reserved | Vendor Space |

**NOTE**

有关表6-32中列出的ARM模块的地址映射，请参阅www.arm.com上的Cortex-M4技术参考手册。

**Table 6-33. RSTCTL Registers**

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| Reset Request | RSTCTL_RESET_REQ | 000h |
| 硬复位状态RSTCTL_HARDRESET_STAT | | 004h |
| 硬复位状态清除RSTCTL_HARDRESET_CLR | | 008h |
| 硬复位状态设置RSTCTL_HARDRESET_SET | | 00Ch |
| 软复位状态RSTCTL_SOFTRESET_STAT | | 010h |
| 软复位状态清除RSTCTL_SOFTRESET_CLR | | 014h |
| 软复位状态设置RSTCTL_SOFTRESET_SET | | 018h |
| PSS复位状态RSTCTL_PSSRESET_STAT | | 100h |
| PSS复位状态清除RSTCTL_PSSRESET_CLR | | 104h |
| PCM复位状态RSTCTL_PCMRESET_STAT | | 108h |
| PCM复位状态清除RSTCTL_PCMRESET_CLR | | 10Ch |
| 引脚复位状态RSTCTL_PINRESET_STAT | | 110h |

**Table 6-33. RSTCTL Registers (continued)**

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| 引脚复位状态清除RSTCTL_PINRESET_CLR_114h | | |
| 重新启动重置状态RSTCTL_REBOOTRESET_STAT_118h | | |
| 重新启动重置状态清除RSTCTL_REBOOTRESET_CLR_11Ch | | |
| CS Reset Status | RSTCTL_CSRESET_STAT | 120h |
| CS复位状态清除RSTCTL_CSRESET_CLR_124h | | |

**Table 6-34. SYSCTL Registers**

| REGISTER NAME | ACRONYM | OFFSET |
|---|---|---|
| Reboot Control | SYS_REBOOT_CTL | 0000h |
| NMI控制和状态SYS_NMI_CTLSTAT_0004h | | |
| 看门狗复位控制SYS_WDTRESET_CTL_0008h | | |
| 外围停止控制SYS_PERIHALT_CTL_000Ch | | |
| SRAM Size | SYS_SRAM_SIZE | 0010h |
| SRAM Bank Enable | SYS_SRAM_BANKEN | 0014h |
| SRAM存储区保留控制SYS_SRAM_BANKRET_0018h | | |
| Flash Size | SYS_FLASH_SIZE | 0020h |
| 数字I / O毛刺滤波器控制SYS_DIO_GLTFLT_CTL_0030h | | |
| IP保护的安全区数据访问解锁SYS_SECDATA_UNLOCK_0040h | | |
| Master Unlock | SYS_MASTER_UNLOCK | 1000h |
| 引导覆盖请求0 SYS_BOOTOVER_REQ0_1004h | | |
| 引导覆盖请求1 SYS_BOOTOVER_REQ1_1008h | | |
| Boot Override Acknowledge SYS_BOOTOVER_ACK_100Ch | | |
| Reset Request | SYS_RESET_REQ | 1010h |
| 复位状态并覆盖SYS_RESET_STATOVER_1014h | | |
| System Status | SYS_SYSTEM_STAT | 1020h |

## 6.4 MSP432P401x的存储器

MSP432P401x
MCU包括用于一般应用目的的闪存和SRAM。此外，这些器件还包括一个备用存储器（总可用SRAM的一部分），它以低功耗模式保留。

### 6.4.1闪存

MSP432P401x
MCU包括一个高耐用性低功耗闪存，支持最多20000次写入或擦除周期。闪存是128位宽，从而通过每次提取返回最多4个32位指令（或最多8个16位指令）来实现高代码执行性能。闪存进一步分为两种类型的子区域：主存储器和信息存储器。

从物理角度来看，闪存包括两个存储体，主存储区和信息存储区在两个存储体之间平均分配。这允许应用程序从一个存储体执行同时读取或执行操作，而另一个存储体可能正在进行编程或擦除操作。

图6-5显示了MSP432P401x MCU上闪存的存储器映射。

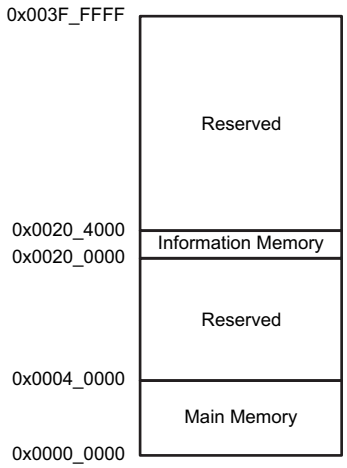



**Figure 6-5. Flash Memory Map**

### 6.4.1.1闪存主存储器（0x0000_0000至0x0003_FFFF）

MSP432P401x
MCU上的闪存主存储器最高可达256KB。闪存主存储器由最多64个扇区组成，每个扇区4KB，最小擦除粒度为4KB（1扇区）。主存储器可以被视为两个独立的相同存储体，每个存储体最多128KB，允许从一个存储体同时读取或执行，而另一个存储体正在进行编程或擦除操作。

### 6.4.1.2闪存信息存储器（0x0020_0000至0x0020_3FFF）

闪存信息存储区域为16KB。闪存信息存储器由四个扇区组成，每个扇区4KB，最小擦除粒度为4KB（1扇区）。表6-35描述了闪存信息存储器的不同区域和每个区域的内容。包含设备描述符（TLV）的闪存信息存储区域在工厂配置用于防止写入和擦除操作。

表6-35。闪存信息存储区域

| REGION | ADDRESS RANGE | CONTENTS | WRITE AND ERASE PROTECTED? |
|---|---|---|---|
| Bank 0, Sector 0 | 0x0020_0000-0x0020_0FFF | Flash Boot-override Mailbox | No. |
| Bank 0, Sector 1 | 0x0020_1000-0x0020_1FFF | 设备描述符（TLV） | 是 |
| Bank 1, Sector 0 | 0x0020_2000-0x0020_2FFF | TI BSL | No |
| Bank 1, Sector 1 | 0x0020_3000-0x0020_3FFF | TI BSL | No |

### 6.4.1.3闪存操作

闪存提供应用程序可以部署的多种读取和编程操作模式。
在单个编程操作中，最多可以编程128位（存储器字宽）（从1设置为0）。

虽然CPU数据总线是32位宽，但闪存可以在启动闪存编程之前缓冲128位写入数据，从而使软件一次编程大块数据更加无缝和高效。此外，闪存还支持突发写入模式，与单独编程字相比，该模式花费的时间更少。有关时序参数的信息，请参阅。

闪存主区和信息存储区以扇区粒度提供写/擦保护控制，以使软件能够优化诸如大块擦除之类的操作，同时保护闪存的某些区域。在低功耗工作模式下，闪存被禁用并进入断电状态以最大限度地减少泄漏。

有关闪存及其各种操作和配置模式的详细信息，请参阅“MSP432P4xx SimpleLink™微控制器技术参考手册”中的闪存控制器（FLCTL）章节。

**NOTE**

根据CPU（MCLK）频率和使用的活动模式，可能需要使用单个/多个等待状态访问闪存。只要工作频率需要更改，应用程序就有责任确保在频率变化生效之前正确配置闪存访问等待状态。有关闪存等待状态要求的详细信息，请参阅电气规范。

### 6.4.2 SRAM

MSP432P401x MCU支持高达64KB的SRAM，其余的1MB SRAM区域保留。

SRAM在代码区和SRAM区都有别名。这使得能够从SRAM快速单周期执行代码，因为Cortex-M4处理器将指令提取管道传输到代码空间以外的存储区。与闪存一样，SRAM可以在低功耗工作模式下断电或置于低泄漏保持状态。

图6-6显示了MSP432P401x MCU上SRAM的存储器映射。

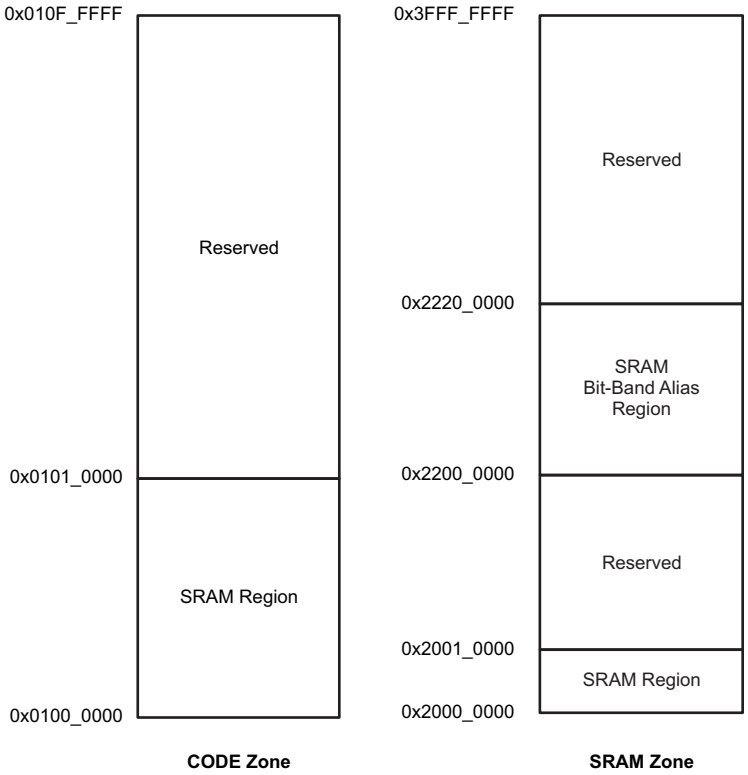



**Figure 6-6. SRAM Map**

#### 6.4.2.1 SRAM Bank使能配置

该应用程序可以优化SRAM的功耗。为此，SRAM分为8 KB存储区，可单独关断。断电的组在有功和低功率工作模式下都保持断电状态，从而在器件在有源和基于保持的低功耗模式之间转换时限制任何不必要的浪涌电流。应用程序还可以在处理中的某个阶段禁用一个（或多个）存储体，并将其启用到另一个阶段。

禁用特定存储区时，对其地址空间的读取将返回0h，并且将丢弃写入。为了防止存储器映射中的“漏洞”，如果启用了特定存储区，则所有较低存储区也被强制为启用状态。这确保了通过一组启用的存储体的连续存储器映射，而不是允许禁用的存储体出现在启用的存储体之间。例如：

- 如果设备中有8个库，则可以接受00111111和00000111的值。
- 00010111之类的值无效，结果库配置自动设置为00011111。
- 例如，对于4存储区SRAM，唯一允许的值为0001,0011,0111和1111。

SRAM的Bank 0始终处于使能状态，无法禁用。对于所有其他存储区，任何启用或禁用更改都会导致SYS_SRAM_BANKEN寄存器的SRAM_RDY位设置为0，直到配置更改生效。在此期间，对SRAM的任何访问都会停止，只有在SRAM存储区准备好进行读或写操作后才能恢复访问。这是透明处理的，不需要任何代码干预。有关SRAM bank启用或禁用延迟，请参阅电气规范中的SRAM特性。

### 6.4.2.2 SRAM Bank保留配置和备份存储器

该应用可以优化LPM3和LPM4工作模式下SRAM的漏电功耗。要启用此功能，可以单独配置每个SRAM bank以进行保留。启用保留的银行将通过LPM3和LPM4模式保留其数据。应用程序还可以保留已启用的银行的子集。

例如，应用程序可能需要32KB的SRAM来满足其处理需求（四个存储区保持启用状态）。但是，在这四个存储体中，只有一个存储体可能包含必须保留在LPM3或LPM4中的关键数据，而其余存储体完全断电以最小化功耗。

SRAM的Bank 0始终保留，无法关闭。因此，它还可以作为LPM3，LPM4和LPM3.5操作模式中的可能备份存储器运行。在LPM3和LPM4模式的情况下，保留了完整的8KB SRAM bank 0，但在LPM3.5模式的情况下，仅保留6KB的SRAM bank 0。在LPM3.5模式下，地址范围0x2000_0000到0x2000_007FF之间的2KB SRAM bank 0不会保留。

## 6.4.3 ROM

MSP432P401x MCU支持32KB ROM，其余1MB区域保留（供将来升级）。
ROM的低2KB保留用于TI内部用途，对此空间的访问会返回错误响应。
ROM的其余部分用于驱动程序库。

**NOTE**

整个ROM区域返回写访问的错误响应。
ROM的低2KB总是返回任何访问的错误响应。

## 6.5 DMA

MSP432P401x MCU采用8通道ARM μDMA。这允许8个同时有效的通道用于存储器和外围设备之间的数据传输，而无需使用CPU的带宽（从而在不需要数据处理时通过空闲CPU来降低功率）。此外，DMA在多种低功耗工作模式下保持有效，允许极低功耗状态，其中数据可以低速传输。

为了获得最大的灵活性，最多八个DMA事件源可以映射到八个通道中的任何一个。这是通过DMA中的配置寄存器控制的。此外，DMA最多可以产生四个中断请求（如第6.5.2节所述）。有关DMA配置的详细信息，请参阅MSP432P4xx SimpleLink™微控制器技术参考手册中的DMA章节。

### 6.5.1 DMA源映射

八个可用通道中的每个通道都有一个控制寄存器，可以选择任何器件级DMA源作为相应通道的最终源。表6-36列出了可用于映射到每个通道的源，具体取决于源配置（SRCCFG）寄存器的值。DMA传输在所选DMA源的上升沿启动。

**Table 6-36. DMA Sources**

| | SRCCFG = 0 | SRCCFG = 1 | SRCCFG = 2 | SRCCFG = 3 | SRCCFG = 4 | SRCCFG = 5 | SRCCFG = 6 | SRCCFG = 7 |
|---|---|---|---|---|---|---|---|---|
| 通道0 | 保留 | eUSCI_A0 TX | eUSCI_B0 TX0 | eUSCI_B3 TX1 | eUSCI_B2 TX2 | eUSCI_B1 TX3 | TA0CCR0 | AES256_Trigger0 |
| 通道1 | 保留 | eUSCI_A0 RX | eUSCI_B0 RX0 | eUSCI_B3 RX1 | eUSCI_B2 RX2 | eUSCI_B1 RX3 | TA0CCR2 | AES256_Trigger1 |
| 通道2 | 保留 | eUSCI_A1 TX | eUSCI_B1 TX0 | eUSCI_B0 TX1 | eUSCI_B3 TX2 | eUSCI_B2 TX3 | TA1CCR0 | AES256_Trigger2 |
| 通道3 | 保留 | eUSCI_A1 RX | eUSCI_B1 RX0 | eUSCI_B0 RX1 | eUSCI_B3 RX2 | eUSCI_B2 RX3 | TA1CCR2 | 保留 |
| 通道4 | 保留 | eUSCI_A2 TX | eUSCI_B2 TX0 | eUSCI_B1 TX1 | eUSCI_B0 TX2 | eUSCI_B3 TX3 | TA2CCR0 | 保留 |
| 通道5 | 保留 | eUSCI_A2 RX | eUSCI_B2 RX0 | eUSCI_B1 RX1 | eUSCI_B0 RX2 | eUSCI_B3 RX3 | TA2CCR2 | 保留 |
| 通道6 | 保留 | eUSCI_A3 TX | eUSCI_B3 TX0 | eUSCI_B2 TX1 | eUSCI_B1 TX2 | eUSCI_B0 TX3 | TA3CCR0 | DMAE0 (External Pin) |
| 通道7 | 保留 | eUSCI_A3 RX | eUSCI_B3 RX0 | eUSCI_B2 RX1 | eUSCI_B1 RX2 | eUSCI_B0 RX3 | TA3CCR2 | ADC14 |

**NOTE**

任何标记为保留的源都未使用。它可用于软件控制的DMA任务，但通常在未来的设备上保留用于增强目的。

### 6.5.2 DMA完成中断

对于ARM μDMA控制器，软件通常负责维护已完成其操作的通道列表。为了提供进一步的灵活性，MSP432P401x DMA支持四个DMA完成中断，这些中断按以下方式映射：

- DMA_INT0：除已映射到DMA_INT1，DMA_INT2或DMA_INT3的所有完成事件外的所有完成事件的逻辑或。
- DMA_INT1，DMA_INT2，DMA_INT3：可以映射到八个通道中任何一个的DMA完成事件。

**NOTE**

软件必须确保将DMA_INT1，DMA_INT2和DMA_INT3映射到不同的通道，以便相同的通道不会在NVIC上产生多个中断。

### 6.5.3 DMA访问权限

DMA可以访问设备的所有存储器和外设配置接口。如果设备配置为IP保护，则对闪存的DMA访问仅限于闪存主区和信息存储区的下半部分（第二组）。这可以防止DMA被用作闪存的上半部分（第一存储体）中的未授权访问源，其中安装了安全数据区域。

## 6.6内存映射访问详细信息

MSP432P401x MCU上的总线系统包含四个主机，可以启动各种类型的事务：

- ICODE: Cortex-M4 instruction fetch bus. Accesses the Code zone only
- DCODE：Cortex-M4数据和文字加载/存储总线。仅访问代码区域。调试器访问Code区域也出现在此总线上。

•SBUS：Cortex-M4数据读写总线。仅访问代码区和PPB内存空间以外的所有区域。调试器访问此空间也会出现在此总线上。

- DMA: Access to all zones except the PPB memory space

**NOTE**

PPB空间仅专用于Cortex-M4专用外设总线。

## 6.6.1主从访问优先级设置

表6-37列出了所有可用的主服务器（行）及其对从服务器（列）的访问权限。如果多个主设备可以访问一个从设备，则表格会列出访问优先级（如果需要仲裁）。表中较小的数字表示较高的仲裁优先级（优先级始终固定）。

表6-37。主和从属访问优先级

| | FLASH MEMORY | ROM | SRAM | PERIPHERALS |
|---|---|---|---|---|
| ICODE | 3 | 2 | 4 | N/A |
| DCODE | 2 (1) | 1 | 2 | N/A |
| SBUS | N/A | N/A | 3 | 2 |
| DMA | 1 (2) | N/A | 1 (3) | 1 |

（1）如果设备在安全模式下运行，则可能会限制从DCODE到闪存的访问。

（2）如果设备在启用IP保护的安全模式下运行，则从DMA到闪存的访问仅限于Bank 1。在这种情况下，访问Bank 0会返回错误响应

（3）尽管SRAM映射到代码和系统空间，但从DMA到SRAM的访问必须仅使用系统空间。代码空间中对SRAM的DMA访问将导致总线错误。

## 6.6.2存储器映射访问响应

表6-38总结了对MSP432P401x MCU整个存储器映射的访问响应。

**Table 6-38. Memory Map Access Response**

| ADDRESS RANGE | DESCRIPTION | READ (1) | WRITE (1) | INSTRUCTION FETCH (1) |
|---|---|---|---|---|
| 0x0000_0000–0x0003_FFFF | Flash Main Memory | OK | OK (2)(3) | OK |
| 0x0004_0000–0x001F_FFFF | Reserved | Error | Error | Error |
| 0x0020_0000–0x0020_3FFF | Flash Information Memory | OK | OK (3) | OK |
| 0x0020_4000–0x00FF_FFFF | Reserved | Error | Error | Error |
| 0x0100_0000–0x0100_FFFF | SRAM | OK | OK | OK |
| 0x0101_0000–0x01FF_FFFF | Reserved | Error | Error | Error |
| 0x0200_0000–0x0200_03FF | ROM (Reserved) | Error | Error | Error |
| 0x0200_0400–0x0200_7FFF | ROM | OK | Error | OK |
| 0x0200_8000–0x1FFF_FFFF | Reserved | Error | Error | Error |
| 0x2000_0000–0x2000_FFFF | SRAM | OK | OK | OK |
| 0x2001_0000–0x21FF_FFFF | Reserved | Error | Error | Error |
| 0x2200_0000–0x23FF_FFFF | SRAM bit-band alias | OK (4) | OK | Error |
| 0x2400_0000–0x3FFF_FFFF | Reserved | Error | Error | Error |
| 0x4000_0000–0x4001_FFFF | Peripheral | OK | OK | Error |
| 0x4002_0000–0x41FF_FFFF | Reserved | Error | Error | Error |

（1）保留存储区在读取和指令提取时返回0h。写入此区域将被忽略

（2）如果用户存储器地址是安全区域的一部分，则该访问如果由未经授权的源启动则返回错误。有关更多详细信息，请参阅在MSP432P4xx上配置安全性和引导加载程序（BSL）。

（3）如果扇区启用了写保护，则忽略对该地址的写操作

（4）如果该位清零，则从位带区域读取返回00h，如果该位置位则返回01h。

表6-38。内存映射访问响应（续）

| ADDRESS RANGE | DESCRIPTION | READ (1) | WRITE (1) | INSTRUCTION FETCH (1) |
|---|---|---|---|---|
| 0x4200_0000–0x43FF_FFFF | Peripheral bit-band alias | OK (4) | OK | Error |
| 0x4400_0000–0xDFFF_FFFF | Reserved | Error | Error | Error |
| 0xE000_0000–0xE003_FFFF | Internal PPB (5) | OK | OK | Error |
| 0xE004_0000–0xE004_0FFF | TPIU (External PPB) | OK | OK | Error |
| 0xE004_1000–0xE004_1FFF | Reserved | Reserved | Reserved | Error |
| 0xE004_2000–0xE004_23FF | Reset Controller (External PPB) | OK | OK | Error |
| 0xE004_2400–0xE004_2FFF | Reserved | Reserved | Reserved | Error |
| 0xE004_3000–0xE004_33FF | SYSCTL (External PPB) | OK | OK | Error |
| 0xE004_3400–0xE004_3FFF | Reserved | Reserved | Reserved | Error |
| 0xE004_4000–0xE004_43FF | SYSCTL (External PPB) | OK | OK | Error |
| 0xE004_4400–0xE00F_EFFF | Reserved | Reserved | Reserved | Error |
| 0xE00F_F000–0xE00F_FFFF | ROM Table (External PPB) | OK | OK | Error |
| 0xE010_0000–0xFFFF_FFFF | Reserved | Error | Error | Error |

（5）有关内部PPB存储器映射的详细信息，请参阅www.arm.com上的Cortex-M4技术参考手册。

## 6.7中断

MSP432P401x

MCU上的Cortex-M4处理器实现了具有64个外部中断线和8个优先级的NVIC。从应用程序的角度来看，设备级的中断源分为两类，即NMI和用户中断。在内部，CPU异常模型以固定且可配置的优先级顺序处理各种异常（内部和外部事件，包括CPU指令，存储器和总线故障条件）。有关处理各种异常优先级（包括CPU重置和故障模型）的详细信息，请参阅www.arm.com上的ARM-V7M体系结构参考手册。

### 6.7.1 NMI

NVIC的NMI输入具有以下可能的来源：

- External NMI pin (if configured in NMI mode)
- Oscillator fault condition
- Power Supply System (PSS) generated interrupts
- Power Control Manager (PCM) generated interrupts

### 6.7.2设备级用户中断

表6-39列出了各种中断源及其与NVIC输入的连接

**NOTE**

某些源可能具有多个中断条件，在这种情况下，必须检查源的相应中断状态/标志寄存器以区分生成条件。

**Table 6-39. NVIC Interrupts**

| NVIC中断输入源 | | |
|---|---|---|
| INTISR[0] | PSS (1) | |
| INTISR[1] | CS (1) | |

（1）此源也可以映射到系统NMI。更多详细信息，请参见“MSP432P4xx SimpleLink™微控制器技术参考手册”。

**Table 6-39. NVIC Interrupts (continued)**

| NVIC中断输入源源 | | |
|---|---|---|
| INTISR[2] | PCM (1) | |
| INTISR[3] | WDT_A | |
| INTISR[4] | FPU_INT (2) | Combined interrupt from flags in the FPSCR (part of Cortex-M4 FPU) |
| INTISR［5］FLCTL闪存控制器中断标志 | | |
| INTISR［6］COMP_E0 Comparator_E0中断标志 | | |
| INTISR［7］COMP_E1 Comparator_E1中断标志 | | |
| INTISR[8] | Timer_A0 | TA0CCTL0.CCIFG |
| INTISR［9］Timer_A0 TA0CCTLx.CCIFG（x = 1到4），TA0CTL.TAIFG | | |
| INTISR[10] | Timer_A1 | TA1CCTL0.CCIFG |
| INTISR［11］Timer_A1 TA1CCTLx.CCIFG（x = 1到4），TA1CTL.TAIFG | | |
| INTISR[12] | Timer_A2 | TA2CCTL0.CCIFG |
| INTISR［13］Timer_A2 TA2CCTLx.CCIFG（x = 1到4），TA2CTL.TAIFG | | |
| INTISR[14] | Timer_A3 | TA3CCTL0.CCIFG |
| INTISR［15］Timer_A3 TA3CCTLx.CCIFG（x = 1到4），TA3CTL.TAIFG | | |
| INTISR［16］eUSCI_A0 UART或SPI模式TX，RX和状态标志 | | |
| INTISR［17］eUSCI_A1 UART或SPI模式TX，RX和状态标志 | | |
| INTISR［18］eUSCI_A2 UART或SPI模式TX，RX和状态标志 | | |
| INTISR［19］eUSCI_A3 UART或SPI模式TX，RX和状态标志 | | |
| INTISR[20] | eUSCI_B0 | SPI or $I^2C$ mode TX, RX, and Status Flags ($I^2C$ in multiple-slave mode) |
| INTISR[21] | eUSCI_B1 | SPI or $I^2C$ mode TX, RX, and Status Flags ($I^2C$ in multiple-slave mode) |
| INTISR[22] | eUSCI_B2 | SPI or $I^2C$ mode TX, RX, and Status Flags ($I^2C$ in multiple-slave mode) |
| INTISR[23] | eUSCI_B3 | SPI or $I^2C$ mode TX, RX, and Status Flags ($I^2C$ in multiple-slave mode) |
| INTISR［24］ADC14 IFG［0-31］，LO / IN / HI-IFG，RDYIFG，OVIFG，TOVIFG | | |
| INTISR［25］Timer32_INT1 Timer32的Timer32中断 | | |
| INTISR［26］Timer32_INT2 Timer32的Timer32中断 | | |
| INTISR［27］Timer32_INTC Timer32组合中断 | | |
| INTISR[28] | AES256 | AESRDYIFG |
| INTISR［29］RTC_C OFIFG，RDYIFG，TEVIFG，AIFG，RT0PSIFG，RT1PSIFG | | |
| INTISR[30] | DMA_ERR | DMA error interrupt |
| INTISR［31］DMA_INT3 DMA完成中断3 | | |
| INTISR［32］DMA_INT2 DMA完成中断2 | | |
| INTISR［33］DMA_INT1 DMA完成中断1 | | |
| INTISR[34] | DMA_INT0(3) | DMA completion interrupt0 |
| INTISR［35］I / O端口P1 P1IFG.x（x = 0到7） | | |
| INTISR［36］I / O端口P2 P2IFG.x（x = 0到7） | | |
| INTISR［37］I / O端口P3 P3IFG.x（x = 0到7） | | |
| INTISR［38］I / O端口P4 P4IFG.x（x = 0到7） | | |
| INTISR［39］I / O端口P5 P5IFG.x（x = 0到7） | | |
| INTISR［40］I / O端口P6 P6IFG.x（x = 0到7） | | |
| INTISR[41] | Reserved | |
| INTISR[42] | Reserved | |
| INTISR[43] | Reserved | |
| INTISR[44] | Reserved | |
| INTISR[45] | Reserved | |
| INTISR[46] | Reserved | |

（2）由于多个浮点异常，Cortex-M4的FPU可能会产生中断。软件负责处理和清除FPSCR中的中断标志。

（3）DMA_INT0具有与DMA_INT1，DMA_INT2或DMA_INT3不同的功能。更多详细信息，请参见第6.5.2节。

**Table 6-39. NVIC Interrupts (continued)**

| NVIC中断输入源源 | | |
|---|---|---|
| INTISR[47] | Reserved | |
| INTISR[48] | Reserved | |
| INTISR[49] | Reserved | |
| INTISR[50] | Reserved | |
| INTISR[51] | Reserved | |
| INTISR[52] | Reserved | |
| INTISR[53] | Reserved | |
| INTISR[54] | Reserved | |
| INTISR[55] | Reserved | |
| INTISR[56] | Reserved | |
| INTISR[57] | Reserved | |
| INTISR[58] | Reserved | |
| INTISR[59] | Reserved | |
| INTISR[60] | Reserved | |
| INTISR[61] | Reserved | |
| INTISR[62] | Reserved | |
| INTISR[63] | Reserved | |

**NOTE**

中断服务程序（ISR）必须确保在从ISR返回之前清除源外设中的相关中断标志。如果不这样做，即使事件已由ISR处理，相同的中断也可能被错误地再次触发为新事件。由于在外设的中断标志寄存器中执行写命令和实际写反映之间可能存在几个延迟周期，因此建议在退出ISR之前执行写操作并等待几个周期。或者，应用程序可以执行显式读取以确保在退出ISR之前清除该标志。

## 6.8系统控制

系统控制包括管理设备整体行为的模块，包括电源管理，操作模式，时钟，重置处理和用户配置设置。

### 6.8.1设备重置

MSP432P401x

MCU支持多种复位。每个类导致设备逻辑的不同启动级别，从而允许应用程序开发人员在代码开发和调试期间基于重置要求启动不同的重置。以下小节介绍了设备中的重置类别

#### 6.8.1.1电源开/关复位（POR）

POR启动应用程序设置和设备配置信息的完整初始化。

这类复位可以由PSS，PCM，RSTn引脚，DCO外部电阻器短路故障时的时钟系统或器件仿真逻辑（通过调试器）启动。从应用程序的角度来看，所有POR源都会将设备返回到相同的初始化状态。

**NOTE**

根据复位源，器件可能会出现与POR不同的唤醒延迟。该实现使得能够优化重置恢复时间。

### 6.8.1.2重启重置

重启复位与POR相同，允许应用模拟POR类复位，无需重启器件或激活RSTn引脚。它也可以通过调试器启动，因此不会影响与设备的调试连接。另一方面，POR导致调试断开。

### 6.8.1.3硬复位

硬重置会重置应用程序设置或修改的所有模块。这包括Cortex-M4的所有外设和非调试逻辑。
MSP432P401x
MCU支持多达16个硬复位源。表6-40列出了重置源分配。复位控制器寄存器可用于识别器件中的复位源。有关详细信息，请参阅“MSP432P4xx
SimpleLink™微控制器技术参考手册”中的“复位控制器”一章。

表6-40。 MSP432P401x硬复位源

| RESET SOURCE NUMBER | SOURCE |
|---|---|
| 0 SYSRESETREQ（Cortex-M4的系统复位输出） | |
| 1 | WDT_A Time-out (1) |
| 2 | WDT_A Password Violation (1) |
| 3 | FLCTL (2) |
| 4 | Reserved (3) |
| 5 | Reserved (3) |
| 6 | Reserved (3) |
| 7 | Reserved (3) |
| 8 | Reserved (3) |
| 9 | Reserved (3) |
| 10 | Reserved (3) |
| 11 | Reserved (3) |
| 12 | Reserved (3) |
| 13 | Reserved (3) |
| 14 | CS (4) |
| 15 | PCM (5) |

（1）WDT_A生成的复位可以映射为硬复位或软复位。
（2）如果检测到电压异常只能破坏闪存读取而不破坏系统的其余部分，则FLCTL可以产生复位。
（3）保留表示此硬复位源当前未使用，留待将来扩展。
（4）CS在技术上不是硬复位源，但如果在时钟源或频率变化期间发生硬复位，CS可以延长复位以允许时钟在释放系统之前稳定下来。这减少了不确定行为的可能性。
（5）PCM在技术上不是硬复位的来源，但如果硬复位导致电源模式改变，PCM可以延长复位以允许系统在释放复位之前稳定。这减少了不确定行为的可能性。

### 6.8.1.4软复位

软复位仅复位系统的执行组件，即Cortex-M4和WDT_A中的非调试逻辑。此重置对所有其他外围设备和系统组件仍然是非侵入性的。 MSP432P401x
MCU支持多达16个软复位源。表6-41列出了重置源分配。复位控制器寄存器可用于识别设计中的复位源。
有关详细信息，请参阅“MSP432P4xx SimpleLink™微控制器技术参考手册”中的“复位控制器”一章。

表6-41。 MSP432P401x软复位源

| RESET SOURCE NUMBER | SOURCE |
|---|---|
| 0 CPU LOCKUP条件（Cortex-M4的LOCKUP输出） | |
| 1 | WDT_A Time-out (1) |
| 2 | WDT_A Password Violation (1) |
| 3 | Reserved (2) |
| 4 | Reserved (2) |
| 5 | Reserved (2) |
| 6 | Reserved (2) |
| 7 | Reserved (2) |
| 8 | Reserved (2) |
| 9 | Reserved (2) |
| 10 | Reserved (2) |
| 11 | Reserved (2) |
| 12 | Reserved (2) |
| 13 | Reserved (2) |
| 14 | Reserved (2) |
| 15 | Reserved (2) |

（1）WDT_A生成的复位可以映射为硬复位或软复位
（2）保留表示此软复位源当前未使用，留待将来扩展。

**NOTE**

为了支持和增强复位条件的调试，复位控制器位于器件的PPB上。这样，即使器件处于硬复位状态或软复位状态，复位控制器也可以保持可访问状态。复位控制器允许覆盖硬复位和软复位，从而允许应用重新获得对器件的控制并隔离卡住复位的原因。

### 6.8.2电源系统（PSS）

PSS控制设备的所有电源相关功能。它由以下组件组成。

#### 6.8.2.1 VCCDET

VCCDET监视器件的DVCC和AVCC引脚上施加的输入电压。当发现VCC低于VCCDET跳变点的工作范围时，它会产生掉电条件，从而启动器件复位（POR类复位）。

### 6.8.2.2高端供电监控器和监控器（SVSMH）

SVSMH监督和监控VCC。
SVSMH具有可编程阈值设置，如果VCC低于所需阈值，则应用程序可以使用该设置生成复位或中断。在管理员模式下，SVSMH生成器件复位（POR类复位）。在监控模式下，SVSMH会产生中断。如果不需要监控和监控电源电压，也可以禁用SVSMH（进一步节省功耗）。

### 6.8.2.3核心电压调节器

MSP432P401x MCU可以编程为使用LDO或DC-DC作为器件核心域中数字逻辑的稳压器。DC-DC为高电流高性能应用提供了显着的功率效率提升。
LDO是一款高效稳压器，可在较低的VCC范围和超低功耗工作模式下提供功率优势。

核心工作电压（LDO或DC-DC的输出）由器件自动设置，具体取决于所选的器件工作模式（更多详细信息，请参见表6-42）。该器件可在LDO和DC-DC工作模式之间实现无缝切换，并实现无缝DC-DC故障安全机制。

## 6.8.3电源控制管理器（PCM）

PCM控制设备的操作模式和模式之间的切换。这由应用程序控制，应用程序可以选择满足其功率和性能要求的模式。表6-42列出了器件的工作模式。

**Table 6-42. MSP432P401x Operating Modes**

| OPERATING MODE | DESCRIPTION |
|---|---|
| AM_LDO_VCORE0基于LDO的有源模式，正常性能，核心电压等级0 | |
| LPM0_LDO_VCORE0与上面相同，但CPU为OFF（无代码执行） | |
| AM_LDO_VCORE1基于LDO的有源模式，最高性能，核心电压等级1 | |
| LPM0_LDO_VCORE1与上面相同，但CPU为OFF（无代码执行） | |
| AM_DCDC_VCORE0基于DC-DC的主动模式，正常性能，核心电压等级0 | |
| LPM0_DCDC_VCORE0与上面相同，但CPU为OFF（无代码执行） | |
| AM_DCDC_VCORE1基于DC-DC的主动模式，最大性能，核心电压等级1 | |
| LPM0_DCDC_VCORE1与上面相同，但CPU为OFF（无代码执行） | |
| AM_LF_VCORE0基于LDO的低频有源模式，核心电压等级为0 | |
| LPM0_LF_VCORE0与上面相同，但CPU为OFF（无代码执行） | |
| AM_LF_VCORE1基于LDO的低频有源模式，核心电压等级为1 | |
| LPM0_LF_VCORE1与上面相同，但CPU为OFF（无代码执行） | |
| LPM3_VCORE0基于LDO的低功耗模式，具有完全状态保持，核心电压等级0，RTC和WDT可以激活 | |
| LPM3_VCORE1基于LDO的低功耗模式，具有完全状态保持，核心电压等级1，RTC和WDT可以激活 | |
| LPM4_VCORE0基于LDO的低功耗模式，具有完全状态保持，核心电压等级为0，所有外设均被禁用。 | |
| LPM4_VCORE1基于LDO的低功耗模式，具有完全状态保持，核心电压等级1，所有外设均禁用 | |
| LPM3.5 | LDO based low-power mode, core voltage level 0, no retention of peripheral registers, RTC and WDT can be active |
| LPM4.5内核电压关闭，仅通过引脚复位或唤醒功能I / O唤醒 | |

### 6.8.4时钟系统（CS）

CS包含设备中各种时钟的来源。它还控制源与设备中不同时钟之间的映射。

#### 6.8.4.1 LFXT

LFXT支持32.768 kHz低频晶体。

#### 6.8.4.2 HFXT

HFXT支持高达48 MHz的高频晶体。

#### 6.8.4.3 DCO

DCO是一款高功效的可调谐内部振荡器，可产生高达48 MHz的频率。使用外部精密电阻时，DCO还支持高精度模式。

### 6.8.4.4超低功耗低频振荡器（VLO）

VLO是一款超低功耗内部振荡器，可在9.4 kHz的典型频率下生成低精度时钟。

### 6.8.4.5低频参考振荡器（REFO）

REFO可用作32.768 kHz时钟的备用低功耗低精度源，而不是LFXT。
REFO也可以编程为产生128 kHz时钟。

### 6.8.4.6模块振荡器（MODOSC）

MODOSC是一个内部时钟源，具有非常低的延迟唤醒时间。它的出厂校准频率为25 MHz。
MODOSC通常用于向不同模块提供“请求时钟”。它可以用作1 Msps采样率的ADC操作的时钟源。

### 6.8.4.7系统振荡器（SYSOSC）

SYSOSC是一个内部时钟源，出厂校准频率为5 MHz。它可以200 ksps采样率用作ADC操作的时钟源。此外，SYSOSC还用于各种系统级控制和管理操作的定时。

### 6.8.4.8故障安全机制

所有使用外部组件运行的时钟源都具有内置的故障安全机制，可自动切换到相关的备份源，从而确保虚假或不稳定的时钟不会影响设备操作。表6-43显示了不同类型的时钟源故障和相应的故障安全时钟。

**Table 6-43. Fail-Safe Clocks**

| Fault Type | Fail-Safe Clock |
|---|---|
| LFXT oscillator fault | REFO clock |
| HFXT oscillator fault | SYSOSC clock |
| 内部电阻模式下DCO外部电阻开路故障 | DCO时钟 |

### 6.8.5系统控制器（SYSCTL）

SYSCTL是一组设备的各种其他功能，包括SRAM组配置，RSTn / NMI功能选择和外设暂停控制。此外，SYSCTL还支持JTAG和SWD锁定以及IP保护等设备安全功能，可用于保护对整个设备存储器映射或闪存的某些选定区域的未授权访问。有关详细信息，请参阅“MSP432P4xx SimpleLink™微控制器技术参考手册”中的“系统控制器”一章。

**NOTE**

与Cortex-M4系统控制寄存器（在内部PPB空间中）的情况一样，系统控制器模块寄存器映射到Cortex-M4外部PPB。这样即使硬重置或软重置处于活动状态，也可以访问系统控制器模块。

## 6.9外围设备

### 6.9.1数字I / O.

最多可实现10个8位I / O端口：

- 所有单独的I / O位均可独立编程。
- 可以实现输入，输出和中断条件的任意组合。
- 所有端口均可编程上拉或下拉。
- 端口P1至P6提供边沿可选中断功能。
- 端口P1至P6上的LPM3，LPM4，LPM3.5和LPM4.5模式的唤醒功能。
- 所有指令均支持对端口控制寄存器的读写访问。
- 端口可以按字节或成对访问（16位宽度）。
- 端口P1至P10和PJ的所有引脚均支持电容触摸功能。
- 引脚P2.0至P2.3上的四个20 mA高驱动I / O.
- 所选数字I / O上的毛刺过滤功能。

#### 6.9.1.1数字I / O上的毛刺滤波

一些具有中断和唤醒功能的数字I / O可以通过使用模拟毛刺滤波器来抑制毛刺，以防止在器件工作期间意外中断或唤醒。模拟滤波器可抑制最小250 ns的宽毛刺。默认情况下，这些所选数字I / O上的毛刺滤波器已启用。如果应用程序中不需要毛刺过滤功能，则可以使用SYS_DIO_GLTFLT_CTL寄存器绕过该毛刺过滤功能。当该寄存器中的GLTFLT_EN位清零时，所有数字I / O上的毛刺滤波器都被旁路。当通过对相应的PySEL0.x和PySEL1.x寄存器进行编程将毛刺滤波器配置为外设或模拟功能时，可以在数字I / O上自动旁路。

**NOTE**

毛刺滤波器在MSP432P401x MCU上的以下数字I / O上实现：P1.0，P1.4，P1.5，P3.0，P3.4，P3.5，P6.6和P6.7。

## 6.9.2端口映射控制器（PMAPCTL）

端口映射控制器允许灵活和可重新配置的数字功能映射。

### 6.9.2.1端口映射定义

MSP432P401x

MCU上的端口映射控制器允许在端口P2，P3和P7上重新配置数字功能映射。表6-44列出了可用的映射。表6-45列出了支持端口映射的所有引脚的默认设置。

表6-44。端口映射助记符和函数

| VALUE | PxMAPy | MNEMONIC | 输入引脚功能 | 输出引脚功能 |
|---|---|---|---|---|
| 0 | PM_NONE | 无 | DVSS | |
| 1 | PM_UCA0CLK | eUSCI_A0 | 时钟输入/输出（由eUSCI控制的方向） | |
| 2 | PM_UCA0RXD | eUSCI_A0 | UART RXD（由eUSCI控制的方向 - 输入） | |
| | PM_UCA0SOMI | eUSCI_A0 | SPI从机输出主机（由eUSCI控制的方向） | |
| 3 | PM_UCA0TXD | eUSCI_A0 | UART TXD（由eUSCI控制的方向 - 输出） | |
| | PM_UCA0SIMO | eUSCI_A0 | 主站输出的SPI从站（由eUSCI控制的方向） | |
| 4 | PM_UCB0CLK | eUSCI_B0 | 时钟输入/输出（由eUSCI控制的方向） | |
| 5 | PM_UCB0SDA | | eUSCI_B0 I2C data (open drain and direction controlled by eUSCI) | |
| | PM_UCB0SIMO | eUSCI_B0 | 主站输出的SPI从站（由eUSCI控制的方向） | |
| 6 | PM_UCB0SCL | | eUSCI_B0 I2C clock (open drain and direction controlled by eUSCI) | |
| | PM_UCB0SOMI | eUSCI_B0 | SPI从机输出主机（由eUSCI控制的方向） | |
| 7 | PM_UCA1STE | eUSCI_A1 | SPI从发送使能（由eUSCI控制的方向） | |
| 8 | PM_UCA1CLK | eUSCI_A1 | 时钟输入/输出（由eUSCI控制的方向） | |
| 9 | PM_UCA1RXD | eUSCI_A1 | UART RXD（由eUSCI控制的方向 - 输入） | |
| | PM_UCA1SOMI | eUSCI_A1 | SPI从机输出主机（由eUSCI控制的方向） | |
| 10 | PM_UCA1TXD | eUSCI_A1 | UART TXD（由eUSCI控制的方向 - 输出） | |
| | PM_UCA1SIMO | eUSCI_A1 | 主站输出的SPI从站（由eUSCI控制的方向） | |
| 11 | PM_UCA2STE | eUSCI_A2 | SPI从发送使能（由eUSCI控制的方向） | |
| 12 | PM_UCA2CLK | eUSCI_A2 | 时钟输入/输出（由eUSCI控制的方向） | |
| 13 | PM_UCA2RXD | eUSCI_A2 | UART RXD（由eUSCI控制的方向 - 输入） | |
| | PM_UCA2SOMI | eUSCI_A2 | SPI从机输出主机（由eUSCI控制的方向） | |
| 14 | PM_UCA2TXD | eUSCI_A2 | UART TXD（由eUSCI控制的方向 - 输出） | |
| | PM_UCA2SIMO | eUSCI_A2 | 主机输出中的SPI从机（由eUSCI控制的方向） | |
| 15 | PM_UCB2STE | eUSCI_B2 | SPI从发送使能（由eUSCI控制的方向） | |
| 16 | PM_UCB2CLK | eUSCI_B2 | 时钟输入/输出（由eUSCI控制的方向） | |
| 17 | PM_UCB2SDA | | eUSCI_B2 I2C data (open drain and direction controlled by eUSCI) | |
| | PM_UCB2SIMO | eUSCI_B2 | 主机输出中的SPI从机（由eUSCI控制的方向） | |
| 18 | PM_UCB2SCL | | eUSCI_B2 I2C clock (open drain and direction controlled by eUSCI) | |
| | PM_UCB2SOMI | eUSCI_B2 | SPI从机输出主机（由eUSCI控制的方向） | |
| 19 | PM_TA0.0 | TA0 | CCR0捕获输入 | CCI0A TA0 CCR0比较输出 |
| 20 | PM_TA0.1 | TA0 | CCR1捕获输入 | CCI1A TA0 CCR1比较输出 |
| 21 | PM_TA0.2 | TA0 | CCR2捕获输入 | CCI2A TA0 CCR2比较输出 |
| 22 | PM_TA0.3 | TA0 | CCR3捕获输入 | CCI3A TA0 CCR3比较输出 |
| 23 | PM_TA0.4 | TA0 | CCR4捕获输入 | CCI4A TA0 CCR4比较输出 |
| 24 | PM_TA1.1 | TA1 | CCR1捕获输入 | CCI1A TA1 CCR1比较输出 |
| 25 | PM_TA1.2 | TA1 | CCR2捕获输入 | CCI2A TA1 CCR2比较输出 |
| 26 | PM_TA1.3 | TA1 | CCR3捕获输入 | CCI3A TA1 CCR3比较输出 |
| 27 | PM_TA1.4 | TA1 | CCR4捕获输入 | CCI4A TA1 CCR4比较输出 |

表6-44。端口映射助记符和函数（续）

| VALUE | PxMAPy MNEMONIC | 输入引脚功能 | 输出引脚功能 |
|---|---|---|---|
| 28 | PM_TA0CLK | Timer_A0外部时钟输入 | 无 |
| | PM_C0OUT | None | Comparator-E0 output |
| 29 | PM_TA1CLK | Timer_A1外部时钟输入 | 无 |
| | PM_C1OUT | None | Comparator-E1 output |
| 30 | PM_DMAE0 | DMAE0 input | None |
| | PM_SMCLK | None | SMCLK |
| 31（0FFh） | （1）PM_ANALOG禁用输出驱动器和输入施密特触发器，以防止施加模拟信号时的寄生交叉电流。 | | |

（1）PM_ANALOG助记符的值为31.端口映射寄存器为5位宽，高位被忽略，导致读取值为31。

**Table 6-45. Default Mapping**

| PIN名称PxMAPy | MNEMONIC | 输入引脚功能 | 输出引脚功能 |
|---|---|---|---|
| P2.0 / PM_UCA1STE | PM_UCA1STE | eUSCI_A1 SPI从发送使能（由eUSCI控制的方向） | |
| P2.1 / PM_UCA1CLK | PM_UCA1CLK | eUSCI_A1时钟输入/输出（由eUSCI控制的方向） | |
| P2.2/PM_UCA1RXD/ PM_UCA1SOMI | PM_UCA1RXD/ PM_UCA1SOMI | eUSCI_A1 UART RXD (direction controlled by eUSCI – Input) eUSCI_A1 SPI slave out master in (direction controlled by eUSCI) | |
| P2.3/PM_UCA1TXD/ PM_UCA1SIMO | PM_UCA1TXD/ PM_UCA1SIMO | eUSCI_A1 UART TXD (direction controlled by eUSCI – output)/ eUSCI_A1 SPI slave in master out (direction controlled by eUSCI) | |
| P2.4/PM_TA0.1(1) | PM_TA0.1 | TA0 CCR1 capture input CCI1A | TA0 CCR1 compare output Out1 |
| P2.5/PM_TA0.2(1) | PM_TA0.2 | TA0 CCR2 capture input CCI2A | TA0 CCR2 compare output Out2 |
| P2.6/PM_TA0.3(1) | PM_TA0.3 | TA0 CCR3 capture input CCI3A | TA0 CCR3 compare output Out3 |
| P2.7/PM_TA0.4(1) | PM_TA0.4 | TA0 CCR4 capture input CCI4A | TA0 CCR4 compare output Out4 |
| P3.0 / PM_UCA2STE | PM_UCA2STE | eUSCI_A2 SPI从发送使能（由eUSCI控制的方向） | |
| P3.1 / PM_UCA2CLK | PM_UCA2CLK | eUSCI_A2时钟输入/输出（由eUSCI控制的方向） | |
| P3.2/PM_UCA2RXD/ PM_UCA2SOMI | PM_UCA2RXD/ PM_UCA2SOMI | eUSCI_A2 UART RXD (direction controlled by eUSCI – input)/ eUSCI_A2 SPI slave out master in (direction controlled by eUSCI) | |
| P3.3/PM_UCA2TXD/ PM_UCA2SIMO | PM_UCA2TXD/ PM_UCA2SIMO | eUSCI_A2 UART TXD (direction controlled by eUSCI – output)/ eUSCI_A2 SPI slave in master out (direction controlled by eUSCI) | |
| P3.4 / PM_UCB2STE | PM_UCB2STE | eUSCI_B2 SPI从发送使能（由eUSCI控制的方向） | |
| P3.5 / PM_UCB2CLK | PM_UCB2CLK | eUSCI_B2时钟输入/输出（由eUSCI控制的方向） | |
| P3.6/PM_UCB2SIMO/ PM_UCB2SDA | PM_UCB2SIMO/ PM_UCB2SDA | eUSCI_B2 SPI slave in master out (direction controlled by eUSCI)/ eUSCI_B2 $I^2C$ data (open drain and direction controlled by eUSCI) | |
| P3.7/PM_UCB2SOMI/ PM_UCB2SCL | PM_UCB2SOMI/ PM_UCB2SCL | eUSCI_B2 SPI slave out master in (direction controlled by eUSCI)/ eUSCI_B2 $I^2C$ clock (open drain and direction controlled by eUSCI) | |
| P7.0/PM_SMCLK/ PM_DMAE0 | PM_SMCLK/ PM_DMAE0 | DMAE0 input | SMCLK |
| P7.1/PM_C0OUT/ PM_TA0CLK | PM_C0OUT/ PM_TA0CLK | Timer_A0 external clock input | Comparator-E0 output |
| P7.2/PM_C1OUT/ PM_TA1CLK | PM_C1OUT/ PM_TA1CLK | Timer_A1 external clock input | Comparator-E1 output |
| P7.3 / PM_TA0.0 | PM_TA0.0 | TA0 CCR0捕获输入CCI0A | TA0 CCR0比较输出Out0 |
| P7.4/PM_TA1.4/C0.5(1) | PM_TA1.4 | TA1 CCR4 capture input CCI4A | TA1 CCR4 compare output Out4 |
| P7.5/PM_TA1.3/C0.4(1) | PM_TA1.3 | TA1 CCR3 capture input CCI3A | TA1 CCR3 compare output Out3 |
| P7.6/PM_TA1.2/C0.3(1) | PM_TA1.2 | TA1 CCR2 capture input CCI2A | TA1 CCR2 compare output Out2 |
| P7.7/PM_TA1.1/C0.2(1) | PM_TA1.1 | TA1 CCR1 capture input CCI1A | TA1 CCR1 compare output Out1 |

（1）64引脚RGC封装不可用。

### 6.9.3 Timer_A

定时器TA0，TA1，TA2和TA3是16位定时器/计数器（Timer_A类型），每个定时器/计数器有5个捕获/比较寄存器。每个定时器支持多个捕获/比较，PWM输出和间隔定时。每个都有广泛的中断功能。可以在溢出条件下从计数器产生中断，并从每个捕获/比较寄存器产生中断。

#### 6.9.3.1 Timer_A信号连接表

表6-46至表6-49列出了器件上Timer_A模块的接口信号以及接口信号与相应引脚或内部信号的连接。以下规则适用于使用的命名约定。

•第一列列出了将时钟和/或触发器输入定时器的器件级引脚或内部信号。默认假设是这些是引脚，除非特别标记为（内部）。用于内部信号的命名法如下：

- CxOUT：比较器x的输出。
- TAx Cy：定时器x，捕捉/比较模块y的输出。

•第二列列出了定时器模块的输入信号。

•第三列列出了定时器的子模块，还包含功能（定时器，捕捉（输入或触发）或比较（输出或PWM））。

•第四列列出了定时器模块的输出信号。

•第五列列出了由Timer输出驱动的器件级引脚或内部信号。

默认假设是这些是引脚，除非特别标记为（内部）。

**NOTE**

表中列出的引脚名称是完整的名称。软件负责确保将引脚用于目标定时器功能的预期模式。

**NOTE**

由定时器输出提供的内部信号可以连接到器件中的其他模块（例如，其他定时器或ADC）（作为触发源）。

**Table 6-46. TA0 Signal Connections**

| DEVICE INPUT PIN OR INTERNAL SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT PIN OR INTERNAL SIGNAL |
|---|---|---|---|---|
| P7.1/PM_C0OUT/PM_TA0CLK | TACLK | Timer | N/A | N/A |
| ACLK (internal) | ACLK | | | |
| SMCLK (internal) | SMCLK | | | |
| C0OUT (internal) | INCLK | | | |
| P7.3/PM_TA0.0 | CCI0A | CCR0 | TA0 | P7.3/PM_TA0.0<br>TA0_C0 (internal) |
| $DV_{SS}$ | CCI0B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |
| P2.4/PM_TA0.1 | CCI1A | CCR1 | TA1 | P2.4/PM_TA0.1<br>TA0_C1 (internal)<br>ADC14 (internal)<br>ADC14SHSx = {1} |
| ACLK (internal) | CCI1B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |
| P2.5/PM_TA0.2 | CCI2A | CCR2 | TA2 | P2.5/PM_TA0.2<br>TA0_C2 (internal)<br>ADC14 (internal)<br>ADC14SHSx = {2} |
| C0OUT (internal) | CCI2B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |
| P2.6/PM_TA0.3 | CCI3A | CCR3 | TA3 | P2.6/PM_TA0.3<br>TA0_C3 (internal) |
| C1OUT (internal) | CCI3B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |
| P2.7/PM_TA0.4 | CCI4A | CCR4 | TA4 | P2.7/PM_TA0.4<br>TA0_C4 (internal) |
| TA1_C4 (Internal) | CCI4B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |

**Table 6-47. TA1 Signal Connections**

| DEVICE INPUT PIN OR INTERNAL SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT PIN OR INTERNAL SIGNAL |
|---|---|---|---|---|
| P7.2/PM_C1OUT/PM_TA1CLK | TACLK | Timer | N/A | N/A |
| ACLK (internal) | ACLK | | | |
| SMCLK (internal) | SMCLK | | | |
| C1OUT (internal) | INCLK | | | |
| P8.0/UCB3STE/TA1.0/C0.1 | CCI0A | CCR0 | TA0 | P8.0/UCB3STE/TA1.0/C0.1<br>TA1_C0 (internal) |
| $DV_{SS}$ | CCI0B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |
| P7.7/PM_TA1.1/C0.2 | CCI1A | CCR1 | TA1 | P7.7/PM_TA1.1/C0.2<br>TA1_C1 (internal)<br>ADC14 (internal)<br>ADC14SHSx = {3} |
| ACLK (internal) | CCI1B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |
| P7.6/PM_TA1.2/C0.3 | CCI2A | CCR2 | TA2 | P7.6/PM_TA1.2/C0.3<br>TA1_C2 (internal)<br>ADC14 (internal)<br>ADC14SHSx = {4} |
| C0OUT (internal) | CCI2B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |
| P7.5/PM_TA1.3/C0.4 | CCI3A | CCR3 | TA3 | P7.5/PM_TA1.3/C0.4<br>TA1_C3 (internal) |
| C1OUT (internal) | CCI3B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |
| P7.4/PM_TA1.4/C0.5 | CCI4A | CCR4 | TA4 | P7.4/PM_TA1.4/C0.5<br>TA1_C4 (internal) |
| TA0_C4 (internal) | CCI4B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |

**Table 6-48. TA2 Signal Connections**

| DEVICE INPUT PIN OR INTERNAL SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT PIN OR INTERNAL SIGNAL |
|---|---|---|---|---|
| P4.2/ACLK/TA2CLK/A11 | TACLK | Timer | N/A | N/A |
| ACLK (internal) | ACLK | | | |
| SMCLK (internal) | SMCLK | | | |
| From Capacitive Touch I/O 0 (internal) | INCLK | | | |
| P8.1/UCB3CLK/TA2.0/C0.0 | CCI0A | CCR0 | TA0 | P8.1/UCB3CLK/TA2.0/C0.0<br>TA2_C0 (internal) |
| $DV_{SS}$ | CCI0B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |
| P5.6/TA2.1/VREF+/VeREF+/C1.7 | CCI1A | CCR1 | TA1 | P5.6/TA2.1/VREF+/VeREF+/C1.7<br>TA2_C1 (internal)<br>ADC14 (internal)<br>ADC14SHSx = {5} |
| ACLK (internal) | CCI1B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |
| P5.7/TA2.2/VREF-/VeREF-/C1.6 | CCI2A | CCR2 | TA2 | P5.7/TA2.2/VREF-/VeREF-/C1.6<br>TA2_C2 (internal)<br>ADC14 (internal)<br>ADC14SHSx = {6} |
| C0OUT (internal) | CCI2B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |
| P6.6/TA2.3/UCB3SIMO/UCB3SDA/C1.1 | CCI3A | CCR3 | TA3 | P6.6/TA2.3/UCB3SIMO/<br>UCB3SDA/C1.1<br>TA2_C3 (internal) |
| TA3_C3 (internal) | CCI3B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |
| P6.7/TA2.4/UCB3SOMI/UCB3SCL/C1.0 | CCI4A | CCR4 | TA4 | P6.7/TA2.4/UCB3SOMI/<br>UCB3SCL/C1.0<br>TA2_C4 (internal) |
| From Capacitive Touch I/O 0 (internal) | CCI4B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |

**Table 6-49. TA3 Signal Connections**

| DEVICE INPUT PIN OR INTERNAL SIGNAL | MODULE INPUT SIGNAL | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT PIN OR INTERNAL SIGNAL |
|---|---|---|---|---|
| P8.3/TA3CLK/A22 | TACLK | Timer | N/A | N/A |
| ACLK (internal) | ACLK | | | |
| SMCLK (internal) | SMCLK | | | |
| From Capacitive Touch I/O 1 (internal) | INCLK | | | |
| P10.4/TA3.0/C0.7 | CCI0A | CCR0 | TA0 | P10.4/TA3.0/C0.7<br>TA3_C0 (internal) |
| $DV_{SS}$ | CCI0B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |
| P10.5/TA3.1/C0.6 | CCI1A | CCR1 | TA1 | P10.5/TA3.1/C0.6<br>TA3_C1 (internal)<br>ADC14 (internal)<br>ADC14SHSx = {7} |
| ACLK (internal) | CCI1B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |
| P8.2/TA3.2/A23 | CCI2A | CCR2 | TA2 | P8.2/TA3.2/A23<br>TA3_C2 (internal) |
| C0OUT (internal) | CCI2B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |
| P9.2/TA3.3 | CCI3A | CCR3 | TA3 | P9.2/TA3.3<br>TA3_C3 (internal) |
| TA2_C3 (internal) | CCI3B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |
| P9.3/TA3.4 | CCI4A | CCR4 | TA4 | P9.3/TA3.4<br>TA3_C4 (internal) |
| From Capacitive Touch I/O 1 (internal) | CCI4B | | | |
| $DV_{SS}$ | GND | | | |
| $DV_{CC}$ | $V_{CC}$ | | | |

### 6.9.4 Timer32

Timer32是ARM双32位定时器模块。它包含两个32位定时器，每个定时器可配置为两个独立的16位定时器。两个定时器可以生成独立事件或组合事件，可以根据应用要求进行处理。
Timer32用完与Cortex-M4 CPU相同的时钟。

### 6.9.5增强型通用串行通信接口（eUSCI）

eUSCI模块用于串行数据通信。
eUSCI模块支持同步通信协议，如SPI（3引脚或4引脚）和I2C，以及异步通信协议（如UART），具有自动波特率检测功能的增强型UART和IrDA。
eUSCI_An模块支持SPI（3引脚或4引脚），UART，增强型UART和IrDA。
eUSCI_Bn模块支持SPI（3引脚或4引脚）和I2C。
MSP432P401x MCU提供多达四个eUSCI_A和四个eUSCI_B模块。

### 6.9.6实时时钟（RTC_C）

RTC_C模块包含集成的实时时钟。它集成了一个内部日历，可以补偿少于31天的月份，包括闰年校正。 RTC_C还支持灵活的报警功能，偏移校准和温度补偿。
RTC_C操作在LPM3和LPM3.5模式下可用，以最大限度地降低功耗。

## 6.9.7 看门狗定时器（WDT_A）

WDT_A模块的主要功能是在出现软件问题时执行受控系统重启。如果所选时间间隔到期，则生成系统重置。如果应用程序中不需要看门狗功能，则可以将模块配置为间隔定时器，并可以选定的时间间隔生成中断。

**CAUTION**

在转换到LPM3或LPM3.5操作模式之前，必须将WDT设置为间隔模式。这允许WDT事件唤醒设备并将其返回到活动操作模式。在看门狗模式下使用WDT可能会因生成的复位而导致不确定的行为。

看门狗可以在超时或密码违规时生成重置。可以将此复位配置为在系统中生成硬复位或软复位。更多详细信息，请参见“MSP432P4xx SimpleLink™微控制器技术参考手册”。通常应将WDT配置为在系统中生成硬重置。软复位会重置CPU，但不会影响系统和外设的其余部分。因此，如果WDT配置为生成软复位，则应用程序应承担软复位可能损坏从CPU进入系统的正在进行的事务的事实。

表6-50列出了可以选择作为WDT_A模块源的时钟。

**Table 6-50. WDT_A Clocks**

| WDTSSEL | NORMAL OPERATION (WATCHDOG AND INTERVAL TIMER MODE) |
|---|---|
| 00 | SMCLK |
| 01 | ACLK |
| 10 | VLOCLK |
| 11 | BCLK |

## 6.9.8 ADC14

ADC14模块支持14位模数转换，采样速率高达1 Msps，具有差分和单端输入。该模块实现了14位SAR内核，采样和保持电路，参考发生器和转换结果缓冲器。具有下限和上限的窗口比较器允许通过不同的窗口比较器中断标志监视CPU独立的结果。

表6-51总结了可用的ADC14外部触发源。

表6-51。 ADC14触发信号连接

| ADC14SHSx | | CONNECTED TRIGGER SOURCE |
|---|---|---|
| BINARY | DECIMAL | |
| 000 | 0 | Software (ADC14SC) |
| 001 | 1 | TA0_C1 |
| 010 | 2 | TA0_C2 |
| 011 | 3 | TA1_C1 |
| 100 | 4 | TA1_C2 |
| 101 | 5 | TA2_C1 |
| 110 | 6 | TA2_C2 |
| 111 | 7 | TA3_C1 |

表6-52，表6-53和表6-54列出了ADC14内部和外部模拟输入之间的可用复用。

表6-52。 100引脚PZ器件上的ADC14通道映射

| ADC14 CHANNEL | EXTERNAL CHANNEL SOURCE (CONTROL BIT = 0) | INTERNAL CHANNEL SOURCE (CONTROL BIT = 1)(1) | CONTROL BIT(2) |
|---|---|---|---|
| 通道23 | A23电池监视器ADC14BATMAP | | |
| 通道22 | A22温度传感器ADC14TCMAP | | |
| 通道21 | A21 | N / A（保留） | ADC14CH0MAP |
| 通道20 | A20 | N / A（保留） | ADC14CH1MAP |
| 通道19 | A19 | N / A（保留） | ADC14CH2MAP |
| 通道18 | A18 | N / A（保留） | ADC14CH3MAP |

（1）如果内部源标记为N / A或保留，则表示只有外部源可用于该通道。

（2）有关包含表中列出的控制位的寄存器的详细信息，请参见“MSP432P4xx SimpleLink™微控制器技术参考手册”中的ADC14章节。

表6-53。在80引脚ZXH器件上进行ADC14通道映射

| ADC14 CHANNEL | EXTERNAL CHANNEL SOURCE (CONTROL BIT = 0) | INTERNAL CHANNEL SOURCE (CONTROL BIT = 1)(1) | CONTROL BIT(2) |
|---|---|---|---|
| 通道15 | A15电池监控器ADC14BATMAP | | |
| 通道14 | A14温度传感器ADC14TCMAP | | |
| 通道13 | A13 | N / A（保留） | ADC14CH0MAP |
| 通道12 | A12 | N / A（保留） | ADC14CH1MAP |
| 通道11 | A11 | N / A（保留） | ADC14CH2MAP |
| 通道10 | A10 | N / A（保留） | ADC14CH3MAP |

（1）如果内部源标记为N / A或保留，则表示只有外部源可用于该通道。

（2）有关包含表中列出的控制位的寄存器的详细信息，请参见“MSP432P4xx SimpleLink™微控制器技术参考手册”中的ADC14章节。

表6-54。 64引脚RGC器件上的ADC14通道映射

| ADC14 CHANNEL | EXTERNAL CHANNEL SOURCE (CONTROL BIT = 0) | INTERNAL CHANNEL SOURCE (CONTROL BIT = 1)(1) | CONTROL BIT(2) |
|---|---|---|---|
| 通道11 A11电池监控器ADC14BATMAP | | | |
| 通道10 A10温度传感器ADC14TCMAP | | | |
| Channel 9 | A9 | N/A (Reserved) | ADC14CH0MAP |
| Channel 8 | A8 | N/A (Reserved) | ADC14CH1MAP |
| Channel 7 | A7 | N/A (Reserved) | ADC14CH2MAP |
| Channel 6 | A6 | N/A (Reserved) | ADC14CH3MAP |

（1）如果内部源标记为N / A或保留，则表示只有外部源可用于该通道。

（2）有关包含表中列出的控制位的寄存器的详细信息，请参见“MSP432P4xx SimpleLink™微控制器技术参考手册”中的ADC14章节。

### 6.9.9 Comparator_E（COMP_E）

COMP_E模块的主要功能是支持精确斜率模数转换，电池电压监控和外部模拟信号监控。

MSP432P401x MCU上有两个COMP_E模块。

### 6.9.10共享参考（REF_A）

REF_A生成所有关键参考电压，可供设备中的各种模拟外设使用。REF_A的参考电压也可以切换到器件引脚上供外部使用。

### 6.9.11 CRC32

CRC32模块根据输入的数据值序列生成签名，并可用于数据检查。它支持CRC32和CRC16计算。

- CRC16计算签名基于CRC16-CCITT标准。
- CRC32计算签名基于CRC32-ISO3309标准。

### 6.9.12 AES256加速器

AES加速器模块根据硬件中的高级加密标准（AES）（FIPS PUB 197），使用128位，192位或256位密钥对128位数据进行加密和解密。

### 6.9.13真随机种子

设备描述符信息（TLV）部分包含128位真随机种子，可用于实现确定性随机数生成器。

## 6.10代码开发和调试

MSP432P401x MCU支持各种方法，用户可以通过这些方法在器件上进行代码开发和调试。

### 6.10.1基于JTAG和SWD的开发，调试和跟踪

该器件支持4引脚JTAG和2引脚SWD工作模式。该器件与当今市场上的所有标准Cortex-M4调试器兼容。设备中的调试逻辑旨在保持对应用程序状态的最小干扰。在低功耗模式下，用户可以使调试器覆盖PSS的状态，从而获得对调试和跟踪功能的访问。

在2引脚SWD模式下，TDO引脚可用于输出串行线跟踪输出（SWO）数据。此外，器件的TDI和TDO引脚可以重新分配为用户I / O.更多详细信息，请参见第6.12.22节和第6.12.23节。

**NOTE**

如果设备已激活调试安全性，则完全禁用对设备的调试器访问。但是，调试器仍然能够扫描CPU的运行/暂停状态。
只有在开始大量擦除设备闪存内容之后，才可能进一步控制和看到设备。

## 6.10.2外围停止控制

系统控制器模块中的外设暂停控制寄存器允许用户在代码开发和调试期间独立控制器件外设的功能。当CPU停止时，该寄存器中的位可以控制相应的外设是否冻结其操作（例如递增，发送和接收）或继续其操作（调试仍然是非侵入式的）。无论外设暂停控制寄存器中的值如何，外设寄存器都可以访问。

### 6.10.3 Bootloader（BSL）

BSL使用户能够使用UART或I2C或SPI串行接口对器件上的闪存或SRAM进行编程。通过BSL访问设备内存受用户定义的密码保护。表6-55列出了使用BSL所需的器件引脚。

**Table 6-55. BSL Pins and Functions**

| DEVICE PIN | BSL FUNCTION |
|---|---|
| P1.2 | UART BSLRXD |
| P1.3 | UART BSLTXD |
| P1.4 | SPI BSLSTE |
| P1.5 | SPI BSLCLK |
| P1.6 | SPI BSLSIMO |
| P1.7 | SPI BSLSOMI |
| P3.6 | $I^2C$ BSLSDA |
| P3.7 | $I^2C$ BSLSCL |

在以下任何条件下调用BSL。

- Flash main memory is erased
- Hardware invocation of BSL
- Software based API calls to BSL functions

用户可以使用端口P1，P2或P3的任何引脚执行BSL的硬件调用。为此目的选择的引脚不应与用于BSL的引脚相同。用户可以通过闪存引导覆盖邮箱配置设备引脚及其极性。然后，可以在配置引脚的电源循环或POR复位事件时调用BSL。

有关BSL功能及其实现的完整说明，请参阅MSP432P401R引导加载程序（BSL）用户指南。

## 6.10.4设备安全

MSP432P401xx MCU为在器件上编程的用户应用代码提供以下两种类型的器件安全性。

- JTAG and SWD Lock
- IP Protection

JTAG和SWD锁定，因为名称表示锁定设备的JTAG和SWD接口。
IP保护对于保护客户软件IP非常有用，例如，在多供应商开发方案中。最多支持四个具有可配置起始地址和大小的IP保护区域。设备的安全配置使用闪存引导覆盖邮箱完成。

此外，SYSCTL模块还为JTAG和SWD锁定或已定义IP保护区域的设备上的应用程序代码提供加密的现场更新基础结构。有关器件安全功能的完整详细信息，请参阅“MSP432P4xx SimpleLink™微控制器技术参考手册”中的系统控制器（SYSCTL）章节。

## 6.11性能基准

MSP432P401xx
MCU在给定的软件配置和配置文件配置下可实现以下性能基准测试。在环境温度为25° C时，系统电源电压为2.97 V，测量这些性能基准。

### 6.11.1 ULPBench性能：192.3 ULPMark-CP

表6-56显示了此性能基准测试的软件配置。表6-57显示了配置文件配置。

**Table 6-56. Software Configuration**

| ITEMS | DETAILS |
|---|---|
| 编译器名称和版本IAR EWARM v7.50.3 | |
| 编译器标志--endian = little --cpu = Cortex-M4F -e --fpu = VFPv4_sp -Ohs --no_size_constraints --mfc | |
| ULPBench Profile and Version | v1.1.X |
| EnergyMonitor Software Version | 1.1.3 |

**Table 6-57. Profile Configuration**

| CONFIGURATION | DETAILS |
|---|---|
| Wakeup Timer Module | RTC |
| 唤醒定时器时钟源外部晶振 | |
| Wakeup Timer Frequency [Hz] | 32768 Hz |
| Wakeup Timer Accuracy [ppm] | 20 ppm |
| Active Power Mode Name | Active Mode |
| 活动模式时钟配置CPU：16 MHz，RTC：32 KHz | |
| Active Mode Voltage Integrity | 1.62 V |
| Inactive Power Mode Name | LPM3 |
| 非活动时钟配置CPU：OFF，RTC：32 kHz | |
| Inactive Mode Voltage Integrity | 1.62 V |

### 6.11.2 CoreMark / MHz性能：3.41

表6-58显示了此性能基准测试的软件配置。表6-59显示了配置文件配置。

**Table 6-58. Software Configuration**

| ITEMS | DETAILS |
|---|---|
| 编译器名称和版本IAR EWARM v6.70.3 | |
| 编译器标志--no_size_constraints --debug --endian = little --cpu = Cortex-M4F -e --fpu = None -Ohs | |
| CoreMark Profile and Version | v1.0 |

**Table 6-59. Profile Configuration**

| CONFIGURATION | DETAILS |
|---|---|
| Active Power Mode Name | Active Mode |
| 活动模式时钟配置CPU：3 MHz | |
| Active Mode Voltage Integrity | 1.62 V |

### 6.11.3 DMIPS / MHz（Dhrystone 2.1）性能：1.22

表6-60显示了此性能基准测试的软件配置。表6-61显示了配置文件配置。

**Table 6-60. Software Configuration**

| ITEMS | DETAILS |
|---|---|
| 编译器名称和版本Keil uVision ARM编译器v5.06（版本20） | |
| Compiler Flags | -c --cpu Cortex-M4.fp -g -O3 -Otime --apcs=interwork --asm --interleave --asm_dir –no_inline –no_multifile |
| Dhrystone Profile and Version | v2.1 |

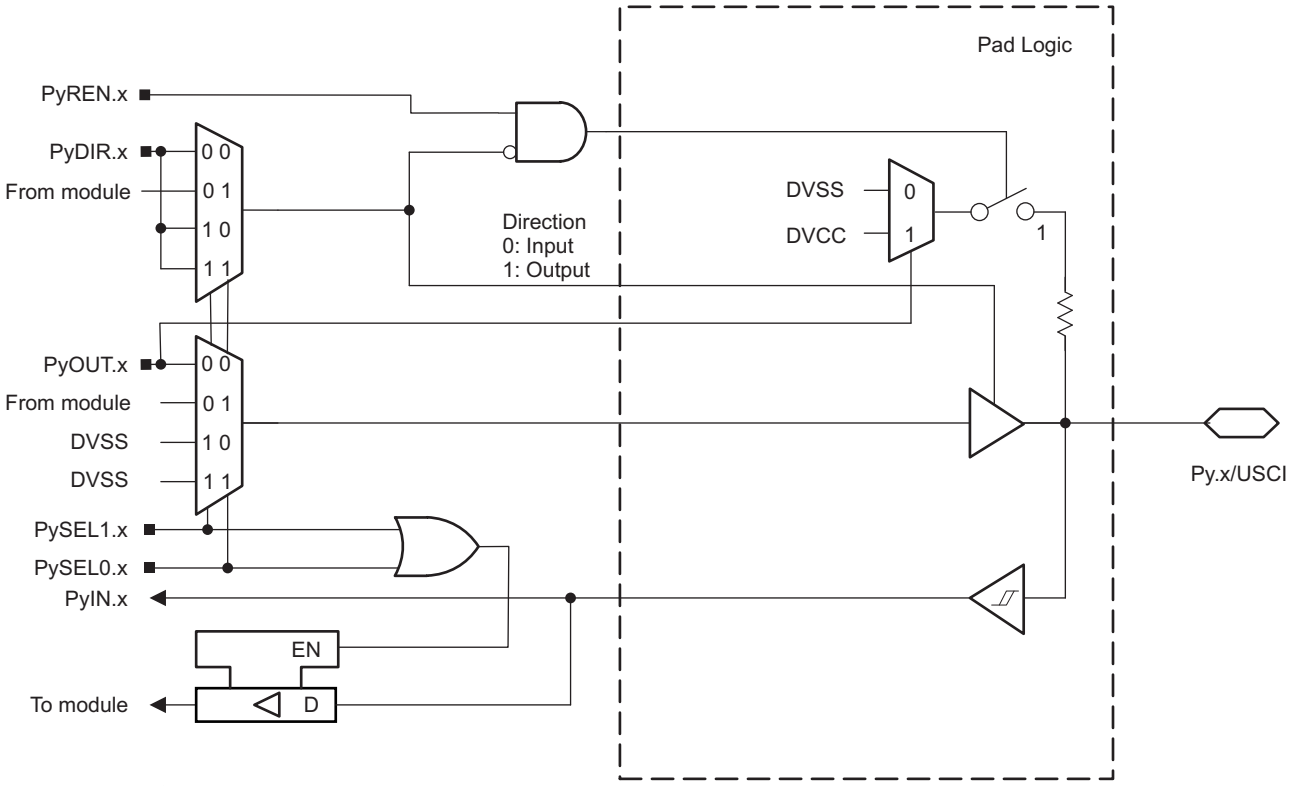
**Table 6-61. Profile Configuration**

| CONFIGURATION | DETAILS |
|---|---|
| Active Power Mode Name | Active Mode |
| 活动模式时钟配置CPU：3 MHz | |
| Active Mode Voltage Integrity | 1.62 V |

## 6.12输入/输出图

### 6.12.1端口P1（P1.0至P1.7）输入/输出，带施密特触发器

端口图如图6-7所示。表6-62总结了引脚功能的选择。




仅限功能表示。

**Figure 6-7. Py.x/USCI Pin Diagram**

表6-62。端口P1（P1.0至P1.7）引脚功能

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x |
| P1.0/UCA0STE | 0 | P1.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCA0STE | X(2) | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 1 |
| | | DVSS | 1 | | |
| P1.1/UCA0CLK | 1 | P1.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCA0CLK | X(2) | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 1 |
| | | DVSS | 1 | | |
| P1.2/UCA0RXD/UCA0SOMI | 2 | P1.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCA0RXD/UCA0SOMI | X(2) | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 1 |
| | | DVSS | 1 | | |
| P1.3/UCA0TXD/UCA0SIMO | 3 | P1.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCA0TXD/UCA0SIMO | X(2) | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 1 |
| | | DVSS | 1 | | |
| P1.4/UCB0STE | 4 | P1.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB0STE | X(3) | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 1 |
| | | DVSS | 1 | | |
| P1.5/UCB0CLK | 5 | P1.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB0CLK | X(3) | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 1 |
| | | DVSS | 1 | | |
| P1.6/UCB0SIMO/UCB0SDA | 6 | P1.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB0SIMO/UCB0SDA | X(3) | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 1 |
| | | DVSS | 1 | | |

(1) X = don't care
（2）由eUSCI_A0模块控制的方向。
（3）方向由eUSCI_B0模块控制。

表6-62。端口P1（P1.0至P1.7）引脚功能（续）

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P1DIR.x | P1SEL1.x | P1SEL0.x |
| P1.7/UCB0SOMI/UCB0SCL | 7 | P1.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB0SOMI/UCB0SCL | X(3) | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 1 |
| | | DVSS | 1 | | |

### 6.12.2端口P2（P2.0至P2.3）输入/输出，带施密特触发器

端口图如图6-7所示。表6-63总结了引脚功能的选择。

表6-63。端口P2（P2.0至P2.3）引脚功能

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | | |
|---|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL1.x | P2SEL0.x | P2MAPx |
| P2.0/PM_UCA1STE | 0 | P2.0 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | UCA1STE | X(2) | 0 | 1 | default |
| | | N/A | 0 | 1 | 0 | X |
| | | DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | X |
| | | DVSS | 1 | | | |
| P2.1/PM_UCA1CLK | 1 | P2.1 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | UCA1CLK | X(2) | 0 | 1 | default |
| | | N/A | 0 | 1 | 0 | X |
| | | DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | X |
| | | DVSS | 1 | | | |
| P2.2/PM_UCA1RXD/PM_UCA1SOMI | 2 | P2.2 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | UCA1RXD/UCA1SOMI | X(2) | 0 | 1 | default |
| | | N/A | 0 | 1 | 0 | X |
| | | DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | X |
| | | DVSS | 1 | | | |
| P2.3/PM_UCA1TXD/PM_UCA1SIMO | 3 | P2.3 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | UCA1TXD/UCA1SIMO | X(2) | 0 | 1 | default |
| | | N/A | 0 | 1 | 0 | X |
| | | DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | X |
| | | DVSS | 1 | | | |

(1) X = don't care

（2）方向由eUSCI_A1模块控制。

6.12.3端口P3（P3.0至P3.7）带施密特触发器的输入/输出

端口图如图6-7所示。表6-64总结了引脚功能的选择。

表6-64。端口P3（P3.0至P3.7）引脚功能

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | | |
|---|---|---|---|---|---|---|
| | | | P3DIR.x | P3SEL1.x | P3SEL0.x | P3MAPx |
| P3.0/PM_UCA2STE | 0 | P3.0 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | UCA2STE | X(2) | 0 | 1 | default |
| | | N/A | 0 | 1 | 0 | X |
| | | DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | X |
| | | DVSS | 1 | | | |
| P3.1/PM_UCA2CLK | 1 | P3.1 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | UCA2CLK | X(2) | 0 | 1 | default |
| | | N/A | 0 | 1 | 0 | X |
| | | DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | X |
| | | DVSS | 1 | | | |
| P3.2/PM_UCA2RXD/PM_UCA2SOMI | 2 | P3.2 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | UCA2RXD/UCA2SOMI | X(2) | 0 | 1 | default |
| | | N/A | 0 | 1 | 0 | X |
| | | DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | X |
| | | DVSS | 1 | | | |
| P3.3/PM_UCA2TXD/PM_UCA2SIMO | 3 | P3.3 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | UCA2TXD/UCA2SIMO | X(2) | 0 | 1 | default |
| | | N/A | 0 | 1 | 0 | X |
| | | DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | X |
| | | DVSS | 1 | | | |
| P3.4/PM_UCB2STE | 4 | P3.4 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | UCB2STE | X(3) | 0 | 1 | default |
| | | N/A | 0 | 1 | 0 | X |
| | | DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | X |
| | | DVSS | 1 | | | |
| P3.5/PM_UCB2CLK | 5 | P3.5 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | UCB2CLK | X(3) | 0 | 1 | default |
| | | N/A | 0 | 1 | 0 | X |
| | | DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | X |
| | | DVSS | 1 | | | |

(1) X = don't care
（2）由eUSCI_A2模块控制的方向。
（3）方向由eUSCI_B2模块控制。

表6-64。端口P3（P3.0至P3.7）引脚功能（续）

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | | |
|---|---|---|---|---|---|---|
| | | | P3DIR.x | P3SEL1.x | P3SEL0.x | P3MAPx |
| P3.6/PM_UCB2SIMO/PM_UCB2SDA | 6 | P3.6 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | UCB2SIMO/UCB2SDA | X(3) | 0 | 1 | default |
| | | N/A | 0 | 1 | 0 | X |
| | | DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | X |
| | | DVSS | 1 | | | |
| P3.7/PM_UCB2SOMI/PM_UCB2SCL | 7 | P3.7 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | UCB2SOMI/UCB2SCL | X(3) | 0 | 1 | default |
| | | N/A | 0 | 1 | 0 | X |
| | | DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | X |
| | | DVSS | 1 | | | |

### 6.12.4端口P9（P9.4至P9.7）带施密特触发器的输入/输出

端口图如图6-7所示。表6-65总结了引脚功能的选择。

表6-65。端口P9（P9.4至P9.7）引脚功能

| PIN NAME (P9.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P9DIR.x | P9SEL1.x | P9SEL0.x |
| P9.4/UCA3STE(2) | 4 | P9.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCA3STE | X(3) | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 1 |
| | | DVSS | 1 | | |
| P9.5/UCA3CLK(2) | 5 | P9.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCA3CLK | X(3) | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 1 |
| | | DVSS | 1 | | |
| P9.6/UCA3RXD/UCA3SOMI(2) | 6 | P9.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCA3RXD/UCA3SOMI | X(3) | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 1 |
| | | DVSS | 1 | | |
| P9.7/UCA3TXD/UCA3SIMO(2) | 7 | P9.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCA3TXD/UCA3SIMO | X(3) | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 1 |
| | | DVSS | 1 | | |

(1) X = don't care
（2）不适用于80ZYH和64RGC封装。
（3）方向由eUSCI_A3模块控制。

## 6.12.5端口P10（P10.0至P10.3）带施密特触发器的输入/输出

端口图如图6-7所示。表6-66总结了引脚功能的选择。

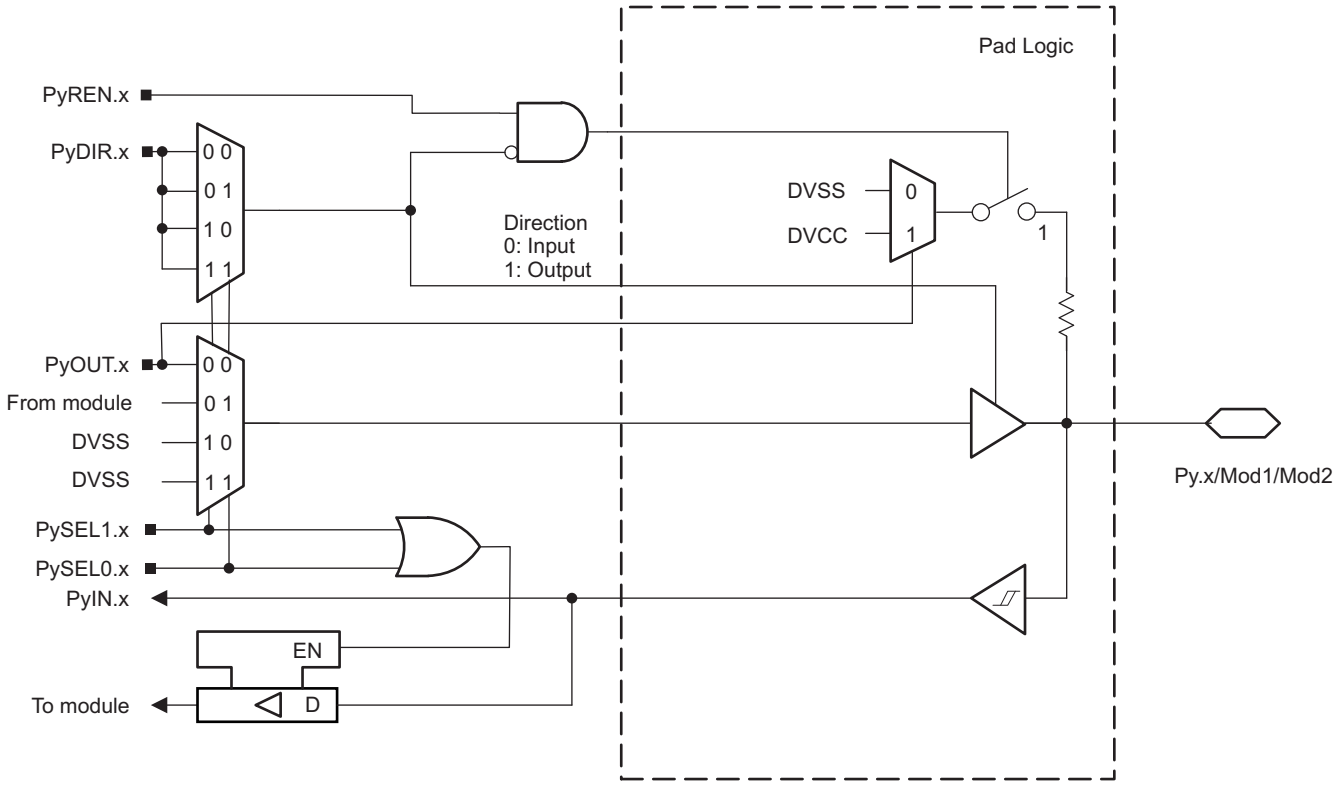
表6-66。端口P10（P10.0至P10.3）引脚功能

| PIN NAME (P10.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P10DIR.x | P10SEL1.x | P10SEL0.x |
| P10.0/UCB3STE(2) | 0 | P10.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB3STE | X(3) | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 1 |
| | | DVSS | 1 | | |
| P10.1/UCB3CLK(2) | 1 | P10.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB3CLK | X(3) | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 1 |
| | | DVSS | 1 | | |
| P10.2/UCB3SIMO/UCB3SDA(2) | 2 | P10.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB3SIMO/UCB3SDA | X(3) | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 1 |
| | | DVSS | 1 | | |
| P10.3/UCB3SOMI/UCB3SCL(2) | 3 | P10.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB3SOMI/UCB3SCL | X(3) | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 1 |
| | | DVSS | 1 | | |

(1) X = don't care
（2）不适用于80ZYH和64RGC封装。
（3）方向由eUSCI_B3模块控制。

6.12.6端口P2（P2.4至P2.7）输入/输出，带施密特触发器

端口图如图6-8所示。表6-67总结了引脚功能的选择。




仅限功能表示。

**Figure 6-8. Py.x/Mod1/Mod2 Pin Diagram**

表6-67。端口P2（P2.4至P2.7）引脚功能

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | | |
|---|---|---|---|---|---|---|
| | | | P2DIR.x | P2SEL1.x | P2SEL0.x | P2MAPx |
| P2.4/PM_TA0.1(2) | 4 | P2.4 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | TA0.CCI1A | 0 | 0 | 1 | default |
| | | TA0.1 | 1 | | | |
| | | N/A | 0 | 1 | 0 | X |
| | | DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | X |
| | | DVSS | 1 | | | |
| P2.5/PM_TA0.2(2) | 5 | P2.5 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | TA0.CCI2A | 0 | 0 | 1 | default |
| | | TA0.2 | 1 | | | |
| | | N/A | 0 | 1 | 0 | X |
| | | DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | X |
| | | DVSS | 1 | | | |
| P2.6/PM_TA0.3(2) | 6 | P2.6 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | TA0.CCI3A | 0 | 0 | 1 | default |
| | | TA0.3 | 1 | | | |
| | | N/A | 0 | 1 | 0 | X |
| | | DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | X |
| | | DVSS | 1 | | | |
| P2.7/PM_TA0.4(2) | 7 | P2.7 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | TA0.CCI4A | 0 | 0 | 1 | default |
| | | TA0.4 | 1 | | | |
| | | N/A | 0 | 1 | 0 | X |
| | | DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | X |
| | | DVSS | 1 | | | |

(1) X = don't care
（2）不适用于64引脚RGC封装。

## 6.12.7端口P7（P7.0至P7.3）输入/输出，带施密特触发器

端口图如图6-8所示。表6-68总结了引脚功能的选择。

表6-68。端口P7（P7.0至P7.3）引脚功能

| PIN NAME (P7.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | | |
|---|---|---|---|---|---|---|
| | | | P7DIR.x | P7SEL1.x | P7SEL0.x | P7MAPx |
| P7.0/PM_SMCLK/ PM_DMAE0 | 0 | P7.0 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | DMAE0 | 0 | 0 | 1 | default |
| | | SMCLK | 1 | | | |
| | | N/A | 0 | 1 | 0 | X |
| | | DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | X |
| | | DVSS | 1 | | | |
| P7.1/PM_C0OUT/ PM_TA0CLK | 1 | P7.1 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | TA0CLK | 0 | 0 | 1 | default |
| | | C0OUT | 1 | | | |
| | | N/A | 0 | 1 | 0 | X |
| | | DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | X |
| | | DVSS | 1 | | | |
| P7.2/PM_C1OUT/ PM_TA1CLK | 2 | P7.2 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | TA1CLK | 0 | 0 | 1 | default |
| | | C1OUT | 1 | | | |
| | | N/A | 0 | 1 | 0 | X |
| | | DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | X |
| | | DVSS | 1 | | | |
| P7.3/PM_TA0.0 | 3 | P7.3 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | TA0.CCI0A | 0 | 0 | 1 | default |
| | | TA0.0 | 1 | | | |
| | | N/A | 0 | 1 | 0 | X |
| | | DVSS | 1 | | | |
| | | N/A | 0 | 1 | 1 | X |
| | | DVSS | 1 | | | |

(1) X = don't care

### 6.12.8端口P9（P9.2和P9.3）带施密特触发器的输入/输出

端口图如图6-8所示。表6-69总结了引脚功能的选择。

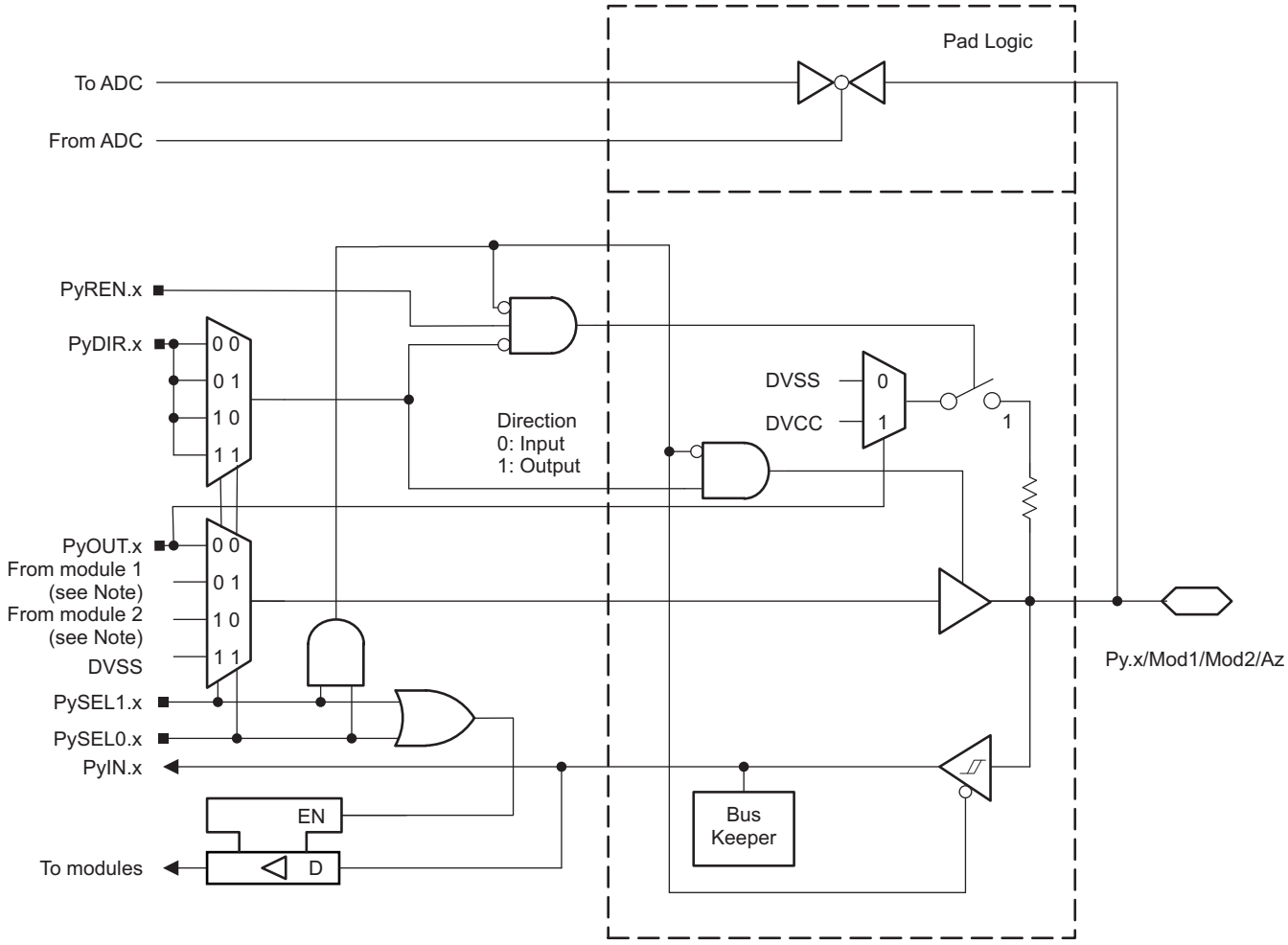
表6-69。端口P9（P9.2和P9.3）引脚功能

| PIN NAME (P9.x) | x | FUNCTION | CONTROL BITS OR SIGNALS | | |
|---|---|---|---|---|---|
| | | | P9DIR.x | P9SEL1.x | P9SEL0.x |
| P9.2/TA3.3(1) | 2 | P9.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA3.CCI3A | 0 | 0 | 1 |
| | | TA3.3 | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 1 |
| | | DVSS | 1 | | |
| P9.3/TA3.4(1) | 3 | P9.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA3.CCI4A | 0 | 0 | 1 |
| | | TA3.4 | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 1 |
| | | DVSS | 1 | | |

（1）不适用于80ZXH和64RGC封装。

6.12.9端口P4（P4.0至P4.7）输入/输出，带施密特触发器

端口图如图6-9所示。表6-70总结了引脚功能的选择。




注意：如果模块1或模块2功能不可用，则输出为DVSS。请参见引脚功能表。

仅限功能表示。

图6-9。 Py.x / Mod1 / Mod2 / Az Pin图

表6-70。端口P4（P4.0至P4.7）引脚功能

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P4DIR.x | P4SEL1.x | P4SEL0.x |
| P4.0/A13(2) | 0 | P4.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | A13(3) | X | 1 | 1 |
| P4.1/A12(2) | 1 | P4.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | A12(3) | X | 1 | 1 |
| P4.2/ACLK/TA2CLK/A11 | 2 | P4.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | ACLK | 1 | | |
| | | TA2CLK | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | A11(3) | X | 1 | 1 |
| P4.3/MCLK/RTCCLK/A10 | 3 | P4.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | MCLK | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | RTCCLK | 1 | | |
| | | A10(3) | X | 1 | 1 |
| P4.4/HSMCLK/SVMHOUT/ A9 | 4 | P4.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | HSMCLK | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | SVMHOUT | 1 | | |
| | | A9(3) | X | 1 | 1 |
| P4.5/A8 | 5 | P4.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | A8(3) | X | 1 | 1 |
| P4.6/A7 | 6 | P4.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | A7(3) | X | 1 | 1 |

(1) X = don't care
（2）不适用于64引脚RGC封装
（3）设置P4SEL1.x和P4SEL0.x会禁用输出驱动器和输入施密特触发器，以防止在施加模拟信号时出现寄生交叉电流。

表6-70。端口P4（P4.0至P4.7）引脚功能（续）

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P4DIR.x | P4SEL1.x | P4SEL0.x |
| P4.7/A6 | 7 | P4.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | A6(3) | X | 1 | 1 |

## 6.12.10端口P5（P5.0至P5.5）带施密特触发器的输入/输出

端口图如图6-9所示。表6-71总结了引脚功能的选择。

表6-71。端口P5（P5.0至P5.5）引脚功能

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P5DIR.x | P5SEL1.x | P5SEL0.x |
| P5.0/A5 | 0 | P5.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | A5(2) | X | 1 | 1 |
| P5.1/A4 | 1 | P5.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | A4(2) | X | 1 | 1 |
| P5.2/A3 | 2 | P5.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | A3(2) | X | 1 | 1 |
| P5.3/A2 | 3 | P5.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | A2(2) | X | 1 | 1 |
| P5.4/A1 | 4 | P5.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | A1(2) | X | 1 | 1 |
| P5.5/A0 | 5 | P5.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | A0(2) | X | 1 | 1 |

(1) X = don't care

（2）设置P5SEL1.x和P5SEL0.x禁用输出驱动器和输入施密特触发器，以防止施加模拟信号时的寄生交叉电流。

## 6.12.11端口P6（P6.0和P6.1）带施密特触发器的输入/输出

端口图如图6-9所示。表6-72总结了引脚功能的选择。

表6-72。端口P6（P6.0和P6.1）引脚功能

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P6DIR.x | P6SEL1.x | P6SEL0.x |
| P6.0/A15(2) | 0 | P6.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | A15(3) | X | 1 | 1 |
| P6.1/A14(2) | 1 | P6.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | A14(3) | X | 1 | 1 |

(1) X = don't care
（2）不适用于64引脚RGC封装
（3）设置P6SEL1.x和P6SEL0.x禁用输出驱动器和输入施密特触发器，以防止施加模拟信号时的寄生交叉电流。

### 6.12.12端口P8（P8.2至P8.7）带施密特触发器的输入/输出

端口图如图6-9所示。表6-73总结了引脚功能的选择。

表6-73。端口P8（P8.2至P8.7）引脚功能

| PIN NAME (P8.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P8DIR.x | P8SEL1.x | P8SEL0.x |
| P8.2/TA3.2/A23(2) | 2 | P8.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA3.CCI2A | 0 | 0 | 1 |
| | | TA3.2 | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | A23(3) | X | 1 | 1 |
| P8.3/TA3CLK/A22(2) | 3 | P8.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA3CLK | 0 | 0 | 1 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | A22(3) | X | 1 | 1 |
| P8.4/A21(2) | 4 | P8.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | A21(3) | X | 1 | 1 |
| P8.5/A20(2) | 5 | P8.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | A20(3) | X | 1 | 1 |
| P8.6/A19(2) | 6 | P8.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | A19(3) | X | 1 | 1 |
| P8.7/A18(2) | 7 | P8.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | A18(3) | X | 1 | 1 |

(1) X = don't care
（2）不适用于80ZXH和64RGC封装。
（3）设置P8SEL1.x和P8SEL0.x禁用输出驱动器和输入施密特触发器，以防止施加模拟信号时的寄生交叉电流。

### 6.12.13端口P9（P9.0和P9.1）带施密特触发器的输入/输出

端口图如图6-9所示。表6-74总结了引脚功能的选择。

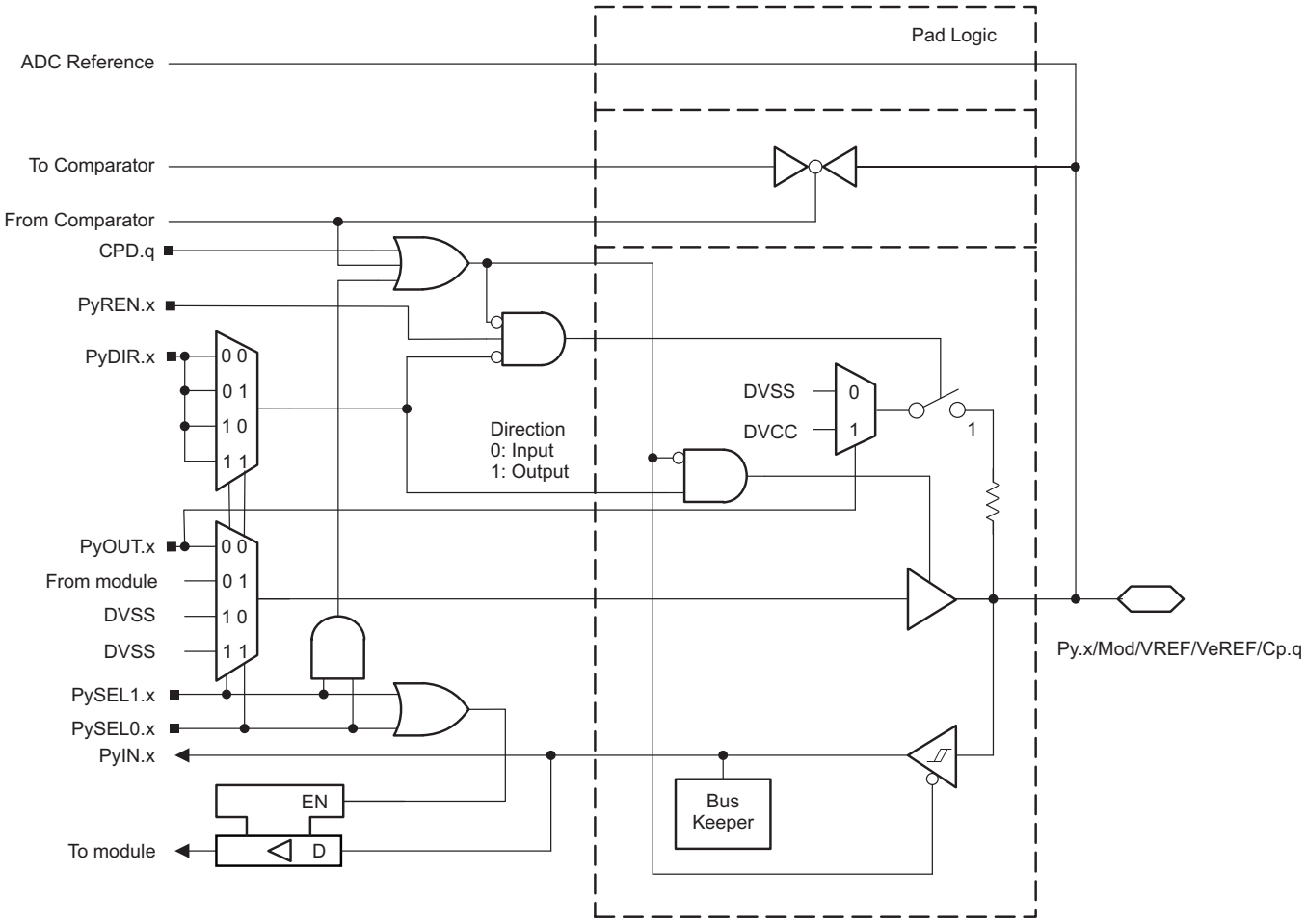
表6-74。端口P9（P9.0和P9.1）引脚功能

| PIN NAME (P9.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P9DIR.x | P9SEL1.x | P9SEL0.x |
| P9.0/A17(2) | 0 | P9.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | A17(3) | X | 1 | 1 |
| P9.1/A16(2) | 1 | P9.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | N/A | 0 | 0 | 1 |
| | | DVSS | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | A16(3) | X | 1 | 1 |

(1) X = don't care
（2）不适用于80ZYH和64RGC封装
（3）设置P9SEL1.x和P9SEL0.x禁用输出驱动器和输入施密特触发器，以防止施加模拟信号时的寄生交叉电流。

6.12.14端口P5（P5.6和P5.7）带施密特触发器的输入/输出

端口图如图6-10所示。表6-75总结了引脚功能的选择。




仅限功能表示。

图6-10。 Py.x / Mod / VREF / VeREF / Cp.q引脚图

表6-75。端口P5（P5.6和P5.7）引脚功能

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P5DIR.x | P5SEL1.x | P5SEL0.x |
| P5.6/TA2.1/VREF+/VeREF+/C1.7 | 6 | P5.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA2.CCI1A | 0 | 0 | 1 |
| | | TA2.1 | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | VREF+, VeREF+, C1.7(2)(3) | X | 1 | 1 |
| P5.7/TA2.2/VREF-/VeREF-/C1.6 | 7 | P5.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA2.CCI2A | 0 | 0 | 1 |
| | | TA2.2 | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | VREF-, VeREF-, C1.6(2)(3) | X | 1 | 1 |

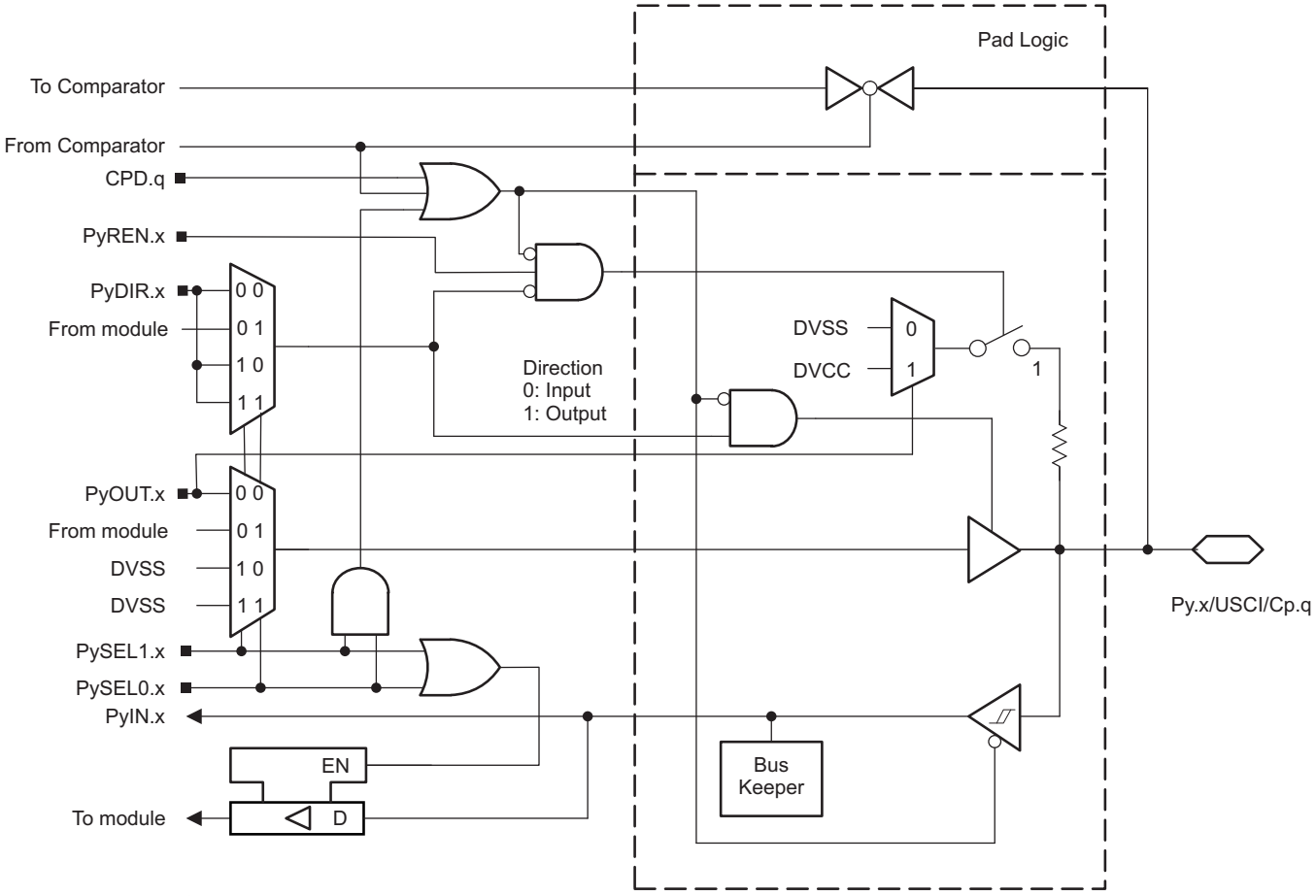
(1) X = don't care

（2）设置P5SEL1.x和P5SEL0.x禁用输出驱动器和输入施密特触发器，以防止施加模拟信号时的寄生交叉电流。

（3）设置比较器的CEPD.q位会禁用输出驱动器和输入施密特触发器，以防止施加模拟信号时的寄生交叉电流。无论相关CEPD.q位的状态如何，选择具有CEIPSEL或CEIMSEL位的比较器多路复用器的C1.q输入引脚都会自动禁用该引脚的输出驱动器和输入缓冲器。

6.12.15端口P6（P6.2至P6.5）带施密特触发器的输入/输出

端口图如图6-11所示。表6-76总结了引脚功能的选择。




仅限功能表示。

**Figure 6-11. Py.x/USCI/Cp.q Pin Diagram**

表6-76。端口P6（P6.2至P6.5）引脚功能

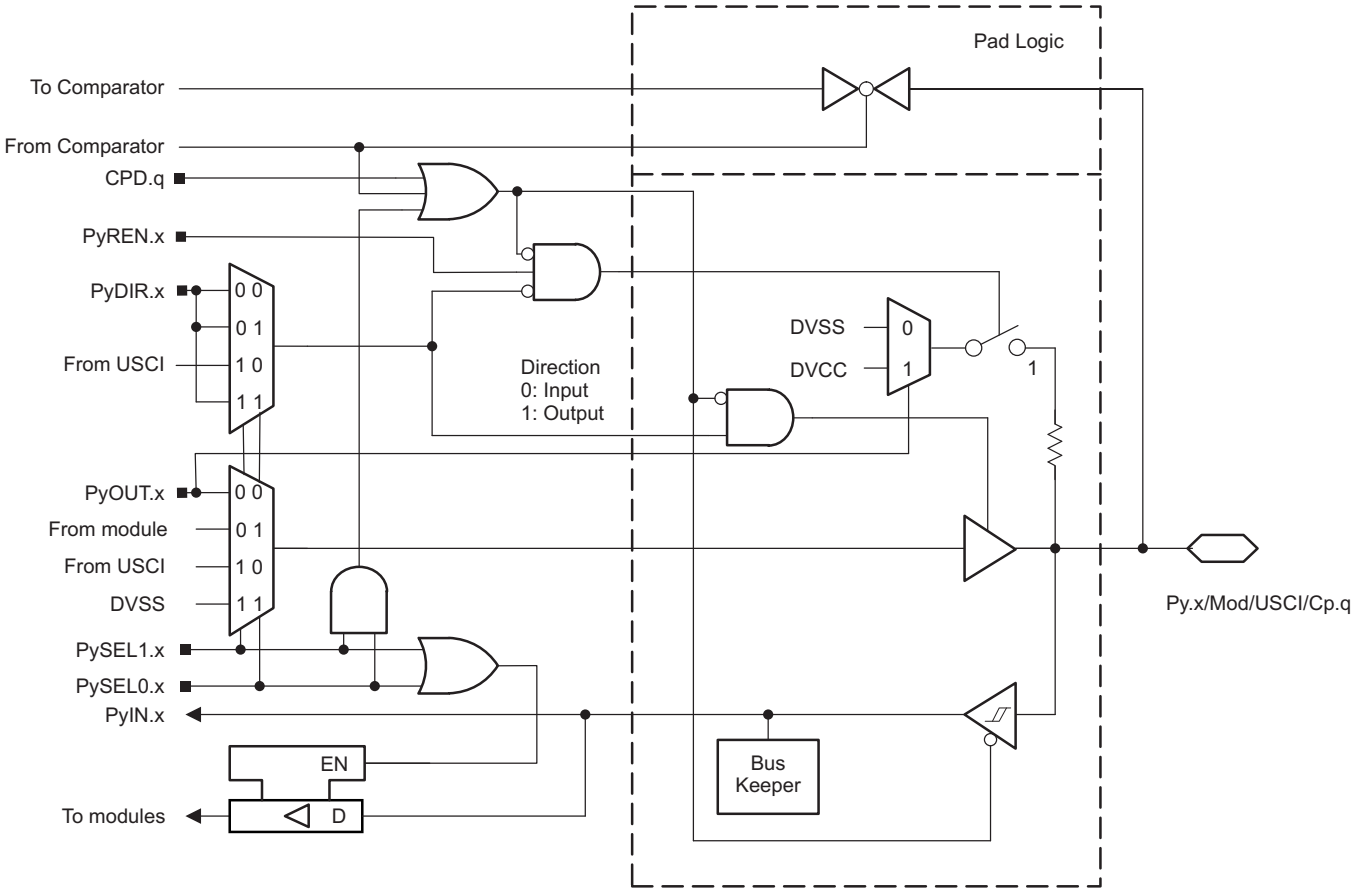
| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P6DIR.x | P6SEL1.x | P6SEL0.x |
| P6.2/UCB1STE/C1.5(2) | 2 | P6.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB1STE | X(3) | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | C1.5(4)(5) | X | 1 | 1 |
| P6.3/UCB1CLK/C1.4(2) | 3 | P6.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB1CLK | X(3) | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | C1.4(4)(5) | X | 1 | 1 |
| P6.4/UCB1SIMO/UCB1SDA/C1.3(2) | 4 | P6.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB1SIMO/UCB1SDA | X(3) | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | C1.3(4)(5) | X | 1 | 1 |
| P6.5/UCB1SOMI/UCB1SCL/C1.2(2) | 5 | P6.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB1SOMI/UCB1SCL | X(3) | 0 | 1 |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | C1.2(4)(5) | X | 1 | 1 |

(1) X = don't care
（2）不适用于64引脚RGC封装
（3）方向由eUSCI_B1模块控制
（4）设置P6SEL1.x和P6SEL0.x禁用输出驱动器和输入施密特触发器，以防止施加模拟信号时的寄生交叉电流。

（5）将比较器的CEPD.q位置1会禁止输出驱动器和输入施密特触发器，以防止施加模拟信号时的寄生交叉电流。无论相关CEPD.q位的状态如何，选择具有CEIPSEL或CEIMSEL位的比较器多路复用器的C1.q输入引脚都会自动禁用该引脚的输出驱动器和输入缓冲器。

6.12.16端口P6（P6.6和P6.7）带施密特触发器的输入/输出

端口图如图6-12所示。表6-77总结了引脚功能的选择。




仅限功能表示。

图6-12。 Py.x / Mod / USCI / Cp.q引脚图

表6-77。端口P6（P6.6和P6.7）引脚功能

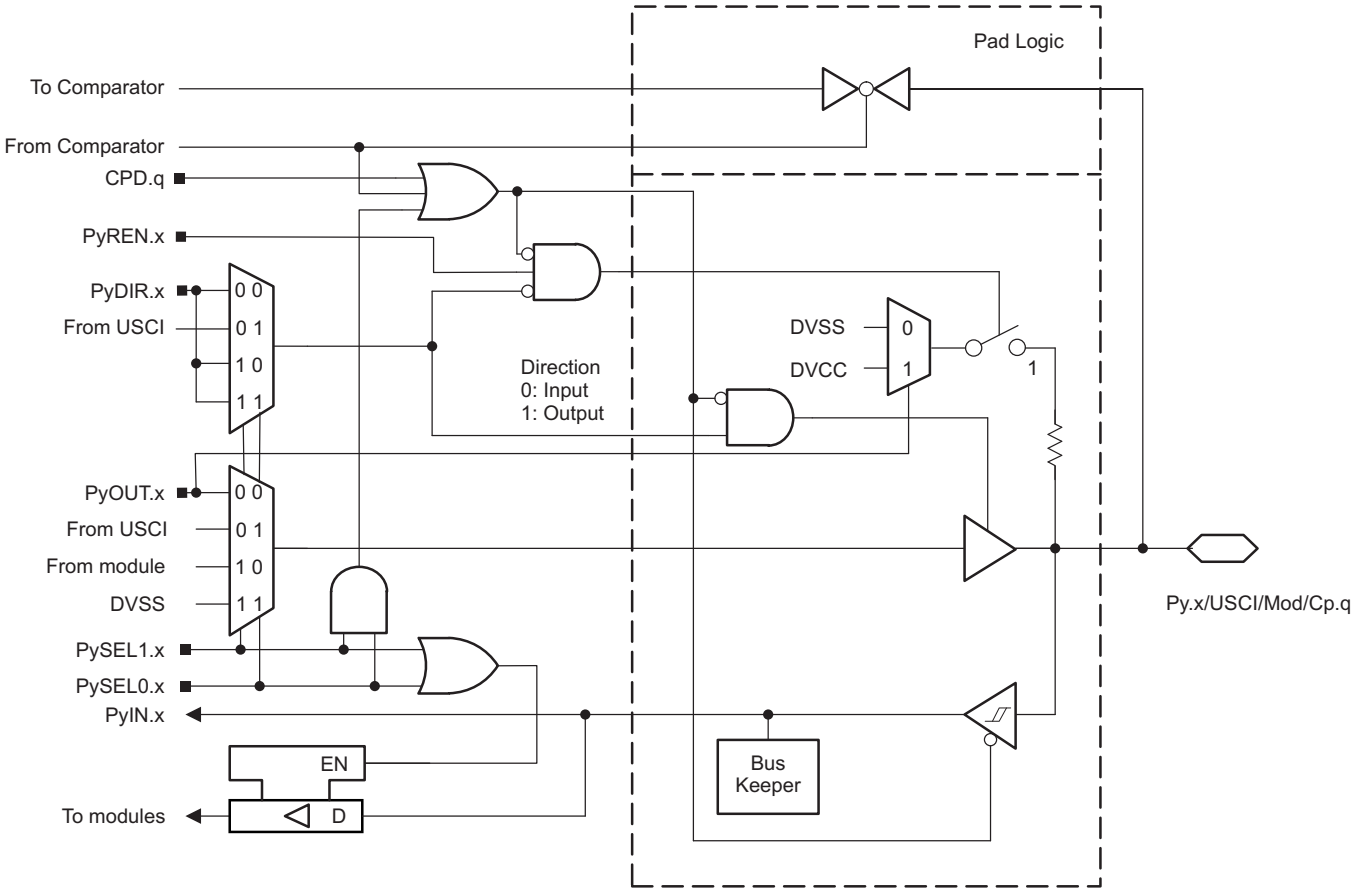
| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P6DIR.x | P6SEL1.x | P6SEL0.x |
| P6.6/TA2.3/UCB3SIMO/UCB3SDA/C1.1 | 6 | P6.6 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA2.CCI3A | 0 | 0 | 1 |
| | | TA2.3 | 1 | | |
| | | UCB3SIMO/UCB3SDA | X(2) | 1 | 0 |
| | | C1.1(3)(4) | X | 1 | 1 |
| P6.7/TA2.4/UCB3SOMI/UCB3SCL/C1.0 | 7 | P6.7 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA2.CCI4A | 0 | 0 | 1 |
| | | TA2.4 | 1 | | |
| | | UCB3SOMI/UCB3SCL | X(2) | 1 | 0 |
| | | C1.0(3)(4) | X | 1 | 1 |

(1) X = don't care
（2）方向由eUSCI_B3模块控制
（3）设置P6SEL1.x和P6SEL0.x禁用输出驱动器和输入施密特触发器，以防止施加模拟信号时的寄生交叉电流。

（4）将比较器的CEPD.q位置1会禁止输出驱动器和输入施密特触发器，以防止施加模拟信号时的寄生交叉电流。无论相关CEPD.q位的状态如何，选择具有CEIPSEL或CEIMSEL位的比较器多路复用器的C1.q输入引脚都会自动禁用该引脚的输出驱动器和输入缓冲器。

6.12.17端口P8（P8.0和P8.1）带施密特触发器的输入/输出

端口图如图6-13所示。表6-78总结了引脚功能的选择。




仅限功能表示。

图6-13。 Py.x / USCI / Mod / Cp.q引脚图

表6-78。端口P8（P8.0和P8.1）引脚功能

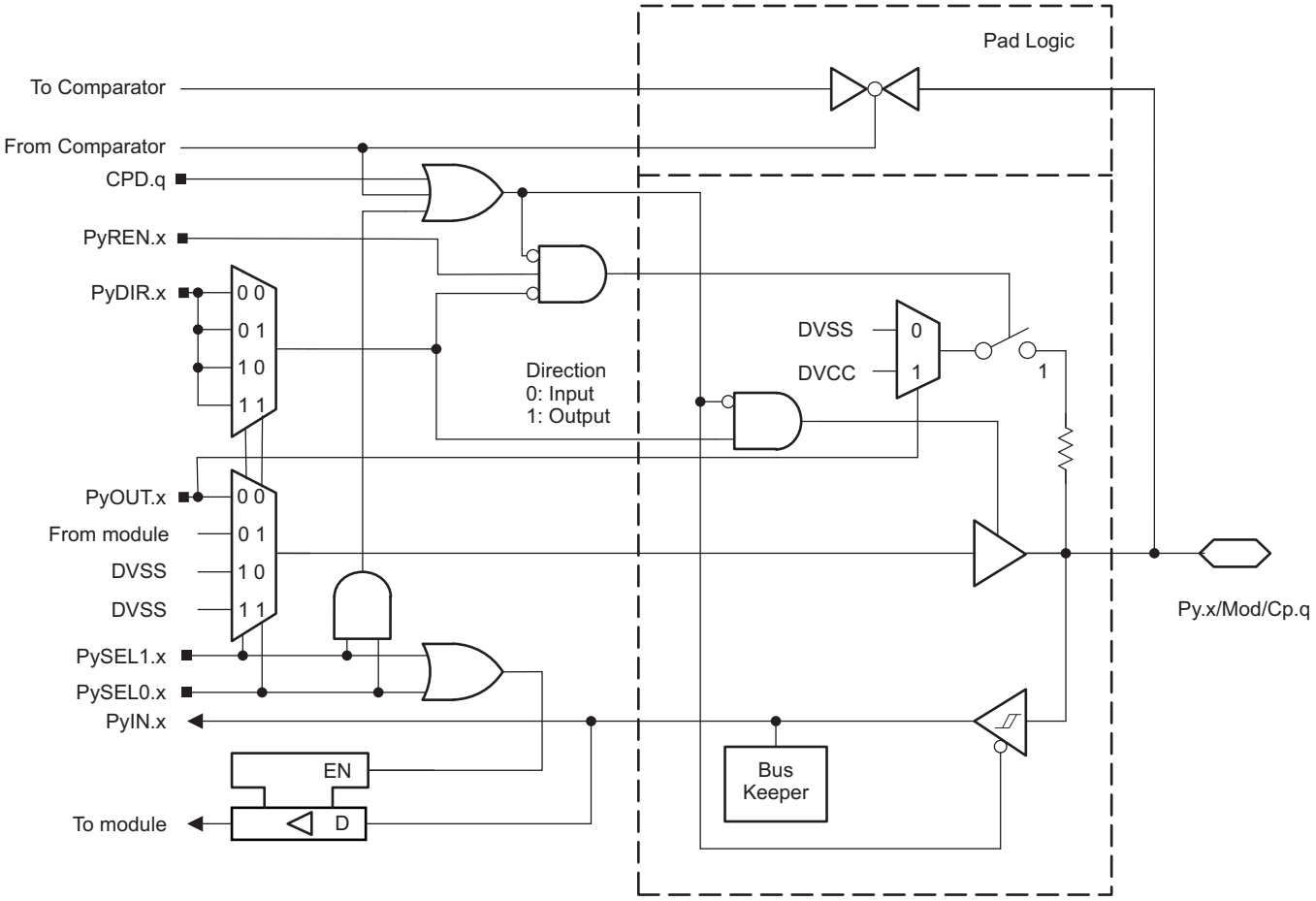
| PIN NAME (P8.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P8DIR.x | P8SEL1.x | P8SEL0.x |
| P8.0/UCB3STE/TA1.0/C0.1 | 0 | P8.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB3STE | X(2) | 0 | 1 |
| | | TA1.CCI0A | 0 | 1 | 0 |
| | | TA1.0 | 1 | | |
| | | C0.1(3)(4) | X | 1 | 1 |
| P8.1/UCB3CLK/TA2.0/C0.0 | 1 | P8.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB3CLK | X(2) | 0 | 1 |
| | | TA2.CCI0A | 0 | 1 | 0 |
| | | TA2.0 | 1 | | |
| | | C0.0(3)(4) | X | 1 | 1 |

(1) X = don't care
（2）方向由eUSCI_B3模块控制
（3）设置P8SEL1.x和P8SEL0.x禁用输出驱动器和输入施密特触发器，以防止施加模拟信号时的寄生交叉电流。

（4）将比较器的CEPD.q位置1会禁止输出驱动器和输入施密特触发器，以防止施加模拟信号时的寄生交叉电流。无论相关CEPD.q位的状态如何，选择具有CEIPSEL或CEIMSEL位的比较器多路复用器的C0.q输入引脚都会自动禁用该引脚的输出驱动器和输入缓冲器。

6.12.18端口P10（P10.4和P10.5）带施密特触发器的输入/输出

端口图如图6-14所示。表6-79总结了引脚功能的选择。




仅限功能表示。

**Figure 6-14. Py.x/Mod/Cp.q Pin Diagram**

表6-79。端口P10（P10.4和P10.5）引脚功能

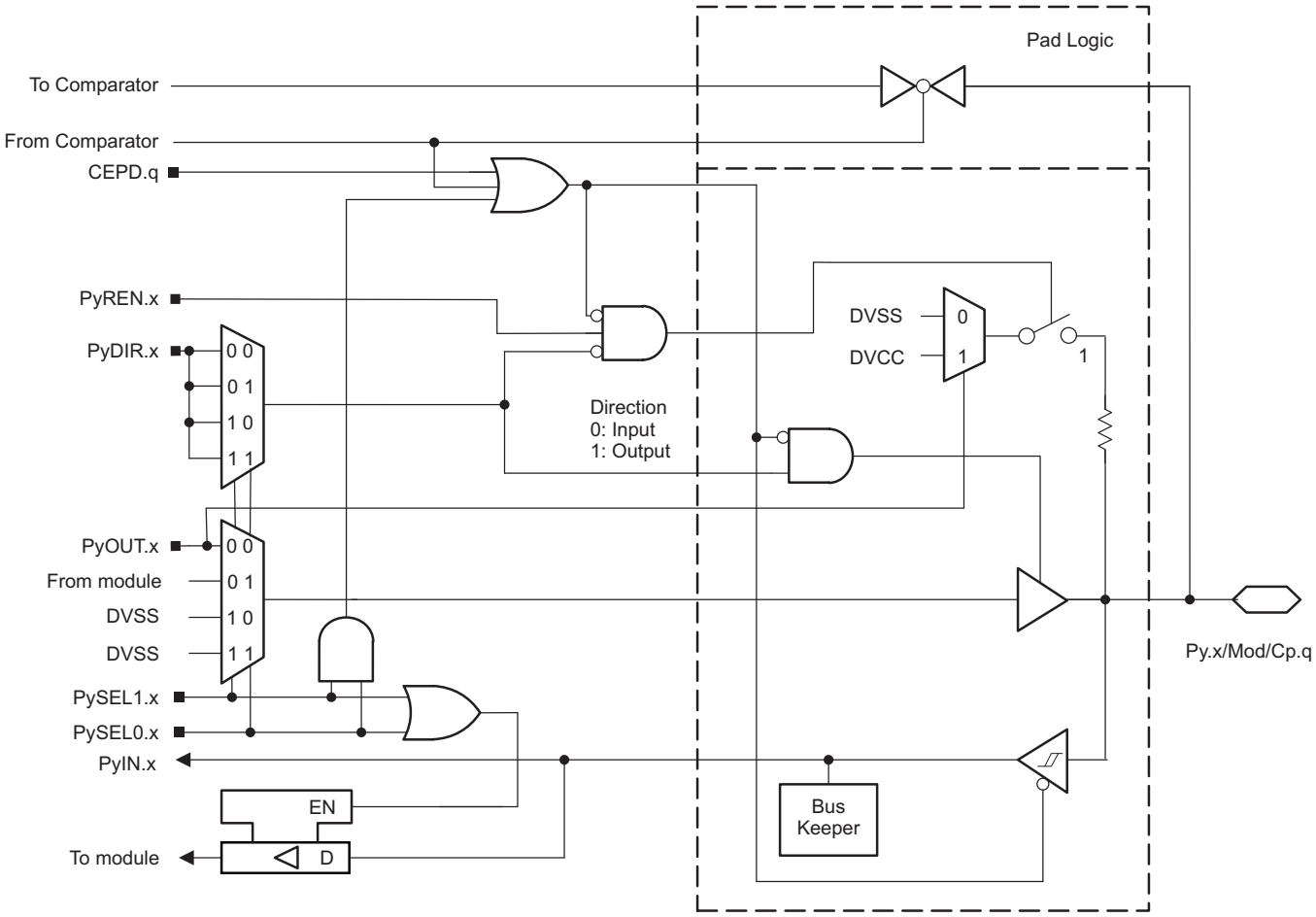
| PIN NAME (P10.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | |
|---|---|---|---|---|---|
| | | | P10DIR.x | P10SEL1.x | P10SEL0.x |
| P10.4/TA3.0/C0.7(2) | 4 | P10.4 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA3.CCI0A | 0 | 0 | 1 |
| | | TA3.0 | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | C0.7(3)(4) | X | 1 | 1 |
| P10.5/TA3.1/C0.6(2) | 5 | P10.5 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | TA3.CCI1A | 0 | 0 | 1 |
| | | TA3.1 | 1 | | |
| | | N/A | 0 | 1 | 0 |
| | | DVSS | 1 | | |
| | | C0.6(3)(4) | X | 1 | 1 |

(1) X = don't care
（2）不适用于80ZYH和64RGC封装
（3）设置P10SEL1.x和P10SEL0.x禁用输出驱动器和输入施密特触发器，以防止施加模拟信号时的寄生交叉电流。

（4）将比较器的CEPD.q位置1会禁止输出驱动器和输入施密特触发器，以防止施加模拟信号时的寄生交叉电流。无论相关CEPD.q位的状态如何，选择具有CEIPSEL或CEIMSEL位的比较器多路复用器的C0.q输入引脚都会自动禁用该引脚的输出驱动器和输入缓冲器。

6.12.19端口P7（P7.4至P7.7）带施密特触发器的输入/输出

端口图如图6-15所示。表6-80总结了引脚功能的选择。




仅限功能表示。

**Figure 6-15. Py.x/Mod/Cp.q Pin Diagram**

表6-80。端口P7（P7.4至P7.7）引脚功能

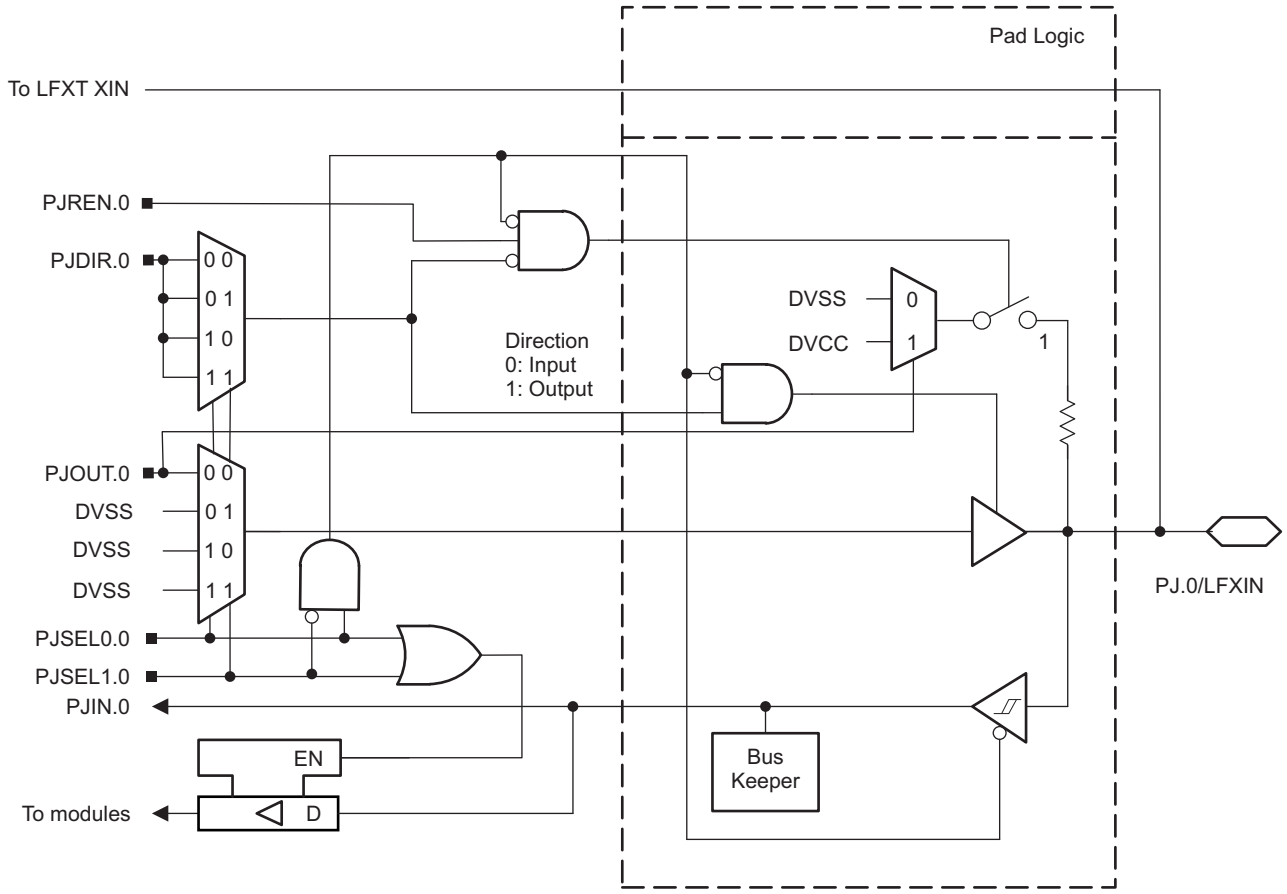
| PIN NAME (P7.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | | |
|---|---|---|---|---|---|---|
| | | | P7DIR.x | P7SEL1.x | P7SEL0.x | P7MAPx |
| P7.4/PM_TA1.4/C0.5(2) | 4 | P7.4 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | TA1.CCI4A | 0 | 0 | 1 | default |
| | | TA1.4 | 1 | | | |
| | | N/A | 0 | 1 | 0 | X |
| | | DVSS | 1 | | | |
| | | C0.5(3)(4) | X | 1 | 1 | X |
| P7.5/PM_TA1.3/C0.4(2) | 5 | P7.5 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | TA1.CCI3A | 0 | 0 | 1 | default |
| | | TA1.3 | 1 | | | |
| | | N/A | 0 | 1 | 0 | X |
| | | DVSS | 1 | | | |
| | | C0.4(3)(4) | X | 1 | 1 | X |
| P7.6/PM_TA1.2/C0.3(2) | 6 | P7.6 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | TA1.CCI2A | 0 | 0 | 1 | default |
| | | TA1.2 | 1 | | | |
| | | N/A | 0 | 1 | 0 | X |
| | | DVSS | 1 | | | |
| | | C0.3(3)(4) | X | 1 | 1 | X |
| P7.7/PM_TA1.1/C0.2(2) | 7 | P7.7 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | TA1.CCI1A | 0 | 0 | 1 | default |
| | | TA1.1 | 1 | | | |
| | | N/A | 0 | 1 | 0 | X |
| | | DVSS | 1 | | | |
| | | C0.2(3)(4) | X | 1 | 1 | X |

(1) X = don't care
（2）不适用于64引脚RGC封装
（3）设置P7SEL1.x和P7SEL0.x禁用输出驱动器和输入施密特触发器，以防止施加模拟信号时的寄生交叉电流。

（4）将比较器的CEPD.q位置1会禁止输出驱动器和输入施密特触发器，以防止施加模拟信号时的寄生交叉电流。无论相关CEPD.q位的状态如何，选择具有CEIPSEL或CEIMSEL位的比较器多路复用器的C0.q输入引脚都会自动禁用该引脚的输出驱动器和输入缓冲器。

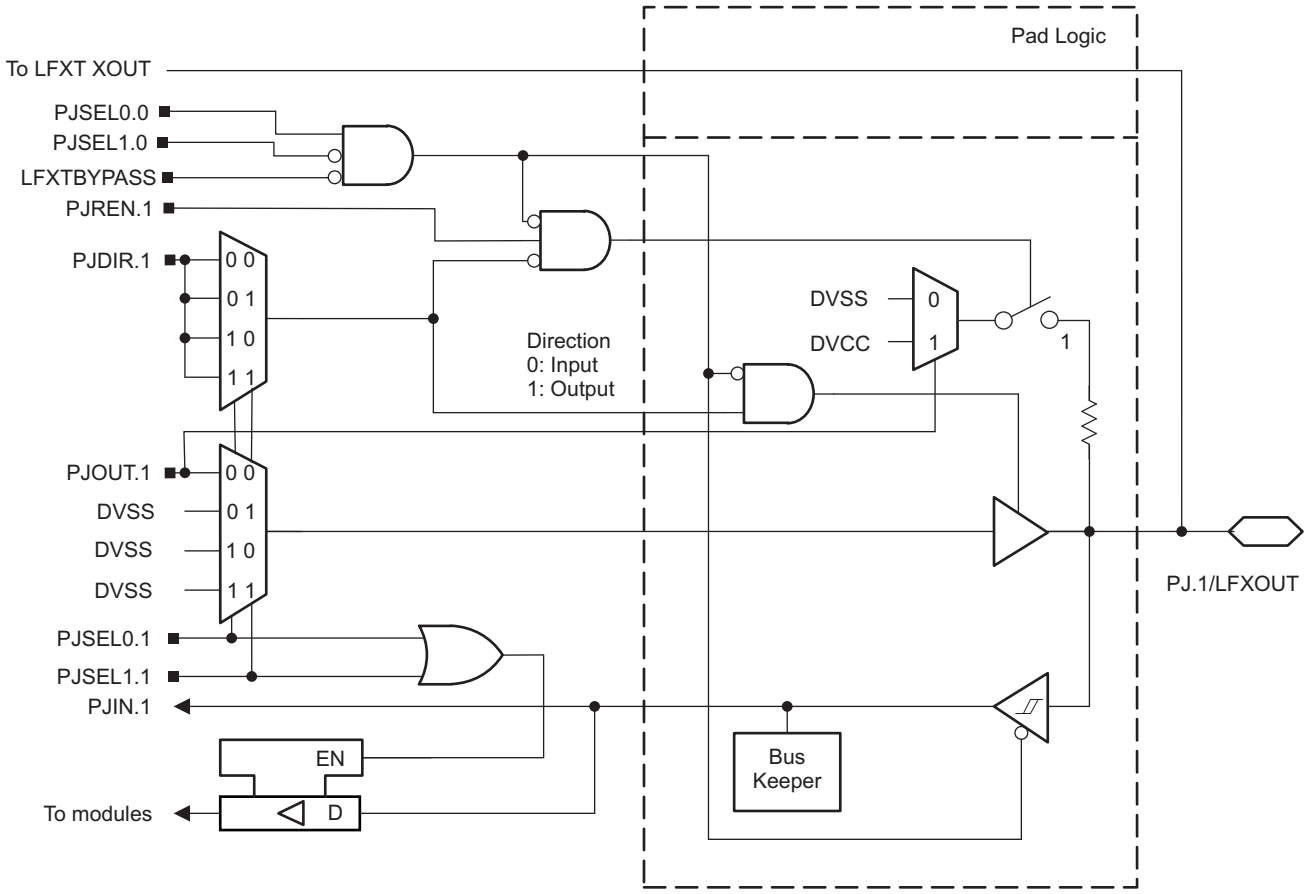
6.12.20端口PJ（PJ.0和PJ.1）带施密特触发器的输入/输出

端口图如图6-16和图6-17所示。表6-81总结了引脚功能的选择。




仅限功能表示。

**Figure 6-16. Port PJ (PJ.0) Diagram**




仅限功能表示。

**Figure 6-17. Port PJ (PJ.1) Diagram**

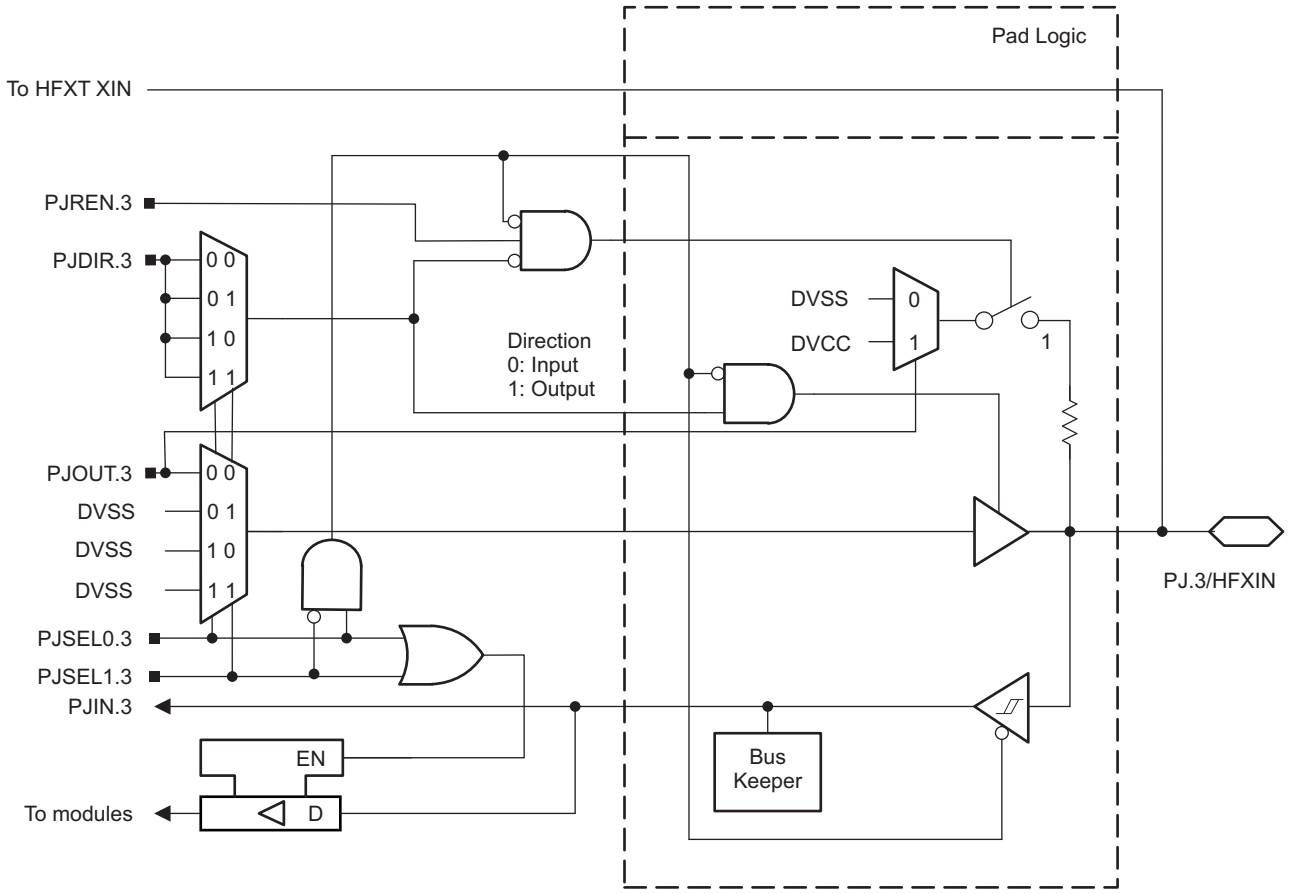
表6-81。端口PJ（PJ.0和PJ.1）引脚功能

| PIN NAME (PJ.x) | x | FUNCTION | CONTROL BITS OR SIGNALS (1) | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | PJDIR.x | PJSEL1.1 | PJSEL0.1 | PJSEL1.0 | PJSEL0.0 | LFXTBYPASS |
| PJ.0/LFXIN | 0 | PJ.0 (I/O) | I: 0; O: 1 | X | X | 0 | 0 | X |
| | | N/A | 0 | X | X | 1 | X | X |
| | | DVSS | 1 | | | | | |
| | | LFXIN crystal mode (2) | X | X | X | 0 | 1 | 0 |
| | | LFXIN bypass mode (2) | X | X | X | 0 | 1 | 1 |
| PJ.1/LFXOUT | 1 | PJ.1 (I/O) | I: 0; O: 1 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | 1 | X | |
| | | | | | | X | X | 1(3) |
| | | N/A | 0 | see(4) | see(4) | 0 | 0 | 0 |
| | | | | | | 1 | X | |
| | | | | | | X | X | 1(3) |
| | | DVSS | 1 | see(4) | see(4) | 0 | 0 | 0 |
| | | | | | | 1 | X | |
| | | | | | | X | X | 1(3) |
| | | LFXOUT crystal mode (2) | X | X | X | 0 | 1 | 0 |

(1) X = don't care
（2）设置PJSEL1.0 = 0且PJSEL0.0 = 1会导致通用I / O被禁用。当LFXTBYPASS = 0时，PJ.0和PJ.1配置为晶振操作，PJSEL1.1和PJSEL0.1无关紧要。当LFXTBYPASS = 1时，PJ.0配置为旁路操作，PJ.1配置为通用I / O。
（3）当PJ.0配置为旁路模式时，PJ.1配置为通用I / O
（4）当PJSEL0.1 = 1或PJSEL1.1 = 1时，禁用通用I / O功能。没有输入功能。当配置为输出时，引脚被主动拉至零。

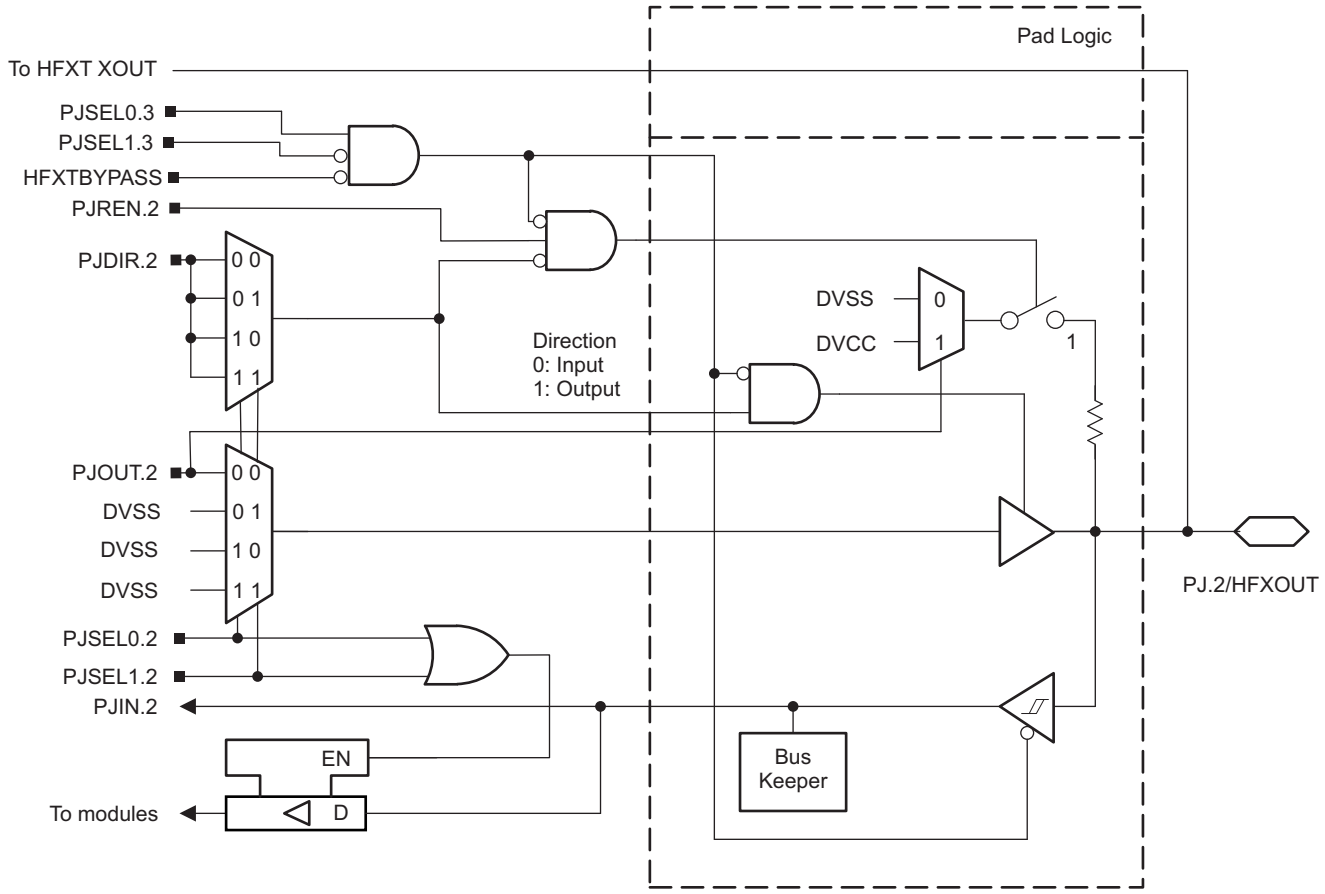
6.12.21端口PJ（PJ.2和PJ.3）带施密特触发器的输入/输出

端口图如图6-18和图6-19所示。表6-82总结了引脚功能的选择。




仅限功能表示。

**Figure 6-18. Port PJ (PJ.2) Diagram**




仅限功能表示。

**Figure 6-19. Port PJ (PJ.3) Diagram**

表6-82。端口PJ（PJ.2和PJ.3）引脚功能

| PIN NAME (PJ.x) | x | FUNCTION | CONTROL BITS OR SIGNALS (1) | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | PJDIR.x | PJSEL1.2 | PJSEL0.2 | PJSEL1.3 | PJSEL0.3 | HFXTBYPASS |
| PJ.3/HFXIN | 3 | PJ.3 (I/O) | I: 0; O: 1 | X | X | 0 | 0 | X |
| | | N/A | 0 | X | X | 1 | X | X |
| | | DVSS | 1 | | | | | |
| | | HFXIN crystal mode (2) | X | X | X | 0 | 1 | 0 |
| | | HFXIN bypass mode (2) | X | X | X | 0 | 1 | 1 |
| PJ.2/HFXOUT | 2 | PJ.2 (I/O) | I: 0; O: 1 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | 1 | X | |
| | | | | | | X | X | 1 (3) |
| | | N/A | 0 | see (4) | see (4) | 0 | 0 | 0 |
| | | | | | | 1 | X | |
| | | | | | | X | X | 1 (3) |
| | | DVSS | 1 | see (4) | see (4) | 0 | 0 | 0 |
| | | | | | | 1 | X | |
| | | | | | | X | X | 1 (3) |
| | | HFXOUT crystal mode (2) | X | X | X | 0 | 1 | 0 |

(1) X = don't care
（2）设置PJSEL1.3 = 0和PJSEL0.3 = 1会导致通用I / O被禁用。当HFXTBYPASS = 0时，PJ.2和PJ.3配置为晶振操作，PJSEL1.2和PJSEL0.2无关紧要。当HFXTBYPASS = 1时，PJ.3配置为旁路操作，PJ.2配置为通用I / O。
（3）当PJ.3配置为旁路模式时，PJ.2配置为通用I / O。
（4）当PJSEL0.2 = 1或PJSEL1.2 = 1时，禁用通用I / O功能。没有输入功能。当配置为输出时，引脚被主动拉至零。

## 6.12.22端口PJ（PJ.4和PJ.5）输入/输出，带施密特触发器

表6-83总结了引脚功能的选择。

表6-83。端口PJ（PJ.4至PJ.5）引脚功能

| PIN NAME (PJ.x) | x | FUNCTION | CONTROL BITS OR SIGNALS(1) | | | SWJ MODE OF OPERATION (1) |
|---|---|---|---|---|---|---|
| | | | PJDIR.x | PJSEL1.x | PJSEL0.x | |
| PJ.4/TDI (2) | 4 | PJ.4 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | TDI | X | 0 | 1 | JTAG (4 wire) |
| | | DVcc | | | | SWD (2 wire) |
| | | DVcc | X | 1 | X | X |
| PJ.5/TDO/SWO (3) | 5 | PJ.5 (I/O) | I: 0; O: 1 | 0 | 0 | X |
| | | TDO | X | 0 | 1 | JTAG (4 wire) |
| | | SWO | | | | SWD (2 wire) |
| | | Hi-Z | X | 1 | X | X |

（1）X表示控制信号或操作模式的值对功能没有影响。
（2）如果PJSEL0.x为1，则该引脚在内部上拉。
（3）在调试配置中使用时，必须通过外部下拉电阻将此引脚接地。

## 6.12.23具有施密特触发器的端口SWCLKTCK和SWDIOTMS

表6-84总结了引脚功能的选择。

表6-84。端口SWCLKTCK和SWDIOTMS引脚功能

| PIN NAME | FUNCTION | SWJ MODE OF OPERATION |
|---|---|---|
| SWCLKTCK (1) | TCK (input) | JTAG (4 wire) |
| | SWCLK (input) | SWD (2 wire) |
| SWDIOTMS (2) | TMS (input) | JTAG (4 wire) |
| | SWDIO (I/O) | SWD (2 wire) |

（1）该引脚内部拉至DVSS
（2）该引脚内部拉至DVCC。

## 6.13设备描述符（TLV）

表6-85总结了MSP432P401xx MCU的器件ID。表6-86列出了MSP432P401xx MCU的器件描述符标签长度值（TLV）结构的内容。

**Table 6-85. Device IDs**

| DEVICE | DEVICE ID |
|---|---|
| MSP432P401RIPZ | 0000A000h |
| MSP432P401MIPZ | 0000A001h |
| MSP432P401RIZXH | 0000A002h |
| MSP432P401MIZXH | 0000A003h |
| MSP432P401RIRGC | 0000A004h |
| MSP432P401MIRGC | 0000A005h |

**Table 6-86. Device Descriptor Table(1)**

| DESCRIPTION | | ADDRESS | VALUE |
|---|---|---|---|
| | TLV checksum | 00201000h | per unit |
| Info Block | Device Info Tag | 00201004h | 0000000Bh |
| | Device Info Length | 00201008h | 00000004h |
| | Device ID | 0020100Ch | See Table 6-85 |
| | Hardware Revision | 00201010h | per unit |
| | Boot-Code Revision | 00201014h | per unit |
| | ROM驱动程序库修订版00201018h每个单元 | | |
| Die Record | Die Record Tag | 0020101Ch | 0000000Ch |
| | Die Record Length | 00201020h | 00000008h |
| | Die X Position | 00201024h | per unit |
| | Die Y Position | 00201028h | per unit |
| | Wafer ID | 0020102Ch | per unit |
| | Lot ID | 00201030h | per unit |
| | Reserved | 00201034h | per unit |
| | Reserved | 00201038h | per unit |
| | Reserved | 0020103Ch | per unit |
| | Test Results | 00201040h | per unit |
| Clock System Calibration | 时钟系统校准标签00201044h 00000003h | | |
| | 时钟系统校准长度00201048h 00000010h | | |
| | DCO IR模式：DCORSEL的频率校准0至4 0020104Ch /单位 | | |
| | DCO IR模式：每单位DCORSEL 5 00201050h的频率校准 | | |
| | Reserved | 00201054h | not defined |
| | Reserved | 00201058h | not defined |
| | Reserved | 0020105Ch | not defined |
| | Reserved | 00201060h | not defined |
| | DCO IR模式：DCOR的DCO常数（K）0至4 00201064h每单位 | | |
| | DCO IR模式：每单位DCORSEL 5 00201068h的DCO常数（K） | | |
| | DCO ER模式：DCORSEL的频率校准0至4 0020106Ch /单位 | | |
| | DCO ER模式：每单位DCORSEL 5 00201070h的频率校准 | | |
| | Reserved | 00201074h | not defined |
| | Reserved | 00201078h | not defined |
| | Reserved | 0020107Ch | not defined |
| | Reserved | 00201080h | not defined |
| | DCO ER模式：DCOREL的DCO常数（K）0至4 00201084h /单位 | | |
| | DCO ER模式：每单位DCORSEL 5 00201088h的DCO常数（K） | | |

(1) per unit = content can differ from device to device

表6-86。设备描述符表（1）（续）

| DESCRIPTION | | ADDRESS | VALUE |
|---|---|---|---|
| ADC14 Calibration | ADC14校准标签00201080h 00000005h | | |
| | ADC14校准长度00201090h 00000018h | | |
| | Reserved | 00201094h | not defined |
| | Reserved | 00201098h | FFFFFFFFh |
| | Reserved | 0020109Ch | FFFFFFFFh |
| | Reserved | 002010A0h | FFFFFFFFh |
| | Reserved | 002010A4h | FFFFFFFFh |
| | Reserved | 002010A8h | FFFFFFFFh |
| | Reserved | 002010ACh | FFFFFFFFh |
| | Reserved | 002010B0h | FFFFFFFFh |
| | Reserved | 002010B4h | FFFFFFFFh |
| | Reserved | 002010B8h | FFFFFFFFh |
| | Reserved | 002010BCh | FFFFFFFFh |
| | Reserved | 002010C0h | FFFFFFFFh |
| | Reserved | 002010C4h | FFFFFFFFh |
| | Reserved | 002010C8h | FFFFFFFFh |
| | Reserved | 002010CCh | FFFFFFFFh |
| | Reserved | 002010D0h | FFFFFFFFh |
| | Reserved | 002010D4h | FFFFFFFFh |
| | Reserved | 002010D8h | not defined |
| | ADC 1.2V参考温度传感器每单位30° C 002010DCh | | |
| | ADC 1.2V参考温度传感器每单位85° C 002010E0h | | |
| | ADC 1.45-V参考温度传感器每单位30° C 002010E4h | | |
| | ADC 1.45-V参考温度传感器每单位85° C 002010E8h | | |
| | ADC 2.5V参考温度传感器每单位30° C 002010ECh | | |
| | ADC 2.5V基准温度传感器每单位85° C 002010F0h | | |
| REF Calibration | REF Calibration Tag | 002010F4h | 00000008h |
| | REF校准长度002010F8h 00000003h | | |
| | Reserved | 002010FCh | not defined |
| | Reserved | 00201100h | not defined |
| | Reserved | 00201104h | not defined |
| Flash Info | Flash Info Tag | 00201108h | 00000004h |
| | Flash Info Length | 0020110Ch | 00000002h |
| | 闪存最大编程脉冲00201110h 00000005h | | |
| | 闪存最大擦除脉冲00201114h 0000014Eh | | |
| Random Number | 128-Bit Random Number Tag | 00201118h | 0000000Dh |
| | Random Number Length | 0020111Ch | 00000004h |
| | 128-Bit Random Number(2) | 00201120h | per unit |
| | | 00201124h | per unit |
| | | 00201128h | per unit |
| | | 0020112Ch | per unit |
| BSL Configuration | BSL配置标签00201130h 0000000Fh | | |
| | BSL配置长度00201134h 00000004h | | |
| | BSL外设接口选择00201138h FFC2D0C0h | | |
| | UART 0020113Ch FCFFFDA0h的BSL端口接口配置 | | |
| | SPI 00201140h F0FF9770h的BSL端口接口配置 | | |
| | I2C 00201144h FCFFFF72h的BSL端口接口配置 | | |
| TLV End | TLV End Word | 00201148h | 0BD0E11Dh |
| | Reserved | 0020114Ch-00201FFFh | FFFFFFFFh |

（2）128位随机数：使用Microsoft®的CryptGenRandom（）函数在生产测试期间生成随机数。

# 6.14识别

## 6.14.1修订标识

设备修订信息显示为设备包上的顶部标记的一部分。特定于设备的勘误表描述了这些标记。有关本数据手册中器件的勘误表的链接，请参见第8.4节。

硬件版本也存储在“信息块”部分的“设备描述符”结构中。有关此值的详细信息，请参见器件描述符结构中的硬件版本条目（参见第6.13节）。

## 6.14.2设备识别

可以从设备包装上的顶侧标记识别设备类型。特定于设备的勘误表描述了这些标记。有关本数据手册中器件的勘误表的链接，请参见第8.4节。

设备标识值也存储在信息块部分的设备描述符结构中。有关此值的详细信息，请参阅器件描述符结构中的器件ID条目（参见第6.13节）。

## 6.14.3基于ARM Cortex-M4F ROM表的部件号

除了器件描述符（TLV）中指定的器件ID之外，MSP432P4xx系列MCU还包含器件的部件号，供IDE识别器件。本节介绍如何在设备上组织此信息。

IEEE 1149.1定义了在JTAG链中使用IDCODE寄存器来提供表6-87中的字段

表6-87。设备识别码的结构

| Bit Position | Field Description |
|---|---|
| 31-28 | Version |
| 27-12 | Part Number of the device |
| 11-1 | Manufacturer Identity |
| 0保留（始终绑定到1） | |

在MSP432P4xx MCU上，所有这些字段都在ARM Cortex-M4 ROM表上实现。可以通过IDE工具（TI内部或第三方）读取部件号以确定设备。图6-20显示了ARM Cortex-M4规范中的外设ID寄存器位描述。有关ARM Cortex-M4外设ID寄存器的位级详细信息，请参阅ARM调试接口V5架构规范。

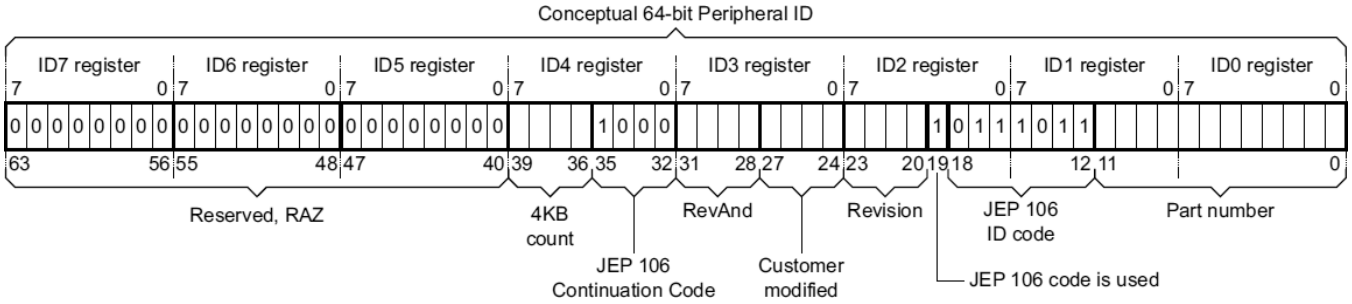



图6-20。 ARM Cortex-M4外设ID寄存器说明

图6-20显示了表6-87中的以下字段无法进行一对一映射

1. 版本：IEEE 1149.1定义了一个4位字段，其中Coresight兼容PID寄存器有4位 each for Revision (major revision) and RevAnd (minor revision)

2. 部件号。IEEE 1149.1定义了一个16位实体。但是，ROM表中的PID寄存器有仅为此目的保留12位（部件号 – PID1和PID0寄存器）。

对于MSP432P4xx

MCU，Revision和RevAnd字段用于跟踪主要和次要修订。客户修改（4位）字段也用于将部件号扩展到16位，以适应ROM表中IEEE 1149.1所需的所有字段。

例如，MSP432P401xx MCU的带有IEEE 1149.1投诉设备IDCODE的ROM表是0000-1011-1001-1010-1111-0000-0010-1111（见图6-21）。

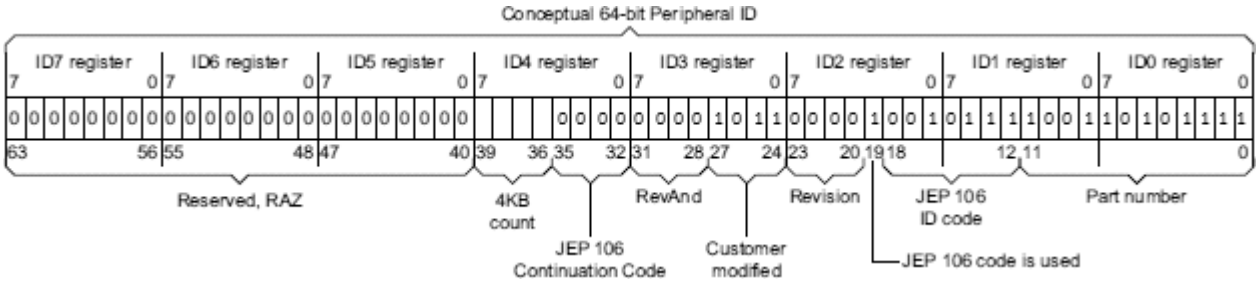



图6-21。 MSP432P401xx MCU的ROM PID条目示例

# 7应用程序，实现和布局

**NOTE**

以下“应用”部分中的信息不是TI组件规范的一部分，TI不保证其准确性或完整性。TI的客户负责确定组件的适用性。客户应验证并测试其设计实现以确认系统功能。

## 7.1设备连接和布局基础知识

本节讨论使用MSP432微控制器进行设计时的建议指南。

这些指南旨在确保器件具有适当的连接，以便进行供电，编程，调试和最佳模拟性能。

### 7.1.1电源去耦和大容量电容器

TI建议将4.7 µ F和100 nF低ESR陶瓷去耦电容的组合连接到每个AVCC和DVCC引脚（见图7-1）。可以使用更高值的电容器，但会影响电源轨的上升时间。去耦电容必须尽可能靠近它们去耦的引脚（几毫米内）。此外，TI建议采用单点连接的分离式接地，以便更好地隔离电路板上的数字到模拟电路，并实现高模拟精度。

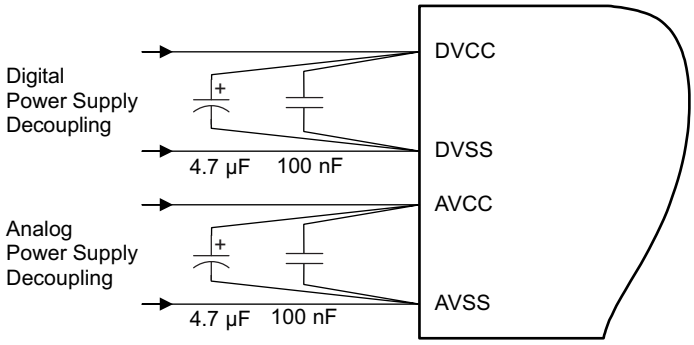



**Figure 7-1. Power Supply Decoupling**

### 7.1.2外部振荡器

该器件支持LFXT引脚上的低频晶振（32.768 kHz）和HFXT引脚上的高频晶振。需要外部旁路电容用于晶体振荡器引脚。

如果选择了适当的LFXTBYPASS或HFXTBYPASS模式，也可以将数字时钟信号应用于符合相应振荡器规格的LFXIN和HFXIN输入引脚。在这种情况下，相关的LFXOUT和HFXOUT引脚可用于其他目的。

图7-2显示了典型的连接图。

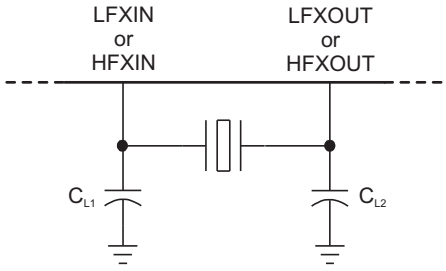



**Figure 7-2. Typical Crystal Connection**

有关使用MSP432器件选择，测试和设计晶体振荡器的更多信息，请参见MSP430 32 kHz晶体振荡器。

### 7.1.3一般布局建议

•外部晶体的正确接地和短走线，以减少寄生电容。有关推荐的布局指南，请参见MSP430 32 kHz晶体振荡器。
•DVCC，AVCC和参考引脚（如果使用）上的正确旁路电容。
•避免在模拟信号线附近布设任何高频信号。例如，保持数字开关信号（例如PWM或JTAG信号）远离振荡器电路。

•有关印刷电路板（PCB）布局注意事项的详细讨论，请参阅电路板布局技术。本文档主要是关于运算放大器编写的，但该指南通常适用于所有混合信号应用。
•应考虑采用适当的ESD电平保护，以保护器件免受意外的高压静电放电。有关指南，请参阅MSP430系统级ESD注意事项。

### 7.1.4做与不做

TI建议从同一电源为AVCC和DVCC引脚供电。至少在上电，断电和设备运行期间，AVCC和DVCC之间的电压差不得超过绝对最大额定值中规定的限值。超过指定的限制可能会导致设备故障。

## 7.2外设和接口特定的设计信息

### 7.2.1 ADC14外设

#### 7.2.1.1部分原理图

图7-3显示了ADC14外部连接的部分原理图。

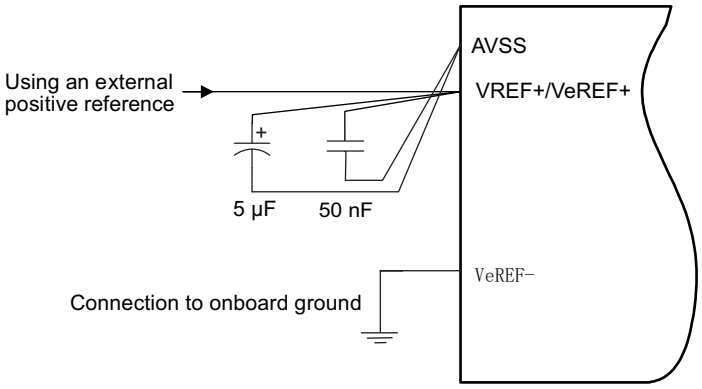



图7-3。 ADC14接地和噪声考虑因素

#### 7.2.1.2设计要求

与任何高分辨率ADC一样，应遵循适当的PCB布局和接地技术，以消除接地环路，不必要的寄生效应和噪声。

当来自ADC的返回电流流过与其他模拟或数字电路共用的路径时，形成接地回路。如果不小心，该电流可以产生较小的不需要的偏移电压，可以增加或减少ADC的参考电压或输入电压。第7.1.1节中的一般准则与第7.2.1.1节中所示的连接相结合可防止这种情况发生。

除了接地之外，由数字开关或开关电源引起的电源线上的纹波和噪声尖峰可能会破坏转换结果。建议使用单独模拟和数字接地层以及单点连接的无噪声设计，以实现高精度。

图7-3显示了使用外部参考电压时推荐的去耦电路。

参考电压必须是稳定的电压才能进行精确测量。在参考电压进入器件之前，通用指南中选择的电容值会滤除高频和低频纹波。在这种情况下，5 µ F电容用于缓冲参考引脚并滤除任何低频纹波。 50 nF旁路电容用于滤除任何高频噪声。

### 7.2.1.3布局指南

部分原理图中显示的元件（见图7-3）应尽可能靠近相应的器件引脚放置。避免长迹线，因为它们会在信号上增加额外的寄生电容，电感和电阻。

避免将模拟输入信号布设在靠近高频引脚（例如，高频PWM）的位置，因为高频开关可以耦合到模拟信号中。

如果ADC14使用差分模式，则模拟差分输入信号必须靠近在一起，以最大限度地降低噪声对结果信号的影响。

# 8设备和文档支持

## 8.1入门和后续步骤

有关MSP432系列微控制器以及可用于开发的工具和库的更多信息，请访问MSP432P4x入门。

## 8.2设备和开发工具命名法

为了指定产品开发周期中的各个阶段，TI为所有MSP432
MCU器件和支持工具的器件编号分配了前缀。每个MSP432
MCU商用系列成员都有三个前缀之一：MSP，PMS或XMS（例如，MSP432P401R）。
TI为其支持工具推荐了三种可能的前缀指示符中的两种：MSP和MSPX。这些前缀代表了从工程原型（使用设备的XMS和工具的MSPX）到完全合格的生产设备和工具（MSP用于设备和MSP用于工具）的产品开发的演进阶段。

设备开发演化流程：

XMS – 不一定代表最终设备电气规格的实验设备

PMS – 最终硅片，符合器件的电气规范，但尚未完成质量和可靠性验证

**MSP** – Fully qualified production device

支持工具开发演化流程：

MSPX – 尚未完成德州仪器内部认证测试的开发支持产品。

MSP – 完全合格的开发支持产品

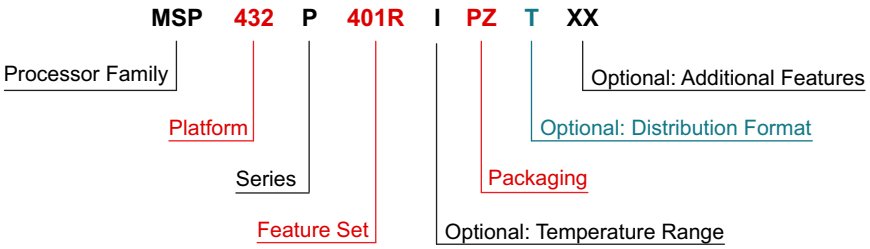
XMS和PMS设备以及MSPX开发支持工具是根据以下免责声明提供的：

"Developmental product is intended for internal evaluation purposes."

MSP设备和MSP开发支持工具已经完全表征，并且已经充分展示了设备的质量和可靠性。
TI的标准保修适用。

预测表明，原型设备（XMS和PMS）的故障率高于标准生产设备。德州仪器（TI）建议不要在任何生产系统中使用这些设备，因为它们的预期最终使用故障率仍未定义。只能使用合格的生产设备。

TI器件命名法还包括带有器件系列名称的后缀。该后缀表示封装类型（例如，PZP）和温度范围（例如，T）。图8-1提供了读取任何系列成员的完整设备名称的图例。




| | | | | |
|---|---|---|---|---|
| **Processor Family** | MSP = Mixed-Signal Processor<br>XMS = Experimental Silicon | | | |
| **Platform** | 432 = TI's 32-Bit Low-Power Microcontroller Platform | | | |
| **Series** | P = Performance and Low-Power Series | | | |
| **Feature Set** | **First Digit**<br>4 = Flash-based devices up to 48 MHz | **Second Digit**<br>0 = General purpose | **Third Digit**<br>1 = ADC14 | **Fourth Digit**<br>R = 256KB of flash 64KB of SRAM<br>M = 128KB of flash 32KB of SRAM |
| **Optional: Temperature Range** | S = 0°C to 50°C<br>I = –40°C to 85°C<br>T = –40°C to 105°C | | | |
| **Packaging** | http://www.ti.com/packaging | | | |
| **Optional: Distribution Format** | T = Small reel<br>R = Large reel<br>No markings = Tube or tray | | | |
| **Optional: Additional Features** | -EP = Enhanced Product (–40°C to 105°C)<br>-HT = Extreme Temperature Parts (–55°C to 150°C)<br>-Q1 = Automotive Q100 Qualified | | | |

**Figure 8-1. Device Nomenclature**

## 8.3工具和软件

所有MSP432微控制器都支持各种软件和硬件开发工具。
TI和各种第三方提供工具。在TI 32位MSP432微控制器上查看所有这些内容。
表8-1列出了支持的调试功能。有关可用硬件功能的详细信息，请参阅Code Composer Studio™IDE 7.1+以获取SimpleLink™MSP432™微控制器用户指南。请参阅使用增强型仿真模块（EEM）进行高级调试，使用Code Composer Studio版本6和MSP高级功耗优化：ULP
Advisor™和EnergyTrace™技术，以获取更多用途信息。

**Table 8-1. Hardware Debug Features**

| FAMILY | JTAG | SWD | NUMBER OF BREAKPOINTS | ITM | DWT | FPB |
|---|---|---|---|---|---|---|
| MSP432P4xx | Yes | Yes | 6 | Yes | Yes | Yes |

Code Composer Studio 6.0及更高版本支持EnergyTrace技术。它需要专门的调试器电路，MSP432 LaunchPad开发套件，XDS110独立调试探针和第二代独立MSP-FET
JTAG仿真器支持该电路。有关更多详细信息，请参阅MSP高级功耗优化：ULP
Advisor™和EnergyTrace™技术，用于SimpleLink™MSP432™微控制器的Code Composer Studio™IDE 7.1+用户指南和MSP432™SimpleLink™微控制器硬件工具用户指南。

### Design Kits and Evaluation Modules

**MSP432P401R LaunchPad开发套件** MSP432P401R LaunchPad开发套件支持您需要开发受益于低功耗操作的高性能应用程序。该套件采用MSP432P401R MCU，包括48 MHz ARM Cortex M4F，80-µA/ MHz有源功率，660-nA待机和RTC操作，14位1 MSPS差分SAR ADC，最高16位ENOB和AES256加速器。

**100-Pin Target Development Board for MSP432P4x MCUs** The MSP-TS432PZ100 is a stand-alone ZIF 套接字目标板，用于通过JTAG接口或串行线调试（SWD 2线JTAG）协议对系统内的MSP432进行编程和调试。该开发板支持采用100引脚LQFP封装（TI封装代码：PZ）的所有MSP432P4xx闪存器件。

### Software

**SimpleLink MSP432软件开发套件（SDK）** SimpleLink MSP432 SDK是一个全面的软件包，使工程师能够在MSP432 MCU上快速开发功能强大的应用程序。SDK由多个兼容的软件组件组成，包括RTOS，驱动程序和中间件，以及如何将这些组件一起使用的示例。此外，还提供了一些示例来演示每个功能区域和每个支持的设备的使用，并作为您自己项目的起点。 SimpleLink MSP432 SDK是TI SimpleLink平台的一部分，可在SimpleLink MCU之间实现100％的代码重用。

**用于MSP432微控制器的RTOS** MSP432 MCU提供与多个TI和第三方的兼容性实时操作系统（RTOS）。请访问此链接，了解每个主要功能以满足您的设计需求。

### Development Tools

**适用于MSP微控制器代码的Code Composer Studio集成开发环境** Composer Studio是一个集成开发环境（IDE），支持所有MSP微控制器设备。 Code Composer Studio包含一套用于开发和调试嵌入式应用程序的嵌入式软件实用程序。它包括优化的C / C ++编译器，源代码编辑器，项目构建环境，调试器，分析器和许多其他功能。有关更多信息，请参阅Code Composer Studio™IDE 7.1+以获取SimpleLink™MSP432™微控制器用户指南。

**ARM® Keil® MDK – Free 32KB IDE** The ARM Keil MDK is a complete debugger and C/C++ compiler 用于构建和调试嵌入式应用程序的工具链。 Keil MDK支持低功耗和高性能MSP432 MCU系列，并包含一个完全集成的调试器，用于源和反汇编级调试，支持复杂的代码和数据断点。有关更多信息，请参阅“用于SimpleLink™MSP432™微控制器的ARM ®Keil®MDK第5版用户指南”。

**IAR Embedded Workbench® Kickstart** IAR Embedded Workbench Kickstart for MSP is a complete 调试器和C / C ++编译器工具链，用于构建和调试基于MSP430和MSP432微控制器的嵌入式应用程序。对于MSP432器件，C / C ++编译器的代码大小限制设置为32KB。有关更多信息，请参阅用于ARM®7.x的IAREmbeddedWorkbench®for SimpleLink™MSP432™微控制器用户指南。

**Debuggers for MSP432 Microcontrollers** MSP432 MCUs are designed to work with a variety of 德州仪器（TI）和第三方供应商的调试器。

**MSP EnergyTrace技术用于MSP430微控制器的EnergyTrace技术是一种能源 –** 基于代码分析的工具，可测量和显示应用的能量曲线，并有助于优化它以实现超低功耗。

**MSP MCU编程器和调试器MSP-FET是一种功能强大的仿真开发工具 – 通常** 称为调试探针 – 允许用户在MSP低功耗微控制器上快速开始应用程序开发。

**MSP-GANG生产编程器MSP Gang编程器是MSP430和MSP432器件** 编程器，可以同时编程多达8个相同的MSP430或MSP432闪存或FRAM器件。 MSP Gang Programmer使用标准RS-232或USB连接连接到主机PC，并提供灵活的编程选项，允许用户完全自定义过程。

引脚复用工具引脚MUX工具是一个软件工具，提供图形用户界面configuring pin multiplexing settings resolving conflicts and specifying I/O cell TI
MPU的特性。结果输出为C头和代码文件，可以导入软件开发工具包或用于配置客户的自定义软件。Pin Mux实用程序的第3版可以自动选择满足用户输入要求的mux配置。

ULP（超低功耗）顾问ULP（超低功耗）顾问是指导开发人员编写的工具
更高效的代码，充分利用MSP和MSP432微控制器独特的超低功耗特性。针对经验丰富的新型微控制器开发人员，ULP
Advisor会根据完整的ULP检查表检查您的代码，以便从您的应用程序中挤出每一个纳米放大器。

## 8.4文档支持

以下文档描述了MSP430P401x MCU。这些文档的副本可在TI网站上获得。

### 接收文档更新通知

要接收文档更新通知（包括芯片勘误表），请访问ti.com上设备的产品文件夹（有关产品文件夹的链接，请参阅第8.5节）。在右上角，单击“提醒我”按钮。这会使您注册接收已更改的产品信息的每周摘要（如果有）。有关更改详细信息，请查看任何修订文档的修订历史记录。

**Errata**

MSP432P401R器件说明书描述了功能规范的已知例外情况
该器件的每个芯片版本。

MSP432P401M器件说明书描述了功能规范的已知例外情况
该器件的每个芯片版本。

**User's Guides**

MSP432P4xx SimpleLink™微控制器技术参考手册详细说明
该器件系列中提供的模块和外设。

适用于SimpleLink™MSP432™微控制器的Code Composer Studio™IDE 7.1+用户指南
手册描述了TI Code Composer Studio
IDE（CCS）7.1及更高版本与MSP432低功耗微控制器的使用。

用于SimpleLink™MSP432™微控制器的IAR Embedded Workbench for ARM 7.x用户指南
本手册介绍了使用IAR Embedded Workbench for
ARM（EWARM）7.x版和MSP432低功耗微控制器。

适用于SimpleLink™MSP432™微控制器的ARM®Keil®MDK第5版用户指南此用户指南
指南描述了ARM Keil MDK版本5与MSP432低功耗微控制器的使用。

用于SimpleLink™MSP432™微控制器的GCC ARM®嵌入式工具链用户指南
手册介绍了使用GCC ARM编译器和GDB调试器进行MSP432编程和调试的设置和基本操作。

MSP432™SimpleLink™微控制器引导加载程序（BSL）用户指南MSP432 BSL支持
用户在原型设计阶段，最终生产和使用中与MSP432微控制器中的嵌入式存储器进行通信。可编程存储器（闪存）和数据存储器（RAM）都可以根据需要进行修改。

MSP432电容式触摸软件库程序员指南MSP432微控制器具
配备执行电容测量所需的外围设备。电容式触摸软件库的目的是创建一个可与MSP432器件中的外设集成的单一接口。本文档介绍了电容式触摸库的配置以及与MSP432器件的配合使用。

### Application Reports

**Platform Migration to SimpleLink™ MSP432™ Microcontrollers** The goals for this migration guide are to help developers accurately assess the effort to port an existing application from one MSP platform to another, and ultimately to derive a porting strategy with complete hardware and software coverage that properly ports the existing application without introducing bugs due to platform differences yet that takes advantages of the unique features or performance improvements in the new platform.

**Designing an Ultra-Low-Power (ULP) Application With SimpleLink™ MSP432™ Microcontrollers** With the growing system complexity in ultra-low-power microcontroller applications, minimizing the overall energy consumption is one of the most difficult problems to solve. Multiple aspects including silicon, other onboard hardware components, and application software must be considered. There are some obvious generic techniques that can be used to reduce energy consumption such as reducing operating voltage or frequency. Many of these generic techniques may not greatly reduce energy consumption independently, but taken as a whole, the results can be significant, as there are many interdependencies across these components.

**Maximizing MSP432P4xx Voltage Regulator Efficiency** This application report describes the relationship of the DC-DC and LDO voltage regulators on the MSP432P4xx MCU, provides guidelines on choosing which is most efficient for your application, and gives board layout considerations for the DC-DC.

**Leveraging Low-Frequency Power Modes on SimpleLink™ MSP432P4xx Microcontrollers** Low power consumption is very important in all battery powered embedded applications. But the operating frequency of these embedded applications can be diverse based the needs of the application. Some applications might require operating at higher frequencies, in the order of several megahertz, while some other applications might require operating at lower frequencies, in the order of a few tens or a few hundreds of kilohertz. There are several microcontrollers in the market that offer good active mode power consumption when the operating frequency is in the order of several megahertz. But it is a challenge to get the power consumption low when the operating frequency is in the order of kilohertz. The low-frequency power modes available on the MSP432P4xx microcontrollers offer very low power consumption when low frequency of operation is used by the target application.

**Software IP Protection on MSP432P4xx Microcontrollers** Differentiations in embedded software applications enable differentiated products. Companies invest significant money in building differentiated software application. Hence, protecting this investment (application or portions of the application) is extremely important. This application note describes how to protect software intellectual property (IP) running on the Texas Instruments MSP432P401x family of microcontrollers.

**Code Conversion Application for MSP432P401R** This application note describes the use of the code conversion application delivered with version 2.0.0 (and above) of the MSP432P401R device header files. In these revisions of the MSP432P401R device header files, the coding style has been adapted to CMSIS. This may lead to compilation errors in user code if the code is not converted. MSP430 style register definitions have also been removed with exception of legacy 16-bit IPs (see msp432p401r_classic.h).

## 8.5 Related Links

Table 8-2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 8-2. Related Links**

| PARTS | PRODUCT FOLDER | ORDER NOW | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| MSP432P401R | Click here | Click here | Click here | Click here | Click here |
| MSP432P401M | Click here | Click here | Click here | Click here | Click here |

## 8.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Community

*TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

TI Embedded Processors Wiki

*Texas Instruments Embedded Processors Wiki*. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

## 8.7 Trademarks

MSP432, LaunchPad, SimpleLink, ULP Advisor, EnergyTrace, E2E are trademarks of Texas Instruments.
ARM, Cortex, Thumb, Keil are registered trademarks of ARM Ltd.
*Bluetooth* is a registered trademark of Bluetooth SIG.
ULPBench, ULPMark are trademarks of EEMBC.
Wi-Fi is a registered trademark of Wi-Fi Alliance.

## 8.8 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.9 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

## 8.10 Glossary

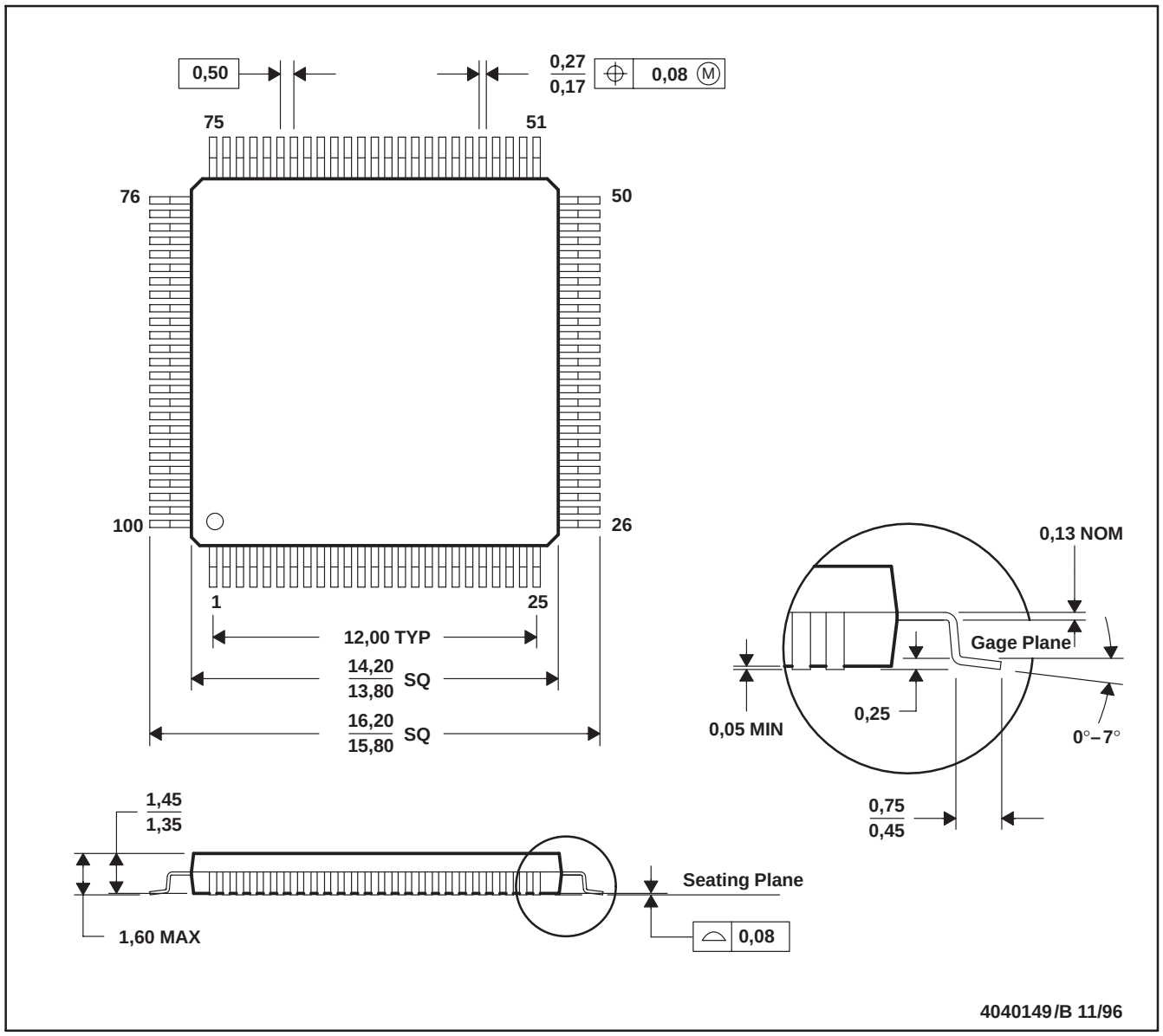
**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.

# 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

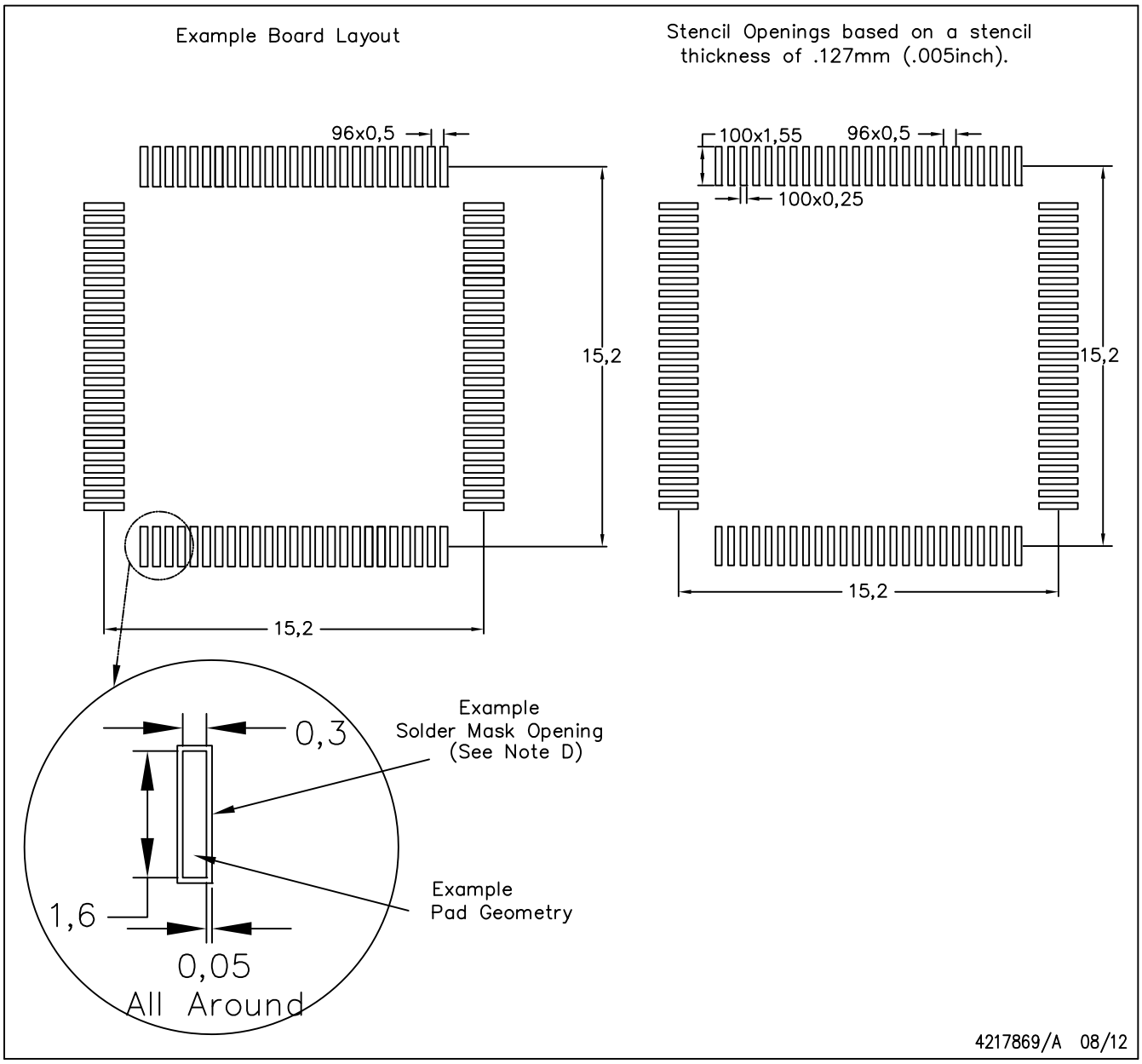
MTQF013A – OCTOBER 1994 – REVISED DECEMBER 1996

**PZ (S-PQFP-G100)** **PLASTIC QUAD FLATPACK**



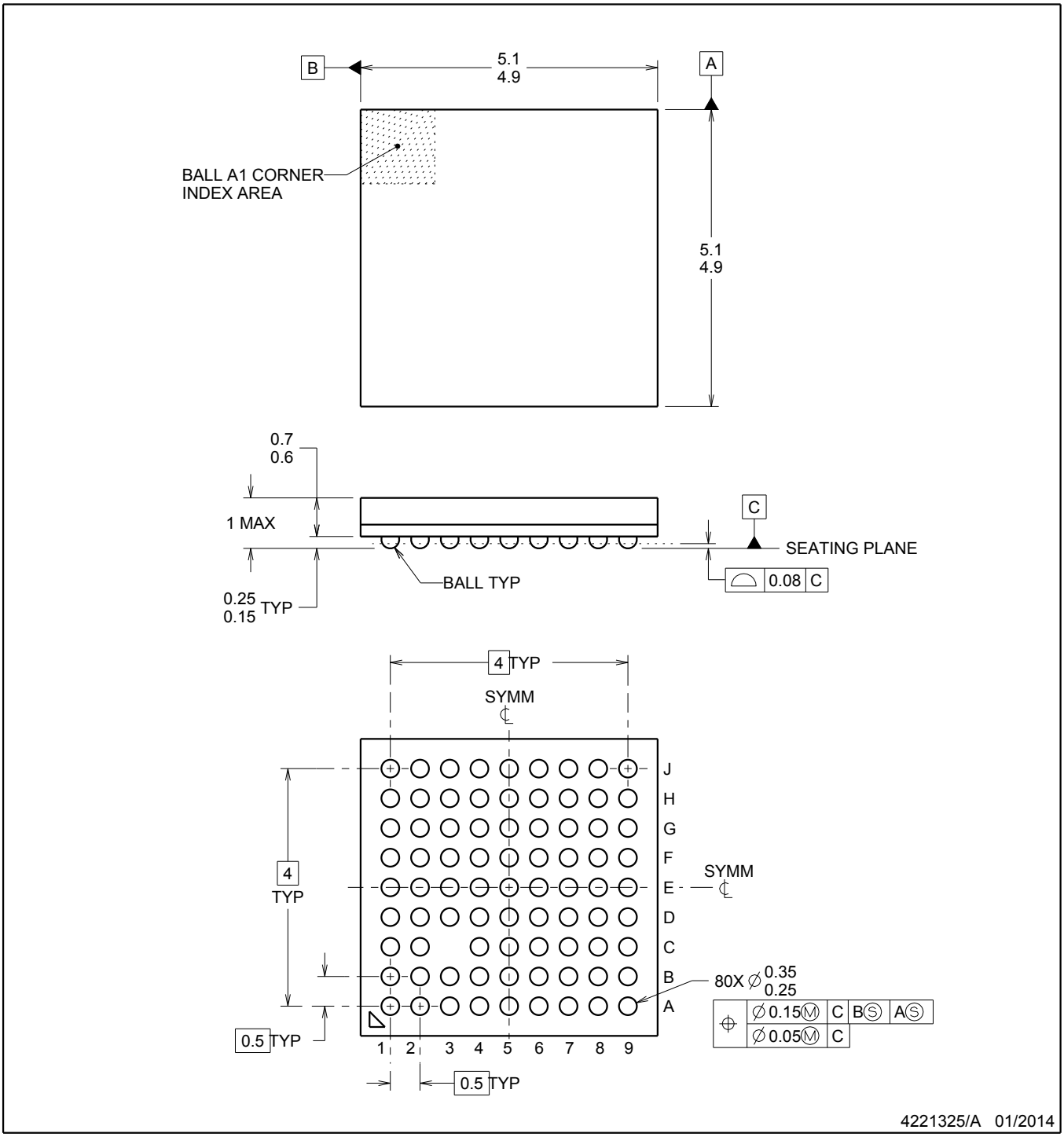

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

# PZ (S–PQFP–G100) PLASTIC QUAD FLAT PACK



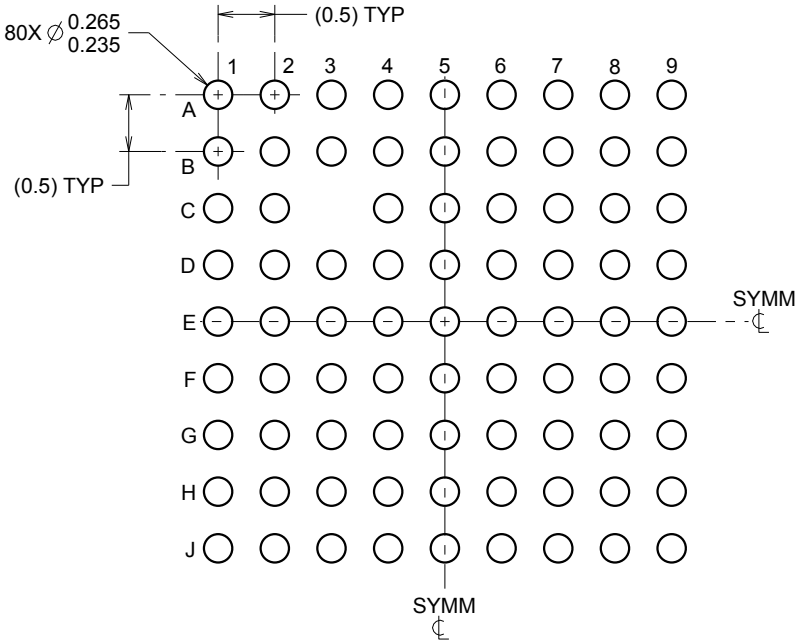

NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

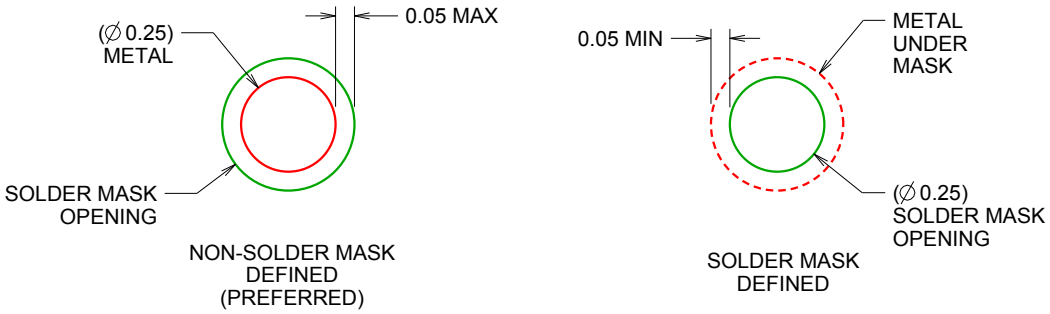



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis is for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This is a Pb-free solder ball design.




LAND PATTERN EXAMPLE
SCALE:15X

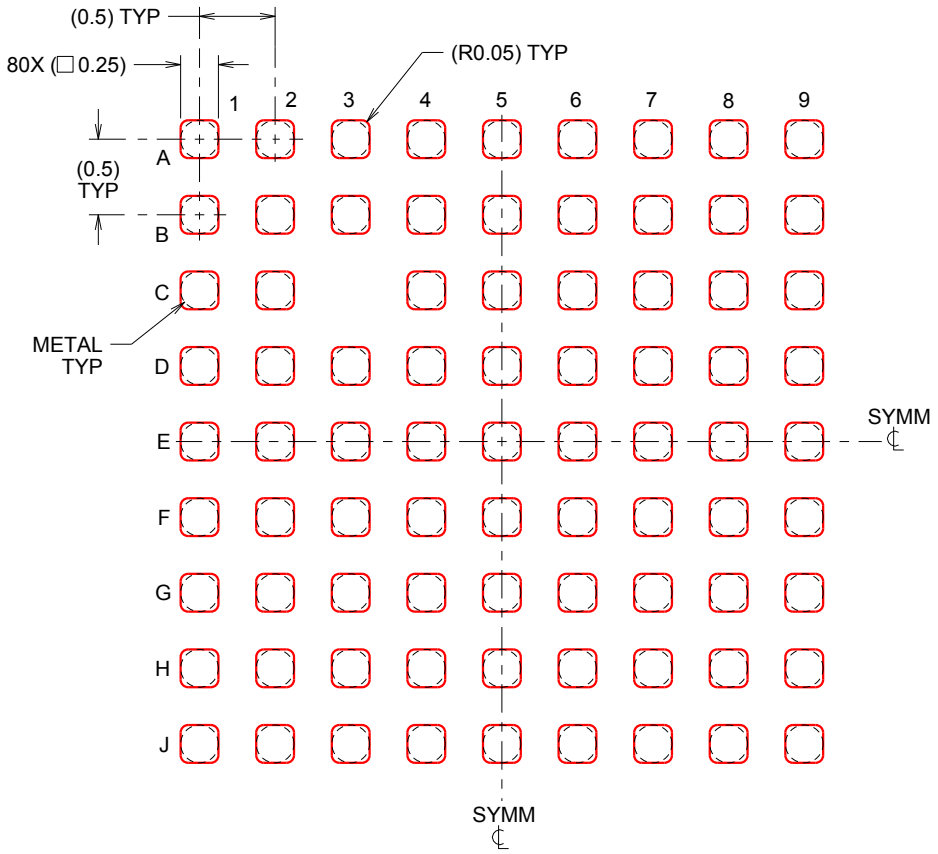



SOLDER MASK DETAILS
NOT TO SCALE

4221325/A 01/2014

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
See Texas Instruments Literature No. SBVA017 (www.ti.com/lit/sbva017).



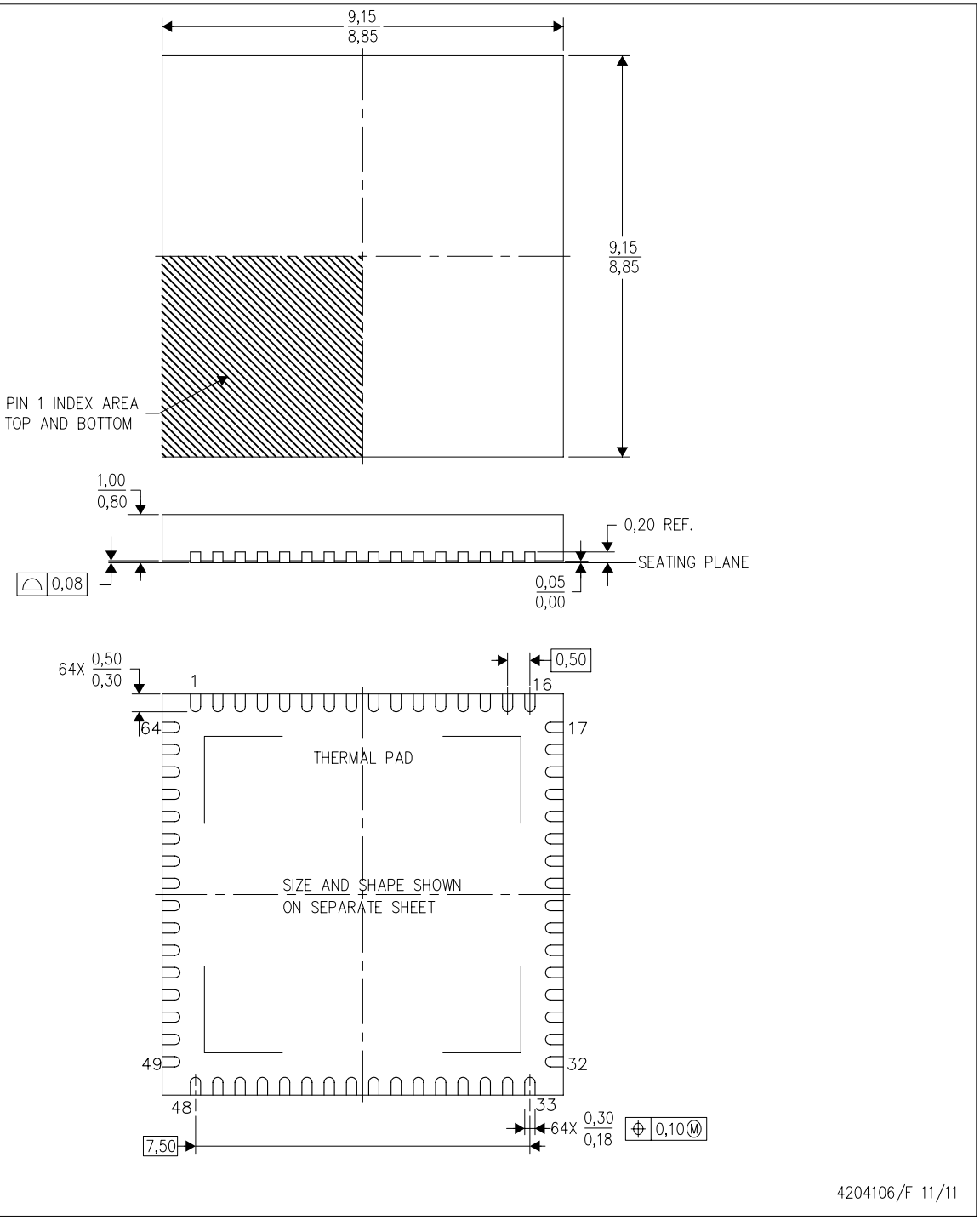

SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:20X

4221325/A 01/2014

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

RGC(S–PVQFN–N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

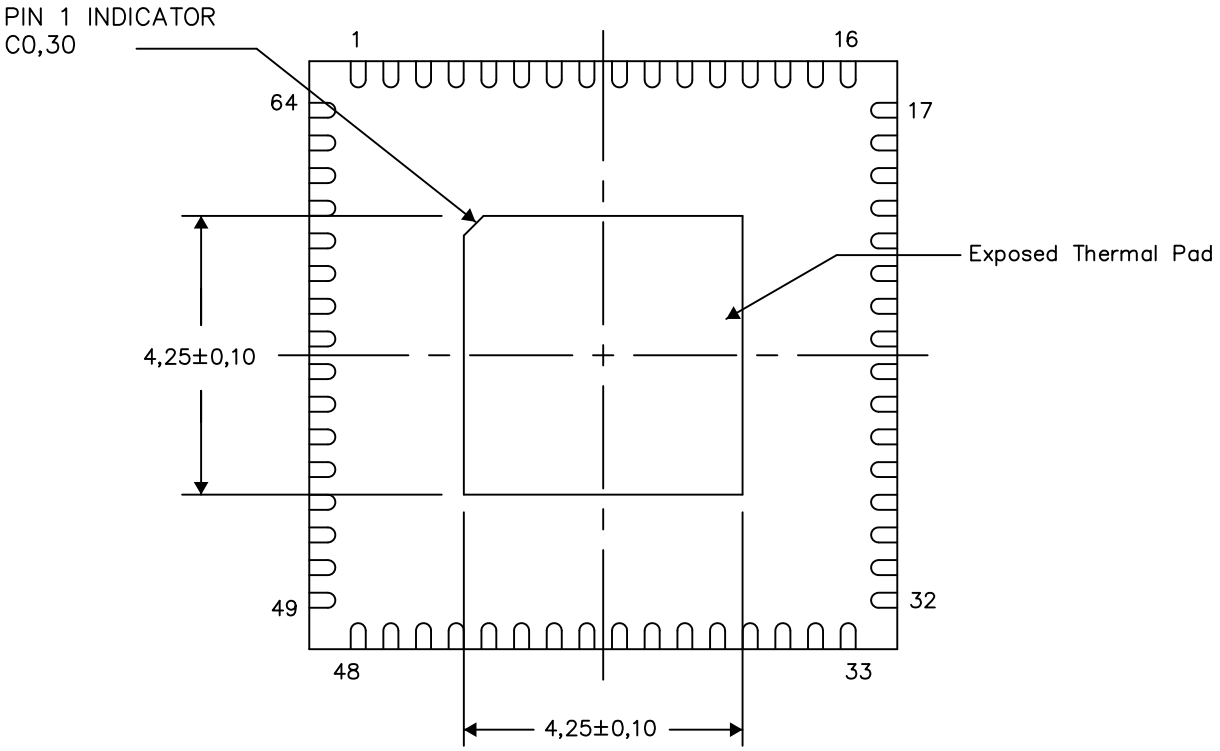
RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Bottom View

Exposed Thermal Pad Dimensions

4206192–3/AE 03/15

NOTE: A. All linear dimensions are in millimeters

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| MSP432P401MIPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | MSP432P401M | Samples |
| MSP432P401MIPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | MSP432P401M | Samples |
| MSP432P401MIRGCR | ACTIVE | VQFN | RGC | 64 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | MSP432P401M | Samples |
| MSP432P401MIRGCT | ACTIVE | VQFN | RGC | 64 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | MSP432P401M | Samples |
| MSP432P401MIZXHR | ACTIVE | NFBGA | ZXH | 80 | 2500 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 85 | P401M | Samples |
| MSP432P401MIZXHT | ACTIVE | NFBGA | ZXH | 80 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 85 | P401M | Samples |
| MSP432P401RIPZ | ACTIVE | LQFP | PZ | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | MSP432P401R | Samples |
| MSP432P401RIPZR | ACTIVE | LQFP | PZ | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | MSP432P401R | Samples |
| MSP432P401RIRGCR | ACTIVE | VQFN | RGC | 64 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | MSP432P401R | Samples |
| MSP432P401RIRGCT | ACTIVE | VQFN | RGC | 64 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | MSP432P401R | Samples |
| MSP432P401RIZXHR | ACTIVE | NFBGA | ZXH | 80 | 2500 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 85 | P401R | Samples |
| MSP432P401RIZXHT | ACTIVE | NFBGA | ZXH | 80 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | -40 to 85 | P401R | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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