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**---------- Clock and Data recovery circuit structure ------------**

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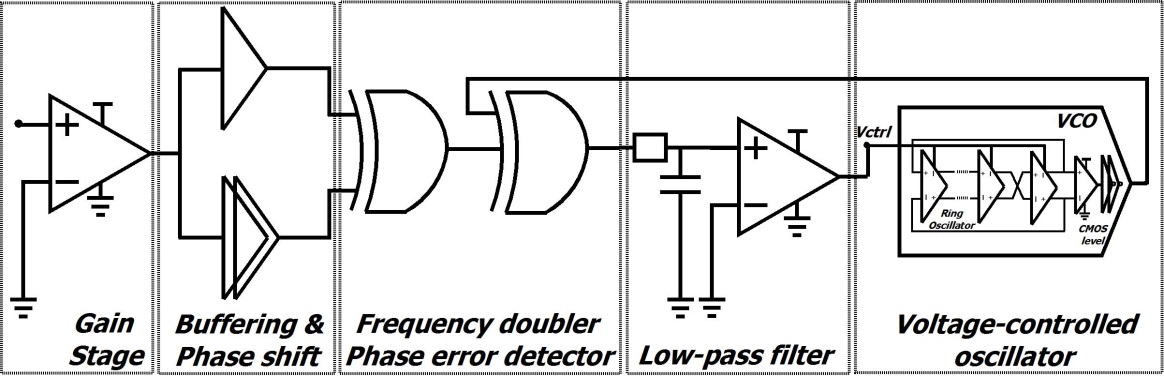


Figure 1. Clock and Data Recovery circuit

**(a) Phase Detector**

1. Input Gain stage: This stage buffers the input data signal as well as isolates the channel by inserting a high impedance component in the path.

2. Frequency doubler: As the PLL needs to extract a clock from data (CDR circuit), this stage allows for the data signal to be delayed, phase shifted and then added back to the original signal. This effectively creates twice the number of transitions. If the input data signal contains a periodic stream of alternations 1's and 0's the result of the F-doubler would be the original clock signal.

3. XOR's: The XOR's are used in the feedback loop for synchronizing the clock output if the VCO and the F-doubled signals. XOR's are a common component in many VCO designs. In our design we fabricated transistor level XOR gates which allowed for a more fine grained specification.

**(b) Low Pass Filter**

The LPF has been designed to rectify the input signal. The output of the phase detector stage is a periodic train of pulses where the duty cycle determines the phase errors. If no phase errors are encountered the signal resembles the clock. When this signal is low pass filtered the result is a slow varying sinusoid with a DC offset. When fed into the VCO it produces a stable output. Any phase errors manifest as variations in the DC offset of the LPF output.

**(c) VCO**

In our design the VCO is designed as MCML ring oscillator (Figure 1). The output of the VCO is used as the clock signal as well as a feedback input for the phase detector.

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**--- CDR Circuit Optimization Rules/Steps ---**

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Please follow these steps for CDR circuit optimization:

1) The circuit is composed of a ring-oscillator-based VCO, which uses differential signalling (MCML logic) for operation. MCML cell library with the required performance and power characteristics needs to be developed for the technology process in use. It is suggested to start from MCML gate optimization procedure.

VCO circuit is usually optimized/tuned first. Ring buffer (a chain of inverters) is extracted from the VCO subcircuit (**cells.spi**) and adjusted for the operation at required frequency inside the main file (**test.spi**). The optimization is performed with the built-in HSPICE optimizer; During this process the replica biasing circuit (**cells.spi**) is also used: the circuit takes control voltage as an input of VCO unit and converts it into the biasing voltage of (current) source MCML transistor, through a push-pull OPAMP. For initial VCO frequency tuning capabilities the ideal opamp (E-element in HSPICE) with a unity gain is used. Once the required frequency is achieved, all the related control parameters are stored for future use with realistic elements (OPAMP). In addition, max - min tuning frequency range should be recorded for the reference.

2) Once the adjustment of the VCO's ring buffer is done (i.e. selected the necessary number of inverters; evaluated power and delay characteristics; Vctrl operating at required (lock) frequency is registered (the ideal elements like OPAMP are still in use)), the corresponding tuning of the realistic OPAMP is performed. The OPAMP is adjusted in such a way that it can provide a similar characteristics (and identical biasing voltages for VCO ring buffers) as the ideal OPAMP. In case of a simple two stage OPAMP, differential stage transistor sizing, current mirror transistor sizing and output stage transistor sizing is optimized. The optimization is performed stage by stage to achieve the required characteristics of the OPAMP (using HSPICE built-in optimizer as used for MCML gate optimization). Usually it is quite difficult to obtain identical control voltages (to that of ideal OPAMP) for the entire tuning range, so a proper testing of optimized realistic OPAMP is required. Please identify the tuning range of the VCO circuit using realistic elements, loads and fanouts, and, record control voltages at both extremes (including the one at reference frequency).

Next, all the tuning procedures related to the CDR unit are performed with the realistic elements ONLY.

3) Once the OPAMP is adjusted, the abstraction of the VCO circuit is created (copy your design back to cells.spi). The subcircuit includes a ring buffer with biasing, CMOS-level regeneration circuit as well as the required differential output buffering.

4) The final adjustments include optimization of a Gain Stage OPAMP, and other adjustments required for the other CDR blocks (delay stage, freq. doubler, others). The incoming DATA is amplified by GAIN STAGE OPAMP. Next, the signal is split and transmitted through a set of delay lines to create a 45\* Phase Shift, which doubles the amount of original signal transitions (the first XOR gate).

5) Inputs of the second XOR gate are: 1) the output of XOR1 gate and, 2) the feedback signal obtained from the VCO. The output of the second XOR2 gate (phase errors) is feed into a low-pass filter, to obtain a slowly varying wave which controls/tunes the VCO. There might be additional OPAMPs, level shifting, and other circuits used for the correct voltage level matching (level obtained from phase error detector + LPF should match the one required for VCO control).

The parameters of the LPF are adjusted by using the "ideal" input pattern with continuous

"0/1" transitions generated every clock period. The output contol voltage of the LPF should match the voltage obtained during the optimization process. Similar adjustments are performed to the defined operation voltage range.

6) Once these steps are performed, the CDR unit is finally tested with the custom traffic patterns, including the one with transitions for each clock period.