

The diagram shows a 3.3V LDO (U2) with input pin VI (pin 3) connected to a +5V supply through capacitor C3 (1uF). The output pin VO (pin 2) is connected to a +3.3V supply through capacitor C4 (1uF). Both the input and output pins are connected to ground. The LDO is also connected to ground at its bottom pin.

J2
Conn_02x03_Odd_Even

VTrefJ 1 2 VTref
3 4 VTref
+3.3V ← 5 ← 6 VTref
+1V8 ←

The diagram illustrates the wiring for a Cortex Debug Connector. It features four connectors: J1 (Conn_02x05_Odd_Even), J3 (Conn_01x06), J5 (Conn_02x03_Odd_Even), and J4 (Conn_02x10_Odd_Even). The connections are as follows:

- J1 (Conn_02x05_Odd_Even):** Pins 1, 3, 5, 7, 9 are connected to GND. Pins 2, 4, 6, 8, 10 are connected to J3 pins 1, 2, 3, 4, 5 respectively.
- J3 (Conn_01x06):** Pin 1 is connected to GND. Pins 2, 3, 4, 5, 6 are connected to J5 pins 1, 2, 3, 4, 5 respectively.
- J5 (Conn_02x03_Odd_Even):** Pin 1 is connected to GND. Pins 2, 3, 4, 5, 6 are connected to J4 pins 1, 2, 3, 4, 5 respectively.
- J4 (Conn_02x10_Odd_Even):** Pins 1, 3, 5, 7, 9, 11, 13, 15, 17, 19 are connected to GND. Pins 2, 4, 6, 8, 10, 12, 14, 16, 18, 20 are connected to the J-Link Interface pins: SWDIO\TMS, SWDCLK\TCK, SWO\TDO, and RESET.

