1. Description

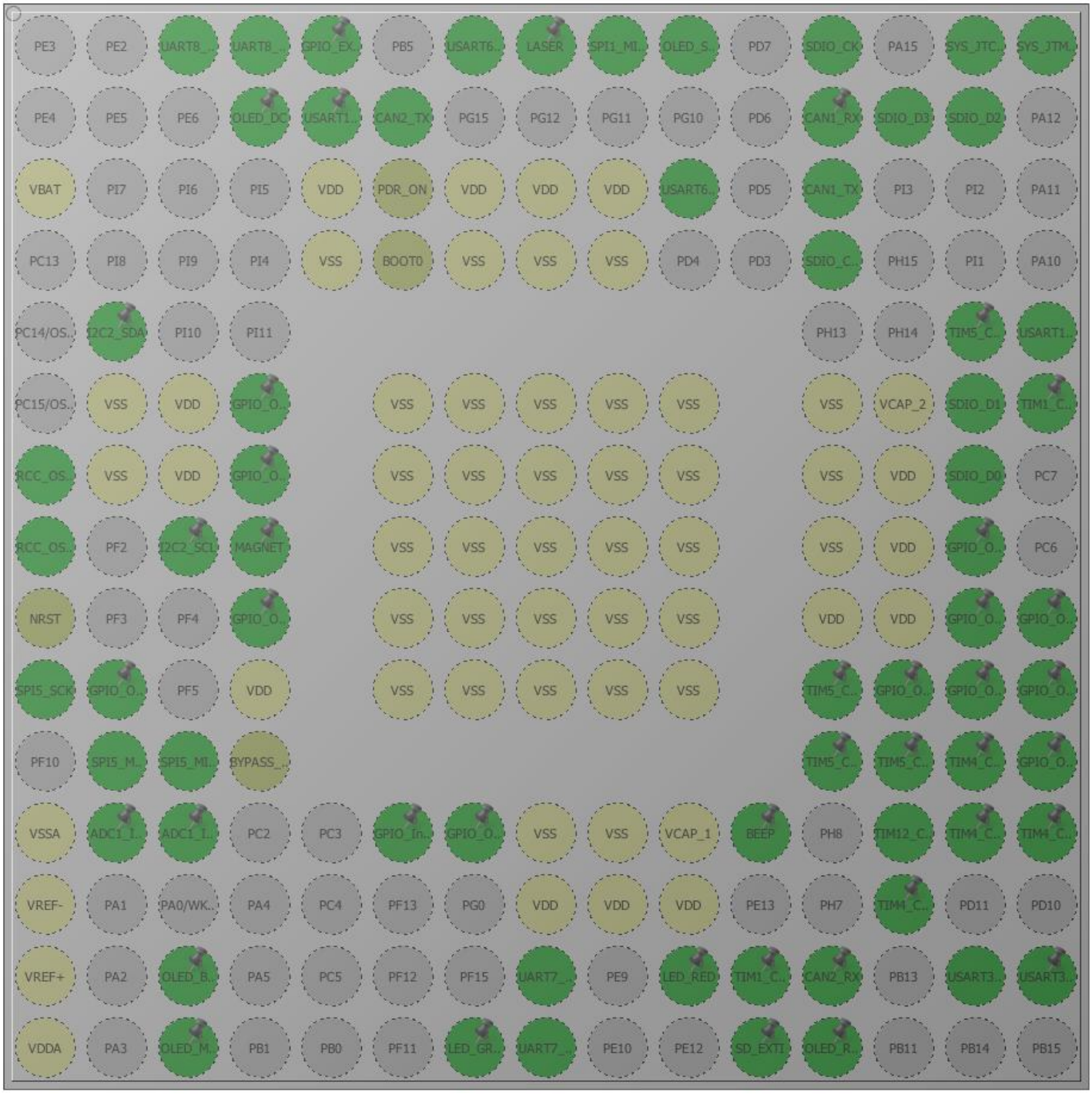
1.1. Project

Project Name	iRM_Embedded_2018
Board Name	iRM_2018_Type_A
Generated with:	STM32CubeMX 4.26.0
Date	07/11/2018

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F427/437
MCU name	STM32F427IIHx
MCU Package	UFBGA176
MCU Pin number	201

2. Pinout Configuration



STM32F427IIHx
UFBGA176 +25 (Top view)

3. Pins Configuration

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
A3	PE1	I/O	UART8_TX	
A4	PE0	I/O	UART8_RX	
A5	PB8	I/O	GPIO_EXTI8	
A7	PG14	I/O	USART6_TX	
A8	PG13 *	I/O	GPIO_Output	LASER
A9	PB4	I/O	SPI1_MISO	
A10	PB3	I/O	SPI1_SCK	OLED_SCK
A12	PC12	I/O	SDIO_CK	
A14	PA14	I/O	SYS_JTCK-SWCLK	
A15	PA13	I/O	SYS_JTMS-SWDIO	
B4	PB9 *	I/O	GPIO_Output	OLED_DC
B5	PB7	I/O	USART1_RX	
B6	PB6	I/O	CAN2_TX	
B12	PD0	I/O	CAN1_RX	
B13	PC11	I/O	SDIO_D3	
B14	PC10	I/O	SDIO_D2	
C1	VBAT	Power		
C5	VDD	Power		
C6	PDR_ON	Reset		
C7	VDD	Power		
C8	VDD	Power		
C9	VDD	Power		
C10	PG9	I/O	USART6_RX	
C12	PD1	I/O	CAN1_TX	
D5	VSS	Power		
D6	BOOT0	Boot		
D7	VSS	Power		
D8	VSS	Power		
D9	VSS	Power		
D12	PD2	I/O	SDIO_CMD	
E2	PF0	I/O	I2C2_SDA	
E14	PI0	I/O	TIM5_CH4	
E15	PA9	I/O	USART1_TX	
F2	VSS	Power		
F3	VDD	Power		
F4	PH2 *	I/O	GPIO_Output	

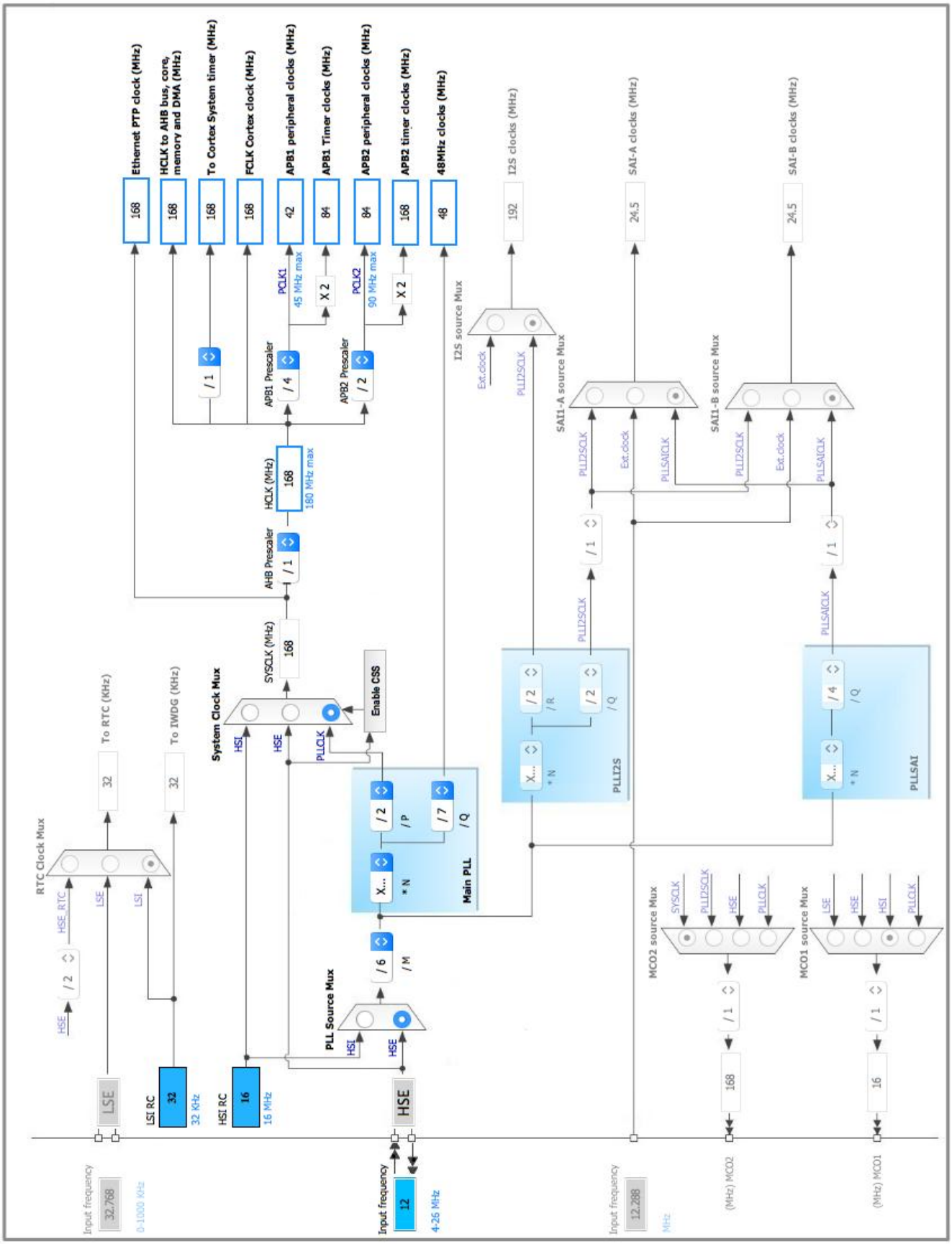
Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
F6	VSS	Power		
F7	VSS	Power		
F8	VSS	Power		
F9	VSS	Power		
F10	VSS	Power		
F12	VSS	Power		
F13	VCAP_2	Power		
F14	PC9	I/O	SDIO_D1	
F15	PA8	I/O	TIM1_CH1	
G1	PH0/OSC_IN	I/O	RCC_OSC_IN	
G2	VSS	Power		
G3	VDD	Power		
G4	PH3 *	I/O	GPIO_Output	
G6	VSS	Power		
G7	VSS	Power		
G8	VSS	Power		
G9	VSS	Power		
G10	VSS	Power		
G12	VSS	Power		
G13	VDD	Power		
G14	PC8	I/O	SDIO_D0	
H1	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
H3	PF1	I/O	I2C2_SCL	
H4	PH4 *	I/O	GPIO_Output	MAGNET
H6	VSS	Power		
H7	VSS	Power		
H8	VSS	Power		
H9	VSS	Power		
H10	VSS	Power		
H12	VSS	Power		
H13	VDD	Power		
H14	PG8 *	I/O	GPIO_Output	
J1	NRST	Reset		
J4	PH5 *	I/O	GPIO_Output	
J6	VSS	Power		
J7	VSS	Power		
J8	VSS	Power		
J9	VSS	Power		
J10	VSS	Power		

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
J12	VDD	Power		
J13	VDD	Power		
J14	PG7 *	I/O	GPIO_Output	
J15	PG6 *	I/O	GPIO_Output	
K1	PF7	I/O	SPI5_SCK	
K2	PF6 *	I/O	GPIO_Output	
K4	VDD	Power		
K6	VSS	Power		
K7	VSS	Power		
K8	VSS	Power		
K9	VSS	Power		
K10	VSS	Power		
K12	PH12	I/O	TIM5_CH3	
K13	PG5 *	I/O	GPIO_Output	
K14	PG4 *	I/O	GPIO_Output	
K15	PG3 *	I/O	GPIO_Output	
L2	PF9	I/O	SPI5_MOSI	
L3	PF8	I/O	SPI5_MISO	
L4	BYPASS_REG	Reset		
L12	PH11	I/O	TIM5_CH2	
L13	PH10	I/O	TIM5_CH1	
L14	PD15	I/O	TIM4_CH4	
L15	PG2 *	I/O	GPIO_Output	
M1	VSSA	Power		
M2	PC0	I/O	ADC1_IN10	
M3	PC1	I/O	ADC1_IN11	
M6	PB2/BOOT1 *	I/O	GPIO_Input	
M7	PG1 *	I/O	GPIO_Output	
M8	VSS	Power		
M9	VSS	Power		
M10	VCAP_1	Power		
M11	PH6	I/O	TIM12_CH1	BEEP
M13	PH9	I/O	TIM12_CH2	
M14	PD14	I/O	TIM4_CH3	
M15	PD13	I/O	TIM4_CH2	
N1	VREF-	Power		
N8	VDD	Power		
N9	VDD	Power		
N10	VDD	Power		

Pin Number UFBGA176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
N13	PD12	I/O	TIM4_CH1	
P1	VREF+	Power		
P3	PA6	I/O	ADC1_IN6	OLED_BUTTON
P8	PE8	I/O	UART7_TX	
P10	PE11 *	I/O	GPIO_Output	LED_RED
P11	PE14	I/O	TIM1_CH4	
P12	PB12	I/O	CAN2_RX	
P14	PD9	I/O	USART3_RX	
P15	PD8	I/O	USART3_TX	
R1	VDDA	Power		
R3	PA7	I/O	SPI1_MOSI	OLED_MOSI
R7	PF14 *	I/O	GPIO_Output	LED_GREEN
R8	PE7	I/O	UART7_RX	
R11	PE15 *	I/O	GPIO_Input	SD_EXTI
R12	PB10 *	I/O	GPIO_Output	OLED_RST

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN6

mode: IN10

mode: IN11

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	**Enabled ***
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	**EOC flag at the end of all conversions ***

ADC_Regular_ConversionMode:

Number Of Conversion	**3 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 6
Sampling Time	**144 Cycles ***
Rank	**2 ***
Channel	**Channel 10 ***
Sampling Time	**144 Cycles ***
Rank	**3 ***
Channel	**Channel 11 ***
Sampling Time	**144 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. CAN1

mode: Mode

5.2.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	**3 ***
Time Quantum	**71.42857142857143 ***
Time Quanta in Bit Segment 1	**9 Times ***
Time Quanta in Bit Segment 2	**4 Times ***
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	**Enable ***
Automatic Wake-Up Mode	Disable
No-Automatic Retransmission	**Enable ***
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal

5.3. CAN2

mode: Mode

5.3.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	**3 ***
Time Quantum	**71.42857142857143 ***
Time Quanta in Bit Segment 1	**9 Times ***
Time Quanta in Bit Segment 2	**4 Times ***
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	**Enable ***
Automatic Wake-Up Mode	Disable
No-Automatic Retransmission	**Enable ***

Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal

5.4. I2C2

I2C: I2C

5.4.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

5.5. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.5.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Disabled

5.6. SDIO

Mode: SD 4 bits Wide bus

5.6.1. Parameter Settings:

SDIO parameters:

Clock transition on which the bit capture is made	Rising transition
SDIO Clock divider bypass	Disable
SDIO Clock output enable when the bus is idle	Disable the power save for the clock
SDIO hardware flow control	The hardware control flow is disabled
SDIOCLK clock divide factor	0

5.7. SPI1

Mode: Full-Duplex Master

5.7.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**64 ***
Baud Rate	**1.3125 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

5.8. SPI5

Mode: Full-Duplex Master

5.8.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**128 ***
Baud Rate	**656.25 KBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

5.9. SYS

Debug: Serial Wire

Timebase Source: TIM3

5.10. TIM1

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel4: PWM Generation CH4

5.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable

Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

5.11. TIM4

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

5.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable

CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

5.12. TIM5

mode: Clock Source

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

5.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (32 bits value)	0
Fast Mode	Disable
CH Polarity	High

5.13. TIM12

mode: Clock Source

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

5.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**83 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

5.14. UART7

Mode: Asynchronous

5.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.15. UART8

Mode: Asynchronous

5.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.16. USART1

Mode: Asynchronous

5.16.1. Parameter Settings:

Basic Parameters:

Baud Rate	**100000 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.17. USART3

Mode: Asynchronous

5.17.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.18. USART6

Mode: Asynchronous

5.18.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.19. FATFS

mode: SD Card

5.19.1. Set Defines:

Version:

FATFS version	R0.12c

Function Parameters:

FS_READONLY (Read-only mode)	Disabled

FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	Enabled with LF -> CRLF conversion
USE_FIND (Find functions)	Disabled
USE_MKFS (Make filesystem function)	Enabled
USE_FASTSEEK (Fast seek function)	Enabled
USE_EXPAND (Use f_expand function)	Disabled
USE_CHMOD (Change attributes function)	Disabled
USE_LABEL (Volume label functions)	Disabled
USE_FORWARD (Forward function)	Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Latin 1
USE_LFN (Use Long Filename)	**Enabled with dynamic working buffer on the STACK ***
MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8
FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	1
MAX_SS (Maximum Sector Size)	512
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_TINY (Tiny mode)	Disabled
FS_EXFAT (Support of exFAT file system)	Disabled
FS_NORTC (Timestamp feature)	Dynamic timestamp
NORTC_YEAR (Year for timestamp)	2015
NORTC_MON (Month for timestamp)	6
NORTC_MDAY (Day for timestamp)	4
FS_REENTRANT (Re-Entrancy)	Enabled
FS_TIMEOUT (Timeout ticks)	1000
SYNC_t (O/S sync object)	osSemaphoreId
FS_LOCK (Number of files opened simultaneously)	2

5.19.2. IPs instances:

SDIO/SDMMC:

SDIO instance	SDIO
Use dma template	Enabled

5.20. FREERTOS

mode: Enabled

5.20.1. Config parameters:

Versions:

FreeRTOS version	9.0.0
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled

Memory management settings:

Memory Allocation	Dynamic
TOTAL_HEAP_SIZE	**65536 ***
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled

USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

5.20.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	**Enabled ***
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	**Enabled ***
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN10	Analog mode	No pull-up and no pull-down	n/a	
	PC1	ADC1_IN11	Analog mode	No pull-up and no pull-down	n/a	
	PA6	ADC1_IN6	Analog mode	No pull-up and no pull-down	n/a	OLED_BUTTON
CAN1	PD0	CAN1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PD1	CAN1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
CAN2	PB6	CAN2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB12	CAN2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
I2C2	PF0	I2C2_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
	PF1	I2C2_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SDIO	PC12	SDIO_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDIO_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDIO_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDIO_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDIO_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC8	SDIO_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SPI1	PB4	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB3	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	OLED_SCK
	PA7	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	OLED_MOSI
SPI5	PF7	SPI5_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PF9	SPI5_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High**	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PF8	SPI5_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SYS	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PE14	TIM1_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM4	PD15	TIM4_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD14	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM5	PI0	TIM5_CH4	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH12	TIM5_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH11	TIM5_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PH10	TIM5_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM12	PH6	TIM12_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	BEEP
	PH9	TIM12_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
UART7	PE8	UART7_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PE7	UART7_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
UART8	PE1	UART8_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PE0	UART8_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
USART1	PB7	USART1_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
USART3	PD9	USART3_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PD8	USART3_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
USART6	PG14	USART6_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PG9	USART6_RX	Alternate Function Push Pull	Pull-up	**Very High**	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
GPIO	PB8	GPIO_EXTI8	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	
	PG13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LASER
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OLED_DC
	PH2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PH3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PH4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MAGNET
	PG8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PH5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PF6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PG2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB2/BOOT1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PG1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_RED
	PF14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_GREEN
	PE15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	SD_EXTI
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OLED_RST

6.2. DMA configuration

DMA request	Stream	Direction	Priority
SDIO_TX	DMA2_Stream3	Memory To Peripheral	Low
SDIO_RX	DMA2_Stream6	Peripheral To Memory	Low
UART8_RX	DMA1_Stream6	Peripheral To Memory	Low
UART8_TX	DMA1_Stream0	Memory To Peripheral	Low
ADC1	DMA2_Stream0	Peripheral To Memory	Low
UART7_RX	DMA1_Stream3	Peripheral To Memory	Low
USART1_RX	DMA2_Stream2	Peripheral To Memory	Low
USART3_RX	DMA1_Stream1	Peripheral To Memory	Low
USART3_TX	DMA1_Stream4	Memory To Peripheral	Low
USART6_RX	DMA2_Stream1	Peripheral To Memory	Low
USART6_TX	DMA2_Stream7	Memory To Peripheral	Low

SDIO_TX: DMA2_Stream3 DMA request Settings:

Mode:	**Peripheral Flow Control ***
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	Word
Peripheral Burst Size:	**4 Increment ***
Memory Burst Size:	4 Increment

SDIO_RX: DMA2_Stream6 DMA request Settings:

Mode:	**Peripheral Flow Control ***
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	Word
Peripheral Burst Size:	**4 Increment ***
Memory Burst Size:	4 Increment

UART8_RX: DMA1_Stream6 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

UART8_TX: DMA1_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

UART7_RX: DMA1_Stream3 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART1_RX: DMA2_Stream2 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART3_RX: DMA1_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART3_TX: DMA1_Stream4 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART6_RX: DMA2_Stream1 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART6_TX: DMA2_Stream7 DMA request Settings:

Mode:	Normal
Use fifo:	Disable

Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
DMA1 stream0 global interrupt	true	5	0
DMA1 stream1 global interrupt	true	5	0
DMA1 stream3 global interrupt	true	5	0
DMA1 stream4 global interrupt	true	5	0
DMA1 stream6 global interrupt	true	5	0
ADC1, ADC2 and ADC3 global interrupts	true	5	0
CAN1 TX interrupts	true	5	0
CAN1 RX0 interrupts	true	5	0
TIM3 global interrupt	true	0	0
USART1 global interrupt	true	5	0
USART3 global interrupt	true	5	0
SDIO global interrupt	true	5	0
DMA2 stream0 global interrupt	true	5	0
DMA2 stream1 global interrupt	true	5	0
DMA2 stream2 global interrupt	true	5	0
DMA2 stream3 global interrupt	true	5	0
CAN2 TX interrupts	true	5	0
CAN2 RX0 interrupts	true	5	0
DMA2 stream6 global interrupt	true	5	0
DMA2 stream7 global interrupt	true	5	0
USART6 global interrupt	true	5	0
UART7 global interrupt	true	5	0
UART8 global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
CAN1 RX1 interrupt	unused		
CAN1 SCE interrupt	unused		
EXTI line[9:5] interrupts	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM4 global interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
SPI1 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
TIM5 global interrupt	unused		
CAN2 RX1 interrupt	unused		
CAN2 SCE interrupt	unused		
FPU global interrupt	unused		
SPI5 global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F427/437
MCU	STM32F427IIHx
Datasheet	024030_Rev9

7.2. Parameter Selection

Temperature	25
Vdd	null

8. Software Pack Report

9. Software Project

9.1. Project Settings

Name	Value
Project Name	iRM_Embedded_2018
Project Folder	/Users/alvin/iRM_Embedded_2018
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F4 V1.21.0

9.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No