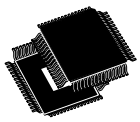
STM32F051x4 STM32F051x6 STM32F051x8

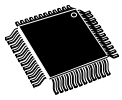
Low- and medium-density advanced ARM™-based 32-bit MCU with 16 to 64 Kbytes Flash, timers, ADC, DAC and comm. interfaces

Datasheet – preliminary data

Features

- Operating conditions:
  - Voltage range: 2.0 V to 3.6 V
- ARM 32-bit Cortex®-M0 CPU (48 MHz max)
- Memories
  - 16 to 64 Kbytes of Flash memory
  - 8 Kbytes of SRAM with HW parity checking
- CRC calculation unit
- Clock management
  - 4 to 32 MHz crystal oscillator
  - 32 kHz oscillator for RTC with calibration
  - Internal 8 MHz RC with x6 PLL option
  - Internal 40 kHz RC oscillator
- Calendar RTC with alarm and periodic wakeup from Stop/Standby
- Reset and supply management
  - Power-on/Power down reset (POR/PDR)
  - Programmable voltage detector (PVD)
- Low power Sleep, Stop, and Standby modes
- V_{BAT} supply for RTC and backup registers
- 5-channel DMA controller
- 1 × 12-bit, 1.0 µs ADC (up to 16 channels)
  - Conversion range: 0 to 3.6V
  - Separate analog supply from 2.4 up to 3.6
- Two fast low-power analog comparators with programmable input and output
- One 12-bit D/A converter
- Up to 55 fast I/Os
  - All mappable on external interrupt vectors
  - Up to 36 I/Os with 5 V tolerant capability
- Up to 18 capacitive sensing channels supporting touchkey, linear and rotary touch sensors
- 96-bit unique ID
- Serial wire debug (SWD)


LQFP64 10x10


LQFP48 7x7


UFQFPN32 5x5

- Up to 11 timers
  - One 16-bit 7-channel advanced-control timer for 6 channels PWM output, with deadtime generation and emergency stop
  - One 32-bit and one 16-bit timer, with up to 4 IC/OC, usable for IR control decoding
  - One 16-bit timer, with 2 IC/OC, 1 OCN, deadtime generation and emergency stop
  - Two 16-bit timers, each with IC/OC and OCN, deadtime generation, emergency stop and modulator gate for IR control
  - One 16-bit timer with 1 IC/OC
  - Independent and system watchdog timers
  - SysTick timer: 24-bit downcounter
  - One 16-bit basic timer to drive the DAC
- Communication interfaces
  - Up to two I^2C interfaces; one supporting Fast Mode Plus (1 Mbit/s) with 20 mA current sink, SMBus/PMBus, and wakeup from STOP
  - Up to two USARTs supporting master synchronous SPI and modem control; one with ISO7816 interface, LIN, IrDA capability, auto baud rate detection and wakeup feature
  - Up to two SPIs (18 Mbit/s) with 4 to 16 programmable bit frame, 1 with I^2S interface multiplexed
  - HDMI CEC interface, wakeup on header reception

Table 1. Device summary

Reference	Part number
STM32F051x4	STM32F051K4, STM32F051C4, STM32F051R4
STM32F051x6	STM32F051K6, STM32F051C6, STM32F051R6
STM32F051x8	STM32F051C8, STM32F051R8, STM32F051K8

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F051xx microcontrollers.

This STM32F051x6 and STM32F051x8 datasheet should be read in conjunction with the STM32F051xx reference manual. The reference manual is available from the STMicroelectronics website www.st.com.

For information on the ARM Cortex™-M0 core please refer to the Cortex™-M0 Technical Reference Manual, available from the www.arm.com website at the following address: http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ddi0432c/index.html.

2 Description

The STM32F051xx family incorporates the high-performance ARM Cortex™-M0 32-bit RISC core operating at a 48 MHz frequency, high-speed embedded memories (Flash memory up to 64 Kbytes and SRAM up to 8 Kbytes), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (up to two I^2Cs, two SPIs, one I2S, one HDMI CEC, and up to two USARTs), one 12-bit ADC, one 12-bit DAC, up to five general-purpose 16-bit timers, a 32-bit timer and an advanced-control PWM timer.

The STM32F051xx family operates in the -40 to +85 °C and -40 to +105 °C temperature ranges, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F051xx family includes devices in three different packages ranging from 32 pins to 64 pins. Depending on the device chosen, different sets of peripherals are included. The description below provides an overview of the complete range of peripherals proposed in this family.

These features make the STM32F051xx microcontroller family suitable for a wide range of applications such as application control and user interfaces, handheld equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms, and HVACs.

Table 2. STM32F051xx family device features and peripheral counts

Peripheral		STM32F051Kx			STM32F051Cx			STM32F051Rx		
Flash (Kbytes)		16	32	64	16	32	64	16	32	64
SRAM (Kbytes)		4		8	4		8	4		8
Timers	Advanced control	1 (16-bit)								
	General purpose	5 (16-bit) 1 (32-bit)								
	Basic	1 (16-bit)								
Comm. interfaces	SPI (I2S)(1)	1(1) (2)		2(1)	1(1) (2)		2(1)	1(1) (2)		2(1)
	I^2C	1(3)		2	1(3)		2	1(3)		2
	USART	1(4)	2		1(4)	2		1(4)	2	
	CEC	1								
12-bit synchronized ADC (number of channels)		1 (10 ext. + 3 int.)						1 (16 ext. + 3 int.)		
GPIOs		27			39			55		
Capacitive sensing channels		14			17			18		
12-bit DAC (number of channels)		1 (1)								
Analog comparator		2								
Max. CPU frequency		48 MHz								
Operating voltage		2.0 to 3.6 V								
Operating temperature		Ambient operating temperature: -40 °C to 85 °C / -40 °C to 105 °C Junction temperature: -40 °C to 125 °C								
Packages		UFQFPN32			LQFP48			LQFP64		

1. The SPI1 interface can be used either in SPI mode or in I2S audio mode.
2. SPI2 is not present
3. I2C2 is not present
4. USART2 is not present

3 Device overview

Figure 1. Block diagram

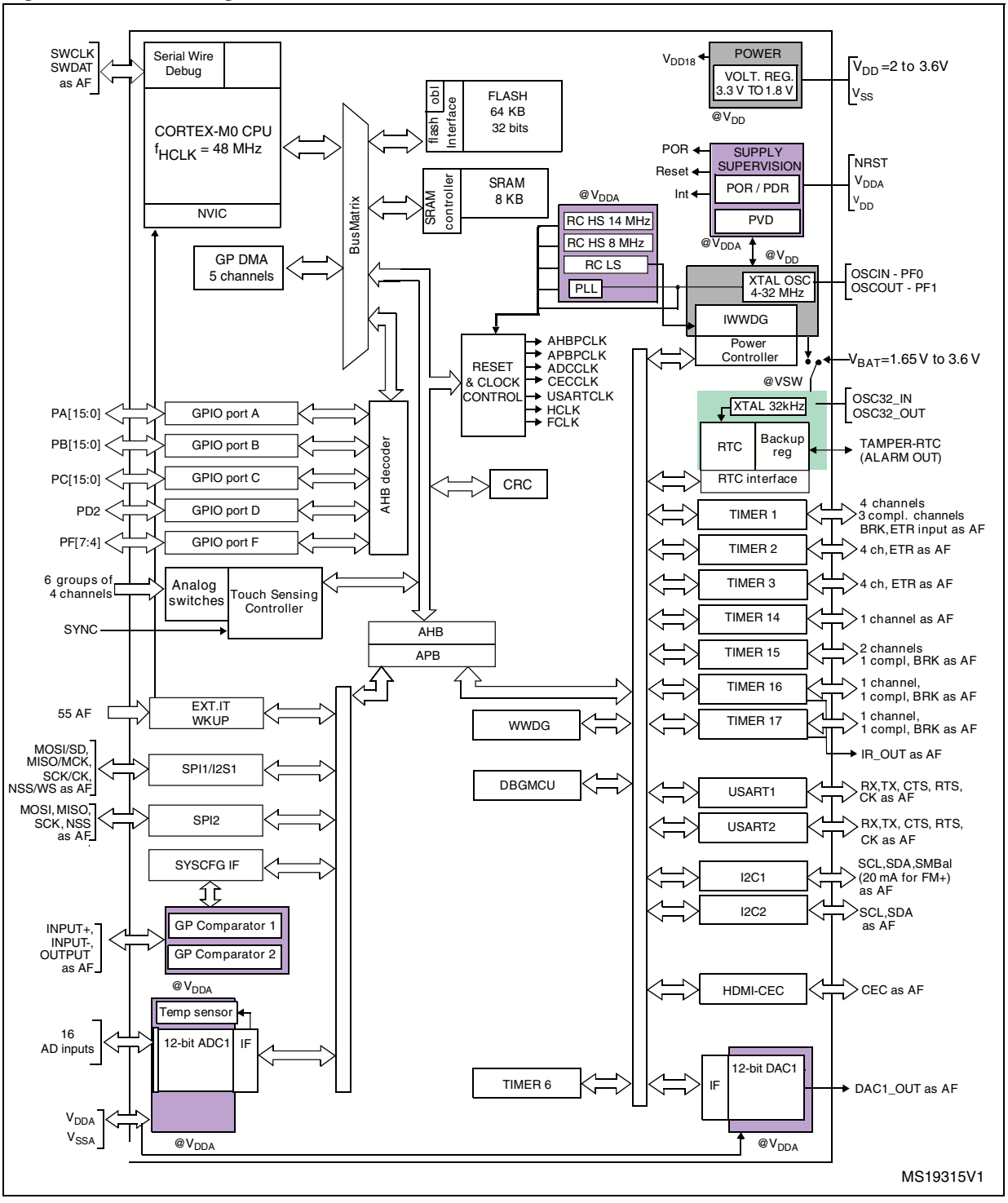
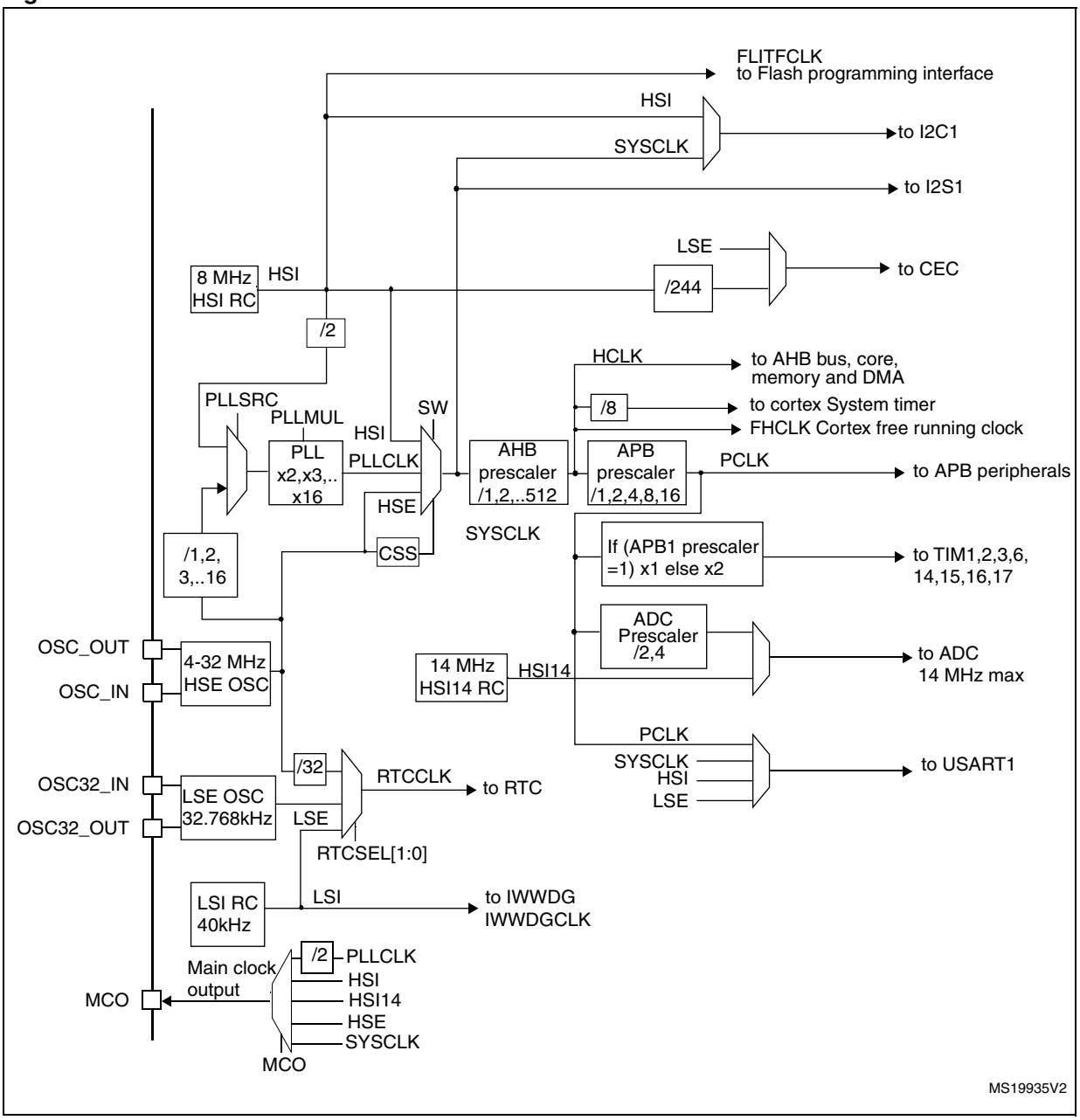


Figure 2. Clock tree



4 Functional overview

4.1 ARM® Cortex™-M0 core with embedded Flash and SRAM

The ARM Cortex™-M0 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex™-M0 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F051xx family has an embedded ARM core and is therefore compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

4.2 Memories

The device has the following features:

- Up to 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
  - 16 to 64 Kbytes of embedded Flash memory for programs and data
  - Option bytes

  The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (Cortex-M0 serial wire) and boot in RAM selection disabled

4.3 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 96-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

4.4 Direct memory access controller (DMA)

The 5-channel general-purpose DMAs manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPI, I2S, I2C, USART, all TIMx timers (except TIM14), DAC and ADC.

4.5 Nested vectored interrupt controller (NVIC)

The STM32F051xx family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex™-M0) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

4.6 Extended interrupt/event controller (EXTI)

The external interrupt/event controller consists of 24 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 55 GPIOs can be connected to the 16 external interrupt lines.

4.7 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.

4.8 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART1.

4.9 Power management

4.9.1 Power supply schemes

- V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{DDA} = 2.0 to 3.6 V: external analog power supply for ADC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC and DAC are used). The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be provided first.
- V_{BAT} = 1.6 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to *Figure 9: Power supply scheme*.

4.9.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

4.9.3 Voltage regulator

The regulator has three operating modes: main (MR), low power (LPR) and power down.

- MR is used in normal operating mode (Run)
- LPR can be used in Stop mode where the power demand is reduced
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode, providing high impedance output.

4.10 Low-power modes

The STM32F051xx family supports three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

  The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external lines, the PVD output, RTC alarm, COMPx, I2C1, USART1 or the CEC.

  The I2C1, USART1 and the CEC can be configured to enable the HSI RC oscillator for processing incoming data. If this is used, the voltage regulator should not be put in the low-power mode but kept in normal mode.

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), a IWDG reset, a rising edge on the WKUP pins, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

4.11 Real-time clock (RTC) and backup registers

The RTC and the 5 backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatically correction for 28, 29 (leap year), 30, and 31 day of the month.
- Programmable alarm with wake up from Stop and Standby mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize it with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- 2 anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32.

4.12 Timers and watchdogs

The STM32F051xx family devices include up to six general-purpose timers, one basic timer and an advanced control timer.

Table 3 compares the features of the advanced-control, general-purpose and basic timers.

Table 3. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced control	TIM1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
General purpose	TIM2	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TIM3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No
	TIM15	16-bit	Up	Any integer between 1 and 65536	Yes	2	Yes
	TIM16, TIM17	16-bit	Up	Any integer between 1 and 65536	Yes	1	Yes
Basic	TIM6	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

4.12.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

4.12.2 General-purpose timers (TIM2..3, TIM14..17)

There are six synchronizable general-purpose timers embedded in the STM32F051xx devices (see *Table 3* for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

TIM2, TIM3

STM32F051xx devices feature two synchronizable 4-channel general-purpose timers. TIM2 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIM3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2 and TIM3 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2 and TIM3 both have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

Its counter can be frozen in debug mode.

TIM15, TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate with TIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16, and TIM17 have a complementary output with dead-time generation and independent DMA request generation

Their counters can be frozen in debug mode.

4.12.3 Basic timer TIM6

This timer is mainly used for DAC trigger generation. It can also be used as a generic 16-bit time base.

4.12.4 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

4.12.5 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

4.12.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source (HCLK or HCLK/8)

4.13 Inter-integrated circuit interfaces (I^2C)

Up to two I^2C interfaces (I2C1 and I2C2) can operate in multimaster or slave modes. Both can support Standard mode (up to 100 kbit/s) or Fast mode (up to 400 kbit/s) and I2C1 supports also Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive.

Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (2 addresses, 1 with configurable mask). They also include programmable analog and digital noise filters.

Table 4. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Disabled when Wakeup from Stop mode is enabled

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I2C interfaces can be served by the DMA controller.

Refer to *Table 5* for the differences between I2C1 and I2C2.

Table 5. STM32F051xx I²C implementation

I2C features(1)	I2C1	I2C2
7-bit addressing mode	X	X
10-bit addressing mode	X	X
Standard mode (up to 100 kbit/s)	X	X
Fast mode (up to 400 kbit/s)	X	X
Fast Mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	
Independent clock	X	
SMBus	X	
Wakeup from STOP	X	

1. X = supported.

4.14 Universal synchronous/asynchronous receiver transmitters (USART)

The device embeds up to two universal synchronous/asynchronous receiver transmitters (USART1 and USART2), which communicate at speeds of up to 6 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. The USART1 supports also SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability, auto baud rate feature and has a clock domain independent from the CPU clock, allowing the USART1 to wake up the MCU from Stop mode.

The USART interfaces can be served by the DMA controller.Serial peripheral interface (SPI).

Refer to *Table 6* for the differences between USART1 and USART2.

Table 6. STM32F051xx USART implementation

USART modes/features(1)	USART1	USART2
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode	X	X
Smartcard mode	X	
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	
LIN mode	X	
Dual clock domain and wakeup from Stop mode	X	
Receiver timeout interrupt	X	
Modbus communication	X	
Auto baud rate detection	X	
Driver Enable	X	X

1. X = supported.

4.15 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I^2S)

Up to two SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

One standard I^2S interface (multiplexed with SPI1) supporting four different audio standards can operate as master or slave at simplex communication mode. It can be configured to transfer 16 and 24 or 32 bits with16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by 8-bit programmable linear prescaler. When operating in master mode it can output a clock for an external audio component at 256 times the sampling frequency.

Refer to *Table 7* for the differences between SPI1 and SPI2.

Table 7. STM32F051x SPI/I2S implementation

SPI features(1)	SPI1	SPI2
Hardware CRC calculation	X	X
Rx/Tx FIFO	X	X
NSS pulse mode	X	X
I2S mode	X	
TI mode	X	X

1. X = supported.

4.16 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI_CEC controller to wakeup the MCU from Stop mode on data reception.

4.17 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

4.18 Touch sensing controller (TSC)

The device has an embedded independent hardware controller (TSC) for controlling touch sensing acquisitions on the I/Os.

Up to 18 touch sensing electrodes can be controlled by the TSC. The touch sensing I/Os are organized in 6 acquisition groups, with up to 4 I/Os in each group.

Table 8. Capacitive sensing GPIOs available on STM32F051x devices

Group	Capacitive sensing signal name	Pin name	Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0	4	TSC_G4_IO1	PA9
	TSC_G1_IO2	PA1		TSC_G4_IO2	PA10
	TSC_G1_IO3	PA2		TSC_G4_IO3	PA11
	TSC_G1_IO4	PA3		TSC_G4_IO4	PA12
2	TSC_G2_IO1	PA4	5	TSC_G5_IO1	PB3
	TSC_G2_IO2	PA5		TSC_G5_IO2	PB4
	TSC_G2_IO3	PA6		TSC_G5_IO3	PB6
	TSC_G2_IO4	PA7		TSC_G5_IO4	PB7
3	TSC_G3_IO1	PB0	6	TSC_G6_IO1	PB11
	TSC_G3_IO2	PB1		TSC_G6_IO2	PB12
	TSC_G3_IO3	PB2		TSC_G6_IO3	PB13
	TSC_G3_IO4	PC5		TSC_G6_IO4	PB14

Table 9. No. of capacitive sensing channels available on STM32F051xx devices

Analog I/O group	Number of capacitive sensing channels		
	STM32F051Rx	STM32F051Cx	STM32F051Kx
G1	3	3	3
G2	3	3	3
G3	3	2	2
G4	3	3	3
G5	3	3	3
G6	3	3	0
Number of capacitive sensing channels	18	17	14

4.19 Analog to digital converter (ADC)

The 12-bit analog to digital converter has up to 16 external and 3 internal (temperature sensor, voltage reference, VBAT voltage measurement) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

4.19.1 Temperature sensor

The temperature sensor generates a voltage that varies linearly with temperature. The conversion range is between 2 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

4.19.2 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC_IN18. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

4.20 Digital-to-analog converter (DAC)

The 12-bit buffered DAC channel can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This digital Interface supports the following features:

- Left or right data alignment in 12-bit mode
- Synchronized update capability
- DMA capability
- External triggers for conversion

Five DAC trigger inputs are used in the device. The DAC is triggered through the timer trigger outputs and the DAC interface is generating it's own DMA requests.

4.21 Fast low power comparators and reference voltage

The device embeds two fast rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pin
- Internal reference voltage or submultiple (1/4, 1/2, 3/4). Refer to *Table 22: Embedded internal reference voltage* for the value and precision of the internal reference voltage.

Both comparators can wake up from STOP mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

The internal voltage reference is also connected to ADC_IN17 input channel of the ADC.

4.21.1 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

5 Pinouts and pin description

Figure 3. LQFP64 64-pin package pinout

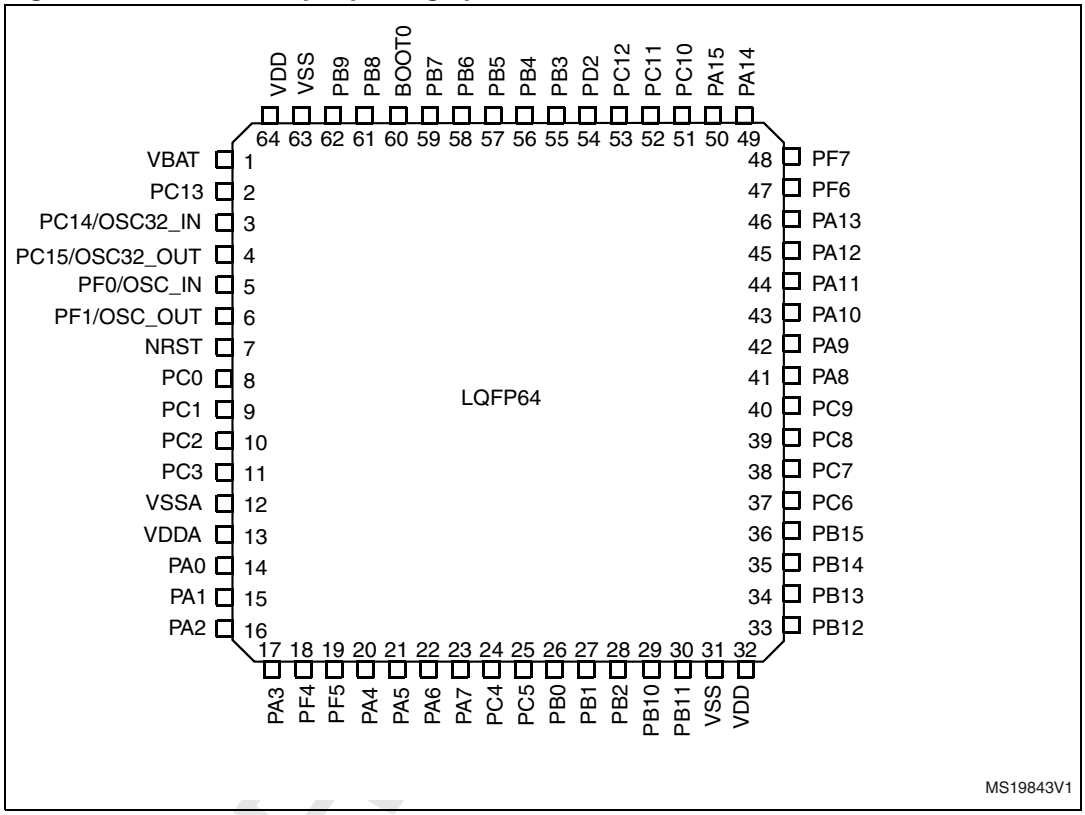


Figure 4. LQFP48 48-pin package pinout

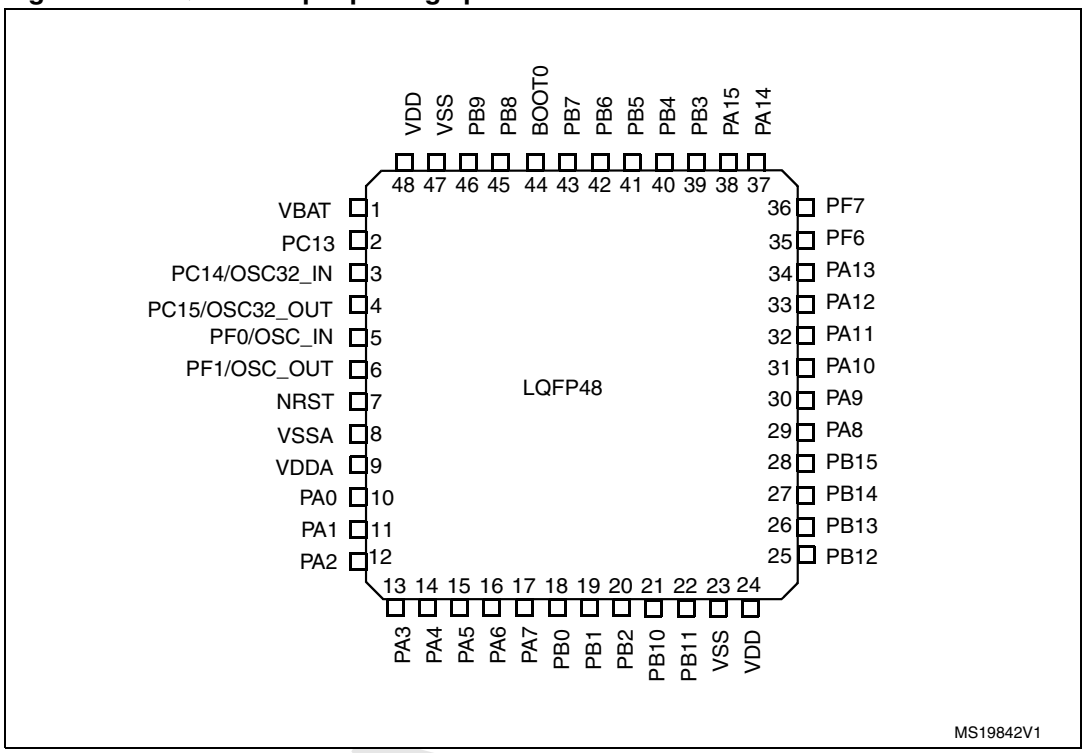


Figure 5. UFQFPN32 32-pin package pinout

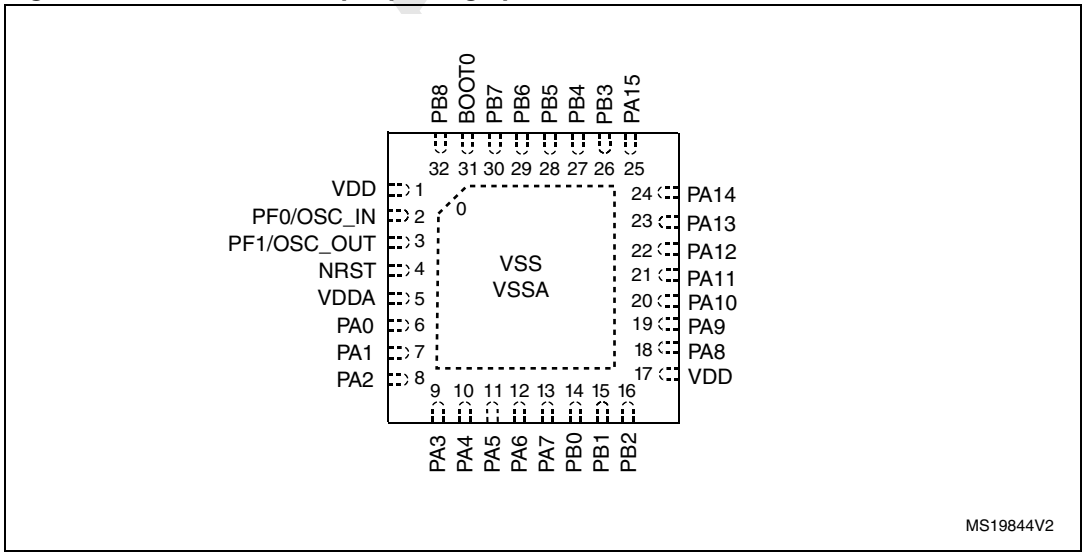


Table 10. Legend/abbreviations used in the pinout table

Name		Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type		S	Supply pin
		I	Input only pin
		I/O	Input / output pin
I/O structure		FT	5 V tolerant I/O
		FTf	5 V tolerant I/O, FM+ capable
		TTa	3.3 V tolerant I/O directly connected to ADC
		TC	Standard 3.3V I/O
		B	Dedicated BOOT0 pin
		RST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Pin functions	Alternate functions	Functions selected through GPIOx_AFR registers	
	Additional functions	Functions directly selected/enabled through peripheral registers	

Table 11. Pin definitions

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	UFQFPN32					Alternate functions	Additional functions
1	1		VBAT	S			Backup power supply	
2	2		PC13	I/O	TC	(1)(2)		RTC_TAMP1, RTC_TS, RTC_OUT, WKUP2
3	3		PC14-OSC32_IN (PC14)	I/O	TC	(1)(2)		OSC32_IN
4	4		PC15-OSC32_OUT (PC15)	I/O	TC	(1)(2)		OSC32_OUT
5	5	2	PF0-OSC_IN (PF0)	I/O	FT			OSC_IN
6	6	3	PF1-OSC_OUT (PF1)	I/O	FT			OSC_OUT
7	7	4	NRST	I/O	RST		Device reset input / internal reset output (active low)	

Table 11. Pin definitions (continued)

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	UFQFPN32					Alternate functions	Additional functions
8			PC0	I/O	TTa		EVENTOUT	ADC_IN10
9			PC1	I/O	TTa		EVENTOUT	ADC_IN11
10			PC2	I/O	TTa		EVENTOUT	ADC_IN12
11			PC3	I/O	TTa		EVENTOUT	ADC_IN13
12	8	0	VSSA	S			Analog ground	
13	9	5	VDDA	S			Analog power supply	
14	10	6	PA0	I/O	TTa		USART2_CTS, TIM2_CH1_ETR, COMP1_OUT, TSC_G1_IO1	ADC_IN0, COMP1_INM6, RTC_TAMP2, WKUP1
15	11	7	PA1	I/O	TTa		USART2_RTS, TIM2_CH2, TSC_G1_IO2, EVENTOUT	ADC_IN1, COMP1_INP
16	12	8	PA2	I/O	TTa		USART2_TX, TIM2_CH3, TIM15_CH1, COMP2_OUT, TSC_G1_IO3	ADC_IN2, COMP2_INM6
17	13	9	PA3	I/O	TTa		USART2_RX, TIM2_CH4, TIM15_CH2, TSC_G1_IO4	ADC_IN3, COMP2_INP
18			PF4	I/O	FT		EVENTOUT	
19			PF5	I/O	FT		EVENTOUT	
20	14	10	PA4	I/O	TTa		SPI1_NSS/I2S1_WS, USART2_CK, TIM14_CH1, TSC_G2_IO1	ADC_IN4, COMP1_INM4, COMP2_INM4, DAC1_OUT
21	15	11	PA5	I/O	TTa		SPI1_SCK/I2S1_CK, CEC, TIM2_CH_ETR, TSC_G2_IO2	ADC_IN5, COMP1_INM5, COMP2_INM5
22	16	12	PA6	I/O	TTa		SPI1_MISO/I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, COMP1_OUT, TSC_G2_IO3, EVENTOUT	ADC_IN6
23	17	13	PA7	I/O	TTa		SPI1_MOSI/I2S1_SD, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, COMP2_OUT, TSC_G2_IO4, EVENTOUT	ADC_IN7
24			PC4	I/O	TTa		EVENTOUT	ADC_IN14
25			PC5	I/O	TTa		TSC_G3_IO1	ADC_IN15
26	18	14	PB0	I/O	TTa		TIM3_CH3, TIM1_CH2N, TSC_G3_IO2, EVENTOUT	ADC_IN8

Table 11. Pin definitions (continued)

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	UFQFPN32					Alternate functions	Additional functions
27	19	15	PB1	I/O	TTa		TIM3_CH4, TIM14_CH1, TIM1_CH3N, TSC_G3_IO3	ADC_IN9
28	20	16	PB2	I/O	FT		TSC_G3_IO4	
29	21		PB10	I/O	FT		I2C2_SCL, CEC, TIM2_CH3, TSC_SYNC	
30	22		PB11	I/O	FT		I2C2_SDA, TIM2_CH4, TSC_G6_IO1, EVENTOUT	
31	23	0	VSS	S			Digital ground	
32	24	17	VDD	S			Digital power supply	
33	25		PB12	I/O	FT		SPI2_NSS, TIM1_BKIN, TSC_G6_IO2, EVENTOUT	
34	26		PB13	I/O	FT		SPI2_SCK, TIM1_CH1N, TSC_G6_IO3	
35	27		PB14	I/O	FT		SPI2_MISO, TIM1_CH2N, TIM15_CH1, TSC_G6_IO4	
36	28		PB15	I/O	FT		SPI2_MOSI, TIM1_CH3N, TIM15_CH1N, TIM15_CH2	RTC_REFIN
37			PC6	I/O	FT		TIM3_CH1	
38			PC7	I/O	FT		TIM3_CH2	
39			PC8	I/O	FT		TIM3_CH3	
40			PC9	I/O	FT		TIM3_CH4	
41	29	18	PA8	I/O	FT		USART1_CK, TIM1_CH1, EVENTOUT, MCO	
42	30	19	PA9	I/O	FT		USART1_TX, TIM1_CH2, TIM15_BKIN, TSC_G4_IO1	
43	31	20	PA10	I/O	FT		USART1_RX, TIM1_CH3, TIM17_BKIN, TSC_G4_IO2	
44	32	21	PA11	I/O	FT		USART1_CTS, TIM1_CH4, COMP1_OUT, TSC_G4_IO3, EVENTOUT	
45	33	22	PA12	I/O	FT		USART1_RTS, TIM1_ETR, COMP2_OUT, TSC_G4_IO4, EVENTOUT	
46	34	23	PA13 (SWDAT)	I/O	FT	(3)	IR_OUT, SWDAT	
47	35		PF6	I/O	FT		I2C2_SCL	
48	36		PF7	I/O	FT		I2C2_SDA	

Table 11. Pin definitions (continued)

Pin number			Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP64	LQFP48	UFQFPN32					Alternate functions	Additional functions
49	37	24	PA14 (SWCLK)	I/O	FT	(3)	USART2_TX, SWCLK	
50	38	25	PA15	I/O	FT		SPI1_NSS/I2S1_WS, USART2_RX, TIM2_CH_ETR, EVENTOUT	
51			PC10	I/O	FT			
52			PC11	I/O	FT			
53			PC12	I/O	FT			
54			PD2	I/O	FT		TIM3_ETR	
55	39	26	PB3	I/O	FT		SPI1_SCK/I2S1_CK, TIM2_CH2, TSC_G5_IO1, EVENTOUT	
56	40	27	PB4	I/O	FT		SPI1_MISO/I2S1_MCK, TIM3_CH1, TSC_G5_IO2, EVENTOUT	
57	41	28	PB5	I/O	FT		SPI1_MOSI/I2S1_SD, I2C1_SMBA, TIM16_BKIN, TIM3_CH2	
58	42	29	PB6	I/O	FTf		I2C1_SCL, USART1_TX, TIM16_CH1N, TSC_G5_IO3	
59	43	30	PB7	I/O	FTf		I2C1_SDA, USART1_RX, TIM17_CH1N, TSC_G5_IO4	
60	44	31	BOOT0	I	B		Boot memory selection	
61	45	32	PB8	I/O	FTf		I2C1_SCL, CEC, TIM16_CH1, TSC_SYNC	
62	46		PB9	I/O	FTf		I2C1_SDA, IR_OUT, TIM17_CH1, EVENTOUT	
63	47	0	VSS	S			Digital ground	
64	48	1	VDD	S			Digital power supply	

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIO PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF
   - these GPIOs must not be used as a current sources (e.g. to drive an LED).

2. After the first backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the Backup registers which is not reset by the main reset. For details on how to manage these GPIOs, refer to the Battery backup domain and BKP register description sections in the reference manual.

3. After reset, these pins are configured as SWDAT and SWCLK alternate functions, and the internal pull-up on SWDAT pin and internal pull-down on SWCLK pin are activated.

Table 12. Alternate functions selected through GPIOA_AFR registers for port A

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0		USART2_CTS	TIM2_CH1_ ETR	TSC_G1_IO1				COMP1_OUT
PA1	EVENTOUT	USART2_RTS	TIM2_CH2	TSC_G1_IO2				
PA2	TIM15_CH1	USART2_TX	TIM2_CH3	TSC_G1_IO3				COMP2_OUT
PA3	TIM15_CH2	USART2_RX	TIM2_CH4	TSC_G1_IO4				
PA4	SPI1_NSS/ I2S1_WS	USART2_CK		TSC_G2_IO1	TIM14_CH1			
PA5	SPI1_SCK/ I2S1_CK	CEC	TIM2_CH1_ ETR	TSC_G2_IO2				
PA6	SPI1_MISO/ I2S1_MCK	TIM3_CH1	TIM1_BKIN	TSC_G2_IO3		TIM16_CH1	EVENTOUT	COMP1_OUT
PA7	SPI1_MOSI/ I2S1_SD	TIM3_CH2	TIM1_CH1N	TSC_G2_IO4	TIM14_CH1	TIM17_CH1	EVENTOUT	COMP2_OUT
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT				
PA9	TIM15_BKIN	USART1_TX	TIM1_CH2	TSC_G4_IO1				
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3	TSC_G4_IO2				
PA11	EVENTOUT	USART1_CTS	TIM1_CH4	TSC_G4_IO3				COMP1_OUT
PA12	EVENTOUT	USART1_RTS	TIM1_ETR	TSC_G4_IO4				COMP2_OUT
PA13	SWDAT	IR_OUT						
PA14	SWCLK	USART2_TX						
PA15	SPI1_NSS/ I2S1_WS	USART2_RX	TIM2_CH1_ ETR	EVENTOUT				

Table 13. Alternate functions selected through GPIOB_AFR registers for port B

Pin name	AF0	AF1	AF2	AF3
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	TSC_G3_IO2
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TSC_G3_IO3
PB2				TSC_G3_IO4
PB3	SPI1_SCK/I2S1_CK	EVENTOUT	TIM2_CH2	TSC_G5_IO1
PB4	SPI1_MISO/I2S1_MCK	TIM3_CH1	EVENTOUT	TSC_G5_IO2
PB5	SPI1_MOSI/I2S1_SD	TIM3_CH2	TIM16_BKIN	I2C1_SMBA
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N	TSC_G5_IO3
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N	TSC_G5_IO4
PB8	CEC	I2C1_SCL	TIM16_CH1	TSC_SYNC
PB9	IR_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT
PB10	CEC	I2C2_SCL	TIM2_CH3	TSC_SYNC
PB11	EVENTOUT	I2C2_SDA	TIM2_CH4	TSC_G6_IO1
PB12	SPI2_NSS	EVENTOUT	TIM1_BKIN	TSC_G6_IO2
PB13	SPI2_SCK		TIM1_CH1N	TSC_G6_IO3
PB14	SPI2_MISO	TIM15_CH1	TIM1_CH2N	TSC_G6_IO4
PB15	SPI2_MOSI	TIM15_CH2	TIM1_CH3N	TIM15_CH1N

6 Memory mapping

Figure 6. STM32F051x memory map

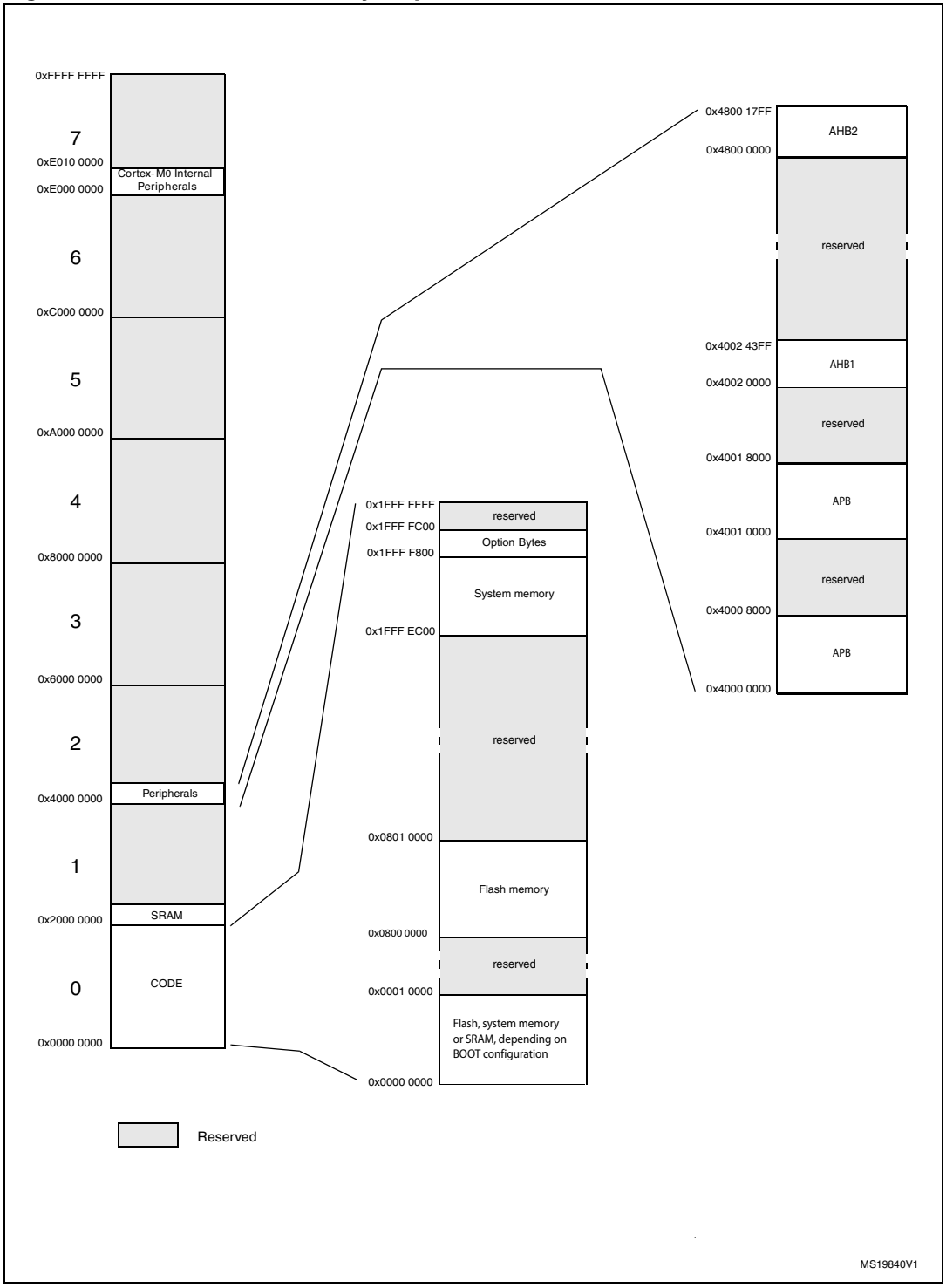


Table 14. STM32F051x peripheral register boundary addresses

Bus	Boundary address	Size	Peripheral
	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1KB	GPIOF
	0x4800 1000 - 0x4800 13FF	1KB	Reserved
	0x4800 0C00 - 0x4800 0FFF	1KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1KB	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1KB	TSC
	0x4002 3400 - 0x4002 3FFF	3KB	Reserved
	0x4002 3000 - 0x4002 33FF	1KB	CRC
	0x4002 2400 - 0x4002 2FFF	3KB	Reserved
	0x4002 2000 - 0x4002 23FF	1KB	FLASH Interface
	0x4002 1400 - 0x4002 1FFF	3KB	Reserved
	0x4002 1000 - 0x4002 13FF	1KB	RCC
	0x4002 0400 - 0x4002 0FFF	3KB	Reserved
	0x4002 0000 - 0x4002 03FF	1KB	DMA
	0x4001 8000 - 0x4001 FFFF	32KB	Reserved
APB	0x4001 5C00 - 0x4001 7FFF	9KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1KB	DBGMCU
	0x4001 4C00 - 0x4001 57FF	3KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1KB	TIM17
	0x4001 4400 - 0x4001 47FF	1KB	TIM16
	0x4001 4000 - 0x4001 43FF	1KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	1KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1KB	USART1
	0x4001 3400 - 0x4001 37FF	1KB	Reserved
	0x4001 3000 - 0x4001 33FF	1KB	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	1KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1KB	Reserved
	0x4001 2400 - 0x4001 27FF	1KB	ADC
	0x4001 0800 - 0x4001 23FF	7KB	Reserved
	0x4001 0400 - 0x4001 07FF	1KB	EXTI
	0x4001 0000 - 0x4001 03FF	1KB	SYSCFG + COMP
	0x4000 8000 - 0x4000 FFFF	32KB	Reserved

Table 14. STM32F051x peripheral register boundary addresses (continued)

Bus	Boundary address	Size	Peripheral
APB	0x4000 7C00 - 0x4000 7FFF	1KB	Reserved
	0x4000 7800 - 0x4000 7BFF	1KB	CEC
	0x4000 7400 - 0x4000 77FF	1KB	DAC
	0x4000 7000 - 0x4000 73FF	1KB	PWR
	0x4000 5C00 - 0x4000 6FFF	5KB	Reserved
	0x4000 5800 - 0x4000 5BFF	1KB	I2C2
	0x4000 5400 - 0x4000 57FF	1KB	I2C1
	0x4000 4800 - 0x4000 53FF	3 KB	Reserved
	0x4000 4400 - 0x4000 47FF	1KB	USART2
	0x4000 3C00 - 0x4000 43FF	2KB	Reserved
	0x4000 3800 - 0x4000 3BFF	1KB	SPI2
	0x4000 3400 - 0x4000 37FF	1KB	Reserved
	0x4000 3000 - 0x4000 33FF	1KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1KB	RTC
	0x4000 2400 - 0x4000 27FF	1KB	Reserved
	0x4000 2000 - 0x4000 23FF	1KB	TIM14
	0x4000 1400 - 0x4000 1FFF	3KB	Reserved
	0x4000 1000 - 0x4000 13FF	1KB	TIM6
	0x4000 0800 - 0x4000 0FFF	2KB	Reserved
	0x4000 0400 - 0x4000 07FF	1KB	TIM3
	0x4000 0000 - 0x4000 03FF	1KB	TIM2

7 Electrical characteristics

7.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

7.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

7.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

7.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

7.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 7*.

7.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 8*.

Figure 7. Pin loading conditions

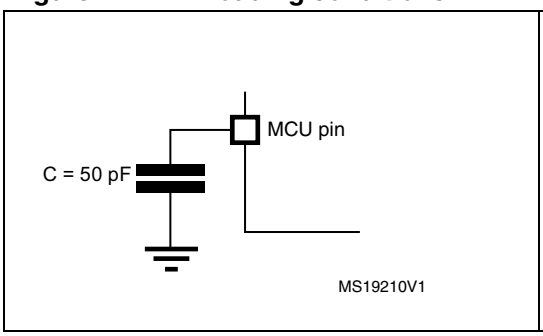
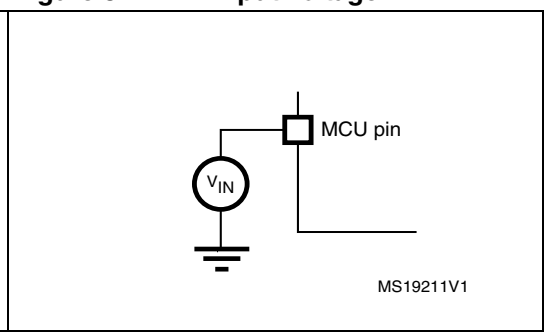
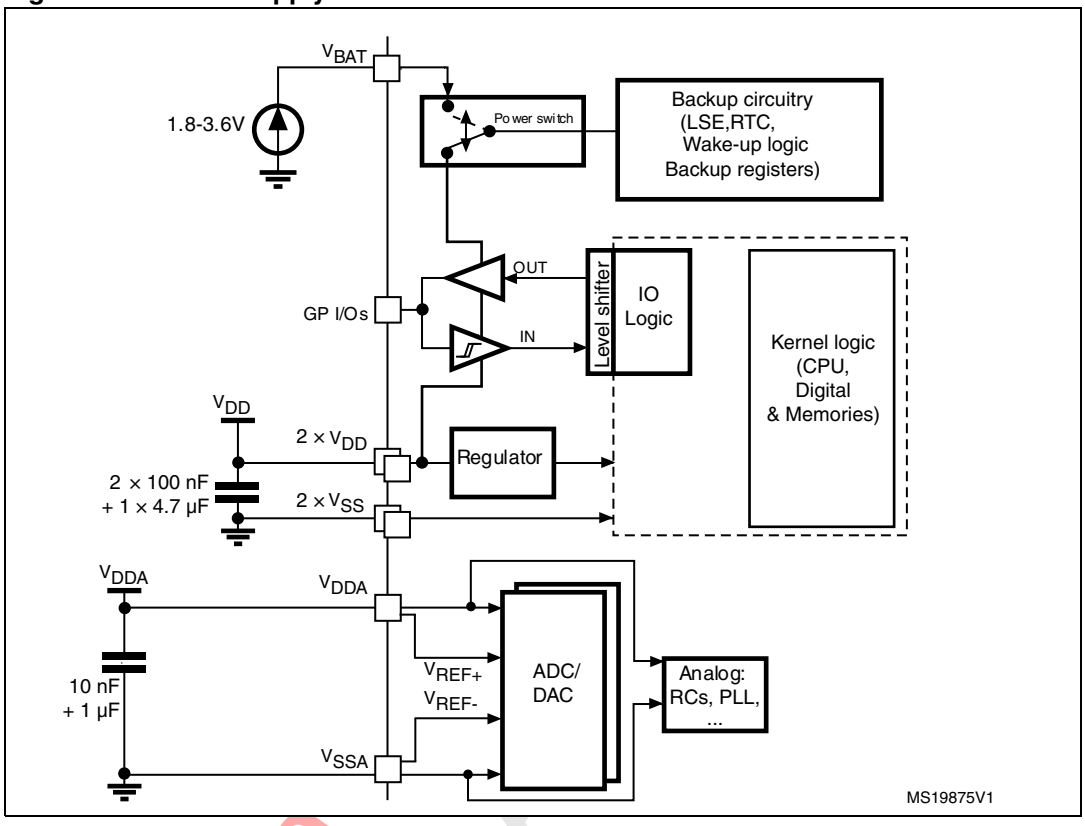


Figure 8. Pin input voltage



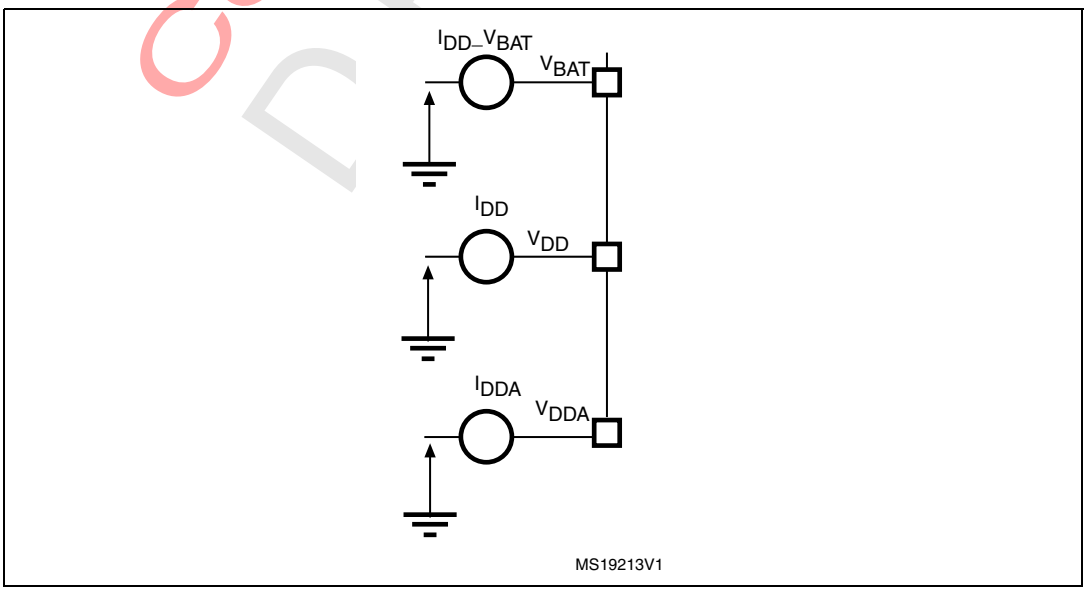
7.1.6 Power supply scheme

Figure 9. Power supply scheme



7.1.7 Current consumption measurement

Figure 10. Current consumption measurement scheme



7.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 15: Voltage characteristics*, *Table 16: Current characteristics*, and *Table 17: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 15. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})	–0.3	4.0	V
V_{DD}–V_{DDA}	Allowed voltage difference for $V_{DD} > V_{DDA}$		0.4	
V_{IN}(2)	Input voltage on FT and FTf pins	V_{SS} – 0.3	V_{DD} + 4.0	
	Input voltage on TTa pins	V_{SS} – 0.3	V_{DDA} + 0.3	
	Input voltage on any other pin	V_{SS} – 0.3	4.0	
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins		50	mV
$\lvert V_{SSX} - V_{SS}\rvert$	Variations between all the different ground pins		50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 7.3.11: Electrical sensitivity characteristics*		

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 16: Current characteristics* for the maximum allowed injected current values.

Table 16. Current characteristics(1)

Symbol	Ratings	Max.	Unit
I_{VDD}	Total current into V_{DD} power lines (source)(2)	TBD	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)(2)	TBD	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current source by any I/Os and control pin	– 25	
$I_{INJ(PIN)}$(3)	Injected current on FT, FTf, and TTa pins	-5/+NA(4)	
	Injected current on any other pin	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	± 25	

1. TBD stands for “to be defined”.
2. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
3. A positive injection is induced by $V_{IN}>V_{DD}$ while a negative injection is induced by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer also to *Table 15: Voltage characteristics* for the maximum allowed input voltage values. Negative injection disturbs the analog performance of the device. See note 2 below *Table 61 on page 81*.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 17. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

7.3 Operating conditions

7.3.1 General operating conditions

Table 18. General operating conditions(1)

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency		0	48	MHz
f_{PCLK}	Internal APB clock frequency		0	48	
V_{DD}	Standard operating voltage		2	3.6	V
V_{DDA}(2)	Analog operating voltage (ADC and DAC not used)	Must have a potential equal to or higher than V_{DD}	2	3.6	V
	Analog operating voltage (ADC and DAC used)		2.4	3.6	
V_{BAT}	Backup operating voltage		1.8	3.6	V
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(3)	LQFP64		TBD	mW
		LQFP48		TBD	
		UFQFPN32		TBD	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low power dissipation(4)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low power dissipation(4)	–40	125	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. TBD stands for “to be defined”.
2. When the ADC is used, refer to *Table 59: ADC characteristics*.
3. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see *Table 17: Thermal characteristics*).
4. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Table 17: Thermal characteristics*).

7.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 19* are derived from tests performed under the ambient temperature condition summarized in *Table 18*.

Table 19. Operating conditions at power-up / power-down(1)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate		TBD		µs/V
	V_{DD} fall time rate		TBD		
t_{VDDA}	V_{DDA} rise time rate		TBD		
	V_{DDA} fall time rate		TBD		

1. TBD stands for “to be defined”.

7.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 20* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 18*.

Table 20. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	Power on/power down reset threshold	Falling edge	1.8(2)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$(1)	PDR hysteresis			40		mV
$t_{RSTTEMPO}$(3)	Reset temporization		1.5	2.5	4.5	ms

1. The PDR detector monitors V_{DD} and also V_{DDA} (if kept enabled in the option bytes). The POR detector monitors only V_{DD}.
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Guaranteed by design, not tested in production.

Table 21. Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min(1)	Typ	Max(1)	Unit
V_{PVD0}	PVD threshold 0	Rising edge	2.1	2.18	2.26	V
		Falling edge	2	2.08	2.16	V
V_{PVD1}	PVD threshold 1	Rising edge	2.19	2.28	2.37	V
		Falling edge	2.09	2.18	2.27	V
V_{PVD2}	PVD threshold 2	Rising edge	2.28	2.38	2.48	V
		Falling edge	2.18	2.28	2.38	V
V_{PVD3}	PVD threshold 3	Rising edge	2.38	2.48	2.58	V
		Falling edge	2.28	2.38	2.48	V
V_{PVD4}	PVD threshold 4	Rising edge	2.47	2.58	2.69	V
		Falling edge	2.37	2.48	2.59	V
V_{PVD5}	PVD threshold 5	Rising edge	2.57	2.68	2.79	V
		Falling edge	2.47	2.58	2.69	V
V_{PVD6}	PVD threshold 6	Rising edge	2.66	2.78	2.9	V
		Falling edge	2.56	2.68	2.8	V
V_{PVD7}	PVD threshold 7	Rising edge	2.76	2.88	3	V
		Falling edge	2.66	2.78	2.9	V
$V_{PVDhyst}$(2)	PVD hysteresis			100		mV

1. Data based on characterization results only, not tested in production.
2. Guaranteed by design, not tested in production.

7.3.4 Embedded reference voltage

The parameters given in *Table 22* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 18*.

Table 22. Embedded internal reference voltage(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.16	1.2	1.25	V
		–40 °C < T_A < +85 °C	1.16	1.2	1.24(2)	V
$T_{S\_vrefint}$(3)	ADC sampling time when reading the internal reference voltage			5.1	17.1(4)	µs
V_{RERINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V ±10 mV			10(4)	mV
T_{Coeff}	Temperature coefficient				100(4)	ppm/°C

1. TBD stands for “to be defined”.
2. Data based on characterization results, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.
4. Guaranteed by design, not tested in production.

7.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 10: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark x.x code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency (0 wait state from 0 to 24 MHz and 1 wait state from 24 to 48 MHz)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The parameters given in *Table 23* to *Table 27* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 18*.

Table 23. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(1)			Typ	Max @ T_A(1)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, executing from Flash	External clock (HSE bypass)	48 MHz	21.2				11.5				mA
			32 MHz	14.3				7.8				
			24 MHz	12.2				7.2				
			8 MHz	4.4				2.7				
			1 MHz	1				0.7				
		Internal clock (HSI)	48 MHz	21.2				11.4				
			32 MHz	14.3				7.9				
			24 MHz	12.2				7.2				
			8 MHz	4.3				2.7				
	Supply current in Run mode, executing from RAM	External clock (HSE bypass)	48 MHz	22	TBD(2)		24	12	TBD(2)		14	
			32 MHz	14.7				8				
			24 MHz	11.2				6.2				
			8 MHz	3.9				2.2				
			1 MHz	0.6				0.5				
		Internal clock (HSI)	48 MHz	22				12				
			32 MHz	15				8				
			24 MHz	11				6.5				
			8 MHz	4				2.5				
	Supply current in Sleep mode, executing from Flash or RAM	External clock (HSE bypass)	48 MHz	12.2	TBD(2)		14.5	2.8	TBD(2)		3.7	
			32 MHz	8.3				2				
			24 MHz	6.4				1.5				
			8 MHz	2.2				0.6				
			1 MHz	0.6				0.2				
		Internal clock (HSI)	48 MHz	14				3				
			32 MHz	9.5				2				
			24 MHz	7.3				1.5				
			8 MHz	2.6				0.65				

1. Data based on characterization results, not tested in production unless otherwise specified.
2. Data based on characterization results and tested in production.

Table 24. Typical and maximum current consumption from V_{DDA} supply at V_{DDA} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(1)			Typ	Max @ T_A(1)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run mode, executing from Flash	External clock (HSE bypass)	48 MHz	341				260				mA
			32 MHz	289				208				
			24 MHz	265				183				
			8 MHz	178				98				
			1 MHz	178				98				
		Internal clock (HSI)	48 MHz	340				340				
			32 MHz	290				290				
			24 MHz	264				264				
			8 MHz	180				180				
	Supply current in Run mode, executing from RAM	External clock (HSE bypass)	48 MHz	340	TBD(2)		TBD(2)	261	TBD(2)		TBD(2)	
			32 MHz	290				208				
			24 MHz	265				184				
			8 MHz	178				98				
			1 MHz	178				98				
		Internal clock (HSI)	48 MHz	341				341				
			32 MHz	290				290				
			24 MHz	265				265				
			8 MHz	179				178				
	Supply current in Sleep mode, executing from Flash or RAM	External clock (HSE bypass)	48 MHz	340	TBD(2)		TBD(2)	340	TBD(2)		TBD(2)	
			32 MHz	289				209				
			24 MHz	265				184				
			8 MHz	179				98				
			1 MHz	179				98				
		Internal clock (HSI)	48 MHz	341				341				
			32 MHz	290				289				
			24 MHz	264				264				
			8 MHz	178				178				

1. Data based on characterization results, not tested in production unless otherwise specified.
2. Data based on characterization results and tested in production.

Table 25. Typical and maximum current consumption from the V_{DDA} supply at V_{DDA} = 2.4 V

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled				All peripherals disabled				Unit
				Typ	Max @ T_A(1)			Typ	Max @ T_A(1)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run mode, executing from Flash	External clock (HSE bypass)	48 MHz	285				215				mA
			32 MHz	237				167				
			24 MHz	215				145				
			8 MHz	135				65				
			1 MHz	135				65				
		Internal clock (HSI)	48 MHz	285				285				
			32 MHz	235				235				
			24 MHz	215				215				
			8 MHz	135				135				
	Supply current in Run mode, executing from RAM	External clock (HSE bypass)	48 MHz	285				215				
			32 MHz	238				168				
			24 MHz	215				145				
			8 MHz	135				65				
			1 MHz	135				65				
		Internal clock (HSI)	48 MHz	286				286				
			32 MHz	238				238				
			24 MHz	215				215				
			8 MHz	135				135				
	Supply current in Sleep mode, executing from Flash or RAM	External clock (HSE bypass)	48 MHz	285				215				
			32 MHz	238				168				
			24 MHz	215				145				
			8 MHz	135				65				
			1 MHz	135				65				
		Internal clock (HSI)	48 MHz	285				285				
			32 MHz	238				238				
			24 MHz	215				215				
			8 MHz	135				135				

1. Data based on characterization results, not tested in production.

Table 26. Typical and maximum current consumptions in Stop and Standby modes(1)

Symbol	Parameter	Conditions	Typ @V_{DD} or V_{DDA}				Max			Unit
			= 2.0 V	= 2.4 V	= 2.7 V	= 3.6 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF				19	TBD	TBD(2)	70	µA
		Regulator in low-power mode, all oscillators OFF				3.7	TBD	TBD(2)	55	
	Supply current in Standby mode	LSI and IWDG ON								
		LSI and IWDG OFF				1.3	TBD	TBD(2)	7	
I_{DDA}	Supply current in Stop mode	Regulator in run mode, all oscillators OFF				3	TBD	TBD(2)	TBD	
		Regulator in low-power mode, all oscillators OFF				2.7	TBD	TBD(2)	TBD	
	Supply current in Standby mode	LSI and IWDG ON								
		LSI and IWDG OFF				2.5	TBD	TBD(2)	TBD	

1. TBD stands for “to be defined”.
2. Data based on characterization results, not tested in production.

Table 27. Typical and maximum current consumption from V_{BAT} supply(1)

Symbol	Parameter	Conditions	Typ @ V_{BAT}				Max			Unit
			= 1.8 V	= 2.4 V	= 2.7 V	= 3.3 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_VBAT}	Backup domain supply current	LSE & RTC ON; "Xtal mode": lower driving capability; LSEDRV[4:3] = '00'	0.43	0.53		0.71		TBD(2)	TBD(2)	µA
		LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[4:3] = '11'	0.75	0.85		1.06				

1. TBD stands for “to be defined”.
2. Data based on characterization results, not tested in production.

Typical current consumption

The measurement of the typical current consumption of the MCU in *Table 28* has been done under the following conditions:

- All I/O pins are in analog input configuration
- The Flash access time is adjusted to the f_{HCLK} frequency (0 wait states from 0 to 24 MHz, 1 wait state from 24 to 48 MHz).
- The HSI oscillator is off
- When the peripherals are enabled, $f_{PCLK} = f_{HCLK}$
- T_A= 25 °C ,V_{DDA}=3.3 V and V_{DD} = 3.3 V unless otherwise specified.
- An 8 MHz crystal is used as the PLL input clock source
- PLL output is selected as SYSCLK for frequencies greater than 8 MHz, f_{CLK} = SYSCLK
- HSE is selected as SYSCLK for frequencies below 8 MHz, f_{CLK} = SYSCLK / N
- AHB prescaler “N” is 1, 2, 4, 8 and 16 for the frequencies 8 MHz, 4 MHz, 2 MHz, 1 MHz and 500 KHz respectively
- A development tool (ULINK) is connected to the board and the parasitic pull-up current is around 30 µA

Table 28. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions		f_{HCLK}	Typ		Unit
					I_{DD}	I_{DDA}	
I_{DD}/I_{DDA}	Supply current in Run mode	Code running from Flash, prefetch off, all peripherals are off	1 wait state	48 MHz	11.45	158	mA
				36 MHz	9	120	
				32 MHz	8.05	108	
			No wait states	24 MHz	7.49	83	
				16 MHz	5.24	60	
			PLL off, no wait states	8 MHz	2.97	2.43	
				4 MHz	1.9	2.43	
				2 MHz	1.31	2.43	
				1 MHz	1.025	2.43	
				500 kHz	0.88	2.43	
		Code running from Flash, prefetch on, all peripherals are on	1 wait state	48 MHz	23.26	158	
				36 MHz	17.63	120	
				32 MHz	15.9	108	
			No wait states	24 MHz	12.4	83	
				16 MHz	8.5	60	
			PLL off, no wait states	8 MHz	4.53	2.43	
				4 MHz	2.77	2.43	
				2 MHz	1.74	2.43	
				1 MHz	1.25	2.43	
				500 kHz	0.995	2.43	

Table 29. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ				Unit
				All peripherals enabled(1)		All peripherals disabled		
				I_{DD}	I_{DDA}	I_{DD}	I_{DDA}	
I_{DD}/I_{DDA}	Supply current in Sleep mode	External clock(2)	48 MHz					mA
			36 MHz					
			24 MHz					
			16 MHz					
			8 MHz					
			4 MHz					
			2 MHz					
			1 MHz					
			500 kHz					
			125 kHz					
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	48 MHz					
			36 MHz					
			24 MHz					
			16 MHz					
			8 MHz					
			4 MHz					
			2 MHz					
			1 MHz					
			500 kHz					
			125 kHz					

1. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
2. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 48: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see *Table 31: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 30. Switching output I/O current consumption(1)

Symbol	Parameter	Conditions	I/O toggling frequency (f_{SW})	Typ	Unit
I_{DDIO}	Supply current	V_{DD} = 3.3 V C_{ext} = 20 pF	TBD	TBD	mA
			TBD	TBD	
			TBD	TBD	
			TBD	TBD	
			TBD	TBD	
		V_{DD} = 3.3 V C_{ext} = 50 pF	TBD	TBD	
			TBD	TBD	
			TBD	TBD	
			TBD	TBD	
			TBD	TBD	
		V_{DD} = 2.4V C_{ext} = 20pF	TBD	TBD	
			TBD	TBD	
			TBD	TBD	
			TBD	TBD	
			TBD	TBD	
		V_{DD} = 2.4V C_{ext} = 50pF	TBD	TBD	
			TBD	TBD	
			TBD	TBD	
			TBD	TBD	
			TBD	TBD	

1. TBD stands for “to be defined”.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 31*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions summarized in *Table 15*

Table 31. Peripheral current consumption(1)

Peripheral	Typical consumption at 25 °C		Unit
	I_{DD}	I_{DDA}	
ADC(2)	0.53	0.964	mA
CEC	0.24		
CRC	0.10		
DAC(3)	0.27	0.408	
DBGMCU	0.18		
DMA	0.35		
GPIOA	0.48		
GPIOB	0.58		
GPIOC	0.12		
GPIOD	0.04		
GPIOF	0.06		
I2C1	0.43		
I2C2	0.42		
PWR	0.22		
SPI1/I2S1	0.63		
SPI2	0.53		
SYSCFG & COMP	0.28	COMP I_{DDA} is specified as I_{COMP} in *Table 63: Comparator characteristics*	
TIM1	1.01		
TIM2	1.00		
TIM3	0.78		
TIM6	0.32		
TIM14	0.45		
TIM15	0.66		
TIM16	0.57		
TIM17	0.59		
TSC	0.28		
USART1	1.07		
USART2	0.48		
WWDG	0.22		

1. f_{HCLK} = 48 MHz, $f_{PCLK} = f_{HCLK}$, default prescaler value for each peripheral.
2. ADC is in ready state after setting the ADEN bit in the ADC_CR register (ADRDY bit in ADC_ISR is high).
3. DAC channel 1 enabled by setting EN1 bit in DAC_CR.

7.3.6 External clock source characteristics

High-speed external user clock generated from an external source

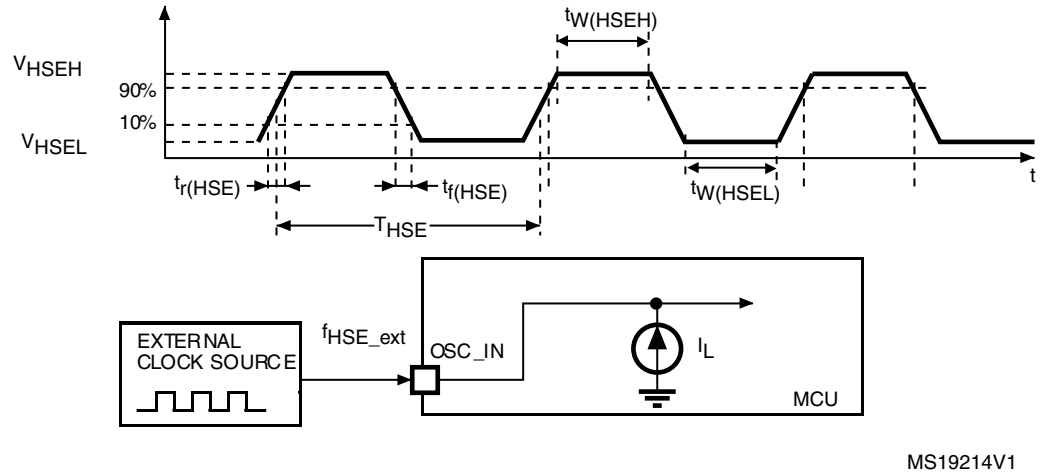
The characteristics given in *Table 32* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 18*.

Table 32. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)		1	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time(1)		15			ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)				20	
$C_{in(HSE)}$	OSC_IN input capacitance(1)			5		pF
I_L	OSC_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			±1	µA

1. Guaranteed by design, not tested in production.

Figure 11. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

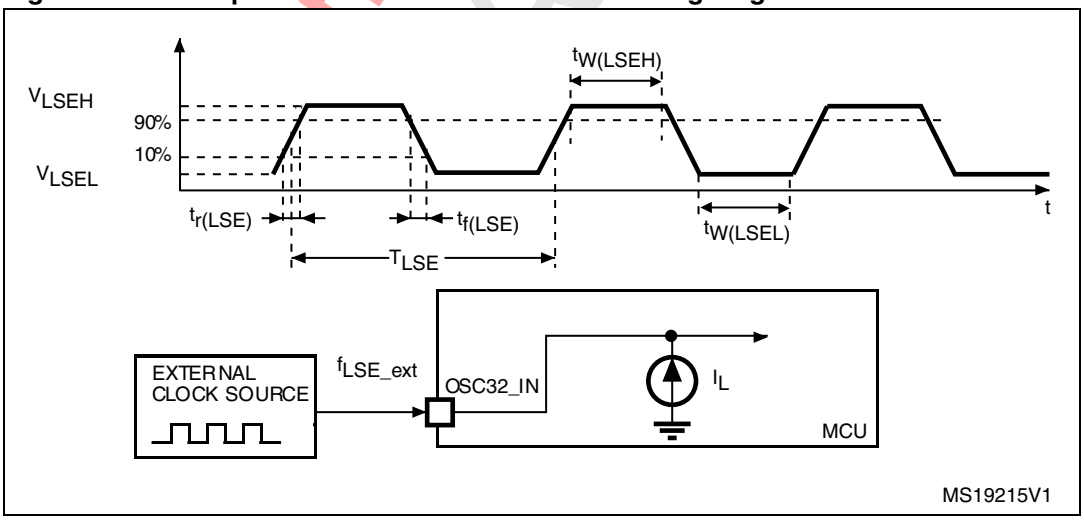
The characteristics given in *Table 33* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 18*.

Table 33. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)			32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$		V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}		$0.3V_{DD}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time(1)		450			ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)				50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)			5		pF
I_L	OSC32_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$			±1	µA

1. Guaranteed by design, not tested in production.

Figure 12. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 34*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

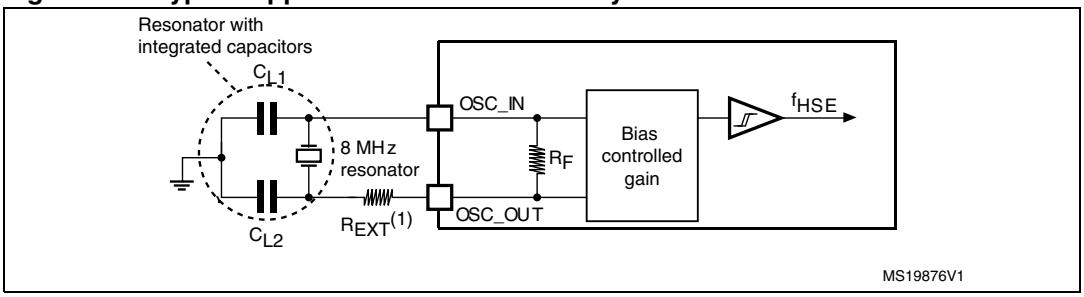
Table 34. HSE oscillator characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		4	8	32	MHz
R_F	Feedback resistor			200		kΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω		30		pF
I_D	HSE driving current	V_{DD}= 3.3 V, V_{IN} = V_{SS} with 30 pF load			TBD	mA
g_m	Oscillator transconductance	Startup	TBD			mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized		2		ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Data based on characterization results, not tested in production.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 13*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 13. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 35*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 35. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)(2)

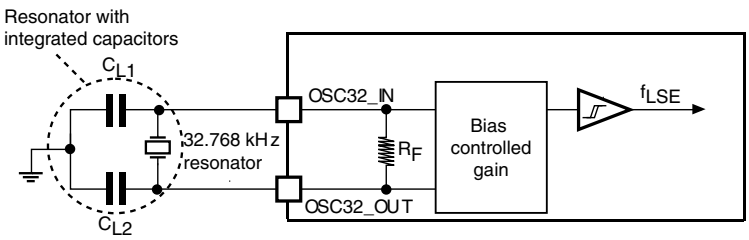
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_F	Feedback resistor				TBD		MΩ
C_{L1}, C_{L2}	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)	R_S = 30 kΩ				TBD	pF
I_D	LSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS}				TBD	µA
g_m	Oscillator transconductance			TBD			µA/V
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	T_A = 50 °C		TBD		s
			T_A = 25 °C		TBD		
			T_A = 10 °C		TBD		
			T_A = 0 °C		TBD		
			T_A = -10 °C		TBD		
			T_A = -20 °C		TBD		
			T_A = -30 °C		TBD		
			T_A = -40 °C		TBD		

1. Data based on characterization results, not tested in production.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see Figure 14). C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.
Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF) it is strongly recommended to use a resonator with a load capacitance $C_L \leq$ 7 pF. Never use a resonator with a load capacitance of 12.5 pF.
Example: if you choose a resonator with a load capacitance of C_L = 6 pF, and C_{stray} = 2 pF, then C_{L1} = C_{L2} = 8 pF.

Figure 14. Typical application with a 32.768 kHz crystal



7.3.7 Internal clock source characteristics

The parameters given in *Table 36* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 18*.

High-speed internal (HSI) RC oscillator

Table 36. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency			8		MHz
TRIM	HSI user trimming step				1(2)	%
$DuCy_{(HSI)}$	Duty cycle		45(2)		55(2)	%
ACC_{HSI}	Accuracy of the HSI oscillator (factory calibrated)	T_A = –40 to 105 °C	–2(3)		2.5(3)	%
		T_A = –10 to 85 °C	–1.5(3)		2.2(3)	%
		T_A = 0 to 70 °C	–1.3(3)		2(3)	%
		T_A = 25 °C	–1.1		1.8	%
$t_{su(HSI)}$	HSI oscillator startup time		1(2)		2(2)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption			80	100(2)	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

High-speed internal 14 MHz (HSI14) RC oscillator (dedicated to ADC)

Table 37. HSI14 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency			14		MHz
TRIM	HSI14 user-trimming step				1(2)	%
$DuCy_{(HSI)}$	Duty cycle		45(2)		55(2)	%
ACC_{HSI14}	Accuracy of the HSI14 oscillator (factory calibrated)	T_A = –40 to 105 °C	TBD		TBD	%
		T_A = –10 to 85 °C	TBD		TBD	%
		T_A = 0 to 70 °C	TBD		TBD	%
		T_A = 25 °C	TBD		TBD	%
$t_{su(HSI14)}$	HSI oscillator startup time		1(2)		2(2)	µs
$I_{DD(HSI14)}$	HSI oscillator power consumption			80	100(2)	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

Low-speed internal (LSI) RC oscillator

Table 38. LSI oscillator characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	35	40	55	kHz
$t_{su(LSI)}$(2)	LSI oscillator startup time			85	µs
$I_{DD(LSI)}$(2)	LSI oscillator power consumption		0.75	1.2	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.

Wakeup time from low-power mode

The wakeup times given in *Table 39* is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 18*.

Table 39. Low-power mode wakeup timings(1)

Symbol	Parameter	Typ	Max	Unit
$t_{WUSLEEP}$(2)	Wakeup from Sleep mode	TBD	-	µs
t_{WUSTOP}(2)	Wakeup from Stop mode (regulator in run mode)	4	TBD	µs
	Wakeup from Stop mode (regulator in low power mode)	6	TBD	
$t_{WUSTDBY}$(2)	Wakeup from Standby mode	TBD	TBD	µs

1. TBD stands for “to be defined”.
2. The wakeup times are measured from the wakeup event to the point in which the user application code reads the first instruction.

7.3.8 PLL characteristics

The parameters given in *Table 40* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 18*.

Table 40. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock(1)	1(2)		24(2)	MHz
	PLL input clock duty cycle	40(2)		60(2)	%
f_{PLL_OUT}	PLL multiplier output clock	16(2)		48	MHz
t_{LOCK}	PLL lock time			TBD(2)	µs
Jitter	Cycle-to-cycle jitter			TBD(2)	ps

1. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.
2. Guaranteed by design, not tested in production.

7.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 41. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	52.5	70	µs
t_{ERASE}	Page (1 KB) erase time	T_A = –40 to +105 °C	20		40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20		40	ms
I_{DD}	Supply current	Read mode f_{HCLK} = 48 MHz with 1 wait state, V_{DD} = 3.3 V			28	mA
		Write mode f_{HCLK} = 48 MHz, V_{DD} = 3.3 V			7	mA
		Erase mode f_{HCLK} = 48 MHz, V_{DD} = 3.3 V			5	mA
		Power-down / Halt mode, V_{DD} = 3.0 to 3.6 V			50	µA
V_{prog}	Programming voltage		2		3.6	V

1. Guaranteed by design, not tested in production.

Table 42. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value Min(1)	Unit
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycles(2) at T_A = 55 °C	20	

1. Data based on characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

7.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 43*. They are based on the EMS levels and classes defined in application note AN1709.

Table 43. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP64, T_A = +25 °C, f_{HCLK} = 48 MHz conforms to IEC 61000-4-2	TBD
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP64, T_A = +25 °C, f_{HCLK} = 48 MHz conforms to IEC 61000-4-4	TBD

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 44. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]		Unit
				8/48 MHz	TBD	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, LQFP64 package compliant with IEC 61967-2	0.1 to 30 MHz	8	TBD	dBµV
			30 to 130 MHz	31	TBD	
			130 MHz to 1GHz	28	TBD	
			SAE EMI Level	4	TBD	-

7.3.11 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 45. ESD absolute maximum ratings(1)

Symbol	Ratings	Conditions	Class	Maximum value(2)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to JESD22-A114	2	TBD	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to JESD22-C101	II	TBD	

1. TBD stands for “to be defined”.
2. Data based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 46. Electrical sensitivities(1)

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	TBD

1. TBD stands for “to be defined”.

7.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 47*

Table 47. I/O current injection susceptibility(1)

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	TBD	TBD	mA
	Injected current on all FT pins	TBD	TBD	
	Injected current on all FTf pins	TBD	TBD	
	Injected current on all TTa pins	TBD	TBD	
	Injected current on any other pin	TBD	TBD	

1. TBD stands for “to be defined”.

7.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 48* are derived from tests performed under the conditions summarized in *Table 18*. All I/Os are CMOS and TTL compliant.

Table 48. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard I/O input low level voltage		–0.3		0.28*(V_{DD}-2 V) +0.8 V	V
	FT and FTf(1) I/O input low level voltage		–0.3		0.32*(V_{DD}-2V) +0.75 V	
	TTa I/O input low level voltage		TBD		TBD	
V_{IH}	Standard I/O input high level voltage		0.41*(V_{DD}-2 V)+1.3 V		V_{DD}+0.3	
	FT and FTf(1) I/O input high level voltage	V_{DD} > 2 V	0.42*(V_{DD}-2 V)+1 V		5.5	
		V_{DD} = 2 V			5.2	
	TTa I/O input low level voltage		TBD		TBD	
V_{hys}	Standard I/O Schmitt trigger voltage hysteresis(2)		200			mV
	FT and FTf I/O Schmitt trigger voltage hysteresis(2)		5% V_{DD}(3)			
	TTa I/O input low level voltage		TBD		TBD	
I_{lkg}	Input leakage current (4)	$V_{SS} \le V_{IN} \le V_{DD}$ Standard I/Os			±1	µA
		V_{IN}= 5 V, I/O FT and FTf			3	
		V_{IN}= TBD, I/O TTa			TBD	
R_{PU}	Weak pull-up equivalent resistor(5)	$V_{IN} = V_{SS}$	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN} = V_{DD}$	30	40	50	kΩ
C_{IO}	I/O pin capacitance			5		pF

1. To sustain a voltage higher than V_{DD}+0.3 the internal pull-up/pull-down resistors must be disabled.
2. Hysteresis voltage between Schmitt trigger switching levels. Data based on characterization, not tested in production.
3. With a minimum of 100 mV.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 15* and *Figure 16* for standard I/Os, and in *Figure 17* and *Figure 18* for 5 V tolerant I/Os.

Figure 15. Standard I/O input characteristics - CMOS port

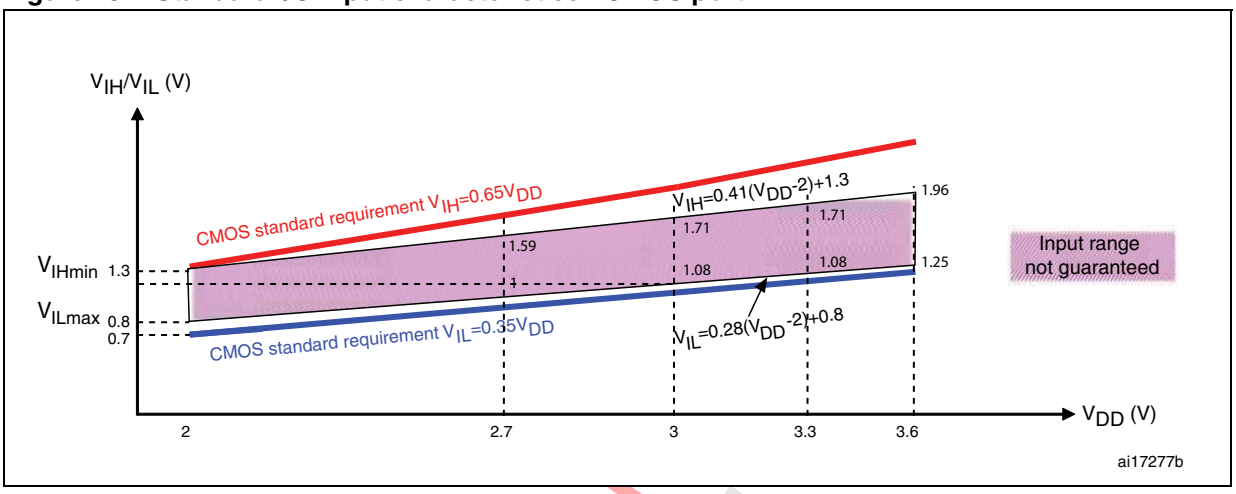


Figure 16. Standard I/O input characteristics - TTL port

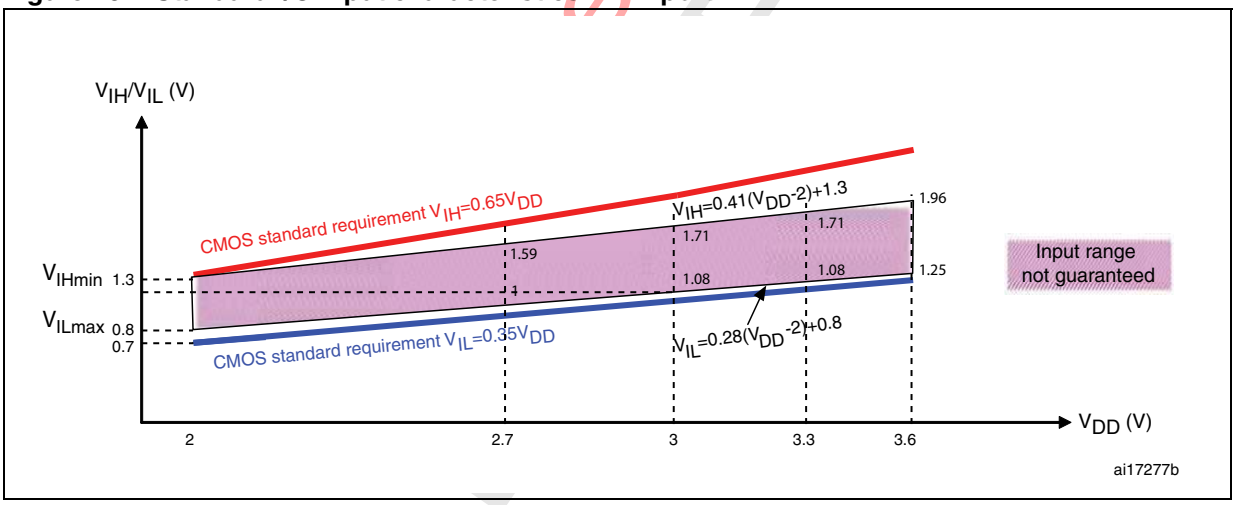


Figure 17. FT and FTf I/O input characteristics - CMOS port

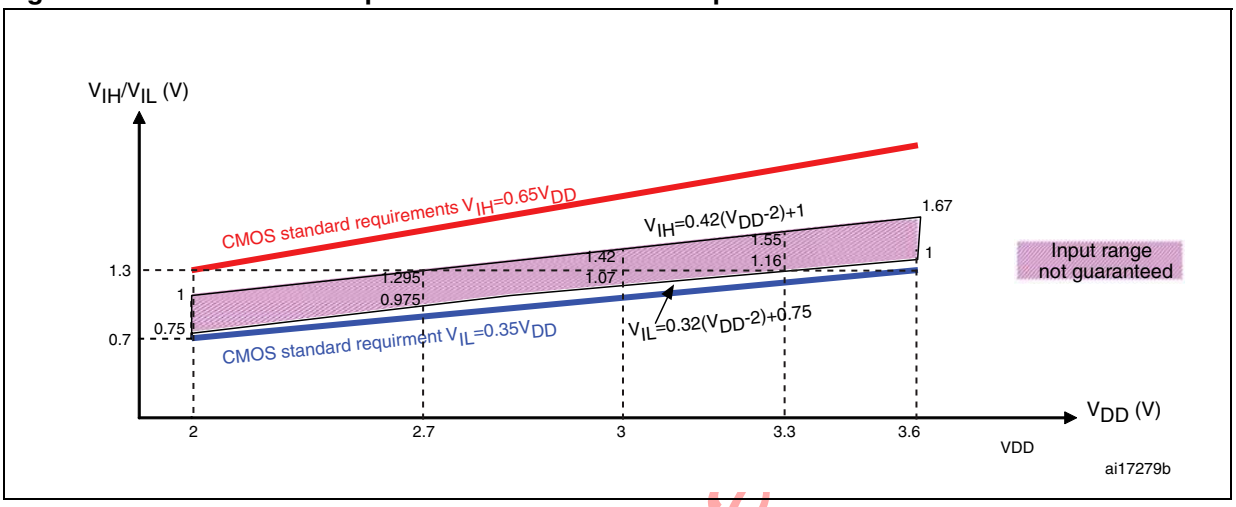


Figure 18. FT and FTf I/O input characteristics - TTL port

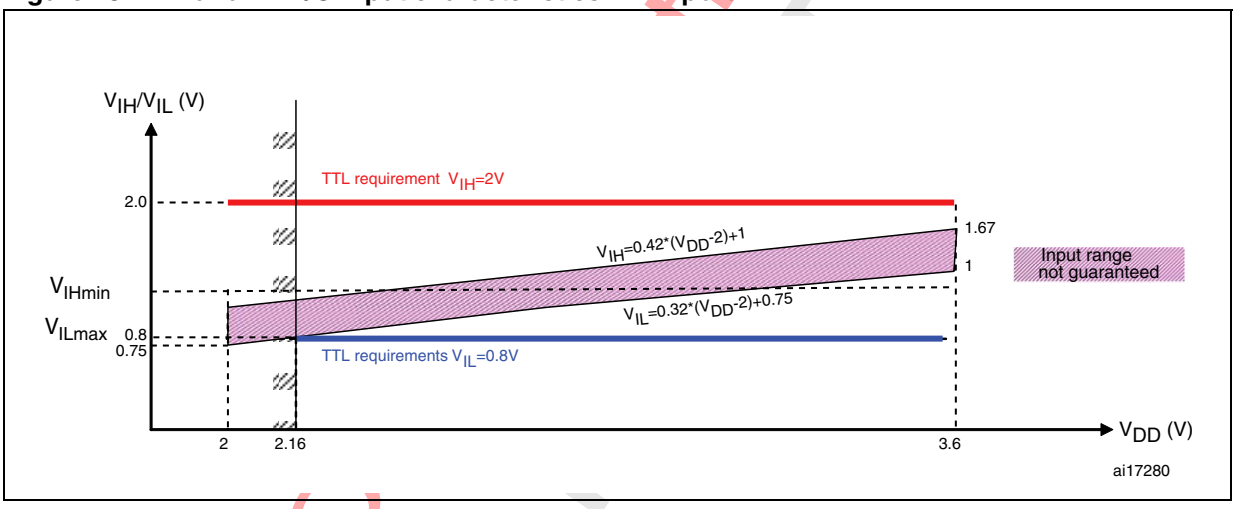
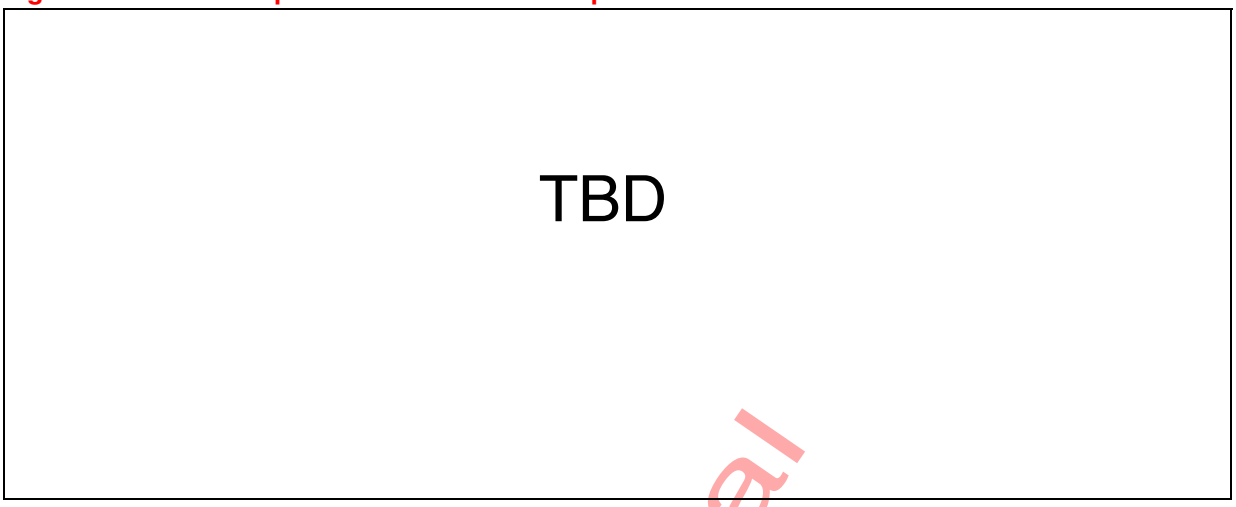


Figure 19. TTa I/O input characteristics - CMOS port

TBD

Figure 20. TTa I/O input characteristics - TTL port



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 7.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 16*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 16*).

Output voltage levels

Unless otherwise specified, the parameters given in *Table 49* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 18*. All I/Os are CMOS and TTL compliant.

Table 49. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS port(2) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V		TBD	V
V_{OH}(3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		TBD		
V_{OL} (1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL port(2) I_{IO} =+ 8mA 2.7 V < V_{DD} < 3.6 V		TBD	V
V_{OH} (3)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		TBD		
V_{OL}(1)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V		TBD	V
V_{OH}(3)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		TBD		
V_{OL}(1)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V		TBD	V
V_{OH}(3)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		TBD		
V_{OLFM+}	Output low level voltage for a FTf I/O pins in FM+ mode	TBD			V

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 16* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Data based on characterization results, not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 21* and *Table 50*, respectively.

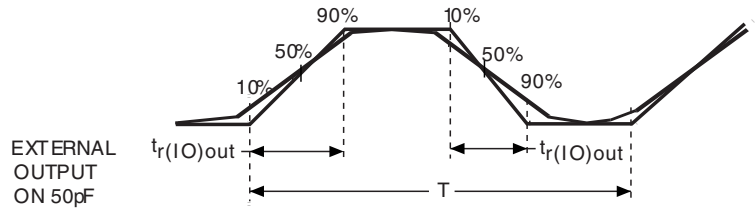
Unless otherwise specified, the parameters given are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 18*.

Table 50. I/O AC characteristics(1)

OSPEEDRy [1:0] value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V		2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V		125(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time			125(3)	
01	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 50 pF, V_{DD} = 2 V to 3.6 V		10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V		25(3)	ns
	$t_{r(IO)out}$	Output low to high level rise time			25(3)	
11	$f_{max(IO)out}$	Maximum frequency(2)	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V		50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V		30	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V		20	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V		5(3)	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V		8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V		12(3)	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V		5(3)	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V		8(3)	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V		12(3)	
FM+ configuration (4)	$f_{max(IO)out}$	Maximum frequency(2)				MHz
	$t_{f(IO)out}$	Output high to low level fall time				ns
	$t_{r(IO)out}$	Output low to high level rise time				
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller		10		ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the RM0091 reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 21*.
3. Guaranteed by design, not tested in production.
4. The I/O speed configuration is bypassed in FM+ I/O mode. Refer to the STM32F05xxx reference manual RM0091 for a description of FM+ I/O mode configuration.

Figure 21. I/O AC characteristics definition



7.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 48*).

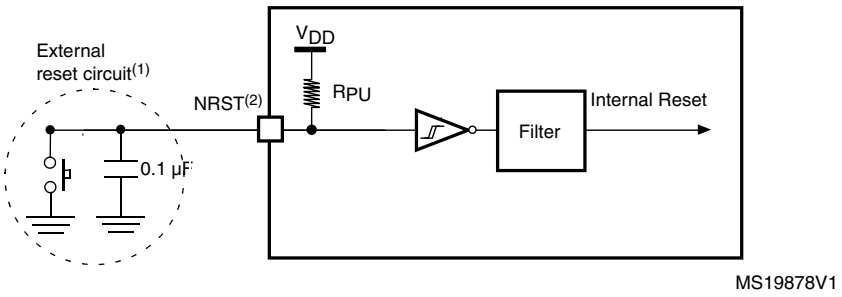
Unless otherwise specified, the parameters given in *Table 51* are derived from tests performed under ambient temperature and VDD supply voltage conditions summarized in *Table 18*.

Table 51. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage		–0.5		0.8	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage		2		V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis			200		mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse				100	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse		300			ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 22. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 51*. Otherwise the reset will not be taken into account by the device.

7.3.15 Timer characteristics

The parameters given in *Table 52* are guaranteed by design.

Refer to *Section 7.3.13: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 52. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time		1		$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	20.8		ns
f_{EXT}	Timer external clock frequency on CH1 to CH4		0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 48 MHz	0	24	MHz
Res_{TIM}	Timer resolution	TIMx (except TIM2)		16	bit
		TIM2		32	
$t_{COUNTER}$	16-bit counter clock period		1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	0.0208	1365	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter			65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz		89.48	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3, TIM6, TIM14, TIM15, TIM16 and TIM17 timers.

Table 53. IWDG min/max timeout period at 40 kHz (LSI) (1)

Prescaler divider	PR[2:0] bits	Min timeout (ms) RL[11:0]= 0x000	Max timeout (ms) RL[11:0]= 0xFFF
/4	0	0.1	409.6
/8	1	0.2	819.2
/16	2	0.4	1638.4
/32	3	0.8	3276.8
/64	4	1.6	6553.6
/128	5	3.2	13107.2
/256	7	6.4	26214.4

1. These timings are given for a 40 kHz clock but the microcontroller's internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 54. WWDG min-max timeout value @48 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value
1	0	TBD	TBD
2	1	TBD	TBD
4	2	TBD	TBD
8	3	TBD	TBD

7.3.16 Communications interfaces

I^2C interface characteristics

Unless otherwise specified, the parameters given in *Table 55* are derived from tests performed under ambient temperature, f_{PCLK1} frequency and V_{DD} supply voltage conditions summarized in *Table 18*.

The I^2C interface meets the requirements of the standard I^2C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

The I^2C characteristics are described in *Table 55*. Refer also to *Section 7.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 55. I^2C characteristics(1)

Symbol	Parameter	Standard mode		Fast mode		Fast Mode Plus		Unit
		Min	Max	Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		0.5		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		0.26		
$t_{su(SDA)}$	SDA setup time	250		100		50		ns
$t_{h(SDA)}$	SDA data hold time	0(2)	3450	0(3)	900(2)	0	450	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000		300		120	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300		300		120	
$t_{h(STA)}$	Start condition hold time	4.0		0.6		0.26		µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7		0.6		0.26		
$t_{su(STO)}$	Stop condition setup time	4.0		0.6		0.26		µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7		1.3		0.5		µs
C_b	Capacitive load for each bus line		400		400		550	pF

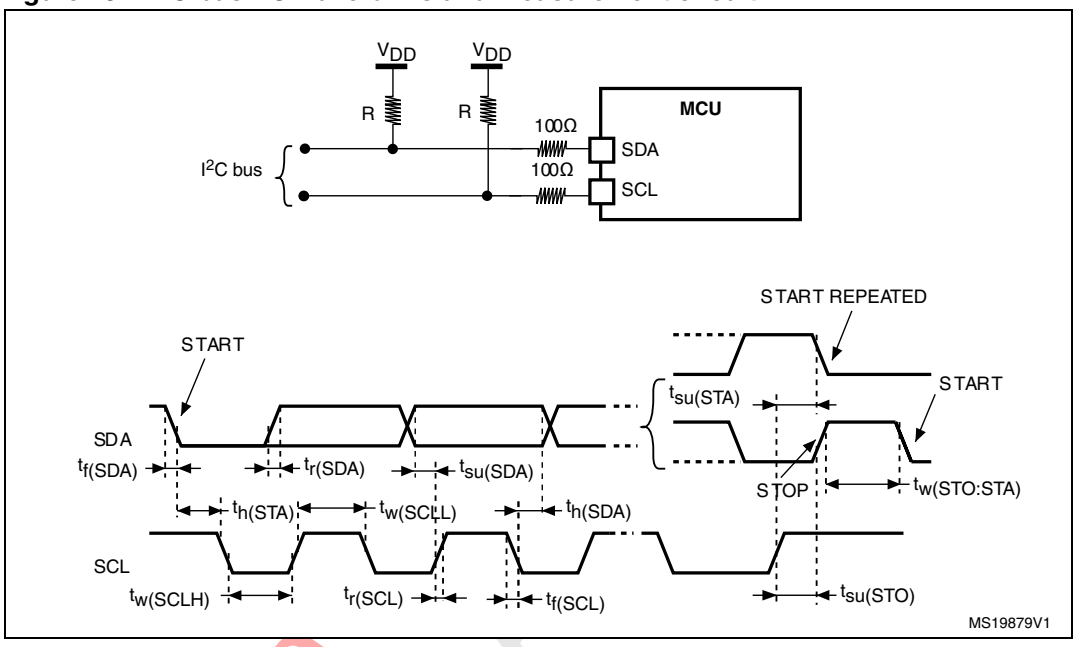
1. The I2C characteristics are the requirements from I2C bus specification rev03. They are guaranteed by design when I2Cx_TIMING register is correctly programmed (Refer to reference manual). These characteristics are not tested in production.
2. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.
3. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.

Table 56. I2C analog filter characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{SP}	Pulse width of spikes that are suppressed by the analog filter	50	260	ns

1. Guaranteed by design, not tested in production.

Figure 23. I²C bus AC waveforms and measurement circuit



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

SPI/I²S characteristics

Unless otherwise specified, the parameters given in *Table 57* for SPI or in *Table 58* for I²S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 18*.

Refer to *Section 7.3.13: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 57. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode		18	MHz
		Slave mode		18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 15 pF		6	ns
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	4Tpclk		ns
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	2Tpclk + 10		
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	Tpclk/2 -2	Tpclk/2 + 1	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode	4		
		Slave mode	5		
$t_{h(MI)}$ (1)	Data input hold time	Master mode	4		
$t_{h(SI)}$ (1)		Slave mode	5		
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	3Tpclk	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	0	18	
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)		22.5	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)		6	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	11.5		
$t_{h(MO)}$ (1)		Master mode (after enable edge)	2		
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	25	75	%

1. Data based on characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 24. SPI timing diagram - slave mode and CPHA = 0

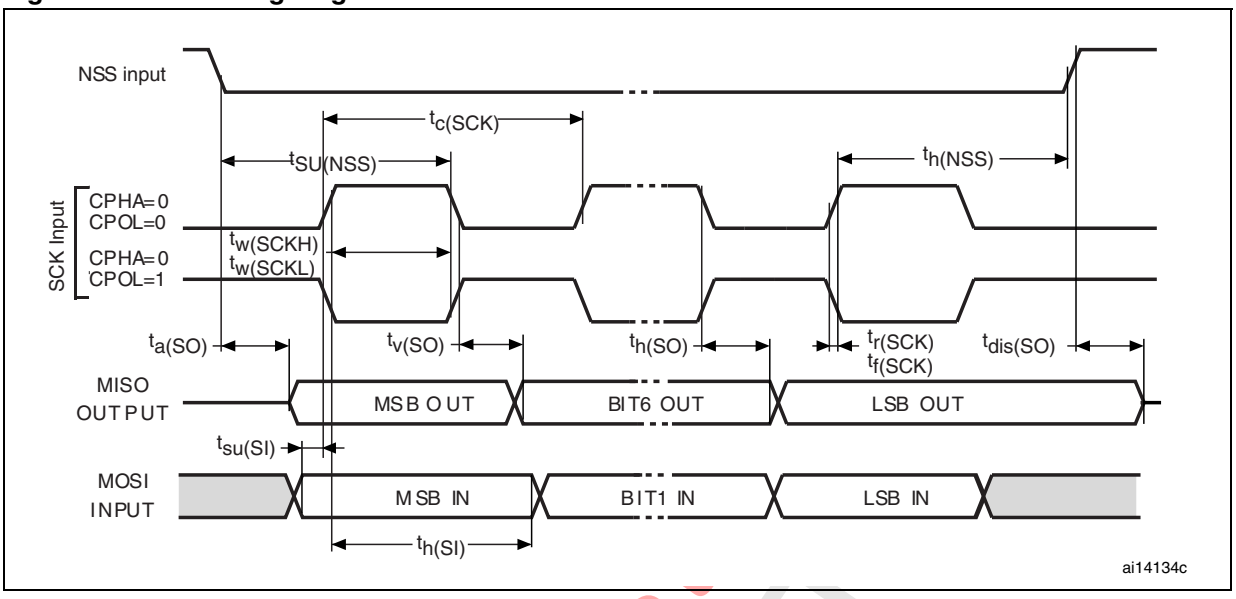
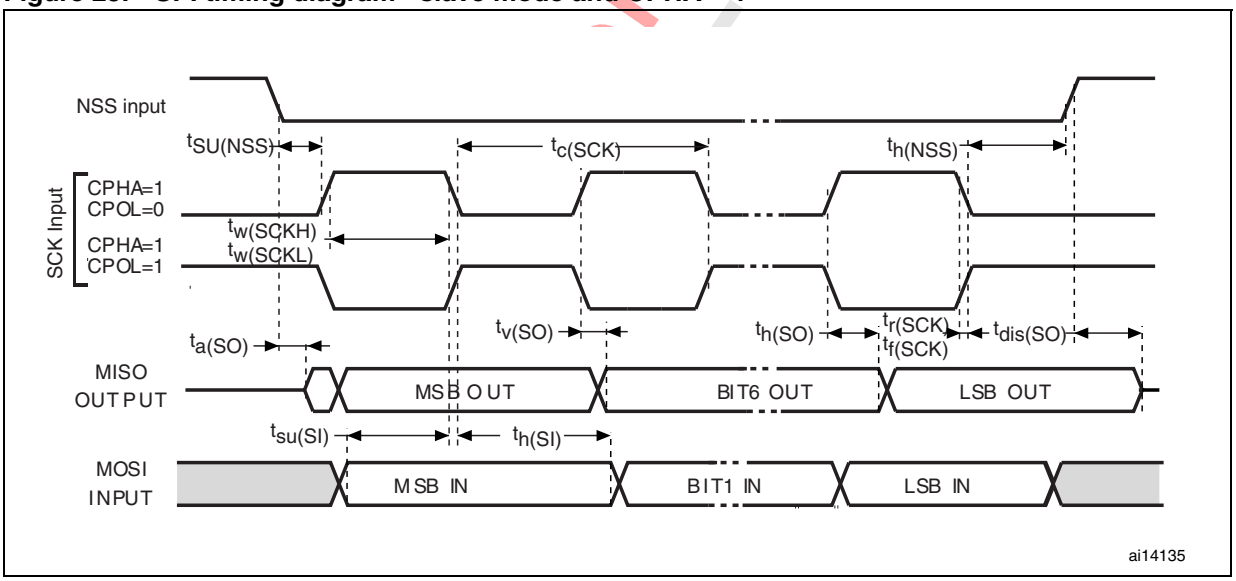
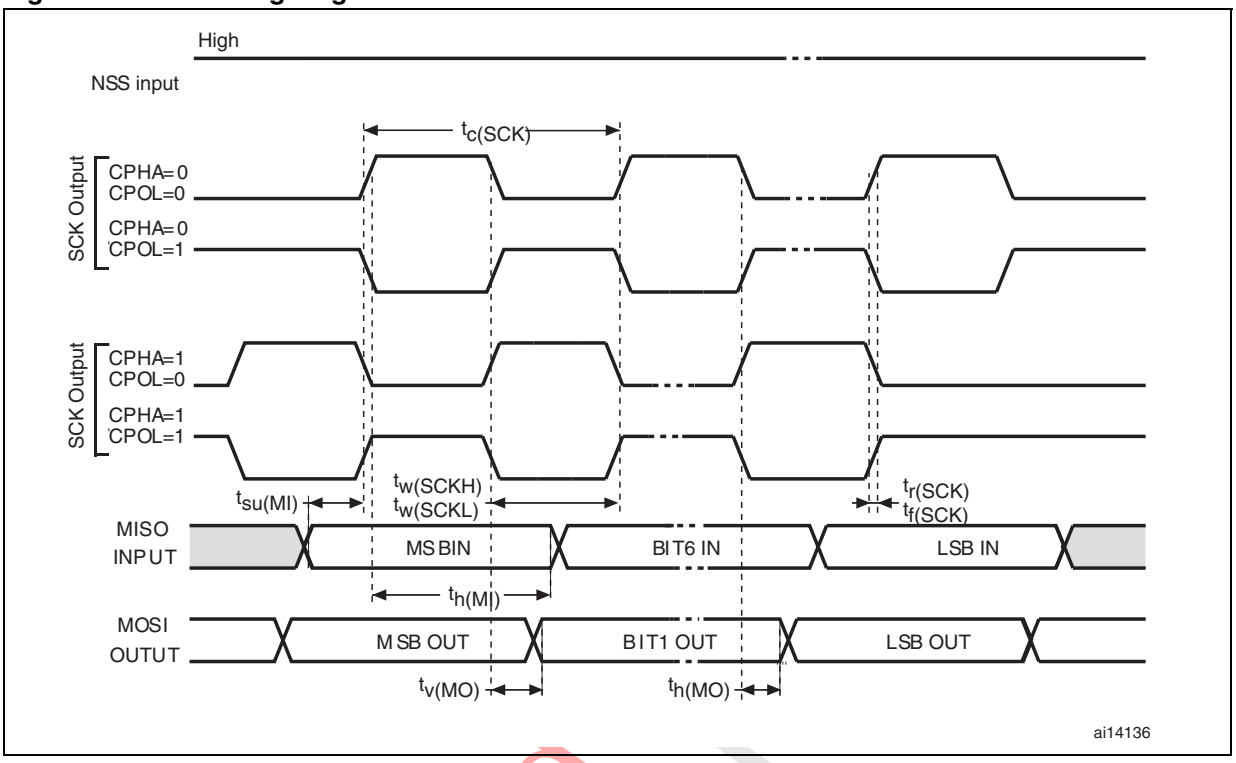


Figure 25. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 26. SPI timing diagram - master mode(1)



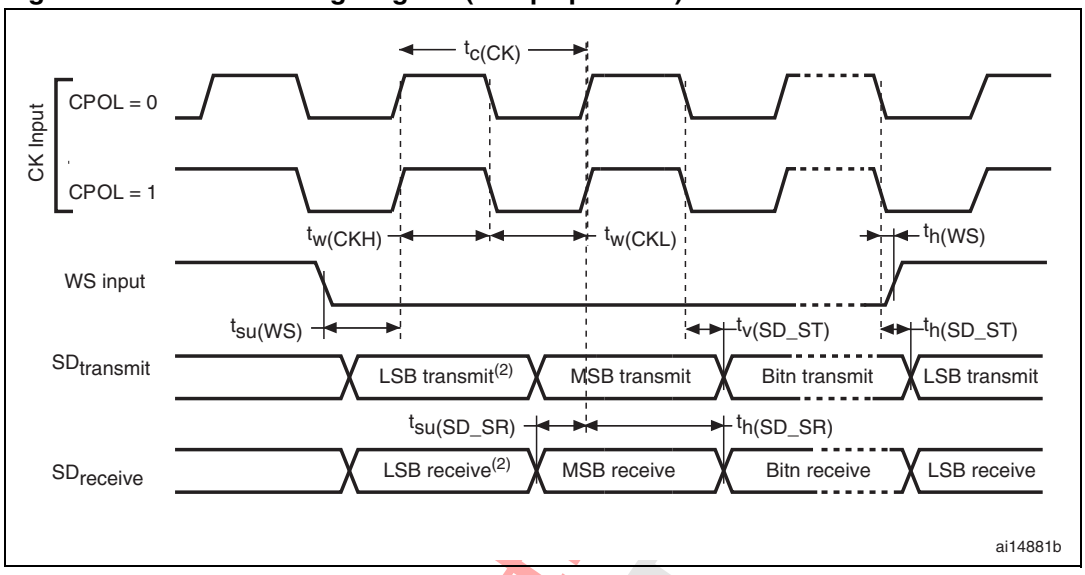
1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 58. I^2S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I^2S clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)	1.597	1.601	MHz
		Slave mode	0	6.5	
$t_{r(CK)}$	I^2S clock rise time	Capacitive load C_L = 15 pF		10	ns
$t_{f(CK)}$	I^2S clock fall time			12	
$t_{w(CKH)}$ (1)	I2S clock high time	Master f_{PCLK}= 16 MHz, audio frequency = 48 kHz	306		
$t_{w(CKL)}$ (1)	I2S clock low time		312		
$t_{v(WS)}$ (1)	WS valid time	Master mode	2		
$t_{h(WS)}$ (1)	WS hold time	Master mode	2		
$t_{su(WS)}$ (1)	WS setup time	Slave mode	7		
$t_{h(WS)}$ (1)	WS hold time	Slave mode	0		
DuCy(SCK)	I2S slave input clock duty cycle	Slave mode	25	75	%
$t_{su(SD\_MR)}$ (1)	Data input setup time	Master receiver	6		ns
$t_{su(SD\_SR)}$ (1)	Data input setup time	Slave receiver	2		
$t_{h(SD\_MR)}$ (1)(2)	Data input hold time	Master receiver	4		
$t_{h(SD\_SR)}$ (1)(2)		Slave receiver	0.5		
$t_{v(SD\_ST)}$ (1)(2)	Data output valid time	Slave transmitter (after enable edge)		31 (3)	
$t_{h(SD\_ST)}$ (1)	Data output hold time	Slave transmitter (after enable edge)	13		
$t_{v(SD\_MT)}$ (1)(2)	Data output valid time	Master transmitter (after enable edge)		4	
$t_{h(SD\_MT)}$ (1)	Data output hold time	Master transmitter (after enable edge)	0		

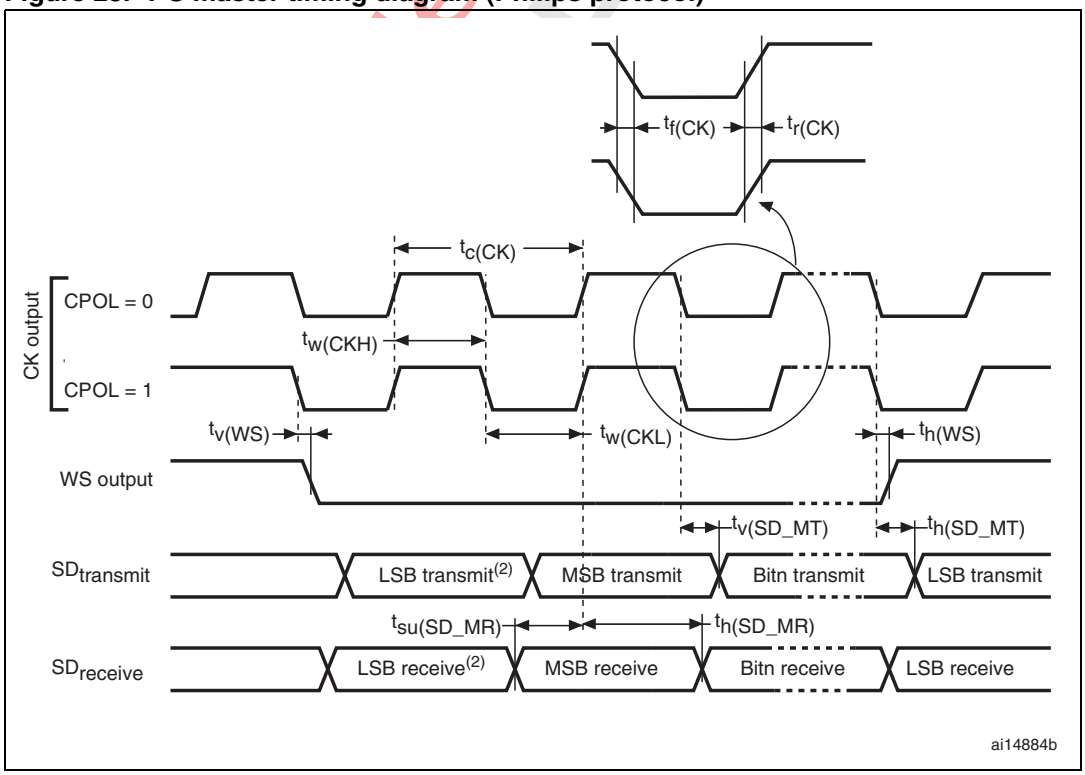
1. Data based on design simulation and/or characterization results, not tested in production.
2. Depends on f_{PCLK}. For example, if f_{PCLK}=8 MHz, then $T_{PCLK} = 1/f_{PLCLK}$ =125 ns.
3. REGOFF value was chosen but in REGON target value is 20 ns

Figure 27. I²S slave timing diagram (Philips protocol)(1)



1. Measurement points are done at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 28. I²S master timing diagram (Philips protocol)(1)



1. Data based on characterization results, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

7.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 59* are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 18*.

Note: It is recommended to perform a calibration after each power-up.

Table 59. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC ON		2.4		3.6	V
f_{ADC}	ADC clock frequency		0.6		14	MHz
f_S(1)	Sampling rate		0.05		1	MHz
f_{TRIG}(1)	External trigger frequency	f_{ADC} = 14 MHz			823	kHz
					17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range		0		V_{DDA}	V
R_{AIN}(1)	External input impedance	See *Equation 1* and *Table 60* for details			50	kΩ
R_{ADC}(1)	Sampling switch resistance				1	kΩ
C_{ADC}(1)	Internal sample and hold capacitor				8	pF
t_{CAL}(1)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
			83			$1/f_{ADC}$
t_{latr}(1)	Trigger conversion latency	f_{ADC} = 14 MHz			0.143	µs
					$2^{???}$	$1/f_{ADC}$
t_S(1)	Sampling time	f_{ADC} = 14 MHz	0.107		17.1	µs
			1.5		239.5	$1/f_{ADC}$
t_{STAB}(1)	Power-up time		0	0	1	µs
t_{CONV}(1)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1		18	µs
			14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Guaranteed by design, not tested in production.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 60. R_{AIN} max for f_{ADC} = 14 MHz(1)

T_s (cycles)	t_S (µs)	R_{AIN} max (kΩ)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

1. Guaranteed by design, not tested in production.

Table 61. ADC accuracy(1)(2) (3)

Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{PCLK} = 48 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3 V to 3.6 V T_A = 25 °C	±1.3	±2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	
ET	Total unadjusted error	f_{PCLK} = 48 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V T_A = -40 to 105 °C	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 7.3.13* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.

Figure 29. ADC accuracy characteristics

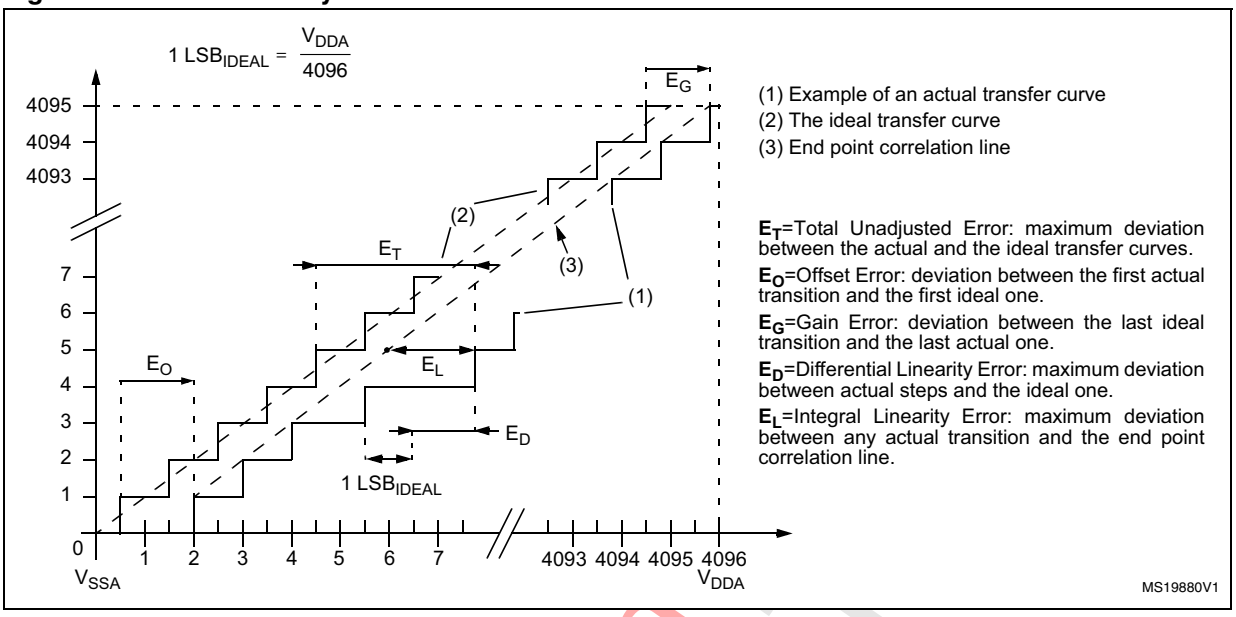
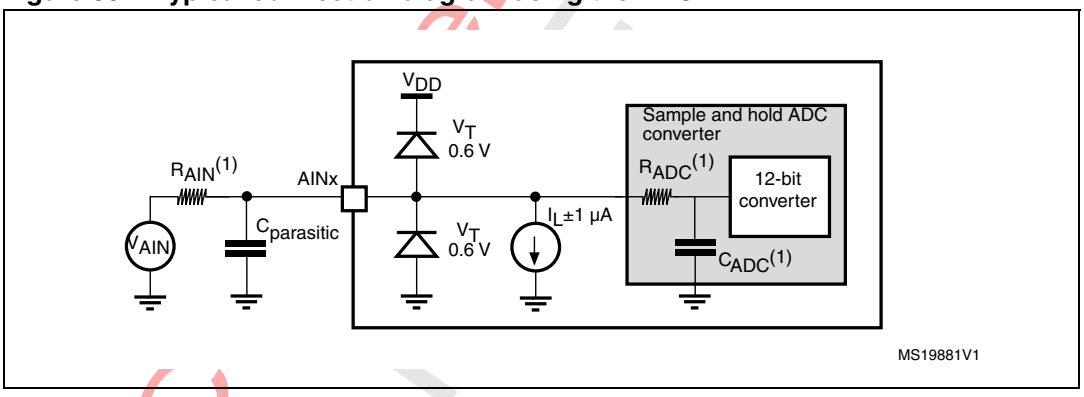


Figure 30. Typical connection diagram using the ADC



1. Refer to *Table 59* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 9*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

7.3.18 DAC electrical specifications

Table 62. DAC characteristics

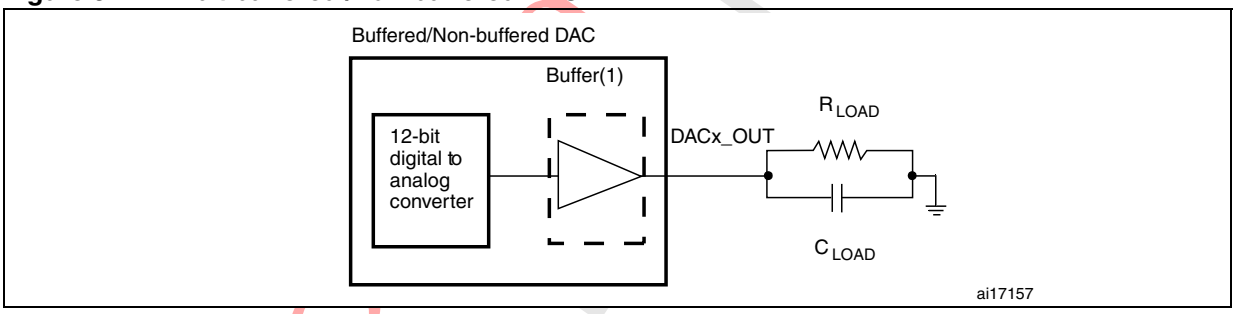
Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDA}	Analog supply voltage for DAC ON	2.4		3.6	V	
R_{LOAD}(1)	Resistive load with buffer ON	5			kΩ	
R_O(1)	Impedance output with buffer OFF			15	kΩ	When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 MΩ
C_{LOAD}(1)	Capacitive load			50	pF	Maximum capacitive load at DAC_OUT pin (when the buffer is ON).
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer ON	0.2			V	It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at V_{DDA} = 3.6 V and (0x155) and (0xEAB) at V_{DDA} = 2.4 V
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer ON			V_{DDA} – 0.2	V	
DAC_OUT min(1)	Lower DAC_OUT voltage with buffer OFF		0.5		mV	It gives the maximum output excursion of the DAC.
DAC_OUT max(1)	Higher DAC_OUT voltage with buffer OFF			V_{DDA} – 1LSB	V	
I_{DDA}	DAC DC current consumption in quiescent mode (Standby mode)			380	µA	With no load, middle code (0x800) on the input
				480	µA	With no load, worst code (0xF1C) on the input
DNL(2)	Differential non linearity Difference between two consecutive code-1LSB)			±0.5	LSB	Given for the DAC in 10-bit configuration
				±2	LSB	Given for the DAC in 12-bit configuration
INL(2)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)			±1	LSB	Given for the DAC in 10-bit configuration
				±4	LSB	Given for the DAC in 12-bit configuration
Offset(2)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{DDA}/2)			±10	mV	Given for the DAC in 12-bit configuration
				±3	LSB	Given for the DAC in 10-bit at V_{DDA} = 3.6 V
				±12	LSB	Given for the DAC in 12-bit at V_{DDA} = 3.6 V
Gain error(2)	Gain error			±0.5	%	Given for the DAC in 12bit configuration

Table 62. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
$t_{SETTLING}$(2)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB		3	4	µs	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ
Update rate(2)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)			1	MS/s	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ
t_{WAKEUP}(2)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)		6.5	10	µs	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ input code between lowest and highest possible ones.
PSRR+ (1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement		–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. Guaranteed by design, not tested in production.
2. Data based on characterization results, not tested in production.

Figure 31. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

7.3.19 Comparator characteristics

Table 63. Comparator characteristics

Symbol	Parameter	Conditions		Min	Typ	Max(1)	Unit
V_{DDA}	Analog supply voltage			1.65		3.6	V
V_{IN}	Comparator input voltage range			0		V_{DDA}	V
V_{SC}	Scaler offset voltage				±5	±10	mV
t_{S_SC}	Scaler startup time from power down					0.1	ms
t_{START}	Comparator startup time					15	µs
t_D	Propagation delay for 200 mV step with 100 mV overdrive	Ultra-low power mode			3.5	6.3	µs
		Low power mode			1.0	2.0	µs
		Medium speed mode			0.4	1.3	µs
		High speed mode	V_{DDA} > 2.7 V		80	120	ns
			2.7 V > V_{DDA} > 2 V		120	200	ns
			2 V > V_{DDA}		180	700	ns
	Propagation delay for full range step with 100 mV overdrive	Ultra-low power mode			4.0	7.5	µs
		Low power mode			1.5	2.6	µs
		Medium speed mode			0.6	1.4	µs
		High speed mode	V_{DDA} > 2.7 V		120	200	ns
			2.7 V > V_{DDA} > 2 V		160	300	ns
			2 V > V_{DDA}		220	1000	ns
V_{offset}	Comparator offset error				±4	±20	mV
dThreshold/dt	Threshold voltage temperature coefficient				15	30	ppm /°C
I_{COMP}	Current consumption	Ultra-low power mode				1	µA
		Low power mode				3	µA
		Medium speed mode				10	µA
		High speed mode				100	µA
V_{hys}	Comparator hysteresis	No hysteresis (COMPxHYST[1:0]=00)			0		mV
		Low hysteresis (COMPxHYST[1:0]=01)		2	7	12	mV
		Medium hysteresis (COMPxHYST[1:0]=10)		5	13	24	mV
		High hysteresis (COMPxHYST[1:0]=11)		11	25	44	mV

1. Data based on characterization results, not tested in production.

7.3.20 Temperature sensor characteristics

Table 64. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature		±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}(1)	Startup time	4		10	µs
T_{S_temp}(1)(2)	ADC sampling time when reading the temperature			17.1	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

7.3.21 V_{BAT} monitoring characteristics

Table 65. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	50	-	KΩ
Q	Ratio on V_{BAT} measurement	-	2	-	
Er(1)	Error on Q	–1	-	+1	%
T_{S_vbat}(1)(2)	ADC sampling time when reading the V_{BAT} 1mV accuracy	5	-	-	µs

1. Guaranteed by design, not tested in production.
2. Shortest sampling time can be determined in the application by multiple iterations.

8 Package characteristics

8.1 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 32. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline(1)

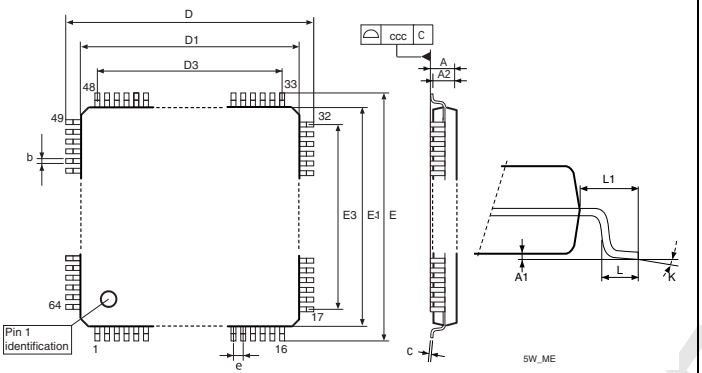
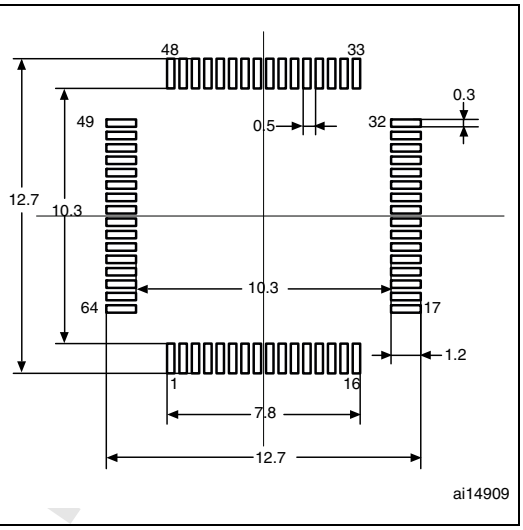


Figure 33. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 66. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	11.800	12.000	12.200	0.4646	0.4724	0.4803
D1	9.800	10.000	10.200	0.3858	0.3937	0.4016
D.		7.500				
E	11.800	12.000	12.200	0.4646	0.4724	0.4803
E1	9.800	10.00	10.200	0.3858	0.3937	0.4016
e		0.500			0.0197	
k	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.75	0.0177	0.0236	0.0295
L1		1.000			0.0394	
ccc		0.080			0.0031	
N	Number of pins					
	64					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 34. LQFP48 – 7 x 7mm, 48-pin low-profile quad flat package outline(1)

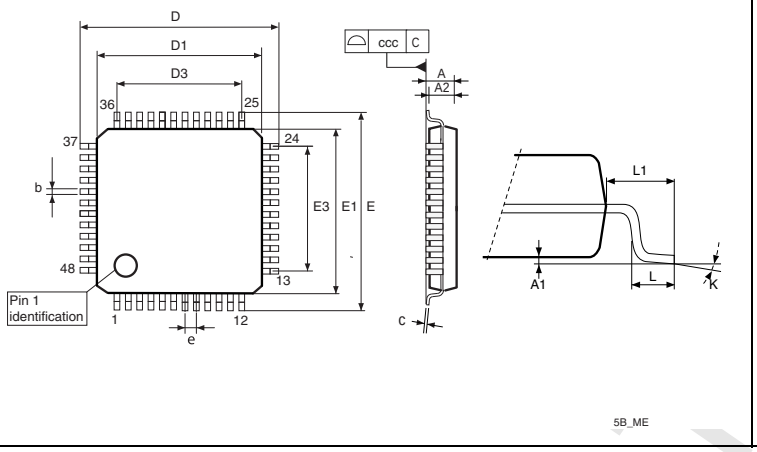
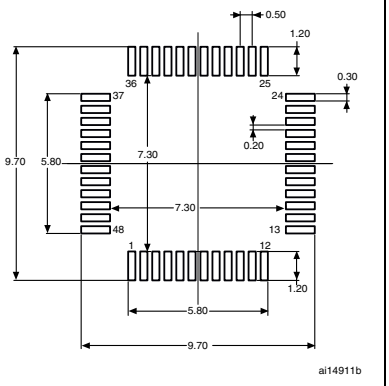


Figure 35. Recommended footprint(1)(2)



1. Drawing is not to scale.
2. Dimensions are in millimeters.

Table 67. LQFP48 – 7 x 7mm, 48-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A			1.600			0.0630
A1	0.050		0.150	0.0020		0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090		0.200	0.0035		0.0079
D	8.800	9.000	9.200	0.3465	0.3543	0.3622
D1	6.800	7.000	7.200	0.2677	0.2756	0.2835
D3		5.500			0.2165	
E	8.800	9.000	9.200	0.3465	0.3543	0.3622
E1	6.800	7.000	7.200	0.2677	0.2756	0.2835
E3		5.500			0.2165	
e		0.500			0.0197	
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1		1.000			0.0394	
k	0°	3.5°	7°	0°	3.5°	7°
ccc		0.080			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 36. UFQFPN32 - 32-lead ultra thin fine pitch quad flat no-lead package outline (5 x 5)(1)(2)(3)

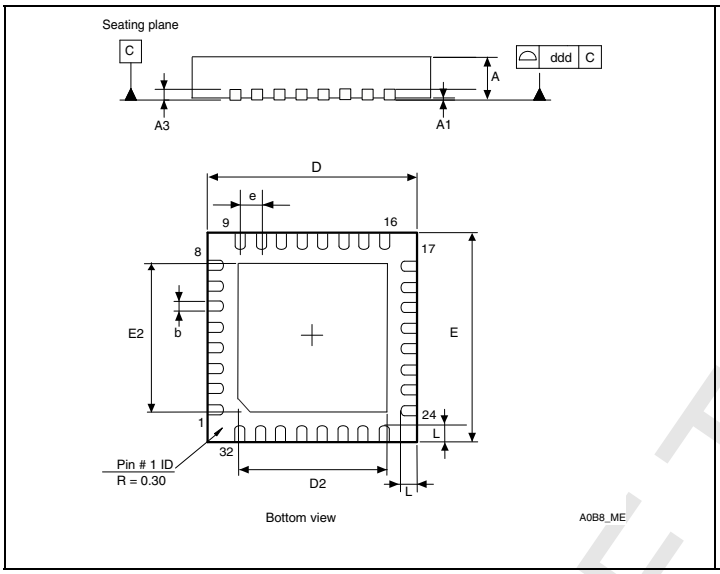
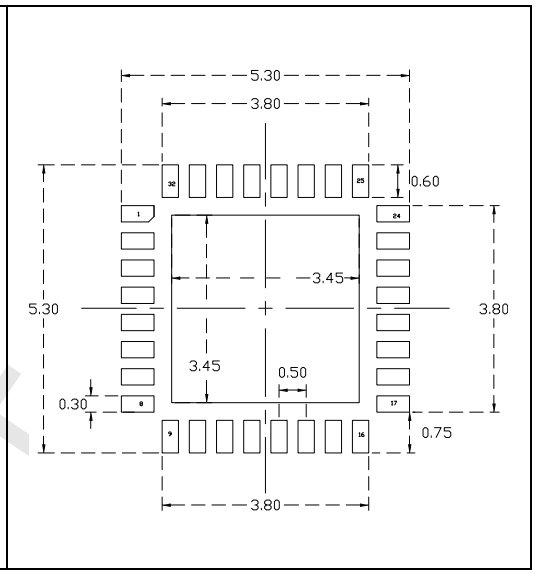


Figure 37. UFQFPN32 recommended footprint(1)(4)



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. This pad is used for the device ground and must be connected. It is referred to as pin 0 in *Table 11: Pin definitions*.
4. Dimensions are in millimeters.

Table 68. UFQFPN32 - 32-lead ultra thin fine pitch quad flat no-lead package (5 x 5), package mechanical data

Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.5	0.55	0.6	0.0197	0.0217	0.0236
A1	0.00	0.02	0.05	0	0.0008	0.0020
A3		0.152			0.006	
b	0.18	0.23	0.28	0.0071	0.0091	0.0110
D	4.90	5.00	5.10	0.1929	0.1969	0.2008
D2		3.50			0.1378	
E	4.90	5.00	5.10	0.1929	0.1969	0.2008
E2	3.40	3.50	3.60	0.1339	0.1378	0.1417
e		0.500			0.0197	
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
ddd	0.08			0.0031		
	Number of pins					
N	32					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

8.2 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 18: General operating conditions on page 41*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 69. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP64 - 10 × 10 mm / 0.5 mm pitch	TBD	°C/W
	Thermal resistance junction-ambient LQFP48 - 7 × 7 mm	TBD	
	Thermal resistance junction-ambient UFQFPN32 - 5 × 5 mm	TBD	

8.2.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

8.2.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section Figure 38.: LQFP64 PD max vs. TA*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F05xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Thus: P_{Dmax} = 447 mW

Using the values obtained in *Table 69* T_{Jmax} is calculated as follows:

– For LQFP64, TBD °C/W

T_{Jmax} = 82 °C + (TBD°C/W × 447 mW) = 82 °C + 20.6 °C = 102.6 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Section Figure 38.: LQFP64 PD max vs. TA*).

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 115 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in *Table 69* T_{Jmax} is calculated as follows:

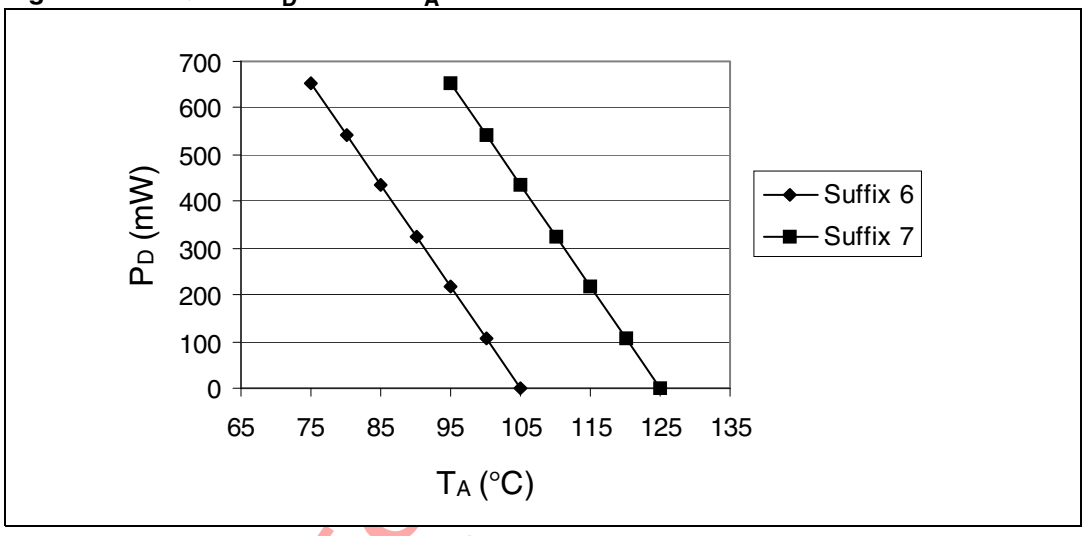
– For LQFP64, TBD °C/W

T_{Jmax} = 115 °C + (TBD °C/W × 134 mW) = 115 °C + 6.2 °C = 121.2 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section Figure 38.: LQFP64 PD max vs. TA*).

Figure 38. LQFP64 P_D max vs. T_A



9 Ordering information scheme

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Example: STM32 F 051 R 8 T 6 x

Device family

STM32 = ARM-based 32-bit microcontroller

Product type

F = General-purpose

Sub-family

051 = STM32F051xx

Pin count

K = 32 pins
C = 48 pins
R = 64 pins

Code size

4 = 16 Kbytes of Flash memory
6 = 32 Kbytes of Flash memory
8 = 64 Kbytes of Flash memory

Package

U = UFQFN
T = LQFP

Temperature range

6 = –40 °C to +85 °C
7 = –40 °C to +105 °C

Options

xxx = programmed parts
TR = tape and real

10 Revision history

Table 70. Document revision history

Date	Revision	Changes
06-Mar-2011	1d	Initial draft
	1e	Added IWDG/WWDG min/max timeout tables.
	1f	Revised Electrical characteristics.
	1g	Implemented changes dated 1st november.
	1h	Implemented changes dated 14th november.
	1i	Updated pinout of UFQFPN32
	1k	Updated section *Section 4.9.2: Power supply supervisors*
	1l	Updated *Table 49* and *Figure 2*
	1m	Added STM32F051x4 16K Flash devices
	1n	Implemented changes dated 31 January
	1o	Added typ power consumption values and SPI/I2C timings
	1p	Added typ power consumption values

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