bq2461x Stand-Alone Synchronous Switched-Mode Li-Ion or Li-Polymer Battery Charger With System Power Selector and Low I_q

1 Features

- 600-kHz NMOS-NMOS Synchronous Buck Converter
- Stand-Alone Charger Support for Li-Ion or Li-Polymer
- 5-V to 28-V VCC Input Operating Range and Supports 1- to 6-Battery Cells (bq24610)
- 5-V to 24-V VCC Input Operating Range and Supports 1- to 5-Battery Cells (bq24617)
- Up to 10-A Charge Current and Adapter Current
- High-Accuracy Voltage and Current Regulation
  - ±0.5% Charge Voltage Accuracy
  - ±3% Charge Current Accuracy
  - ±3% Adapter Current Accuracy
- Integration
  - Automatic System Power Selection From Adapter or Battery
  - Internal Loop Compensation and Soft Start
  - Dynamic Power Management
- Safety Protection
  - Input Overvoltage Protection
  - Battery Thermistor Sense Hot and Cold Charge Suspend
  - Battery Detection
  - Reverse Protection Input FET
  - Programmable Safety Timer
  - Charge Overcurrent Protection
  - Battery Short Protection
  - Battery Overvoltage Protection
  - Thermal Shutdown
- Status Outputs
  - Adapter Present
  - Charger Operation Status
- Charge Enable Pin
- 6-V Gate Drive for Synchronous Buck Converter
- 30-ns Driver Dead-Time and 99.5% Maximum Effective Duty Cycle
- Energy Star Low Quiescent Current I_q
  - < 15-µA Off-State Battery Discharge Current
  - < 1.5-mA Off-State Input Quiescent Current

2 Applications

- Netbooks, Mobile Internet Devices, and Ultra-Mobile PCs
- Personal Digital Assistants (PDAs)
- Handheld Terminals
- Industrial and Medical Equipment
- Portable Equipment

3 Description

The bq2461x is a highly integrated Li-ion or Li-polymer switched-mode battery charge controller. The device offers a constant-frequency synchronous switching PWM controller with high-accuracy charge current and voltage regulation, charge preconditioning, termination, adapter current regulation, and charge status monitoring.

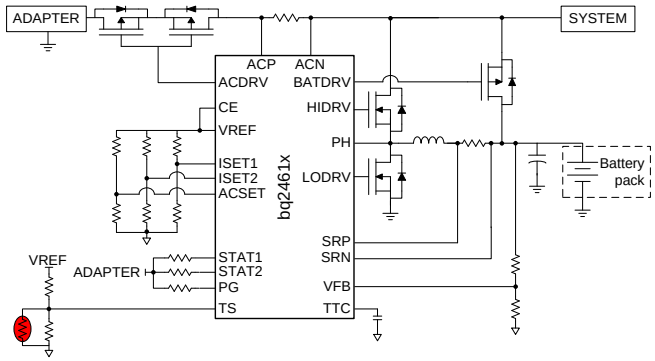
The bq2461x charges the battery in three phases: preconditioning, constant current, and constant voltage.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq24610	VQFN (24)	4.00 mm × 4.00 mm
bq24617		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (September 2013) to Revision C — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision A (October 2011) to Revision B — **Page**

- Changed Figure 14, pin V_{LTFH} to: V_{LTF_HYS} ... 20

Changes from Original (December 2009) to Revision A — **Page**

- Corrected equation for calculating RT2 ... 21
- Corrected equation for calculating I_{COUT} ... 28

5 Description (continued)

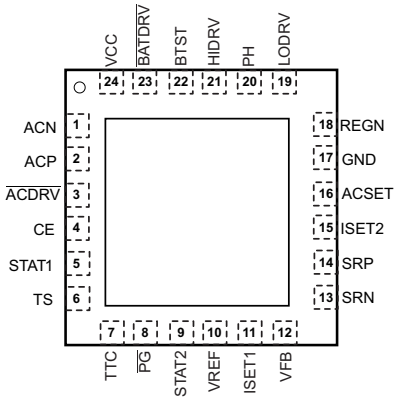
Charge is terminated when the current reaches a minimum user-selectable level. A programmable charge timer provides a safety backup. The bq2461x automatically restarts the charge cycle if the battery voltage falls below an internal threshold, and enters a low quiescent current sleep mode when the input voltage falls below the battery voltage.

6 Device Comparison Table

	bq24600	bq24610	bq24616	bq24617	bq24618	bq24650
Cell chemistry	Li-Ion/Li-Polymer	Li-Ion/Li-Polymer	Li-Ion/Li-Polymer	Li-Ion/Li-Polymer	Li-Ion/Li-Polymer	Li-Ion/Li-Polymer
Number of cells in series (minimum to maximum, 4.2 V/cell)	1 to 6	1 to 6	1 to 6	1 to 5	1 to 6	1 to 6
Charge voltage (minimum to maximum) (V)	2.1 to 26	2.1 to 26	2.1 to 26	2.1 to 22	2.1 to 26	2.1 to 26
Input voltage range (minimum to maximum) (V)	5 to 28	5 to 28	5 to 28	5 to 24	4.7 to 28	5 to 28
Input overvoltage (V)	32	32	32	26	32	32
Maximum battery charging current (A)	10	10	10	10	10	10
Switching frequency (kHz)	1200	600	600	600	600	600
JEITA charging temperature profile	No	No	Yes	No	No	No
DPM	No	I_{IN} DPM	I_{IN} DPM	I_{IN} DPM	I_{IN} DPM	V_{IN} DPM

7 Pin Configuration and Functions

RGE Package
24-Pin VQFN
Top View



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
$\overline{\text{ACDRV}}$	3	AC adapter to system MOSFET driver output. Connect through a 1-kΩ resistor to the gate of the ACFET P-channel power MOSFET and the reverse conduction blocking P-channel power MOSFET. The internal gate drive is asymmetrical, allowing a quick turnoff and slow turnon, in addition to the internal break-before-make logic with respect to $\overline{\text{BATDRV}}$. If needed, an optional capacitor from gate to source of the ACFET is used to slow down the ON and OFF times.
ACN	1	Adapter current-sense resistor, negative input. A 0.1-µF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering. An optional 0.1-µF ceramic capacitor is placed from the ACN pin to GND for common-mode filtering.
ACP	2	Adapter current-sense resistor, positive input. A 0.1-µF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering. A 0.1-µF ceramic capacitor is placed from the ACP pin to GND for common-mode filtering.
ACSET	16	Adapter current-set input. The voltage of the ACSET pin programs the input current regulation set point during Dynamic Power Management (DPM).
$\overline{\text{BATDRV}}$	23	Battery-to-system MOSFET driver output. Gate drive for the battery-to-system load BAT PMOS power FET to isolate the system from the battery to prevent current flow from the system to the battery, while allowing a low-impedance path from battery to system. Connect this pin through a 1-kΩ resistor to the gate of the input BAT P-channel MOSFET. Connect the source of the FET to the system-load voltage node. Connect the drain of the FET to the battery pack positive terminal. The internal gate drive is asymmetrical to allow a quick turnoff and slow turnon, in addition to the internal break-before-make logic with respect to $\overline{\text{ACDRV}}$. If needed, an optional capacitor from gate to source of the BATFET is used to slow down the ON and OFF times.
BTST	22	PWM high-side driver positive supply. Connect a 0.1-µF bootstrap capacitor from PH to BTST, and a bootstrap Schottky diode from REGN to BTST.
CE	4	Charge enable active HIGH logic input. HI enables charge. LO disables charge. It has an internal 1-MΩ pulldown resistor.
GND	17	Low-current sensitive analog and digital ground. On PCB layout, connect with the thermal pad underneath the IC.
HIDRV	21	PWM high-side driver output. Connect to the gate of the high-side power MOSFET with a short trace.
ISET1	11	Fast-charge current-set input. The voltage of the ISET1 pin programs the fast-charge current regulation set point.
ISET2	15	Precharge and termination current set input. The voltage of the ISET2 pin programs the precharge current regulation set point and termination current trigger point.
LODRV	19	PWM low-side driver output. Connect to the gate of the low-side power MOSFET with a short trace.
$\overline{\text{PG}}$	8	Open-drain power-good status output. Active LOW when IC has a valid VCC (not in UVLO or ACOV or SLEEP mode). Active HIGH when IC has an invalid VCC. $\overline{\text{PG}}$ can be used to drive an LED or communicate with a host processor.
PH	20	PWM high-side driver negative supply. Connect to the phase-switching node (junction of the low-side power MOSFET drain, high-side power MOSFET source, and output inductor).
REGN	18	PWM low-side driver positive 6-V supply output. Connect a 1-µF ceramic capacitor from REGN to the GND pin, close to the IC. Use for low-side driver and high-side driver bootstrap voltage by connecting a small-signal Schottky diode from REGN to BTST.

Pin Functions (continued)

PIN		DESCRIPTION
NAME	NO.	
SRN	13	Charge current-sense resistor, negative input. A 0.1-µF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. An optional 0.1-µF ceramic capacitor is placed from the SRN pin to GND for common-mode filtering.
SRP	14	Charge current sense resistor, positive input. A 0.1-µF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. A 0.1-µF ceramic capacitor is placed from the SRP pin to GND for common-mode filtering.
STAT1	5	Open-drain charge status pin to indicate various charger operation (see Table 2).
STAT2	9	Open-drain charge status pin to indicate various charger operations (see Table 2).
Thermal pad	—	Exposed pad beneath the IC. Always solder the thermal pad to the board, and have vias on the thermal pad plane star-connecting to GND and ground plane for high-current power converter. It also serves as a thermal pad to dissipate the heat.
TS	6	Temperature qualification voltage input for battery pack negative temperature coefficient thermistor. Program the hot and cold temperature window with a resistor divider from VREF to TS to GND (see Figure 15).
TTC	7	SafetyTimer and termination control. Connect a capacitor from this node to GND to set the timer. When this input is LOW, the timer and termination are disabled. When this input is HIGH, the timer is disabled but termination is allowed.
VCC	24	IC power positive supply. Connect through a 10-Ω resistor to the common-source (diode-OR) point: source of high-side P-channel MOSFET and source of reverse-blocking power P-channel MOSFET. Place a 1-µF ceramic capacitor from VCC to the GND pin close to the IC.
VFB	12	Output voltage analog feedback adjustment. Connect the output of a resistive voltage divider from the battery terminals to this node to adjust the output battery regulation voltage.
VREF	10	3.3-V regulated voltage output. Place a 1-µF ceramic capacitor from VREF to GND pin close to the IC. This voltage could be used for programming of voltage and current regulation and for programming the TS threshold.

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

		MIN	MAX	UNIT
Voltage	VCC, ACP, ACN, SRP, SRN, $\overline{\text{BATDRV}}$, $\overline{\text{ACDRV}}$, CE, STAT1, STAT2, $\overline{\text{PG}}$	–0.3	33	V
	PH	–2	36	
	VFB	–0.3	16	
	REGN, LODRV, ACSET, TS, TTC	–0.3	7	
	BTST, HIDRV with respect to GND	–0.3	39	
	VREF, ISET1, ISET2	–0.3	3.6	
Maximum difference voltage	ACP–ACN, SRP–SRN	–0.5	0.5	V
T_J Junction temperature		–40	155	°C
T_{stg} Storage temperature		–55	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND if not specified. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the data book for thermal limitations and considerations of packages.
(3) Must have a series resistor between battery pack to VFB if battery-pack voltage is expected to be greater than 16 V. Usually the resistor-divider top resistor takes care of this.

8.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

		MIN	MAX	UNIT
Voltage	**bq24610**: VCC, ACP, ACN, SRP, SRN, $\overline{\text{BATDRV}}$, $\overline{\text{ACDRV}}$, CE, STAT1, STAT2, $\overline{\text{PG}}$	–0.3	28	V
	bq24617: VCC, ACP, ACN, SRP, SRN, $\overline{\text{BATDRV}}$, $\overline{\text{ACDRV}}$, CE, STAT1, STAT2, $\overline{\text{PG}}$	–0.3	24	V
	PH	–2	30	V
	VFB	–0.3	14	V
	REGN, LODRV, ACSET, TS, TTC	–0.3	6.5	V
	BTST, HIDRV with respect to GND	–0.3	34	V
	ISET1, ISET2	–0.3	3.3	V
	VREF		3.3	V
Maximum difference voltage	ACP–ACN, SRP–SRN	–0.2	0.2	V
T_J Junction temperature		0	125	°C

8.4 Thermal Information

THERMAL METRIC (1)		bq2461x RGE [VQFN] 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

8.5 Electrical Characteristics

5 V ≤ V_{VCC} ≤ 28 V, 0°C < T_J < 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CONDITIONS						
V_{VCC_OP}	VCC input voltage operating range(610)		5		28	V
	VCC input voltage operating range(617)		5		24	
QUIESCENT CURRENTS						
I_{BAT}	Total battery discharge current (sum of currents into VCC, BTST, PH, ACP, ACN, SRP, SRN, VFB), VFB ≤ 2.1 V	V_{VCC} < V_{SRN}, V_{VCC} > V_{UVLO} (SLEEP)			15	µA
	Battery discharge current (sum of currents into BTST, PH, SRP, SRN, VFB), VFB ≤ 2.1 V	V_{VCC} > V_{SRN}, V_{VCC} > V_{UVLO} CE = LOW			5	
		V_{VCC} > V_{SRN}, V_{VCC} > V_{VCCLOW} CE = HIGH, charge done			5	
I_{AC}	Adapter supply current (current into VCC, ACP, ACN pin)	V_{VCC} > V_{SRN}, V_{VCC} > V_{UVLO} CE = LOW (IC quiescent current)		1	1.5	mA
		V_{VCC} > V_{SRN}, V_{VCC} >V_{VCCLOW} , CE = HIGH, charge done		2	5	
		V_{VCC} > V_{SRN}, V_{VCC} >V_{VCCLOW} , CE = HIGH, charging, Qg_total = 20 nC		25		
CHARGE VOLTAGE REGULATION						
V_{FB}	Feedback regulation voltage			2.1		V
	Charge voltage regulation accuracy	T_J = 0°C to 85°C	–0.5%		0.5%	
		T_J = –40°C to 125°C	–0.7%		0.7%	
I_{VFB}	Leakage current into VFB pin	VFB = 2.1 V			100	nA
CURRENT REGULATION – FAST CHARGE						
V_{ISET1}	ISET1 voltage range				2	V
V_{IREG_CHG}	SRP-SRN current-sense voltage range	V_{IREG_CHG} = V_{SRP} – V_{SRN}			100	mV
K_{ISET1}	Charge current set factor (amps of charge current per volt on ISET1 pin)	R_{SENSE} = 10 mΩ		5		A/V
	Charge current regulation accuracy	V_{IREG_CHG} = 40 mV	–3%		3%	
		V_{IREG_CHG} = 20 mV	–4%		4%	
		V_{IREG_CHG} = 5 mV	–25%		25%	
		V_{IREG_CHG} = 1.5 mV (V_{SRN} > 3.1 V)	–40%		40%	
I_{ISET1}	Leakage current into ISET1 pin	V_{ISET1} = 2 V			100	nA
CURRENT REGULATION – PRECHARGE						
V_{ISET2}	ISET2 voltage range				2	V
K_{ISET2}	Precharge current set factor (amps of precharge current per volt on ISET2 pin)	R_{SENSE} = 10 mΩ		1		A/V
	Precharge current regulation accuracy	V_{IREG_PRECH} = 20 mV	–4%		4%	
		V_{IREG_PRECH} = 5 mV	–25%		25%	
		V_{IREG_PRECH} = 1.5 mV (V_{SRN} < 3.1 V)	–55%		55%	
I_{ISET2}	Leakage current into ISET2 pin	V_{ISET2} = 2 V			100	nA
CHARGE TERMINATION						
K_{TERM}	Termination current set factor (amps of termination current per volt on ISET2 pin)	R_{SENSE} = 10 mΩ		1		A/V

Electrical Characteristics (continued)

5 V ≤ V_{VCC} ≤ 28 V, 0°C < T_J < 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Termination current accuracy	V_{ITERM} = 20 mV	–4%		4%	
		V_{ITERM} = 5 mV	–25%		25%	
		V_{ITERM} = 1.5 mV	–45%		45%	
	Deglitch time for termination (both edge)			100		ms
t_{QUAL}	Termination qualification time	V_{BAT} > V_{RECH} and I_{CHG}<I_{TERM}		250		ms
I_{QUAL}	Termination qualification current	Discharge current once termination is detected		2		mA
INPUT CURRENT REGULATION						
V_{ACSET}	ACSET voltage range				2	V
V_{IREG_DPM}	ACP-ACN current-sense voltage range	V_{IREG_DPM} = V_{ACP} – V_{ACN}			100	mV
K_{ACSET}	Input current set factor (amps of input current per volt on ACSET pin)	R_{SENSE} = 10 mΩ		5		A/V
I_{ACSET}	Input current regulation accuracy leakage current in to ACSET pin	V_{IREG_DPM} = 40 mV	–3%		3%	
		V_{IREG_DPM} = 20 mV	–4%		4%	
		V_{IREG_DPM} = 5 mV	–25%		25%	
I_{ISET1}	Leakage current in to ACSET pin	V_{ACSET} = 2 V			100	nA
INPUT UNDERVOLTAGE LOCKOUT COMPARATOR (UVLO)						
V_{UVLO}	AC undervoltage rising threshold	Measure on VCC	3.65	3.85	4	V
V_{UVLO_HYS}	AC undervoltage hysteresis, falling			350		mV
VCC LOWV COMPARATOR						
	Falling threshold, disable charge	Measure on VCC		4.1		V
	Rising threshold, resume charge			4.35	4.5	V
SLEEP COMPARATOR (REVERSE DISCHARGING PROTECTION)						
V_{SLEEP_FALL}	SLEEP falling threshold	V_{VCC} – V_{SRN} to enter SLEEP	40	100	150	mV
V_{SLEEP_HYS}	SLEEP hysteresis			500		mV
	SLEEP rising delay	VCC falling below SRN, delay to turn off ACFET		1		µs
	SLEEP falling delay	VCC rising above SRN, delay to turn on ACFET		30		µs
	SLEEP rising shutdown deglitch	VCC falling below SRN, delay to enter SLEEP mode		100		ms
	SLEEP falling power-up deglitch	VCC rising above SRN, delay to exit SLEEP mode		30		ms
ACN / SRN COMPARATOR						
$V_{ACN\text{-}SRN\_FALL}$	ACN to SRN falling threshold	V_{ACN} – V_{SRN} to turn on BATFET	100	200	310	mV
$V_{ACN\text{-}SRN\_HYS}$	ACN to SRN rising hysteresis			100		mV
	ACN to SRN rising deglitch	V_{ACN} – V_{SRN} > $V_{ACN\text{-}SRN\_RISE}$		2		ms
	ACN to SRN falling deglitch	V_{ACN} – V_{SRN} < $V_{ACN\text{-}SRN\_FALL}$		50		µs
BAT LOWV COMPARATOR						
V_{LOWV}	Precharge to fast-charge transition (LOWV threshold)	Measured on VFB pin, rising	1.534	1.55	1.566	V
V_{LOWV_HYS}	LOWV hysteresis			100		mV
	LOWV rising deglitch	VFB falling below V_{LOWV}		25		ms
	LOWV falling deglitch	VFB rising above V_{LOWV} + V_{LOWV_HYS}		25		ms
RECHARGE COMPARATOR						
V_{RECHG}	Recharge threshold (with-respect-to V_{REG})	Measured on VFB pin, falling	35	50	65	mV
	Recharge rising deglitch	VFB decreasing below V_{RECHG}		10		ms
	Recharge falling deglitch	VFB decreasing above V_{RECHG}		10		ms

Electrical Characteristics (continued)

5 V ≤ V_{VCC} ≤ 28 V, 0°C < T_J < 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BAT OVERVOLTAGE COMPARATOR						
V_{OV_RISE}	Overvoltage rising threshold	As percentage of V_{FB}		104%		
V_{OV_FALL}	Overvoltage falling threshold	As percentage of V_{FB}		102%		
INPUT OVERVOLTAGE COMPARATOR (ACOV)						
V_{ACOV}	AC overvoltage rising threshold on VCC (bq24610)		31.04	32	32.96	V
V_{ACOV_HYS}	AC overvoltage falling hysteresis (bq24610)			1		V
V_{ACOV}	AC overvoltage rising threshold on VCC (bq24617)		25.22	26	26.78	V
V_{ACOV_HYS}	AC overvoltage falling hysteresis(bq24617)			820		mV
	AC overvoltage deglitch (both edge)	Delay to changing the STAT pins		1		ms
	AC overvoltage rising deglitch	Delay to disable charge		1		ms
	AC overvoltage falling deglitch	Delay to resume charge		20		ms
THERMAL SHUTDOWN COMPARATOR						
T_{SHUT}	Thermal shutdown rising temperature	Temperature increasing		145		°C
T_{SHUT_HYS}	Thermal shutdown hysteresis			15		°C
	Thermal shutdown rising deglitch	Temperature increasing		100		µs
	Thermal shutdown falling deglitch	Temperature decreasing		10		ms
THERMISTOR COMPARATOR						
V_{LTF}	Cold temperature rising threshold	As Percentage to V_{VREF}	72.5%	73.5%	74.5%	
V_{LTF_HYS}	Rising hysteresis	As Percentage to V_{VREF}	0.2%	0.4%	0.6%	
V_{HTF}	Hot temperature rising threshold	As Percentage to V_{VREF}	36.2%	37%	37.8%	
V_{TCO}	Cut-off temperature rising threshold	As Percentage to V_{VREF}	33.7%	34.4%	35.1%	
	Deglitch time for temperature out-of-range detection	V_{TS} > V_{LTF}, or V_{TS} < V_{TCO}, or V_{TS} < V_{HTF}		400		ms
	Deglitch time for temperature in-valid-range detection	V_{TS} < V_{LTF} – V_{LTF_HYS} or V_{TS} >V_{TCO}, or V_{TS} > V_{HTF}		20		ms
CHARGE OVERCURRENT COMPARATOR (CYCLE-BY-CYCLE)						
V_{OC}	Charge overcurrent falling threshold	Current rising, in nonsynchronous mode, mesure on $V_{(SRP-SRN)}$, V_{SRP} < 2 V		45.5		mV
		Current rising, as percentage of $V_{(IREG\_CHG)}$, in synchronous mode, V_{SRP} > 2.2 V		160%		
	Charge overcurrent threshold floor	Minimum OCP threshold in synchronous mode, measure on $V_{(SRP-SRN)}$, V_{SRP} > 2.2 V		50		mV
	Charge overcurrent threshold ceiling	Maximum OCP threshold in synchronous mode, measure on $V_{(SRP-SRN)}$, V_{SRP} > 2.2 V		180		mV
CHARGE UNDERCURRENT COMPARATOR (CYCLE-BY-CYCLE)						
$V_{ISYNSET}$	Charge undercurrent falling threshold	Switch from SYNCH to NON-SYNCH, V_{SRP} > 2.2 V	1	5	9	mV
BATTERY SHORTED COMPARATOR (BATSHORT)						
V_{BATSHT}	BAT short falling threshold, forced nonsynchronous mode	V_{SRP} falling		2		V
V_{BATSHT_HYS}	BAT short rising hysteresis			200		mV
V_{BATSHT_DEG}	Deglitch on both edge			1		µs

Electrical Characteristics (continued)

5 V ≤ V_{VCC} ≤ 28 V, 0°C < T_J < 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOW CHARGE CURRENT COMPARATOR						
V_{LC}	Low charge current (average) falling threshold to force into nonsynchronous mode	Measure on $V_{(SRP-SRN)}$		1.25		mV
V_{LC_HYS}	Low charge current rising hysteresis			1.25		mV
V_{LC_DEG}	Deglitch on both edge			1		µs
VREF REGULATOR						
V_{VREF_REG}	VREF regulator voltage	V_{VCC} > V_{UVLO}, (0- to 35-mA load)	3.267	3.3	3.333	V
I_{VREF_LIM}	VREF current limit	V_{VREF} = 0 V, V_{VCC} > V_{UVLO}	35			mA
REGN REGULATOR						
V_{REGN_REG}	REGN regulator voltage	V_{VCC} > 10 V, CE = HIGH, (0- to 40-mA load)	5.7	6	6.3	V
I_{REGN_LIM}	REGN current limit	V_{REGN} = 0 V, V_{VCC} > V_{UVLO}, CE = HIGH	40			mA
TTC INPUT AND SAFETY TIMER						
T_{PRECHG}	Precharge safety timer range(1)	Precharge time before fault occurs	1440	1800	2160	s
T_{CHARGE}	Fast charge safety timer range, with +/– 10% accuracy(1)	Tchg = C_{TTC} × K_{TTC}	1		10	h
	Fast charge timer accuracy(1)	0.01 µF ≤ C_{TTC} ≤ 0.11 µF	–10%		10%	
K_{TTC}	Timer multiplier			5.6		min/nF
	TTC low threshold	V_{TTC} below this threshold disables the safety timer and termination			0.4	V
	TTC oscillator high threshold			1.5		V
	TTC oscillator low threshold			1		V
	TTC source/sink current		45	50	55	µA
BATTERY SWITCH (BATFET) DRIVER						
$R_{DS\_BAT\_OFF}$	BATFET turnoff resistance	V_{ACN} > 5 V			150	Ω
$R_{DS\_BAT\_ON}$	BATFET turnon resistance	V_{ACN} > 5 V			20	kΩ
V_{BATDRV_REG}	BATFET drive voltage	V_{BATDRV_REG} = V_{ACN} – V_{BATDRV} when V_{ACN} > 5 V and BATFET is on	4.2		7	V
AC SWITCH (ACFET) DRIVER						
$R_{DS\_AC\_OFF}$	ACFET turnoff resistance	V_{VCC} > 5 V			30	Ω
$R_{DS\_AC\_ON}$	ACFET turnon resistance	V_{VCC} > 5 V			20	kΩ
V_{ACDRV_REG}	ACFET drive voltage	V_{ACDRV_REG} = V_{VCC} – V_{ACDRV} when V_{VCC} > 5 V and ACFET is on	4.2		7	V
AC / BAT MOSFET DRIVERS TIMING						
	Driver dead time	Dead time when switching between AC and BAT		10		µs
BATTERY DETECTION						
t_{WAKE}	Wake time	Max time charge is enabled		500		ms
I_{WAKE}	Wake current	R_{SENSE} = 10 mΩ	50	125	200	mA
$t_{DISCHARGE}$	Discharge time	Maximum time discharge current is applied		1		s
$I_{DISCHARGE}$	Discharge current			8		mA
I_{FAULT}	Fault current after a timeout fault			2		mA
V_{WAKE}	Wake threshold (with-respect-to V_{REG})	Voltage on VFB to detect battery absent during wake		50		mV
V_{DISCH}	Discharge threshold	Voltage on VFB to detect battery absent during discharge		1.55		V

(1) Verified by design.

Electrical Characteristics (continued)

5 V ≤ V_{VCC} ≤ 28 V, 0°C < T_J < 125°C, typical values are at T_A = 25°C, with respect to GND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM HIGH-SIDE DRIVER (HIDRV)						
$R_{DS\_HI\_ON}$	High-side driver (HSD) turnon resistance	$V_{BTST} – V_{PH}$ = 5.5 V		3.3	6	Ω
$R_{DS\_HI\_OFF}$	High-side driver turnoff resistance	$V_{BTST} – V_{PH}$ = 5.5 V		1	1.3	Ω
$V_{BTST\_REFRESH}$	Bootstrap refresh comparator threshold voltage	$V_{BTST} – V_{PH}$ when low side refresh pulse is requested	4	4.2		V
PWM LOW-SIDE DRIVER (LODRV)						
$R_{DS\_LO\_ON}$	Low-side driver (LSD) turnon resistance			4.1	7	Ω
$R_{DS\_LO\_OFF}$	Low-side driver turnoff resistance			1	1.4	Ω
PWM DRIVERS TIMING						
	Driver dead time	Dead time when switching between LSD and HSD, no load at LSD and HSD		30		ns
PWM OSCILLATOR						
V_{RAMP_HEIGHT}	PWM ramp height	As percentage of VCC		7%		
	PWM switching frequency(1)		510	600	690	kHz
INTERNAL SOFT START (8 steps to regulation current ICHG)						
	Soft-start steps			8		step
	Soft-start step time			1.6		ms
CHARGER SECTION POWER-UP SEQUENCING						
	Charge-enable delay after power up	Delay from CE = 1 to charger is allowed to turn on		1.5		s
LOGIC IO PIN CHARACTERISTICS (CE, STAT1, STAT2, $\overline{PG}$)						
V_{IN_LO}	CE input low threshold voltage				0.8	V
V_{IN_HI}	CE input high threshold voltage		2.1			
V_{BIAS_CE}	CE input bias current	V = 3.3 V (CE has internal 1-MΩ pulldown resistor)			6	µA
V_{OUT_LO}	STAT1, STAT2, $\overline{PG}$ output-low saturation voltage	Sink Current = 5 mA			0.5	V
I_{OUT_HI}	Leakage current	V = 32 V			1.2	µA

8.6 Typical Characteristics

Table 1. Table of Graphs

	FIGURE
REF REGN and $\overline{PG}$ Power Up (CE = 1)	Figure 1
Charge Enable	Figure 2
Current Soft Start (CE = 1)	Figure 3
Charge Disable	Figure 4
Continuous Conduction Mode Switching Waveforms	Figure 5
Cycle-by-Cycle Synchronous to Nonsynchronous	Figure 6
100% Duty and Refresh Pulse	Figure 7
Transient System Load (DPM)	Figure 8
Battery Insertion	Figure 9
Battery-to-Ground Short Protection	Figure 10
Battery-to-Ground Short Transition	Figure 11
Efficiency vs Output Current	Figure 12

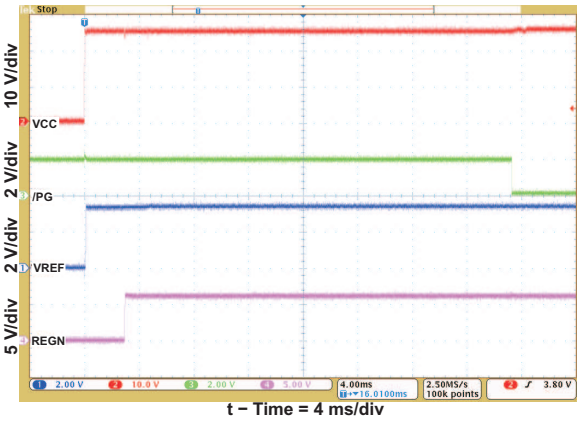


Figure 1. REF REGN and $\overline{PG}$ Power Up (CE = 1)

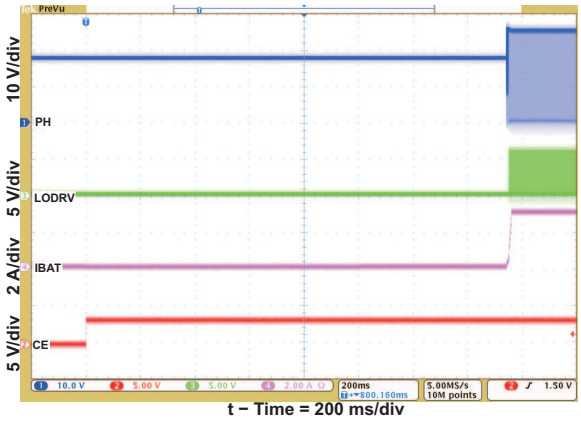


Figure 2. Charge Enable

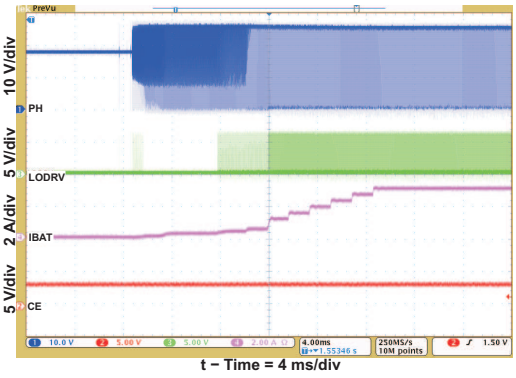


Figure 3. Current Soft Start (CE = 1)

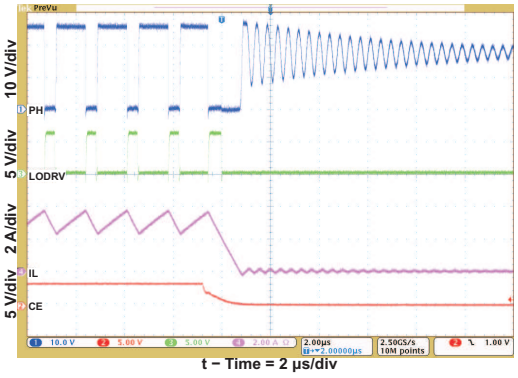


Figure 4. Charge Disable

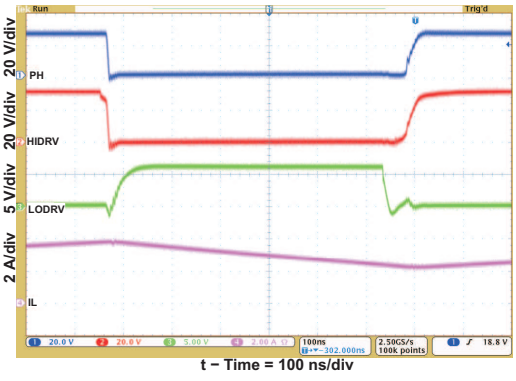


Figure 5. Continuous Conduction Mode Switching Waveforms

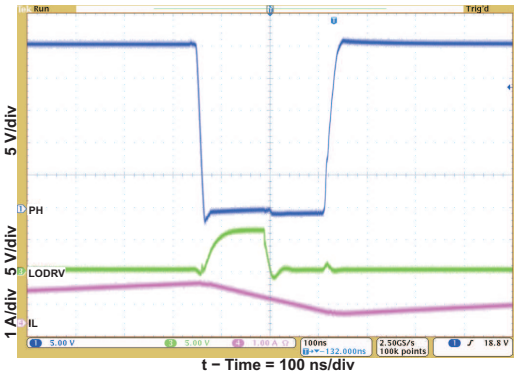


Figure 6. Cycle-by-Cycle Synchronous to Nonsynchronous

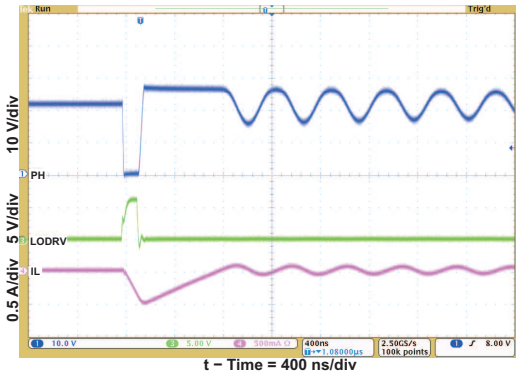


Figure 7. 100% Duty and Refresh Pulse

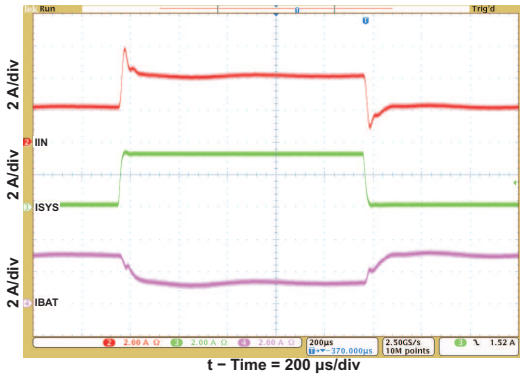


Figure 8. Transient System Load (DPM)

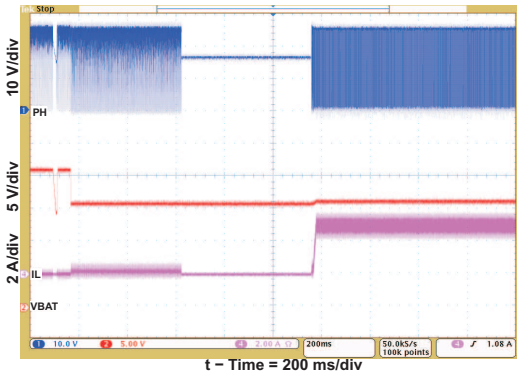


Figure 9. Battery Insertion

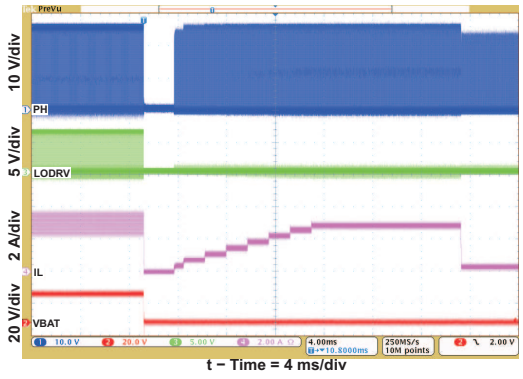


Figure 10. Battery-to-GND Short Protection

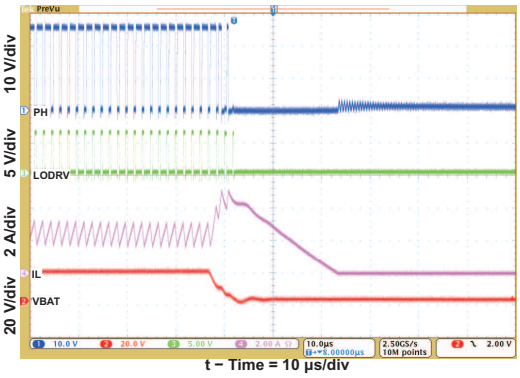


Figure 11. Battery-to-GND Short Transition

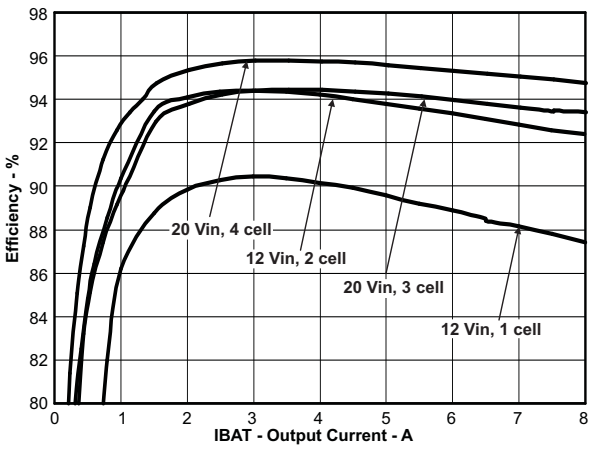


Figure 12. Efficiency vs Output Current

9 Detailed Description

9.1 Overview

The bq2461x device is a stand-alone, integrated Li-ion or Li-polymer battery charger. The device employs a switched-mode synchronous buck PWM controller with constant switching frequency. The device controls external switches to prevent battery discharge back to the input, connect the adapter to the system, and connect the battery to the system using 6-V gate drives for better system efficiency. The bq2461x features Dynamic Power Management (DPM) which reduces battery charge current when the input power limit is reached to avoid overloading the AC adapter when supplying current to the system and the battery charger simultaneously. A highly accurate current-sense amplifier enables precise measurement of input current from the AC adapter to monitor the overall system power. The input current limit can be configured through the ACSET pin of the device.

The bq2461x has a battery detect scheme that allows it to automatically detect the presence and absence of a battery. When the battery is detected, charging begins in one of three phases (depending upon battery voltage): precharge, constant current (fast-charge current regulation), and constant voltage (fast-charge voltage regulation). The device will terminate charging when the termination current threshold has been reached and will begin a recharge cycle when the battery voltage has dropped below the recharge threshold (V_{RECHG}). Precharge, constant current, and termination current can be configured through the ISET1 and ISET2 pins, allowing for flexibility in battery charging profile. During charging, the integrated fault monitors of the device, such as battery overvoltage protection, battery short detection (V_{BATSHT}), thermal shutdown (internal T_{SHUT} and TS pin), safety timer expiration (TTC pin), and input voltage protection (V_{ACOV}), ensure battery safety.

The bq2461x has three status pins (STAT1, STAT2, and $\overline{PG}$) to indicate the charging status and input voltage (AC adapter) status. These pins can be used to drive LEDs or communicate with a host processor.

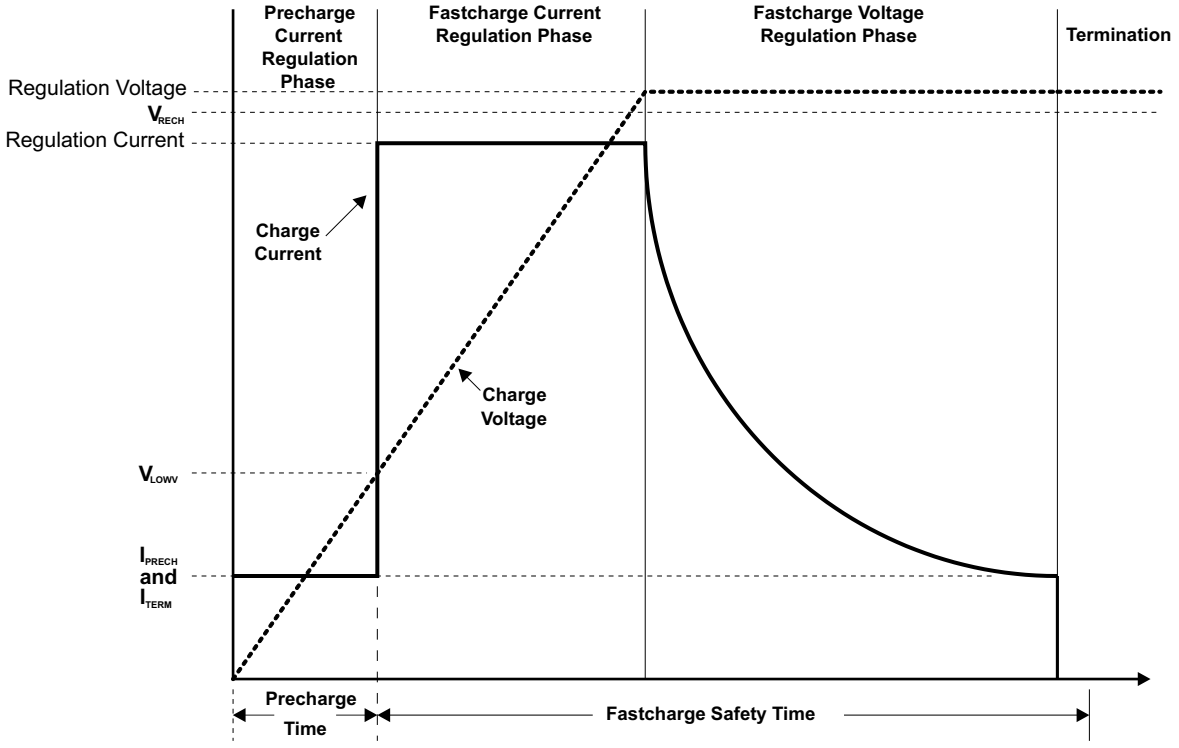
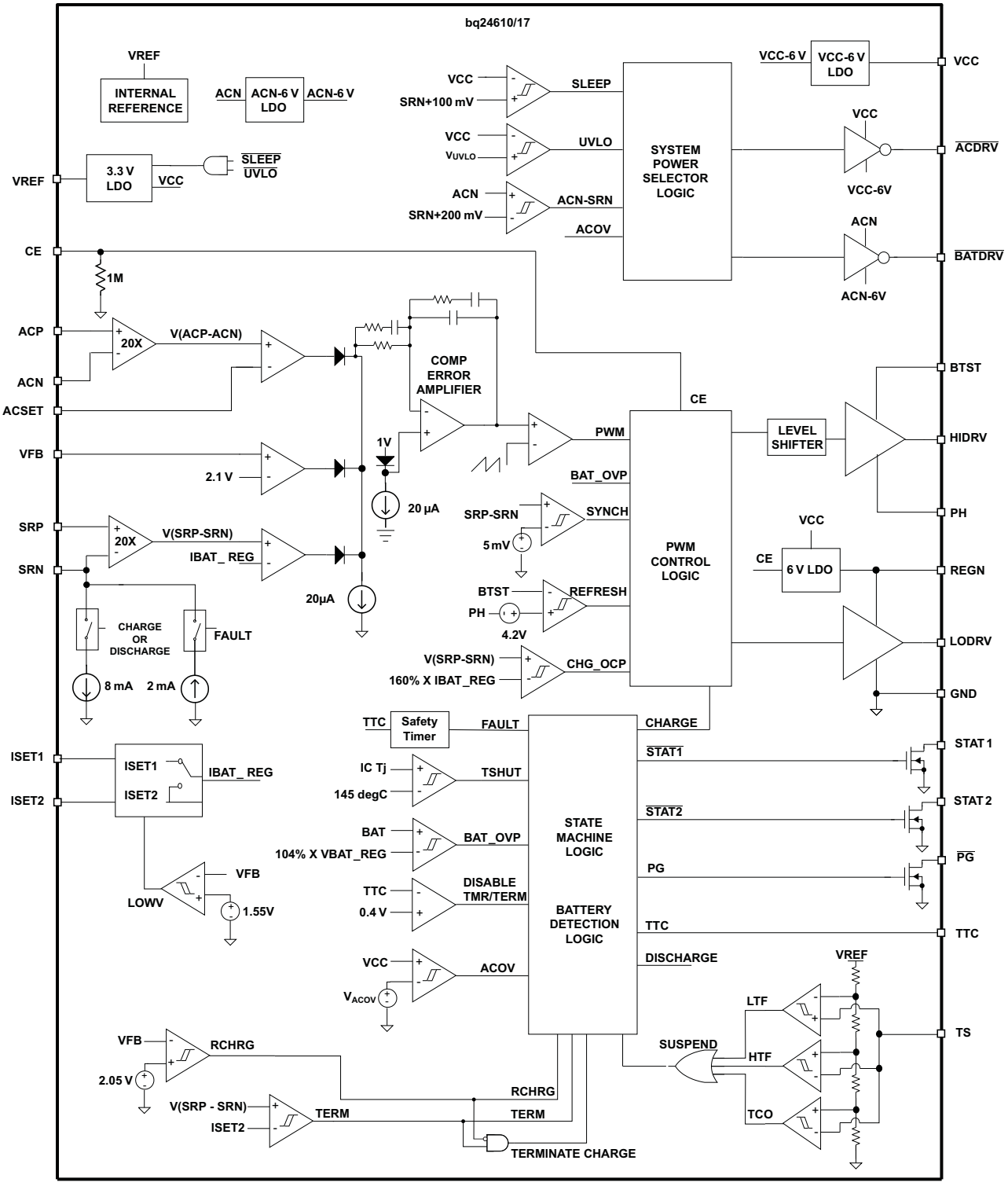


Figure 13. Typical Charging Profile

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Battery Voltage Regulation

The bq2461x uses a high-accuracy voltage bandgap and regulator for the high charging voltage accuracy. The charge voltage is programmed through a resistor divider from the battery to ground, with the midpoint tied to the VFB pin. The voltage at the VFB pin is regulated to 2.1 V, giving the following equation for the regulation voltage:

$$V_{BAT} = 2.1\ V \times \left[1 + \frac{R2}{R1}\right], \quad (1)$$

where

- R2 is connected from VFB to the battery and R1 is connected from VFB to GND.

9.3.2 Battery Current Regulation

The ISET1 input sets the maximum fast-charging current. Battery charge current is sensed by resistor R_{SR} connected between SRP and SRN. The full-scale differential voltage between SRP and SRN is 100 mV. Thus, for a 10-mΩ sense resistor, the maximum charging current is 10 A. The equation for charge current is:

$$I_{CHARGE} = \frac{V_{ISET1}}{20 \times R_{SR}} \quad (2)$$

V_{ISET1}, the input voltage range of ISET1, is from 0 V to 2 V. The SRP and SRN pins are used to sense voltage across R_{SR} with default value of 10 mΩ. However, resistors of other values can also be used. A larger sense resistor gives a larger sense voltage and a higher regulation accuracy, but at the expense of higher conduction loss.

9.3.3 Input Adapter Current Regulation

The total input from an AC adapter or other DC source is a function of the system supply current and the battery charging current. System current normally fluctuates as portions of the systems are powered up or down. Without DPM, the source must be able to supply the maximum system current and the maximum charger input current simultaneously. By using DPM, the battery charger reduces the charging current when the input current exceeds the input current limit set by ACSET. The current capability of the AC adapter can be lowered, reducing system cost.

Similar to setting battery regulation current, adapter current is sensed by resistor R_{AC} connected between ACP and ACN. Its maximum value is set by ACSET using Equation 3:

$$I_{DPM} = \frac{V_{ACSET}}{20 \times R_{AC}} \quad (3)$$

V_{ACSET}, the input voltage range of ACSET, is from 0 V to 2 V. The ACP and ACN pins are used to sense voltage across R_{AC} with default value of 10 mΩ. However, resistors of other values can also be used. A larger the sense resistor gives a larger sense voltage and a higher regulation accuracy, but at the expense of higher conduction loss.

9.3.4 Precharge

On power up, if the battery voltage is below the V_{LOWV} threshold, the bq2461x applies the precharge current to the battery. This feature is intended to revive deeply discharged cells. If the V_{LOWV} threshold is not reached within 30 minutes of initiating precharge, the charger turns off and a FAULT is indicated on the status pins.

The precharge current is determined by the voltage, V_{ISET2}, on the ISET2 pin.

$$I_{PRECHARGE} = \frac{V_{ISET2}}{100 \times R_{SR}} \quad (4)$$

9.3.5 Charge Termination, Recharge, and Safety Timer

The bq2461x monitors the charging current during the voltage regulation phase. When V_{TTC} is valid, termination is detected while the voltage on the VFB pin is higher than the V_{RECH} threshold AND the charge current is less than the I_{TERM} threshold, as calculated in Equation 5:

Feature Description (continued)

$$I_{TERM} = \frac{V_{ISET2}}{100 \times R_{SR}} \quad (5)$$

The input voltage of ISET2 is from 0 V to 2 V. The minimum precharge/termination current is clamped to be around 125 mA with default 10-mΩ sensing resistor. As a safety backup, the bq2461x also provides a programmable charge timer. The charge time is programmed by the capacitor connected between the TTC pin and GND, and is given by Equation 6

$$t_{CHARGE} = C_{TTC} \times K_{TTC} \quad (6)$$

where

- C_{TTC} (range from 0.01 µF to 0.11 µF to give 1- to 10-h safety time) is the capacitor connected from TTC pin to GND.
- K_{TTC} is the constant multiplier (5.6 min/nF).

A new charge cycle is initiated and safety timer is reset when one of the following conditions occurs:

- The battery voltage falls below the recharge threshold.
- A power-on-reset (POR) event occurs.
- CE is toggled.

The TTC pin may be taken LOW to disable termination and to disable the safety timer. If TTC is pulled to VREF, the bq2461x continues to allow termination, but disables the safety timer. TTC taken low resets the safety timer. When ACOV, VCCLOWV, and SLEEP mode resume normal, the safety timer is reset.

9.3.6 Power Up

The bq2461x uses a SLEEP comparator to determine the source of power on the VCC pin, because VCC can be supplied either from the battery or the adapter. If the VCC voltage is greater than the SRN voltage, bq2461x enables the ACFET and disables BATFET. If all other conditions are met for charging, the bq2461x then attempts to charge the battery (see *Enable and Disable Charging*). If the SRN voltage is greater than VCC, indicating that the battery is the power source, the bq2461x enables the BATFET and enters a low quiescent current (<15 µA) SLEEP mode to minimize current drain from the battery.

If VCC is below the UVLO threshold, the device is disabled, ACFET turns off and BATFET turns on.

9.3.7 Enable and Disable Charging

The following conditions must be valid before charge is enabled:

- CE is HIGH.
- The device is not in undervoltage lockout (UVLO) and not in VCCLOWV mode.
- The device is not in SLEEP mode.
- The VCC voltage is lower than the AC overvoltage threshold (VCC < V_{ACOV}).
- 30-ms delay is complete after initial power up.
- The REGN LDO and VREF LDO voltages are at the correct levels.
- Thermal shut (TSHUT) is not valid.
- TS fault is not detected.

One of the following conditions will stop ongoing charging:

- CE is LOW.
- Adapter is removed, causing the device to enter UVLO, VCCLOWV, or SLEEP mode.
- Adapter is over voltage.
- The REGN or VREF LDO is overloaded.
- TSHUT IC temperature threshold is reached (145°C on rising edge with 15°C hysteresis).
- TS voltage goes out of range, indicating the battery temperature is too hot or too cold.
- TTC safety timer out.

Feature Description (continued)

9.3.8 System Power Selector

The bq2461x automatically switches adapter or battery power to the system load. The battery is connected to the system by default during power up or during SLEEP mode. The battery is disconnected from the system and then the adapter is connected to the system 30 ms after exiting SLEEP. An automatic break-before-make logic prevents shoot-through currents when the selectors switch.

The $\overline{\text{ACDRV}}$ is used to drive a pair of back-to-back P-channel power MOSFETs between the adapter and ACP with sources connected together and to VCC. The FET connected to the adapter prevents reverse discharge from the battery to the adapter when turned off. The P-channel FET with the drain connected to the adapter input provides reverse battery discharge protection when off; and also minimizes system power dissipation with its low $r_{DS(on)}$, compared to a Schottky diode. The other P-channel FET connected to ACP separates the battery from the adapter, and provides a limited dI/dt when connecting the adapter to the system by controlling the FET turnon time. The $\overline{\text{BATDRV}}$ controls a P-channel power MOSFET placed between BAT and the system.

When the adapter is not detected, $\overline{\text{ACDRV}}$ is pulled to VCC to keep ACFET off, disconnecting the adapter from system. $\overline{\text{BATDRV}}$ stays at ACN-6V to connect the battery to the system.

Approximately 30 ms after the device comes out of SLEEP mode, the system begins to switch from the battery to the adapter. The break-before-make logic keeps both ACFET and BATFET off for 10 µs before ACFET turns on. This prevents shoot-through current or any large discharging current from going into the battery. $\overline{\text{BATDRV}}$ is pulled up to ACN and the $\overline{\text{ACDRV}}$ pin is set to VCC-6V by an internal regulator to turn on P-channel ACFET, connecting the adapter to the system.

When the adapter is removed, the system waits until VCC drops back to within 200 mV above SRN to switch from the adapter back to the battery. The break-before-make logic still keeps 10 µs dead time. The $\overline{\text{ACDRV}}$ is pulled up to VCC and the $\overline{\text{BATDRV}}$ pin is set to ACN-6V by an internal regulator to turn on P-channel BATFET, connecting the battery to the system.

Asymmetrical gate drive (fast turnoff and slow turnon) for the $\overline{\text{ACDRV}}$ and $\overline{\text{BATDRV}}$ drivers provides fast turnoff and slow turnon of the ACFET and BATFET to help the break-before-make logic and to allow a soft start at turnon of either FET. The soft-start time can be further increased by putting a capacitor from gate to source of the P-channel power MOSFETs.

9.3.9 Automatic Internal Soft-Start Charger Current

The charger automatically soft starts the charger regulation current every time the charger goes into fast charge to ensure there is no overshoot or stress on the output capacitors or the power converter. The soft start consists of stepping-up the charge regulation current into eight evenly divided steps up to the programmed charge current. Each step lasts around 1.6 ms, for a typical rise time of 12.8 ms. No external components are needed for this function.

9.3.10 Converter Operation

The synchronous buck PWM converter uses a fixed-frequency voltage mode with feed-forward control scheme. A type-III compensation network allows using ceramic capacitors at the output of the converter. The compensation input stage is connected internally between the feedback output (FBO) and the error amplifier input (EAI). The feedback compensation stage is connected between the error amplifier input (EAI) and error amplifier output (EAO). The LC output filter is selected to give a resonant frequency of 12 kHz to 17 kHz for bq2461x, where the resonant frequency, f_o, is given by:

$$f_o = \frac{1}{2\pi\sqrt{L_o C_o}} \tag{7}$$

An internal saw-tooth ramp is compared to the internal EAO error control signal to vary the duty cycle of the converter. The ramp height is 7% of the input adapter voltage, making it always directly proportional to the input adapter voltage. This cancels out any loop gain variation due to a change in input voltage, and simplifies the loop compensation. The ramp is offset by 300 mV in order to allow zero-percent duty cycle when the EAO signal is below the ramp. The EAO signal is also allowed to exceed the sawtooth ramp signal in order to get a 100% duty-cycle PWM request. Internal gate-drive logic allows achieving 99.5% duty cycle while ensuring the N-channel

Feature Description (continued)

upper device always has enough voltage to stay fully on. If the BTST pin to PH pin voltage falls below 4.2 V for more than 3 cycles, then the high-side N-channel power MOSFET is turned off and the low-side N-channel power MOSFET is turned on to pull the PH node down and recharge the BTST capacitor. Then the high-side driver returns to 100% duty-cycle operation until the (BTST-PH) voltage is detected to fall low again due to leakage current discharging the BTST capacitor below 4.2 V, and the reset pulse is reissued.

The fixed-frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current, and temperature, simplifying output filter design and keeping it out of the audible noise region. Also see *Application and Implementation* for how to select the inductor, capacitor, and MOSFET.

9.3.11 Synchronous and Nonsynchronous Operation

The charger operates in synchronous mode when the SRP-SRN voltage is above 5 mV (0.5-A inductor current for a 10 mΩ sense resistor). During synchronous mode, the internal gate-drive logic ensures there is break-before-make complimentary switching to prevent shoot-through currents. During the 30 ns dead time where both FETs are off, the body diode of the low-side power MOSFET conducts the inductor current. Having the low-side FET turn on keeps the power dissipation low, and allows safely charging at high currents. During synchronous mode, the inductor current is always flowing and the converter operates in Continuous Conduction Mode (CCM), creating a fixed two-pole system.

The charger operates in nonsynchronous mode when the SRP-SRN voltage is below 5 mV (0.5-A inductor current for a 10-mΩ sense resistor). The charger is forced into nonsynchronous mode when battery voltage is lower than 2 V or when the average SRP-SRN voltage is lower than 1.25 mV.

During nonsynchronous operation, the body diode of lower-side MOSFET can conduct the positive inductor current after the high-side N-channel power MOSFET turns off. When the load current decreases and the inductor current drops to zero, the body diode is turned off and the inductor current becomes discontinuous. This mode is called Discontinuous Conduction Mode (DCM). During DCM, the low-side N-channel power MOSFET turns on for around 80 ns when the bootstrap capacitor voltage drops below 4.2 V; then the low-side power MOSFET turns off and stays off until the beginning of the next cycle, where the high-side power MOSFET is turned on again. The 80-ns low-side MOSFET on-time is required to ensure the bootstrap capacitor is always recharged and able to keep the high-side power MOSFET on during the next cycle. This is important for battery chargers, where unlike regular DC-DC converters, there is a battery load that maintains a voltage and can both source and sink current. The 80-ns low-side pulse pulls the PH node (connection between high- and low-side MOSFET) down, allowing the bootstrap capacitor to recharge up to the REGN LDO value. After the 80 ns, the low-side MOSFET is kept off to prevent negative inductor current from occurring.

At very low currents during nonsynchronous operation, there may be a small amount of negative inductor current during the 80-ns recharge pulse. The charge should be low enough to be absorbed by the input capacitance. Whenever the converter goes into zero-percent duty cycle, the high-side MOSFET does not turn on, and the low-side MOSFET does not turn on (only 80 ns recharge pulse) either, and there is almost no discharge from the battery.

During the DCM mode, the loop response automatically changes and has a single-pole system at which the pole is proportional to the load current because the converter does not sink current and only the load provides a current sink. This means at very low currents, the loop response is slower, as there is less sinking current available to discharge the output voltage.

9.3.12 Cycle-by-Cycle Charge Undercurrent Protection

If the SRP-SRN voltage decreases below 5 mV (the charger is also forced into nonsynchronous mode when the average SRP-SRN voltage is lower than 1.25 mV), the low-side FET is turned off for the remainder of the switching cycle to prevent negative inductor current. During DCM, the low-side FET only turns on for around 80 ns when the bootstrap capacitor voltage drops below 4.2 V to provide refresh charge for the bootstrap capacitor. This is important to prevent negative inductor current from causing a boost effect in which the input voltage increases, as power is transferred from the battery to the input capacitors and leads to an overvoltage stress on the VCC node and potentially causes damage to the system.

9.3.13 Input Overvoltage Protection (ACOV)

ACOV provides protection to prevent system damage due to high input voltage. Once the adapter voltage reaches the ACOV threshold, charge is disabled and the system is switched to the battery instead of the adapter.

Feature Description (continued)

9.3.14 Input Undervoltage Lockout (UVLO)

The system must have a minimum VCC voltage to allow proper operation. This VCC voltage could come from either input adapter or battery, because a conduction path exists from the battery to VCC through the high-side NMOS body diode. When VCC is below the UVLO threshold, all circuits on the IC are disabled, and the gate-drive bias to ACFET and BATFET is disabled.

9.3.15 Battery Overvoltage Protection

The converter does not allow the high-side FET to turn on until the BAT voltage goes below 102% of the regulation voltage. This allows one-cycle response to an overvoltage condition, such as occurs when the load is removed or the battery is disconnected. An 8-mA current sink from SRP to GND is on only during charge and allows discharging the stored output inductor energy that is transferred to the output capacitors. BATOVP also suspends the safety timer.

9.3.16 Cycle-by-Cycle Charge Overcurrent Protection

The charger has a secondary cycle-to-cycle overcurrent protection. It monitors the charge current, and prevents the current from exceeding 160% of the programmed charge current. The high-side gate drive turns off when the overcurrent is detected, and automatically resumes when the current falls below the overcurrent threshold.

9.3.17 Thermal Shutdown Protection

The QFN package has low thermal impedance, which provides good thermal conduction from the silicon to the ambient, to keep junction temperatures low. As an added level of protection, the charger converter turns off and self-protects whenever the junction temperature exceeds the TSHUT threshold of 145°C. The charger stays off until the junction temperature falls below 130°C; then the charger will soft start again if all other enable charge conditions are valid. Thermal shutdown also suspends the safety timer.

9.3.18 Temperature Qualification

The controller continuously monitors battery temperature by measuring the voltage between the TS pin and GND. A negative temperature coefficient thermistor (NTC) and an external voltage divider typically develop this voltage. The controller compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the battery temperature must be within the V_{LTF} to V_{HTF} thresholds. If battery temperature is outside of this range, the controller suspends charge and the safety timer, and waits until the battery temperature is within the V_{LTF} to V_{HTF} range. During the charge cycle, the battery temperature must be within the V_{LTF} to V_{TCO} thresholds. If battery temperature is outside of this range, the controller suspends charge and waits until the battery temperature is within the V_{LTF} to V_{HTF} range. The controller suspends charge by turning off the PWM charge FETs. Figure 14 summarizes the operation.

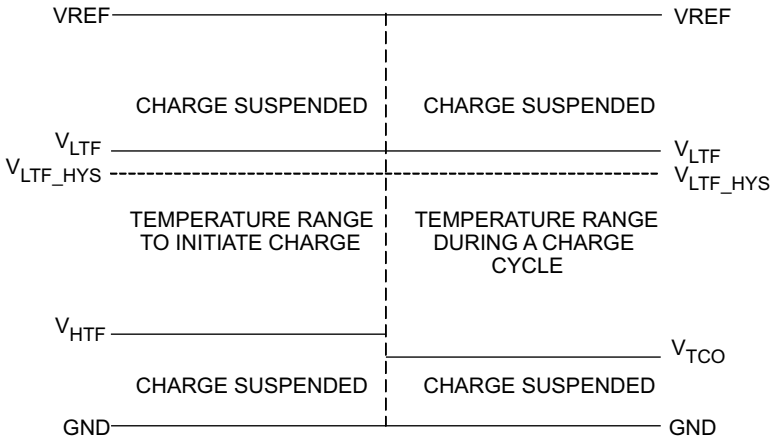


Figure 14. TS Pin, Thermistor Sense Thresholds

Feature Description (continued)

Assuming a 103AT NTC thermistor on the battery pack as shown in Figure 19, the value RT1 and RT2 can be determined by using the following equations:

$$RT2 = \frac{V_{VREF} \times RTH_{COLD} \times RTH_{HOT} \times \left(\frac{1}{V_{LTF}} - \frac{1}{V_{TCO}}\right)}{RTH_{HOT} \times \left(\frac{V_{VREF}}{V_{TCO}} - 1\right) - RTH_{COLD} \times \left(\frac{V_{VREF}}{V_{LTF}} - 1\right)} \quad (8)$$

$$RT1 = \frac{\frac{V_{VREF}}{V_{LTF}} - 1}{\frac{1}{RT2} + \frac{1}{RTH_{COLD}}} \quad (9)$$

For example, 103AT NTC thermistors are used to monitor the battery pack temperature. Select T_{COLD} = 0ºC and T_{CUT_OFF} = 45ºC; then we get R_{T2} = 430 kΩ, R_{T1} = 9.31 kΩ. A small RC filter is suggested to use for system-level ESD protection.

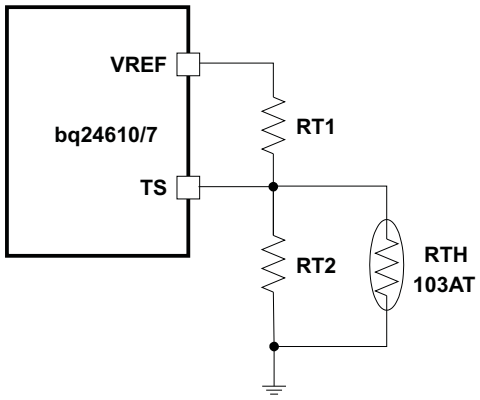


Figure 15. TS Resistor Network

9.3.19 Timer Fault Recovery

The bq2461x provides a recovery method to deal with timer fault conditions. The following summarizes this method:

Condition 1: The battery voltage is above the recharge threshold and a timeout fault occurs.

Recovery Method: The timer fault clears when the battery voltage falls below the recharge threshold, and battery detection will begin. Taking CE low or a POR condition also clears the fault.

Condition 2: The battery voltage is below the recharge threshold and a timeout fault occurs.

Recovery Method: Under this scenario, the bq2461x applies the I_{FAULT} current to the battery. This small current is used to detect a battery removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the battery voltage goes above the recharge threshold, the bq2461x disables the fault current and executes the recovery method described in Condition 1. Taking CE low or a POR condition also clears the fault.

9.3.20 $\overline{PG}$ Output

The open-drain $\overline{PG}$ (power-good) output indicates whether the VCC voltage is valid or not. The open-drain FET turns on whenever bq2461x has a valid VCC input (not in UVLO or ACOV or SLEEP mode). The $\overline{PG}$pin can be used to drive an LED or communicate to the host processor.

Feature Description (continued)

9.3.21 CE (Charge Enable)

The CE digital input is used to disable or enable the charge process. A high-level signal on this pin enables charge, provided all the other conditions for charge are met (see *Enable and Disable Charging*). A high-to-low transition on this pin also resets all timers and fault conditions. There is an internal 1-MΩ pulldown resistor on the CE pin, so if CE is floated the charge does not turn on.

9.3.22 Charge Status Outputs

The open-drain STAT1 and STAT2 outputs indicate various charger operations as shown in the Table 2. These status pins can be used to drive LEDs or communicate with the host processor. OFF indicates that the open-drain transistor is turned off.

Table 2. STAT Pin Definition for bq2461x

CHARGE STATE	STAT1	STAT2
Charge in progress	ON	OFF
Charge complete	OFF	ON
Charge suspend, timer fault, overvoltage, sleep mode, battery absent	OFF	OFF

9.3.23 Battery Detection

For applications with removable battery packs, bq2461x provides a battery-absent detection scheme to reliably detect insertion or removal of battery packs.

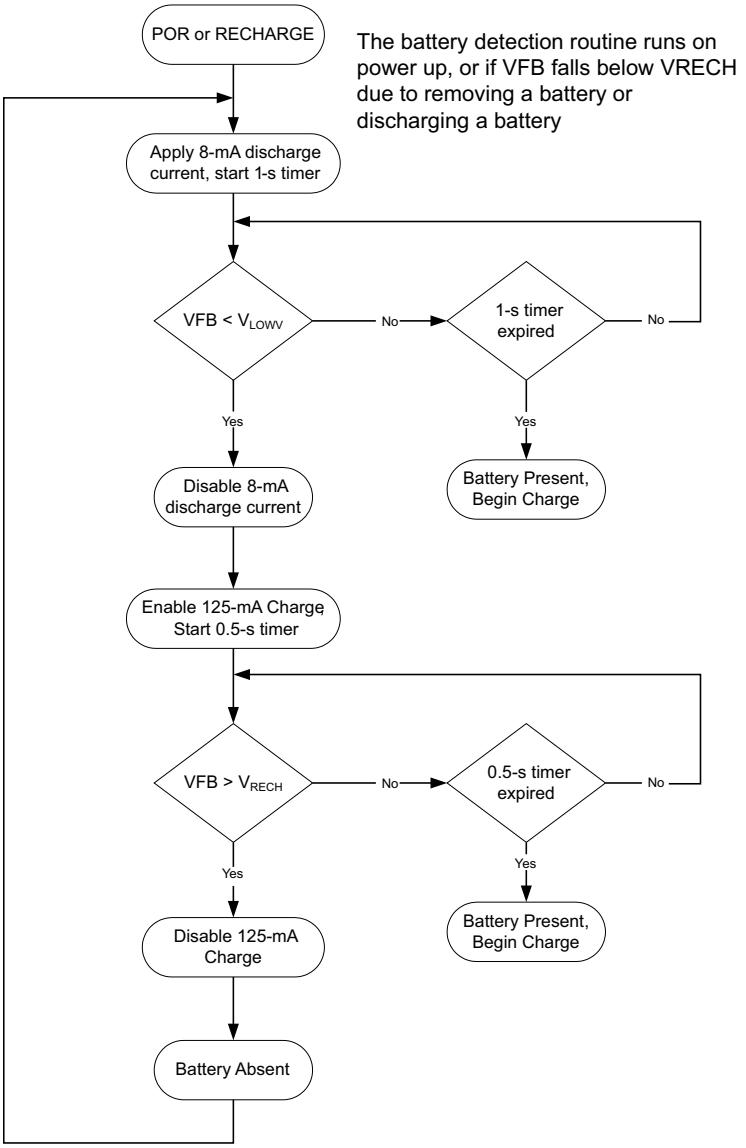


Figure 16. Battery Detection Flow Chart

Once the device has powered up, an 8-mA discharge current is applied to the SRN terminal. If the battery voltage falls below the LOWV threshold within 1 second, the discharge source is turned off, and the charger is turned on at low charge current (125 mA). If the battery voltage rises above the recharge threshold within 500 ms, there is no battery present and the cycle restarts. If either the 500-ms or 1-second timer times out before its respective threshold is hit, a battery is detected and a charge cycle is initiated.

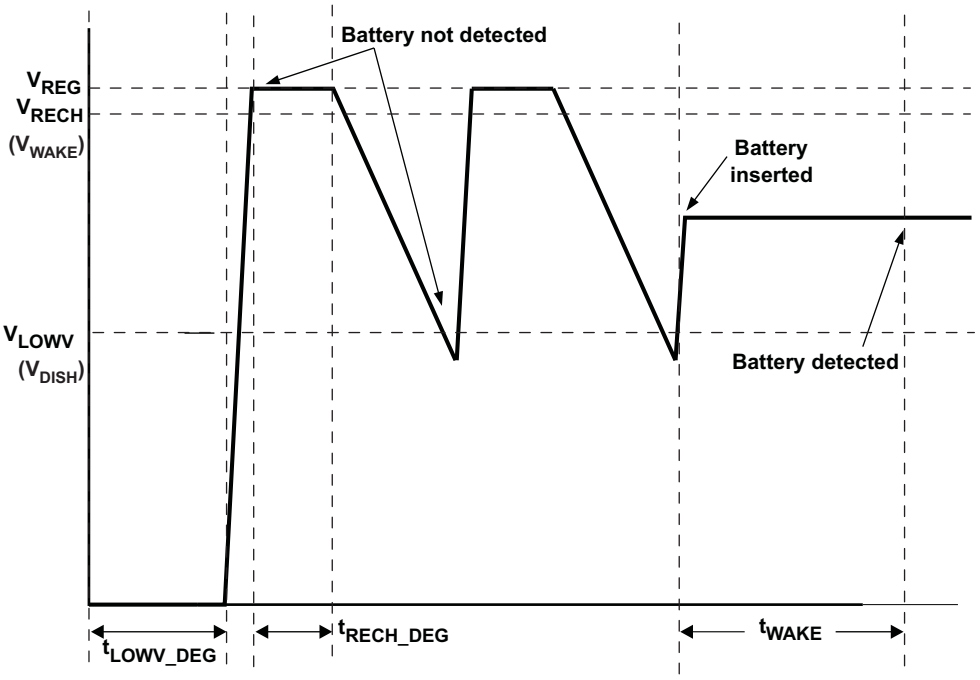


Figure 17. Battery Detect Timing Diagram

Ensure that the total output capacitance at the battery node is not so large that the discharge current source cannot pull the voltage below the LOWV threshold during the 1-second discharge time. The maximum output capacitance can be calculated as follows:

$$C_{MAX} = \frac{I_{DISCH} \times t_{DISCH}}{0.5 \times \left[1 + \frac{R_2}{R_1}\right]} \quad (10)$$

where

- C_{MAX} is the maximum output capacitance.
- I_{DISCH} is the discharge current.
- t_{DISCH} is the discharge time.
- R_2 and R_1 are the voltage feedback resistors from the battery to the VFB pin.

The 0.5 factor is the difference between the RECHARGE and the LOWV thresholds at the VFB pin.

Example

For a 3-cell Li+ charger, with R2 = 500 kΩ, R1 = 100 kΩ (giving 12.6 V for voltage regulation), I_{DISCH} = 8 mA, t_{DISCH} = 1 second,

$$C_{MAX} = \frac{8mA \times 1sec}{0.5 \times \left[1 + \frac{500k}{100k}\right]} = 2.7\ mF \quad (11)$$

Based on these calculations, no more than 2.7 mF should be allowed on the battery node for proper operation of the battery detection circuit.

9.4 Device Functional Modes

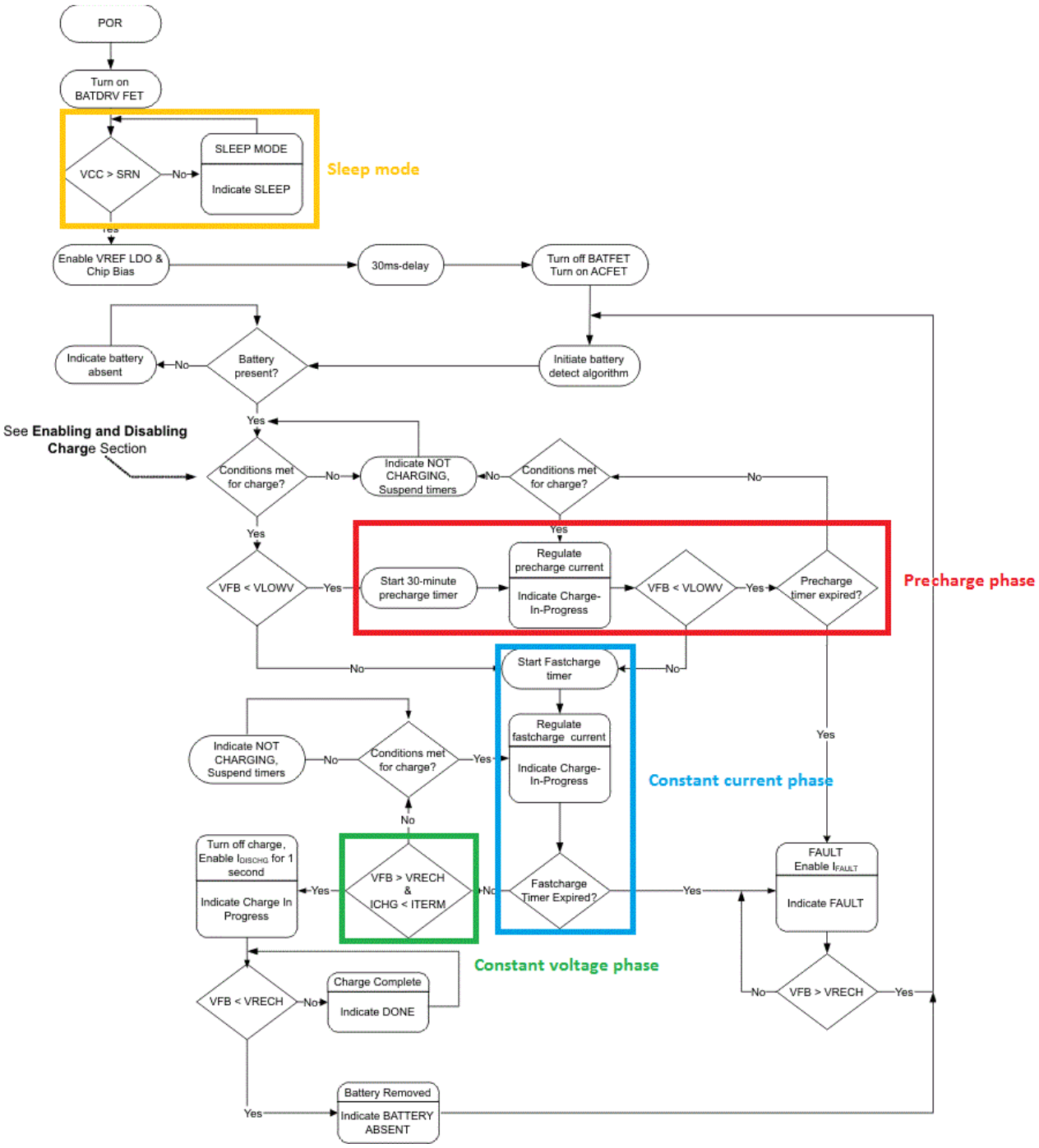


Figure 18. Device Operation Flow Chart

10 Application and Implementation

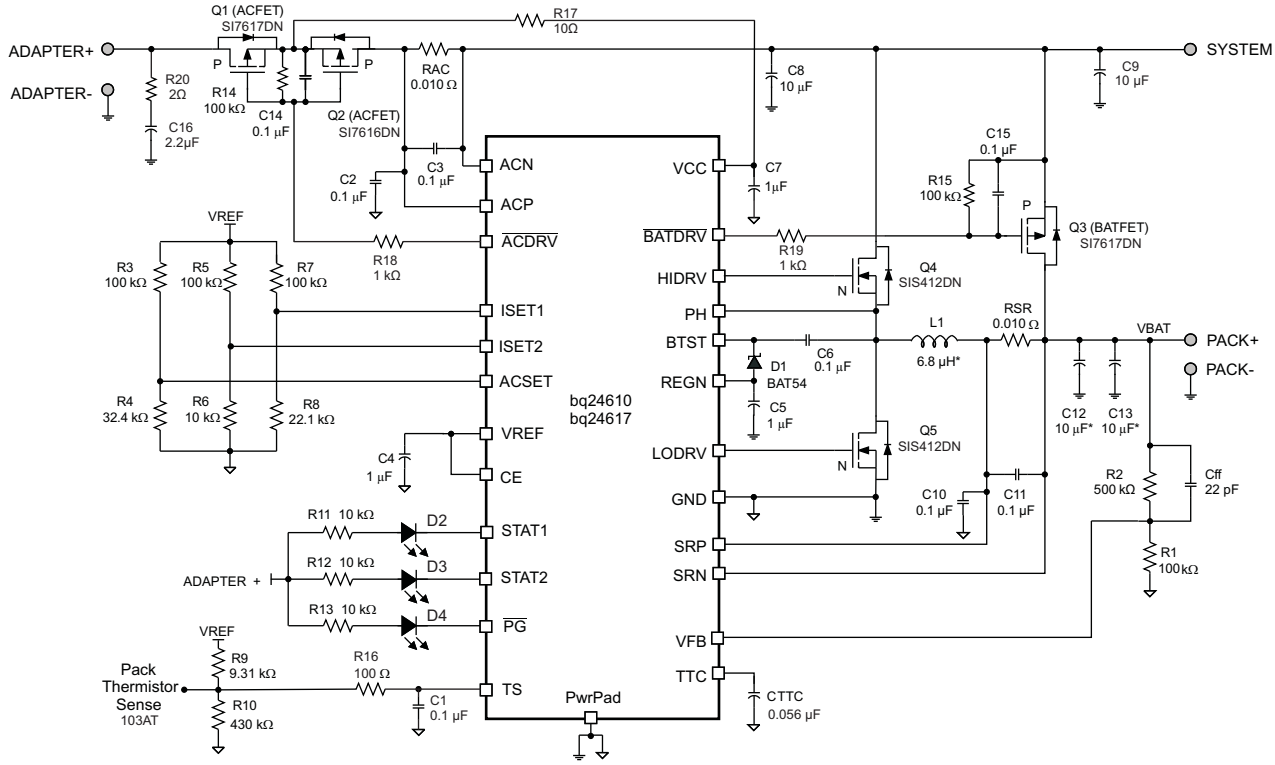
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The bq2461x battery charger is ideal for high current charging (up to 10 A) and can charge battery packs consisting of single cells or multiple cells in series. The bq24610EVM evaluation module is a complete charge module for evaluating the bq2461x. The application curves were taken using the bq24610EVM. Refer to the EVM user's guide (SLUU396) for EVM information.

10.2 Typical Application



VIN = 19 V, 3-cell, $I_{adapter\_limit}$ = 4 A, I_{charge} = 3 A, $I_{pre\text{-}charge}$ = I_{term} = 0.3 A, 5-hour saftey timer

Figure 19. System Schematic

Typical Application (continued)

10.2.1 Design Requirements

For this design example, use the parameters listed in Table 3 as the input parameters.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
AC adapter voltage (VIN)	19 V
AC adapter current limit	4 A
Battery charge voltage (number of cells in series)	12.6 V (3 cells)
Battery charge current (during constant current phase)	3 A
Precharge and termination current	0.3 A
Safety timer	5 hours

10.2.2 Detailed Design Procedure

10.2.2.1 Inductor Selection

The bq2461x has 600-kHz switching frequency to allow the use of small inductor and capacitor values. Inductor saturation current should be higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \quad (12)$$

The inductor ripple current depends on input voltage (V_{IN}), duty cycle ($D = V_{OUT}/V_{IN}$), switching frequency (f_s) and inductance (L):

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1 - D)}{f_S \times L} \quad (13)$$

The maximum inductor ripple current happens with D = 0.5 or close to 0.5. For example, the battery charging voltage range is from 9 V to 12.6 V for a 3-cell battery pack. For 20-V adapter voltage, 10-V battery voltage gives the maximum inductor ripple current. Another example is a 4-cell battery, the battery voltage range is from 12 V to 16.8 V, and 12-V battery voltage gives the maximum inductor ripple current.

Usually inductor ripple is designed in the range of (20%–40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

The bq2461x has cycle-by-cycle charge undercurrent protection (UCP) by monitoring the charging-current sensing resistor to prevent negative inductor current. The typical UCP threshold is 5-mV falling edge corresponding to 0.5-A falling edge for a 10-mΩ charging-current sensing resistor.

10.2.2.2 Input Capacitor

The input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst-case RMS ripple current is half of the charging current when the duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst-case capacitor RMS current I_{CIN} occurs where the duty cycle is closest to 50% and can be estimated by the following equation:

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1-D)} \quad (14)$$

A low-ESR ceramic capacitor such as X7R or X5R is preferred for the input decoupling capacitor and should be placed to the drain of the high-side MOSFET and source of the low-side MOSFET as close as possible. The voltage rating of the capacitor must be higher than the normal input voltage level. A 25-V or higher-rating capacitor is preferred for 20-V input voltage. 10-µF to 20-µF capacitance is suggested for typical of 3-A to 4-A charging current.

10.2.2.3 Output Capacitor

Output capacitor also should have enough ripple-current rating to absorb the output switching ripple current. The output capacitor RMS current I_{COUT} is given:

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (15)$$

The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_o = \frac{1}{8LCf_s^2}\left(V_{BAT} - \frac{V_{BAT}^2}{V_{IN}}\right) \quad (16)$$

At a certain input/output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

The bq2461x has an internal loop compensator. To get good loop stability, the resonant frequency of the output inductor and output capacitor should be designed between 12 kHz and 17 kHz. The preferred ceramic capacitor has a 25-V or higher rating, X7R or X5R for 4-cell application.

10.2.2.4 Power MOSFETs Selection

Two external N-channel MOSFETs are used for a synchronous switching battery charger. The gate drivers are internally integrated into the IC with 6 V of gate drive voltage. 30-V or higher-voltage rating MOSFETs are preferred for 20-V input voltage and 40-V or higher-rating MOSFETs are preferred for 20-V to 28-V input voltage.

Figure-of-merit (FOM) is usually used for selecting the proper MOSFET based on a tradeoff between the conduction loss and switching loss. For a top-side MOSFET, FOM is defined as the product of the MOSFET ON-resistance, $r_{DS(on)}$, and the gate-to-drain charge, Q_{GD}. For a bottom-side MOSFET, FOM is defined as the product of the MOSFET ON-resistance, $r_{DS(on)}$, and the total gate charge, Q_G.

$$FOM_{top} = R_{DS(on)} \times Q_{GD} \qquad FOM_{bottom} = R_{DS(on)} \times Q_G \quad (17)$$

The lower the FOM value, the lower the total power loss. Usually lower $r_{DS(on)}$ has higher cost with the same package size.

The top-side MOSFET loss includes conduction loss and switching loss. It is a function of duty cycle ($D = V_{OUT}/V_{IN}$), charging current (I_{CHG}), the MOSFET ON-resistance $t_{DS(on)}$), input voltage (V_{IN}), switching frequency (f_S), turnon time (t_{on}) and turnoff time (t_{off}):

$$P_{top} = D \times I_{CHG}^2 \times R_{DS(on)} + \frac{1}{2} \times V_{IN} \times I_{CHG} \times \left(t_{on} + t_{off}\right) \times f_S \quad (18)$$

The first item represents the conduction loss. Usually MOSFET $r_{DS(on)}$ increases by 50% with 100ºC junction temperature rise. The second term represents the switching loss. The MOSFET turnon and turnoff times are given by:

$$t_{on} = \frac{Q_{SW}}{I_{on}}, \; t_{off} = \frac{Q_{SW}}{I_{off}}$$

where

- Q_{sw} is the switching charge.
- I_{on} is the turnon gate-driving current.
- I_{off} is the turnoff gate driving current. (19)

If the switching charge is not given in the MOSFET data sheet, it can be estimated by gate-to-drain charge (Q_{GD}) and gate-to-source charge (Q_{GS}):

$$Q_{SW} = Q_{GD} + \frac{1}{2} \times Q_{GS} \quad (20)$$

Total gate-driving current can be estimated by the REGN voltage (V_{REGN}), MOSFET plateau voltage (V_{plt}), total turnon gate resistance (R_{on}), and turnoff gate resistance (R_{off}) of the gate driver:

$$I_{on} = \frac{V_{REGN} - V_{plt}}{R_{on}}, \; I_{off} = \frac{V_{plt}}{R_{off}} \quad (21)$$

The conduction loss of the bottom-side MOSFET is calculated with the following equation when it operates in synchronous CCM:

$$P_{bottom} = (1 - D) \times I_{CHG}^2 \times R_{DS(on)} \quad (22)$$

If the SRP-SRN voltage decreases below 5 mV (the charger is also forced into nonsynchronous mode when the average SRP-SRN voltage is lower than 1.25 mV), the low-side FET is turned off for the remainder of the switching cycle to prevent negative inductor current.

As a result, all the freewheeling current goes through the body diode of the bottom-side MOSFET. The maximum charging current in nonsynchronous mode can be up to 0.9 A (0.5 A typical) for a 10-mΩ charging-current sensing resistor, considering IC tolerance. Choose the bottom-side MOSFET with either an internal Schottky or body diode capable of carrying the maximum nonsynchronous-mode charging current.

MOSFET gate-driver power loss contributes to the dominant losses on the controller IC when the buck converter is switching. Choosing the MOSFET with a small Q_{g_total} reduces the IC power loss to avoid thermal shutdown.

$$P_{ICLoss\_driver} = V_{IN} \cdot Q_{g\_total} \cdot f_s \quad (23)$$

where

- Q_{g_total} is the total gate charge for both upper and lower MOSFETs at 6-V V_{REGN}.

10.2.2.5 Input Filter Design

During adapter hot plug-in, the parasitic inductance and input capacitor from the adapter cable form a second-order system. The voltage spike at the VCC pin may be beyond the IC maximum voltage rating and damage the IC. The input filter must be carefully designed and tested to prevent an overvoltage event on the VCC pin. The ACP/ACN pins must be placed after the input ACFET in order to avoid overvoltage stress on these pins during hot plug-in.

There are several methods for damping or limiting the overvoltage spike during adapter hot plug-in. An electrolytic capacitor with high ESR as an input capacitor can damp the overvoltage spike well below the IC maximum pin voltage rating. A high-current capability TVS Zener diode can also limit the overvoltage level to an IC safe level. However these two solutions may not have low cost or small size.

A cost-effective and small size-solution is shown in Figure 20. The R1 and C1 are composed of a damping RC network to damp the hot plug-in oscillation. As a result, the overvoltage spike is limited to a safe level. D1 is used for reverse voltage protection for the VCC pin (it can be the body diode of input ACFET). C2 is VCC pin decoupling capacitor and it should be placed as close as possible to the VCC pin. R2 and C2 form a damping RC network to further protect the IC from high dv/dt and high-voltage spike. The C2 value should be less than the C1 value so R1 can be dominant over the ESR of C1 to get enough damping effect for hot plug-in. The R1 and R2 packages must be sized to handle in-rush current power loss according to resistor manufacturer's datasheet. The filter component values always must be verified with the real application and minor adjustments may be needed to fit in the real application circuit.

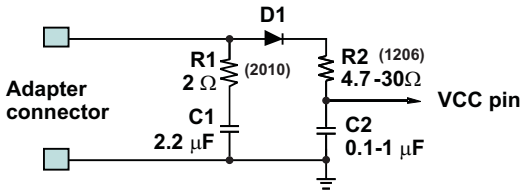


Figure 20. Input Filter

10.2.2.6 Inductor, Capacitor, and Sense Resistor Selection Guidelines

The bq2461x provides internal loop compensation. With this scheme, best stability occurs when the LC resonant frequency, f_o, is approximately 12 kHz to 17 kHz for bq2461x.

Table 4 provides a summary of typical LC components for various charge currents:

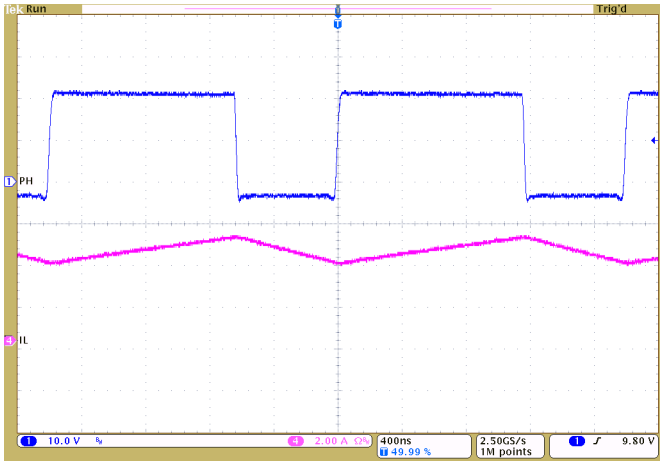
Table 4. Typical Inductor, Capacitor, and Sense Resistor Values as a Function of Charge Current for bq2461x (600-kHz Switching Frequency)

CHARGE CURRENT	2 A	4 A	6 A	8 A	10 A
Output inductor L_O	6.8 µH	6.8 µH	4.7 µH	3.3 µH	3.3 µH
Output capacitor C_O	20 µF	20 µF	30 µF	40 µF	40 µF
Sense resistor	10 mΩ	10 mΩ	10 mΩ	10 mΩ	10 mΩ

Table 5. Component List for Typical System Circuit of Figure 19

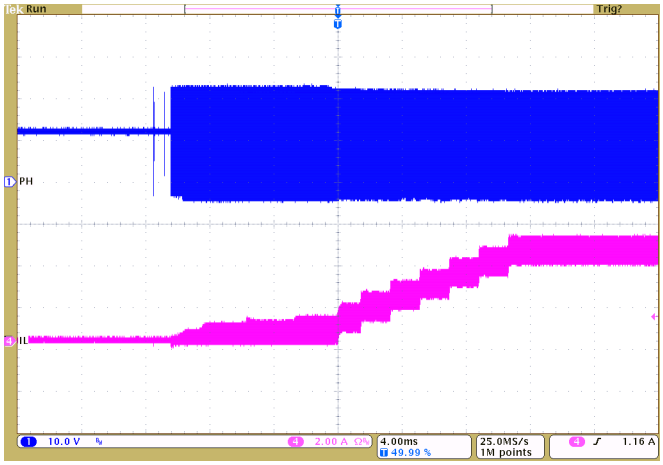
PART DESIGNATOR	QTY	DESCRIPTION
Q1, Q2, Q3	3	P-channel MOSFET, –30 V, –35 A, PowerPAK 1212-8, Vishay-Siliconix, Si7617DN
Q4, Q5	2	N-channel MOSFET, 30 V, 12 A, PowerPAK 1212-8, Vishay-Siliconix, Sis412DN
D1	1	Diode, dual Schottky, 30 V, 200 mA, SOT23, Fairchild, BAT54C
D2, D3, D4	3	LED diode, green, 2.1 V, 20 mA, LTST-C190GKT
R_{AC}, R_{SR}	2	Sense resistor, 10 mΩ, 2010, Vishay-Dale, WSL2010R0100F
L1	1	Inductor, 6.8 µH, 5.5A, Vishay-Dale IHLP2525CZ
C8, C9, C12, C13	4	Capacitor, ceramic, 10 µF, 35 V, 20%, X7R
C4, C5	2	Capacitor, ceramic, 1 µF, 16 V, 10%, X7R
C1, C3, C6, C11	4	Capacitor, ceramic, 0.1 µF, 16 V, 10%, X7R
C2, C10	2	Capacitor, ceramic, 0.1 µF, 50 V, 10%, X7R
C7	1	Capacitor, ceramic, 1 µF, 50 V, 10%, X7R
C14, C15 (Optional)	2	Capacitor, ceramic, 0.1 µF, 50 V, 10%, X7R
C16	1	Capacitor, ceramic, 2.2 µF, 35 V, 10%, X7R
C_{ff}	1	Capacitor, ceramic, 22 pF, 25 V, 10%, X7R
C_{TTC}	1	Capacitor, ceramic, 0.056 µF, 16 V, 5%, X7R
R1, R3, R5, R7	4	Resistor, chip, 100 kΩ, 1/16 W, 0.5%
R2	1	Resistor, chip, 500 kΩ, 1/16 W, 0.5%
R4	1	Resistor, chip, 32.4 kΩ, 1/16 W, 0.5%
R6	1	Resistor, chip, 10 kΩ, 1/16 W, 0.5%
R8	1	Resistor, chip, 22.1 kΩ, 1/16 W, 0.5%
R9	1	Resistor, chip, 9.31 kΩ, 1/16 W, 1%
R10	1	Resistor, chip, 430 kΩ, 1/16 W, 1%
R11, R12, R13, R18, R19	5	Resistor, chip, 10 kΩ, 1/16 W, 5%
R14, R15 (optional)	2	Resistor, chip, 100 kΩ, 1/16 W, 5%
R16	1	Resistor, chip, 100 Ω, 1/16 W, 5%
R17	1	Resistor, chip, 10 Ω, 1/4 W, 5%
R20	1	Resistor, chip, 2 Ω, 1 W, 5%

10.2.3 Application Curves



V_{IN}: 19 V V_{BAT}: 12 V I_{CHG} = 4 A

Figure 21. Continuous Conduction Mode Switching Waveform



V_{IN}: 19 V V_{BAT}: 12 V

Figure 22. Battery Charging Soft Start

11 Power Supply Recommendations

For proper operation of bq2461x, VCC must be from 5 V to 28 V (bq24610) or 24 V (bq24617). To begin charging, VCC must be higher than SRN by at least 500 mV (otherwise, the device will be in sleep mode). TI recommends an input voltage of at least 1.5 V to 2 V higher than the battery voltage, taking into consideration the DC losses in the high-side FET (Rdson), inductor (DCR), and input sense resistor (between ACP and ACN), the body diode drop of RBFET between VCC and input power supply, and battery sense resistor (between SRP and SRN). Power limit for the input supply must be greater than the maximum power required by either the system load or for battery charging (the greater of the two).

12 Layout

12.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high-frequency current-path loop (see Figure 23) is important to prevent electrical and magnetic field radiation and high-frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout of the PCB according to this specific order is essential.

1. Place the input capacitor as close as possible to switching MOSFET supply and ground connections and use the shortest possible copper trace connection. These parts should be placed on the same layer of the PCB instead of on different layers and using vias to make this connection.
2. The IC should be placed close to the switching MOSFET gate terminals to keep the gate-drive signal traces short for a clean MOSFET drive. The IC can be placed on the other side of the PCB from the switching MOSFETs.
3. Place the inductor input terminal as close as possible to the switching MOSFET output terminal. Minimize the copper area of this trace to lower electrical and magnetic field radiation, but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
4. The charging-current sensing resistor should be placed right next to the inductor output. Route the sense leads connected across the sensing resistor back to the IC in same layer, close to each other (minimize loop area) and do not route the sense leads through a high-current path (see Figure 24 for Kelvin connection for best current accuracy). Place the decoupling capacitor on these traces next to the IC.
5. Place the output capacitor next to the sensing resistor output and ground.
6. Output capacitor ground connections must be tied to the same copper that connects to the input capacitor ground before connecting to system ground.
7. Route the analog ground separately from the power ground and use a single ground connection to tie the charger power ground to the charger analog ground. Just beneath the IC, use the copper-pour for analog ground, but avoid power pins to reduce inductive and capacitive noise coupling. Connect analog ground to GND. Connect analog ground and power ground together using the thermal pad as the single ground connection point. Or use a 0-Ω resistor to tie analog ground to power ground (thermal pad should tie to analog ground in this case). A star connection under the thermal pad is highly recommended.
8. It is critical to solder the exposed thermal pad on the back side of the IC package to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
9. Place decoupling capacitors next to the IC pins and make trace connection as short as possible.
10. Size and number of all vias must be enough for a given current path.

See the EVM design (SLUU396) for the recommended component placement with trace and via locations.

For the QFN information, see SCBA017 and SLUA271.

12.2 Layout Example

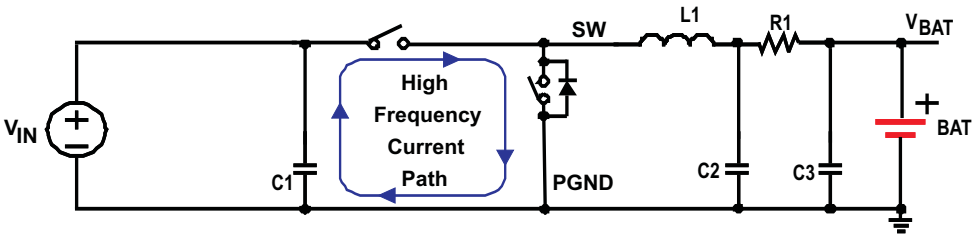


Figure 23. High-Frequency Current Path

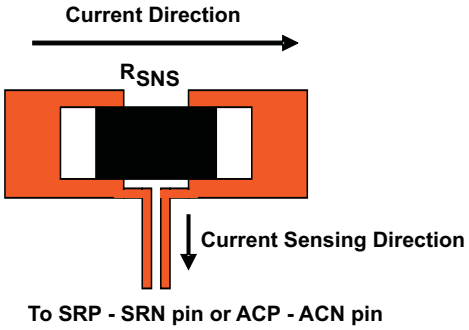


Figure 24. Sensing Resistor PCB Layout

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 6. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
bq24610	Click here	Click here	Click here	Click here	Click here
bq24617	Click here	Click here	Click here	Click here	Click here

13.3 Trademarks

All trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24610RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OAS	Samples
BQ24610RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OAS	Samples
BQ24617RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OFB	Samples
BQ24617RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OFB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

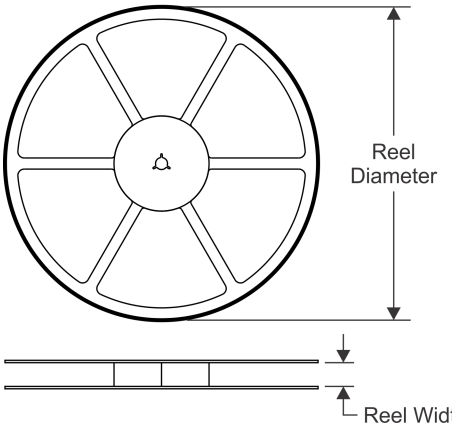
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

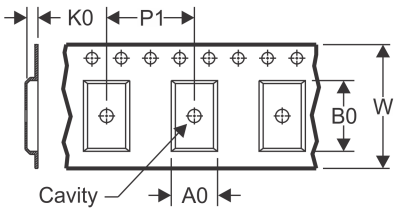
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

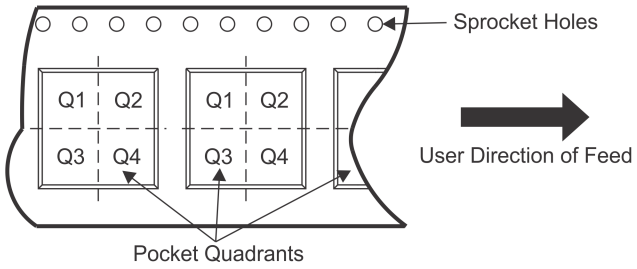


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

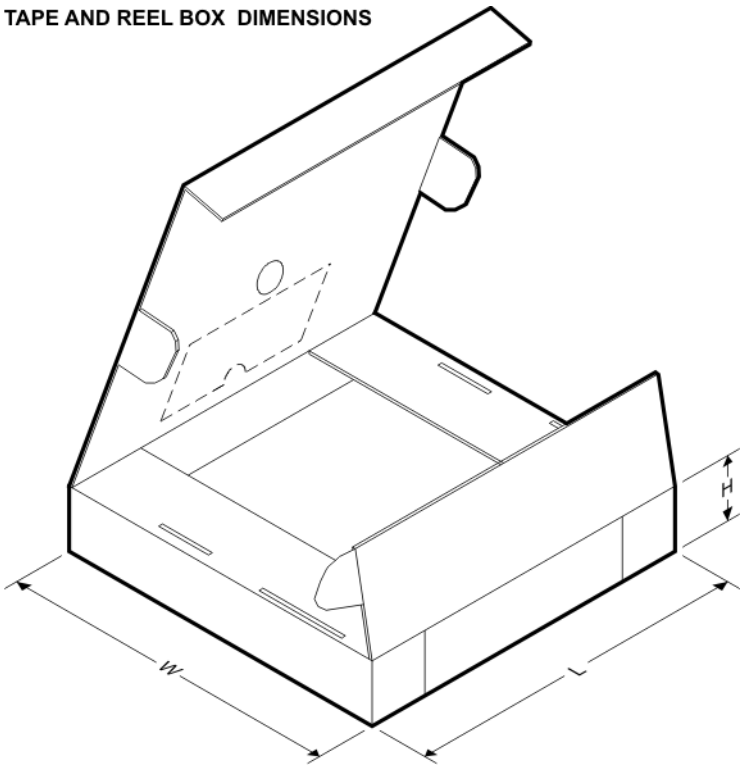
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24610RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24610RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24610RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24610RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24617RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24617RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24617RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ24617RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

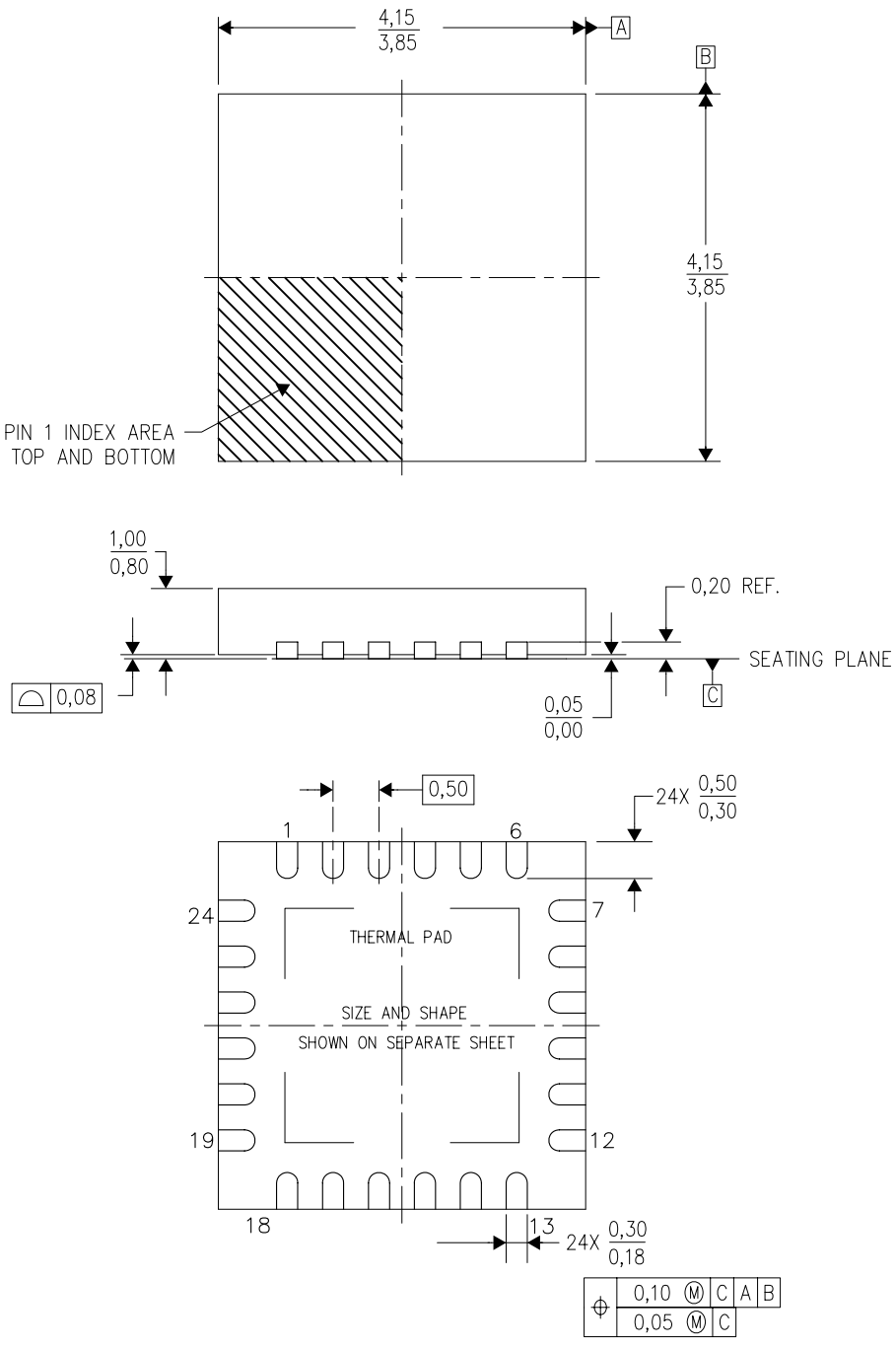
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24610RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ24610RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ24610RGET	VQFN	RGE	24	250	210.0	185.0	35.0
BQ24610RGET	VQFN	RGE	24	250	210.0	185.0	35.0
BQ24617RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ24617RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ24617RGET	VQFN	RGE	24	250	210.0	185.0	35.0
BQ24617RGET	VQFN	RGE	24	250	210.0	185.0	35.0

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

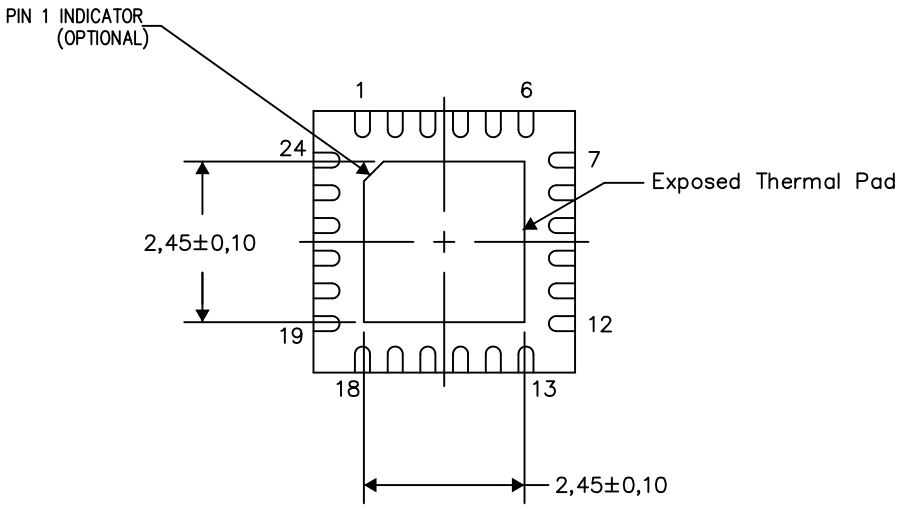
RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



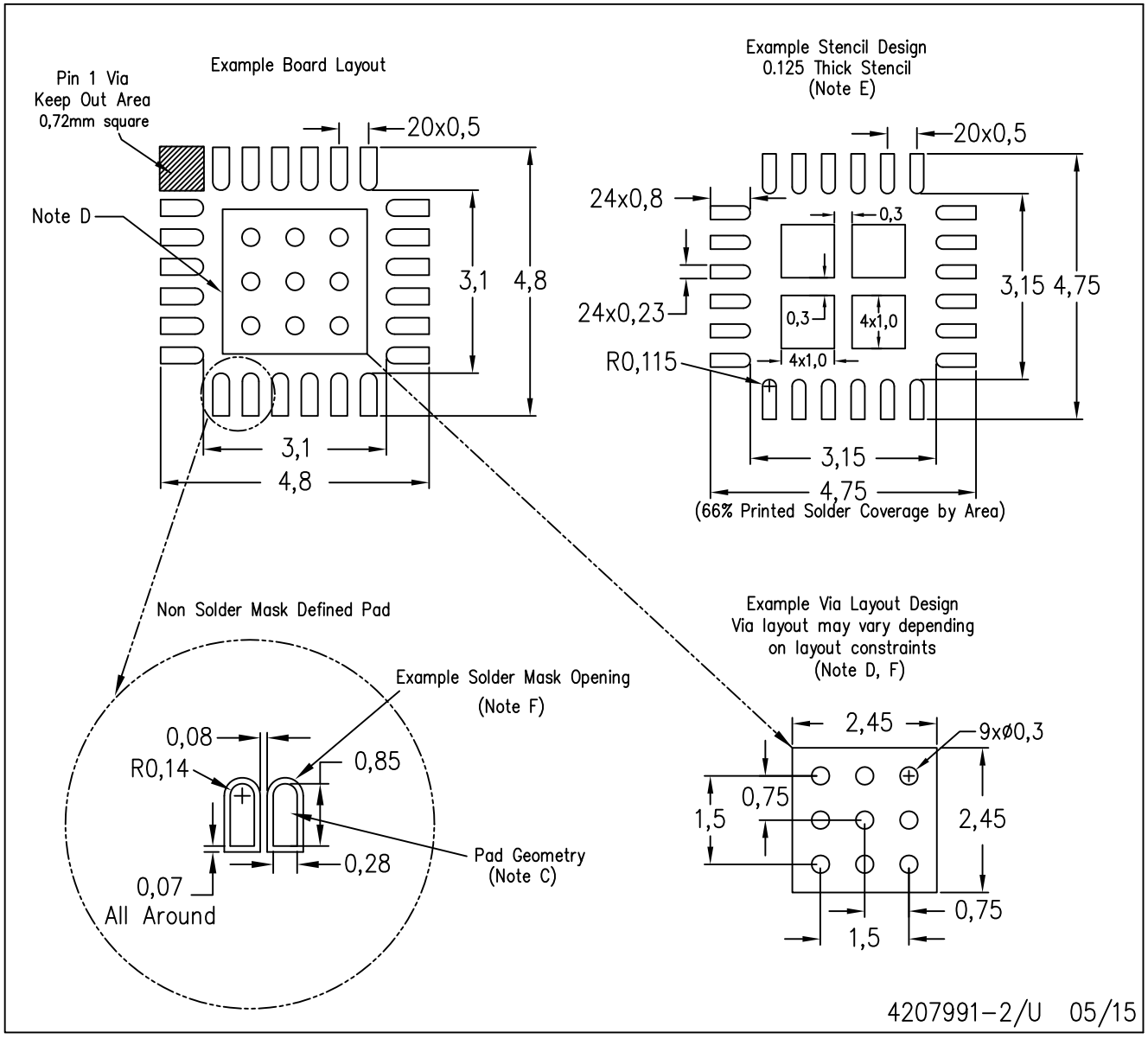
Bottom View

Exposed Thermal Pad Dimensions

4206344–3/AK 08/15

NOTES: A. All linear dimensions are in millimeters

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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