POSITIONING

UBX-M8030

u-blox M8 GNSS chips

Data Sheet

Highlights:

- u-blox M8 position engine featuring excellent accuracy and time-to-first-fix performance
- Concurrent GNSS engine for GPS, GLONASS, BeiDou and QZSS
- Dual-frequency RF front-end
- AssistNow Online, Offline and Autonomous for faster TTFF
- Minimal board space
- Low power consumption
- Minimal e-BOM
- Pin-compatible to UBX-G7020-KT/KA

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Document status information	
Objective Specification	This document contains target values. Revised and supplementary data will be published later.
Advance Information	This document contains data based on early testing. Revised and supplementary data will be published later.
Early Production Information	This document contains data from product verification. Revised and supplementary data may be published later.
Production Information	This document contains the final product specification.

This document applies to the following products:

Name	Type number	ROM/FLASH version	PCN reference
UBX-M8030-KT QFN40 package (Standard grade)	UBX-M8030-KT-A0200A UBX-M8030-KT-B2000A	0.22 / 2.00 2.01	N/A
UBX-M8030-KA QFN40 package (Automotive grade)	UBX-M8030-KA-B2000A	2.01	N/A
UBX-M8030-CT WL-CSP47 (Standard grade)	UBX-M8030-CT-A0200A UBX-M8030-CT-B2000A	0.22 / 2.00 2.01	N/A

Contents

1 Functional description

1.1 Overview

Featuring a single die solution, low power consumption and low costs, the UBX-M8030 GNSS chips are concurrent GNSS (GPS, GLONASS, BeiDou, QZSS and Galileo-ready) positioning chips developed to meet the requirements of an extensive range of applications and end-products. Based on the high performance u-blox M8 position engine, these receivers provide exceptional sensitivity and acquisition times without requiring an external host. u-blox' advanced RF-design and interference suppression enable reliable positioning even in difficult signal conditions.

The dual-frequency RF front-end allows concurrent reception of two GNSS systems, e.g. GPS and GLONASS.

u-blox M8 platform delivers high performance with low power consumption and low costs. An integrated DC/DC converter and intelligent power management are breakthroughs for low-power applications. The minimal BOM requires as few as 8 external components and the small footprint further reduces costs by enabling 2-layer PCB integration. Supporting TCXO or lower price GNSS oscillators further ensures a minimal cost of ownership. LDOs and an LNA are built-in, and costly external memory is not needed. This makes UBX M8030 positioning chips the ideal solutions for cost sensitive applications that don't require firmware update capability. For applications needing firmware update or data logging capabilities, the UBX-M8030 can be connected to an external SQI flash memory.

1.2 Highlights

- u-blox M8 position engine featuring:
  - over 2 million effective correlators
  - down to 1 s acquisition time
  - cold start acquisition sensitivity of -148 dBm and -167 dBm tracking sensitivity
  - up to 5 Hz navigation update rate in multi-GNSS mode and up to 10 Hz in GPS-only mode
- Supports GPS, QZSS, GLONASS, BeiDou and is ready for Galileo
- Supports u-blox' AssistNow Online / AssistNow Offline A-GNSS services and is OMA SUPL 1.0 compliant
- Supports u-blox' AssistNow Autonomous (no connectivity required)
- Supports crystal oscillator and TCXO
- Supports a built-in DC/DC converter and an intelligent, user configurable power management
- Supports data logging
- Standard and automotive grade 5.0 x 5.0 mm^2 QFN40 package with 0.4 mm pitch
- Standard grade 2.99 x 3.21 mm^2 WL-CSP47 package for a minimum footprint
- Minimal eBOM costs and minimum board space (< 30 mm^2) for a complete receiver implementation

1.3 Performance

Parameter	Specification		
Receiver type	72-channel u-blox M8 engine GPS L1C/A SBAS L1C/A QZSS L1C/A GLONASS L1OF Galileo E1B/C[1]		
Time-To-First-Fix[2]		TCXO	Crystal
	Cold start	26 s	27 s
	Hot start	1.5 s	1.5 s
	Aided starts[3]	2 s	4 s
Sensitivity [4]		TCXO	Crystal
	Tracking & Navigation	-167 dBm	-164 dBm
	Reacquisition	-160 dBm	-159 dBm
	Cold start	-148 dBm	-147 dBm
	Hot start	-156 dBm	-156 dBm
Horizontal position accuracy[5]	Default mode (includes SBAS and QZSS)	2.0 m	
Accuracy of time pulse signal	RMS 99%	30 ns 60 ns	
Frequency of time pulse signal		0.25 Hz … 10 MHz	
Max navigation update rate		5 Hz	
Velocity accuracy[6]		0.05 m/s	
Heading accuracy[6]		0.3 degrees	
Operational limits[7]	Dynamics Altitude Velocity	≤ 4 g 50,000 m 500 m/s	

Table 1: u-blox M8030 performance in multi-GNSS mode (using GPS and GLONASS concurrently)

[1] Ready to support Galileo E1B/C when available with a flash firmware update
[2] All satellites at -130 dBm
[3] Dependent on aiding data connection speed and latency
[4] Demonstrated with a good external LNA
[5] CEP, 50%, 24 hours static, -130 dBm, > 6 SVs
[6] 50% @ 30 m/s
[7] Assuming Airborne < 4 g platform

1.4 Block diagram

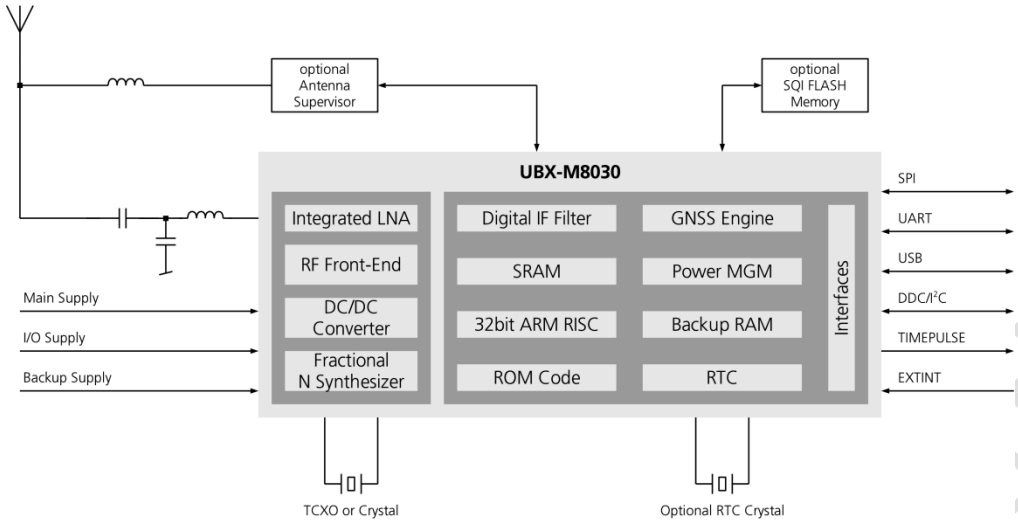


Figure 1: UBX-M8030 block diagram

1.5 GNSS

u-blox M8030 GNSS chips are concurrent GNSS receivers and can receive and track multiple GNSS system (e.g. GPS, GLONASS, BeiDou and QZSS signals). Because of the dual-frequency RF front-end architecture, two of the three signals (GPS L1C/A, GLONASS L1OF and BeiDou B1) can be received and processed concurrently. By default the M8030 receivers are configured for concurrent GPS and GLONASS reception including QZSS and SBAS. If power consumption is a key factor, then the receiver should be configured for single GNSS operation using either GPS or GLONASS or BeiDou and disabling QZSS and SBAS.

☞ Galileo, QZSS and SBAS share the same frequency band as GPS and can always be processed in conjunction with GPS.

1.5.1 GPS

u-blox M8030 receivers are designed to receive and track the L1C/A signals provided at 1575.42 MHz by the Global Positioning System.

☞ GPS can be received and processed concurrently with GLONASS or BeiDou.

1.5.2 GLONASS

The Russian GLONASS satellite system is an alternative system to the US-based Global Positioning System (GPS). u-blox M8030 receivers are designed to receive and track the L1OF signals provided at 1602 MHz + k*562.5 kHz by GLONASS, where k is the satellite's frequency channel number (k = -7, -6,..., 5, 6). The ability to receive and track GLONASS L1OF satellite signals allows design of GLONASS receivers where required by regulations.

☞ GLONASS can be received and processed concurrently with GPS or BeiDou.

1.5.3 BeiDou

u-blox M8030 receivers are designed to receive and track the B1 signals provided at 1561.098 MHz by the BeiDou Navigation Satellite System. The ability to receive and track BeiDou B1 satellite signals in conjunction with GPS results in higher coverage, improved reliability and better accuracy. At the moment BeiDou is not fully operational and provides regional coverage only. Global coverage is scheduled for 2020.

☞ BeiDou can be received and processed concurrently with GPS or GLONASS.

1.5.4 Galileo

u-blox M8030 receivers are ready to receive and track GPS and Galileo signals concurrently, enhancing accuracy and coverage. When Galileo E1B/C signals become available, u-blox M8030 receivers equipped with an SQI flash memory device will be capable of receiving and processing them via a firmware update.

1.5.5 QZSS

The Quasi-Zenith Satellite System (QZSS) is a regional navigation satellite system that transmits additional GPS L1C/A signals for the Pacific region covering Japan and Australia. u-blox M8030 receivers are able to receive and track these signals concurrently with GPS signals, resulting in better availability especially under bad signal conditions, e.g. in urban canyons.

☞ The L1-SAIF signal provided by QZSS is not supported.

1.6 Augmented GNSS

1.6.1 Assisted GNSS (A-GNSS)

Supply of aiding information, such as ephemeris, almanac, rough last position and time, will reduce the time to first fix significantly and improve the acquisition sensitivity. All u-blox M8030 ICs support the u-blox AssistNow Online and AssistNow Offline A-GNSS services, support AssistNow Autonomous, and are OMA SUPL compliant.

1.6.1.1 AssistNow™ Online

With AssistNow Online, an internet-connected GNSS device downloads assistance data from u-blox' AssistNow Online Service at system start-up. AssistNow Online is network-operator independent and globally available. u-blox only sends ephemeris data for those satellites currently visible to the device requesting the data, thus minimizing the amount of data transferred.

Supply of aiding information, such as ephemeris, almanac, rough last position and time, will reduce the time to first fix significantly and improve the acquisition sensitivity.

1.6.1.2 AssistNow™ Offline

With AssistNow Offline, users download u-blox' long-term orbit data from the Internet at their convenience. The orbit data can be stored in the GNSS receiver's SQI flash memory (if available) or in the memory of the application processor. Thus the service requires no connectivity at system start-up and enables a position fix within seconds, even when no network is available. AssistNow Offline offers augmentation for up to 35 days.

1.6.1.3 AssistNow™ Autonomous

AssistNow Autonomous provides aiding information without the need for a host or external network connection. Based on previous broadcast satellite ephemeris data downloaded to and stored by the GNSS receiver, AssistNow Autonomous automatically generates accurate satellite orbital data ("AssistNow Autonomous data") that is usable for future GNSS position fixes. The concept capitalizes on the periodic nature of GNSS satellites: their position in the sky is basically repeated every 24 hours. By capturing strategic ephemeris data at specific times of the day, the receiver can predict accurate satellite ephemeris for up to five days after initial reception. If using AssistNow Autonomous, the use of an SQI flash memory is highly recommended.

u-blox' AssistNow Autonomous benefits are:

- Faster fix in situations where GNSS satellite signals are weak
- No connectivity required
- Compatible with AssistNow Online and Offline (can work stand-alone, or in tandem with these services)
- No integration effort; calculations are done in the background, transparent to the user.

☞ For more details see the *u-blox M8 Receiver Description Including Protocol Specification* [2]

1.6.2 Augmentation Systems

1.6.2.1 Satellite-Based Augmentation System (SBAS)

u-blox M8030 receivers support SBAS. These systems supplement GPS data with additional regional or wide area GPS augmentation data. The system broadcasts augmentation data via satellite and this information can be used by GNSS receivers to improve the resulting precision. SBAS satellites can be used as additional satellites for ranging (navigation), further enhancing precision and availability. The following SBAS types are supported with u-blox M8: WAAS, EGNOS and MSAS.

1.6.2.2 Differential GPS (D-GPS)

u-blox M8030 receivers support Differential-GPS data according RTCM 10402.3: "RECOMMENDED STANDARDS FOR DIFFERENTIAL GNSS". The use of Differential-GPS data improves GPS position accuracy. RTCM cannot be used together with SBAS. The RTCM implementation supports the following RTCM 2.3 messages:

Message Type	Description
1	Differential GPS Corrections
2	Delta Differential GPS Corrections
3	GPS Reference Station Parameters
9	GPS Partial Correction Set

Table 2: Supported RTCM 2.3 messages

☞ For more details see the *u-blox M8 Receiver Description Including Protocol Specification* [2]

1.7 Data logging

u-blox M8030 receivers can be used in data logging applications. The data logging feature enables continuous storage of position, velocity and time information to an external SQI flash memory. The information can be downloaded from the receiver later for further analysis or for conversion to a mapping tool. For more information see the *u-blox M8 Receiver Description Including Protocol Specification* [2].

1.8 Protocols and interfaces

Protocol	Type
NMEA 0183 V2.3 and V4.x	Input/output, ASCII
UBX	Input/output, binary, u-blox proprietary
RTCM 2.3	Input, messages 1, 2, 3, 9

Table 4: Available Protocols

All protocols are available on UART, USB, DDC (I^2C compliant) and SPI. For specification of the various protocols see the *u-blox M8 Receiver Description Including Protocol Specification* [2].

2 RF subsystem

The RF subsystem implements a dual-frequency architecture. The input signal is a 100 MHz wide portion of the spectrum centered at about 1575 MHz. The received GNSS signals are amplified by a single-ended low-noise amplifier, and then fed to a gain block, which offers further amplification, thus reducing the noise figure requirements for the first mixing stage. The gain block also provides a single-ended to differential conversion. After the first down-conversion the multi-GNSS signals are split up into two channels. Both channels are fed to a complex mixing scheme, which provides a second down-conversion to separate signals from different GNSS. Afterwards the I and Q signals of both channels are low-pass filtered and amplified by separate Programmable Gain Amplifiers (PGA). The I and Q signals of both channels are then sent to the baseband section, where A/D conversion, signal processing and final image rejection takes place.

2.1 Low noise amplifier

The low noise amplifier (LNA) makes use of a single stage configuration and requires external matching to function satisfactorily. For improved performance an external LNA should be added. Depending on the application it might be useful to consider additional external filtering to improve robustness against interference.

2.2 Gain block

A single stage differential amplifier follows the LNA providing further amplification and conversion from single-ended to differential signaling.

2.3 First Mixer and signal splitting

u-blox M8030 receivers make use of a passive IQ mixer topology to first convert the multi-GNSS signals to an intermediate frequency. At this stage the signals are split into two similar IF channels. Both channels are further amplified with each fed to a mixer to select a particular GNSS signal band. For single GNSS operation, only one channel is active; the other channel is turned off to reduce power consumption.

2.4 Second Mixer and low-pass filter

A complex mixing scheme is used to shift signals from the selected GNSS center frequency down to an low intermediate frequency close to a few MHz.

The subsequent low-pass filter removes any high-frequency mixing products from the desired signal. Their cut-off frequency is adjustable to compensate IC for any process variation.

2.5 Programmable gain amplifier

The programmable gain amplifiers (PGA) are used to provide the ADCs with appropriate input levels. They make use of a four stage approach consisting of three variable gain stages. The PGA gain is adjusted by firmware based on the ADC output signal values, providing an automatic gain control (AGC) for the receiver.

2.6 ADC

Two 5-bit ADCs are used for A/D conversion. The output signaling of the ADCs are differential I and Q signals, which are processed in the following baseband subsystem.

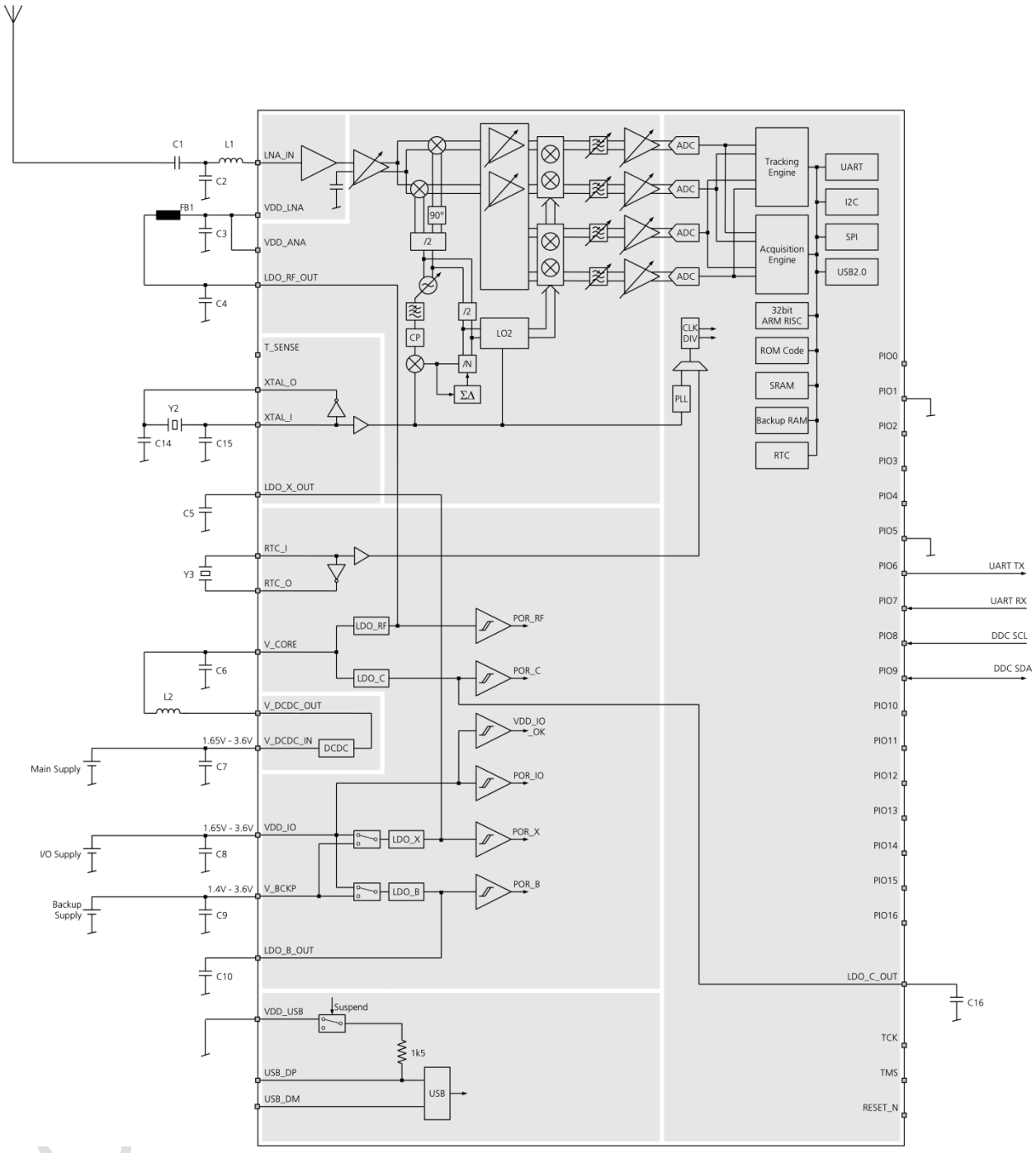


Figure 2: UBX-M8030 RF and baseband subsystems

3 Baseband subsystem

The baseband subsystem integrates a Cortex-M3™ CPU and all the memory required for embedded firmware execution. Specific hardware required for signal acquisition and tracking and a wide selection of interfaces are provided. Analog functional blocks such as PLL, A/D converters and Power Management Unit (PMU) are fully integrated. The u-blox M8 embedded firmware provides all the algorithms needed to calculate navigation data output.

Figure 3 shows the block diagram for the baseband section. Selected functional blocks are described in the following sections.

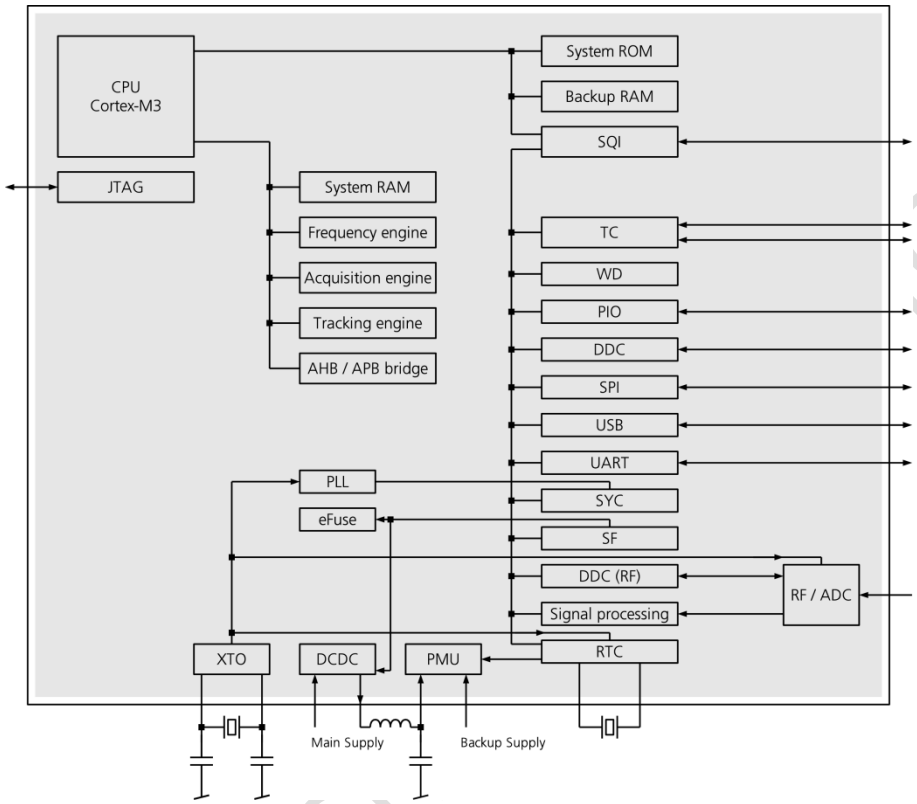


Figure 3: UBX-M8030 baseband subsystem

3.1 GNSS processing engines

The acquisition and tracking engines are the main hardware components that perform the GNSS signal processing. Both engines can remove residual carrier (Doppler) offset and perform correlation with GNSS codes.

Since acquisition and tracking functions are completely separate, the acquisition engine can be shut down completely when it's not needed. Additionally, even if all channels of the tracking engine are fully loaded, the full power of the acquisition engine is at the disposal of the firmware.

Both engines feature dedicated memory blocks in order to keep silicon area and power consumption to a minimum. State-of-the-art clock management allow adapting the power consumption to the actual processing state of the firmware and its corresponding hardware needs.

Embedded firmware employs various strategies in order to make the best use of the two engines. The user may tune the configuration for a particular application by changing the settings.

3.2 Interfaces

A number of interfaces are available either for data communication or memory access. The embedded firmware uses these interfaces according to their respective protocol specifications. For specific applications, the firmware also supports the connection of peripheral devices, such as external memories or sensors, to some of the interfaces.

☞ The digital I/Os of the baseband part are supplied with VDD_IO from the host system. The wide range of VDD_IO allows seamless interfacing to standard logic voltage levels independently of the baseband supply voltage level. However, in many applications VDD_IO will be simply connected to the main supply voltage. Without supplying VDD_IO, the system will be kept in reset state.

3.2.1 UART

The UBX-M8030 makes use of a UART interface, which can be used for communication with a host. It supports configurable baud rates. For supported transfer rates see the *u-blox M8 Receiver Description Including Protocol Specification* [2]. By default, PIO6 and PIO7 are used for the UART interface, but they can be mapped to PIO15 and PIO16 in case of conflict with the SPI interface (see section 3.2.3).

3.2.2 USB

A USB interface, which is compatible to USB version 2.0 FS (Full Speed, 12 Mbit/s), can be used for communication as an alternative to the UART. The pull-up resistor on pin USB_DP is integrated to signal a full-speed device to the host. The VDD_USB pin supplies the USB interface. The USB-M8030 (TID: 40001548) is listed on the USB-IF Integrator's List.

3.2.3 SPI

The SPI interface is designed to allow communication to a host CPU. The interface can be operated in slave mode only. The maximum transfer rate using SPI is 1 Mbit/s and the maximum SPI clock frequency is 5.5 MHz. Note that SPI is not available in the default configuration, because its pins are shared with the UART and DDC interfaces. The SPI interface can be enabled by connecting PIO10 to ground (see section 5.1.1). In this case the DDC interface for data communication is no longer available. The UART interface can be mapped to PIO15 and PIO16.

3.2.4 Display Data Channel (DDC)

An I^2C compliant DDC interface is available for communication with an external host CPU. The interface can be operated in slave mode only. The DDC protocol and electrical interface are fully compatible with Fast-Mode of the I^2C industry standard. Since the maximum SCL clock frequency is 400 kHz, the maximum transfer rate is 400 kbit/s.

3.2.5 Serial Quad Interface (SQI)

The SQI is used to connect the UBX-M8030 with an external flash memory. The flash memory is required for firmware updates, data logging and future product variations. In addition, it can be used to store configurations and to save AssistNow Offline data.

☞ For more information see the *UBX-M8030 Hardware Integration Manual* [1]

3.2.6 JTAG

The JTAG interface can be used for boundary scan testing. The UBX-M8030 provides two dedicated pins and two PIOs for this purpose. Both pins and PIOs are listed in Table 13.

☞ For more information see the *UBX-M8030 Hardware Integration Manual* [1]

3.3 Peripheral Input Output (PIO)

The PIO block has two basic functions.

- It provides I/O pins for the interfaces. The configuration of the pins is determined by the dedicated interface.
- It allows the use of I/O pins as general-purpose I/O.

PIO #	Default Function	I/O	Remarks	Alternative Functions
0	SQI_D0 or CFG_FFU2	I/O I	Data line 0 to external SQI flash memory or reserved configuration pin. If PIO5 is connected to GND (no SQI flash memory is used), it acts as a reserved configuration pin.	
1	SQI_D1 or CFG_DCDC	I/O I	Data line 1 to external SQI flash memory or configuration pin. If PIO5 is connected to GND (no SQI flash memory is used), it acts as a configuration pin to enable DC/DC converter.	
2	SQI_D2 or CFG_OSC3	I/O I	Data line 2 to external SQI flash memory or configuration pin. If PIO5 is connected to GND (no SQI flash memory is used), it acts as an oscillator configuration pin.	
3	SQI_D3 or CFG_OSC2	I/O I	Data line 3 to external SQI flash memory or configuration pin. If PIO5 is connected to GND (no SQI flash memory is used), it acts as an oscillator configuration pin.	
4	SQI_CLK or CFG_OSC1	O I	Clock for external SQI flash memory or configuration pin. If PIO5 is connected to GND (no SQI flash memory is used), it acts as an oscillator configuration pin.	
5	SQI_CS or CONFIG_SEL	O I	Chip select for external SQI flash memory or configuration enable pin. If low at startup (no SQI flash memory is used), then PIO0 to PIO4 become configuration pins.	
6	TX or MISO	O O	UART TX (if PIO10 is high or left open at startup) SPI MISO (if PIO10 is low at startup)	TX-ready
7	RX or MOSI	I I	UART RX (if PIO10 is high or left open at startup) SPI MOSI (if PIO10 is low at startup)	
8	SCL or SCK	I I	DDC clock (if PIO10 is high or left open at startup) SPI clock (if PIO10 is low at startup)	
9	SDA or CS_N	I/O I	DDC data (if PIO10 is high or left open at startup) SPI chip select (if PIO10 is low at startup)	
10	D_SEL	I	Communication interface selection pin. Selects the communication interface available on PIO6 to PIO9.	
11	TIMEPULSE1	O	Time pulse 1 output, 1pps	
12	SAFEBOOT_N	I	If low at startup, the receiver will start in Safe Boot Mode. Used in production for setting the Low Level Configuration, programming the SQI flash memory and testing purposes.	TIMEPULSE2
13	-	I	No function by default, leave open.	EXTINT0, TX-ready
14	-	I	No function by default, leave open.	EXTINT1, ANT_DET, TX-ready
15	ANT_OK	I	Antenna status of antenna supervisor.	ANT_SHORT_N, UART_TX, TX-ready
16	ANT_OFF	O	Antenna power control of antenna supervisor.	UART_RX, TX-ready

Table 5: Default functions of PIOs

☞ For more information see the *UBX-M8030 Hardware Integration Manual* [1]

3.4 Watchdog (WD)

u-blox M8 includes a watchdog timer, that prevents system-lockups caused if the software gets trapped in a deadlock. During normal operation, the firmware resets the watchdog's internal counter at regular intervals before timer overflow occurs.

3.5 Clock generation

3.5.1 Crystal and TCXO oscillator

The oscillator circuit supplies the reference frequency for the RF and the Baseband PLL. The clock frequency for UBX-M8030 is 26 MHz. One can choose an external crystal as frequency reference or an external TCXO for frequency generation. In the latter case the internal circuit is used as a buffer/driver amplifier for the TCXO. A TCXO provides accelerated weak signal acquisition, which enables faster start and reacquisition times. The crystal oscillator provides good performance in a cost effective solution and reduced power consumption compared to the TCXO. With UBX-M8030 a "single crystal" operation is introduced, where the 26 MHz crystal oscillator can also be used to provide a frequency reference to the RTC without using an additional crystal for the RTC. For this reason the clocking oscillator is supplied internally by a separate power domain called LDO_X, which can be powered via VDD_IO or V_BCKP.

3.5.2 PLL

The fully integrated, low-power, fractional sigma-delta PLL generates the system frequency from a wide range of reference frequencies supplied by crystal or TCXO oscillators. The PLL output frequency is programmable; maximum frequency is 120 MHz for the system clock and 96 MHz for the SQI clock. When a USB device is connected, the PLL also provides the USB interface with the required 48 MHz clock.

3.5.3 Real-Time Clock (RTC)

The RTC is driven internally by a 32768 Hz oscillator, which makes use of an external RTC crystal. The signal for the RTC can also be derived from the 26 MHz crystal oscillator or can be shared from another RTC oscillator used within the application. If the main supply voltage fails and a battery is connected to V_BCKP, parts of the baseband section switch off, but the RTC still runs providing a timing reference for the receiver. This operating mode is called Hardware Backup Mode, which enables all relevant data to be saved in the backup RAM to allow a subsequent hot or warm start.

The RTC crystal is optional, but it is required in Power Save Mode for optimized power consumption. In these cases, the current time is maintained in the RTC and ephemeris and other last known data is kept in the backup RAM. In A-GNSS based systems, the RTC is not required when coarse or fine time information is available from the network.

☞ If backup RAM and RTC are not used, the backup battery backup battery is not needed and V_BCKP should be connected to VDD_IO.

3.6 Power Management Unit (PMU)

The PMU provides four power domains that are internally generated by LDOs and supervised by several voltage monitors:

1. Backup - the backup domain runs the RTC section and the backup memory. The backup domain provides three modes:
   - Run mode: when the voltage level at VDD_IO allows proper system operation.
   - SW backup mode: if the voltage at VDD_IO is still OK, but the LDOs for the other power domains are switched off by software command.
   - HW backup mode: when the voltage at VDD_IO fails, but an external battery is connected to V_BCKP. In this case the PMU will automatically switch off the remaining blocks but keeps RTC and backup memory alive.
2. Core - the core domain is the main power domain for the baseband subsystem. Its LDO_C can be connected directly to a main power supply via V_CORE or supplied by the built-in DC/DC converter.
3. RF - the RF domain supplies the RF subsystem. The LDO of the RF domain is called LDO_RF. Its input is internally connected to the input of LDO_C of the core domain (see Figure 2).
4. Clock - the clock domain supplies the oscillator. Its LDO_X may be supplied by either the main power supply connected to VDD_IO or an external backup battery connected to V_BCKP (see section 3.6.1).

3.6.1 DC/DC converter

u-blox M8030 chips integrate a DC/DC converter, allowing reduced power consumption especially when using a main supply voltage above 2.5 V. To use the DC/DC converter the main power supply must be connected to V_DCDC_IN and a capacitor and an inductor must be added to connect V_DCDC_OUT to V_CORE as shown in Figure 2. If a converter is not used, connect V_DCDC_IN/V_DCDC_OUT to V_CORE.

☞ For more information see the *UBX-M8030 Hardware Integration Manual* [1]

3.7 Memory

3.7.1 Backup RAM

u-blox M8030 receivers include an internal backup RAM, which enables all relevant data to be saved in case of a power failure. Furthermore, it can be used to store configuration data.

3.7.2 eFuse memory

u-blox M8030 receivers make use of an integrated eFuse memory, which permanently saves configuration settings. The eFuse memory can also be used to store the low level configuration.

4 Operating modes

u-blox M8030 receivers offers a power-optimized architecture with built-in autonomous power saving functions to minimize power consumption at any given time. Furthermore, the receiver can operate in two operating modes:

- Continuous Mode for best GNSS performance
- Power Save Mode to optimize power consumption

In addition, a high efficiency DC/DC converter is integrated to allow low power consumption even for higher main supply voltages.

4.1 Continuous Mode

Continuous Mode uses the acquisition engine at full performance, resulting in the shortest possible TTFF and the highest sensitivity. It searches for all possible satellites until the almanac is completely downloaded. The receiver then switches to the tracking engine to lower the power consumption.

Thus, a lower tracking current consumption level will be achieved when:

- A valid GNSS position is obtained
- The entire almanac has been downloaded
- The ephemeris for each satellite in view is valid

4.2 Power Save Mode

For power sensitive applications, u-blox M8030 receivers provide a Power Save Mode for reduced power consumption.

Power Save Mode uses two dedicated operations called ON/OFF and Cyclic tracking, that reduce average current consumption in different ways to match the needs of the specific application. These operations can be set by using a specific ubx message.

☞ For more information about power management strategies, see the *u-blox M8 Receiver Description Including Protocol Specification* [2].

☞ For ROM/FLASH firmware version 2.00 and 2.01 the Power Save Mode is only available when using GPS-only mode.

☞ For a description of power management strategies, see the *u-blox 6 Receiver Description Including Protocol Specification* [2].

5 System configuration

u-blox M8030 receivers must be configured to specify the I/O communication and the interactions with external hardware. The general configuration procedure for the UBX-M8030 is as follows:

1. **Communication Interface Configuration** - The first step is always to select the interface for communication to the host CPU by configuring the PIO10 (D_SEL) input.
2. **Configuration pins** – If no external SQI flash memory is connected to the chip, some of the Low Level Configuration settings can be set by setting the configuration pins PIO0 to PIO5. The rest of the Low Level Current Configuration can be changed after start-up or anytime during normal operation by sending a UBX-CFG-OTP message to the receiver.
3. **Low Level Configuration** – If an external SQI flash is connected, the receiver must initially start up in Safe Boot Mode for setting the Low Level Configuration in the eFuse memory. This ensures that subsequent starts-ups of the UBX-M8030 chip will work properly.

5.1 Configuring the communication interface

5.1.1 PIO10 (D_SEL)

At start-up, the PIO10 pin determines which data interfaces are used for communication. If PIO10 is set to logical "1" or is not connected, UART and DDC become available. If PIO10 is set to logical "0", i.e. connected to GND, the UBX-M8030 can communicate to a host via SPI.

PIO #	PIO10="1" (left open)	PIO10="0" (connected to GND)
6	UART TX	SPI MISO
7	UART RX	SPI MOSI
8	DDC SCL	SPI CLK
9	DDC SDA	SPI CS_N

Table 6: Data interface selection by PIO10

☞ If PIO10 is connected to ground, then the UART interface can still be available when remapped to PIO15 and PIO16 (see the *u-blox M8 Receiver Description Including Protocol Specification* [2]).

5.2 Configuration pins

If no flash memory is used, PIO5 can be set to logical "0". Additional PIOs then become configuration (CONFIG) pins for configuring dedicated hardware settings at system startup.

☞ All PIOs include an internal pull-up resistor.

☞ PIO0 is a reserved pin and must not be connected.

5.2.1 PIO5 (CONFIG_SEL)

If PIO5 is set to logical "0", then PIO0 to PIO4 become available as configuration pins.

PIO1	Configuration	Remarks
1	DC/DC converter disabled	
0	DC/DC converter enabled	Requires additional circuitry

Table 7: PIO to enable the DC/DC converter

PIO2	PIO3	PIO4	Configuration	Remarks
1	1	1	LDO_X_OUT = 1.5 V	When using a crystal with a 19 pF load
0	1	1	Reserved	
1	0	1	LDO_X_OUT = 1.5 V	When using a crystal with a 7 pF load
0	0	1	Reserved	
1	1	0	LDO_X_OUT = 3.0 V	LDO_X_OUT is used to supply a 3.0 V TCXO.
0	1	0	LDO_X_OUT = 1.9 V	LDO_X_OUT is used to supply a 1.8 V TCXO.
1	0	0	LDO_X_OUT = 2.6 V	LDO_X_OUT should be used to enable a 3.0 V TCXO. The TCXO has to be supplied by VDD_IO.
0	0	0	LDO_X_OUT = 1.6 V	LDO_X_OUT should be used to enable a 1.8 V TCXO. The TCXO has to be supplied by VDD_IO.

Table 8: PIOs to configure the oscillator

5.3 Low Level Configuration

u-blox M8030 receivers make use of eFuse technology, which is used to set the Low Level Configuration, permanently changing the default hardware configuration or remapping the PIOs. The default function of the PIOs can be seen in Table 5.

☞ For more information about Low Level Configuration, see the *u-blox M8 Receiver Description Including Protocol Specification* [2] or the *UBX-M8030 Hardware Integration Manual* [1].

5.4 Safe Boot Mode

If PIO12 is set to logical "0" at startup, the receiver enters Safe Boot Mode. In this mode the receiver does not calculate positioning data, but is in a defined state that allows such actions as changing the Low Level Configuration by eFuse, programming the flash memory in production, or recovering a corrupted flash memory.

☞ For more information about using Safe Boot Mode see the *UBX-M8030 Hardware Integration Manual* [1].

5.5 System reset

The UBX-M8030 chips provide a RESET_N pin to restore the system to its default state. To trigger a reset, the dedicated pin has to be shorted to ground for at least 10 ms. The RESET_N pin is a state-triggered input using an internal 10 kΩ pull-up-resistor. In normal operation the RESET_N has to be left open.

☞ A system reset won't affect the temporary GNSS data saved in the backup memory

6 Pin definition

6.1 Pin assignment

Section 6.1.1 / 6.1.2 shows the ball/pin assignments. Most PIOs are configurable and have shared functions. Use special care when designing with these pins since the overall function of the device can be affected. The default configuration of the PIOs is listed in Table 5.

☞ For more information see the *u-blox M8 Receiver Description Including Protocol Specification* [2].

6.1.1 WL-CSP47 (UBX-M8030-CT)

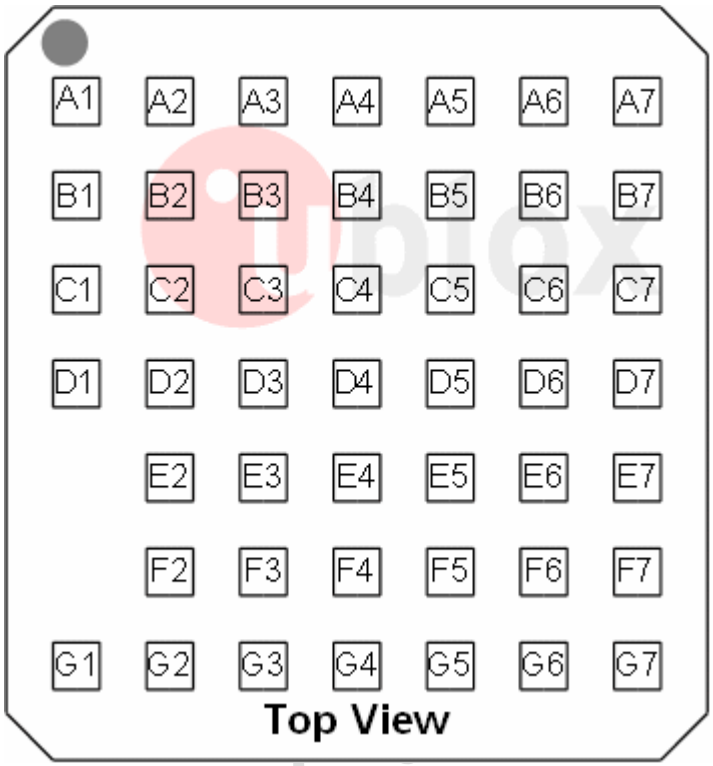


Figure 4: UBX-M8030-CT top view

	1	2	3	4	5	6	7
A	V_BCKP	RTC_O	RTC_I	PIO6	PIO7	V_DCDC_IN	V_DCDC_OUT
B	VDD_IO	VDD_USB	USB_DP	TCK	RESET_N	T_SENSE	V_CORE
C	LDO_B_OUT	USB_DM	PIO14	PIO13	TMS	GND	LDO_C_OUT
D	LDO_X_OUT	XTAL_O	GND	GND	GND	PIO3	PIO2
E	-	XTAL_I	GND	PIO15	PIO10	PIO5	PIO4
F	-	GND	VDD_ANA	PIO16	PIO12	PIO11	PIO0
G	LNA_IN	GND	VDD_LNA	LDO_RF_OUT	PIO9	PIO8	PIO1

Table 9: UBX-M8030-CT ball assignment

6.1.2 QFN40 (UBX-M8030-KT, UBX-M8030-KA)

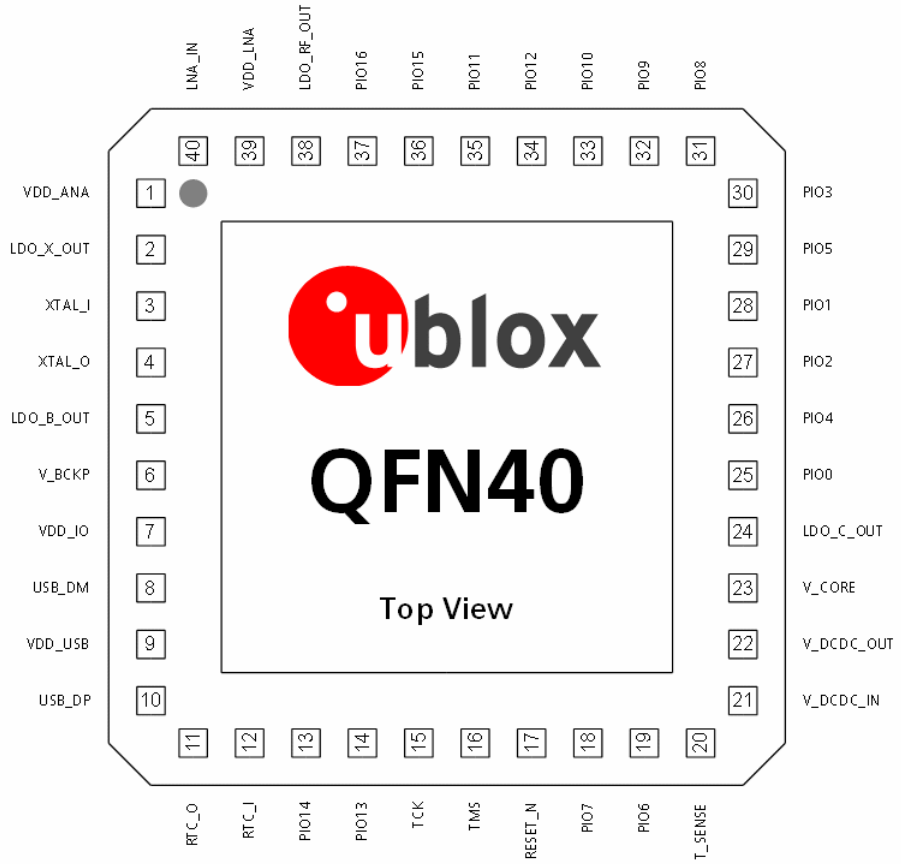


Figure 5: UBX-M8030-KT/KA pin assignment

☞ For multiple function PIOs, select the specific signal by sending the specific configuration message or e-fusing.

6.2 Pin description

Name	Ball WL-CSP47	Pin QFN40	Power Domain	I/O Reset	I/O Core off	Description
V_DCDC_IN	A7	21	DC/DC	-	-	DC/DC Input
V_DCDC_OUT	A6	22	DC/DC	-	-	DC/DC Output
V_CORE	B7	23	Core	-	-	Main Core Supply
V_BCKP	A1	6	Backup	-	-	Backup Cell Supply
VDD_IO	B1	7	IO	-	-	I/O Ring Power Supply
VDD_USB	B2	9	USB	-	-	USB Power Supply
VDD_ANA	F3	1	RF	-	-	Analog Power Supply
VDD_LNA	G3	39	RF/LNA	-	-	LNA Power Supply
LDO_RF_OUT	G4	38	RF	-	-	RF Power Output (Capacitor to ground is required!)
LDO_C_OUT	C7	24	Core	-	-	Core Power Output (Capacitor to ground is required!)
LDO_B_OUT	C1	5	Backup	-	-	Backup Power Output (Capacitor to ground is required!)
LDO_X_OUT	D1	2	Clock	-	-	Clock Power Output (Capacitor to ground is required!)
GND	C6	-	DC/DC	-	-	Ground (VSS_DCDC)
GND	D3	-	CORE	-	-	Ground (VSS_DIGITAL)
GND	E3	-	RF	-	-	Ground (VSS_ANALOG)
GND	D4	-	Core	-	-	Ground (VSS_DIGITAL)
GND	D5	-	Core	-	-	Ground (VSS_DIGITAL)
GND	F2	-	RF	-	-	Ground (VSUB_LNA)
GND	G2	-	RF	-	-	Ground (VSS_LNA)

Table 10: Power Management

Name	Ball WL-CSP47	Pin QFN40	Power Domain	I/O Reset	I/O Pwr off	Description
LNA_IN	G1	40	RF/LNA	Input	Input	LNA Input (LNA requires an external input matching!)
XTAL_I	E2	3	Clock	Input	Input	XTO Input
XTAL_O	D2	4	Clock	Output	Output	XTO Output
RTC_I	A3	12	Backup	Input	Input	RTC Input
RTC_O	A2	11	Backup	Output	Output	RTC Output
T_SENSE	B6	20	Clock	Input	Input	ADC Input (This pin is not supported with FW2.00 and FW 2.01)
RESET_N	B5	17	IO	-	Input	System Reset

Table 11: System

Name	Ball WL-CSP47	Pin QFN40	Power Domain	I/O Reset	I/O Pwr off	Description
VDD_USB	B2	9	USB	-	-	USB Power Supply (see table 9)
USB_DP	B3	10	USB	Input	Input	I/O Differential USB D+
USB_DM	C2	8	USB	Input	Input	I/O Differential USB D-

Table 12: USB

Name	Ball WL-CSP47	Pin QFN40	Power Domain	I/O Reset	I/O Pwr off	Description
TCK	B4	15	IO	Input Pull-down	Input Pull-down	JTAG Test Clock Input
TMS	C5	16	IO	Input Pull-up	Input Pull-up	JTAG Test Mode Select
PIO13 / TDI	C4	14	IO	Input Pull-up	Input Pull-up	JTAG Test Data Input (TDI function is not provided by default. The PIO has to be remapped!)
PIO14 / TDO	C3	13	IO	Input Pull-up	Input Pull-up	JTAG Test Data Output (TDO function is not provided by default. The PIO has to be remapped!)

Table 13: JTAG

Name	Ball WL-CSP47	Pin QFN40	Power Domain	I/O Reset	I/O Pwr off	Description
PIO0	F7	25	IO	Input Pull-up	Input Pull-up	I/O PIO0 or CONFIG pin
PIO1	G7	28	IO	Input Pull-up	Input Pull-up	I/O PIO1 or CONFIG pin
PIO2	D7	27	IO	Input Pull-up	Input Pull-up	I/O PIO2 or CONFIG pin
PIO3	D6	30	IO	Input Pull-up	Input Pull-up	I/O PIO3 or CONFIG pin
PIO4	E7	26	IO	Input Pull-up	Input Pull-up	I/O PIO4 or CONFIG pin
PIO5	E6	29	IO	Input Pull-up	Input Pull-up	I/O PIO5 or CONFIG_SEL
PIO6	A4	19	IO	Input Pull-up	Input Pull-up	I/O PIO6
PIO7	A5	18	IO	Input Pull-up	Input Pull-up	I/O PIO7
PIO8	G6	31	IO	Input Pull-up	Input Pull-up	I/O PIO8
PIO9	G5	32	IO	Input Pull-up	Input Pull-up	I/O PIO9
PIO10	E5	33	IO	Input Pull-up	Input Pull-up	D_SEL
PIO11	F6	35	IO	Input Pull-up	Input Pull-up	I/O PIO11
PIO12	F5	34	IO	Input Pull-up	Input Pull-up	SAFEBOOT_N
PIO13	C4	14	IO	Input Pull-up	Input Pull-up	I/O PIO13
PIO14	C3	13	IO	Input Pull-up	Input Pull-up	I/O PIO14
PIO15	E4	36	IO	Input Pull-up	Input Pull-up	I/O PIO15
PIO16	F4	37	IO	Input Pull-up	Input Pull-up	I/O PIO16

Table 14: PIOs

7 Electrical specification

The limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Where application information is given, it is advisory only and does not form part of the specification. For more information regarding power management see the *UBX-M8030 Hardware Integration Manual* [1].

7.1 Absolute maximum rating

Symbol	Parameter	Min.	Max.	Unit
V_CORE, V_DCDC_IN, V_DCDC_OUT	Supply voltage baseband main core and RF LDOs inputs Input voltage of the internal DC/DC converter Output voltage of the internal DC/DC converter	-0.5	3.6	V
VDD_IO	Supply voltage I/O ring	-0.5	3.6	V
VDD_USB	Supply voltage USB	-0.5	3.6	V
V_BCKP	Supply voltage baseband backup core and TCXO LDOs inputs	-0.5	3.6	V
VDD_ANA, VDD_LNA	Supply voltage RF front-end	-0.5	1.6	V
Vi	Input voltage on XTAL_I	-0.5	3.6	V
Vi_{ANA}	Input voltage on RTC_I	-0.5	1.6	V
Vi_{DIG}	Input voltage on PIO0-16, RESET_N, TCK and TMS	-0.5	3.6	V
Prfin	RF Input power on LNA_IN		+15	dBm
Ptot	Total power dissipation		500	mW
Tjun	Junction temperature	-40	+105	°C
Ts	Storage temperature	-40	+125	°C

Table 15: Absolute maximum ratings

Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. The product is not protected against overvoltage or reversed voltages. If necessary, voltage spikes exceeding the power supply voltage specification, given in table above, must be limited to values within the specified boundaries by using appropriate protection diodes.

7.2 Operating conditions

☞ The test conditions specified in Table 16 apply to all characteristics defined in this section.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Tamb	Ambient temperature		-40	+25	+85	°C
GND	Ground			0		V
LDO_RF_OUT	LDO output voltage			1.2		V
LDO_C_OUT	LDO output voltage			1.2		V
LDO_B_OUT	LDO output voltage			1.2		V
LDO_X_OUT	LDO output voltage	VDD_IO = 1.65 V … 3.6 V		1.5		V
		VDD_IO = 1.65 V … 2.0 V		1.6		V
		VDD_IO = 2.0 V … 3.6 V		1.9		V
		VDD_IO = 2.7 V … 3.0 V		2.6		V
		VDD_IO = 3.1 V … 3.6 V		3.0		V
V_CORE	Core supply voltage			3.3		V
V_BCKP	Backup battery supply voltage			3.3		V
VDD_IO	Supply voltage I/O ring			3.3		V
VDD_USB	Supply voltage USB			3.3		V
VDD_ANA	Supply voltage for RF front-end supplied by LDO_RF_OUT			1.2		V
VDD_LNA	Supply voltage for RF front-end supplied by LDO_RF_OUT			1.2		V
Fref	Reference frequency			26		MHz

Table 16: Test conditions

☞ All specifications are at an ambient temperature of 25°C. Extreme operating temperatures can significantly impact specification values. Applications operating near the temperature limits should be tested to ensure the specification.

7.2.1 DC electrical characteristic

☞ For block diagrams of the Power Management Unit (PMU) see the *UBX-M8030 Hardware Integration Manual* [1].

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD_IO	Supply voltage for PIOs and input voltage for LDO_B and LDO_X	1.65	3.3	3.6	V
VDD_USB	Supply voltage USB	3.0	3.3	3.6	V
V_CORE	Input voltage for LDO_C and LDO_RF	1.4	3.3	3.6	V
V_BCKP	Input voltage for LDO_B and LDO_X (HW Backup Mode)	1.4		3.6	V
V_DCDC_IN	Input voltage for DC/DC converter	1.65		3.6	V

Table 17: Power supply pins

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
$I_{LDO\_X\_OUT}$	LDO_X output current[8]			1.5		mA
LDO_X_OUT	LDO_X output voltage[9]	for a 19 pF crystal	1.3	1.5	1.6	V
LDO_RF_OUT	LDO_RF output voltage		1.1	1.2	1.3	V
LDO_B_OUT	LDO_B output voltage		1.1	1.2	1.3	V
LDO_C_OUT	LDO_C output voltage		1.1	1.2	1.3	V
VDD_ANA	Power pin		1.1	1.2	1.3	V
VDD_LNA	Power pin		1.1	1.2	1.3	V
V_SWITCH	Voltage on VDD_IO to switch from V_BCKP to VDD_IO supply			1.4		V
POR_IO	Threshold value for VDD_IO configured by eFuse	1.8 V SQI flash memory 3.0 V SQI flash memory 3.3 V SQI flash memory			1.54 2.69 3.00	V V V

Table 18: Power management unit

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Ileak	Leakage current input pins			< 1		nA
Vil	Low level input voltage		0		0.2*VDD_IO	V
Vih	High level input voltage		0.7*VDD_IO		VDD_IO+0.5	V
Vol	Low level output voltage for PIO0-5	Iol = 12 mA			0.4	V
Voh	High level output voltage for PIO0-5	Ioh = 12 mA	VDD_IO -0.4			V
Vol	Low level output voltage for PIO6-16	Iol = 4 mA			0.4	V
Voh	High level output voltage for PIO6-16	Ioh = 4 mA	VDD_IO -0.4			V
Rpu	Pull-up resistor for PIO0-5,8,9, 11-14			11		kΩ
Rpu	Pull-up resistor for PIO6,7,10, 15,16 and TMS			115		kΩ
Rpd	Pull-down resistor for TCK			98		kΩ

Table 19: Digital IO pins

[8] Depending on VDD_IO and selected LDO_X output voltage
[9] LDO_X output voltage is configurable (see Table 10)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Ileak	Leakage current input pins				1	µA
Vil	Low level input voltage	VDD_USB >= 3.0 V	0		0.8	V
Vih	High level input voltage	VDD_USB >= 3.0 V	2.0		VDD_USB	V
Vol	Low level output voltage	R_L = 1.425 kΩ to VDD_USB, VDD_USB >= 3.0 V, 22 Ω external series resistor			0.3	V
Voh	High level output voltage	R_L = 14.25 kΩ to GND, VDD_USB >= 3.0, 22 Ω external series resistor	2.8			V
Rpui	Pull-up resistor, Idle State		870	900	950	Ω
Rpuo	Pull-up resistor, Operational State		1400	1490	1600	Ω

Table 20: USB pins

7.2.2 Baseband parameters

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
RTC_Fxtal	RTC crystal resonant frequency			32768		Hz
RTC_T_start	RTC startup time		0.2	0.35	0.9	sec
RTC_Iosc	32768 Hz OSC current source			0.4		µA
RTC_Amp	32768 Hz OSC oscillation amplitude	ESR = 80 kΩ	50		350	mVpp
RTC_ESR	32768 Hz Xtal equivalent series resistance				100	kΩ
RTC_CL	RTC integrated load capacitance	ESR = 80 kΩ	4	7	12	pF
RTC_Vil	RTC low level input voltage	Shared RTC oscillator input	0.0		0.2	V
RTC_Vih	RTC high level input voltage	Shared RTC oscillator input	0.8		1.2	V
DCDC_eff	DC/DC efficiency	3.3 V @ input, 4 mA - 80 mA, External components: L = 2.2 uH, C = 4.7pF		85		%
V_DCDC_out	DC/DC output voltage	DC/DC enabled, bypass inactive		1.4		V
T_SENSE_freq	Measurement ADC delta-sigma frequency			500		kHz
T_SENSE _IH	Measurement ADC high current for ΔVbe			320		µA
T_SENSE _IL	Measurement ADC low current for ΔVbe			10		µA
T_SENSE _Acc	Measurement ADC accuracy	JTM trimmed at 60 °C	-2.5		2.5	°C

Table 21: Baseband parameters

7.2.3 RF parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Fin	Receiver input frequency		1550	1575.42	1650	MHz
LNA_IN	LNA input impedance			11.5-j60		Ω
LNA_S11[10]	LNA input return loss	50 Ω environment		-10		dB
NFtot[10]	Receiver chain noise figure	50 Ω environment		3.0		dB
Ext_Gain[10]	External gain before matching	50 Ω environment			50	dB
TCXO_Freq	TCXO frequency			26		MHz
TCXO_IN_Vpp	TCXO input peak-to-peak voltage			0.8		V_{pp}
XTAL_Freq	XTO frequency			26		MHz
XTAL_Drive	XTAL drive level	@26 MHz, 15 Ω < ESR < 60 Ω			100	µW

Table 22: RF parameters

7.2.4 Current consumption

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{BCKP}	V_BCKP backup current using the RTC crystal	HW Backup Mode, LDO_B_OUT = 1.2V, VDD_IO = V_CORE = 0V		15		µA
I_{BCKP}	V_BCKP backup current using the 26MHz XTO in "single crystal" operation	HW Backup Mode, LDO_B_OUT = 1.2V, VDD_IO = V_CORE = 0V Crystal ESR = 20 Ω		185		µA
I_{VDD_IO}	VDD_IO backup current using the RTC crystal	SW Backup Mode, LDO_B_OUT = 1.2V, VDD_IO = V_CORE = 3V, LDO_C_OUT = LDO_RF_OUT = LDO_X_OUT = 0V		20		µA
I_{VDD_IO}	VDD_IO backup current using a 7pF 26MHz XTO in "single crystal" operation	SW Backup Mode, LDO_B_OUT = 1.2V, VDD_IO = V_CORE = 3V, LDO_C_OUT = LDO_RF_OUT = 0V, LDO_X_OUT = 1.5V		100		µA
I_{SLEEP}	V_CORE sleep core current	Sleep Mode, LDO_C_OUT = LDO_RF_OUT= 1.2V		125		µA

Table 23: Current Consumption

[10] Measured with external noise matching

7.3 Indicative power requirements

Table 24 lists examples of the total system supply current including RF and baseband section for a possible application.

Values in Table 24 are provided for customer information only as an example of typical current requirements. Values are characterized on samples – actual power requirements can vary depending on FW version used, external circuitry, number of SVs tracked, signal strength, type and time of start, duration, and conditions of test.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{PEAK}	Peak current	Start-up			100	mA
I_{VDD_IO} [11]	VDD_IO current	Tracking (GPS-only, Continuous Mode)		0.5		mA
		Tracking (GPS and GLONASS concurrently, Continuous Mode)		0.5		mA
		Tracking (GPS-only, Power Save Mode)[14]		0.5		mA
I_{V_CORE} [12]	V_CORE current	Acquisition (GPS-only)		33.6		mA
		Acquisition (GPS and GLONASS concurrently)		43.2		mA
		Tracking (GPS-only, Continuous Mode)		29.9		mA
		Tracking (GPS and GLONASS concurrently, Continuous Mode)		42.7		mA
		Tracking (GPS-only, Power Save Mode)[14]		8.3		mA
$I_{V\_DCDC\_IN}$ [13]	V_DCDC_IN current	Acquisition (GPS-only)		18.3		mA
		Acquisition (GPS and GLONASS concurrently)		24.2		mA
		Tracking (GPS-only, Continuous Mode)		16.9		mA
		Tracking (GPS and GLONASS concurrently, Continuous Mode)		24.0		mA
		Tracking (GPS-only, Power Save Mode)[14]		4.6		mA

Table 24: Currents to calculate the indicative power requirements

For more information about power requirements, see the *UBX-M8030 Hardware Integration Manual* [1].

All values in Table 23 and Table 24 are measured at 25°C ambient temperature.

[11] VDD_IO = 3.0 V, Current depends on the number of used PIOs.
[12] V_CORE = 1.4 V, DC/DC converter disabled. Simulated GNSS constellation using power levels of -130 dBm.
[13] V_DCDC_IN = 3.0 V, DC/DC converter enabled. Simulated GNSS constellation using power levels of -130 dBm.
[14] Power Save Mode in cyclic tracking operation, update period 1 sec.

7.4 SPI timing diagrams

In order to avoid incorrect operation of the SPI, the user needs to comply with certain timing conditions. The following signals need to be considered for timing constraints:

Symbol	Description
SPI CS_N (SS_N)	Slave select signal
SPI CLK (SCK)	Slave clock signal

Table 25: Symbol description

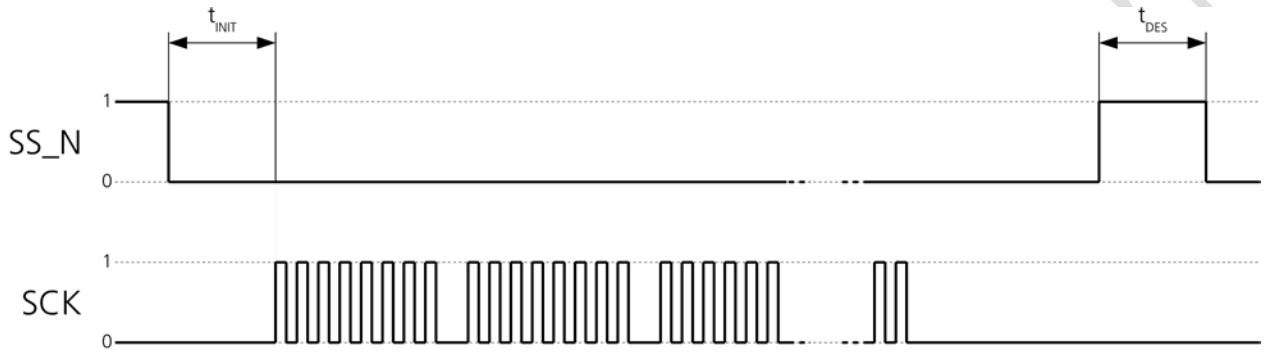


Figure 6: SPI timing diagram

7.4.1 Timing recommendations

The recommendations below are based on a firmware running from SQI flash memory.

Parameter	Description	Recommendation
t_{INIT}	Initialization Time	500 µs
t_{DES}	Deselect Time	1 ms.
Bit rate		1 Mb/s

Table 26: SPI timing recommendations

☞ The values in the above table result from the requirement of an error-free transmission. By allowing just a few errors and disabling the glitch filter, the bit rate can be increased considerably.

7.5 DDC timing diagrams

The DDC interface is I²C Fast Mode compliant. For timing parameters consult the I²C standard.

☞ The maximum bit rate is 400 kbit/s. The interface stretches the clock when slowed down while serving interrupts, so real bit rates may be slightly lower.

8 Mechanical specification

8.1 WL-CSP47 (UBX-M8030-CT)

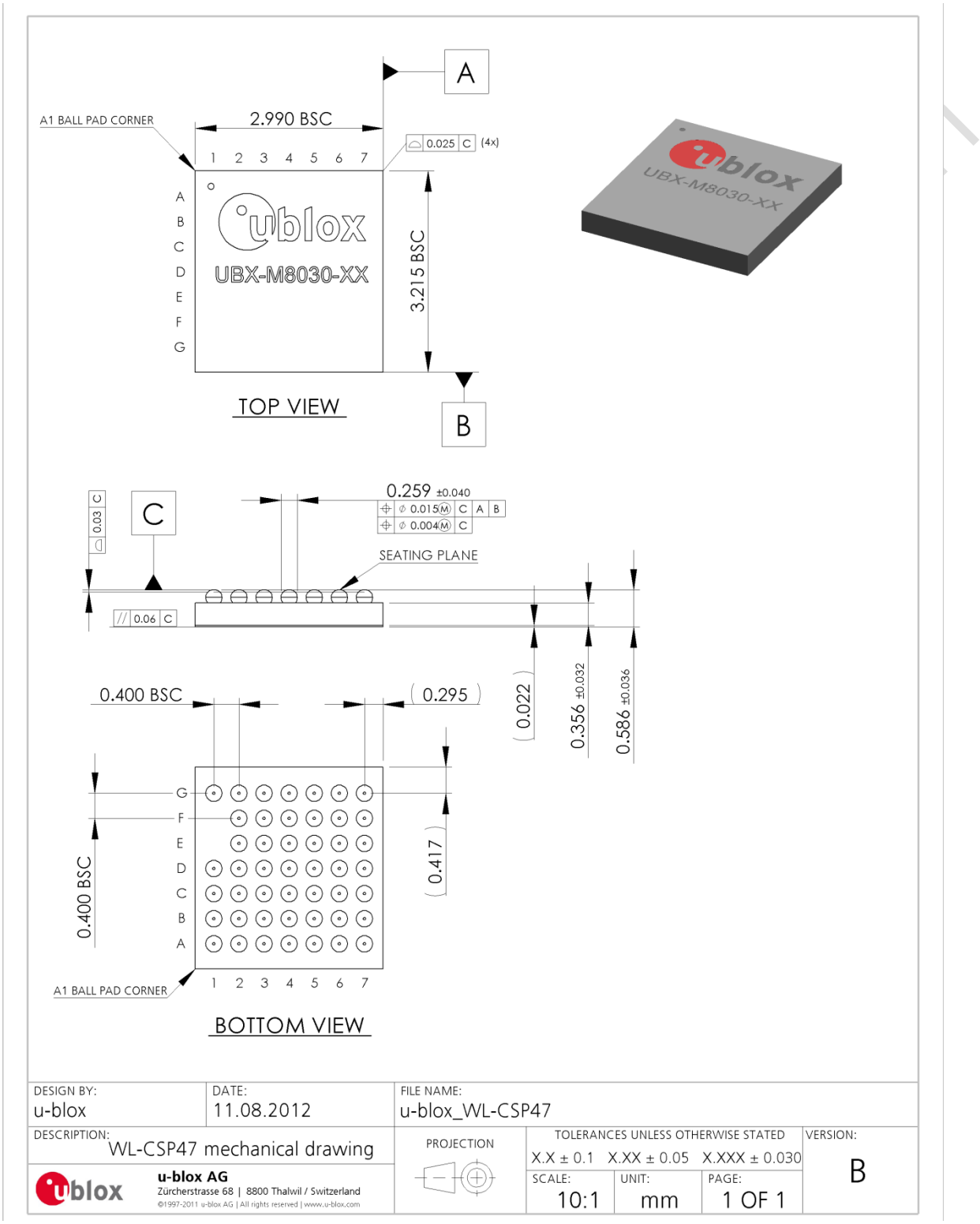


Figure 7: UBX-M8030-CT mechanical drawing

8.2 QFN40 (UBX-M8030-KT, UBX-M8030-KA)

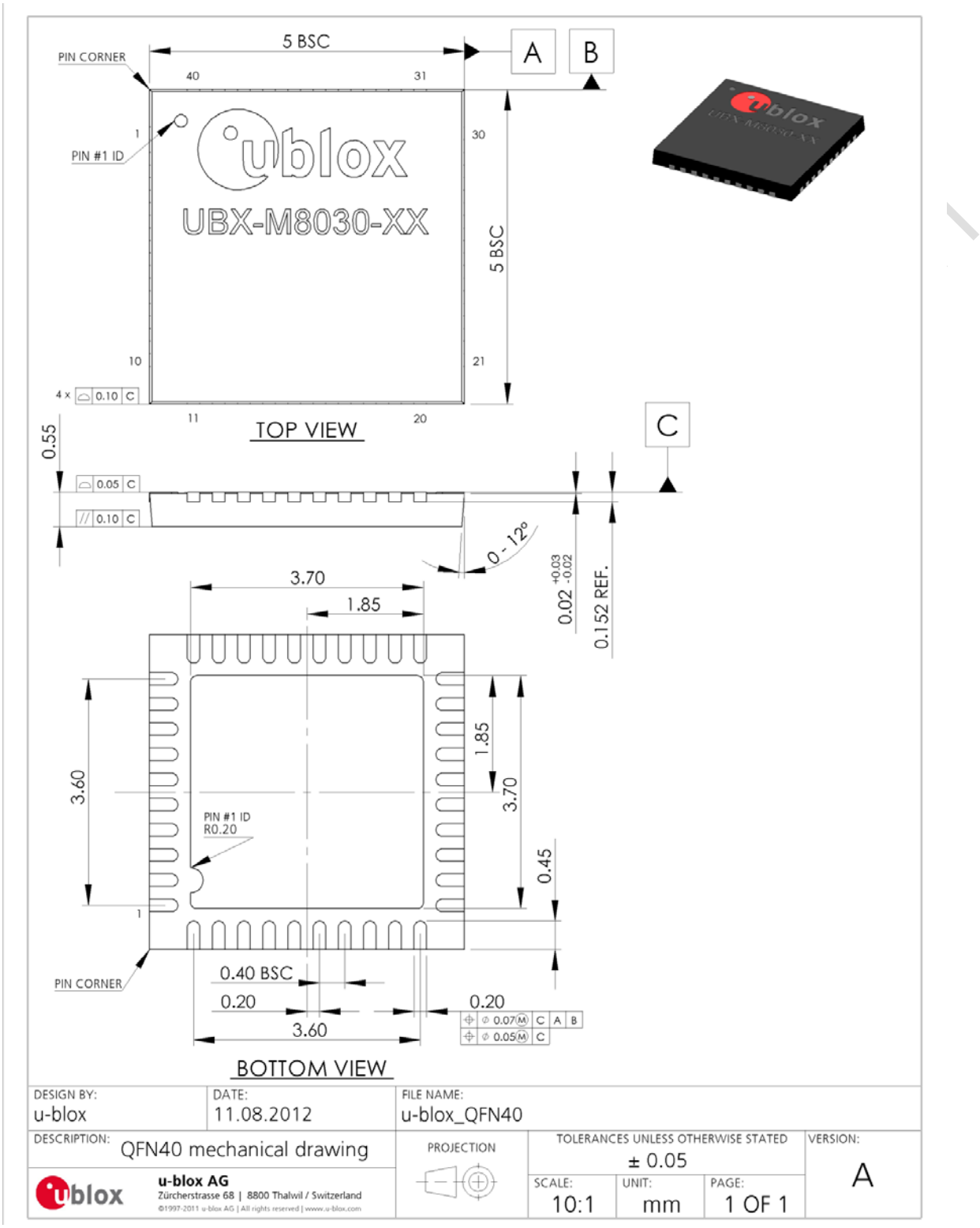


Figure 8: UBX-M8030-KT/KA mechanical drawing

9 Reliability tests and approvals

9.1 Reliability tests

u-blox M8030 chips are qualified according to appropriate JEDEC standards, e.g. JESD47 *Stress-Test-Driven Qualification of Integrated Circuits.*

The UBX-M8030-KT and UBX-M8030-KA chips are qualified according to *AEC-Q100 Failure Mechanism Based Stress Test Qualification For Integrated Circuits.*

9.2 Approvals

Products marked with this lead-free symbol on the product label comply with the "Directive 2002/95/EC of the European Parliament and the Council on the Restriction of Use of certain Hazardous Substances in Electrical and Electronic Equipment" (RoHS).

UBX-M8030-CT, UBX-M8030-KT, and UBX-M8030-KA are RoHS compliant and green (no halogens).

10 Product handling

10.1 Packaging

UBX-M8030 chips are delivered as hermetically sealed, reeled tapes in order to enable efficient production, production lot set-up and tear-down. For more information about packaging, see the *u-blox Package Information Guide* [3].

Figure 9: Reeled u-blox chips

10.1.1 Reels

UBX-M8030 chips are deliverable in quantities of 5000/4000pcs on a reel, they are delivered using reel Type A as described in the *u-blox Package Information Guide* [3].

IC Package	Reel Type	Delivery Quantity
WL-CSP47	A	5000
QFN40	A	4000

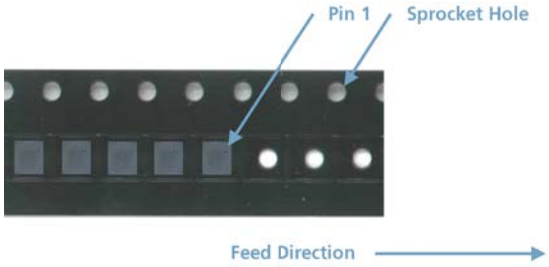
Table 28: Reel information for UBX-M8030 chips

IC Package	Tape Width	Flange Combination
WL-CSP47	12 mm	4 mm + 8 mm
QFN40	12 mm	4 mm + 8 mm

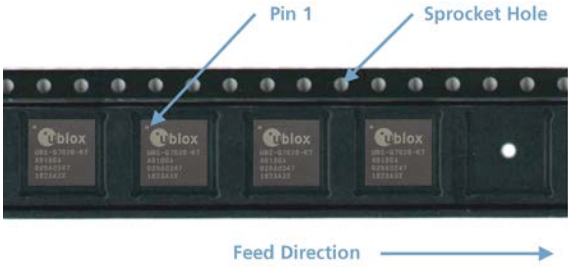
Table 29: Reel composition of two halves

10.1.2 Tapes

Figure 10 shows the feed direction and illustrates the orientation of the UBX-M8030 chips on the tape: The chips are placed such that the pin 1 is at the upper right for the WL-CSP47 and at the upper left for the QFN40.



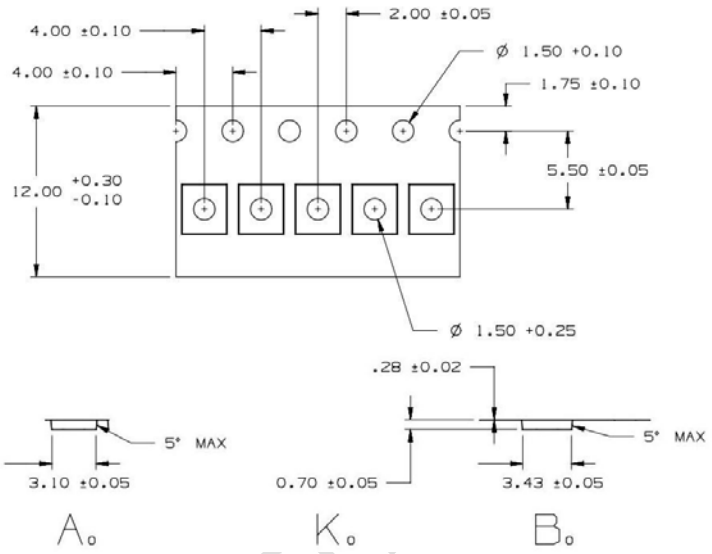
WL-CSP47



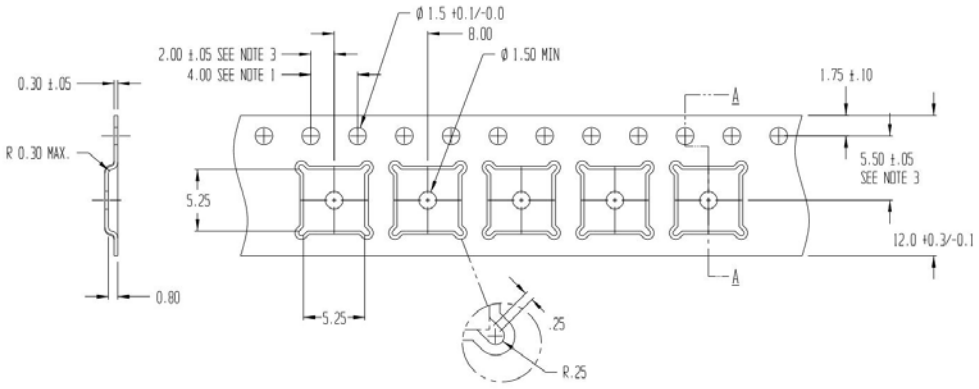
QFN40

Figure 10: Orientation of UBX-M8030 chips on the tape

The dimensions of the tapes for UBX-M8030 chips are specified in Figure 11 (measurements in mm).



WL-CSP47 tape dimensions (mm)



QFN40 tape dimensions (mm)

Figure 11: UBX-M8030 tape dimensions (mm)

10.2 Moisture Sensitivity Levels

The Moisture Sensitivity Levels (MSL) for UBX-M8030 chips are specified in Table 30. For more information regarding moisture sensitivity levels, labeling, storage and drying see the *u-blox Package Information Guide* [3].

Package	MSL Level
WL-CSP47	1
QFN40	1

Table 30: MSL levels

For MSL standard see IPC/JEDEC J-STD-020, which can be downloaded from www.jedec.org.

10.3 ESD handling precautions

UBX-M8030 chips contain highly sensitive electronic circuitry and are Electrostatic Sensitive Devices (ESD). Observe precautions for handling! Failure to observe these precautions can result in severe damage to the GNSS receiver!

11 Default messages

Interface	Settings
UART Output	9600 Baud, 8 bits, no parity bit, 1 stop bit Configured to transmit both NMEA and UBX protocols, but only following NMEA and no UBX messages have been activated at start-up: **GGA, GLL, GSA, GSV, RMC, TTG, TXT**
USB Output	Configured to transmit both NMEA and UBX protocols, but only following NMEA and no UBX messages have been activated at start-up: **GGA, GLL, GSA, GSV, RMC, TTG, TXT** USB Power Mode: Bus Powered
UART Input	9600 Baud, 8 bits, no parity bit, 1 stop bit, Autobauding disabled Automatically accepts following protocols without need of explicit configuration: UBX, NMEA, RTCM The GNSS receiver supports interleaved UBX and NMEA messages.
USB Input	Automatically accepts following protocols without need of explicit configuration: UBX, NMEA, RTCM The GNSS receiver supports interleaved UBX and NMEA messages. USB Power Mode: Bus Powered

Table 31: Default messages

☞ Refer to the *u-blox M8 Receiver Description Including Protocol Specification* [2] for information about further settings.

12 Labeling and ordering information

12.1 Product labeling

12.1.1 WL-CSP47 (UBX-M8030-CT)

WL-CSP47 semiconductor products provide 4 lines of text:

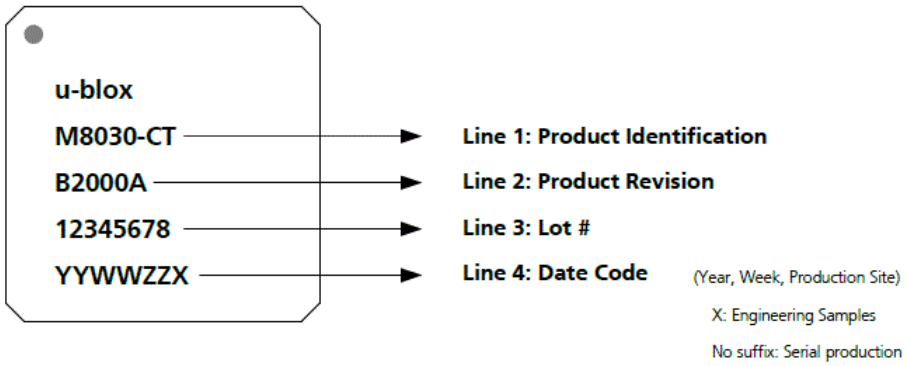


Figure 12: Description of WL-CSP47 product label

12.1.2 QFN40 (UBX-M8030-KT, UBX-M8030-KA)

QFN40 semiconductor products provide 4 lines of text:

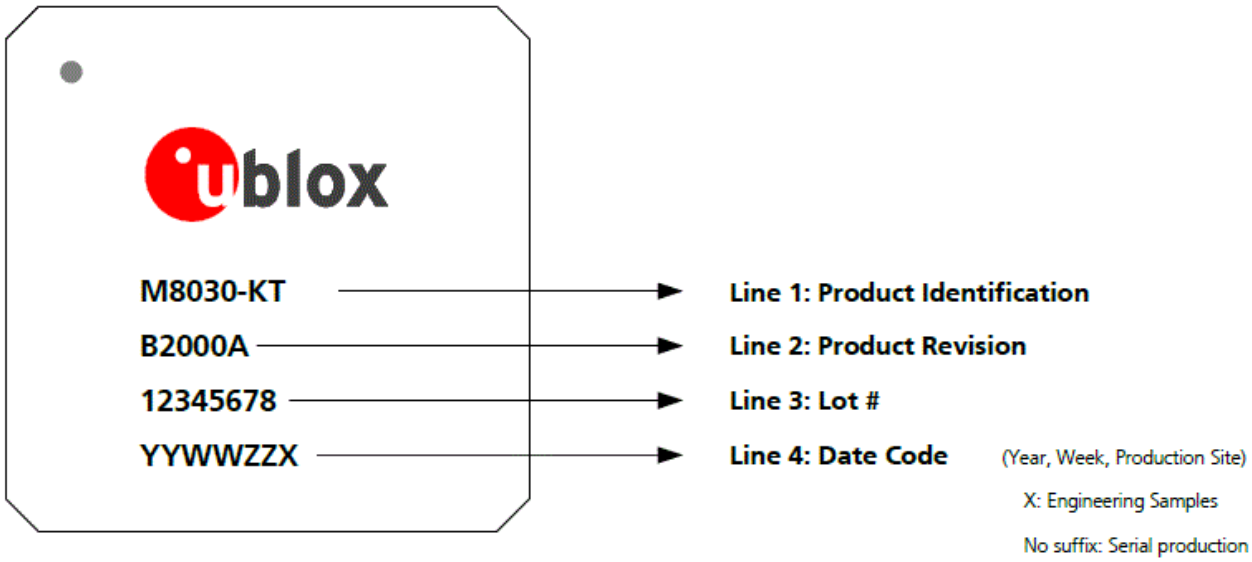


Figure 13: Description of QFN product label

12.2 Explanation of product codes

Three different product code formats are used. The **Product Name** is used in documentation such as this datasheet and identifies all u-blox M8 products, independent of packaging and quality grade. The **Ordering Code** includes packaging and quality, while the **Type Number** includes the hardware and firmware versions. Table 32 below details these three different formats:

Format	Structure
Product Name	Mmmnn
Ordering Code	UBX-Mmmnn-PT-VV
Type Number	UBX-Mmmnn-PT-RffooS

Table 32: Product code formats

The parts of the product code are explained in Table 33.

Code	Meaning	Example
UBX	u-blox	
M	Product platform	M = Multi-Constellation GNSS
mm	Baseband	80 = u-blox M8 BB section
nn	RF	30 = u-blox M8 RF section
P	Package type	C= WL-CSP47 K= QFN40
T	Quality grade	T = Standard A = Automotive
VV	Optional chip variant	
R	Hardware revision	Increasing alphabetic character
ff	Firmware revision	Increasing number
oo	eFuse revision	Increasing number
S	RF hardware revision	Increasing alphabetic character

Table 33: Part identification code

12.3 Ordering codes

Ordering No.	Product
UBX-M8030-CT	u-blox M8 GNSS receiver, 47 pin WL-CSP
UBX-M8030-KT	u-blox M8 GNSS receiver, 40 pin QFN

Table 34: Product ordering codes for standard grade chips

Ordering No.	Product
UBX-M8030-KA	u-blox M8 GNSS receiver, 40 pin QFN

Table 35: Product ordering codes for automotive grade chip

☞ Product changes affecting form, fit or function are documented by u-blox. For a list of Product Change Notifications (PCNs) see our website at: http://www.u-blox.com/en/notifications.html.

Related documents

[1] UBX-M8030, u-blox M8 GNSS chips, Hardware Integration Manual, Docu. No. UBX-13001708
[2] u-blox M8 Receiver Description Including Protocol Specification V15, Docu. No. UBX-13002887
[3] u-blox Package Information Guide, Docu. No. G-X-11004

☞ For regular updates to u-blox documentation and to receive product change notifications please register on our homepage.

Revision history

Revision	Date	Name	Status / Comments
1	8 May 2013	ffel	Initial version
2	15 Jul. 2013	ffel	Objective Specification
R03	21 Oct. 2013	ffel	Release of firmware version FW2

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