CS-2110 Quiz 3A

Alan Chiang

TOTAL POINTS

100 / 100

QUESTION 1

- 1 Completing Circuits 40 / 40
 - + 0 Graded. Rubric items are ordered from top AND gate to bottom. Order does not matter within connections to the OR gate.
 - + 5 The inputs to this gate can technically be anything.
 - + 5 A: o B: o Cin: Connected
 - + 5 A: o B: Connected Cin: o
 - + 5 A: Connected B: o C: o
 - + 5 A: o B: Connected C: Connected
 - + 5 A: Connected B: o C: Connected
 - + 5 A: Connected B: Connected C: o
 - + 5 A: Connected B: Connected C: Connected

QUESTION 2

- 2 Daisy Chaining 20 / 20
 - + O Graded
 - + 20 Carry out of each one bit adder should be hooked up to the carry in of the next adder.

QUESTION 3

- 3 Multiplexer 10 / 10
 - + O Graded
 - + 5 A combinational logic circuit that takes in a number of different inputs and selects one of the inputs to output based on the values of the control bit.
 - + 5 Ex. Picking an output for an ALU.

QUESTION 4

- 4 DeMorgan's 10 / 10
 - + O Graded
 - + 10 Using a NOR gate.
 - + 5 Correctly identified ~(AIB) but did not

draw/describe circuit.

QUESTION 5

- 5 Decoder Outputs 5/5
 - + O Graded
 - + 5 4

QUESTION 6

- 6 Multiplexer Outputs 5 / 5
 - + O Graded
 - +51

QUESTION 7

- 7 Subtractor 10 / 10
 - + O Graded
 - + 5 Making one of the inputs negative by using a NOT and then adding one to it.
 - + 5 Adding the negated input with another input.

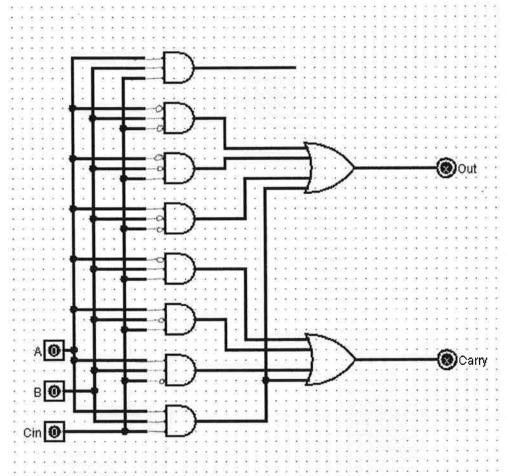
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Name: Alan Chiang

Section: _

Completing Circuits: (____/ 60)

1. Given this unfinished 1 bit full adder, complete the adder by connecting the wires between the inputs and the gates. You can either connect the wire directly or use a O to negate the connection between the and the AND gates. Order does not matter, as long as the outputs are correct for all combinations of inputs.



Explain the concept of daisy chaining with regards to creating multibit adders out of one bit full

Adder 2. Explain the concept of vally original adders. You may use a drawing to help explain your answer.

A=Ainput B=Binput Daisy chaining means linking multiple one-bit adders together ci=(arryin Such that the carry-out of a previous adder is the Co=(arryout carry-in of the next one.

A= I Input bits Input bits Input bits More input bits

and so on

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Name: Alan Chiang Section:	
Short Answer: (/ 40) You may answer these questions by drawing a circuit diagram where applicable.	
1. What is a multiplexer? Give an example of a situation in which you would use one. A device that uses n selector bits to select one of 2" inputs to be the one output. Multiplexors are used in ALUs to choose one of multiple operations, like addition, subtraction, is 2. How can you evaluate ~A & ~B with a circuit without using an AND gate?	Output Multiple of 4, multiple (et
Use De Morgan's Law, which says ~A & ~B is equin to A B. Then just connect input A and input A	ralent

3. Given a **Decoder** with **2** select bits, how many outputs can the decoder have?

4. Given a Multiplexer with 2 select bits, how many outputs can the multiplexer have?

1 output

5. Create a 4 bit subtractor using full adders, gates, and Logisim wiring components...

