

Toyon Research Corporation

Lab 7: Correlation Decoding

Chilipepper Tutorial Projects

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Lab 7: Correlation Decoding

Introduction

This lab will extend the previous labs and allow you to decode the received signal to extract the original message. The Analog to Digital Conversion (ADC) used to receive the signal will take place on the Chilipepper board. The FMC initialization and microcontroller (MCU) signal control will be handled in software using the Xilinx Software Development Kit (SDK). The frequency estimation, band-pass filtering, and timing recovery of the signal from the previous labs will take place on the FPGA via an exported Simulink Pcore. Finally, the testing of results will be done using ChipScope and MATLAB. This lab assumes prior knowledge of the workings of HDL Coder as well as the Xilinx EDK environment. It is recommended that you complete the previous labs before completing this lab.

This lab is created using:

- MATLAB 2013a
- Xilinx ISE Design Suite 14.4 with EDK and System Generator
- Windows 7, 64-bit

Procedure

This lab is organized into a series of steps, each including general instructions and supplementary steps, allowing you to take advantage of the lab according to your experience level.

This lab consists of the following basic steps:

- Generate HDL code from a MATLAB algorithm
- Create and export Simulink models using System Generator
- Configure your created PCores and export the design into SDK
- Create software to run your design
- Test and verify your results

Objectives

After completing this lab, you will be able to:

- Create a Simulink model to implement a basic signal receiver
- Receive and Decode a QPSK transmitted pattern
- Create a software application to test your design
- Verify your results in ChipScope and analyze them using MATLAB

Generate HDL Code

Step 1

This section will show you how to create your MATLAB function and test bench files as well as the process for generating the HDL code used in the Simulink model.

1.1 MATLAB Functions

Your MATLAB functions will eventually become a core that will be synthesized into hardware. The algorithm describes the operations in each clock cycle, and processes data on a sample-by-sample basis. This lab builds on the MATLAB algorithm used in Lab 6 and adds correlation to extract the original packet. This allows the user to successfully decode the original message payload. The first function used is shown in Figure 1-1.

```
function [r_out, s_f_out, s_c_out, s_t_out, t_est_out, f_est_out, ...
        byte_out, en_out, s_p_out, s_o_out] = ...
        qpsk_rx(i_in, q_in, mu_foc_in, mu_toc_in)

%scale input data coming from the Chilipepper ADC to be purely fractional
% to avoid scaling issues
r_in = complex(i_in, q_in);

%frequency offset estimation. Note that time constant is input as integer
[s_f_i, s_f_q, fe] = qpsk_rx_foc(i_in, q_in, mu_foc_in);
% Square-root raised-cosine band-limited filtering
[s_c_i, s_c_q] = qpsk_rx_srrc(s_f_i, s_f_q);
% Time offset estimation. Output data changes at the symbol rate.
[s_t_i, s_t_q, tauh] = qpsk_rx_toc(s_c_i, s_c_q, mu_toc_in);
% Determine start of packet using front-loaded training sequence
[byte, en, s_p, s_o] = qpsk_rx_correlator(s_t_i, s_t_q);

%correlator output. en notifies byte changes (change is @ OSRATE)
byte_out = byte;
en_out = en;
% estimation and correlation values
t_est_out = tauh;
f_est_out = fe;
s_p_out = s_p;
s_o_out = s_o;
% original signal out (real version)
r_out = real(r_in);
% incremental signal outputs after frequency estimation, filtering, and
% timing estimation
s_f_out = complex(s_f_i, s_f_q);
s_c_out = complex(s_c_i, s_c_q);
s_t_out = complex(s_t_i, s_t_q);
end
```

Figure 1-1: MATLAB function to analyze received signal.

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This function is almost identical to the one used in the previous lab, however it adds the rx correlator function call.

1. Create a directory for the project under C:\QPSK_Projects\Project_7.
2. Create a MATLAB directory within the main project directory.
3. Create a new **MATLAB function** with the contents of Figure 1-1.
4. **Save** this function as `qpsk_rx.m` inside the project directory.

The first task of this function is implementing the frequency and timing correction covered in the previous labs. The code for this functionality is assumed to have been created previously and is not shown in this lab. The same is true for the raised-cosine band-limited filter function. Please refer to the previous labs for the code used within these functions. The correlation is handled by the function `qpsk_rx_correlator.m` which can be seen in **Appendix A**. This function implements an algorithm which attempts to read the input bits by converting the symbol constellations into bit sequences. The output is in Bytes, and each byte is only sent out at the OS rate. This Byte change is also indicated with the `en_out` notification.

5. Create a new **MATLAB function** with the contents of Appendix A.
6. Save this function as `qpsk_rx_correlator.m` inside the MATLAB project directory

1.2 MATLAB Test Bench

Now that you have added the code needed to further analyze the signal, we also need to slightly modify the previously created test bench script for the functions. For this lab the objective of the test bench script is not only to observe the output graph of the result, but also to verify the ascii message received. To accomplish this, we need to account for more output data from the QPSK rx function. Just as before, this script will need to simulate a transmitted waveform for the initial analysis. After the algorithm has been verified using simulated data, and the FPGA design completed, you will again need to verify the algorithms with actual data from ChipScope. This will be done later in Section 6 of this lab. The code used for this script is shown in **Appendix B**.

Note

There is a variable called `sim` in the script which allows you to either load your received waveform data from ChipScope or simulate a received QPSK signal in MATLAB and analyze the results. Setting it to 1 simulates the waveform, 0 loads it from a ChipScope prn file.

1. Create a new **MATLAB script** with the contents of Appendix B.

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2. Save this function as `qpsk_tb.m` inside the project directory

These are the only files required for the analysis of a received waveform when using exported ChipScope data. However to use simulated data for initial verification of the algorithm, you must also add the files used in the QPSK lab to your project directory. For your reference a list of the required files is given below. Refer to Lab 3 Output QPSK to recreate these files, or download them from the Chilipepper Github Repo¹.

Required files for creating Simulated QPSK waveform

- `make_train_lut.m`
- `CreateAppend16BitCRC.m`
- `qpsk_tx.m`
- `qpsk_tx_byte2sym.m`
- `qpsk_srrc.m`
- `mybitget.m`

Also be sure you have the required files used in the previous lab for DC_Offset correction, frequency estimation as well as timing offset estimation. Once you have all the required MATLAB files in your project directory, you can run the test bench script to view the waveform analysis. You may have to run the script twice to create the needed LUT files. Your data should look similar to the results shown in Figures 1-2 and 1-3. Be sure you have the `sim` variable in the test bench script set to 1. Feel free to modify the original ASCII string in the test bench script to test the algorithm for different messages.

¹ https://github.com/Toyon/Chilipepper/tree/master/Labs/Lab_7/Matlab

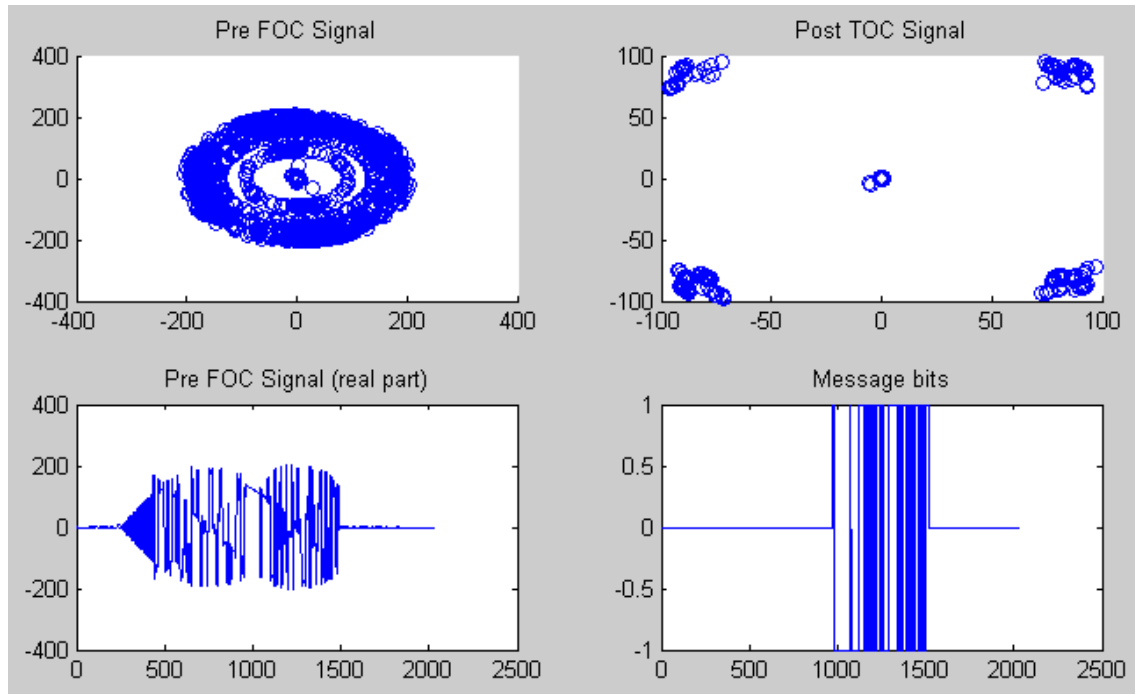


Figure 1-2: Analysis results for simulated QPSK signal

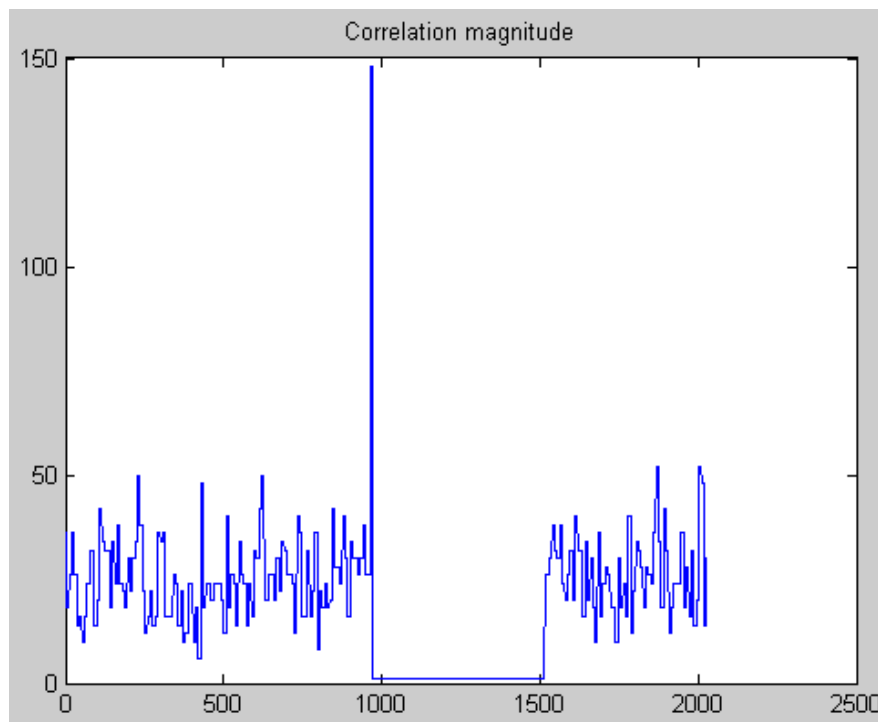


Figure 1-3: correlation magnitude for simulated QPSK signal during training sequence detection

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As you can see from the results of the figures, the new MATLAB function allows for detecting the front loaded training sequence, which is used to verify the start of a new packet. The correlation between the signal and the sequence is clearly seen in Figure 1-3, and this result is used to begin the next phase of the algorithm, which is packing the bits into each byte sequence.

1.3 RX HDL Coder Project

Using the same steps outlined in the previous labs, create a new HDL coder project called rx_qpsk. Add your MATLAB function `qpsk_rx.m` and your test bench script `qpsk_tb.m` to the **MATLAB Function** and **MATLAB Test Bench** categories respectively.

Once you open your Workflow Advisor, you should be greeted with a screen similar to Figure 1-4 which allows you to define input types for your function. You can also allow them to be auto-defined by simply selecting run, and letting MATLAB analyze your design. For the inputs listed for the `qpsk_rx` function, the auto-defined types are fine.

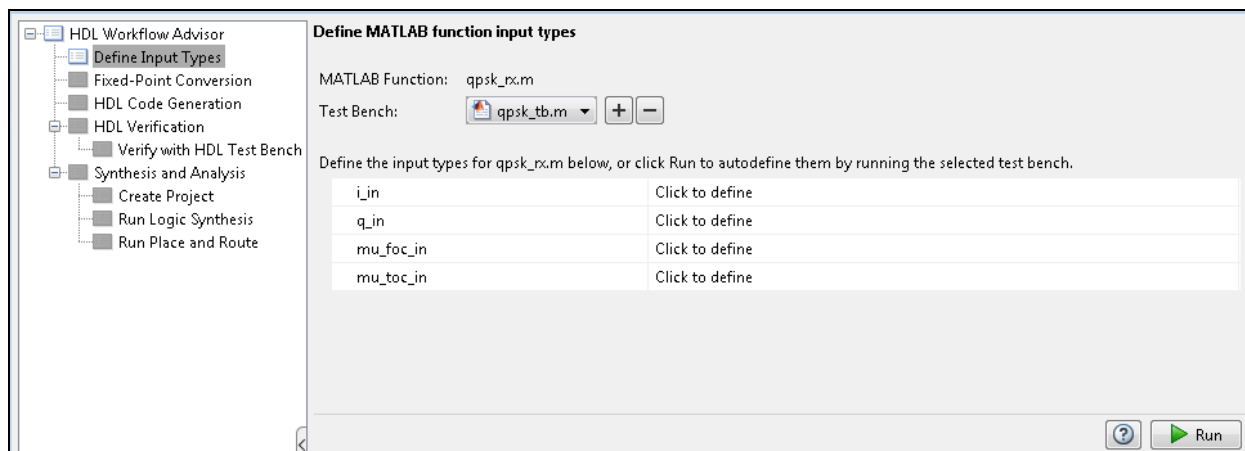


Figure 1-4: HDL Code Generation Workflow Advisor

1. Open Workflow Advisor and select “Run” to define the input types.
2. Click on Fixed-Point Conversion and select run this task. This process may take awhile.

Once the process is completed, you should receive a popup that says “Validation succeeded”. This means that MATLAB has successfully analyzed your design and selected fixed point types to replace the floating point arithmetic required in your algorithm. However, not all of the automatic selections are sufficient for our FPGA design; therefore several of the conversions will need to be modified.

3. Using the function dropdown menu at the top of the HDL Code Generation screen, select each of the functions in the design and make the following modifications.

Note

Many of the Fixed-Point conversions are the same as those used in the previous labs. For your convenience, this lab only shows the Functions which have more input/output variables than the previous labs, and whose proposed types need to be modified. Refer to the previous lab for information on all other proposed types.

qpsk_rx

Input						
i_in	double	-204	204		Yes	numerictype(1, 12, 0)
mu_foc_in	double	40	40		Yes	numerictype(0, 12, 0)
mu_toc_in	double	327	327		Yes	numerictype(0, 12, 0)
q_in	double	-204	206		Yes	numerictype(1, 12, 0)
Output						
byte_out	double	0	211		Yes	numerictype(0, 8, 0)
en_out	double	0	1		Yes	numerictype(0, 1, 0)
f_est_out	double	-0.01	1		No	numerictype(1, 26, 12)
r_out	double	-204	204		Yes	numerictype(1, 12, 0)
s_c_out	complex double	-98.16	97.57		No	numerictype(1, 26, 12)
s_f_out	complex double	-162.2	159.73		No	numerictype(1, 26, 12)
s_o_out	double	1	148		Yes	numerictype(0, 12, 0)
s_p_out	double	-1	1		Yes	numerictype(1, 2, 0)
s_t_out	complex double	-95.93	95.96		No	numerictype(1, 26, 12)
t_est_out	double	-0.8	1.12		No	numerictype(1, 20, 12)
Local						
byte	double	0	211		Yes	numerictype(0, 8, 0)
en	double	0	1		Yes	numerictype(0, 1, 0)
fe	double	-0.01	1		No	numerictype(1, 26, 12)
r_in	complex double	-204	206		Yes	numerictype(1, 12, 0)
s_c_i	double	-96.57	97.57		No	numerictype(1, 26, 12)
s_c_q	double	-98.16	95.84		No	numerictype(1, 26, 12)
s_f_i	double	-160.48	159.73		No	numerictype(1, 26, 12)
s_f_q	double	-162.2	157.79		No	numerictype(1, 26, 12)
s_o	double	1	148		Yes	numerictype(0, 12, 0)
s_p	double	-1	1		Yes	numerictype(1, 2, 0)
s_t_i	double	-94.3	95.96		No	numerictype(1, 26, 12)
s_t_q	double	-95.93	95.58		No	numerictype(1, 26, 12)
tau_h	double	-0.8	1.12		No	numerictype(1, 20, 12)

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qpsk_rx_correlator

▲ Input						
s_i_in	double	-94.3	95.96		No	numerictype(1, 26, 12)
s_q_in	double	-95.93	95.58		No	numerictype(1, 26, 12)
▲ Output						
byte_out	double	0	211		Yes	numerictype(0, 8, 0)
en_out	double	0	1		Yes	numerictype(0, 1, 0)
o_out	double	1	148		Yes	numerictype(0, 12, 0)
s_out	double	-1	1		Yes	numerictype(1, 2, 0)
▲ Persistent						
bits	1 x 8 double	0	1		Yes	numerictype(0, 1, 0)
byteCount	double	0	17		Yes	numerictype(0, 12, 0)
counter	double	0	8		Yes	numerictype(0, 4, 0)
detPacket	double	0	1		Yes	numerictype(0, 1, 0)
ip	double	0	30		Yes	numerictype(0, 12, 0)
numBytes	double	11	1000		Yes	numerictype(0, 12, 0)
oLatch	double	0	148		Yes	numerictype(0, 12, 0)
op	double	0	130		Yes	numerictype(0, 12, 0)
q	double	0	1		Yes	numerictype(0, 2, 0)
sBuf_i	1 x 65 double	-1	1		Yes	numerictype(1, 2, 0)
sBuf_q	1 x 65 double	-1	1		Yes	numerictype(1, 2, 0)
sLatch	double	-1	1		Yes	numerictype(1, 2, 0)
symCount	double	0	4		Yes	numerictype(0, 3, 0)
▲ Local						
BIT_TO_BYTE	8 x 1 double	1	128		Yes	numerictype(0, 8, 0)
OS_RATE	double	8	8		Yes	numerictype(0, 4, 0)
sc_iWithi	double	-17	21		Yes	numerictype(1, 13, 0)
sc_iWithq	double	-65	29		Yes	numerictype(1, 13, 0)
sc_qWithi	double	-15	65		Yes	numerictype(1, 13, 0)
sc_qWithq	double	-19	19		Yes	numerictype(1, 13, 0)
sHard_i	double	-1	1		Yes	numerictype(1, 2, 0)
sHard_i_t	double	-1	1		Yes	numerictype(1, 2, 0)
sHard_q	double	-1	1		Yes	numerictype(1, 2, 0)
sHard_q_t	double	-1	1		Yes	numerictype(1, 2, 0)
ss_i	double	-1	1		Yes	numerictype(1, 2, 0)
ss_q	double	-1	1		Yes	numerictype(1, 2, 0)
t_i	65 x 1 double	-1	1		Yes	numerictype(1, 2, 0)
t_q	65 x 1 double	-1	1		Yes	numerictype(1, 2, 0)

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Once all modifications have been made, select “Validate Types” in the top right area of the top toolbar to verify the design for your modified Fixed-Point conversions. Again, once the process is complete, you should get a message saying Validation Succeeded.

4. Select Validate Types to verify the new design
5. Click on HDL Code Generation and modify the settings according to the previous labs. There is no pipelining required for this project. Right Click and select run this task to generate your Xilinx Block Box Design.
6. Once created, copy the black box and System generator Blocks to a new Model just as in the previous labs.
7. Save the new model as rx.slx into the sysgen directory “Lab_7\sysgen”.
8. Copy the `qpsk_rx_FixPt_xsgbbxcfg.m` file into your Sysgen folder just as in the previous labs.
9. Create the hdl folder inside the Sysgen folder and copy your vhd files into this directory. Make sure you modify the previously copied m file to point to the new location of the vhd files.

Create and export Simulink models

Step 2

This section will show you how to create and customize your Simulink models to properly receive a signal and control the Chilipepper MCU and ADC. For additional information on this process, see lab 2.

2.1 Create MCU Simulink Design

The **Simulink model**² in Figure 2-1 will be used for the control signals to and from the **MCU**.

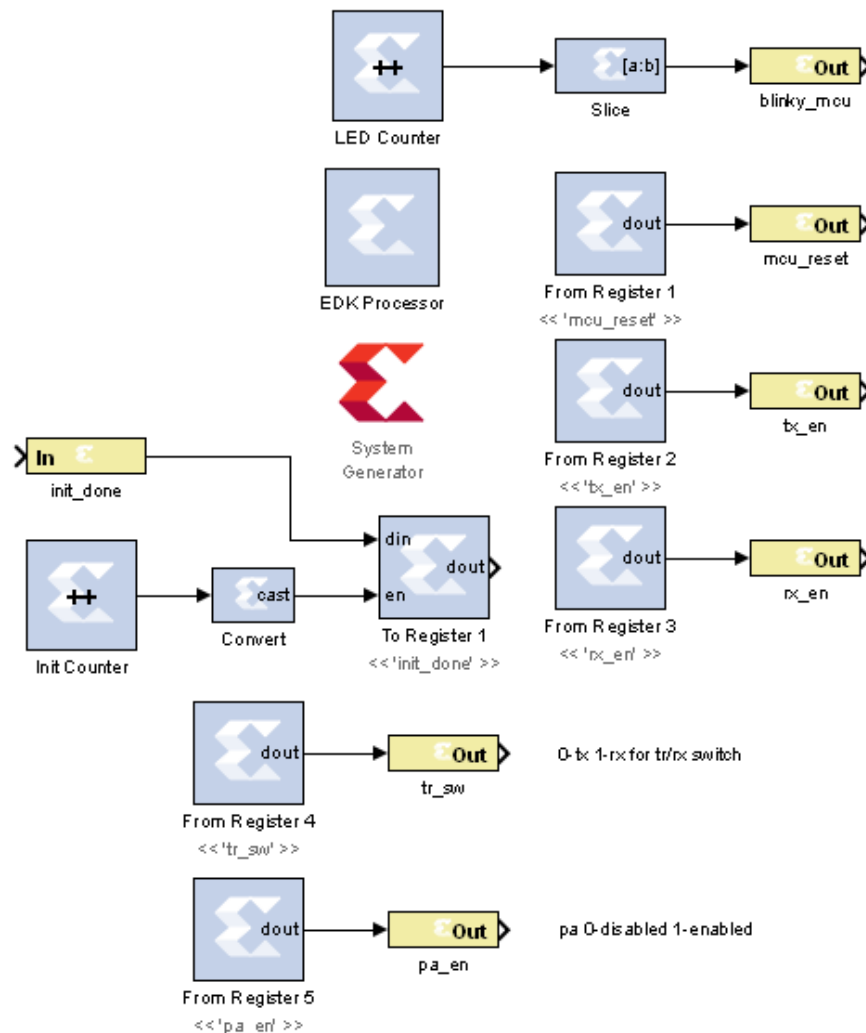


Figure 2-1: Simulink model for MCU control

² This model can be downloaded from https://github.com/Toyon/Chilipepper/tree/master/Labs/Lab_7/sysgen

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1. To create a new Simulink model, open MATLAB and click on the **Simulink Library** button in the Home menu.
2. Select **File → New → Model**
3. **Configure** this model and the system generator the same as in Lab 1, and **save** the design into the Sysgen folder. **Be sure to change the cfg file as well to find the files in your new directory structure.** Name the file **mcu.slx** or something similar.



2.2 Create Receiver Simulink Design

The **Simulink model**³ In Figure 2-2 will be used for receiving the ADC output and sending the data to ChipScope for extraction.

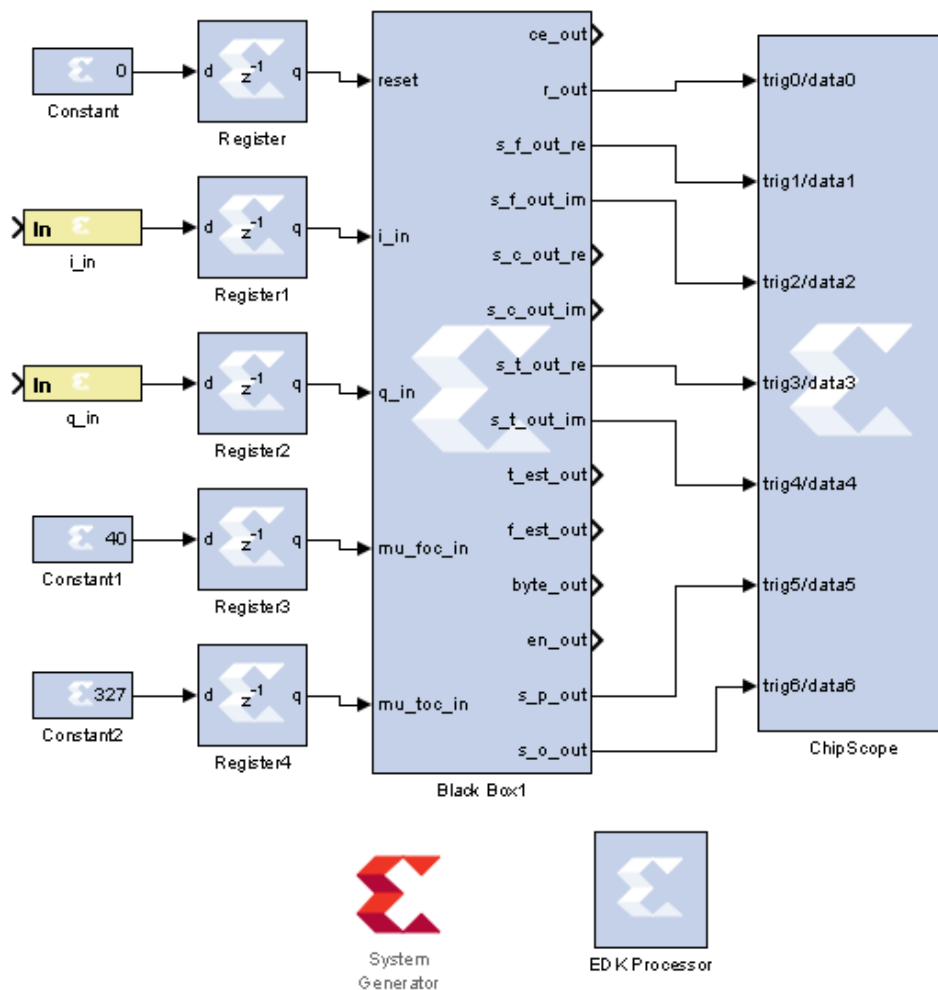


Figure 2-2: Simulink model for receiving DC Offset output

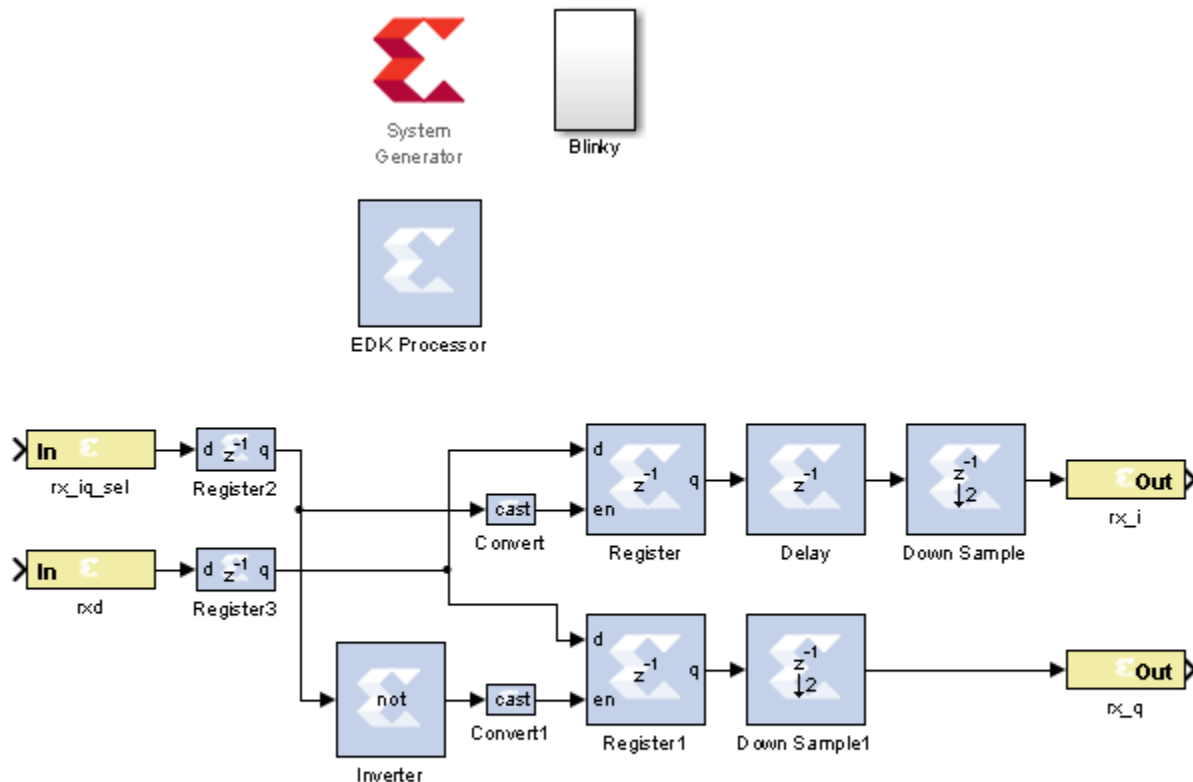
³ This model can be downloaded from https://github.com/Toyon/Chilipepper/tree/master/Labs/Lab_7/sysgen

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1. **Modify** the Simulink model `rx.slx` created earlier to look similar to Figure 2.2.
2. Both `i_in` and `q_in` should be signed 12 bit (0 decimal bits) inputs. The constant for `mu_foc_in` should be set to `floor(.01*2^12)` and for `mu_toc_in` should be `floor(.01*8*2^12)`.
2. **Save** the design into the Sysgen folder. **Be sure to change the cfg file as well to find the files in your new directory structure.** Name the file `rx.slx` or something similar.

2.3 Create ADC driver Simulink Design

The **Simulink model**⁴ In Figure 2-3 will be used for creating the signals which drive the **ADC** on Chilipepper.



By default inphase is IQ_sel high and quadrature is IQ_sel low

This core runs at 40 MHz and demultiplexes the rx_d data into two 20 MHz streams for I and Q

Figure 2-3: Simulink model for ADC control

⁴ This model can be downloaded from https://github.com/Toyon/Chilipepper/tree/master/Labs/Lab_7/sysgen

1. **Create** a new Simulink model and add the components from the Simulink blockset.
2. The white box labeled “Blinky” is simply a subsystem of the **Counter Slice** and LED **Gateway Out** blocks. The Blocks used for this subsystem are shown in Figure 2-4. Configure the Blinky subsystem identically to the other LED out systems in the previous labs.

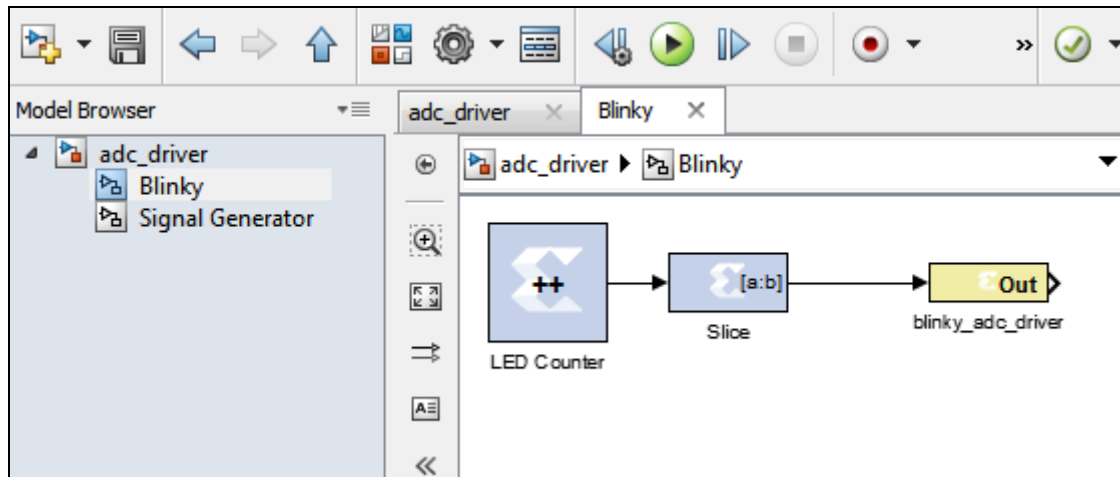


Figure 2-4: Blinky Subsystem

2.4 DC Offset Core

The last **Simulink model**⁵ needed for this FPGA design is the DC Offset model created in a previous lab. For your reference this model is shown in Figure 2-5 below.

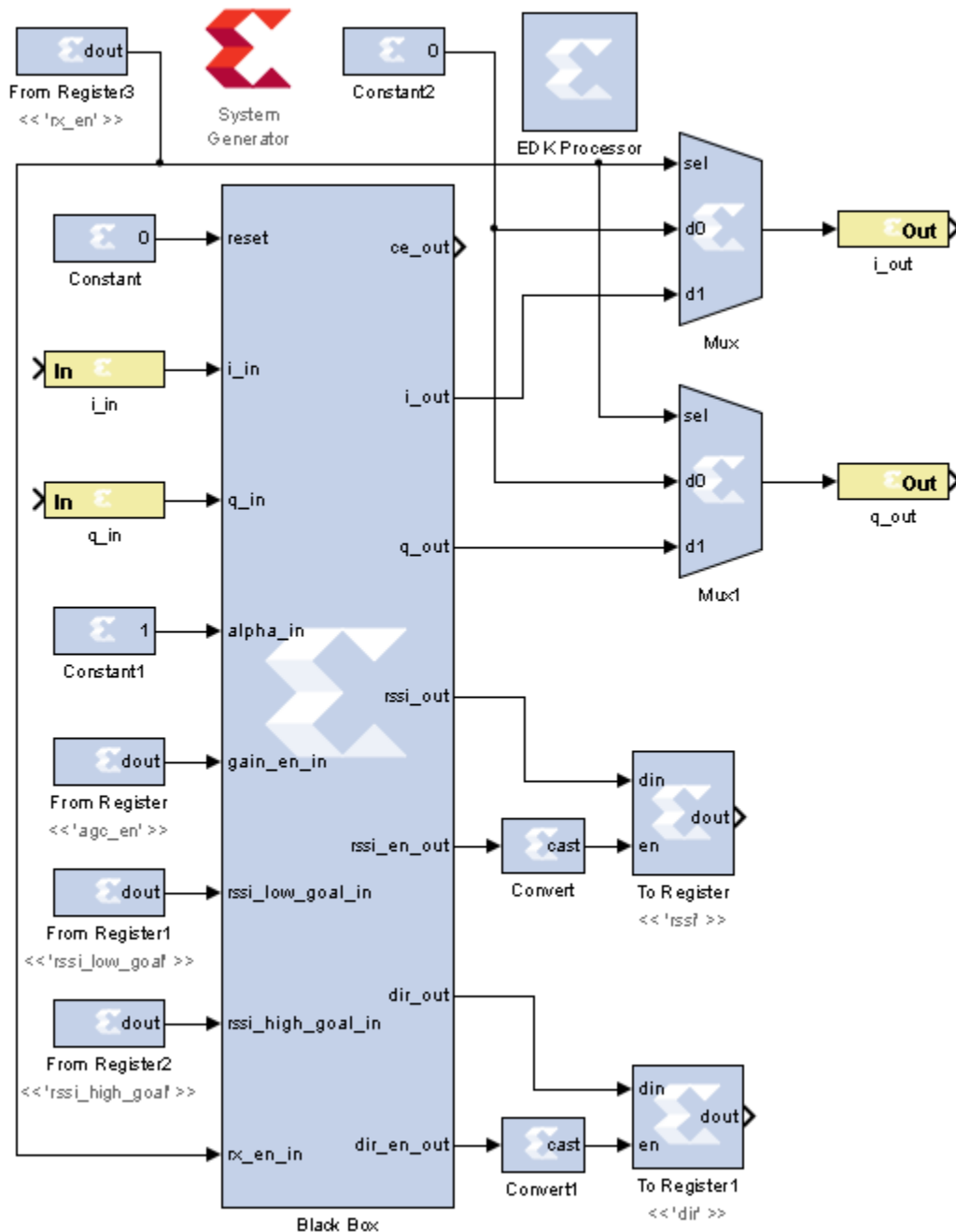


Figure 2-5: Simulink model for receiving ADC output and applying DC Offset Correction

⁵ This model can be downloaded from https://github.com/Toyon/Chilipepper/tree/master/Labs/Lab_7/sysgen

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1. Copy the `DC_Offset` Simulink files into your new project directory.

Note

Be sure to copy the vhd and config files to the new directory. You may use the Simulink files on the GitHub Repo as a reference. Additionally, you can open the old `DC_Offset` Simulink model and reconfigure its Pcore settings to point to the new EDK project directory, then recreate it.

Refer to Lab 0 Step 3 to **Create a New Blank EDK Project**. Be sure to follow the directory structure used. Once your project is created, **export** each model 1 by 1 into the newly created EDK project. Be sure your **Compilation Settings** are correct as shown in Lab 0 Section 4.1. Once each Simulink model has been exported successfully, you're ready to configure your FPGA design.

Configure Cores and Export Design

Step 3

This section will show you how to integrate your PCores into your FPGA design using EDK. There are several components that must be configured for the design of this project. A quick list of the cores needed is given below. Refer to lab 0 sections 4.3 and 5.1 for information on how to add cores to the design.

3.1 Needed IP Cores

- ADC Driver PCore created in Simulink
- MCU PCore created in Simulink
- rx PCore created in Simulink
- DC Offset PCore created in Simulink
- Clock Generator IP Core
- Processing System IP Core
- AXI Interconnect IP Core
- GPIO Cores for LEDs
- AXI_UART (Lite) Core

In addition, several of these cores will require external ports. Be sure that you have access to modifying the external port settings. Refer to Figure 3-1 Below.

Name	Connected Port	Direction	Range
+ External Ports			
+ axi_interconnect_1			
+ processing_system7_0			
+ adc_driver_axiw_0			
+ axi_gpio_led			
+ axi_uartlite_0			
+ dc_offset_axiw_0			
+ mcu_axiw_0			
+ rx_axiw_0			
+ clock_generator_0			

Figure 3-1: EDK project ports list

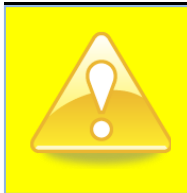
3.2 Configuring the Pcore Ports

Each of the ports used in this lab can be configured exactly as the previous labs design. Refer to Lab 5 for more information on individual port configuration.

3.3 Pin Assignments

Once the ports are configured correctly, the sysgen clock for the cores should be set as well. The last step is to setup the **pin assignments** for the external ports.

1. Rename the pins of the external ports so they are easily identifiable. Figure 2-3 shows the names used in this demo, however you don't have to use the same naming convention.
2. Open the **Project** tab.
3. Double-click on the **UCF File: data\system.ucf** from this panel, to open the constraints file.
4. Fill in the pin out information for your design using Figure 3-2 below as a reference.



Be sure that the **orientation** of the `RXD` pins is set correctly. If you follow the pin list in the figure above, you must **reverse** the `RXD` pins in the external ports assignment section. This is done using the same method used in Lab 0 Section 5.2 for the LEDs.

5. Prior to EDK version 14.4, Xilinx had a [documented issue](http://www.xilinx.com/support/answers/51739.htm)⁶ with AXI-bus generation for Simulink PCores targeting the Zynq FPGA. Refer to this issue for more information. As in Lab 0 section 5.2, this bug must be corrected if your **EDK version is 14.3 or lower**. The steps to perform are identical to those in the previous labs; however they must be performed for **all** of the PCores used in this lab.
6. Select the **Export Design** button from the navigator window on the left. Click the **Export and Launch SDK** button. This process may take awhile.

⁶ Issue can be found at <http://www.xilinx.com/support/answers/51739.htm>

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```
##### PL clocks and reset #####
NET clock_generator_0_pll_pin          LOC = D18 | IOSTANDARD = LVCMOS25;
NET clock_generator_0_pll_pin          TNM_NET = clock_generator_0_pll;
TIMESPEC TS_clock_generator_0_pll = PERIOD clock_generator_0_pll 40.000 MHz;

##### Rx – FMC interface at 2.5V #####
NET clock_generator_0_rx_clk_pin        LOC = J18          | IOSTANDARD = LVCMOS25 | DRIVE = 4 | SLEW = FAST;
NET adc_driver_axiw_0_rx_iq_sel_pin     LOC = N19          | IOSTANDARD = LVCMOS25;
NET adc_driver_axiw_0_rxd_pin[0]        LOC = M21          | IOSTANDARD = LVCMOS25;
NET adc_driver_axiw_0_rxd_pin[1]        LOC = J21          | IOSTANDARD = LVCMOS25;
NET adc_driver_axiw_0_rxd_pin[2]        LOC = M22          | IOSTANDARD = LVCMOS25;
NET adc_driver_axiw_0_rxd_pin[3]        LOC = J22          | IOSTANDARD = LVCMOS25;
NET adc_driver_axiw_0_rxd_pin[4]        LOC = T16          | IOSTANDARD = LVCMOS25;
NET adc_driver_axiw_0_rxd_pin[5]        LOC = P20          | IOSTANDARD = LVCMOS25;
NET adc_driver_axiw_0_rxd_pin[6]        LOC = T17          | IOSTANDARD = LVCMOS25;
NET adc_driver_axiw_0_rxd_pin[7]        LOC = N17          | IOSTANDARD = LVCMOS25;
NET adc_driver_axiw_0_rxd_pin[8]        LOC = J20          | IOSTANDARD = LVCMOS25;
NET adc_driver_axiw_0_rxd_pin[9]        LOC = P21          | IOSTANDARD = LVCMOS25;
NET adc_driver_axiw_0_rxd_pin[10]       LOC = N18          | IOSTANDARD = LVCMOS25;
NET adc_driver_axiw_0_rxd_pin[11]       LOC = J16          | IOSTANDARD = LVCMOS25;

##### MCU Interface #####
NET clock_generator_0_tx_clk_pin        LOC = C17          | IOSTANDARD = LVCMOS25 | DRIVE = 4 | SLEW = FAST;

##### MCU Interface #####
NET axi_uartlite_0_RX_pin              LOC = R19          | IOSTANDARD = LVCMOS25 | DRIVE = 4 | SLEW = FAST;
NET axi_uartlite_0_TX_pin              LOC = L21          | IOSTANDARD = LVCMOS25 | DRIVE = 4 | SLEW = FAST;
NET mcu_axiw_0_mcu_reset_pin           LOC = K20          | IOSTANDARD = LVCMOS25 | DRIVE = 4 | SLEW = FAST;
NET mcu_axiw_0_tx_en_pin               LOC = D22          | IOSTANDARD = LVCMOS25 | DRIVE = 4 | SLEW = FAST;
NET mcu_axiw_0_tr_sw_pin               LOC = D20          | IOSTANDARD = LVCMOS25 | DRIVE = 4 | SLEW = FAST;
NET mcu_axiw_0_rx_en_pin               LOC = C22          | IOSTANDARD = LVCMOS25 | DRIVE = 4 | SLEW = FAST;
NET mcu_axiw_0_pa_en_pin               LOC = E21          | IOSTANDARD = LVCMOS25 | DRIVE = 4 | SLEW = FAST;
NET mcu_axiw_0_init_done_pin           LOC = K19          | IOSTANDARD = LVCMOS25;

##### LEDs #####
NET axi_gpio_led_GPIO0_IO_pin          LOC = T22 | IOSTANDARD=LVCMOS33; # "LD0"
NET axi_gpio_led_GPIO2_IO_pin          LOC = T21 | IOSTANDARD=LVCMOS33; # "LD1"
NET mcu_axiw_0_blinky_mcu_pin          LOC = U22 | IOSTANDARD=LVCMOS33; # "LD2"
NET adc_driver_axiw_0_blinky_adc_driver_pin LOC = U21 | IOSTANDARD=LVCMOS33; # "LD3"
NET clock_generator_0_LOCKED_pin        LOC = V22 | IOSTANDARD=LVCMOS33; # "LD4"
```

Figure 3-2: EDK project pin assignments

Create software project

Step 4

Once the design is compiled and exported, you'll be greeted with a screen asking you where you would like to store your software project. It is very helpful to create the workspace folder in the same directory as your Sysgen and EDK folders. Doing this will keep all relevant files in the same location.

4.1 Creating a new C Project

This section will show you how to create a C program to test your receive tone project.

1. Select **File** → **New** → **Application Project**.
2. Name the project `qpsk_rx` or something similar and leave the other settings at their defaults. Be sure to select **Hello World** from the **Select Project Template** section.
3. Click **Finish**. You should now see your project folder, as well as a **board support package** (bsp) folder.
4. If you navigate into the project folder, and into the src folder, you should see a `helloworld.c` file. This is the file we will be using to create our software design. Feel free to give the file a more descriptive name such as `main.c` or something similar.
5. **Double click** the file to open it and **replace** all of its contents with the code in Figure 4-1.

Note

It would be helpful if you have completed the Embedded System Design tutorial in the *ZedBoard AP SoC Concepts Tools and Techniques Guide*. Refer to Lab 1 for more information on the MCU signal control using C code within SDK.

Creating Wireless Transceivers Using MATLAB to HDL translation and Toyon Chilipepper

```

#include <stdio.h>
#include "platform.h"
#include "xbasic_types.h"
#include "xgpio.h"
#include "xparameters.h"
#include "xstatus.h"
#include "chilipepper.h"
#include "xuartps.h"
#include "xil_printf.h"
#include "xscugic.h"
#include "xil_exception.h"

XGpio gpio_blinky;
int SetupPeripherals( void );

int main()
{
    int gain;
    int aliveLed = 0;
    static int BlinkCount = 0;
    init_platform();
    if(SetupPeripherals() != XST_SUCCESS)
        return -1;

    if ( Chilipepper_Initialize() != 0 )
        return -1;

    Chilipepper_SetPA( 1 );
    Chilipepper_SetTxRxSw( 1 ); // 0- transmit, 1-receive
    while (1)
    {
        gain = Chilipepper_ControlAgc(); //update the Chilipepper AGC
        BlinkCount += 1;
        if (BlinkCount > 500000)
        {
            if (aliveLed == 0)
                aliveLed = 1;
            else
                aliveLed = 0;
            BlinkCount = 1;
            XGpio_DiscreteWrite(&gpio_blinky, 2, aliveLed); //blink LEDs
            XGpio_DiscreteWrite(&gpio_blinky, 1, ~aliveLed);
        }
    }
    cleanup_platform();
    return 0;
}

int SetupPeripherals( void )
{
    XGpio_Initialize(&gpio_blinky, XPAR_AXI_GPIO_LED_DEVICE_ID);
    XGpio_SetDataDirection(&gpio_blinky, 2, 0);
    XGpio_SetDataDirection(&gpio_blinky, 1, 0);
    XGpio_DiscreteWrite(&gpio_blinky, 1, 0);
    XGpio_DiscreteWrite(&gpio_blinky, 2, 0);
    return XST_SUCCESS;
}

```

Figure 4-1: Code outline for SDK project

4.2 Adding Supporting files

In addition to the main c file, you need the library files for the Chilipepper board. The 2 required files for this Lab are Chilipepper.c and Chilipepper.h and can be found on the github repo. Place these files in the src directory of your project workspace.

1. [Chilipepper.c](#) – This file is the primary library file for the Chilipepper board. It contains functions for modifying the MCU registers as well as basic helper functions for tasks such as initialization, transmitting, and receiving.
2. [Chilipepper.h](#) – This file holds the function prototypes for the Chilipepper.c functions.

Note

In addition to the Library files, you also need to include a Math library which contains the `pow` function that is used when creating the CRC. See Lab 3 section 4.1 for more information on how to add the Math Library to your project.

The Chilipepper.c library file is configured for both TX and RX cores as well as a UART to talk to the on board MCU and configure its settings. To use the library file properly, you must specify which of these features you will use. To do this, modify lines 8-12 of the Chilipepper.c file to define a variable for the cores you will be using. Your code should resemble the following, as we will be using all cores except the TX_DRIVER for this Lab.

```
#define MCU_UART
#define MCU_DRIVER
#define DC_OFFSET
//#define TX_DRIVER
#define RX_DRIVER
```



If you are still not able to compile your C design due to include errors, you may need to tell SDK where your PCore drivers are stored. If you click on Xilinx Tools → Repositories, you can specify (in Global Repositories) where the EDK directory of your project is. (This will need to be changed for each new project)

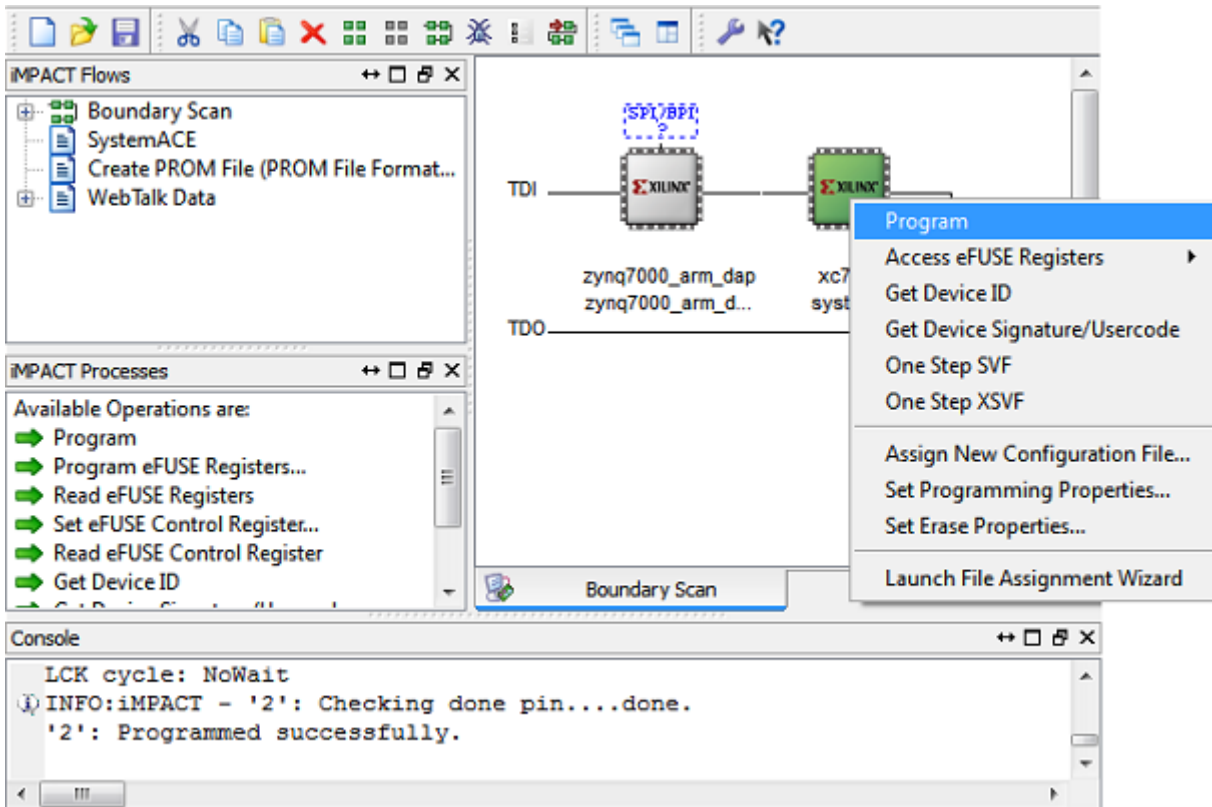
4.3 Loading Hardware Platform with iMPACT

Once your program is written and compiled you are ready to test the design! This is done by programming the FPGA with your hardware descriptions defined in the bit file generated in EDK, and running your software on top of this design. For this lab, you can verify your design by connecting two Chilipepper boards together using an attenuator. On one board, you should run the latest version of Lab 3 which allows you to either send a single packet via button press, or multiple packets using the switch on the FPGA.

1. Connect the Chilipepper to the FPGA board and verify all cables are connected properly and the jumper settings are correct. Verify this by using the *Chilipepper user guide* and the *ZED Board Hardware users guide* as a reference. Also See Lab 0 for details on Jumper Configuration.
2. Once the FPGA and radio board are connected correctly, turn on the board.
3. Open iMPACT in the ISE Design tools.
4. Select no if Impact asks you to load the last saved project.
5. Select yes to allow iMPACT to automatically create a new project for you. If you receive any connection errors, verify your USB or JTAG programmer cables are connected properly.
6. Select the Automatic option for the JTAG boundary scan setting and click ok.
7. Hit yes to assign configuration files. Bypass the first file selection, but for the second selection, browse to the location of your system.bit file. It should be inside the "Implementation" folder of your EDK project folder.
8. Select ok on the next screen verifying that the board displayed is your Zynq xc7z020 board. It should look similar to Figure 4-2 below.
9. Right click on the xc7z020 board icon (should be on the right), select program and hit ok.

Note

If you are running lab 3 from a second PC, you will need to repeat this process for the second board using the Lab 3 system.bit file. Alternatively, you can run Lab 3 directly from the SD card by loading a standard SD card with the Boot.bin file for lab 3, which can be found on the github repo.



4-2: iMPACT configuration screen

To load Lab 3 via SD card:

1. Place the file on the SD card, and place the card inside the SD slot of the FPGA.
2. Configure the jumpers on the FPGA as shown in Figure 4-3.
3. Turn on the board, and the program should load after about 30 seconds. Check for the blue light, indicated the load was successful.

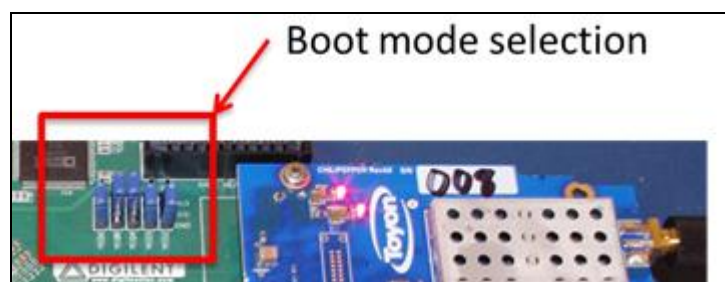



Figure 4-3: Jumper configuration needed to load a project via SD card

4.4 Debugging with SDK

If the hardware design is correct, you should see the LEDs start blinking on the board, as well as a blue light indicating the program was successful. You should also see the LED blinking on the second FPGA indicating the Lab 3 project is working properly. You can now return to the SDK project screen to test your software.

1. Test it by **right clicking** the project name folder and selecting **Debug As → Launch on Hardware**.
2. You should now be taken to a screen which shows the first pointer initialization as highlighted. You can now start the software program by clicking the  (play) button in the top menu.


If the software initialization worked, you should see a green light on the Chilipepper as well as LED0 and LED1 blinking alternatively.

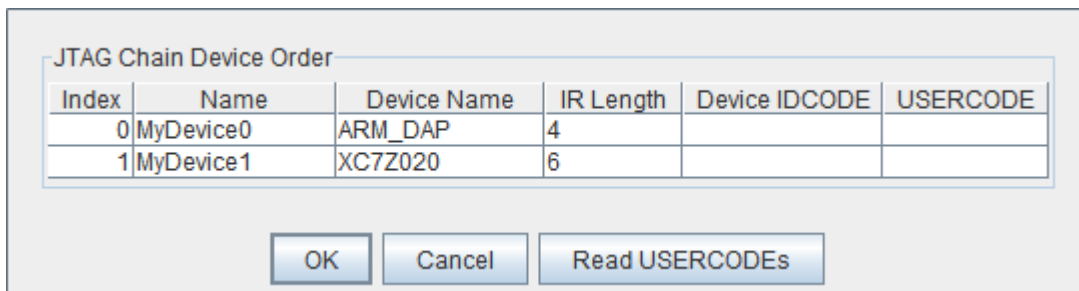
Testing and Design Verification

Step 5

5.1 Verification with ChipScope Pro

There are several methods available for verifying the received QPSK transmission. This lab focuses on verification using ChipScope Pro, as well as exporting to MATLAB for further analysis.

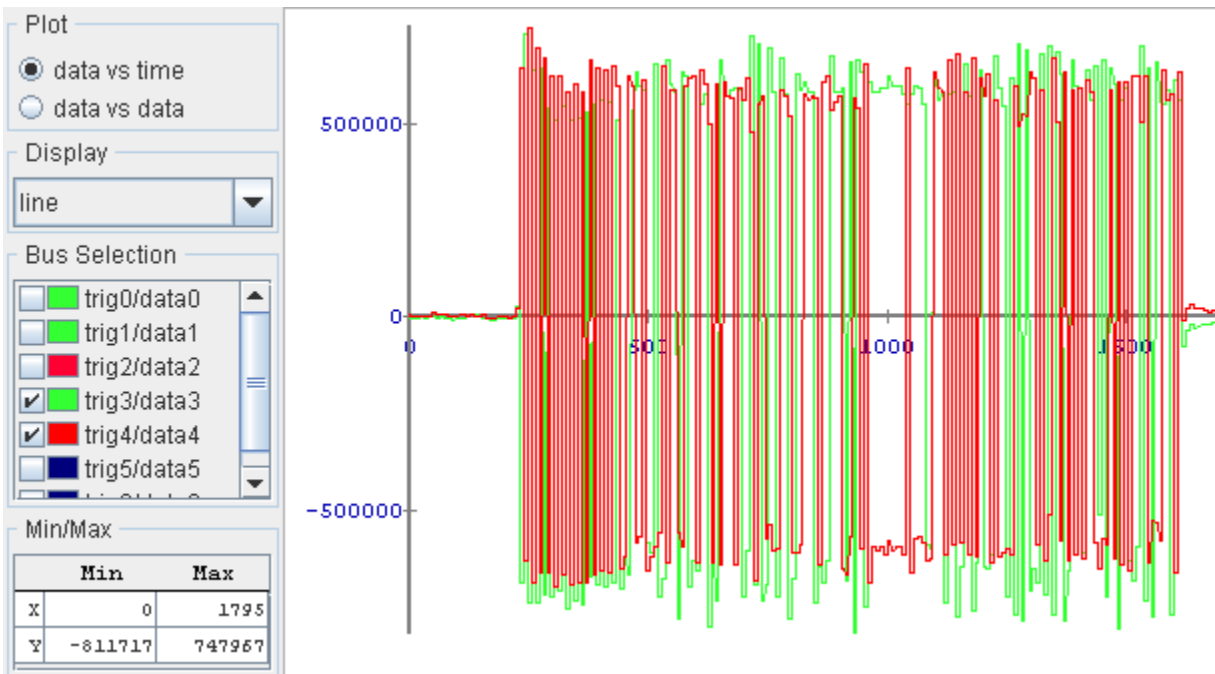
1. To verify the received signal, you will need to open **ChipScope Pro Analyzer**. Be sure that the JTAG cable is connected to the FPGA board properly (or the 6 pin output of the Chilipepper).
2. Once the program opens, click the  (open cable) button to open your JTAG connection to the board. If your jumpers are configured correctly, you should see the following devices on the cable.



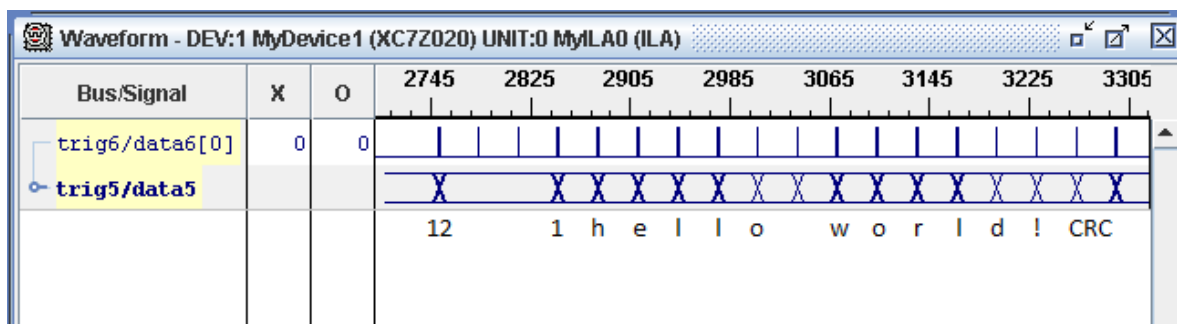
3. Select ok to get to the Analyzer main screen. Open the file menu and select **Import**.
4. Click **Select New File**, and browse to the location of your ChipScope **CDC file**, which is located in the Sysgen/netlist folder of your project directory. This file was created for you when you generated your PCores from your Simulink Model design. It tells the ChipScope program how to interpret the data it is receiving from the JTAG port.
5. Next double click on the **bus plot** option in the New Project menu in the top left hand side of the screen. This will open a window which allows you to view a signal **value vs. time** plot of your waveforms.
6. Under Data Port in the Signals Dev menu on the left side of the screen, right click on the trig4/data4 and trig5/data5 ports, and change their **bus radix** to **signed decimal**. Click OK to accept the default decimal values.
7. On the Bus Plot screen, you can change the color of each of the signals to get a better view of each individual signal. Click the **check box** next to any of the signals you wish to see on the plot.

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8. To correctly view the received signal in ChipScope, you must catch the signal in the window which is currently being viewed in ChipScope. This is much easier to do if you flip the switch on the Lab 3 demo to allow for continuous packet transmission.
9. Click the **play button** in the top menu bar until you get a full display of the signal. Additionally you can set up triggering options for periodic or continuous playback of the received signal. Your received signal should look similar to Figure 5-1 below.



5-1: both i and q channels of the QPSK waveform in ChipScope Pro



5-2: Received packet from Lab 3 QPSK transmit after correlation.

As you can see clearly from Figure 5-2, the `en_out` out line goes high when a new byte is ready, and the `byte_out` then has the correlated data, whose value is shown in the area below. Zooming into the ChipScope Waveform plot can verify this. Be sure you set the radix to ASCII if you want to see the actual character transmitted.

5.2 Exporting into MATLAB

Now that you have verified the received signal, you can get a pretty good idea of what your QPSK waveform looks like. However, ChipScope allows you to export the data received directly into MATLAB for further analysis.

1. It will be helpful later in your MATLAB code if you rename your **Data Port variables**. Right click on the Ports, and **change the names** to something more descriptive, such as `real_out` ... `byte_out`, `en_out`, `s_p_out`, `s_o_out`, etc. respectively. If needed, you can use the Simulink model to find which signal each port has.
2. Set the radix of your `byte_out` data to signed decimal before you export it to MATLAB. Also select the check box next to the signals you want to export in ChipScope Bus Plot. For verification of the packet you only need the `byte_out` output.
3. Open the file menu and select **Export**.
4. Click the **ASCII** radio box, select **Bus Plot Buses** under Signals to export, and then click **export**.
5. It is recommended that you save this file into the project directory with your MATLAB files. Call it something descriptive such as **rx_data.prn**.

5.3 MATLAB Analysis

The last step is to verify the correctness of the rx PCore by verifying the received bytes from the rx correlator. The rx module designed earlier in MATLAB returns the Byte and Byte_en outputs which should be enough to verify that the packet was received correctly. Therefore, we would expect that decoding the payload of these bytes should correctly display the transmitted ASCII message.

1. Verify correlator functionality by running the following MATLAB script. You may have to change the load values depending on which variables you exported from ChipScope.

Creating Wireless Transceivers Using MATLAB to HDL translation and Toyon Chilipepper

```

fid = fopen('rx_data.prn');
M = textscan(fid, '%d %d %d %d %d', 'Headerlines', 1);
fclose(fid);
i_out_toc = double(cell2mat(M(3)));
q_out_toc = double(M{4});
byte_array = double(M{5});
byte_array = byte_array';

figure(1)
subplot(1,2,1)
scatter(i_out_toc, q_out_toc)
title('Scatter Plot of rx with TOC');
subplot(1,2,2)
plot(i_out_toc);
title('Signal Post TOC (real part)');

[a,b,bytes] = find(byte_array);

numRecBytes = bytes(1)
%+2 represents number of header bits
msgBytes = bytes((1+2):(numRecBytes+2));

native2unicode(msgBytes)

```

Your plot and output should look similar to Figures 5-3 and 5-4 below.

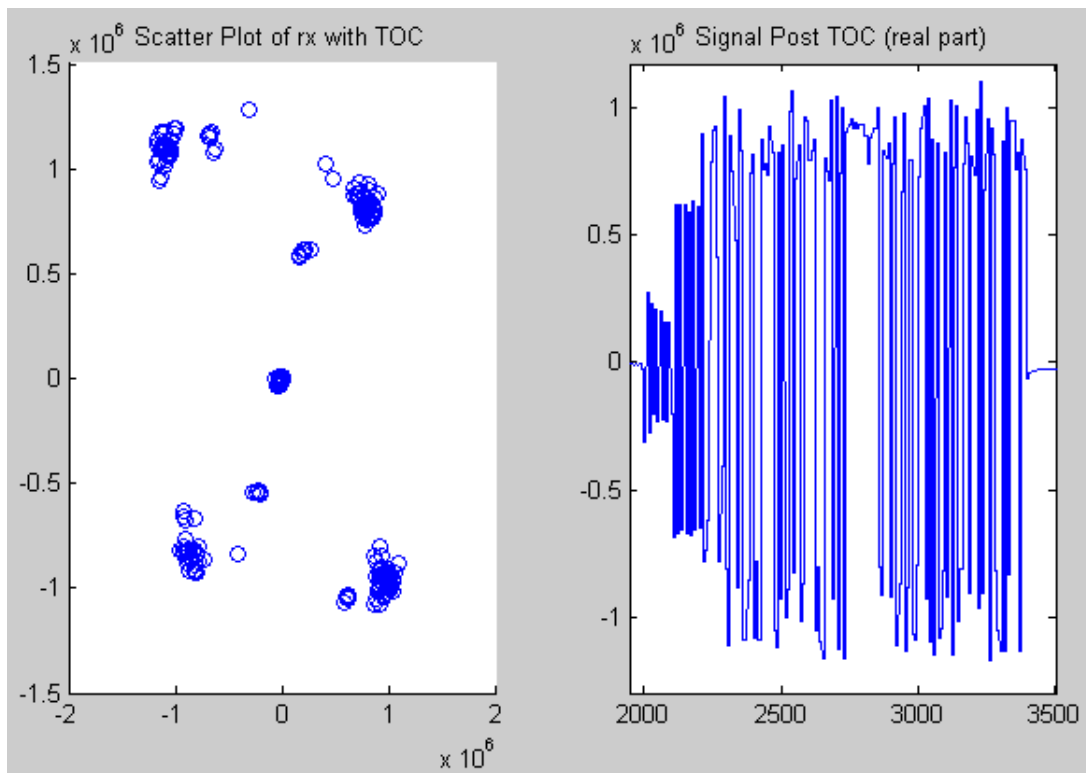



Figure 5-3: Scatter Plot of the transmitted and received QPSK waveform post timing Offset Correction.



```
Command Window
>> rx_analysis

numRecBytes =

    12

ans =

hello world!
```

5-4: result of the byte_out output from the QPSK Packet.

Appendix A MATLAB Correlation Function

MATLAB function qpsk_rx_correlation.m

```

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% QPSK demonstration packet-based transceiver for Chilipepper
% Toyon Research Corp.
% http://www.toyon.com/chilipepper.php
% Created 10/17/2012
% embedded@toyon.com
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% There are two major goals with this core. The first is to find the peak
% of the training sequence and then to subsequently pull out and pack the
% bits. The number of bytes transmitted is in the packet so we extract this
% to determine how many bytes to pull out.
% The second goal is to send these bytes off to the Microblaze processor.
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%#codegen
function [byte_out, en_out, s_out, o_out] = ...
    qpsk_rx_correlator(s_i_in, s_q_in)

    persistent counter
    persistent sBuf_i sBuf_q
    persistent oLatch sLatch
    persistent q detPacket
    persistent ip op
    persistent bits symCount byteCount numBytes
    t_i = TB_i;
    t_q = TB_q;
    OS_RATE = 8;
    BIT_TO_BYTE = [1 2 4 8 16 32 64 128]';

    if isempty(counter)
        counter = 0;
        sBuf_i = zeros(1,65);
        sBuf_q = zeros(1,65);
        sLatch = 0;
        oLatch = 0;
        q = 0;
        detPacket = 0;
        ip = 0; op = 0;
        bits = zeros(1,8);
        symCount = 0;
        byteCount = 0;
        numBytes = 1000;
    end
    byte_out = 0;
    en_out = 0;
    % found a packet, now we're ready to write the data out
    if counter == 0 && detPacket == 1

```


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```

    if s_i_in < 0
        sHard_i_t = -1;
    else
        sHard_i_t = 1;
    end
    if s_q_in < 0
        sHard_q_t = -1;
    else
        sHard_q_t = 1;
    end
    sHard_i = 0; sHard_q = 0;
    switch q
        case 0
            sHard_i = sHard_i_t;
            sHard_q = sHard_q_t;
        case 1
            sHard_i = sHard_q_t;
            sHard_q = -sHard_i_t;
        case 2
            sHard_i = -sHard_i_t;
            sHard_q = -sHard_q_t;
        case 3
            sHard_i = -sHard_q_t;
            sHard_q = sHard_i_t;
    end
    sLatch = sHard_i;
    oLatch = 1;
    bits(symCount*2+1) = (sHard_i+1)/2;
    bits(symCount*2+2) = (sHard_q+1)/2;

    symCount = symCount + 1;
    if symCount >= 4
        byteCount = byteCount + 1;
        symCount = 0;
        byte_out = bits*BIT_TO_BYTE;
        en_out = 1;
        % first byte is number of bytes in payload
        if byteCount == 1
            numBytes = byte_out;
        end
        % if we exceed the packet ID
        if byteCount > 3
            % exit if we've written all the bytes or above reasonable
            % threshold
            if byteCount == numBytes+6 || byteCount > 256
                detPacket = 0;
                counter = 1;
            end
        end
    end
end
end
end
%let's see if we can find a packet. only do so if MCU is ok to rcv packet
if counter == 0 && detPacket == 0

```

Creating Wireless Transceivers Using MATLAB to HDL translation and Toyon Chilipepper

```

    sLatch = 0;
    if s_i_in < 0
        ss_i = -1;
    else
        ss_i = 1;
    end
    if s_q_in < 0
        ss_q = -1;
    else
        ss_q = 1;
    end

    sBuf_i = [sBuf_i(2:end) ss_i];
    sBuf_q = [sBuf_q(2:end) ss_q];

    sc_iWithi = sBuf_i*t_i;
    sc_iWithq = sBuf_i*t_q;
    sc_qWithi = sBuf_q*t_i;
    sc_qWithq = sBuf_q*t_q;

    ip = abs(sc_iWithi)+abs(sc_qWithq);
    op = abs(sc_iWithq)+abs(sc_qWithi);

    % we found a packet. While we have frequency offset lock we don't
    % know the phase offset. Here we use the inphase and quadrature
    % phasing to determine how to rotate around the circle
    if ip > 100 % 0 or 180 angle
        if sc_iWithi > 10 && sc_qWithq > 10
            q = 0; % 0 degrees
        else
            q = 2; % 180 degrees;
        end
        detPacket = 1;
    end
    if op > 100
        if sc_iWithq > 10 && sc_qWithi < 10
            q = 3; % 90 degrees
        else
            q = 1; % 270 degrees;
        end
        detPacket = 1;
    end
    oLatch = ip+op;
    symCount = 0;
    byteCount = 0;
    numBytes = 1000;
end
s_out = sLatch;
o_out = oLatch;
counter = counter + 1;
if counter >= OS_RATE % only pull data once every OS_RATE clocks
    counter = 0;
end
end
end

```

Appendix B MATLAB Test Bench

MATLAB script qpsk_tb.m

```

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Model/simulation parameters
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
sim=1;
OS_RATE = 8;
SNR = 1;
fc = 10e3/20e6; % sample rate is 20 MHz, top is 10 kHz offset
muFOC = floor(.01*2^12)/2^12;
muTOC = floor(.01*8*2^12)/2^12;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Initialize LUTs
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
make_src_lut;
make_train_lut;
make_trig_lut;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
if (sim)
    %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    % Emulate microprocessor packet creation
    %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    % data payload creation
    messageASCII = 'Hello World!';
    message = double(unicode2native(messageASCII));
    % add on length of message to the front with four bytes
    msgLength = length(message);
    messageWithNumBytes = [ ...
        mod(msgLength,2^8) ...
        mod(floor(msgLength/2^8),2^8) ...
        mod(floor(msgLength/2^16),2^8) ...
        1 ... % message ID
        message];
    % add two bytes at the end, which is a CRC
    messageWithCRC = CreateAppend16BitCRC(messageWithNumBytes);
    m1 = length(messageWithCRC);
    %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

    %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    % FPGA radio transmit core
    %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
    data_in = 0;
    empty_in = 1;
    tx_en_in = 0;
    numBytesFromFifo = 0;
    num_samp = m1*8*2*2*3;
    x = zeros(1,num_samp);
    CORE_LATENCY = 4;

```

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```

data_buf = zeros(1,CORE_LATENCY);
empty_buf = ones(1,CORE_LATENCY);
clear_buf = zeros(1,CORE_LATENCY);
tx_en_buf = zeros(1,CORE_LATENCY);
for i1 = 1:num_samp
    % first thing the processor does is clear the internal tx fifo
    if i1 == 1
        clear_fifo_in = 1;
    else
        clear_fifo_in = 0;
    end

    if i1 == 5 % wait a little bit then begin to load the fifo
        empty_in = 0;
        numBytesFromFifo = 0;
    end

    data_buf = [data_buf(2:end) data_in];
    empty_buf = [empty_buf(2:end) empty_in];
    clear_buf = [clear_buf(2:end) clear_fifo_in];
    tx_en_buf = [tx_en_buf(2:end) tx_en_in];
    [i_out, q_out, re_byte_out, tx_done_out, d1, d2, d3] = ...
        qpsk_tx(data_buf(1),empty_buf(1),clear_buf(1),tx_en_buf(1));
    x_out = complex(i_out,q_out)/2^11;
    x(i1) = x_out;

    %% Emulate read FIFO AXI interface
    if re_byte_out == 1 && numBytesFromFifo < length(messageWithCRC)
        data_in = messageWithCRC(numBytesFromFifo+1);
        numBytesFromFifo = numBytesFromFifo + 1;
    end
    % processor loaded all bytes into FIFO so begin transmitting
    if numBytesFromFifo == length(messageWithCRC)
        empty_in = 1;
        tx_en_in = 1;
    end
end

index = find(abs(x) > sum(SRRC))+24*8; % constant is pad bits
offset = index(1)+6+length(TB_i)*OS_RATE;
idx = offset:8:(offset+8*ml*4-1);
y = x(idx); % four symbols per byte of data
sc = zeros(1, (msgLength+6)*8);
sc(1:2:end) = real(y);
sc(2:2:end) = imag(y);
sh = sign(sc);
sb = (sh+1)/2;
d = zeros(1,ml);
for i1 = 1:ml
    si = sb(1+(i1-1)*8:i1*8);
    d(i1) = bi2de(si);
end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

```

Creating Wireless Transceivers Using MATLAB to HDL translation and Toyon Chilipepper

```

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Emulate channel
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% pad on either side with zeros
p = complex(zeros(1,100),zeros(1,100));
xp = [p x p]; % pad
% Apply frequency offset and receive/over-the-air AWGN
y = xp.*exp(1i*2*pi*fc*(0:length(xp)-1));
rC = y/max(abs(y)).*1*2^11; % this controls receive gain
r = awgn(rC,SNR,0,1);
r1 = rC;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Load Chipscope samples
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
if (~sim)
    fid = fopen('rx.prn');
    M = textscan(fid,'%d %d %d %d','Headerlines',1);
    fclose(fid);
    is = double(M{3});
    qs = double(M{4});
    r = complex(is,qs);
end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% Main receiver core
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
r_out = zeros(1,length(r));
s_f = zeros(1,length(r));
s_t = zeros(1,length(r));
s_c = zeros(1,length(r));
f_est = zeros(1,length(r));
t_est = zeros(1,length(r));
s_p = zeros(1,length(r));
s_o = zeros(1,length(r));
byte_count = 0;
if (sim)
    bytes = zeros(1,m1);
end
for i1 = 1:length(r)+200
    if i1 > length(r)
        r_in = 0;
    else
        r_in = r(i1);
    end
    i_in = round(real(r_in));
    q_in = round(imag(r_in));
    [r_out(i1), s_f(i1), s_c(i1), s_t(i1), t_est(i1), f_est(i1), ...
        byte, en, s_p(i1), s_o(i1)] = ...
        qpsk_rx(i_in, q_in, floor(muFOC*2^12), floor(muTOC*2^12));

    if en == 1
        byte_count = byte_count + 1;
        bytes(byte_count) = byte;
    end
end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

```

```
figure(2)
subplot(2,2,1)
scatter(real(r),imag(r))
title('Pre FOC Signal');
subplot(2,2,3)
plot(real(r_out));
title('Pre FOC Signal (real part)');
subplot(2,2,2)
scatter(real(s_t),imag(s_t))
title('Post TOC Signal');
subplot(2,2,4)
plot(real(s_p));
title('Message bits');

figure(3)
axis([0 length(s_p) -1.25 1.25]);
plot(s_o);
title('Correlation magnitude');

numRecBytes = bytes(1)+bytes(2)+bytes(3);
msgBytes = bytes((1+4):(numRecBytes+4));

if (sim)
    if sum(msgBytes-message) == 0
        disp('Received message correctly');
    else
        disp('Received message incorrectly');
    end
    native2unicode(bytes);
    native2unicode(msgBytes)
end

if (~sim)
    native2unicode(msgBytes)
end
```