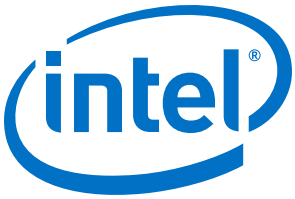

Cyclone 10 LP Advance Information Brief

AIB-01029
2017.02.13

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Contents

Cyclone 10 LP Advance Information Brief

The Intel® Cyclone® 10 LP FPGAs are designed to accommodate low static power consumption and low cost requirements for high-volume and cost-sensitive applications.

Cyclone 10 LP devices provide a high density sea of programmable gates, on-board resources, and general purpose I/Os. These resources satisfies the requirements of I/O expansion and chip to chip interfacing. The Cyclone 10 LP architecture suits smart and connected end applications across many market segments:

- Industrial and automotive
- Broadcast, wireline, and wireless
- Compute and storage
- Government, military, and aerospace
- Medical, consumer, and smart energy

The free but powerful Quartus® Prime, Lite Edition software suite of design tools meets the requirements of several classes of users:

- Existing FPGA designers
- Embedded designers using the FPGA with Nios® II processor
- Students and hobbyists who are new to FPGA

Related Links

Software Development Tools, Nios II Processor
Provides more information about the Nios II 32-bit soft IP processor and Embedded Design Suite (EDS).

Summary of Cyclone 10 LP Features

Table 1. Summary of Features for Cyclone 10 LP Devices

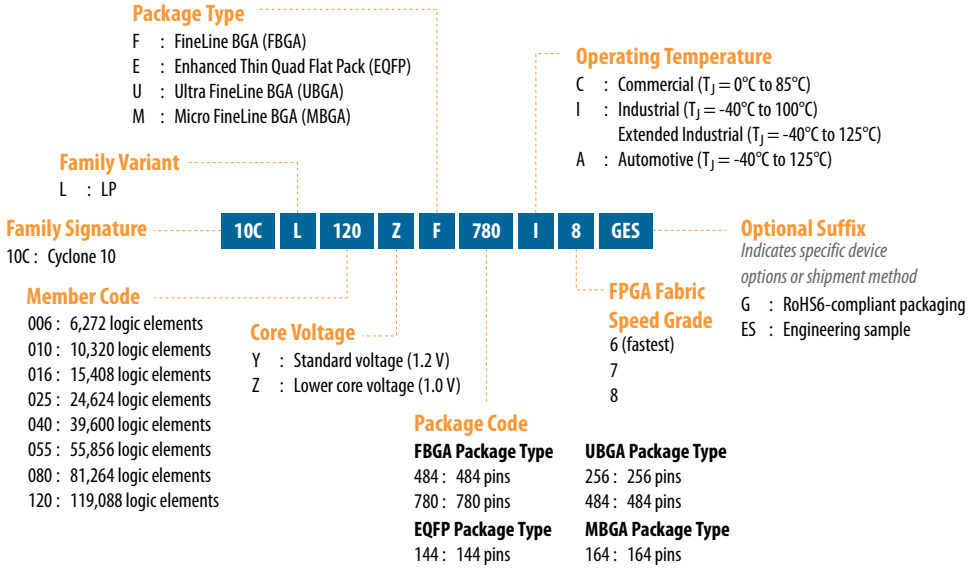
Feature	Description
Technology	• Low-cost, low-power FPGA fabric • 1.0 V and 1.2 V core voltage options • Available in commercial, industrial, and automotive temperature grades
Packaging	• Several package types and footprints: — FineLine BGA (FBGA) — Enhanced Thin Quad Flat Pack (EQFP) — Ultra FineLine BGA (UBGA) — Micro FineLine BGA (MBGA) • Multiple device densities with pin migration capability • RoHS6 compliance

continued...

Feature	Description
Core architecture	• Logic elements (LEs)—four-input look-up table (LUT) and register • Abundant routing/metal interconnect between all LEs
Internal memory blocks	• M9K—9-kilobits (Kb) of embedded SRAM memory blocks, cascadable • Configurable as RAM (single-port, simple dual port, or true dual port), FIFO buffers, or ROM
Embedded multiplier blocks	• One 18 × 18 or two 9 × 9 multiplier modes, cascadable • Complete suite of DSP IPs for algorithmic acceleration
Clock networks	• Global clocks that drive throughout entire device, feeding all device quadrants • Up to 15 dedicated clock pins that can drive up to 20 global clocks
Phase-locked loops (PLLs)	• Up to four general purpose PLLs • Provides robust clock management and synthesis
General-purpose I/Os (GPIOs)	• Multiple I/O standards support • Programmable I/O features • True LVDS and emulated LVDS transmitters and receivers • On-chip termination (OCT)
SEU mitigation	SEU detection during configuration and operation
Configuration	• Active serial (AS), active parallel (AP), passive serial (PS), fast passive parallel (FPP) • JTAG configuration scheme • Configuration data decompression • Remote system upgrade

Cyclone 10 LP Available Options

Figure 1. Sample Ordering Code and Available Options for Cyclone 10 LP Devices—Preliminary



Cyclone 10 LP Maximum Resources

Table 2. Maximum Resource Counts for Cyclone 10 LP Devices

Resource		Device							
		10CL006	10CL010	10CL016	10CL025	10CL040	10CL055	10CL080	10CL120
Logic Elements (LE)		6,272	10,320	15,408	24,624	39,600	55,856	81,264	119,088
M9K Memory	Block	30	46	56	66	126	260	305	432
	Capacity (Kb)	270	414	504	594	1,134	2,340	2,745	3,888
18 × 18 Multiplier		15	23	56	66	126	156	244	288
PLL		2	2	4	4	4	4	4	4
Clock		20	20	20	20	20	20	20	20
Maximum I/O		176	176	340	325	325	321	423	525
Maximum LVDS		65	65	137	124	124	132	178	230

Cyclone 10 LP Package Plan

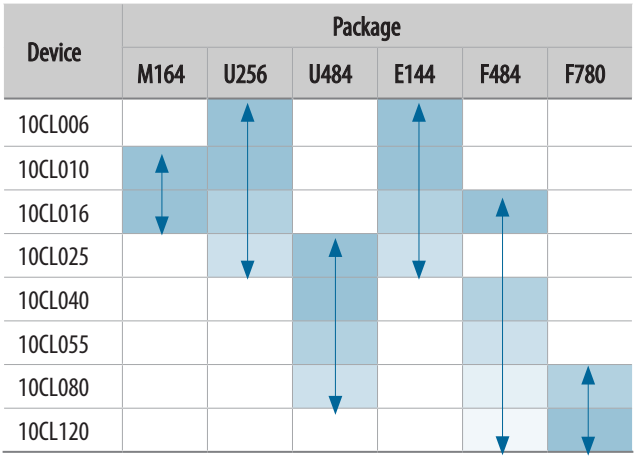
Table 3. Package Plan for Cyclone 10 LP Devices

Device	Package											
	Type	M164 164-pin MBGA		U256 256-pin UBGA		U484 484-pin UBGA		E144 144-pin EQFP		F484 484-pin FBGA		F780 780-pin FBGA	
	Size	8 mm × 8 mm		14 mm × 14 mm		19 mm × 19 mm		22 mm × 22 mm		23 mm × 23 mm		29 mm × 29 mm	
	Ball Pitch	0.5 mm		0.8 mm		0.8 mm		0.5 mm		1.0 mm		1.0 mm	
	I/O Type	GPIO	LVDS	GPIO	LVDS	GPIO	LVDS	GPIO	LVDS	GPIO	LVDS	GPIO	LVDS
10CL006		—	—	176	65	—	—	88	22	—	—	—	—
10CL010		71	22	176	65	—	—	88	22	—	—	—	—
10CL016		71	22	162	53	—	—	78	19	340	137	—	—
10CL025		—	—	150	52	325	124	76	18	—	—	—	—
10CL040		—	—	—	—	325	124	—	—	325	124	—	—
10CL055		—	—	—	—	321	132	—	—	321	132	—	—
10CL080		—	—	—	—	289	110	—	—	289	110	423	178
10CL120		—	—	—	—	—	—	—	—	277	103	525	230

Cyclone 10 LP I/O Vertical Migration

Figure 2. Migration Capability Across Cyclone 10 LP Devices

- The arrows indicate the migration paths. The devices included in each vertical migration path are shaded. Devices with lesser I/O resources in the same path have lighter shades.
- To achieve full I/O migration across devices in the same migration path, restrict I/O usage to match the device with the lowest I/O count.

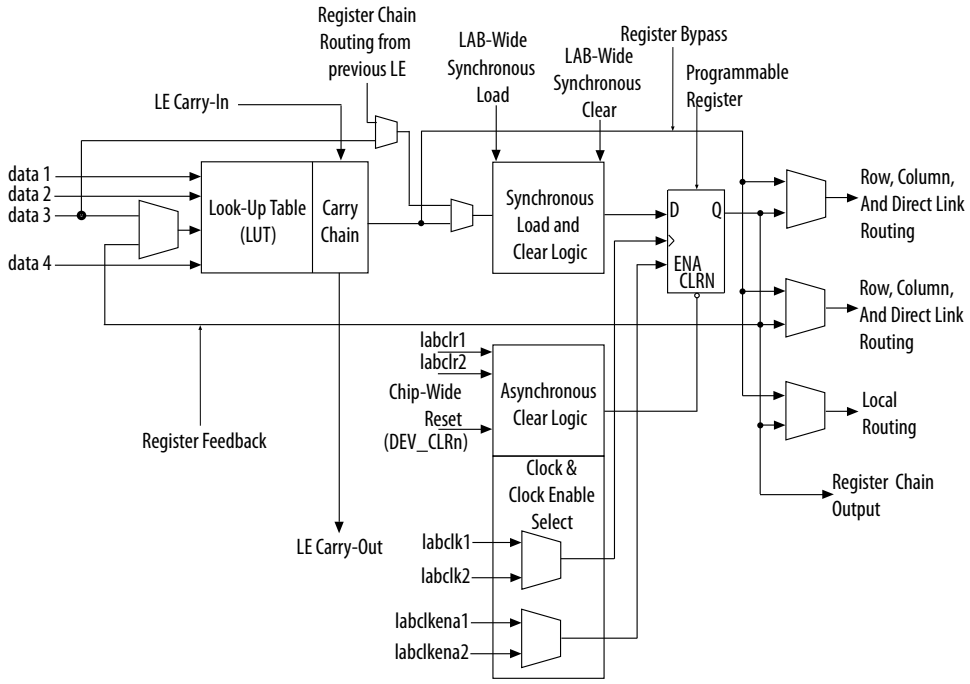


Note: To verify the pin migration compatibility, use the Pin Migration View window in the Quartus Prime software Pin Planner.

Logic Elements and Logic Array Blocks

The LAB consists of 16 logic elements (LE) and a LAB-wide control block. An LE is the smallest unit of logic in the Cyclone 10 LP device architecture. Each LE has four inputs, a four-input look-up table (LUT), a register, and output logic. The four-input LUT is a function generator that can implement any function with four variables.

Figure 3. Cyclone 10 LP Device Family LEs



Embedded Multipliers

Each embedded multiplier block in Cyclone 10 LP devices supports one individual 18 × 18-bit multiplier or two individual 9 × 9-bit multipliers. You can cascade the multiplier blocks to form wider or deeper logic structures.

You can control the operation of the embedded multiplier blocks using the following options:

- Parameterize the relevant IP cores with the Quartus Prime parameter editor
- Infer the multipliers directly with VHDL or Verilog HDL

Intel and partners offer popular DSP IPs for Cyclone 10 LP devices, including:

- Finite impulse response (FIR)
- Fast Fourier transform (FFT)
- Numerically controlled oscillator (NCO) functions

For a streamlined DSP design flow, the DSP Builder tool integrates the Quartus Prime software with MathWorks Simulink and MATLAB design environments.

Embedded Memory Blocks

The embedded memory structure consists of M9K memory blocks columns. Each M9K memory block of a Cyclone 10 LP device provides 9 Kb of on-chip memory. You can cascade the memory blocks to form wider or deeper logic structures.

You can configure the M9K memory blocks as RAM, FIFO buffers, or ROM.

Table 4. M9K Operation Modes and Port Widths

Operation Modes	Port Widths
Single port	×1, ×2, ×4, ×8, ×9, ×16, ×18, ×32, and ×36
Simple dual port	×1, ×2, ×4, ×8, ×9, ×16, ×18, ×32, and ×36
True dual port	×1, ×2, ×4, ×8, ×9, ×16, and ×18

Clocking and PLL

Cyclone 10 LP devices feature global clock (GCLK) networks, dedicated clock pins, and general purpose PLLs.

- Up to 20 GCLK networks that drive throughout the device
- Up to 15 dedicated clock pins
- Up to four general purpose PLLs with five outputs per PLL

The PLLs provide robust clock management and synthesis for the Cyclone 10 LP device. You can dynamically reconfigure the PLLs in user mode to change the clock phase or frequency.

FPGA General Purpose I/O

Cyclone 10 LP devices offer highly configurable GPIOs with these features:

- Support for over 20 popular single-ended and differential I/O standards.
- Programmable bus hold, pull-up resistors, delay, and drive strength.
- Programmable slew-rate control to optimize signal integrity.
- Calibrated on-chip series termination (R_S OCT) or driver impedance matching (R_S) for single-endd I/O standards.
- True and emulated LVDS buffers with LVDS SERDES implemented using logic elements in the device core.
- Hot socketing support.

Configuration

Cyclone 10 LP devices use SRAM cells to store configuration data. Configuration data is downloaded to the Cyclone 10 LP device each time the device powers up.

You can use EPCS or EPCQ (AS x1) flash configuration devices to store configuration data and configure the Cyclone 10 LP FPGAs.

- Cyclone 10 LP devices support 1.5 V, 1.8 V, 2.5 V, 3.0 V, and 3.3 V programming voltages and several configuration schemes.
- The single-event upset (SEU) mitigation feature detects cyclic redundancy check (CRC) errors automatically during configuration and optionally during user mode[1].

1 User mode error detection is not supported on 1.0 V core voltage Cyclone 10 LP device variants.

Table 5. Configuration Schemes and Features Supported by Cyclone 10 LP Devices

Configuration Scheme	Configuration Method	Decompression	Remote System Upgrade
Active serial (AS)	Serial configuration device	Yes	Yes
Active parallel (AP)[2]	Supported flash memory	—	Yes
Passive serial (PS)	External host with flash memory	Yes	Yes
	Download cable	Yes	—
Fast passive parallel (FPP)	External host with flash memory	—	Yes
JTAG	External host with flash memory	—	—
	Download cable	—	—

Related Links

Configuration Devices
Provides more information about the EPCS and EPCQ configuration devices.

Power Management

Cyclone 10 LP devices are built on optimized low-power process:

- Available in two core voltage options: 1.2 V and 1.0 V
- Hot socketing compliant without needing external components or special design requirements

To accelerate your design schedule, combine Intel Cyclone 10 LP FPGAs with Enpirion® Power Solutions. Intel's ultra-compact and efficient Enpirion PowerSoCs are ideal for meeting Cyclone 10 LP power requirements. Enpirion PowerSoCs integrate most of the required components to provide you fully-validated and straightforward solutions with up to 96% efficiency. These advantages reduce your power supply design time and allow you to focus on your IP and FPGA designs.

Related Links

Enpirion Power Solutions
Provides more information about Enpirion PowerSoC devices.

Document Revision History for Cyclone 10 LP Advance Information Brief

Date	Version	Changes
February 2017	2017.02.13	Initial release.

2 Available only for the 10CL040, 10CL055, 10CL080, and 10CL120 devices.