

The TLV320AIC3254-Q1 features two miniDSP cores. The first miniDSP core is tightly coupled to the ADC, the second miniDSP core is tightly coupled to the DAC. The fully programmable algorithms for the miniDSP must be loaded into the device after power up. The miniDSPs have direct access to the digital stereo audio stream on the ADC and on the DAC side, offering the possibility for advanced, very-low group delay DSP algorithms. Each miniDSP can run up to 1152 instructions on every audio sample at a 48kHz sample rate. The two cores can run fully synchronized and can exchange data. Typical algorithms for the TLV320AIC3254-Q1 miniDSPs are active noise cancellation, acoustic echo cancellation or advanced DSP sound enhancement algorithms.

Software

Software development for the TLV320AIC3254-Q1 is supported through TI's comprehensive PurePath Studio Development Environment; a powerful, easy-to-use tool designed specifically to simplify software development on the TLV320AIC3254-Q1 miniDSP audio platform. The Graphical Development Environment consists of a library of common audio functions that can be dragged-and-dropped into an audio signal flow and graphically connected together. The DSP code can then be assembled from the graphical signal flow with the click of a mouse.

Please visit the TLV320AIC3254-Q1 product folder on www.ti.com to learn more about PurePath Studio and the latest status on available, ready-to-use DSP algorithms.

Register Map Summary

Table 11. Summary of Register Map

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
0	0	0x00	0x00	Page Select Register
0	1	0x00	0x01	Software Reset Register
0	2	0x00	0x02	Reserved Register
0	3	0x00	0x03	Reserved Register
0	4	0x00	0x04	Clock Setting Register 1, Multiplexers
0	5	0x00	0x05	Clock Setting Register 2, PLL P and R Values
0	6	0x00	0x06	Clock Setting Register 3, PLL J Values
0	7	0x00	0x07	Clock Setting Register 4, PLL D Values (MSB)
0	8	0x00	0x08	Clock Setting Register 5, PLL D Values (LSB)
0	9-10	0x00	0x09-0x0A	Reserved Register
0	11	0x00	0x0B	Clock Setting Register 6, NDAC Values
0	12	0x00	0x0C	Clock Setting Register 7, MDAC Values
0	13	0x00	0x0D	DAC OSR Setting Register 1, MSB Value
0	14	0x00	0x0E	DAC OSR Setting Register 2, LSB Value
0	15	0x00	0x0F	miniDSP_D Instruction Control Register 1
0	16	0x00	0x10	miniDSP_D Instruction Control Register 2
0	17	0x00	0x11	miniDSP_D Interpolation Factor Setting Register
0	18	0x00	0x12	Clock Setting Register 8, NADC Values
0	19	0x00	0x13	Clock Setting Register 9, MADC Values
0	20	0x00	0x14	ADC Oversampling (AOSR) Register
0	21	0x00	0x15	miniDSP_A Instruction Control Register 1
0	22	0x00	0x16	miniDSP_A Instruction Control Register 2
0	23	0x00	0x17	miniDSP_A Decimation Factor Setting Register
0	24	0x00	0x18	Reserved Register
0	25	0x00	0x19	Clock Setting Register 10, Multiplexers
0	26	0x00	0x1A	Clock Setting Register 11, CLKOUT M divider value
0	27	0x00	0x1B	Audio Interface Setting Register 1
0	28	0x00	0x1C	Audio Interface Setting Register 2, Data offset setting

Table 11. Summary of Register Map (continued)

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
0	29	0x00	0x1D	Audio Interface Setting Register 3
0	30	0x00	0x1E	Clock Setting Register 12, BCLK N Divider
0	31	0x00	0x1F	Audio Interface Setting Register 4, Secondary Audio Interface
0	32	0x00	0x20	Audio Interface Setting Register 5
0	33	0x00	0x21	Audio Interface Setting Register 6
0	34	0x00	0x22	Digital Interface Misc. Setting Register
0	35	0x00	0x23	Reserved Register
0	36	0x00	0x24	ADC Flag Register
0	37	0x00	0x25	DAC Flag Register 1
0	38	0x00	0x26	DAC Flag Register 2
0	39-41	0x00	0x27-0x29	Reserved Register
0	42	0x00	0x2A	Sticky Flag Register 1
0	43	0x00	0x2B	Interrupt Flag Register 1
0	44	0x00	0x2C	Sticky Flag Register 2
0	45	0x00	0x2D	Sticky Flag Register 3
0	46	0x00	0x2E	Interrupt Flag Register 2
0	47	0x00	0x2F	Interrupt Flag Register 3
0	48	0x00	0x30	INT1 Interrupt Control Register
0	49	0x00	0x31	INT2 Interrupt Control Register
0	50-51	0x00	0x32-0x33	Reserved Register
0	52	0x00	0x34	GPIO/MFP5 Control Register
0	53	0x00	0x35	DOUT/MFP2 Function Control Register
0	54	0x00	0x36	DIN/MFP1 Function Control Register
0	55	0x00	0x37	MISO/MFP4 Function Control Register
0	56	0x00	0x38	SCLK/MFP3 Function Control Register
0	57-59	0x00	0x39-0x3B	Reserved Registers
0	60	0x00	0x3C	DAC Signal Processing Block Control Register
0	61	0x00	0x3D	ADC Signal Processing Block Control Register
0	62	0x00	0x3E	miniDSP_A and miniDSP_D Configuration Register
0	63	0x00	0x3F	DAC Channel Setup Register 1
0	64	0x00	0x40	DAC Channel Setup Register 2
0	65	0x00	0x41	Left DAC Channel Digital Volume Control Register
0	66	0x00	0x42	Right DAC Channel Digital Volume Control Register
0	67	0x00	0x43	Headset Detection Configuration Register
0	68	0x00	0x44	DRC Control Register 1
0	69	0x00	0x45	DRC Control Register 2
0	70	0x00	0x46	DRC Control Register 3
0	71	0x00	0x47	Beep Generator Register 1
0	72	0x00	0x48	Beep Generator Register 2
0	73	0x00	0x49	Beep Generator Register 3
0	74	0x00	0x4A	Beep Generator Register 4
0	75	0x00	0x4B	Beep Generator Register 5
0	76	0x00	0x4C	Beep Generator Register 6
0	77	0x00	0x4D	Beep Generator Register 7
0	78	0x00	0x4E	Beep Generator Register 8
0	79	0x00	0x4F	Beep Generator Register 9

Table 11. Summary of Register Map (continued)

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
0	80	0x00	0x50	Reserved Register
0	81	0x00	0x51	ADC Channel Setup Register
0	82	0x00	0x52	ADC Fine Gain Adjust Register
0	83	0x00	0x53	Left ADC Channel Volume Control Register
0	84	0x00	0x54	Right ADC Channel Volume Control Register
0	85	0x00	0x55	ADC Phase Adjust Register
0	86	0x00	0x56	Left Channel AGC Control Register 1
0	87	0x00	0x57	Left Channel AGC Control Register 2
0	88	0x00	0x58	Left Channel AGC Control Register 3
0	89	0x00	0x59	Left Channel AGC Control Register 4
0	90	0x00	0x5A	Left Channel AGC Control Register 5
0	91	0x00	0x5B	Left Channel AGC Control Register 6
0	92	0x00	0x5C	Left Channel AGC Control Register 7
0	93	0x00	0x5D	Left Channel AGC Control Register 8
0	94	0x00	0x5E	Right Channel AGC Control Register 1
0	95	0x00	0x5F	Right Channel AGC Control Register 2
0	96	0x00	0x60	Right Channel AGC Control Register 3
0	97	0x00	0x61	Right Channel AGC Control Register 4
0	98	0x00	0x62	Right Channel AGC Control Register 5
0	99	0x00	0x63	Right Channel AGC Control Register 6
0	100	0x00	0x64	Right Channel AGC Control Register 7
0	101	0x00	0x65	Right Channel AGC Control Register 8
0	102	0x00	0x66	DC Measurement Register 1
0	103	0x00	0x67	DC Measurement Register 2
0	104	0x00	0x68	Left Channel DC Measurement Output Register 1
0	105	0x00	0x69	Left Channel DC Measurement Output Register 2
0	106	0x00	0x6A	Left Channel DC Measurement Output Register 3
0	107	0x00	0x6B	Right Channel DC Measurement Output Register 1
0	108	0x00	0x6C	Right Channel DC Measurement Output Register 2
0	109	0x00	0x6D	Right Channel DC Measurement Output Register 3
0	110-127	0x00	0x6E-0x7F	Reserved Register
1	0	0x01	0x00	Page Select Register
1	1	0x01	0x01	Power Configuration Register
1	2	0x01	0x02	LDO Control Register
1	3	0x01	0x03	Playback Configuration Register 1
1	4	0x01	0x04	Playback Configuration Register 2
1	5-8	0x01	0x05-0x08	Reserved Register
1	9	0x01	0x09	Output Driver Power Control Register
1	10	0x01	0x0A	Common Mode Control Register
1	11	0x01	0x0B	Over Current Protection Configuration Register
1	12	0x01	0x0C	HPL Routing Selection Register
1	13	0x01	0x0D	HPR Routing Selection Register
1	14	0x01	0x0E	LOL Routing Selection Register
1	15	0x01	0x0F	LOR Routing Selection Register
1	16	0x01	0x10	HPL Driver Gain Setting Register
1	17	0x01	0x11	HPR Driver Gain Setting Register

Table 11. Summary of Register Map (continued)

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
1	18	0x01	0x12	LOL Driver Gain Setting Register
1	19	0x01	0x13	LOR Driver Gain Setting Register
1	20	0x01	0x14	Headphone Driver Startup Control Register
1	21	0x01	0x15	Reserved Register
1	22	0x01	0x16	IN1L to HPL Volume Control Register
1	23	0x01	0x17	IN1R to HPR Volume Control Register
1	24	0x01	0x18	Mixer Amplifier Left Volume Control Register
1	25	0x01	0x19	Mixer Amplifier Right Volume Control Register
1	26-50	0x01	0x1A-0x32	Reserved Register
1	51	0x01	0x33	MICBIAS Configuration Register
1	52	0x01	0x34	Left MICPGA Positive Terminal Input Routing Configuration Register
1	53	0x01	0x35	Reserved Register
1	54	0x01	0x36	Left MICPGA Negative Terminal Input Routing Configuration Register
1	55	0x01	0x37	Right MICPGA Positive Terminal Input Routing Configuration Register
1	56	0x01	0x38	Reserved Register
1	57	0x01	0x39	Right MICPGA Negative Terminal Input Routing Configuration Register
1	58	0x01	0x3A	Floating Input Configuration Register
1	59	0x01	0x3B	Left MICPGA Volume Control Register
1	60	0x01	0x3C	Right MICPGA Volume Control Register
1	61	0x01	0x3D	ADC Power Tune Configuration Register
1	62	0x01	0x3E	ADC Analog Volume Control Flag Register
1	63	0x01	0x3F	DAC Analog Gain Control Flag Register
1	64-70	0x01	0x40-0x46	Reserved Register
1	71	0x01	0x47	Analog Input Quick Charging Configuration Register
1	72-122	0x01	0x48-0x7A	Reserved Register
1	123	0x01	0x7B	Reference Power-up Configuration Register
1	124-127	0x01	0x7C-0x7F	Reserved Register
8	0	0x08	0x00	Page Select Register
8	1	0x08	0x01	ADC Adaptive Filter Configuration Register
8	2-7	0x08	0x02-0x07	Reserved
8	8-127	0x08	0x08-0x7F	ADC Coefficients Buffer-A C(0:29)
9-16	0	0x09-0x10	0x00	Page Select Register
9-16	1-7	0x09-0x10	0x01-0x07	Reserved
9-16	8-127	0x09-0x10	0x08-0x7F	ADC Coefficients Buffer-A C(30:255)
26-34	0	0x1A-0x22	0x00	Page Select Register
26-34	1-7	0x1A-0x22	0x01-0x07	Reserved.
26-34	8-127	0x1A-0x22	0x08-0x7F	ADC Coefficients Buffer-B C(0:255)
44	0	0x2C	0x00	Page Select Register
44	1	0x2C	0x01	DAC Adaptive Filter Configuration Register
44	2-7	0x2C	0x02-0x07	Reserved
44	8-127	0x2C	0x08-0x7F	DAC Coefficients Buffer-A C(0:29)
45-52	0	0x2D-0x34	0x00	Page Select Register
45-52	1-7	0x2D-0x34	0x01-0x07	Reserved.
45-52	8-127	0x2D-0x34	0x08-0x7F	DAC Coefficients Buffer-A C(30:255)
62-70	0	0x3E-0x46	0x00	Page Select Register
62-70	1-7	0x3E-0x46	0x01-0x07	Reserved.

Table 11. Summary of Register Map (continued)

Decimal		Hex		DESCRIPTION
PAGE NO.	REG. NO.	PAGE NO.	REG. NO.	
62-70	8-127	0x3E-0x46	0x08-0x7F	DAC Coefficients Buffer-B C(0:255)
80-114	0	0x50-0x72	0x00	Page Select Register
80-114	1-7	0x50-0x72	0x01-0x07	Reserved.
80-114	8-127	0x50-0x72	0x08-0x7F	miniDSP_A Instructions
152-186	0	0x98-0xBA	0x00	Page Select Register
152-186	1-7	0x98-0xBA	0x01-0x07	Reserved.
152-186	8-127	0x98-0xBA	0x08-0x7F	miniDSP_D Instructions