GC9306

a-Si TFT LCD Single Chip Driver
240RGBx320 Resolution and 262K color

DataSheet

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List Of Contents

1. Introduction

The GC9306 is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 240RGBx320dots, comprising a 720-channel source driver, a 320-channel gate driver, 172,800 bytes GRAM for graphic display data of 240RGBx320 dots, and power supply circuit.

The GC9306 supports parallel 8-/9-/16-/18-bit data bus MCU interface, 6-/16-/18-bit data bus RGB interface and 3-/4-line serial peripheral interface (SPI) and 2 lane SPI data transmission. The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

The GC9306 can operate with 1.65V ~ 3.3V I/O interface voltage and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. GC9306 supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the GC9306 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

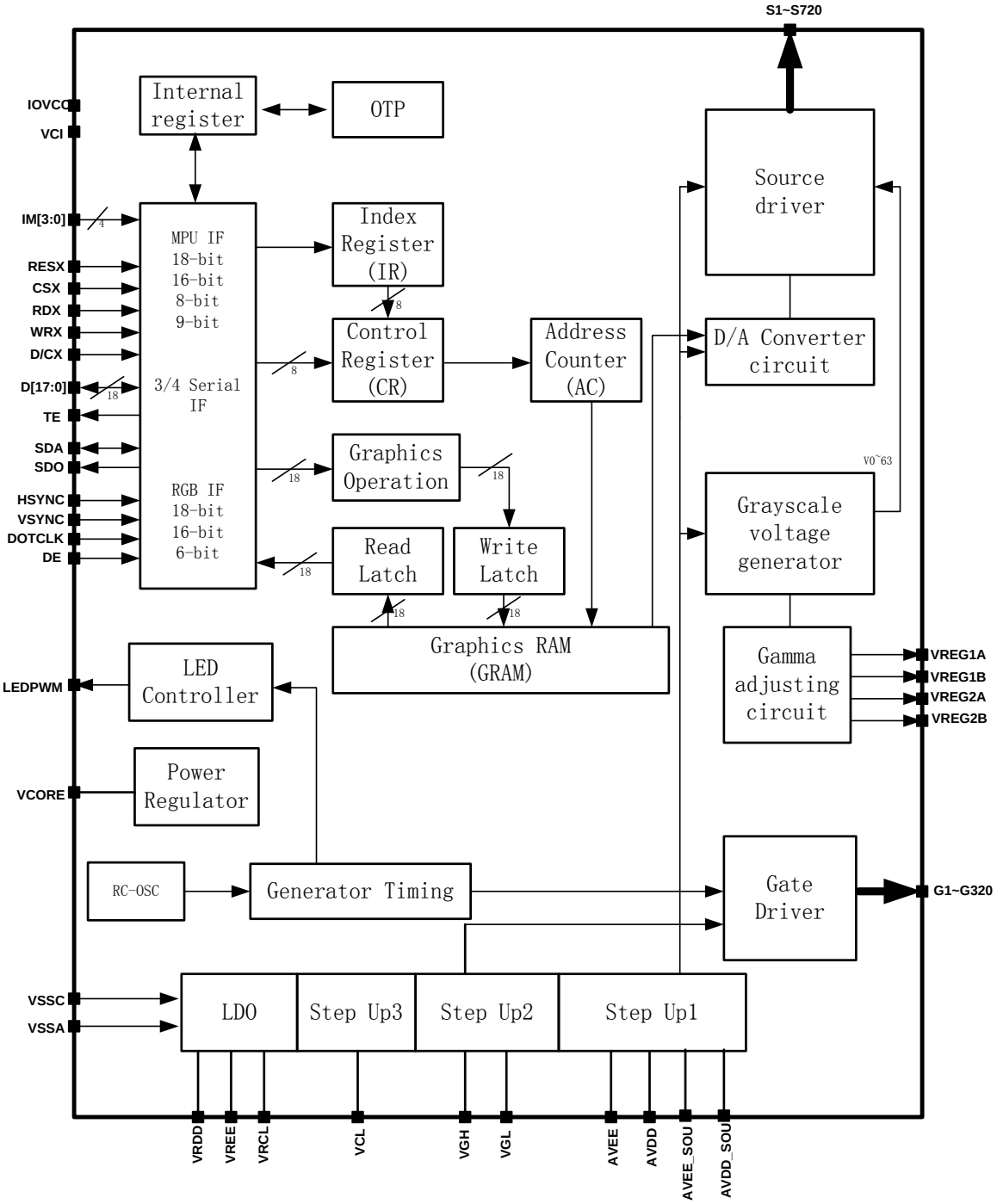
2. Features

- No need for external electronic component
- Display resolution: [240xRGB](H) x 320(V)
- Output:
  - 720 source outputs
  - 320 gate outputs
- a-TFT LCD driver with on-chip full display RAM: 172,800 bytes
- System Interface
  - 8-bits, 9-bits, 16-bits, 18-bits interface with 8080-I /8080-II series MCU
  - 6-bits, 16-bits, 18-bits RGB interface with graphic controller
  - 3-line / 4-line serial interface and 2 lane mode serial interface
- Display mode:
  - Full color mode (Idle mode OFF): 262K-color (selectable color depth mode by software)
  - Reduce color mode (Idle mode ON): 8-color
- Power saving mode:
  - Sleep mode
- On chip functions:
  - Timing generator
  - Oscillator
  - DC/DC converter
  - Dot/column inversion
- Low -power consumption architecture
  - Low operating power supplies:
    - IOVCC = 1.65V ~ 3.3V (logic)
    - VCI = 2.5V ~ 3.3V (analog)
- LCD Voltage drive:
  - Source/Gamma power supply voltage
    - AVDD - GND = 6.5V ~7.5V
    - AVEE - GND = -5.5V ~ -4.5V
    - AVDD_SOU - GND = 6.5V ~ 7.5V
    - AVEE_SOU - GND = -5.5V ~ -4.5V
    - VCL - GND = -3.0V ~ -1.5V
  - Gate driver output voltage
    - VGH - GND = 10.0V ~ 12.0V
    - VGL - GND = -11.0V ~ -9.0V
    - VGH - VGL ≦23V
- Operate temperature range: -40℃to 80℃
- a-Si TFT LCD storage capacitor : Cst on Common structure only

3. Block Diagram

3.1. Block diagram

Figure1



3.2. Pin Description

Table 1.

Power Supply Pins			
Pin Name	I/O	Type	Descriptions
IOVCC	I	Digital Power	Low voltage power supply for interface logic circuits(1.65~3.3V)
VCI	I	Analog Power	High voltage power supply for analog circuit blocks(2.5~3.3V)
VCORE	O	Digital Power	Regulated Low voltage level for interface circuits Don't apply any external power to this pad
VSSA	I	Analog Ground	System ground level for analog circuit blocks Connect to VSSA on the FPC to prevent noise.
VSSC	I	Digital Ground	System ground level for Digital circuit blocks Connect to VSSC on the FPC to prevent noise.

Table 2

<table>
<tr><th colspan="4">Interface Logic Signals</th></tr>
<tr><th>Pin Name</th><th>I/O</th><th>Type</th><th>Descriptions</th></tr>
<tr><td>IM[3:0]</td><td>I</td><td>(IOVCC/GND)</td><td>-Select the MCU interface mode
<table>
<tr><th rowspan="2">IM3</th><th rowspan="2">IM2</th><th rowspan="2">IM1</th><th rowspan="2">IM0</th><th rowspan="2">MCU-Interface</th><th colspan="2">Pins in use</th></tr>
<tr><th>Register</th><th>GRAM</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>8080 MCU 8-bit bus interface I</td><td>D[7:0]</td><td>D[7:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>8080 MCU16-bit bus interface I</td><td>D[7:0]</td><td>D[15:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>8080 MCU 9-bit bus interface I</td><td>D[7:0]</td><td>D[8:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8080 MCU18-bit bus interface I</td><td>D[7:0]</td><td>D[17:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface I</td><td colspan="2">SDA: In/OUT</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data serial interface I</td><td colspan="2">SDA: In/OUT</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>8080 MCU 16-bit bus interface II</td><td>D[8:1]</td><td>D[17:10] ,D[8:1]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>8080 MCU 8-bit bus interface II</td><td>D[17:10]</td><td>D[17:10]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>8080 MCU 18-bit bus interface II</td><td>D[8:1]</td><td>D[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>8080 MCU 9-bit bus interface II</td><td>D[17:10]</td><td>D[17:9]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface II</td><td colspan="2">SDI:In
SDO:Out</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data serial interface II</td><td colspan="2">SDI:In
SDO:Out</td></tr>
</table>
MPU Parallel interface bus and serial interface select
If use RGB Interface must select serial interface.
*:Fix this pin at IOVCC or GND.</td></tr>
<tr><td>RESX</td><td>I</td><td>MCU
(IOVCC/GND)</td><td>This signal will reset the device and must be applied to properly initialize the chip.
Signal is active low.</td></tr>
<tr><td>CSX</td><td>I</td><td>MCU
(IOVCC/GND)</td><td>Chip select input pin("Low" enable).
This pin can be permanently fixed "Low" in MPU interface mode only.</td></tr>
<tr><td>D/CX
(SCL)</td><td>I</td><td>MCU
(IOVCC/
GND)</td><td>This pin is used to select "Data or Command" in the parallel interface
When DCX='1', data is selected.
When DCX='0', command is selected.
This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface.
If not used, this pin should be connected to IOVCC or GND.</td></tr>
</table>

RDX	I	MCU (IOVCC/ GND)	8080-I/8080-II system (RDX): Serves as a read signal and MCU read data at the rising edge. Fix to IOVCC level when not in use
WRX (D/CX)	I	MCU (IOVCC/ GND)	8080-I/8080-II system (WRX): Serves as a write signal and writes data at the rising edge. 4-line system (D/CX): Serves as command or parameter select. 2 lane mode serial interface: Serves as the second SDA Fix to IOVCC level when not in use.
D[17:0]	I/O	MCU (IOVCC/ GND)	18-bit parallel bi-directional data bus for MCU system and RGB interface mode Fix to VSS level when not in use
SDI/SDA	I/O	MCU (IOVCC/ GND)	When IM[3]:Low, Serial in/out signal. When IM[3]:High, Serial input signal. The data is applied on the rising edge of the SCL signal. If not used, fix this pin at IOVCC or GND.
SDO	O	MCU (IOVCC/GND)	Serial output signal. The data is outputted on the falling edge of the SCL signal. If not used, open this pin
TE	O	MCU (IOVCC/ GND)	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.
DOTCLK	I	MCU (IOVCC/GND)	Dot clock signal for RGB interface operation. Fix to IOVCC or VSSC level when not in use.
VSYNC	I	MCU (IOVCC/GND)	Frame synchronizing signal for RGB interface operation. Fix to IOVCC or VSSC level when not in use.
HSYNC	I	MCU (IOVCC/ GND)	Line synchronizing signal for RGB interface operation. Fix to IOVCC or VSSC level when not in use.
DE	I	MCU (IOVCC/ GND)	Data enable signal for RGB interface operation. Fix to IOVCC or GND level when not in use.

Note:

1. If CSX is connected to GND in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore there will be no influence to the Power Consumption of the display module.

2. When CSX='1', there is no influence to the parallel and serial interface.

Table 3

LCD Driver Input/Output Pins			
Pin Name	I/O	Type	Descriptions
S720~S1	O	Source	Source output signals.. Leave the pin to open when not in use.
G320~G1	O	Gate	Gate output signals. Leave the pin to open when not in use.
VRDD	O	Power	Power supply for AVDD & AVDD_SOU.
VREE	O	Power	Power supply for AVEE & AVEE_SOU.
VRCL	O	Power	Power supply for VCL.
AVDD	O	Power	Output voltage of 1st step up circuit(3*VRDD).Input voltage to 2nd step up circuit. Generated power output pad for source driver block.
AVEE	O	Power	Output voltage of 1st step up circuit(-2*VREE).Input voltage to 2nd step up circuit. Generated power output pad for source driver block.
VGH	O	Power	Power supply for the gate driver(Positive).
VGL	O	Power	Power supply for the gate driver(Negative).
VCL	O	Power	Power supply for VGH and VGL. VCL=0~-VCI
VREG1A	O	-	internal generated stable power for source driver unit VREG1A is the highest positive grayscale reference voltage of source driver
VREG1B	O	-	internal generated stable power for source driver unit VREG1B is the lowest positive grayscale reference voltage of source driver
VREG2A	O	-	internal generated stable power for source driver unit VREG2A is the highest negative grayscale reference voltage of source driver
VREG2B	O	-	internal generated stable power for source driver unit VREG2B is the highest negative grayscale reference voltage of source driver
LEDPWM	O		Output pin for PWM(Pulse width Modulation) signal of LED driving. If not used,open this pad.

Table 4

Test Pins			
Pin Name	I/O	Type	Descriptions
DUMMY	-	Open	Input pads used only for test purpose at IC-side. During normal operation ,leave these pads open.

Liquid crystal power supply specifications Table

Table 5

No.	Item		Description
1	TFT Source Driver		720 pins (240*RGB)
2	TFT Gate Driver		320 pins
3	TFT Display's Capacitor Structure		Cst structure only (Cs on Common)
4	Liquid Crystal Drive Output	S1~S720	V0~V63 grayscales
		G1~G320	VGH-VGL
5	Input Voltage	IOVCC	1.65~3.30V
		VCI	2.50~3.30V
6	Liquid Crystal Drive Voltages	AVDD	6.5~7.5V
		AVEE	-5.5V~-4.5V
		VGH	10.0~12.0V
		VGL	-11.0~--9.0V
		VCL	-3.0~-1.5V
		VGH-VGL	Max.23.0V
		AVDD_SOU	6.5-7.5V
		AVEE_SOU	-5.5V~-4.5V
7	Internal Step-up Circuits	AVDD	VCI*3
		AVEE	VCI*-2
		VGH	VCI*5
		VGL	VCI*-5
		VCL	VCI*-1

3.3 PAD coordinates

Pad-No.	Pad-name	X	Y		Pad-No.	Pad-name	X	Y		Pad-No.	Pad-name	X	Y		Pad-No.	Pad-name	X	Y		Pad-No.	Pad-name	X	Y
1	DUMMY	-7292.5	-250.5		51	DUMMY	-4292.5	-250.5		101	VSSC	-1292.5	-250.5		151	BC	2245	-250.5		201	AVEE	5432.5	-250.5
2	DUMMY	-7232.5	-250.5		52	BGR_OUT	-4232.5	-250.5		102	VSSC	-1232.5	-250.5		152	VPP	2330	-250.5		202	AVEE	5492.5	-250.5
3	VCOM	-7172.5	-250.5		53	VRDD	-4172.5	-250.5		103	VSSC	-1172.5	-250.5		153	DUMMY	2402.5	-250.5		203	AVEE	5552.5	-250.5
4	VCOM	-7112.5	-250.5		54	VRDD	-4112.5	-250.5		104	VSSC	-1112.5	-250.5		154	DUMMY	2462.5	-250.5		204	AVEE	5612.5	-250.5
5	VCOM	-7052.5	-250.5		55	VRDD	-4052.5	-250.5		105	VSSC	-1052.5	-250.5		155	DUMMY	2535	-250.5		205	AVEE	5672.5	-250.5
6	VCOM	-6992.5	-250.5		56	VRDD	-3992.5	-250.5		106	DUMMY	-992.5	-250.5		156	DUMMY	2620	-250.5		206	VSSC	5732.5	-250.5
7	VCOM	-6932.5	-250.5		57	VRDD	-3932.5	-250.5		107	VSSC	-932.5	-250.5		157	DUMMY	2705	-250.5		207	VSSC	5792.5	-250.5
8	VCOM	-6872.5	-250.5		58	VRDD	-3872.5	-250.5		108	VSSC	-872.5	-250.5		158	DUMMY	2790	-250.5		208	VSSC	5852.5	-250.5
9	VCOM	-6812.5	-250.5		59	VRDD	-3812.5	-250.5		109	DUMMY	-812.5	-250.5		159	DUMMY	2875	-250.5		209	VSSC	5912.5	-250.5
10	VCOM	-6752.5	-250.5		60	VCORE	-3752.5	-250.5		110	IM<3>	-752.5	-250.5		160	DUMMY	2960	-250.5		210	VSSC	5972.5	-250.5
11	DUMMY	-6692.5	-250.5		61	VCORE	-3692.5	-250.5		111	IM<2>	-692.5	-250.5		161	DUMMY	3032.5	-250.5		211	VSSC	6032.5	-250.5
12	VGH	-6632.5	-250.5		62	VCORE	-3632.5	-250.5		112	IM<1>	-632.5	-250.5		162	IOVCC	3092.5	-250.5		212	VSSC	6092.5	-250.5
13	VGH	-6572.5	-250.5		63	VCORE	-3572.5	-250.5		113	IM<0>	-572.5	-250.5		163	IOVCC	3152.5	-250.5		213	VSSC	6152.5	-250.5
14	VGL	-6512.5	-250.5		64	VCORE	-3512.5	-250.5		114	RESX	-512.5	-250.5		164	IOVCC	3212.5	-250.5		214	GVDDN	6212.5	-250.5
15	VGL	-6452.5	-250.5		65	VCORE	-3452.5	-250.5		115	CSX	-452.5	-250.5		165	IOVCC	3272.5	-250.5		215	GVDDN	6272.5	-250.5
16	VCL	-6392.5	-250.5		66	VCORE	-3392.5	-250.5		116	DCX	-392.5	-250.5		166	IOVCC	3332.5	-250.5		216	GVDDN	6332.5	-250.5
17	VCL	-6332.5	-250.5		67	VSSC	-3332.5	-250.5		117	WRX	-332.5	-250.5		167	IOVCC	3392.5	-250.5		217	GVDDN	6392.5	-250.5
18	VRCL	-6272.5	-250.5		68	VSSC	-3272.5	-250.5		118	RDX	-272.5	-250.5		168	IOVCC	3452.5	-250.5		218	GVDDN	6452.5	-250.5
19	VRCL	-6212.5	-250.5		69	VSSC	-3212.5	-250.5		119	DUMMY	-212.5	-250.5		169	DUMMY	3512.5	-250.5		219	GVDDN	6512.5	-250.5
20	DUMMY	-6152.5	-250.5		70	VSSC	-3152.5	-250.5		120	VSYNC	-152.5	-250.5		170	DUMMY	3572.5	-250.5		220	GVDDN	6572.5	-250.5
21	DUMMY	-6092.5	-250.5		71	VSSC	-3092.5	-250.5		121	HSYNC	-92.5	-250.5		171	DUMMY	3632.5	-250.5		221	GVDDN	6632.5	-250.5
22	AVDD	-6032.5	-250.5		72	VSSC	-3032.5	-250.5		122	ENABL	-32.5	-250.5		172	DUMMY	3692.5	-250.5		222	GVDDN	6692.5	-250.5
23	AVDD	-5972.5	-250.5		73	VSSC	-2972.5	-250.5		123	DOTCLK	27.5	-250.5		173	DUMMY	3752.5	-250.5		223	VCOM	6752.5	-250.5
24	AVDD	-5912.5	-250.5		74	VCI	-2912.5	-250.5		124	DUMMY	87.5	-250.5		174	DUMMY	3812.5	-250.5		224	VCOM	6812.5	-250.5
25	DUMMY	-5852.5	-250.5		75	VCI	-2852.5	-250.5		125	SDA	160	-250.5		175	DUMMY	3872.5	-250.5		225	VCOM	6872.5	-250.5
26	DUMMY	-5792.5	-250.5		76	VCI	-2792.5	-250.5		126	DB<0>	245	-250.5		176	DUMMY	3932.5	-250.5		226	VCOM	6932.5	-250.5
27	DUMMY	-5732.5	-250.5		77	VCI	-2732.5	-250.5		127	DB<1>	330	-250.5		177	DUMMY	3992.5	-250.5		227	VCOM	6992.5	-250.5
28	DUMMY	-5672.5	-250.5		78	VCI	-2672.5	-250.5		128	DB<2>	415	-250.5		178	DUMMY	4052.5	-250.5		228	VCOM	7052.5	-250.5
29	DUMMY	-5612.5	-250.5		79	VCI	-2612.5	-250.5		129	DB<3>	500	-250.5		179	DUMMY	4112.5	-250.5		229	VCOM	7112.5	-250.5
30	DUMMY	-5552.5	-250.5		80	VCI	-2552.5	-250.5		130	DUMMY	572.5	-250.5		180	DUMMY	4172.5	-250.5		230	VCOM	7172.5	-250.5
31	AVEE_SOU	-5492.5	-250.5		81	VCI	-2492.5	-250.5		131	DB<4>	645	-250.5		181	DUMMY	4232.5	-250.5		231	DUMMY	7232.5	-250.5
32	AVDD_SOU	-5432.5	-250.5		82	VSSA	-2432.5	-250.5		132	DB<5>	730	-250.5		182	DUMMY	4292.5	-250.5		232	DUMMY	7292.5	-250.5
33	DUMMY	-5372.5	-250.5		83	VSSA	-2372.5	-250.5		133	DB<6>	815	-250.5		183	VREG1A	4352.5	-250.5		233	DUMMY	7399	233
34	DUMMY	-5312.5	-250.5		84	VSSA	-2312.5	-250.5		134	DB<7>	900	-250.5		184	DUMMY	4412.5	-250.5		234	DUMMY	7385	115
35	DUMMY	-5252.5	-250.5		85	VSSA	-2252.5	-250.5		135	DUMMY	972.5	-250.5		185	DUMMY	4472.5	-250.5		235	DUMMY	7371	233
36	DUMMY	-5192.5	-250.5		86	VSSA	-2192.5	-250.5		136	DB<8>	1045	-250.5		186	DUMMY	4532.5	-250.5		236	G<2>	7357	115
37	DUMMY	-5132.5	-250.5		87	VSSA	-2132.5	-250.5		137	DB<9>	1130	-250.5		187	GVDDP	4592.5	-250.5		237	G<4>	7343	233
38	DUMMY	-5072.5	-250.5		88	VSSA	-2072.5	-250.5		138	DB<10>	1215	-250.5		188	DUMMY	4652.5	-250.5		238	G<6>	7329	115
39	VX4	-5012.5	-250.5		89	VSSA	-2012.5	-250.5		139	DB<11>	1300	-250.5		189	DUMMY	4712.5	-250.5		239	G<8>	7315	233
40	DUMMY	-4952.5	-250.5		90	VSSA	-1952.5	-250.5		140	OSC_TEST	1372.5	-250.5		190	DUMMY	4772.5	-250.5		240	G<10>	7301	115
41	DUMMY	-4892.5	-250.5		91	VSSC	-1892.5	-250.5		141	DB<12>	1445	-250.5		191	DUMMY	4832.5	-250.5		241	G<12>	7287	233
42	DUMMY	-4832.5	-250.5		92	VSSC	-1832.5	-250.5		142	DB<13>	1530	-250.5		192	DUMMY	4892.5	-250.5		242	G<14>	7273	115
43	DUMMY	-4772.5	-250.5		93	VSSC	-1772.5	-250.5		143	DB<14>	1615	-250.5		193	VREF_OUT	4952.5	-250.5		243	G<16>	7259	233
44	DUMMY	-4712.5	-250.5		94	VSSC	-1712.5	-250.5		144	DB<15>	1700	-250.5		194	DUMMY	5012.5	-250.5		244	G<18>	7245	115
45	DUMMY	-4652.5	-250.5		95	VSSC	-1652.5	-250.5		145	DUMMY	1772.5	-250.5		195	DUMMY	5072.5	-250.5		245	G<20>	7231	233
46	DUMMY	-4592.5	-250.5		96	VSSC	-1592.5	-250.5		146	DB<16>	1845	-250.5		196	DUMMY	5132.5	-250.5		246	G<22>	7217	115
47	DUMMY	-4532.5	-250.5		97	VSSC	-1532.5	-250.5		147	DB<17>	1930	-250.5		197	DUMMY	5192.5	-250.5		247	G<24>	7203	233
48	DUMMY	-4472.5	-250.5		98	VSSC	-1472.5	-250.5		148	OSC_IN	2002.5	-250.5		198	AVEE	5252.5	-250.5		248	G<26>	7189	115
49	DUMMY	-4412.5	-250.5		99	VSSC	-1412.5	-250.5		149	TE	2075	-250.5		199	AVEE	5312.5	-250.5		249	G<28>	7175	233
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769	S<347>	-231	233		819	S<297>	-931	233		869	S<247>	-1631	233		919	S<197>	-2331	233		969	S<147>	-3031	233
770	S<346>	-245	115		820	S<296>	-945	115		870	S<246>	-1645	115		920	S<196>	-2345	115		970	S<146>	-3045	115
771	S<345>	-259	233		821	S<295>	-959	233		871	S<245>	-1659	233		921	S<195>	-2359	233		971	S<145>	-3059	233
772	S<344>	-273	115		822	S<294>	-973	115		872	S<244>	-1673	115		922	S<194>	-2373	115		972	S<144>	-3073	115
773	S<343>	-287	233		823	S<293>	-987	233		873	S<243>	-1687	233		923	S<193>	-2387	233		973	S<143>	-3087	233
774	S<342>	-301	115		824	S<292>	-1001	115		874	S<242>	-1701	115		924	S<192>	-2401	115		974	S<142>	-3101	115
775	S<341>	-315	233		825	S<291>	-1015	233		875	S<241>	-1715	233		925	S<191>	-2415	233		975	S<141>	-3115	233
776	S<340>	-329	115		826	S<290>	-1029	115		876	S<240>	-1729	115		926	S<190>	-2429	115		976	S<140>	-3129	115
777	S<339>	-343	233		827	S<289>	-1043	233		877	S<239>	-1743	233		927	S<189>	-2443	233		977	S<139>	-3143	233
778	S<338>	-357	115		828	S<288>	-1057	115		878	S<238>	-1757	115		928	S<188>	-2457	115		978	S<138>	-3157	115
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780	S<336>	-385	115		830	S<286>	-1085	115		880	S<236>	-1785	115		930	S<186>	-2485	115		980	S<136>	-3185	115
781	S<335>	-399	233		831	S<285>	-1099	233		881	S<235>	-1799	233		931	S<185>	-2499	233		981	S<135>	-3199	233
782	S<334>	-413	115		832	S<284>	-1113	115		882	S<234>	-1813	115		932	S<184>	-2513	115		982	S<134>	-3213	115

783	S<333>	-427	233		833	S<283>	-1127	233		883	S<233>	-1827	233		933	S<183>	-2527	233		983	S<133>	-3227	233
784	S<332>	-441	115		834	S<282>	-1141	115		884	S<232>	-1841	115		934	S<182>	-2541	115		984	S<132>	-3241	115
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790	S<326>	-525	115		840	S<276>	-1225	115		890	S<226>	-1925	115		940	S<176>	-2625	115		990	S<126>	-3325	115
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794	S<322>	-581	115		844	S<272>	-1281	115		894	S<222>	-1981	115		944	S<172>	-2681	115		994	S<122>	-3381	115
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796	S<320>	-609	115		846	S<270>	-1309	115		896	S<220>	-2009	115		946	S<170>	-2709	115		996	S<120>	-3409	115
797	S<319>	-623	233		847	S<269>	-1323	233		897	S<219>	-2023	233		947	S<169>	-2723	233		997	S<119>	-3423	233
798	S<318>	-637	115		848	S<268>	-1337	115		898	S<218>	-2037	115		948	S<168>	-2737	115		998	S<118>	-3437	115
799	S<317>	-651	233		849	S<267>	-1351	233		899	S<217>	-2051	233		949	S<167>	-2751	233		999	S<117>	-3451	233
800	S<316>	-665	115		850	S<266>	-1365	115		900	S<216>	-2065	115		950	S<166>	-2765	115		1000	S<116>	-3465	115

Pad-No.	Pad-name	X	Y		Pad-No.	Pad-name	X	Y		Pad-No.	Pad-name	X	Y		Pad-No.	Pad-name	X	Y		Pad-No.	Pad-name	X	Y
1001	S<115>	-3479	233		1051	S<65>	-4179	233		1101	S<15>	-4879	233		1151	G<249>	-5621	233		1201	G<149>	-6321	233
1002	S<114>	-3493	115		1052	S<64>	-4193	115		1102	S<14>	-4893	115		1152	G<247>	-5635	115		1202	G<147>	-6335	115
1003	S<113>	-3507	233		1053	S<63>	-4207	233		1103	S<13>	-4907	233		1153	G<245>	-5649	233		1203	G<145>	-6349	233
1004	S<112>	-3521	115		1054	S<62>	-4221	115		1104	S<12>	-4921	115		1154	G<243>	-5663	115		1204	G<143>	-6363	115
1005	S<111>	-3535	233		1055	S<61>	-4235	233		1105	S<11>	-4935	233		1155	G<241>	-5677	233		1205	G<141>	-6377	233
1006	S<110>	-3549	115		1056	S<60>	-4249	115		1106	S<10>	-4949	115		1156	G<239>	-5691	115		1206	G<139>	-6391	115
1007	S<109>	-3563	233		1057	S<59>	-4263	233		1107	S<9>	-4963	233		1157	G<237>	-5705	233		1207	G<137>	-6405	233
1008	S<108>	-3577	115		1058	S<58>	-4277	115		1108	S<8>	-4977	115		1158	G<235>	-5719	115		1208	G<135>	-6419	115
1009	S<107>	-3591	233		1059	S<57>	-4291	233		1109	S<7>	-4991	233		1159	G<233>	-5733	233		1209	G<133>	-6433	233
1010	S<106>	-3605	115		1060	S<56>	-4305	115		1110	S<6>	-5005	115		1160	G<231>	-5747	115		1210	G<131>	-6447	115
1011	S<105>	-3619	233		1061	S<55>	-4319	233		1111	S<5>	-5019	233		1161	G<229>	-5761	233		1211	G<129>	-6461	233
1012	S<104>	-3633	115		1062	S<54>	-4333	115		1112	S<4>	-5033	115		1162	G<227>	-5775	115		1212	G<127>	-6475	115
1013	S<103>	-3647	233		1063	S<53>	-4347	233		1113	S<3>	-5047	233		1163	G<225>	-5789	233		1213	G<125>	-6489	233
1014	S<102>	-3661	115		1064	S<52>	-4361	115		1114	S<2>	-5061	115		1164	G<223>	-5803	115		1214	G<123>	-6503	115
1015	S<101>	-3675	233		1065	S<51>	-4375	233		1115	S<1>	-5075	233		1165	G<221>	-5817	233		1215	G<121>	-6517	233
1016	S<100>	-3689	115		1066	S<50>	-4389	115		1116	G<319>	-5131	115		1166	G<219>	-5831	115		1216	G<119>	-6531	115
1017	S<99>	-3703	233		1067	S<49>	-4403	233		1117	G<317>	-5145	233		1167	G<217>	-5845	233		1217	G<117>	-6545	233
1018	S<98>	-3717	115		1068	S<48>	-4417	115		1118	G<315>	-5159	115		1168	G<215>	-5859	115		1218	G<115>	-6559	115
1019	S<97>	-3731	233		1069	S<47>	-4431	233		1119	G<313>	-5173	233		1169	G<213>	-5873	233		1219	G<113>	-6573	233
1020	S<96>	-3745	115		1070	S<46>	-4445	115		1120	G<311>	-5187	115		1170	G<211>	-5887	115		1220	G<111>	-6587	115
1021	S<95>	-3759	233		1071	S<45>	-4459	233		1121	G<309>	-5201	233		1171	G<209>	-5901	233		1221	G<109>	-6601	233
1022	S<94>	-3773	115		1072	S<44>	-4473	115		1122	G<307>	-5215	115		1172	G<207>	-5915	115		1222	G<107>	-6615	115
1023	S<93>	-3787	233		1073	S<43>	-4487	233		1123	G<305>	-5229	233		1173	G<205>	-5929	233		1223	G<105>	-6629	233
1024	S<92>	-3801	115		1074	S<42>	-4501	115		1124	G<303>	-5243	115		1174	G<203>	-5943	115		1224	G<103>	-6643	115
1025	S<91>	-3815	233		1075	S<41>	-4515	233		1125	G<301>	-5257	233		1175	G<201>	-5957	233		1225	G<101>	-6657	233
1026	S<90>	-3829	115		1076	S<40>	-4529	115		1126	G<299>	-5271	115		1176	G<199>	-5971	115		1226	G<99>	-6671	115
1027	S<89>	-3843	233		1077	S<39>	-4543	233		1127	G<297>	-5285	233		1177	G<197>	-5985	233		1227	G<97>	-6685	233
1028	S<88>	-3857	115		1078	S<38>	-4557	115		1128	G<295>	-5299	115		1178	G<195>	-5999	115		1228	G<95>	-6699	115
1029	S<87>	-3871	233		1079	S<37>	-4571	233		1129	G<293>	-5313	233		1179	G<193>	-6013	233		1229	G<93>	-6713	233
1030	S<86>	-3885	115		1080	S<36>	-4585	115		1130	G<291>	-5327	115		1180	G<191>	-6027	115		1230	G<91>	-6727	115
1031	S<85>	-3899	233		1081	S<35>	-4599	233		1131	G<289>	-5341	233		1181	G<189>	-6041	233		1231	G<89>	-6741	233
1032	S<84>	-3913	115		1082	S<34>	-4613	115		1132	G<287>	-5355	115		1182	G<187>	-6055	115		1232	G<87>	-6755	115
1033	S<83>	-3927	233		1083	S<33>	-4627	233		1133	G<285>	-5369	233		1183	G<185>	-6069	233		1233	G<85>	-6769	233
1034	S<82>	-3941	115		1084	S<32>	-4641	115		1134	G<283>	-5383	115		1184	G<183>	-6083	115		1234	G<83>	-6783	115
1035	S<81>	-3955	233		1085	S<31>	-4655	233		1135	G<281>	-5397	233		1185	G<181>	-6097	233		1235	G<81>	-6797	233
1036	S<80>	-3969	115		1086	S<30>	-4669	115		1136	G<279>	-5411	115		1186	G<179>	-6111	115		1236	G<79>	-6811	115
1037	S<79>	-3983	233		1087	S<29>	-4683	233		1137	G<277>	-5425	233		1187	G<177>	-6125	233		1237	G<77>	-6825	233
1038	S<78>	-3997	115		1088	S<28>	-4697	115		1138	G<275>	-5439	115		1188	G<175>	-6139	115		1238	G<75>	-6839	115
1039	S<77>	-4011	233		1089	S<27>	-4711	233		1139	G<273>	-5453	233		1189	G<173>	-6153	233		1239	G<73>	-6853	233
1040	S<76>	-4025	115		1090	S<26>	-4725	115		1140	G<271>	-5467	115		1190	G<171>	-6167	115		1240	G<71>	-6867	115
1041	S<75>	-4039	233		1091	S<25>	-4739	233		1141	G<269>	-5481	233		1191	G<169>	-6181	233		1241	G<69>	-6881	233
1042	S<74>	-4053	115		1092	S<24>	-4753	115		1142	G<267>	-5495	115		1192	G<167>	-6195	115		1242	G<67>	-6895	115
1043	S<73>	-4067	233		1093	S<23>	-4767	233		1143	G<265>	-5509	233		1193	G<165>	-6209	233		1243	G<65>	-6909	233
1044	S<72>	-4081	115		1094	S<22>	-4781	115		1144	G<263>	-5523	115		1194	G<163>	-6223	115		1244	G<63>	-6923	115

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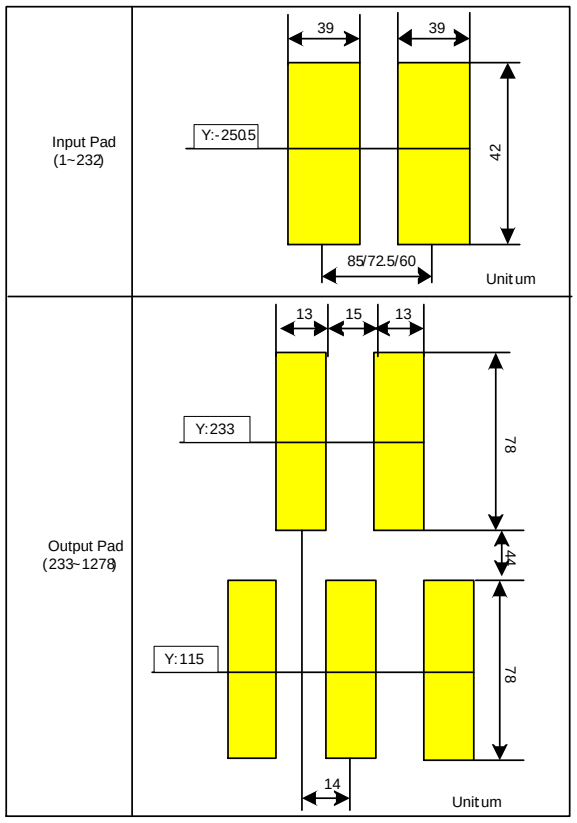
1146	G<259>	-5551	109.5		1096	S<20>	-4809	115		1146	G<259>	-5551	115		1196	G<159>	-6251	115		1246	G<59>	-6951	115
1147	G<257>	-5565	231.5		1097	S<19>	-4823	233		1147	G<257>	-5565	233		1197	G<157>	-6265	233		1247	G<57>	-6965	233
1148	G<255>	-5579	109.5		1098	S<18>	-4837	115		1148	G<255>	-5579	115		1198	G<155>	-6279	115		1248	G<55>	-6979	115
1149	G<253>	-5593	231.5		1099	S<17>	-4851	233		1149	G<253>	-5593	233		1199	G<153>	-6293	233		1249	G<53>	-6993	233
1150	G<251>	-5607	109.5		1100	S<16>	-4865	115		1150	G<251>	-5607	115		1200	G<151>	-6307	115		1250	G<51>	-7007	115

Pad-No.	Pad-name	X	Y
1251	G<49>	-7021	233
1252	G<47>	-7035	115
1253	G<45>	-7049	233
1254	G<43>	-7063	115
1255	G<41>	-7077	233
1256	G<39>	-7091	115
1257	G<37>	-7105	233
1258	G<35>	-7119	115
1259	G<33>	-7133	233
1260	G<31>	-7147	115
1261	G<29>	-7161	233
1262	G<27>	-7175	115
1263	G<25>	-7189	233
1264	G<23>	-7203	115
1265	G<21>	-7217	233
1266	G<19>	-7231	115
1267	G<17>	-7245	233
1268	G<15>	-7259	115
1269	G<13>	-7273	233
1270	G<11>	-7287	115
1271	G<9>	-7301	233
1272	G<7>	-7315	115
1273	G<5>	-7329	233
1274	G<3>	-7343	115
1275	G<1>	-7357	233
1276	DUMMY<23>	-7371	115
1277	DUMMY<22>	-7385	233
1278	DUMMY<24>	-7399	115

BUMP Size



Chip Size: 15360um x 640um

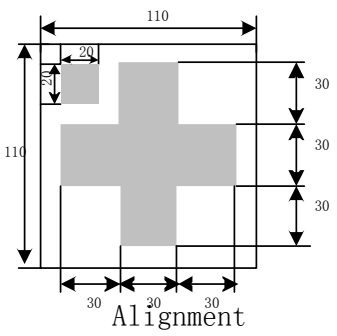
Chip thickness: 782um(typ.)

Pad Location: Pad Center

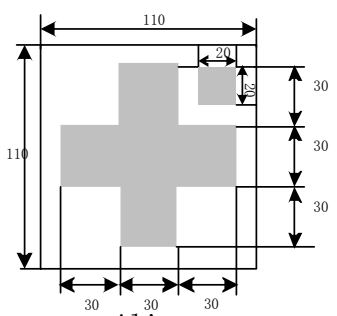
Coordinate Origin: Chip center

Au bump height: 9um(typ.)

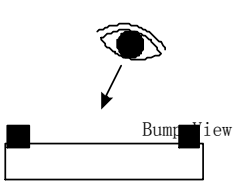
Alignment Marks

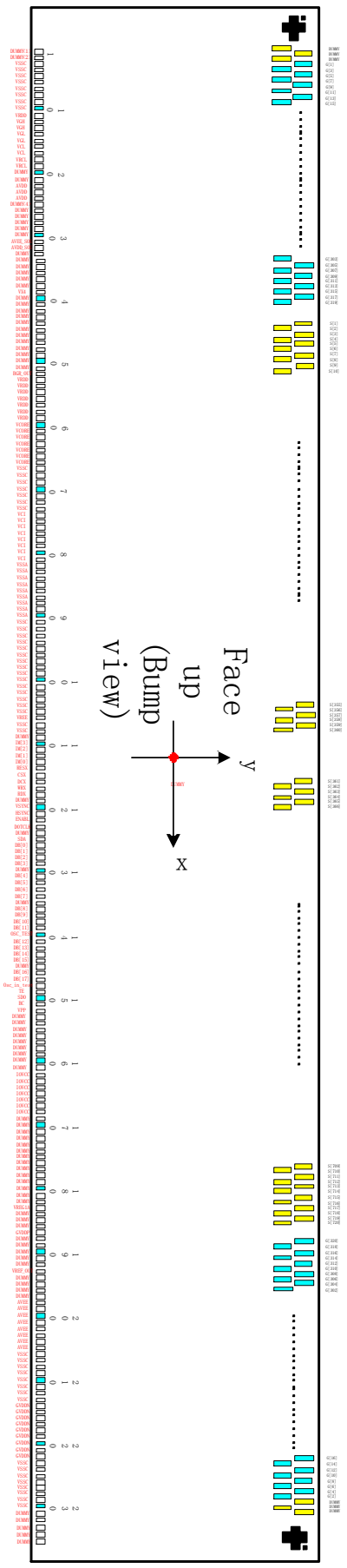


Alignment Mark:A1



Alignment Mark:A2





4. Interface setting

4.1. MCU interfaces

GC9306 provides the 8-/9-/16-/18-bit parallel system interface for 8080-I /8080- II series, and 3-/4-line serial system interface for serial data input. The input system interface is selected by external pins IM [3:0] and the bit formal per pixel color order is selected by DBI [2:0] 3-bits of 3Ah register.

4.1.1. MCU interface selection

The selection of interface is done by setting external pins IM [3:0] as shown in the following table.

Table 6

IM3	IM2	IM1	IM0	MCU-Interface Mode	Pins in use	
					Register/Content	GRAM
0	0	0	0	8080 MCU 8-bit bus interface I	D[7:0]	D[7:0],WRX,RDX,CSX,D/CX
0	0	0	1	8080 MCU 16-bit bus interface I	D[7:0]	D[15:0],WRX,RDX,CSX,D/CX
0	0	1	0	8080 MCU 9-bit bus interface I	D[7:0]	D[8:0],WRX,RDX,CSX,D/CX
0	0	1	1	8080 MCU 18-bit bus interface I	D[7:0]	D[17:0],WRX,RDX,CSX,D/CX
0	1	0	1	3-wire 9-bit data serial interface I	SCL,SDA,CSX	
0	1	1	0	4-wire 8-bit data serial interface I	SCL,SDA,D/CX,CSX	
1	0	0	0	8080 MCU 16-bit bus interface II	D[8:1]	D[17:10],D[8:1],WRX,RDX,CSX,D/CX
1	0	0	1	8080 MCU 8-bit bus interface II	D[17:10]	D[17:10],WRX,RDX,CSX,D/CX
1	0	1	0	8080 MCU 18-bit bus interface II	D[8:1]	D[17:0],WRX,RDX,CSX,D/CX
1	0	1	1	8080 MCU 9-bit bus interface II	D[17:10]	D[17:9],WRX,RDX,CSX,D/CX
1	1	0	1	3-wire 9-bit data serial interface II	SCL,SDI,SDO,CSX	
1	1	1	0	4-wire 8-bit data serial interface II	SCL,SDI,SDO,D/CX,CSX	

4.1.2. 8080-Ⅰ Series Parallel Interface

GC9306 can be accessed via 8-/9-/16-/18-bit MCU 8080-I series parallel interface. The chip select CSX (active low) is used to enable or disable GC9306 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

GC9306 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D[17:0] bits are commands.

The 8080-I series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080-I Interface selection is done when IM3 pin is low state (VSSC level). Interface bus width can be selected by IM [2:0] bits.
The selection of 8080-I series parallel interface is shown as the table in the following.

Table 7

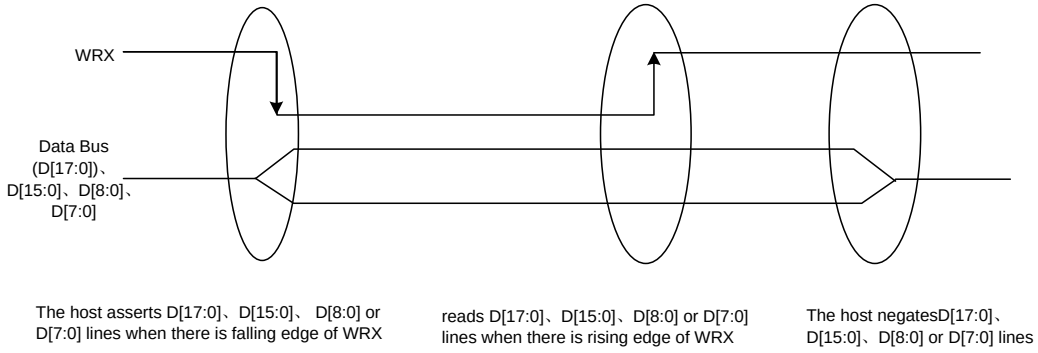
IM3	IM2	IM1	IM0	MCU-Interface	CSX	WRX	RDX	D/CX	Function
0	0	0	0	8080 MCU 8-bit bus interface I	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	0	0	1	8080 MCU 16-bit bus interface I	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	0	1	0	8080 MCU 9-bit bus interface I	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
0	0	1	1	8080 MCU 18-bit bus interface I	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.

4.1.3. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is SRAM data or command's parameter.

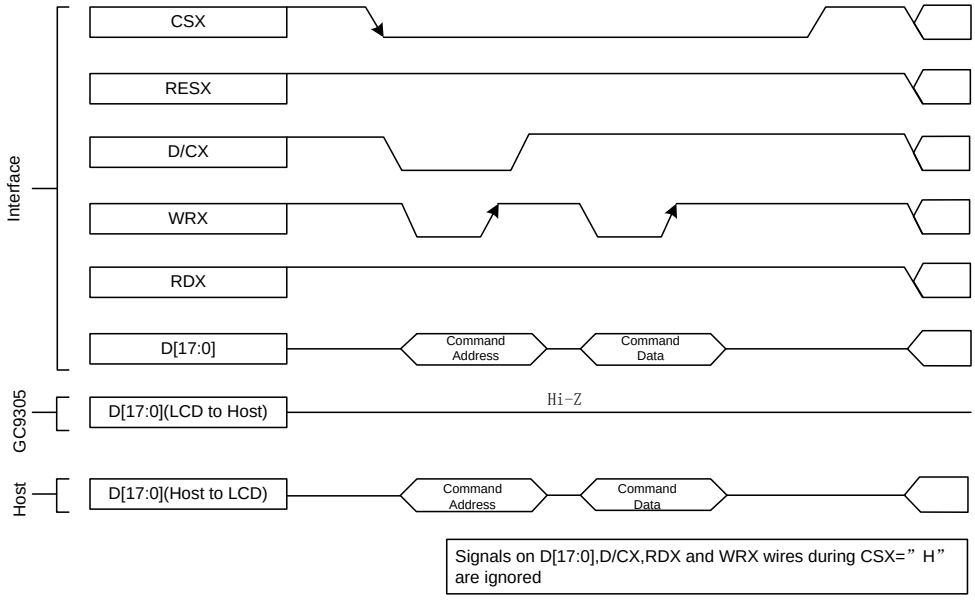
The following figure shows a write cycle for the 8080-I MCU interface.

Figure 2.



Note: WRX is an unsynchronized signal (It can be stopped)

Figure 3.

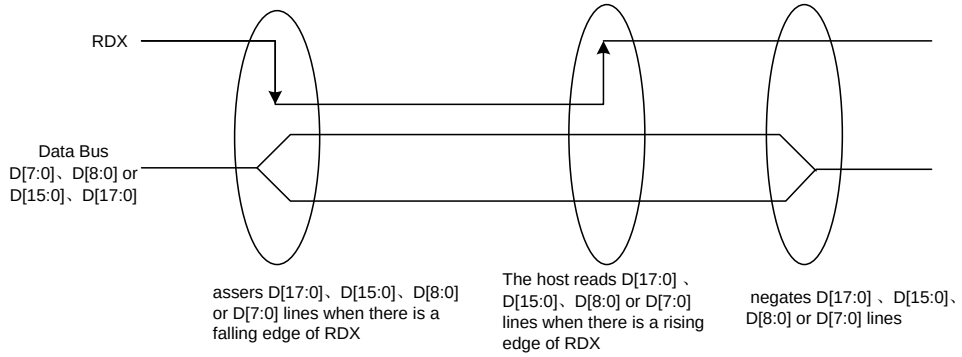


4.1.4. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle, while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

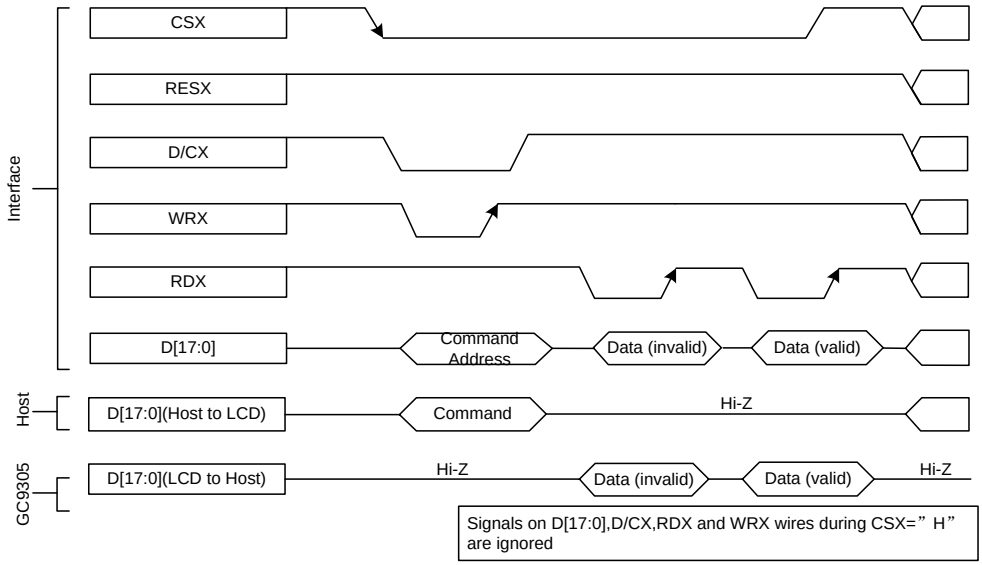
The following figure shows the read cycle for the 8080-I MCU interface.

Figure 4.



Note: RDX is an unsynchronized signal (It can be stopped).

Figure 5.



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

4.1.5. 8080-Ⅱ Series Parallel Interface

GC9306 can be accessed via 8-/9-/16-/18-bit MCU 8080-Ⅱ series parallel interface. The chip select CSX (active low) is used to enable or disable GC9306 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

GC9306 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D[17:0] bits are commands.

The 8080-II series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080-II Interface selection is done when IM3 pin is high state (IOVCC level). Interface bus width can be selected by IM [2:0] bits.

The selection of 8080-II series parallel interface is shown as the table in the following.

Table 8

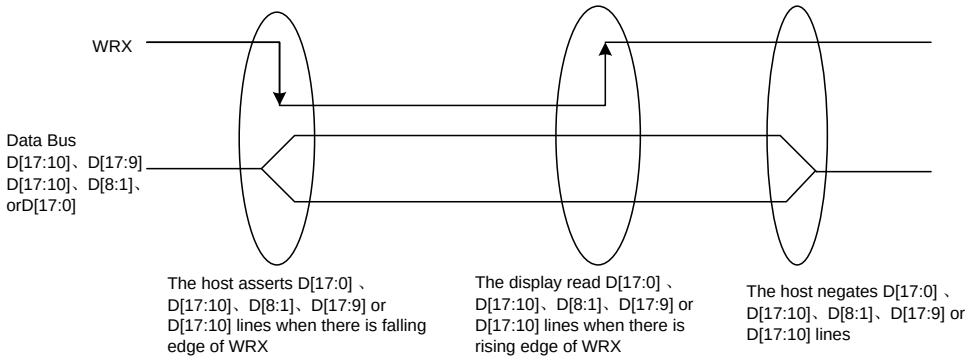
IM3	IM2	IM1	IM0	MCU-Interface	CSX	WRX	RDX	D/CX	Function
1	0	0	0	8080 MCU 16-bit bus interface II	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
1	0	0	1	8080 MCU 8-bit bus interface II	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
1	0	1	0	8080 MCU 18-bit bus interface II	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.
1	0	1	1	8080 MCU 9-bit bus interface II	"L"	↑	"H"	"L"	Write command code.
					"L"	"H"	↑	"H"	Read internal status.
					"L"	↑	"H"	"H"	Write parameter or display data.
					"L"	"H"	↑	"H"	Reads parameter or display data.

4.1.6. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

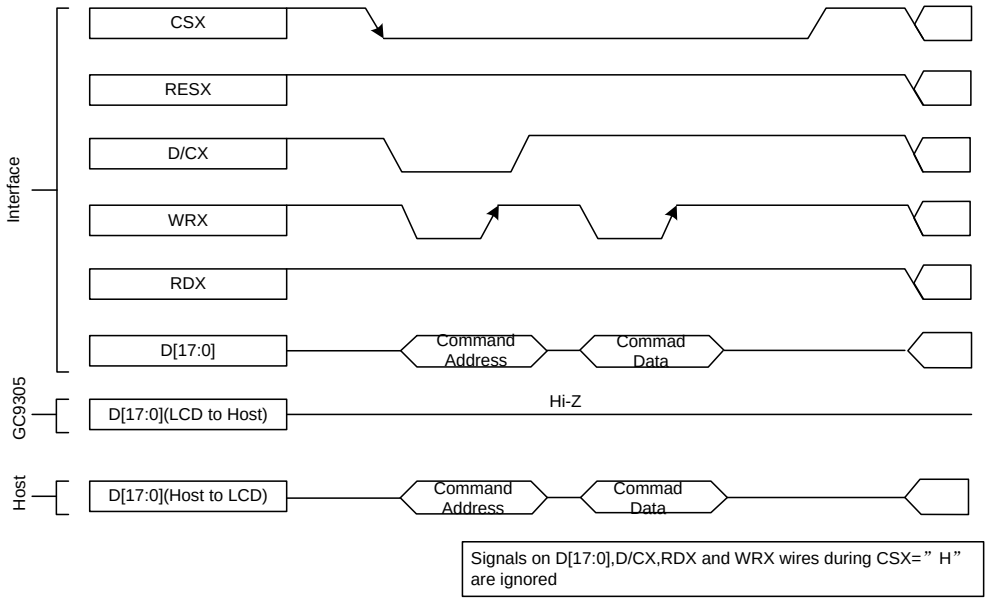
The following figure shows a write cycle for the 8080-II MCU interface.

Figure 6.



Note: WRX is an unsynchronized signal (It can be stopped)

Figure 7.

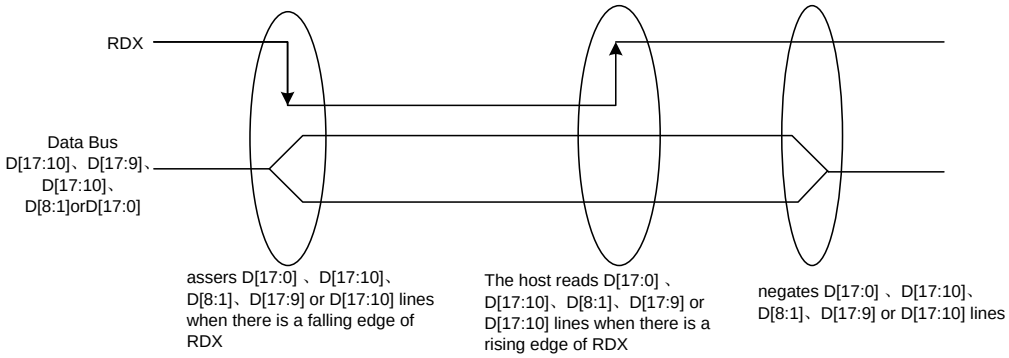


4.1.7. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

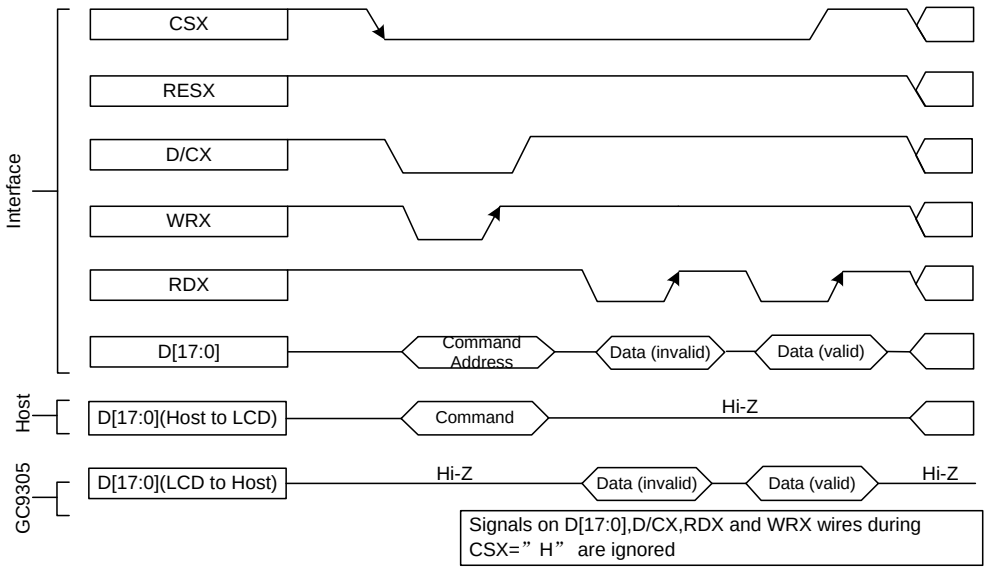
The following figure shows the read cycle for the 8080-II MCU interface.

Figure 8.



Note: RDX is an unsynchronized signal (It can be stopped).

Figure 9.



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

4.1.8. Serial Interface

The selection of interface is done by IM [3:0] bits. Please refer to the Table in the following.

Table 8.

IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	D/CX	SCL	Function
0	1	0	1	3-line serial interface	“L”	-		Read/Write command, parameter or display data.
0	1	1	0	4-line serial interface	“L”	"H/L"		Read/Write command, parameter or display data.
1	1	0	1	3-line serial interface	“L”	-		Read/Write command, parameter or display data.
1	1	1	0	4-line serial interface	“L”	"H/L"		Read/Write command, parameter or display data.

GC9306 supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between host and GC9306. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO). The 4-line serial mode consists of the Data/ Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO) for data transmission. The data bus (D [17:0]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

4.1.9. Write Cycle Sequence

The write mode of the interface means that host writes commands or data to GC9306. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is “low”, the transmission byte is interpreted as a command byte. If the D/CX bit is “high”, the transmission byte is stored as the display data RAM(Memory write command),or command register as parameter.

Any instruction can be sent in any order to GC9306 and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.

Figure 10.

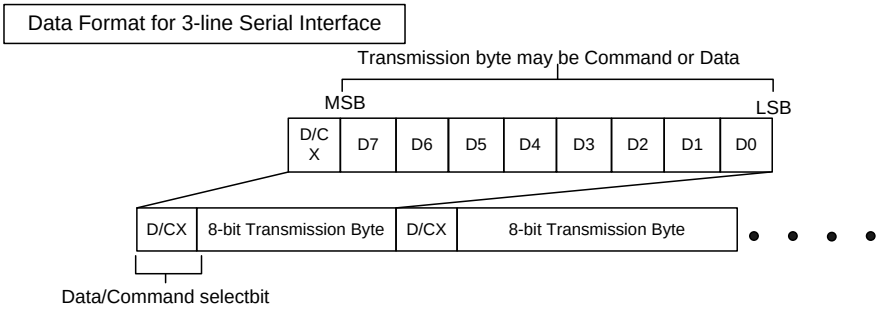
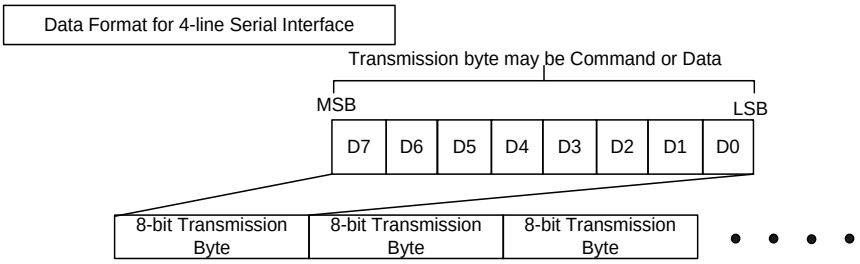


Figure11.



Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by GC9306 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.

Figure 12.

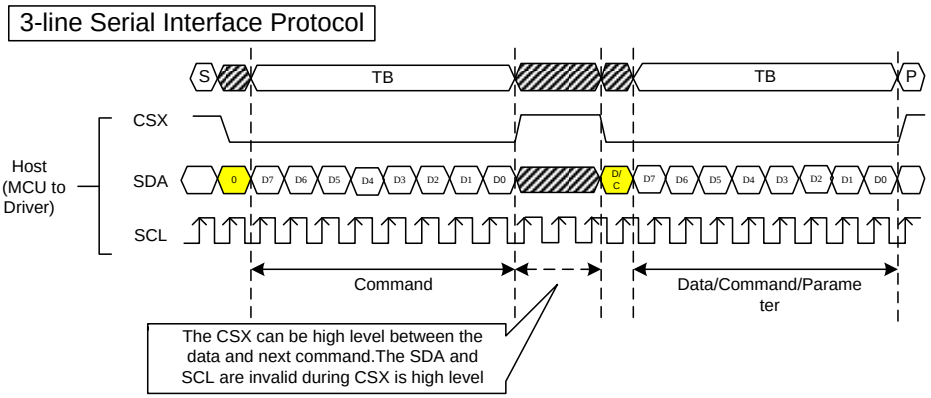
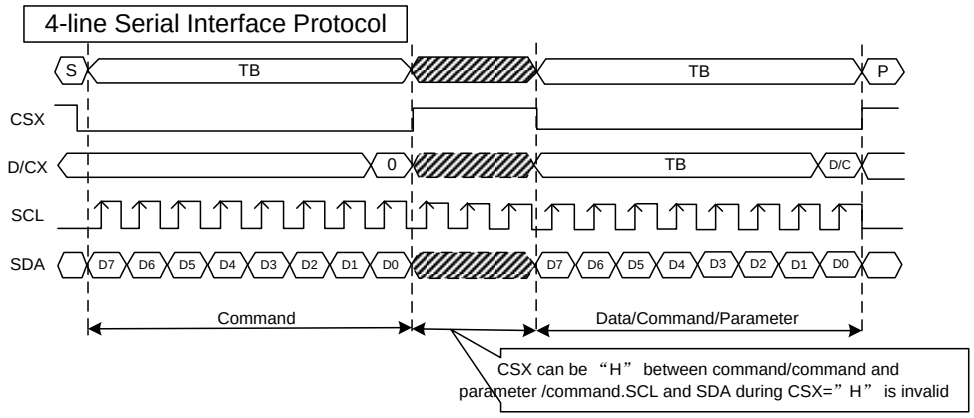


Figure 13.



4.1.10. Read Cycle Sequence

The read mode of interface means that the host reads register's parameter from GC9306. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. GC9306 latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

Figure 14.

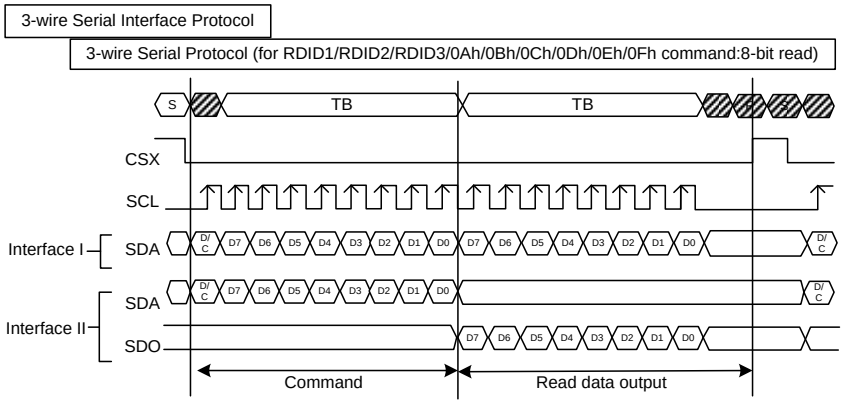


Figure 15.

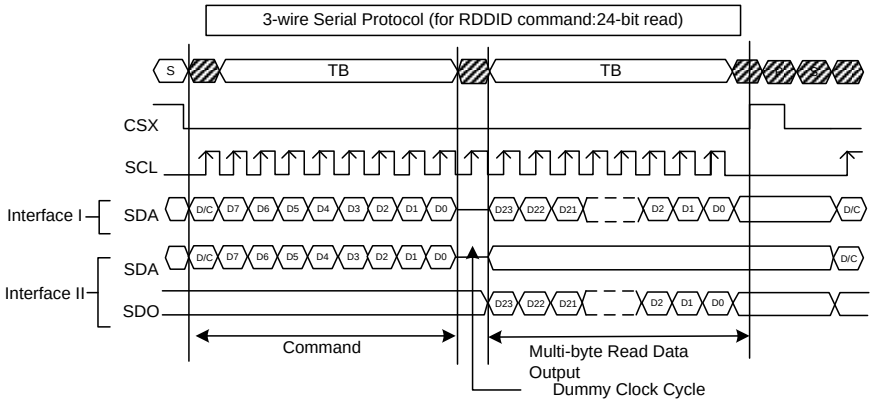


Figure 16.

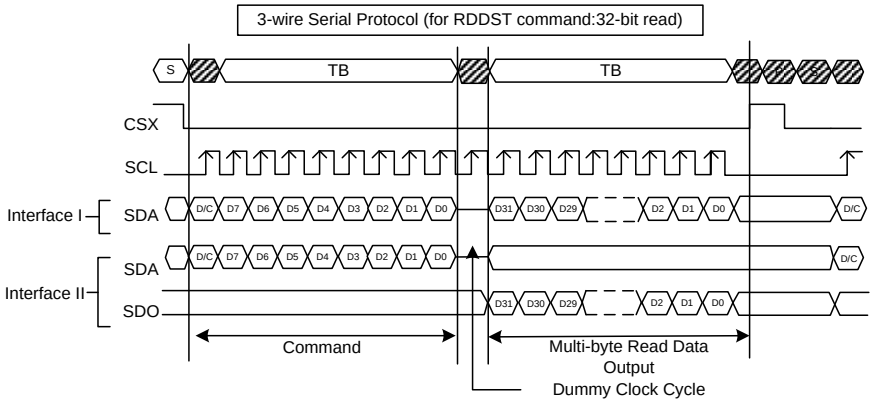


Figure 17.

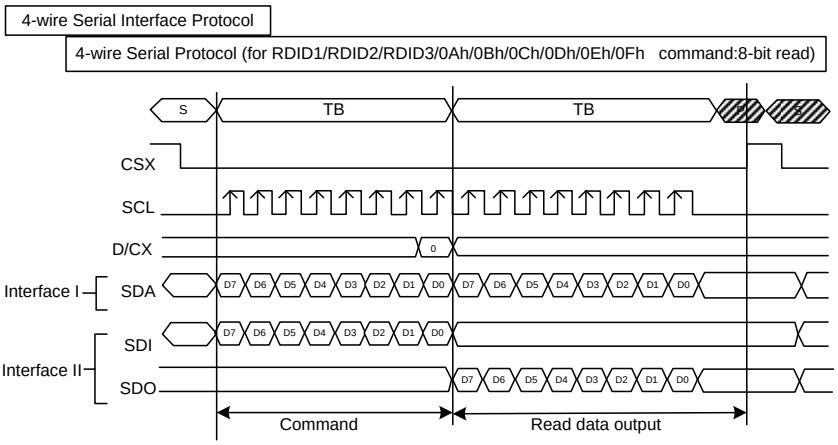


Figure 18.

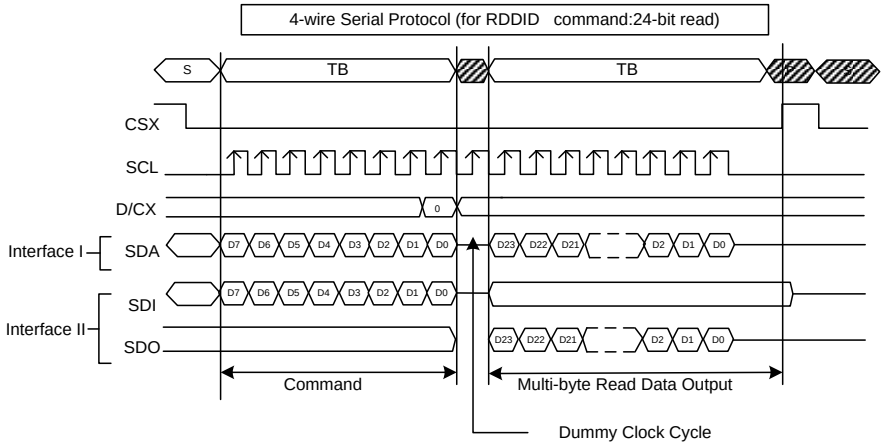
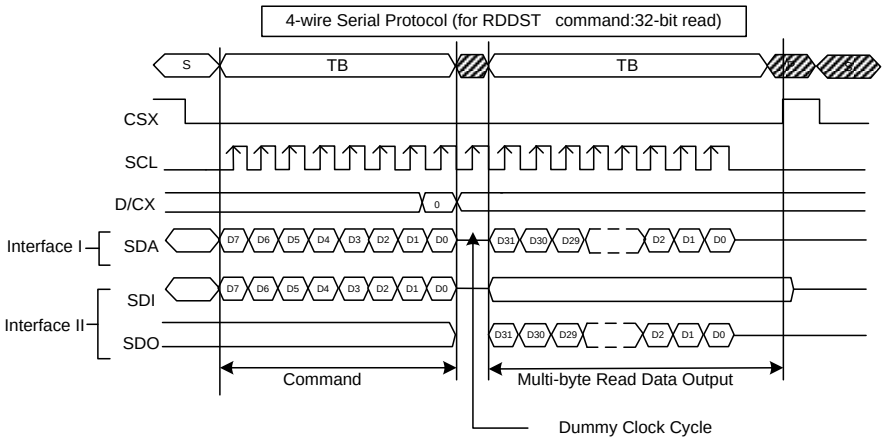


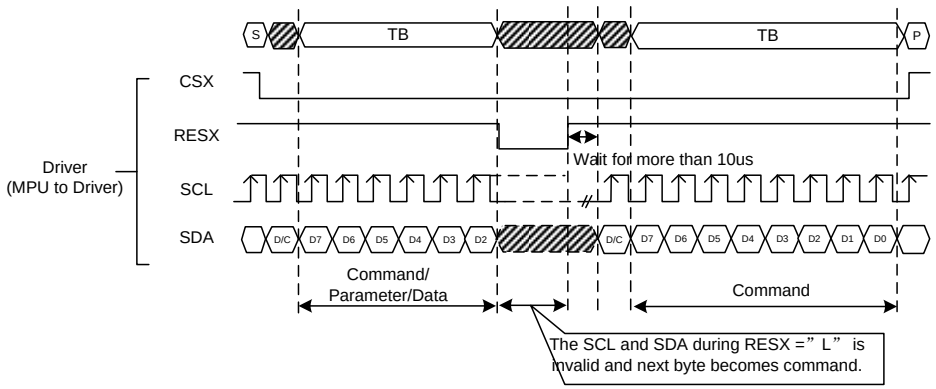
Figure 19.



4.1.11. Data Transfer Break and Recovery

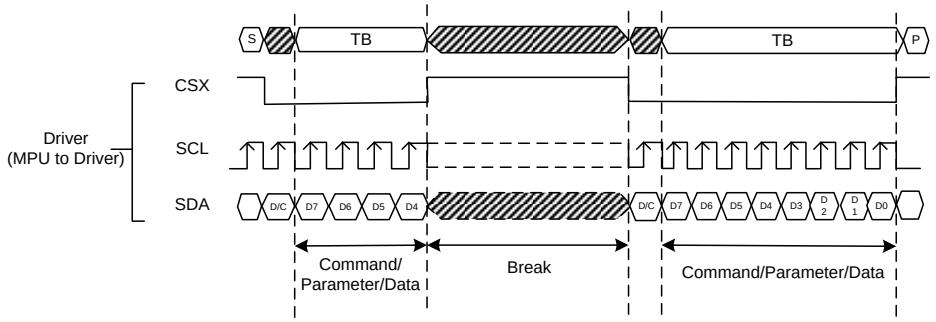
If there is a break in data transmission by RESX pulse, while transferring a command or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.

Figure 20.



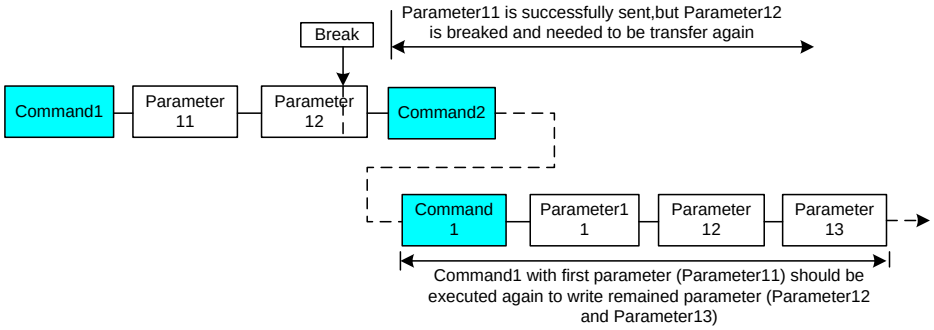
If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.

Figure 21.



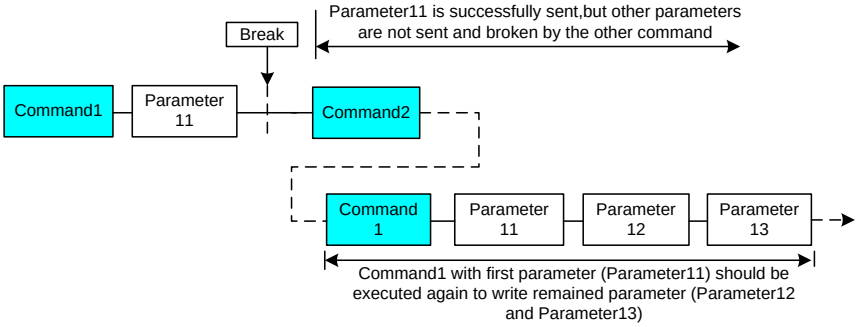
If a two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

Figure 22.



If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.

Figure 23.



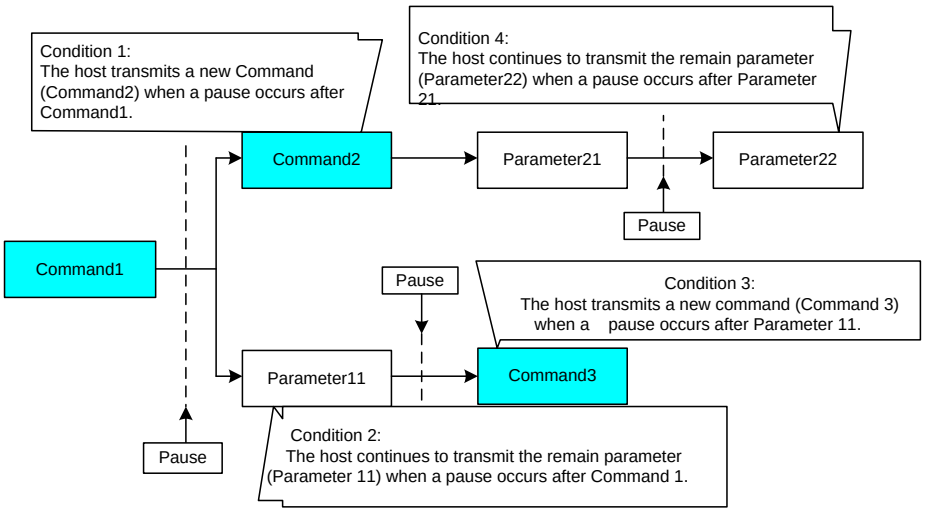
4.1.12. Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then GC9306 will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters(if appropriate) or a new command when the chip select pin is next enabled as shown below.

This applies to the following 4 conditions:

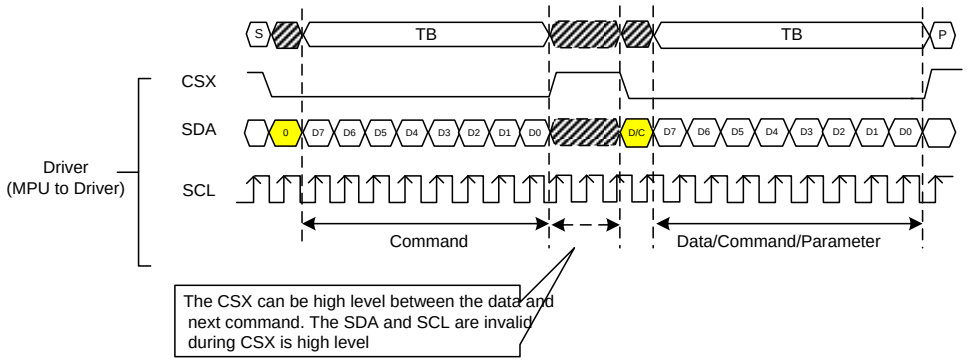
1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter

Figure 24.



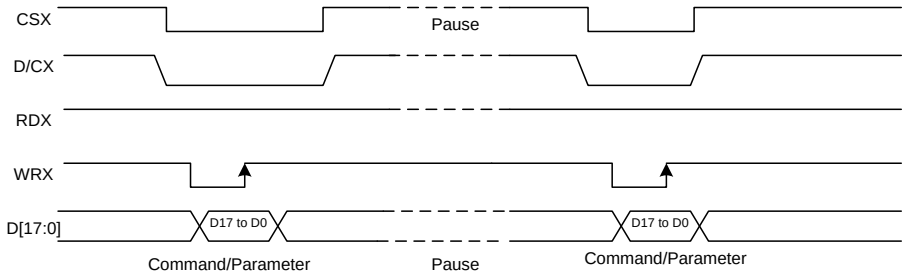
4.1.13. Serial Interface Pause (3_wire)

Figure 25.



4.1.14. Parallel Interface Pause

Figure 26.



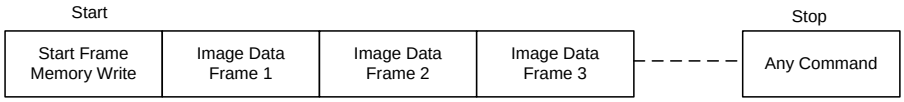
4.1.15. Data Transfer Mode

GC9306 can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

4.1.16. Data Transfer Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.

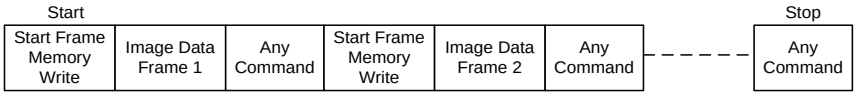
Figure 27.



4.1.17. Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.

Figure 28.



Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

4.2. RGB Interface

4.2.1. RGB Interface Selection

GC9306 has two kinds of RGB interface and these interfaces can be selected by RCM [1:0] bits. When RCM [1:0] bits are set to “10”, the DE mode is selected which utilizes VSYNC, HSYNC, DOTCLK, DE, D [17:0] pins; when RCM [1:0] bits are set to “11”, the SYNC mode is selected which utilizes which utilizes VSYNC, HSYNC,DOTCLK, D [17:0] pins. Using RGB interface must selection serial interface.
GC9306 supports several pixel formats that can be selected by RIM bit of F6h command. The selection of a given interfaces is done by setting RCM [1:0] as show in the following table.

Table 9

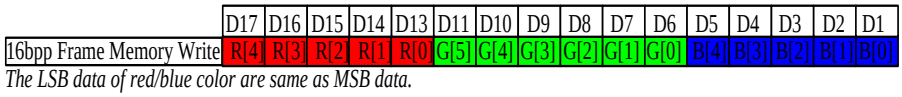
RCM[1:0]		RIM	DPI[1:0]			RGB interface Mode	RGB Mode	Used Pins
1	0	0	1	1	0	18-bit RGB interface (262K colors)	DE Mode Valid data is determined by the DE signal	VSYNC,HSYNC,DE,DOTCLK,D[17:0]
1	0	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC,HSYNC,DE,DOTCLK,D[17:13] & D[11:1]
1	0	1	-			6-bit RGB interface (262K colors)		VSYNC,HSYNC,DE,DOTCLK,D[5:0]
1	1	0	1	1	0	18-bit RGB interface (262K colors)	SYNC Mode In SYNC mode, DE signal is ignored;blanking porch is determined by B5h command	VSYNC,HSYNC,DOTCLK, D[17:0]
1	1	0	1	0	1	16-bit RGB interface (65K colors)		VSYNC,HSYNC,DOTCLK, D[17:13] & D[11:1]
1	1	1	-			6-bit RGB interface (262K colors)		VSYNC,HSYNC,DOTCLK, D[5:0]

18-bit data bus interface (D[17:0] is used) , RIM=0

Figure 29.

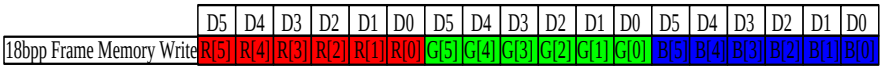
16-bit data bus interface (D[17:13] & D[11:1] is used) , DPI[2:0] = 101, and RIM=0

Figure 30.



6-bit data bus interface (D[5:0] is used) , RIM=1

Figure 31.



Pixel clock (DOTCLK) is running all the time without stopping and used to enter VSYNC, HSYNC, DE and D[17:0] states when there is a rising edge of the DOTCLK. Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

In DE mode, Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the DOTCLK signal. D [17:0] are used to tell what is the information of the image that is transferred on the display (When DE= '0' (low) and there is a rising edge of DOTCLK). D [17:0] can be '0' (low) or '1' (high). These lines are read by a rising edge of the DOTCLK signal. In SYNC mode, the valid display data in inputted in pixel unit via D [17:0] according to HFP/HBP settings of HSYNC signal and VFP/VBP setting of VSYNC. In both RGB interface modes, the input display data is written to GRAM first then outputs corresponding source voltage according the gray data from GRAM.

Figure32.

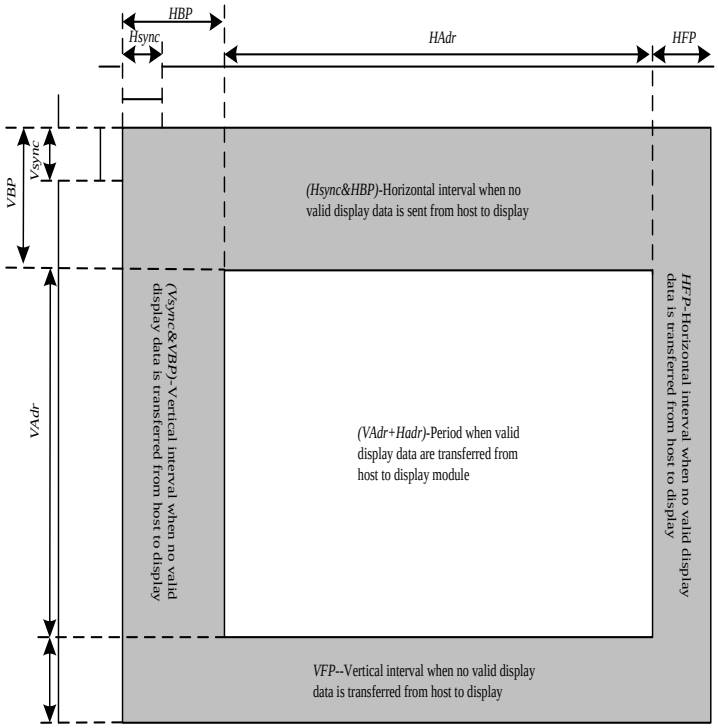


Table 10.

Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Address	HAdr		-	240	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	320	-	Line

Vertical Front Porch	VFP		3	4	-	Line

Notes:

1. Vertical period (one frame) shall be equal to the sum of VBP + VAdr + VFP.

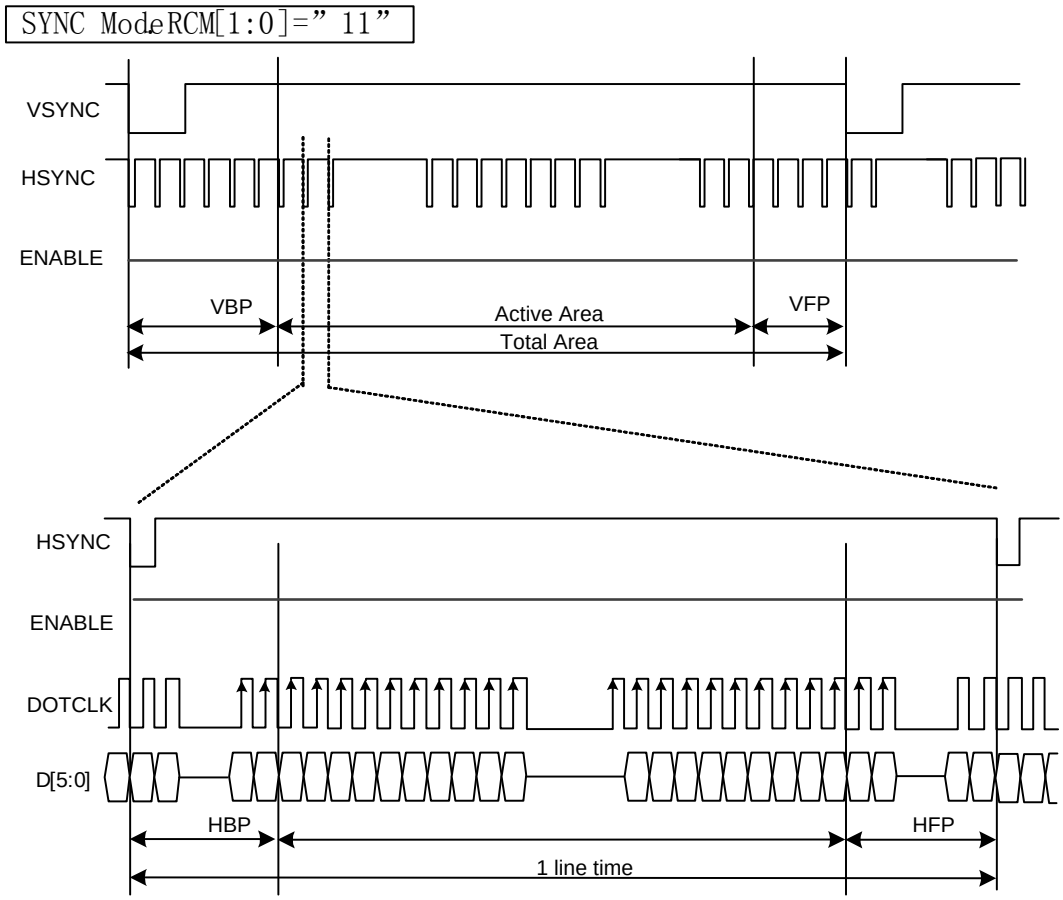
2. Horizontal period (one line) shall be equal to the sum of HBP + HAdr + HFP.

3. Control signals Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

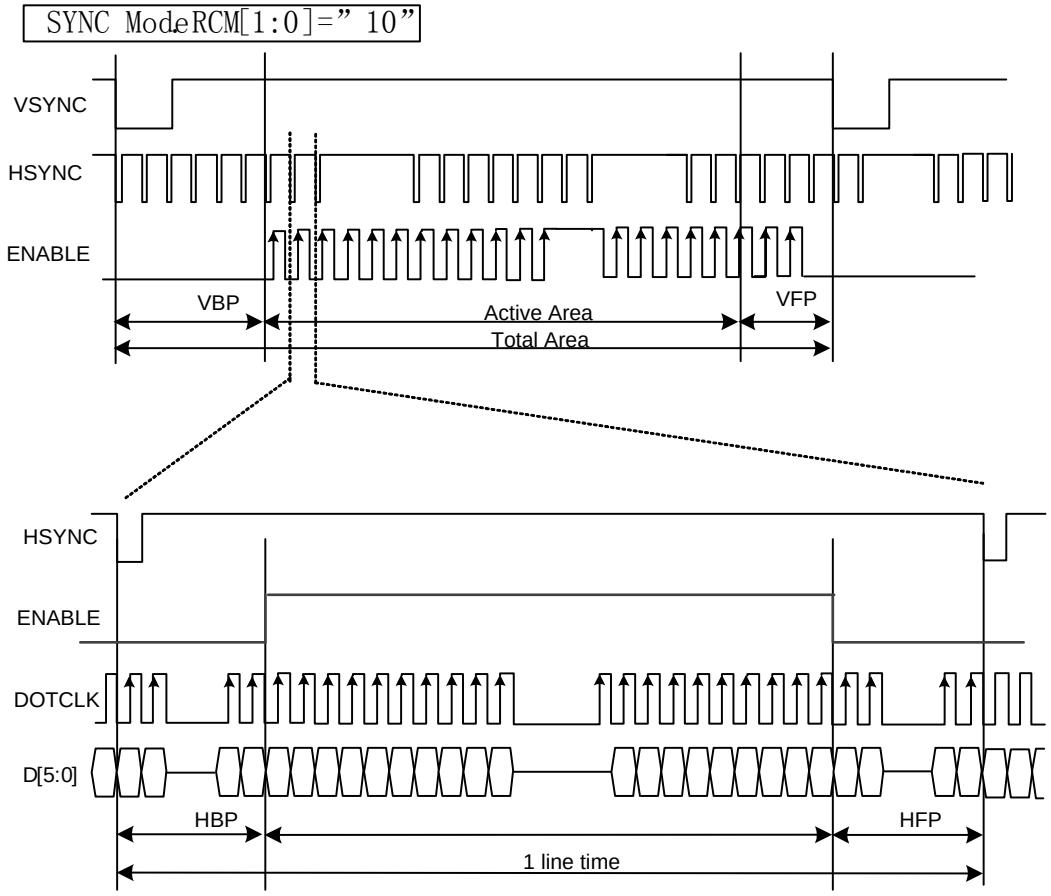
4.2.2. RGB Interface Timing

The timing chart of 18/16-bit RGB interface mode1 and mode 2 is shown as below.

Figure33.



Mode1 RGB SYNC mode



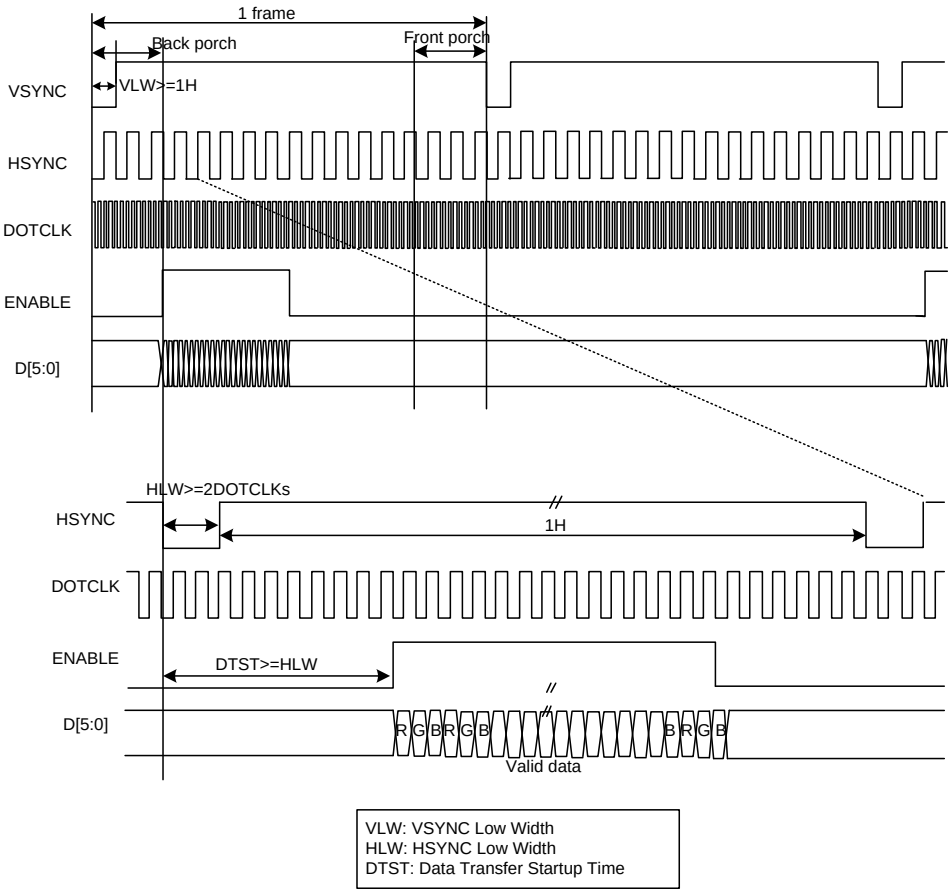
Mode2 RGB SYNC+DE mode

Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.

The timing chart of 6-bit RGB interface mode is shown as below:

Figure34.



Note 1: 6-bit RGB interface mode only used in the DE interface.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.

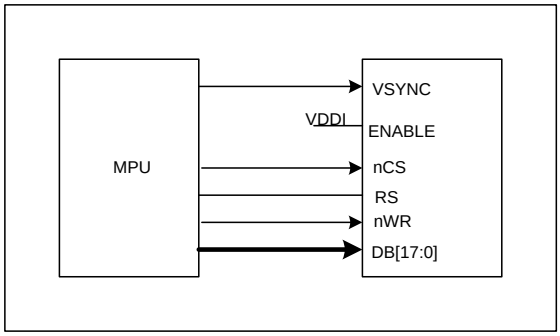
Note 3: In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLK.

Note 4: In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and DE to 3 multiples of DOTCLK.

4.3. VSYNC Interface

GC9306 supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the 8080-Ⅰ/8080-Ⅱ system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = “10” and RM = “0”.

Figure35.



Note 1:In the VSYNC mode,the pin ENABLE should connect to IOVCC.

In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.

Figure36.

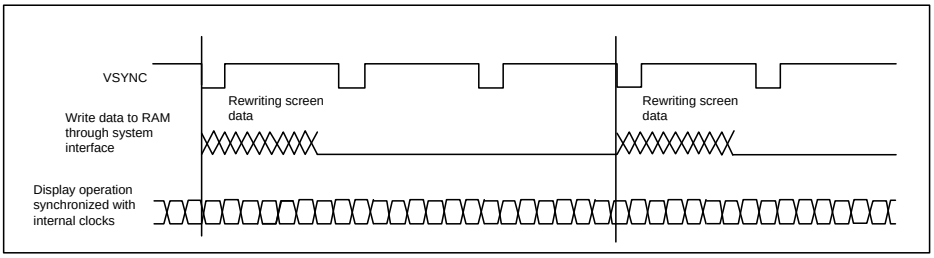
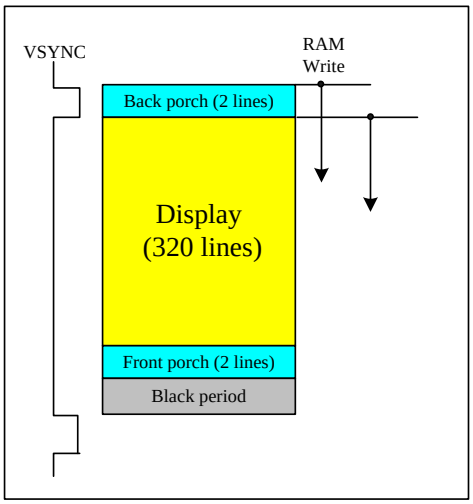


Figure37.



Notes in using the VSYNC interface

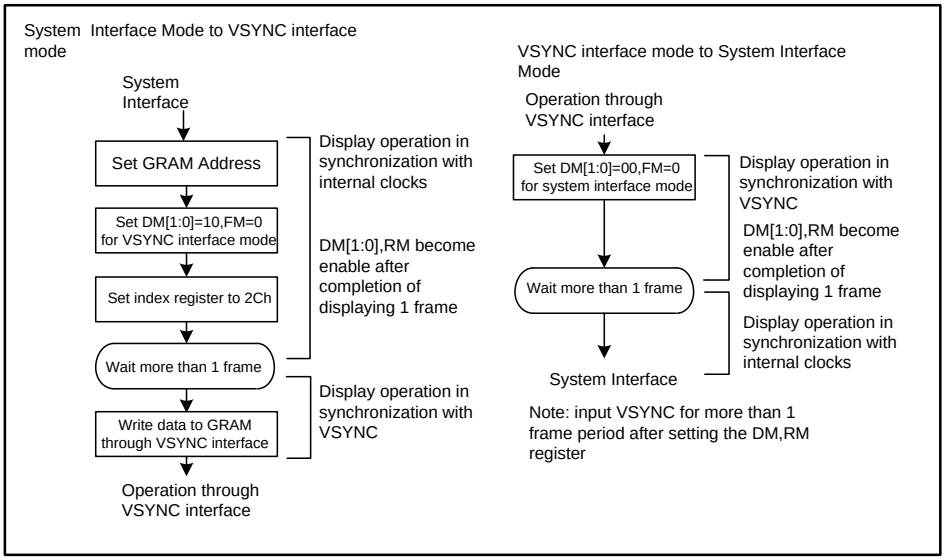
1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into consideration.

2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.

3. When switching from the internal clock operation mode (DM[1:0] = “00”) to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.

4. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode.

Figure38.



4.4. Display Data RAM (DDRAM)

GC9306 has an integrated 240x320x18-bit graphic type static RAM. This 172,800-byte memory allows storing a 240xRGBx320 image with an 18-bit resolution (262K-color). There is no abnormal visible effect on the display when there are simultaneous panel display read and interface read/write to the same location of the frame memory.

4.5. Display Data Format

GC9306 supplies 18-/16-/9-/8-bit parallel MCU interface with 8080-Ⅰ/8080-Ⅱ series, 3-/4-line serial interface and 6-/16-18-bit parallel RGB interface. The parallel MCU interface and serial interface mode can be selected by external pins IM [3:0] and RGB interface mode can be selected by software command parameters RCM[1:0].

4.5.1. 3-line Serial Interface

The 3-line/9-bit serial bus interface of GC9306 can be used by setting external pin as IM [3:0] to “0101” for serial interface I or IM [3:0] to “1101” for serial interface II. The shown figure is the example of 3-line SPI

interface.

Figure39.

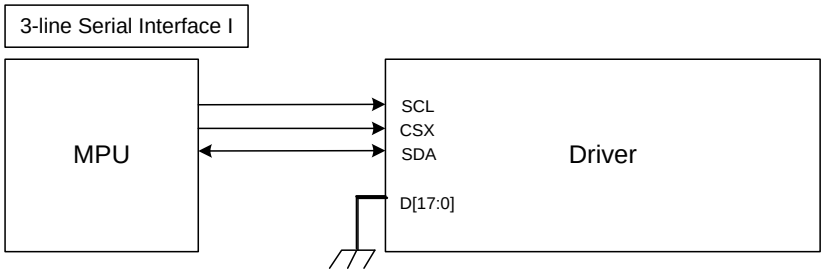
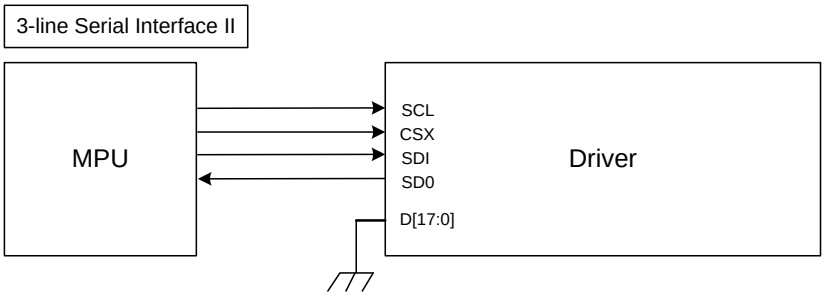


Figure40.



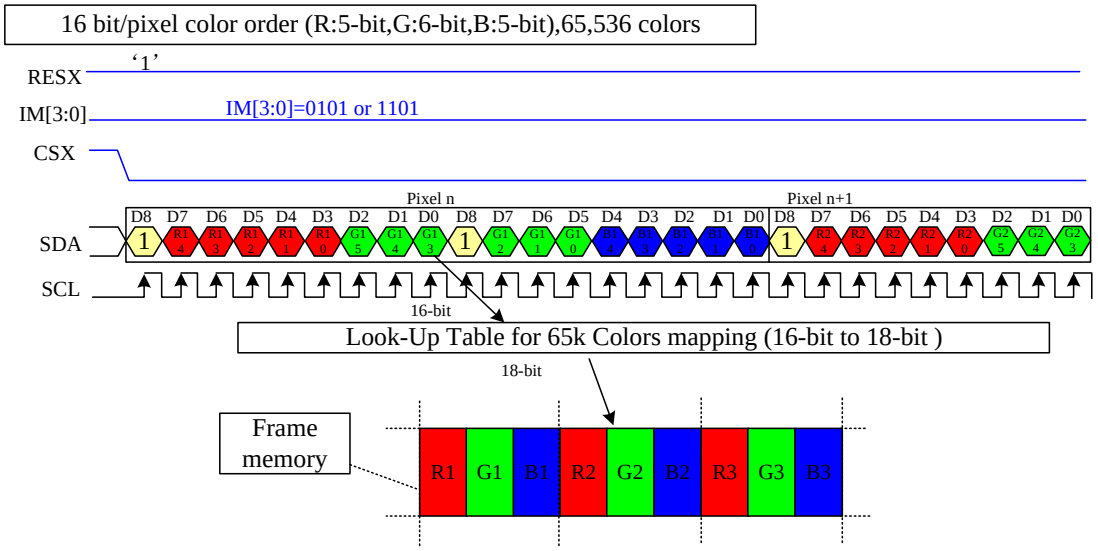
In 3-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-65k colors, RGB 5, 6, 5 -bits input

-262k colors, RGB 6, 6, 6 -bits input.

1)65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

Figure41.



Note 1: The pixel data with 16-bit color depth information.

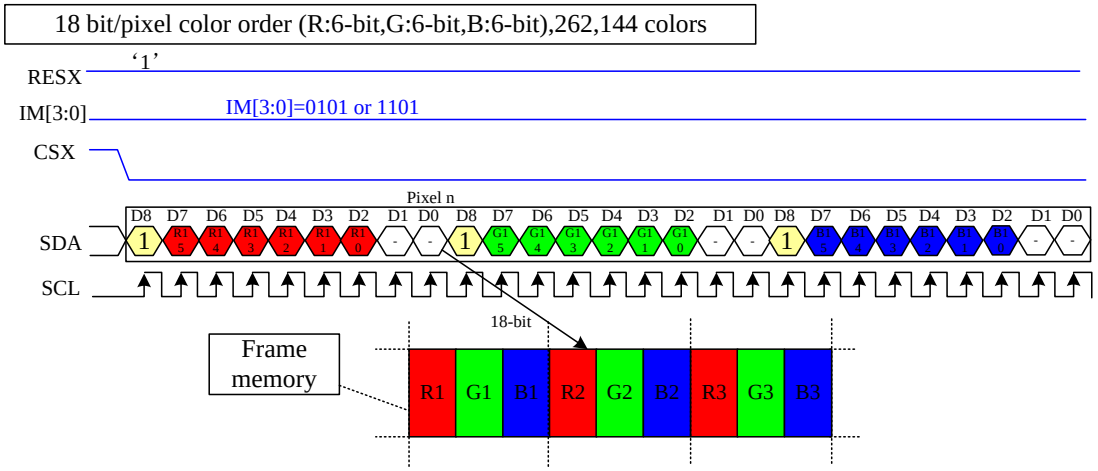
Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

2)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

Figure42.



Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are : Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care - Can be set "0" or "1".

4.5.2. 4-line Serial Interface

The 4-line/8-bit serial bus interface of GC9306 can be used by setting external pin as IM [3:0] to “0110” for serial interface I or IM [3:0] to “1110” for serial interface II. The shown figure is the example of 4-line SPI interface.

Figure43.

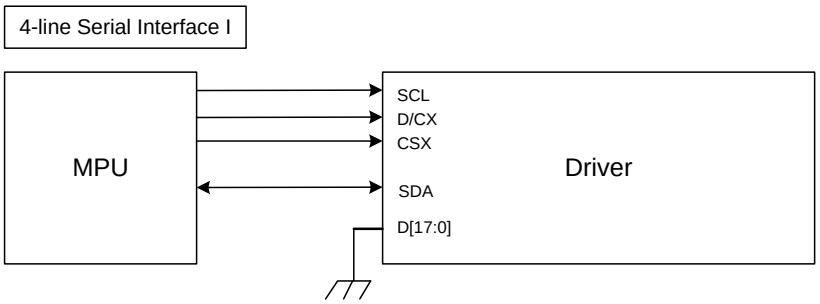
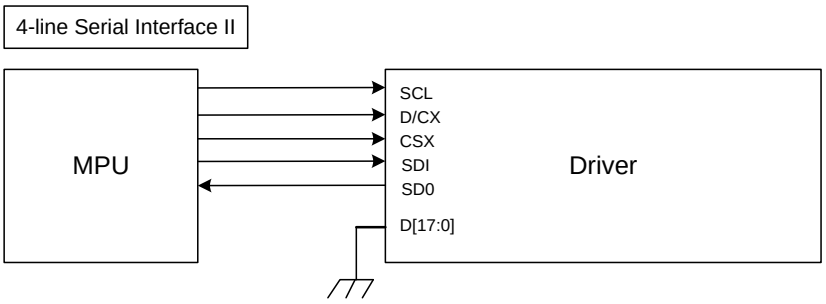


Figure44.

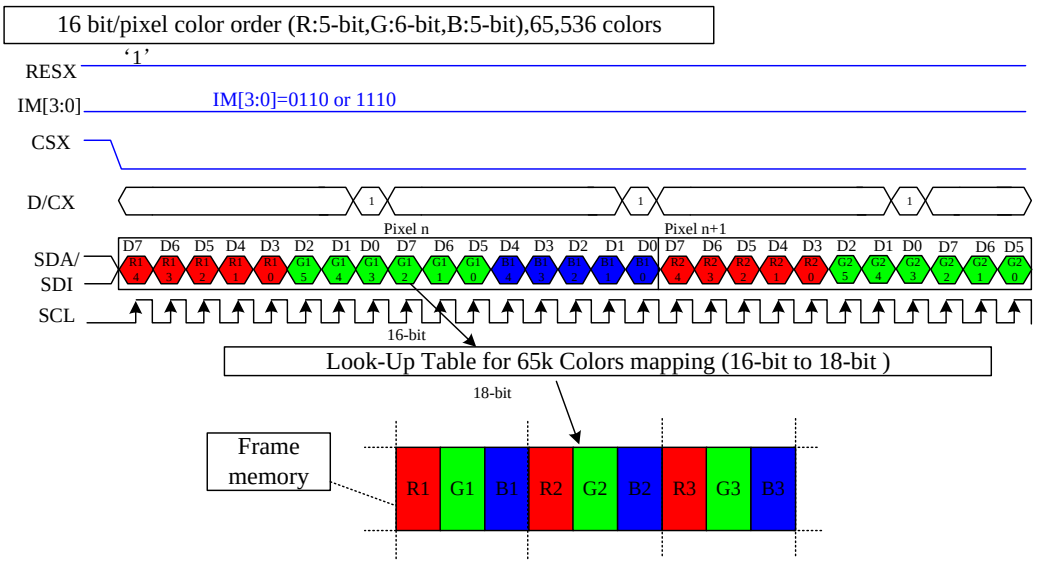


In 4-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-65k colors, RGB 5, 6, 5 -bits input.

-262k colors, RGB 6, 6, 6 -bits input.

Figure45.



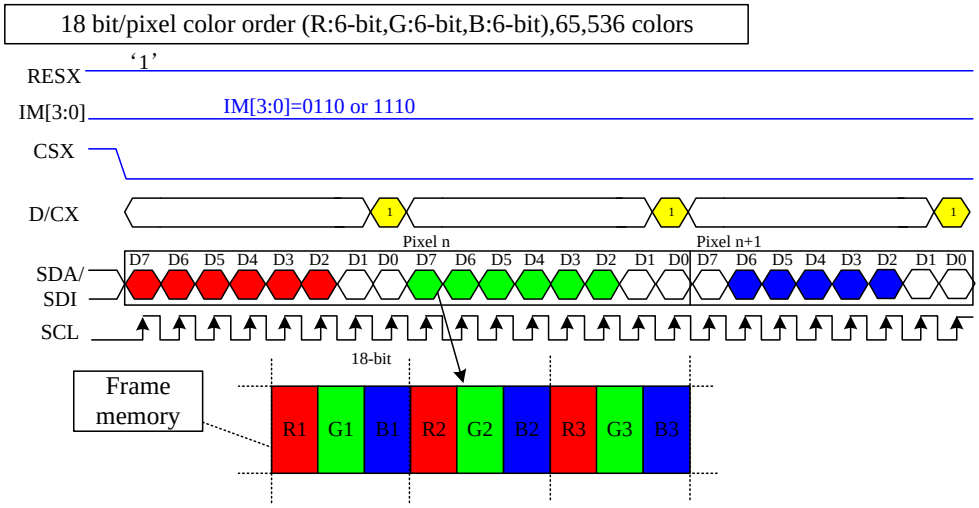
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

Figure46.



Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= Don't care –Can be set "0" or "1".

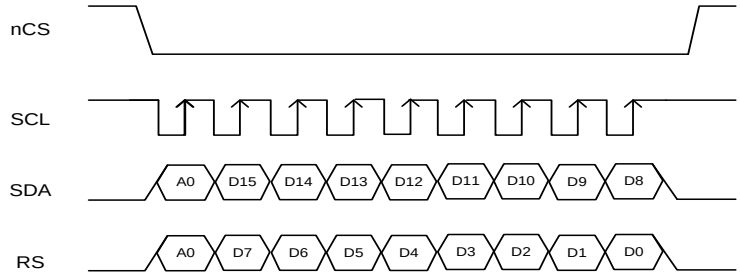
4.5.3. 2-data-line mode

This mode is active when 2data_en (E9h[3]) set to “1” in 3-wire. Only frame pixle data write transitions are sent in 2-data-line mode, register write/read is still sent in 3-wire.

The chip-select nCS (active low) enables and disables the serial interface. SCL is the serial data clock. SDA and RS are serial data lines.

Serial data must be input to SDA in the sequence A0, D15 to D10 and RS in the sequence A0, D7 to D0. The GC9306 reads the data at the rising edge of SCL signal. The first bit of serial data A0 is data/command flag. It must be set to "1", D15 to D0 bits are display RAM data.

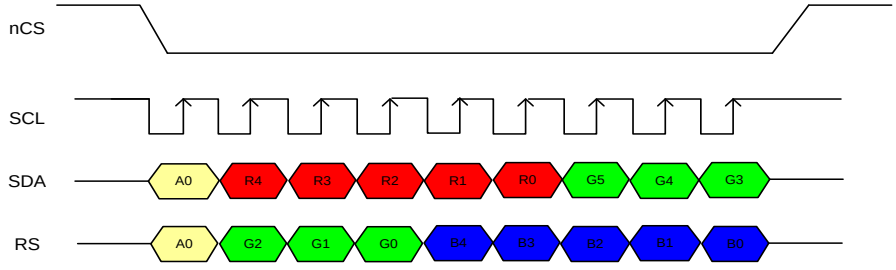
Figure47.



Five data formats are supported in 2-data-line mode, which is indicated by 2data_mdt (E9h[2:0]) .

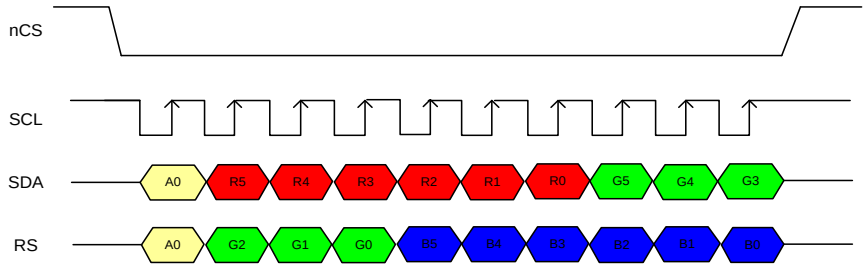
1)RGB565 1pixel/transition(65K color,2data_mdt[2:0]=’000’)

Figure48.



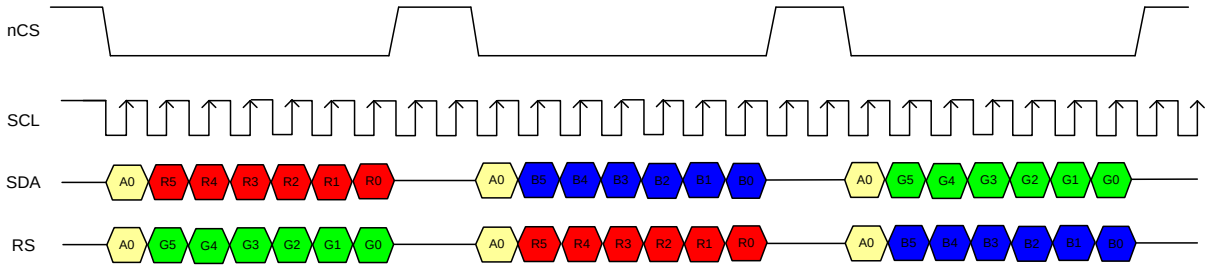
2)RGB666 1pixel/transition(262K color,2data_mdt[2:0]=’001’)

Figure49.



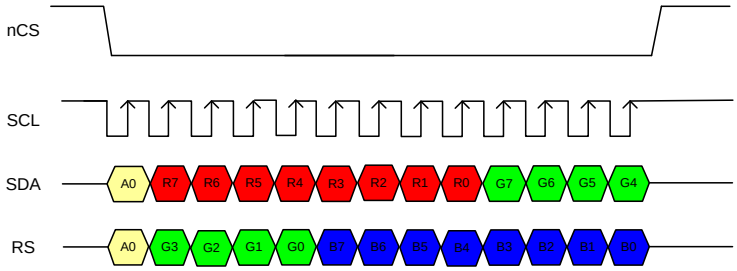
3)RGB666 2/3pixel/transition(262K color,2data_mdt[2:0]=’010’)

Figure50.



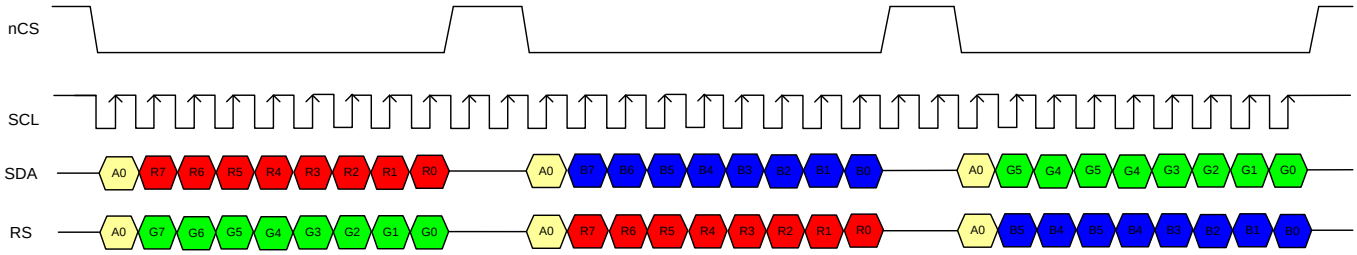
4)RGB888 1pixel/transition(4M color,2data_mdt[2:0]=’100’)

Figure51.



5)RGB888 2/3pixel/transition(4M color,2data_mdt[2:0]=’110’)

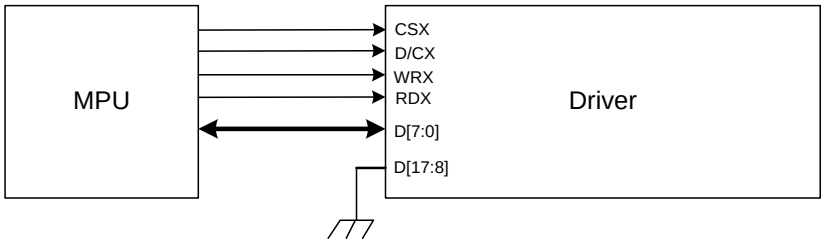
Figure52.



4.5.4. 8-bit Parallel MCU Interface

The 8080-Ⅰsystem 8-bit parallel bus interface of GC9306 can be used by setting external pin as IM [3:0] to“0000”.The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.

Figure53.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1) 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to “101”.

Table 11.

Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D7	C7	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

2) 262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to “110”.

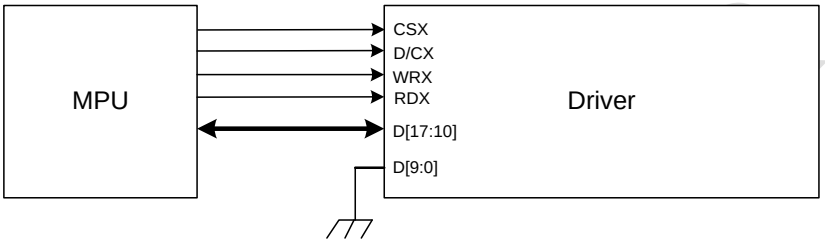
Table12.

Count	0	1	2	3	…	718	719	720
D/CX	0	1	1	1	…	1	1	1
D7	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	…	239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	…	239R2	239G2	239B2

D3	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D1	C1				…			
D0	C0				…			

The 8080-II system 8-bit parallel bus interface of GC9306 can be used by settings as IM [3:0] =”1001”. The following shown figure is the example of interface with 8080-Ⅱ MCU system interface.

Figure54.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1) 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to “101”.

Table13.

Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D17	C7	0R4	0G2	1R4	1G2	…	238R4	238G2	239R4	239G2
D16	C6	0R3	0G1	1R3	1G1	…	238R3	238G1	239R3	239G1
D15	C5	0R2	0G0	1R2	1G0	…	238R2	238G0	239R2	239G0
D14	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D13	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D12	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D11	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D10	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

2) 262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to“110”.

Table14.

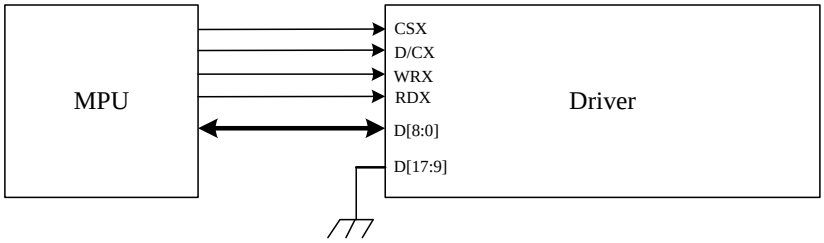
Count	0	1	2	3	…	718	719	720
D/CX	0	1	1	1	…	1	1	1
D17	C7	0R5	0G5	0B5	…	239R5	239G5	239B5
D16	C6	0R4	0G4	0B4	…	239R4	239G4	239B4
D15	C5	0R3	0G3	0B3	…	239R3	239G3	239B3

D14	C4	0R2	0G2	0B2	…	239R2	239G2	239B2
D13	C3	0R1	0G1	0B1	…	239R1	239G1	239B1
D12	C2	0R0	0G0	0B0	…	239R0	239G0	239B0
D11	C1				…			
D10	C0				…			

4.5.5. 9-bit Parallel MCU Interface

The 8080-I system 9-bit parallel bus interface of GC9306 can be selected by setting hardware pin IM [3:0] to “0010”. The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.

Figure55.



1)262K-Colors,:18-bit/pixel(RGB 6, 6, 6 -bits input).

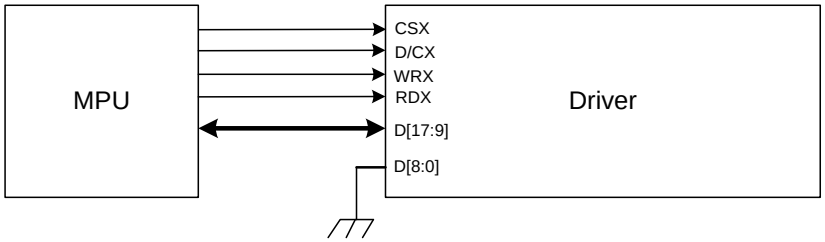
There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to “110”.

Table15.

Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D8		0R5	0G2	1R5	1G2	…	238R5	238G2	239R5	239G2
D7	C7	0R4	0G1	1R4	1G1	…	238R4	238G1	239R4	239G1
D6	C6	0R3	0G0	1R3	1G0	…	238R3	238G0	239R3	239G0
D5	C5	0R2	0B5	1R2	1B5	…	238R2	238B5	239R2	239B5
D4	C4	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

The 8080- Ⅱ system 9-bit parallel bus interface of GC9306 can be selected by setting hardware pin IM [3:0] to “1011”. The following shown figure is the example of interface with 8080- MCU system interface.

Figure56.



1)262K-Colors,:18-bit/pixel(RGB 6, 6, 6 -bits input).

There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to “110”.

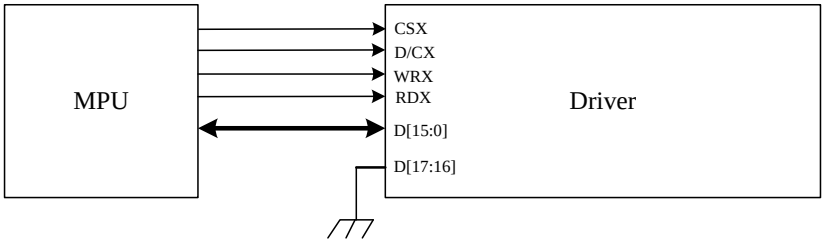
Table16.

Count	0	1	2	3	4	…	477	478	479	480
D/CX	0	1	1	1	1	…	1	1	1	1
D17	C7	0R5	0G2	1R5	1G2	…	238R5	238G2	239R5	239G2
D16	C6	0R4	0G1	1R4	1G1	…	238R4	238G1	239R4	239G1
D15	C5	0R3	0G0	1R3	1G0	…	238R3	238G0	239R3	239G0
D14	C4	0R2	0B5	1R2	1B5	…	238R2	238B5	239R2	239B5
D13	C3	0R1	0B4	1R1	1B4	…	238R1	238B4	239R1	239B4
D12	C2	0R0	0B3	1R0	1B3	…	238R0	238B3	239R0	239B3
D11	C1	0G5	0B2	1G5	1B2	…	238G5	238B2	239G5	239B2
D10	C0	0G4	0B1	1G4	1B1	…	238G4	238B1	239G4	239B1
D9		0G3	0B0	1G3	1B0	…	238G3	238B0	239G3	239B0

4.5.6. 16-bit Parallel MCU Interface

The 8080-Ⅰsystem 16-bit parallel bus interface of GC9306 can be selected by setting hardware pin IM[3:0] to “0001”.The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.

Figure57.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1)65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “101”.

Table17.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D15		0R4	1R4	2R4	…	237R4	238R4	239R4
D14		0R3	1R3	2R3	…	237R3	238R3	239R3
D13		0R2	1R2	2R2	…	237R2	238R2	239R2
D12		0R1	1R1	2R1	…	237R1	238R1	239R1
D11		0R0	1R0	2R0	…	237R0	238R0	239R0
D10		0G5	1G5	2G5	…	237G5	238G5	239G5
D9		0G4	1G4	2G4	…	237G4	238G4	239G4
D8		0G3	1G3	2G3	…	237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

2)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to “110”.

1)MDT[1:0]=“00”

Table18.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D15		0R5	0B5	1G5	…	238R5	238B5	239G5
D14		0R4	0B4	1G4	…	238R4	238B4	239G4
D13		0R3	0B3	1G3	…	238R3	238B3	239G3
D12		0R2	0B2	1G2	…	238R2	238B2	239G2
D11		0R1	0B1	1G1	…	238R1	238B1	239G1
D10		0R0	0B0	1G0	…	238R0	238B0	239G0
D9								
D8								
D7	C7	0G5	1R5	1B5	…	238G5	239R5	239B5
D6	C6	0G4	1R4	1B4	…	238G4	239R4	239B4
D5	C5	0G3	1R3	1B3	…	238G3	239R3	239B3
D4	C4	0G2	1R2	1B2	…	238G2	239R2	239B2
D3	C3	0G1	1R1	1B1	…	238G1	239R1	239B1
D2	C2	0G0	1R0	1B0	…	238G0	239R0	239B0
D1	C1							
D0	C0							

2)MDT[1:0]=“01”

Table19.

Count	0	1	2	3		…	357	358	479	480
D/CX	0	1	1	1		…	1	1	1	1
D15		0R5	0B5	1R5	1B5	…	238R5	238B5	239R5	239B5
D14		0R4	0B4	1R4	1B4	…	238R4	238B4	239R4	239B4
D13		0R3	0B3	1R3	1B3	…	238R3	238B3	239R3	239B3
D12		0R2	0B2	1R2	1B2	…	238R2	238B2	239R2	239B2
D11		0R1	0B1	1R1	1B1	…	238R1	238B1	239R1	239B1
D10		0R0	0B0	1R0	1B0	…	238R0	238B0	239R0	239B0
D9						…				
D8						…				
D7	C7	0G5		1G5		…	238G5		239G5	
D6	C6	0G4		1G4		…	238G4		239G4	
D5	C5	0G3		1G3		…	238G3		239G3	
D4	C4	0G2		1G2		…	238G2		239G2	
D3	C3	0G1		1G1		…	238G1		239G1	
D2	C2	0G0		1G0		…	238G0		239G0	
D1	C1					…				
D0	C0					…				

3)MDT[1:0]=“10”

Table20.

Count	0	1	2	3		…	357	358	479	480
D/CX	0	1	1	1		…	1	1	1	1
D15		0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D14		0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0
D13		0R3		1R3		…	238R3		239R3	
D12		0R2		1R2		…	238R2		239R2	
D11		0R1		1R1		…	238R1		239R1	
D10		0R0		1R0		…	238R0		239R0	
D9		0G5		1G5		…	238G5		239G5	
D8		0G4		1G4		…	238G4		239G4	
D7	C7	0G3		1G3		…	238G3		239G3	
D6	C6	0G2		1G2		…	238G2		239G2	
D5	C5	0G1		1G1		…	238G1		239G1	
D4	C4	0G0		1G0		…	238G0		239G0	
D3	C3	0B5		1B5		…	238B5		239B5	
D2	C2	0B4		1B4		…	238B4		239B4	
D1	C1	0B3		1B3		…	238B3		239B3	
D0	C0	0B2		1B2		…	238B2		239B2	

4)MDT[1:0]= “11”

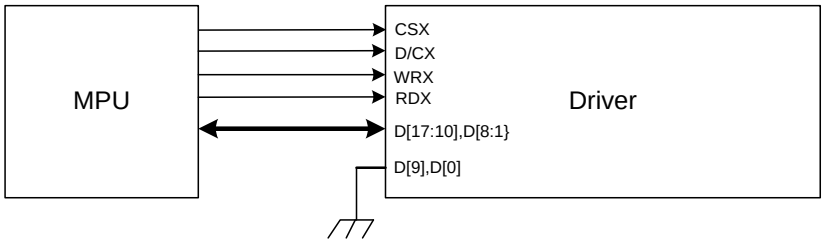
Table21.

Count	0	1	2	3		…	357	358	479	480
D/CX	0	1	1	1		…	1	1	1	1
D15			0R3		1R3	…		238R3		239R3
D14			0R2		1R2	…		238R2		239R2
D13			0R1		1R1	…		238R1		239R1
D12			0R0		1R0	…		238R0		239R0
D11			0G5		1G5	…		238G5		239G5
D10			0G4		1G4	…		238G4		239G4
D9			0G3		1G3	…		238G3		239G3
D8			0G2		1G2	…		238G2		239G2
D7	C7		0G1		1G1	…		238G1		239G1
D6	C6		0G0		1G0	…		238G0		239G0
D5	C5		0B5		1B5	…		238B5		239B5
D4	C4		0B4		1B4	…		238B4		239B4
D3	C3		0B3		1B3	…		238B3		239B3
D2	C2		0B2		1B2	…		238B2		239B2
D1	C1	0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D0	C0	0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0

The 8080-II system 16-bit parallel bus interface of GC9306 can be selected by settings IM [3:0] =”1000”.

The following shown figure is the example of interface with 8080- MCU system interface.

Figure58.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1) 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Table22.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17		0R4	1R4	2R4	…	237R4	238R4	239R4
D16		0R3	1R3	2R3	…	237R3	238R3	239R3
D15		0R2	1R2	2R2	…	237R2	238R2	239R2
D14		0R1	1R1	2R1	…	237R1	238R1	239R1
D13		0R0	1R0	2R0	…	237R0	238R0	239R0
D12		0G5	1G5	2G5	…	237G5	238G5	239G5
D11		0G4	1G4	2G4	…	237G4	238G4	239G4
D10		0G3	1G3	2G3	…	237G3	238G3	239G3
D8	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D7	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D6	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D5	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D4	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D3	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D2	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D1	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

2)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "110".

1)MDT[1:0]=00

Table23.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1

D17		0R5	0B5	1G5	…	238R5	238B5	239G5	
D16		0R4	0B4	1G4	…	238R4	238B4	239G4	
D15		0R3	0B3	1G3	…	238R3	238B3	239G3	
D14		0R2	0B2	1G2	…	238R2	238B2	239G2	
D13		0R1	0B1	1G1	…	238R1	238B1	239G1	
D12		0R0	0B0	1G0	…	238R0	238B0	239G0	
D11									
D10									
D8	C7	0G5	1R5	1B5	…	238G5	239R5	239B5	
D7	C6	0G4	1R4	1B4	…	238G4	239R4	239B4	
D6	C5	0G3	1R3	1B3	…	238G3	239R3	239B3	
D5	C4	0G2	1R2	1B2	…	238G2	239R2	239B2	
D4	C3	0G1	1R1	1B1	…	238G1	239R1	239B1	
D3	C2	0G0	1R0	1B0	…	238G0	239R0	239B0	
D2	C1								
D1	C0								

2)MDT[1:0]=01

Table24.

Count	0	1	2	3		…	357	358	479	480
D/CX	0	1	1	1		…	1	1	1	1
D17		0R5	0B5	1R5	1B5	…	238R5	238B5	239R5	239B5
D16		0R4	0B4	1R4	1B4	…	238R4	238B4	239R4	239B4
D15		0R3	0B3	1R3	1B3	…	238R3	238B3	239R3	239B3
D14		0R2	0B2	1R2	1B2	…	238R2	238B2	239R2	239B2
D13		0R1	0B1	1R1	1B1	…	238R1	238B1	239R1	239B1
D12		0R0	0B0	1R0	1B0	…	238R0	238B0	239R0	239B0
D11						…				
D10						…				
D8	C7	0G5		1G5		…	238G5		239G5	
D7	C6	0G4		1G4		…	238G4		239G4	
D6	C5	0G3		1G3		…	238G3		239G3	
D5	C4	0G2		1G2		…	238G2		239G2	
D4	C3	0G1		1G1		…	238G1		239G1	
D3	C2	0G0		1G0		…	238G0		239G0	
D2	C1					…				
D1	C0					…				

3)MDT[1:0]=10

Table25.

Count	0	1	2	3		…	357	358	479	480

D/CX	0	1	1	1		…	1	1	1	1
D17		0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D16		0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0
D15		0R3		1R3		…	238R3		239R3	
D14		0R2		1R2		…	238R2		239R2	
D13		0R1		1R1		…	238R1		239R1	
D12		0R0		1R0		…	238R0		239R0	
D11		0G5		1G5		…	238G5		239G5	
D10		0G4		1G4		…	238G4		239G4	
D8	C7	0G3		1G3		…	238G3		239G3	
D7	C6	0G2		1G2		…	238G2		239G2	
D6	C5	0G1		1G1		…	238G1		239G1	
D5	C4	0G0		1G0		…	238G0		239G0	
D4	C3	0B5		1B5		…	238B5		239B5	
D3	C2	0B4		1B4		…	238B4		239B4	
D2	C1	0B3		1B3		…	238B3		239B3	
D1	C0	0B2		1B2		…	238B2		239B2	

4)MDT[1:0]=11

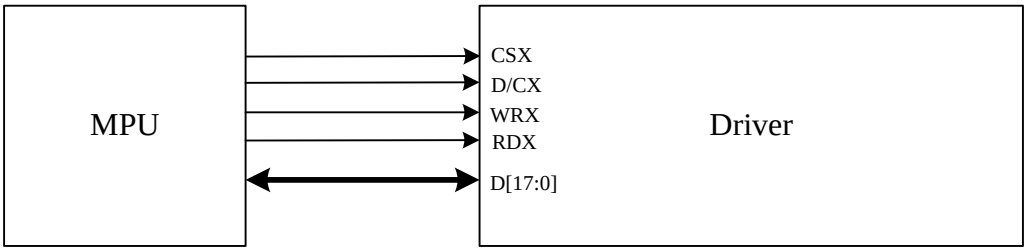
Table26.

Count	0	1	2	3		…	357	358	479	480
D/CX	0	1	1	1		…	1	1	1	1
D17			0R3		1R3	…		238R3		239R3
D16			0R2		1R2	…		238R2		239R2
D15			0R1		1R1	…		238R1		239R1
D14			0R0		1R0	…		238R0		239R0
D13			0G5		1G5	…		238G5		239G5
D12			0G4		1G4	…		238G4		239G4
D11			0G3		1G3	…		238G3		239G3
D10			0G2		1G2	…		238G2		239G2
D8	C7		0G1		1G1	…		238G1		239G1
D7	C6		0G0		1G0	…		238G0		239G0
D6	C5		0B5		1B5	…		238B5		239B5
D5	C4		0B4		1B4	…		238B4		239B4
D4	C3		0B3		1B3	…		238B3		239B3
D3	C2		0B2		1B2	…		238B2		239B2
D2	C1	0R5	0B1	1R5	1B1	…	238R5	238B1	239R5	239B1
D1	C0	0R4	0B0	1R4	1B0	…	238R4	238B0	239R4	239B0

4.5.7. 18-bit Parallel MCU Interface

The 8080-I system 18-bit parallel bus interface of GC9306 can be selected by setting hardware pin IM[3:0] to “0011”.The following shown figure is the example of interface with 8080-I MCU system interface.

Figure58.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1) 65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “101”.

Table27.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17								
D16								
D15		0R4	1R4	2R4	…	237R4	238R4	239R4
D14		0R3	1R3	2R3	…	237R3	238R3	239R3
D13		0R2	1R2	2R2	…	237R2	238R2	239R2
D12		0R1	1R1	2R1	…	237R1	238R1	239R1
D11		0R0	1R0	2R0	…	237R0	238R0	239R0
D10		0G5	1G5	2G5	…	237G5	238G5	239G5
D9		0G4	1G4	2G4	…	237G4	238G4	239G4
D8		0G3	1G3	2G3	…	237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

2)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

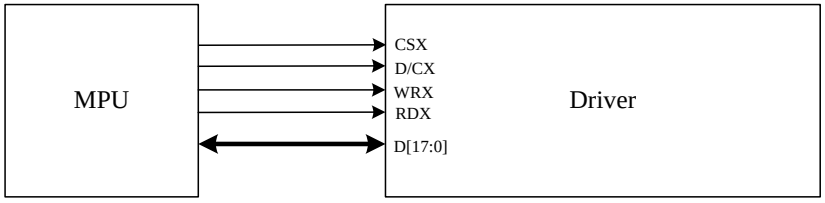
One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "110".

Table28.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17		0R5	1R5	2R5	…	237R5	238R5	239R5
D16		0R4	1R4	2R4	…	237R4	238R4	239R4
D15		0R3	1R3	2R3	…	237R3	238R3	239R3
D14		0R2	1R2	2R2	…	237R2	238R2	239R2
D13		0R1	1R1	2R1	…	237R1	238R1	239R1
D12		0R0	1R0	2R0	…	237R0	238R0	239R0
D11		0G5	1G5	2G5	…	237G5	238G5	239G5
D10		0G4	1G4	2G4	…	237G4	238G4	239G4
D9		0G3	1G3	2G3	…	237G3	238G3	239G3
D8		0G2	1G2	2G2	…	237G2	238G2	239G2
D7	C7	0G1	1G1	2G1	…	237G1	238G1	239G1
D6	C6	0G0	1G0	2G0	…	237G0	238G0	239G0
D5	C5	0B5	1B5	2B5	…	237B5	238B5	239B5
D4	C4	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	…	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	…	237B0	238B0	239B0

The 8080-II system 18-bit parallel bus interface mode can be selected by settings IM [3:0] ="1010". The following shown figure is the example of interface with 8080- MCU system interface.

Figure59.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

1)65K-Colors:16-bit/pixel(RGB 5, 6, 5 -bits input).

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Table29.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17								
D16								
D15		0R4	1R4	2R4	…	237R4	238R4	239R4
D14		0R3	1R3	2R3	…	237R3	238R3	239R3
D13		0R2	1R2	2R2	…	237R2	238R2	239R2
D12		0R1	1R1	2R1	…	237R1	238R1	239R1
D11		0R0	1R0	2R0	…	237R0	238R0	239R0
D10		0G5	1G5	2G5	…	237G5	238G5	239G5
D9		0G4	1G4	2G4	…	237G4	238G4	239G4
D8	C7	0G3	1G3	2G3	…	237G3	238G3	239G3
D7	C6	0G2	1G2	2G2	…	237G2	238G2	239G2
D6	C5	0G1	1G1	2G1	…	237G1	238G1	239G1
D5	C4	0G0	1G0	2G0	…	237G0	238G0	239G0
D4	C3	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C2	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C1	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C0	0B1	1B1	2B1	…	237B1	238B1	239B1
D0		0B0	1B0	2B0	…	237B0	238B0	239B0

2)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to “110”.

Table30.

Count	0	1	2	3	…	238	239	240
D/CX	0	1	1	1	…	1	1	1
D17		0R5	1R5	2R5	…	237R5	238R5	239R5
D16		0R4	1R4	2R4	…	237R4	238R4	239R4
D15		0R3	1R3	2R3	…	237R3	238R3	239R3
D14		0R2	1R2	2R2	…	237R2	238R2	239R2
D13		0R1	1R1	2R1	…	237R1	238R1	239R1
D12		0R0	1R0	2R0	…	237R0	238R0	239R0
D11		0G5	1G5	2G5	…	237G5	238G5	239G5
D10		0G4	1G4	2G4	…	237G4	238G4	239G4
D9		0G3	1G3	2G3	…	237G3	238G3	239G3
D8	C7	0G2	1G2	2G2	…	237G2	238G2	239G2
D7	C6	0G1	1G1	2G1	…	237G1	238G1	239G1
D6	C5	0G0	1G0	2G0	…	237G0	238G0	239G0
D5	C4	0B5	1B5	2B5	…	237B5	238B5	239B5

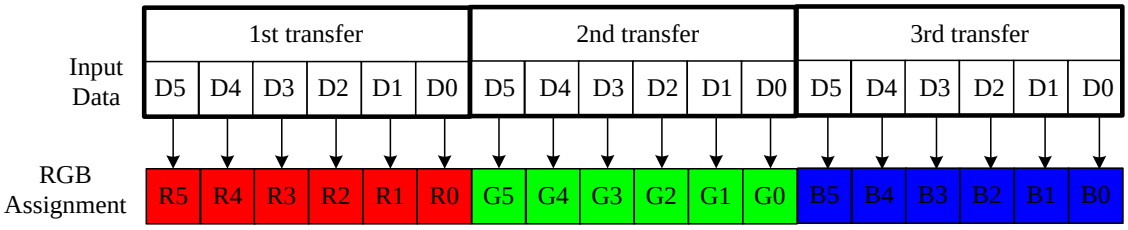
D4	C3	0B4	1B4	2B4	…	237B4	238B4	239B4
D3	C2	0B3	1B3	2B3	…	237B3	238B3	239B3
D2	C1	0B2	1B2	2B2	…	237B2	238B2	239B2
D1	C0	0B1	1B1	2B1	…	237B1	238B1	239B1
D0		0B0	1B0	2B0	…	237B0	238B0	239B0

4.5.8. 6-bit Parallel RGB Interface

The 6-bit RGB interface is selected by setting the RIM bit to “1”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (D [5:0]) according to the data enable signal (DE) when RCM [1:0] are set to “10”. the valid display data is inputted in pixel unit via D [5:0] according to the VFP/VBP and HFP/HBP settings. Unused pins must be connected to GND to ensure normally operation. Registers can be set by the SPI system interface.

1)262K-Colors:18-bit/pixel(RGB 6, 6, 6 -bits input).

Figure60.



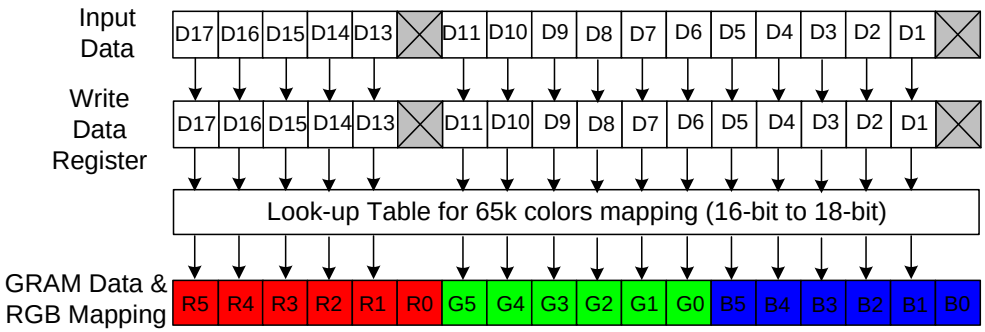
GC9306 has data transfer counters to count the first, second, third data transfer in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK).Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.

4.5.9. 16-bit Parallel RGB Interface

The 16-bit RGB interface is selected by setting the DPI [2:0] bits to “101”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data is transferred to the internal GRAM in synchronization with the display operation via 16-bit RGB data bus (D[17:13] & D[11:0]) according to the data enable signal (DE). The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D[17:13] & D[11:0] according to the VFP/VBP and HFP/HBP settings. The unused D12 and D0 pins must be connected to GND for ensure normally operation. Registers can be set by the SPI system interface.

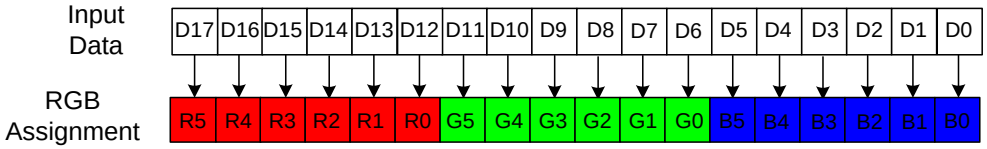
Figure62.



4.5.10. 18-bit Parallel RGB Interface

The 18-bit RGB interface is selected by setting the DPI [2:0] bits to “110”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 18-bit RGB data bus (D [17:0]) according to the data enable signal (DE) when RCM [1:0] are set to “10”. The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D[17:0] according to the VFP/VBP and HFP/HBP settings. Registers can be set by the SPI system interface.

Figure63.



5. Function Description

5.1. Display data GRAM mapping

The display data RAM stores display dots and consists of 1,382,400 bits (240x18x320 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

Every pixel (18-bit) data in GRAM is located by a (Page, Column) address (Y, X). By specifying the arbitrary window address **SC, EC** bits and **SP, EP** bits, it is possible to access the GRAM by setting RAMWR or RAMRD commands from start positions of the window address.

GRAM address for display panel position as shown in the following table

Table31.

(00,00)h	(00,01)h	....	(00,ED)h	(00,EE)h	(00,EF)h
(01,00)h	(01,01)h	....	(01,ED)h	(01,EE)h	(01,EF)h
(02,00)h	(02,01)h	....	(02,ED)h	(02,EE)h	(02,EF)h
(03,00)h	(03,01)h	....	(03,ED)h	(03,EE)h	(03,EF)h
. . .	. . .	. . .	. . .	. . .	. . .
(13D,00)h	(13D,01)h	....	(13D,ED)h	(13D,EE)h	(13D,EF)h
(13E,00)h	(13E,01)h	....	(13E,ED)h	(13E,EE)h	(13E,EF)h
(13F,00)h	(13F,01)h	....	(13F,ED)h	(13F,EE)h	(13F,EF)h

5.2. Address Counter (AC) of GRAM

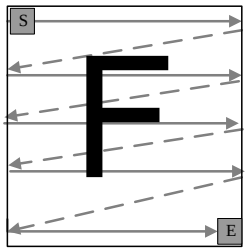
The GC9306 contains an address counter (AC) which assigns address for writing/reading pixel data to/from GRAM. The address pointers set the position of GRAM. Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (**MV, MX** and **MY** bits) setting.

To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data being written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the (start: **SC**, end: **EC**) and the (start: **SP**, end: **EP**). Therefore, the data can be written consecutively without thinking a data wrap

by those bit function.

Image data sending order from host and data stream update as shown in the following figure.

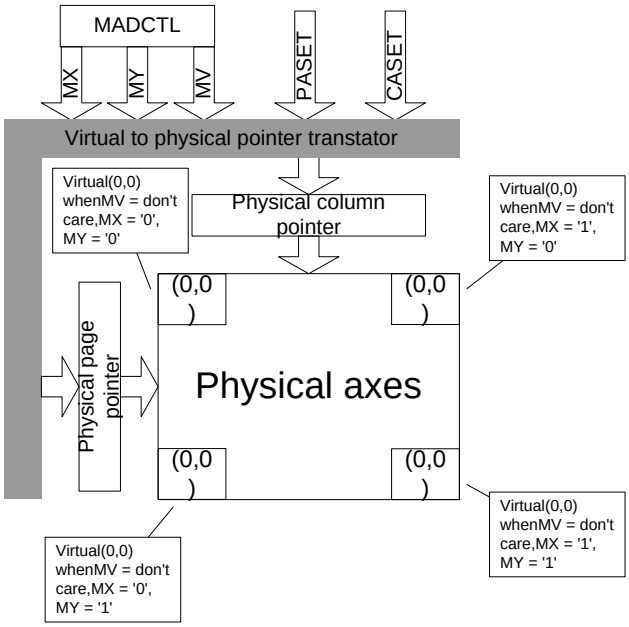
Figure64.



The data is written in the order illustrated above. The counter which dictates where in the physical memory the data is to be written is controlled by **MV, MX** and **MY** bits setting

Image data writing control:

Figure65.



CASET and PASET control for physical column/page pointers:

Table32.

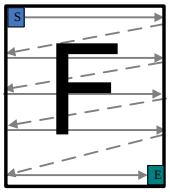
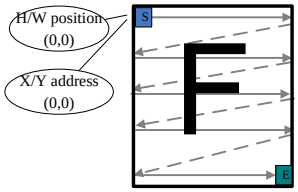
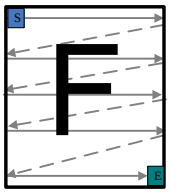
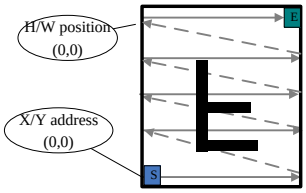
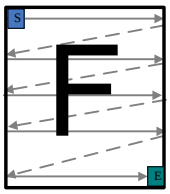
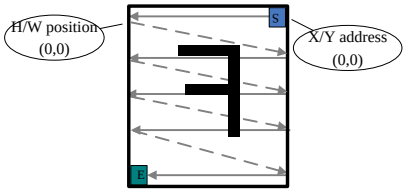
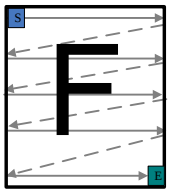
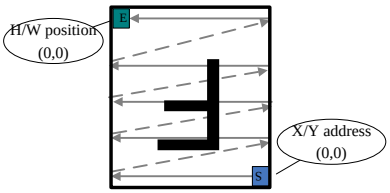
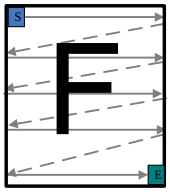
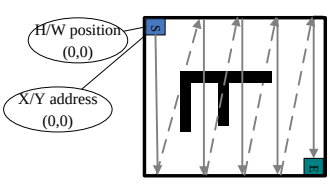
MV	MX	MY	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (319 - Physical Page Pointer)
0	1	0	Direct to (239 - Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (239 - Physical Column Pointer)	Direct to (319 - Physical Page Pointer)
0	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
0	0	1	Direct to (319 - Physical Page Pointer)	Direct to Physical Column Pointer

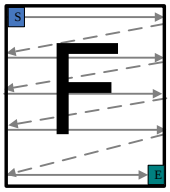
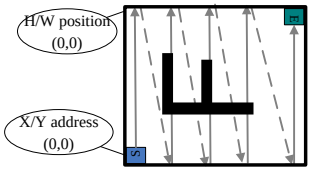
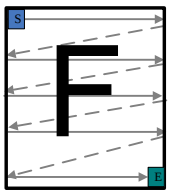
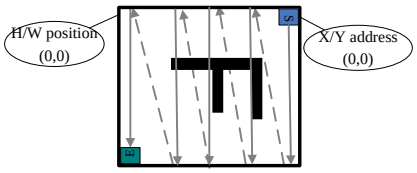
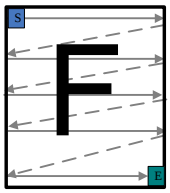
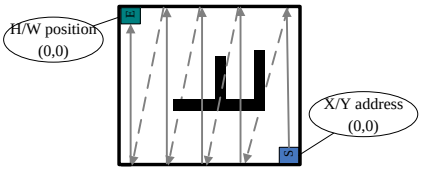
0	1	0	Direct to Physical Page Pointer	Direct to (239 - Physical Column Pointer)
0	1	1	Direct to (319 - Physical Page Pointer)	Direct to (239 - Physical Column Pointer)

condition	Column Counter	Page Counter
When RAMWR/RAMRD command is accepted	Return to "Start Column"	Return to "Start Page"
Complete Pixel Pair Write/Read action	Increment by 1	No change
The Column counter value is larger than "End column."	Return to "Start Column"	Increment by 1
The Page counter value is larger than "End page".	Return to "Start column"	Return to "Start Page"

The following figure depicts the GRAM address update method with MV, MX and MY bit setting.

Table33.

Display data direction	MV	MX	MY	Image in the Host	Image in the Driver (GRAM)
normal	0	0	0		
Y-invert	0	0	1		
X-invert	0	1	0		
Y-invert X-invert	0	1	1		
X-Y exchange	1	0	0		

X-Y exchange Y-invert	1	0	1		
X-Y exchange X-invert	1	1	0		
X-Y exchange Y-invert X-invert	1	1	1		

5.3. GRAM to display address mapping

By setting the **SS**, the relation between the source output channel and the GRAM address can be changed as reverse display. By setting the **GS** , the relation between the gate output channel and the GRAM address can be changed as reverse display. By setting the **BGR**, the relation between the source output channel and the <R>, <G>, <B> dot allocation can be reversed for different LCD color filter arrangement. The following Tables show relations among the GRAM data allocation, the source output channel, and the R, G, B dot allocation.

GRAM X address and display panel position:

Table34.

BGR="0"														
Source	**SS="0"**	S1	S2	S3	S4	S5	S6	------	S715	S716	S717	S718	S719	S720
Output	**SS="1"**	S718	S719	S720	S715	S716	S717	------	S4	S5	S6	S1	S2	S3
GRAM X address		"00"h			"01"h			------	"EE"h			"EF"h		
RGB data		R	G	B	R	G	B	------	R	G	B	R	G	B
Pixel		Pixel1			Pixel2			------	Pixel239			Pixel240		
BGR="1"														
Source	**SS="0"**	S3	S2	S1	S6	S5	S4	------	S717	S716	S715	S720	S719	S718
Output	**SS="1"**	S720	S719	S718	S717	S716	S715	------	S6	S5	S4	S3	S2	S1
GRAM X address		"00"h			"01"h			------	"EE"h			"EF"h		
RGB data		R	G	B	R	G	B	------	R	G	B	R	G	B
Pixel		Pixel1			Pixel2			------	Pixel239			Pixel240		

GRAM address and display panel position (GS_Panel =’0’):

Table35.

S/G pins	S1	S2	S3	S4	S5	S6	S7	S8	S9	----	S712	S713	S714	S715	S716	S717	S718	S719	S720
G1	0000h			0001h			0002h			----	00EDh			00EEh			00EFh		
G2	0100h			0101h			0102h			----	01EDh			01EEh			01EFh		
G3	0200h			0201h			0202h			----	02EDh			02EEh			02EFh		
G4	0300h			0301h			0302h			----	03EDh			03EEh			03EFh		
G5	0400h			0401h			0402h			----	04EDh			04EEh			04EFh		
G6	0500h			0501h			0502h			----	05EDh			05EEh			05EFh		
⋮	⋮			⋮			⋮			⋮	⋮			⋮			⋮		
G315	13A00h			13A01h			13A02h			----	13AEDh			13AEEh			13AEFh		
G316	13B00h			13B01h			13B02h			----	13BEDh			13BEEh			13BEFh		
G317	13C00h			13C01h			13C02h			----	13CEDh			13CEEh			13CEFh		
G318	13D00h			13D01h			13D02h			----	13DEDh			13DEEh			13DEFh		
G319	13E00h			13E01h			13E02h			----	13EEDh			13EEEh			13EEFh		
G320	13F00h			13F01h			13F02h			----	13FEDh			13FEEh			13FEFh		

GRAM address and display panel position (GS_Panel =’1’):

Table36.

S/G pins	S1	S2	S3	S4	S5	S6	S7	S8	S9	----	S712	S713	S714	S715	S716	S717	S718	S719	S720
G320	0000h			0001h			0002h			----	00EDh			00EEh			00EFh		
G319	0100h			0101h			0102h			----	01EDh			01EEh			01EFh		
G318	0200h			0201h			0202h			----	02EDh			02EEh			02EFh		
G317	0300h			0301h			0302h			----	03EDh			03EEh			03EFh		
G316	0400h			0401h			0402h			----	04EDh			04EEh			04EFh		
G315	0500h			0501h			0502h			----	05EDh			05EEh			05EFh		
⋮	⋮			⋮			⋮			⋮	⋮			⋮			⋮		
G6	13A00h			13A01h			13A02h			----	13AEDh			13AEEh			13AEFh		
G5	13B00h			13B01h			13B02h			----	13BEDh			13BEEh			13BEFh		
G4	13C00h			13C01h			13C02h			----	13CEDh			13CEEh			13CEFh		
G3	13D00h			13D01h			13D02h			----	13DEDh			13DEEh			13DEFh		
G2	13E00h			13E01h			13E02h			----	13EEDh			13EEEh			13EEFh		
G1	13F00h			13F01h			13F02h			----	13FEDh			13FEEh			13FEFh		

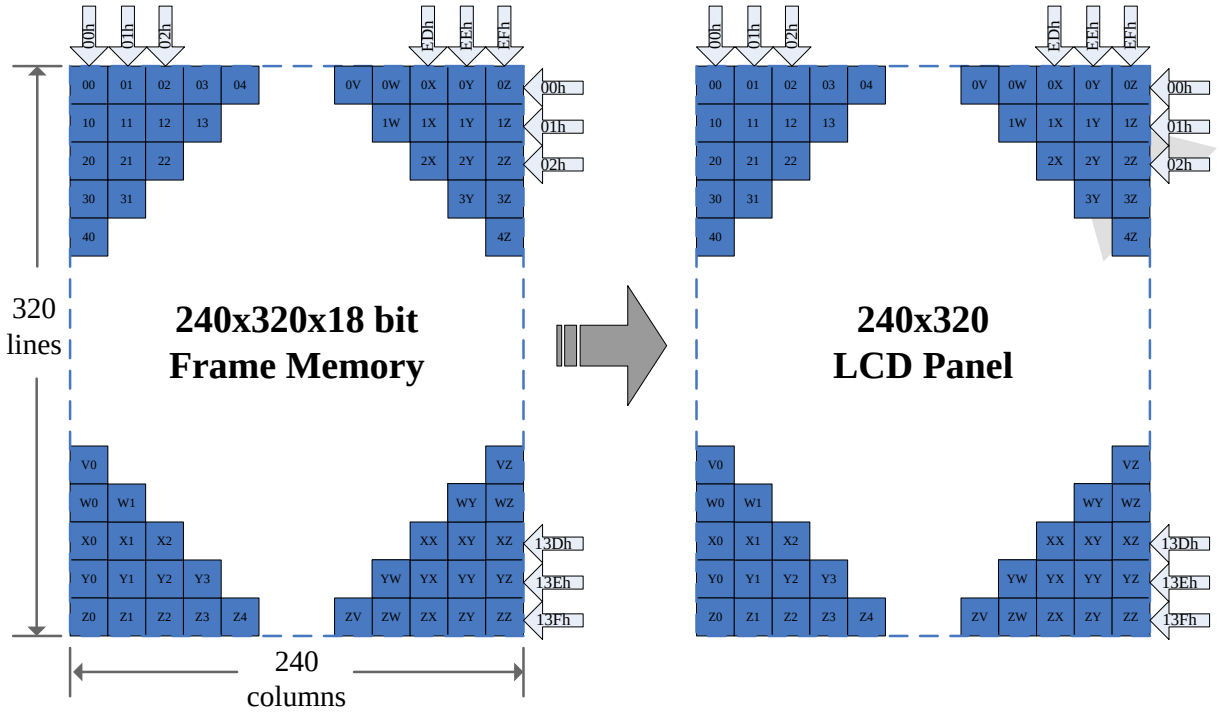
GC9306 supports three kinds of display mode: one is Normal Display Mode, the other is Partial Display Mode, and Scrolling Display Mode.

5.3.1. Normal display on or partial mode on, vertical scroll off

In this mode, content of the frame memory within an area where column pointer is 0000h to 00EFh and page pointer is 0000h to 013Fh is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0,0)

Figure66.

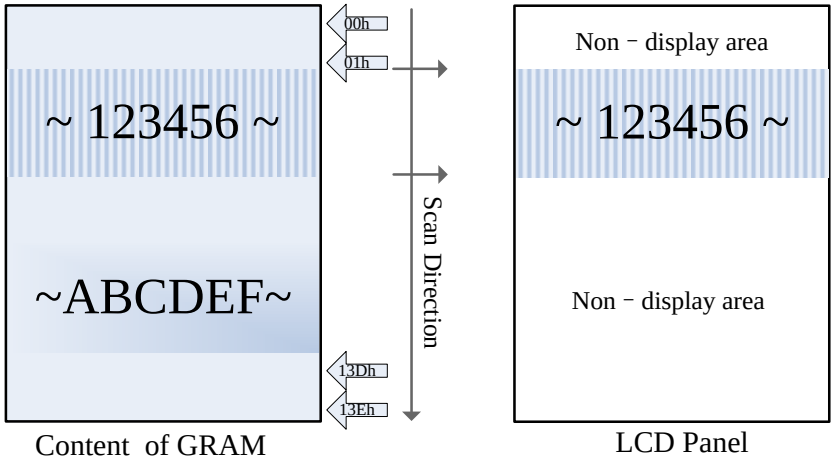


Example1:

(1) partial mode on (setting 12h)

(2) SR [15:0] =50DEC, ER [15:0] =150DEC, MADCTL's **B4(ML)='0'** (GS='0').

Figure67.

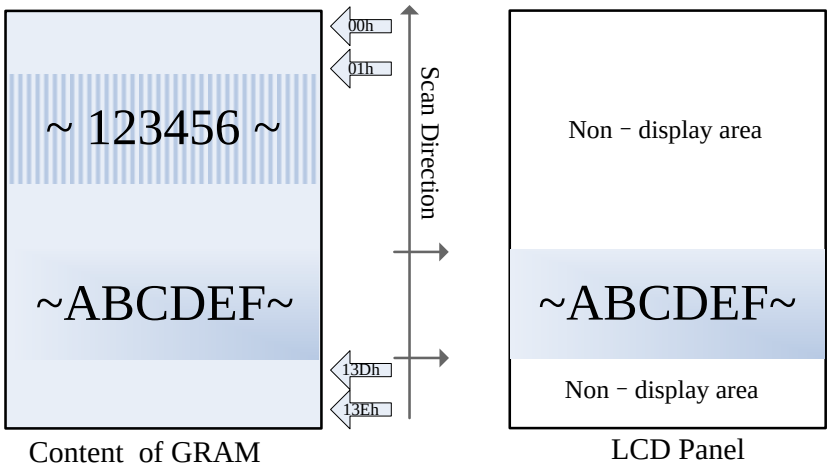


Example2:

(1) partial mode on (setting 12h)

(2) SR [15:0] =50DEC, ER [15:0] =150DEC, MADCTL's **B4(ML)='1'** (GS='0').

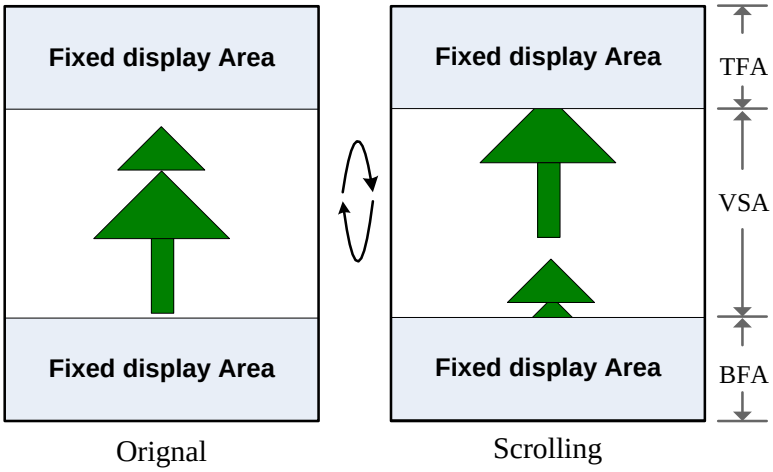
Figure68.



5.3.2. Vertical scroll display mode

When setting R37h, the scrolling display mode is active, and the vertical scrolling display is specified by **TFA, VSA ,BFA** bits (R33h) and **VSP** bits (R37h).

Figure69.

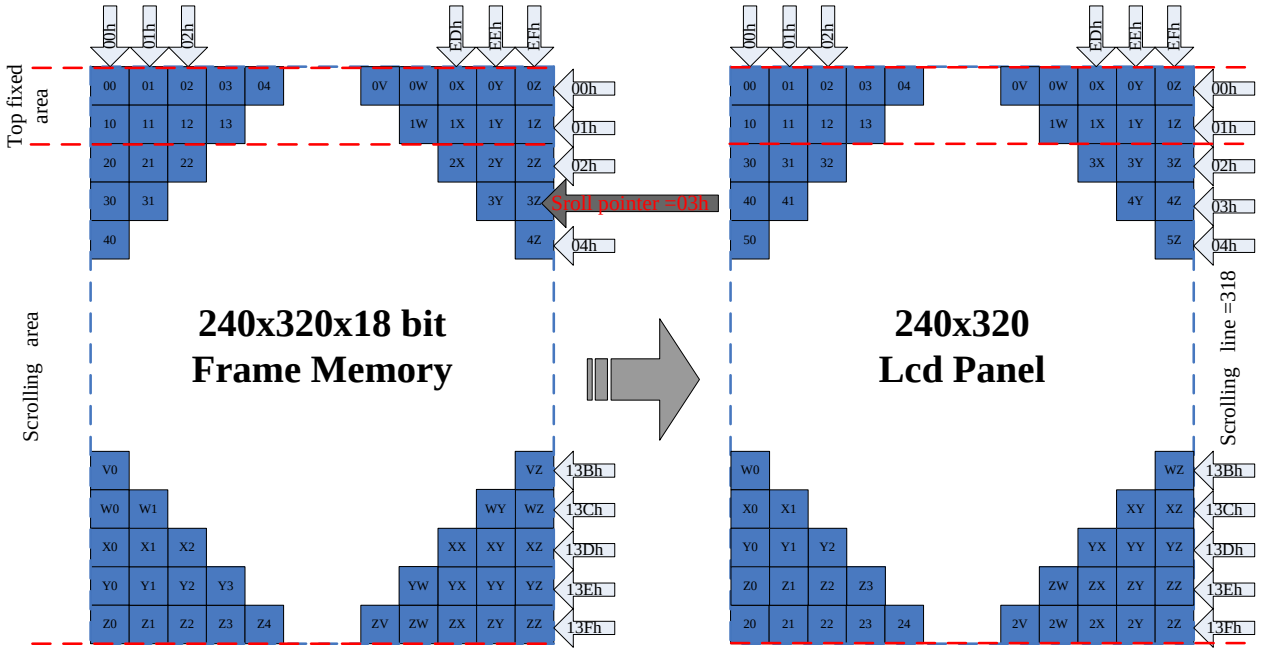


When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) =320. In this case, scrolling is applied as shown below.

Example 1 .TFA='2d', VSA='318d', BFA='0d', VSP='3d' (SS='0', GS='0')

Memory map of vertical scrolling 1:

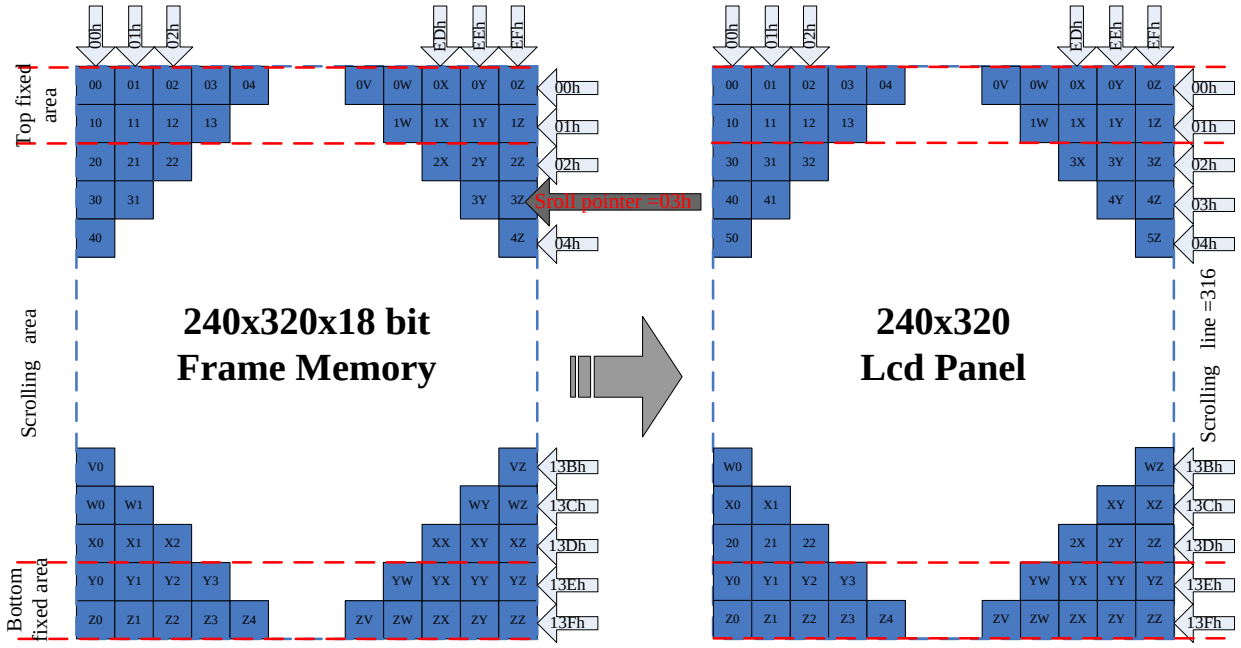
Figure70.



Example 2 .TFA='2d', VSA='316d', BFA='2d', VSP='3d' (SS='0', GS='0')

Memory map of vertical scrolling 2:

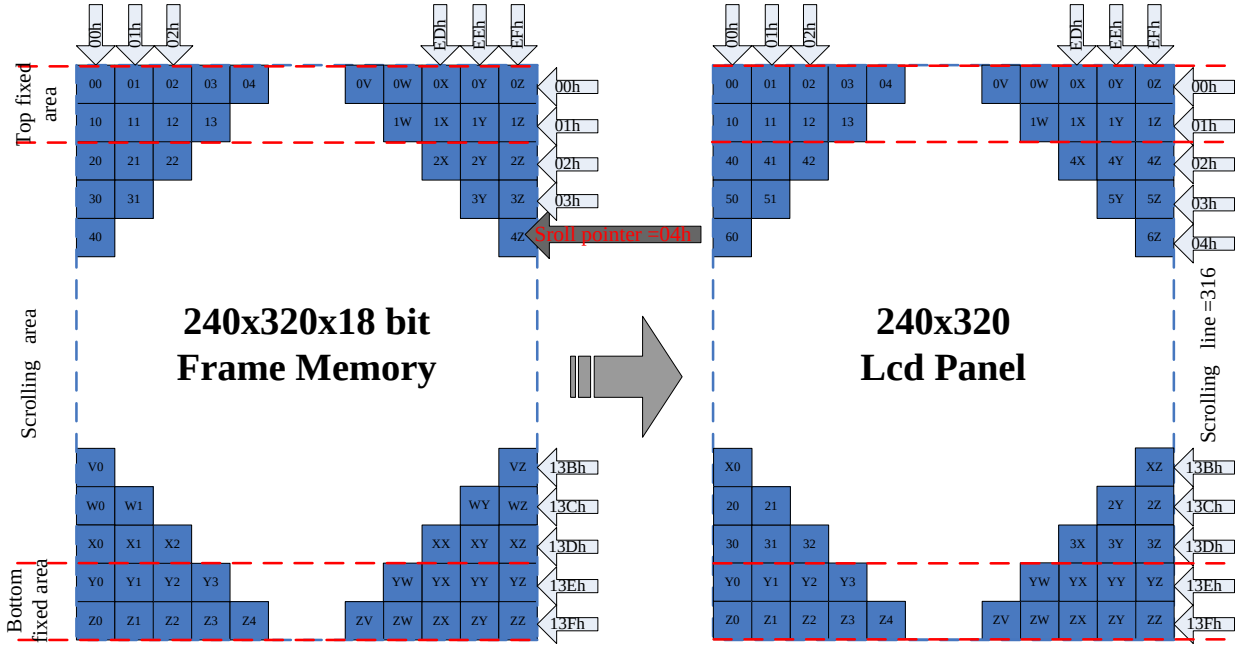
Figure71.



Example 3 .TFA='2d', VSA='316d', BFA='2d', VSP='4d' (SS='0', GS='0')

Memory map of vertical scrolling 3:

Figure72.



Vertical scroll example

There are 2 types of vertical scrolling, which are determined by the **TFA, VSA, BFA** bits and **VSP** bits

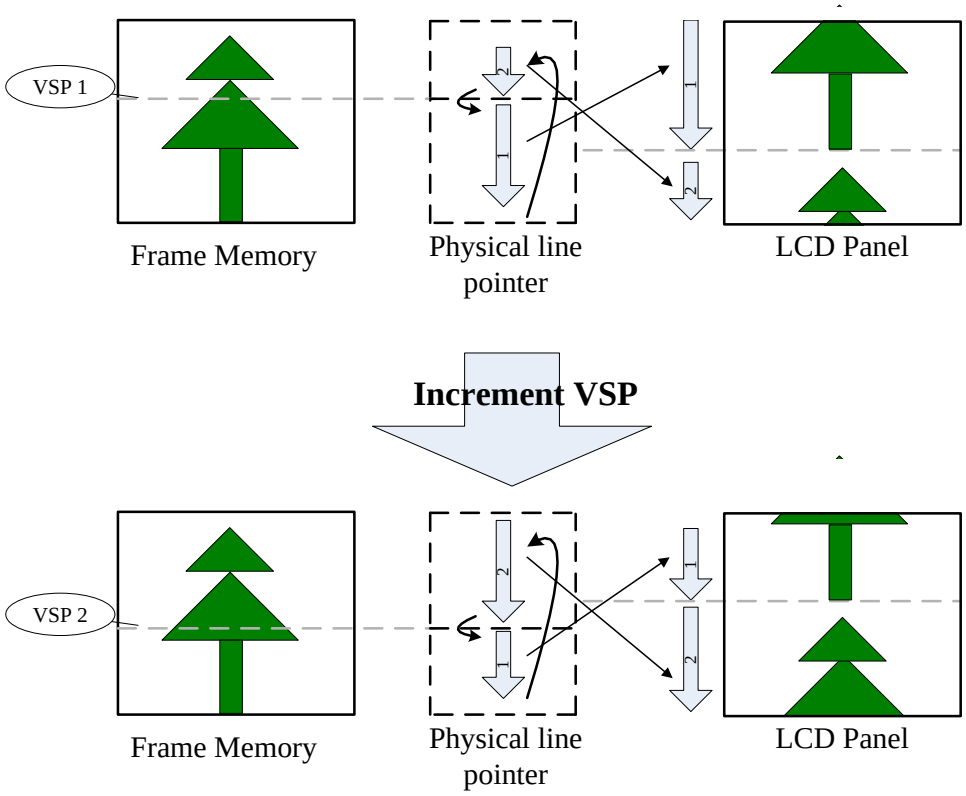
Case 1: TFA + VSA + BFA ≠ '320d'

N/A. Do not set TFA + VSA + BFA ≠ '320d'. In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA = '320d' (Scrolling)

Example (1) When TFA='0d', VSA='320d', BFA='0d' and VSP1='40d' & VSP2='140d' (SS ='0',GS='0')

Figure73.

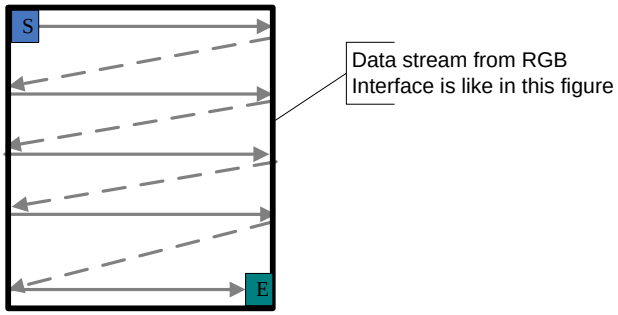


5.3.3. Updating order on display active area in RGB interface mode

There is defined different kind of updating orders for display in RGB interface mode (**RCM [1:0]** =’1x’).

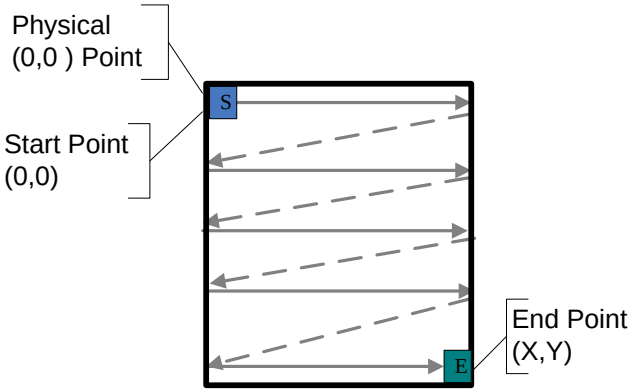
These updating are controlled by **MY** and **MX** bits. Data streaming direction from the host to the display is described in the following figure.

Figure74.



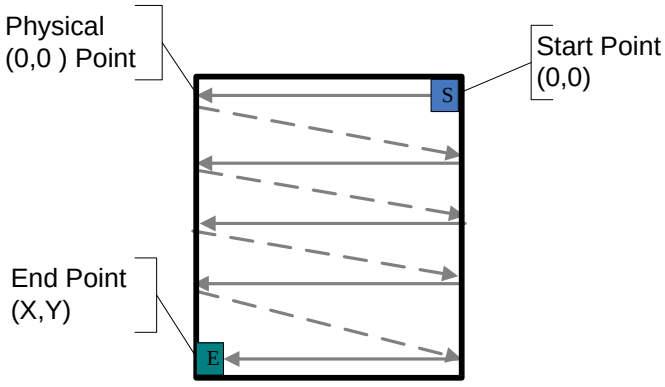
Updating order when MY = ‘0’ and MX = ‘0’

Figure75.



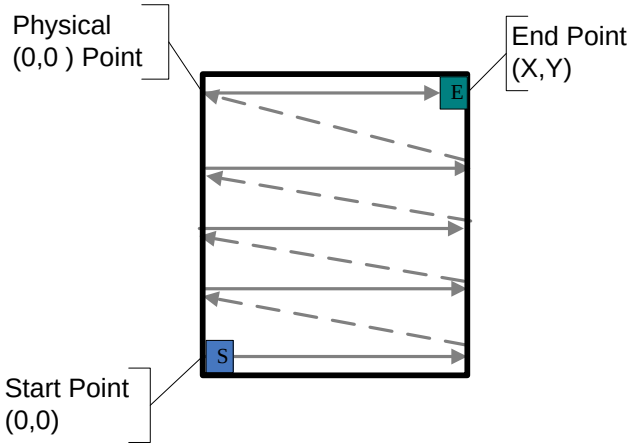
Updating order when MY = ‘0’ and MX = ‘1’

Figure76.



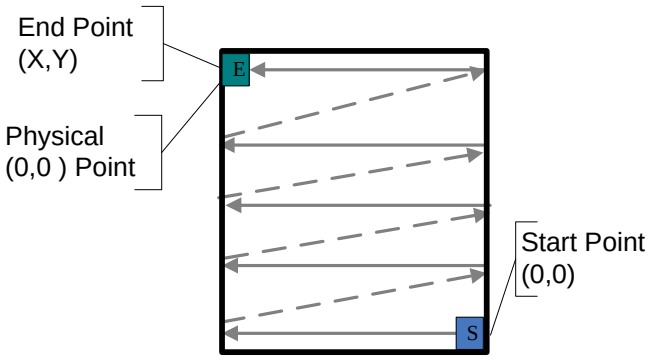
Updating order when MY = ‘1’ and MX = ‘0’

Figure77.



Updating order when MY = '1' and MX = '1'

Figure78.



Rules for updating order on display active area in RGB interface display mode:

Table37.

Condition	Horizontal Counter	Vertical Counter
An active VS signal is received	Return to 0	Return to 0
Single Pixel information of the active area is received	Increment by 1	No change
An active HS signal between two active area lines	Return to 0	Increment by 1
The Horizontal counter value is larger than X and the Vertical counter value is larger than Y	Return to 0 "Start Column"	Return to "Start Page"

Note: Pixel order is RGB on the display.

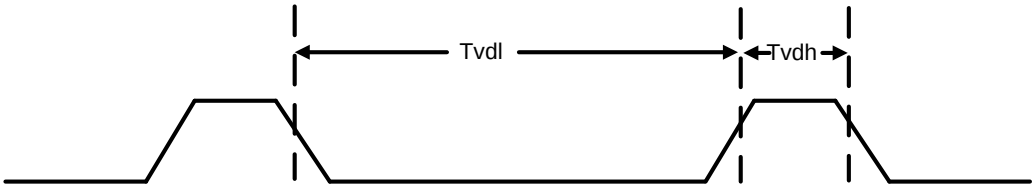
5.4. Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

5.4.1. Tearing effect line modes

Mode 1, The Tearing Effect Output signal consists of V-Blanking Information only:

Figure79.

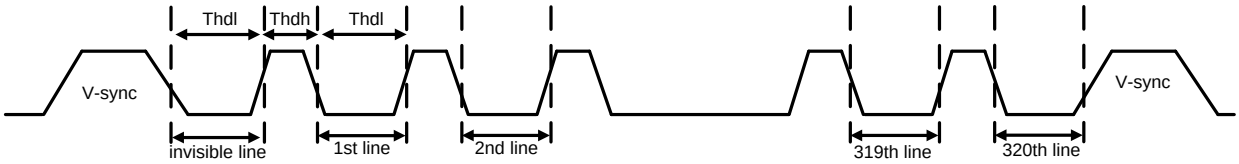


tVdh= The LCD display is not updated from the Frame Memory

tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Mode 2, The Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 320 H-sync pulses per field.

Figure80.



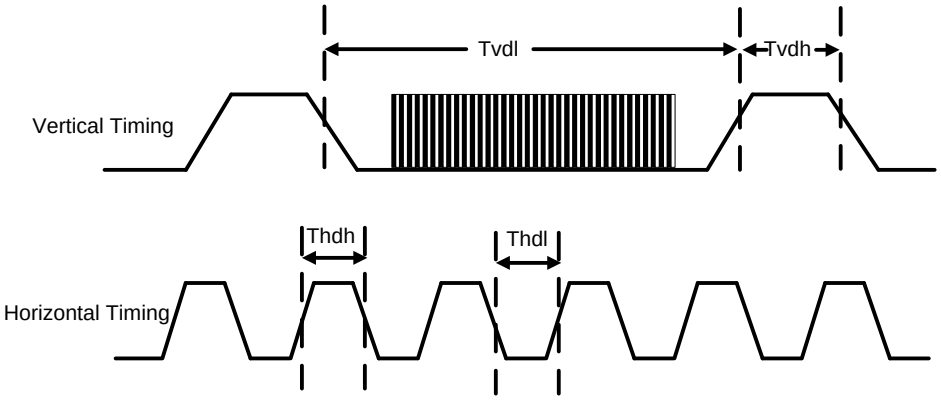
thdh= The LCD display is not updated from the Frame Memory

thdl= The LCD display is updated from the Frame Memory (except Invisible Line – see above)

5.4.2. Tearing effect line timing

The Tearing Effect signal is described below.

Figure81.



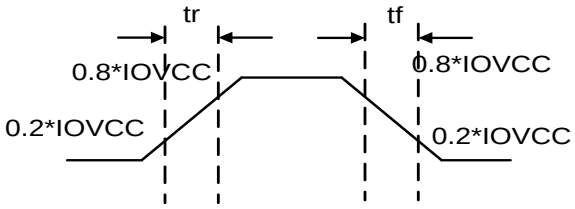
Idle Mode Off (Frame Rate = 60 Hz)

Table38.

Symbol	Parameter	Spec.			Description
		Min.	Max.	Unit	
tvdl	Vertical Timing Low Duration	TBD	-	ms	-
tvdh	Vertical Timing High Duration	1000	-	us	-
thdl	Horizontal Timing Low Duration	TBD	-	us	-
thdh	Horizontal Timing High Duration	TBD	500	us	-

Note: Idle Mode Off (Frame Rate = 60 Hz) ,The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.

Figure82.



The Tearing Effect Output Line is fed back to the MCU and should be used to avoid Tearing Effect.

5.5. Source driver

The GC9306 contains a 720 channels of source driver (S1~S720) which is used for driving the source line of TFT LCD panel. The source driver converts the digital data from GRAM into the analog voltage for 720 channels and generates corresponding
gray scale voltage output, which can realize a 262K colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

5.6. Gate driver

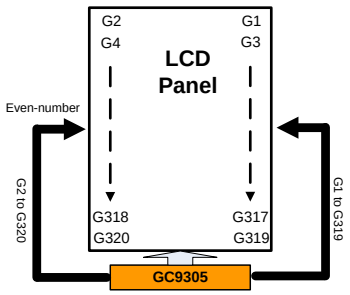
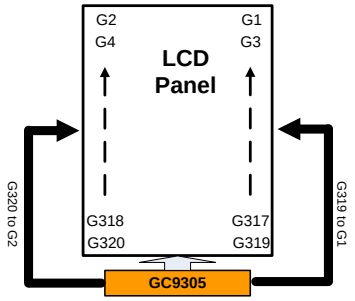
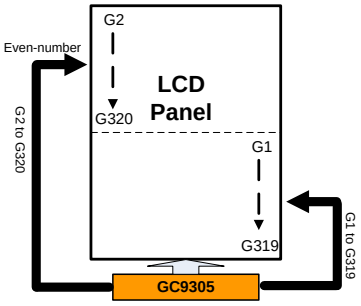
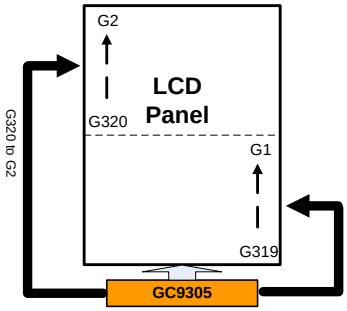
The GC9306 contains a 320 gate channels of gate driver (G1~G320) which is usedfor driving the gate. The gate driver level is VGH when scan some line, VGL the other lines.

5.7. Scan mode setting

GS: Sets the direction of scan by the gate driver, The scan direction determined by GS = 0 can be reversed by setting GS = 1.

SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.

Table39.

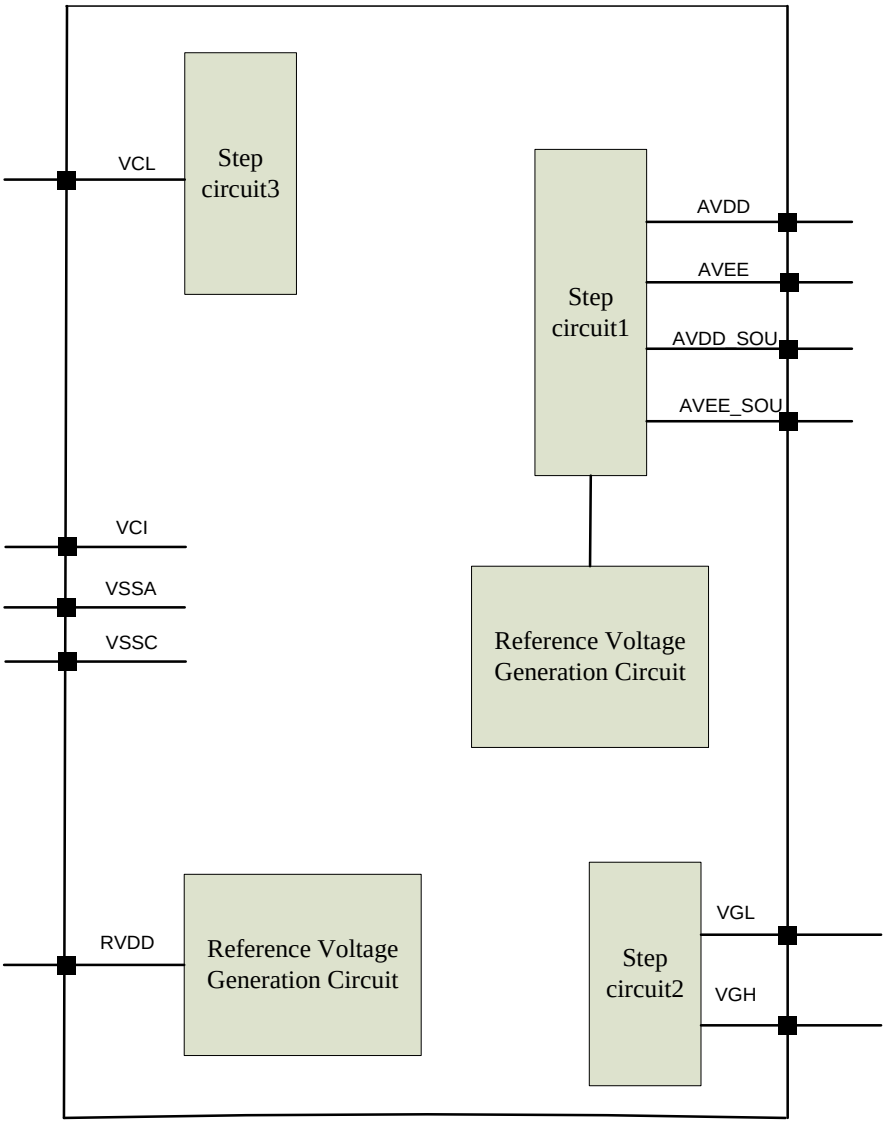
SM	GS	Scan Direction	Gate Output Sequence
0	0		G1 G2 G3 G4 ---> G317 G318 G319 G320
0	1		G320 G319 G 318 G317 ---> G4 G3 G2 G1
1	0		G1 G3 ---> G317 G319 --> G2 G4 ---> G318 G320
1	1		G320 G318 ---> G4 G2 --> G319 G317 ---> G3 G1

5.8. LCD power generation circuit

5.8.1. Power supply circuit

The power circuit of GC9306 is used to generate supply voltages for LCD panel driving.

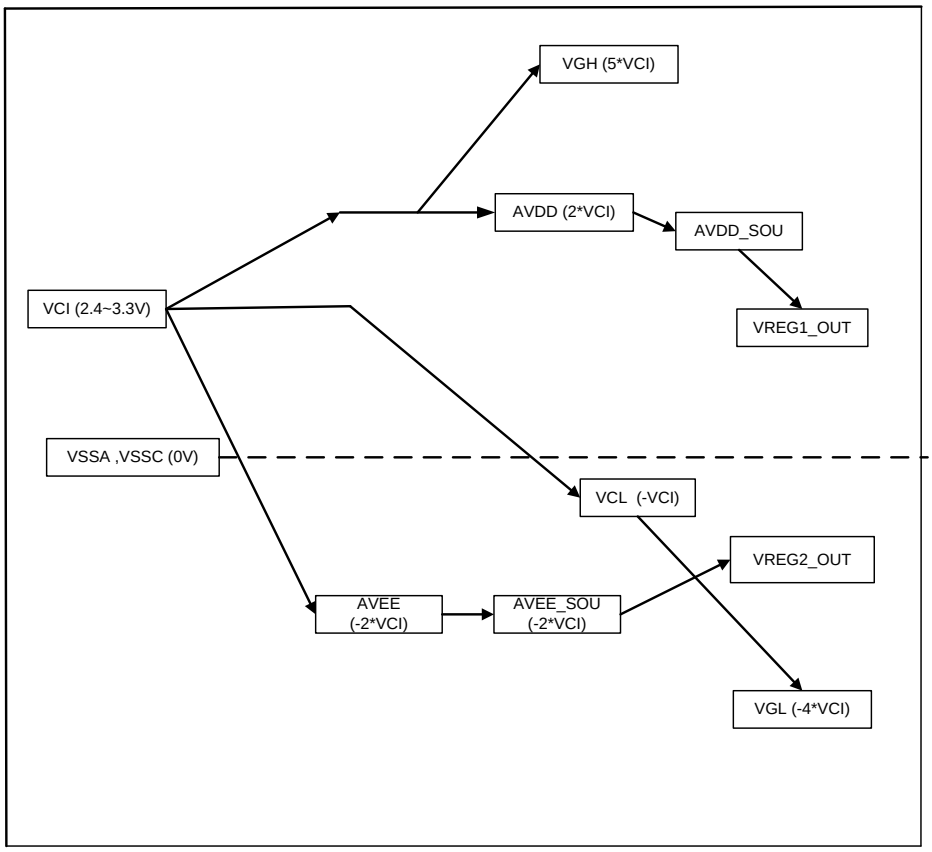
Figure83.



5.8.2. LCD power generation scheme

The boost voltage generated is shown as below.

Figure84.



LCD power generation scheme

5.9. Gamma Correction

GC9306 incorporates the γ-correction function to display 262,144 colors for the LCD panel. The γ-correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers for positive and negative polarities, to make GC9306 available with liquid crystal panels of various characteristics.

Figure85.

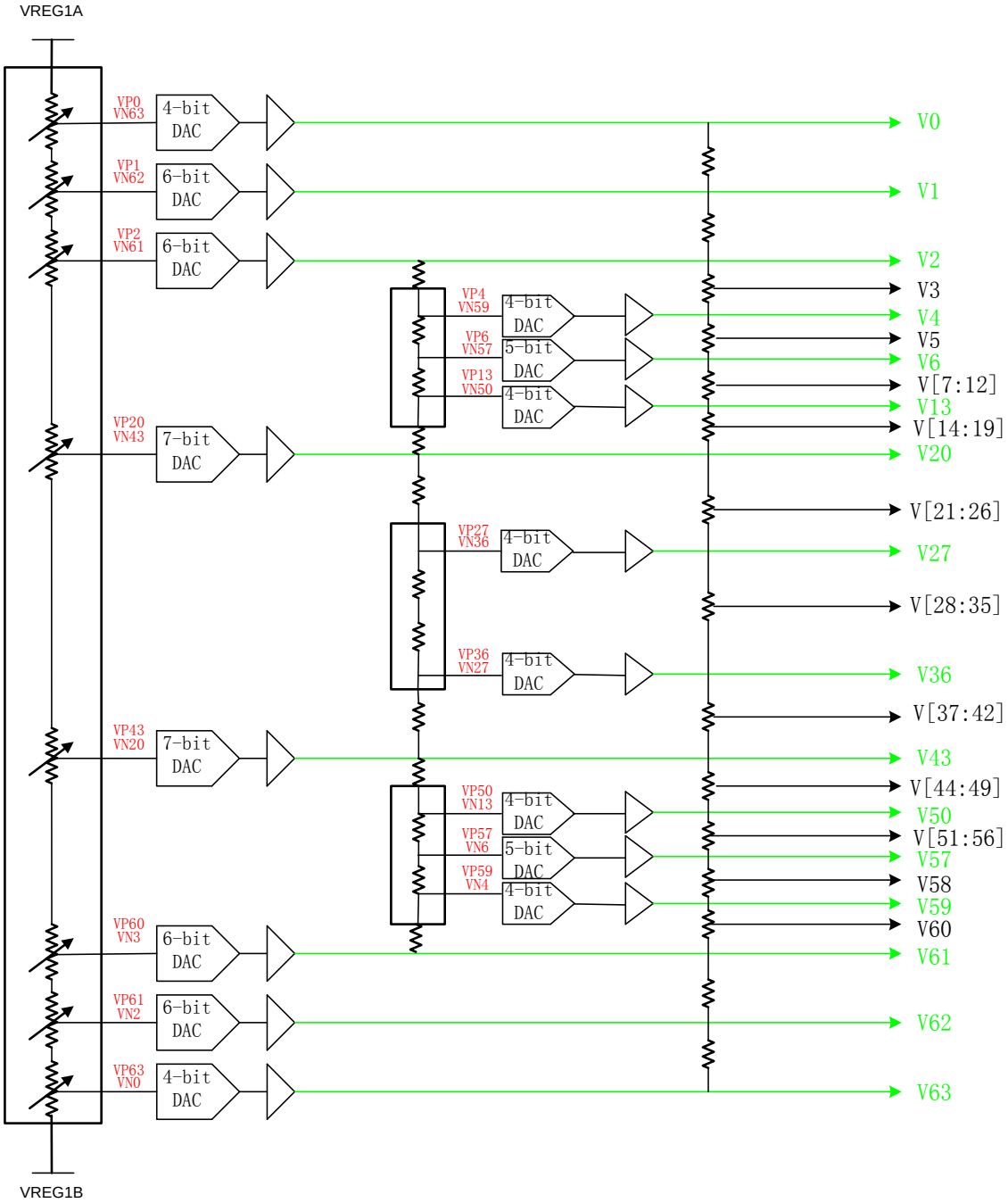
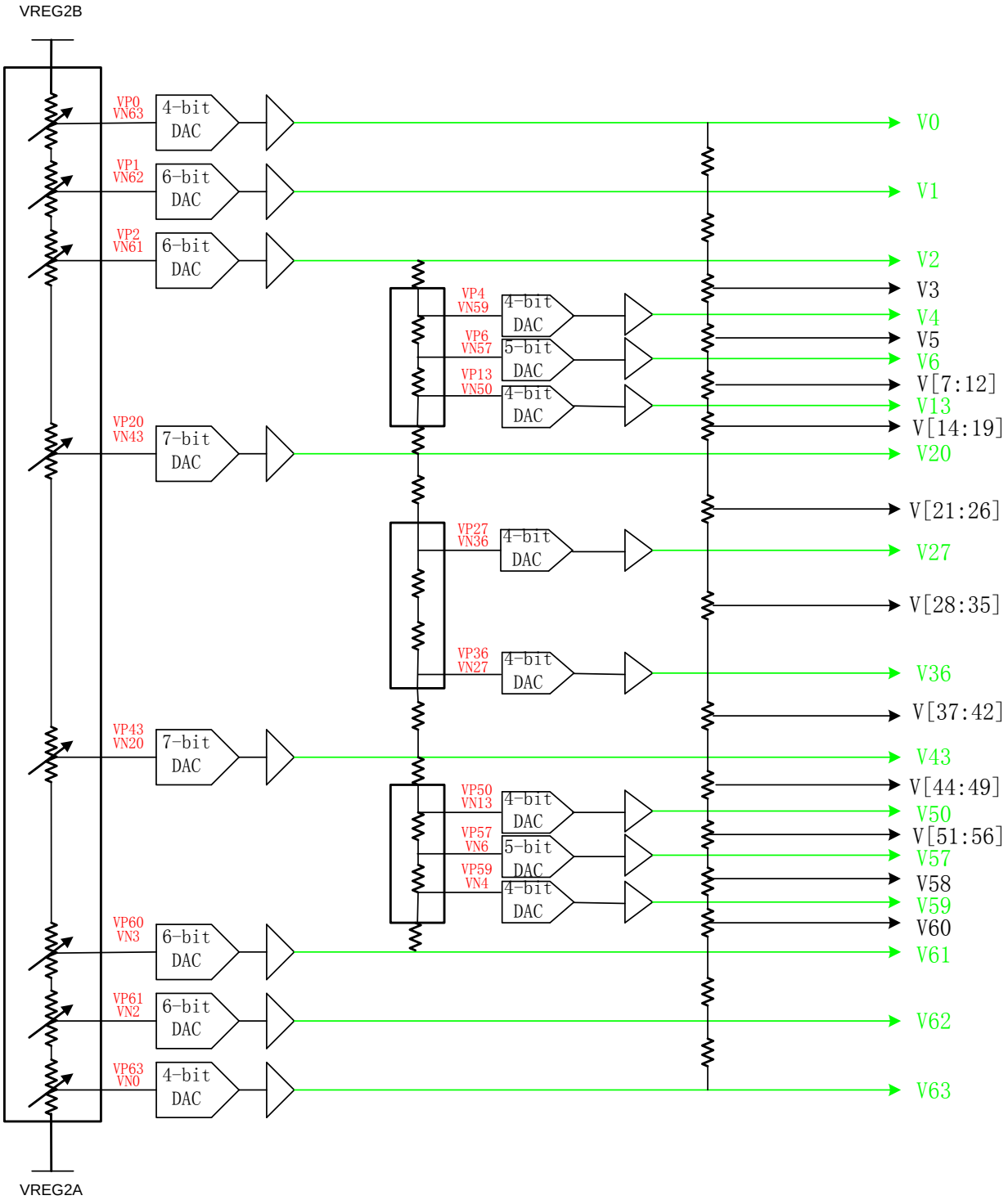
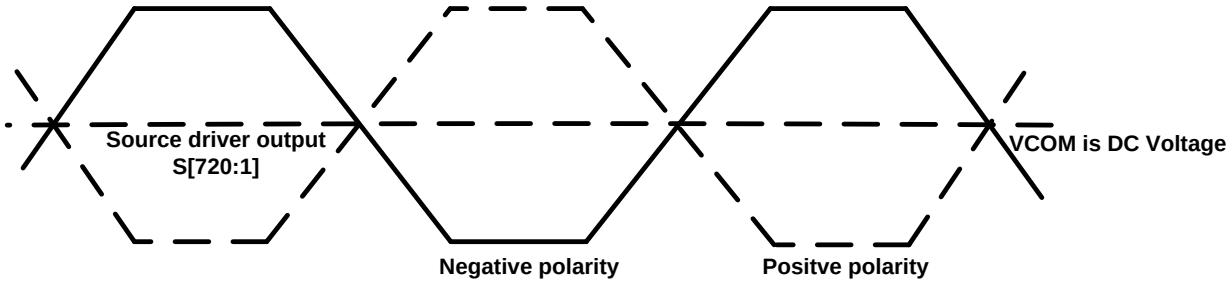


Figure86.



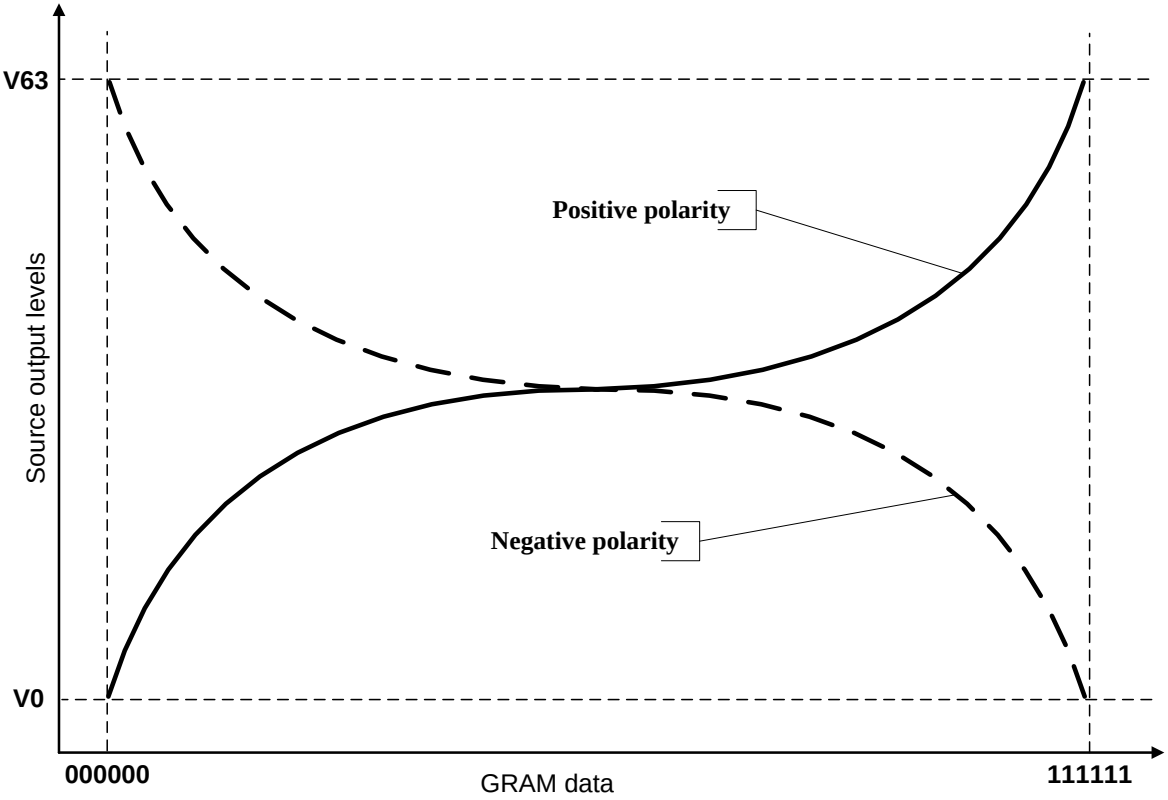
Grayscale Voltage Generation

Figure87.Dot inversion



Relationship between Source Output and VCOM

Figure88.



5.10. Power Level Definition

5.10.1. Power Levels

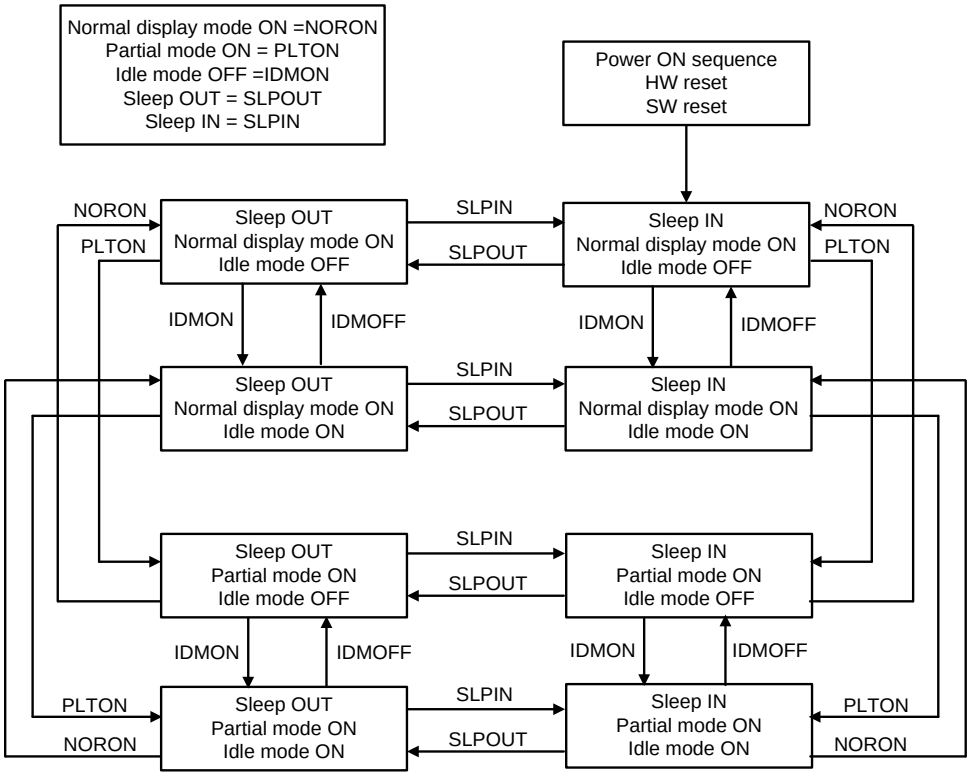
6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
   In this mode, the display is able to show maximum 262,144 colors.
2. Partial Mode On, Idle Mode Off, Sleep Out.
   In this mode part of the display is used with maximum 262,144 colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
   In this mode, the full display area is used but with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out.
   In this mode, part of the display is used but with 8 colors.
5. Sleep In Mode.
   In this mode, the DC : DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with IOVCC power supply. Contents of the memory are safe.
6. Power Off Mode.
   In this mode, both VCI and IOVCC are removed.

Note1: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

5.10.2. Power Flow Chart

Figure89.



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.

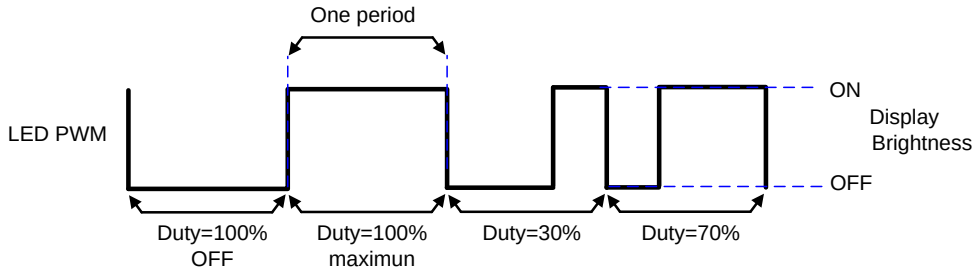
5.10.3.Brightness control block

There is an external output signal from brightness block, LEDPWM to control the LED driver IC in order to control display brightness.

There are resister bits, DBV[7:0] of R51h, for display brightness of manual brightness setting. The LEDPWM duty is calculated as DBV[7:0]/255 x period (affected by OSC frequency).

For example: LEDPWM period = 3ms, and DBV[7:0] = '200DEC'. Then LEDPWM duty = 200 / 255=78.1%. Correspond to the LEDPWM period = 3 ms, the high-level of LEDPWM (high effective) = 2.344ms, and the low-level of LEDPWM = 0.656ms.

Figure90.



LEDPWM output duty

5.11. Input/output pin state

5.11.1. Output pins

Table40.

Output or Bi-directional pins	After Power On	After Hardware Reset
DB17 to DB0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)
SDA	High-Z (Inactive)	High-Z (Inactive)
SDO	High-Z (Inactive)	High-Z (Inactive)
TE	Low	Low
LEDPWM	Low	Low

Characteristics of output pins

5.11.2. Input pins

Table41.

Input pins	During Power On Process	After Power On	After Hardware Reset	During Power Off Process
RESX	Input valid	Input valid	Input valid	Input valid
CSX	Input invalid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input invalid
SDA	Input invalid	Input valid	Input valid	Input invalid
VSYNC	Input invalid	Input valid	Input valid	Input invalid
HSYNC	Input invalid	Input valid	Input valid	Input invalid
DE	Input invalid	Input valid	Input valid	Input invalid
DOTCLK	Input invalid	Input valid	Input valid	Input invalid
D[17:0]	Input invalid	Input valid	Input valid	Input invalid
IM[3:0]	Input invalid	Input valid	Input valid	Input invalid

Characteristics of input pins

6. Command

6.1. Command List

Regulative Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Read Display Identification Information 2	0	1	↑	XX	0	0	0	0	0	1	0	0	04h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	ID2_1[7:0]								00
	1	↑	1	XX	ID2_2[7:0]								93
	1	↑	1	XX	ID2_3[7:0]								06
Read Display Status	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	D[31:25]							X	00
	1	↑	1	XX	X	D[22:20]			D[19:16]				61
	1	↑	1	XX	X	X	X	X	X	D[10:8]			00
	1	↑	1	XX	D[7:5]			X	X	X	X	X	00
Enter Sleep Mode	0	1	↑	XX	0	0	0	1	0	0	0	0	10h
Sleep OUT	0	1	↑	XX	0	0	0	1	0	0	0	1	11h
Partial Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	0	12h
Normal Display Mode ON	0	1	↑	XX	0	0	0	1	0	0	1	1	13h
Display Inversion OFF	0	1	↑	XX	0	0	1	0	0	0	0	0	20h
Display Inversion ON	0	1	↑	XX	0	0	1	0	0	0	0	1	21h
Display OFF	0	1	↑	XX	0	0	1	0	1	0	0	0	28h
Display ON	0	1	↑	XX	0	0	1	0	1	0	0	1	29h
Column Address Set	0	1	↑	XX	0	0	1	0	1	0	1	0	2Ah
	1	1	↑	XX	SC[15:8]								00
	1	1	↑	XX	SC[7:0]								00
	1	1	↑	XX	EC[15:8]								00
	1	1	↑	XX	EC[7:0]								EFh
Page Address Set	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh
	1	1	↑	XX	SP[15:8]								00
	1	1	↑	XX	SP[7:0]								00

	1	1	↑	XX	EP[15:8]								01h
	1	1	↑	XX	EP[7:0]								3Fh
Memory Write	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch
	1	1	↑	D[17:0]									XX
Partial Area	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
	1	1	↑	XX	SR[15:8]								00
	1	1	↑	XX	SR[7:0]								00
	1	1	↑	XX	ER[15:8]								01
	1	1	↑	XX	ER[7:0]								3F
Vertical Scrolling Definition	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
	1	1	↑	XX	TFA[15:8]								00
	1	1	↑	XX	TFA[7:0]								00
	1	1	↑	XX	VSA[15:8]								01
	1	1	↑	XX	VSA[7:0]								40
Tearing Effect Line OFF	0	1	↑	XX	0	0	1	1	0	1	0	0	34h
Tearing Effect Line ON	0	1	↑	XX	0	0	1	1	0	1	0	1	35h
	1	1	↑	XX	X	X	X	X	X	X	X	M	00
Memory Access Control	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	X	X	00
Vertical Scrolling Start Address	0	1	↑	XX	0	0	1	1	0	1	1	1	37h
	1	1	↑	XX	VSP[15:8]								00
	1	1	↑	XX	VSP[7:0]								00
Idle Mode OFF	0	1	↑	XX	0	0	1	1	1	0	0	0	38h
Idle Mode ON	0	1	↑	XX	0	0	1	1	1	0	0	1	39h
Pixel Format Set	0	1	↑	XX	0	0	1	1	1	0	1	0	3Ah
	1	1	↑	XX	X	DPI[2:0]			X	DBI[2:0]			66
Write Memory Continue	0	1	↑	XX	0	0	1	1	1	1	0	0	3Ch
	1	1	↑	D[17:0]									XX
Set Tear Scanline	0	1	↑	XX	0	1	0	0	0	1	0	0	44h
	1	1	↑	XX	X	X	X	X	X	X	X	STS[8]	00
	1	1	↑	XX	STS[7:0]								00
Get Scanline	0	1	↑	XX	0	1	0	0	0	1	0	1	45h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	X	X	X	X		GTS [8]	00
	1	↑	1	XX	GTS[7:0]								00
Write Display Brightness	0	1	↑	XX	0	1	0	1	0	0	0	1	51h
	1	↑	1	XX	DBV[7:0]								00
Write CTRL Display	0	1	↑	XX	0	1	0	1	0	0	1	1	53h
	1	1	↑	XX	X	X	BCTRL	X	DD	BL	X	X	00

Read ID1	0	1	↑	XX	1	1	0	1	1	1	0	0	DAh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver ID [7:0]								00h
Read ID2	0	1	↑	XX	1	1	0	1	1	1	0	0	DBh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver ID [7:0]								93h
Read ID3	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver ID [7:0]								06h

Extended Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RGB Interface Signal Control	0	1	↑	XX	1	0	1	1	0	0	0	0	B0h
	1	1	↑	XX	X	RCM[1:0]		X	VSPL	HSPL	DPL	EPL	01
Blanking Porch Control	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
	1	1	↑	XX	0	VFP[6:0]							08
	1	1	↑	XX	0	VBP[6:0]							02
	1	1	↑	XX	0	0	0	XX					XX
	1	1	↑	XX	0	0	0	HBP[4:0]					14
Display Function Control	0	1	1	XX	1	0	1	1	0	1	1	0	B6
	1	1	1	XX	X	X	X	X	X	X	X	X	00
	1	1	1	XX	REV	GS	SS	SM	X	X	X	X	80
	1	1	1	XX	X	X	NL[5:0]						27
Interface Control	0	1	↑	XX	1	1	1	1	0	1	1	0	F6h
	1	1	↑	XX	X	X	X	X	BGR_EOR	X	X	WEMODE	01
	1	1	↑	XX	X	X	X	X	X	X	MDT[1:0]		00
	1	1	↑	XX	X	X	X	X	DM[1:0]		RM	RIM	00

Inter Command Set													
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Power Criterion Control	0	1	↑	XX	1	0	1	0	0	0	1	1	A3h
	1	1	↑	XX	0	0	0	0	0	0	vcire	0	00
Vcore voltage Control	0	1	↑	XX	1	0	1	0	0	1	0	0	A4h
	1	1	↑	XX	0	1	0	0	vdd_ad[3:0]				44
Vreg1a voltage Control	0	1	↑	XX	1	0	1	0	0	1	1	0	A6h
	1	1	↑	XX			vreg1_vap[5:0]						2a
Vreg1b voltage Control	0	1	↑	XX	1	0	1	0	0	1	1	1	A7h
	1	1	↑	XX			vreg1_vbp[5:0]						25
Vreg2a voltage Control	0	1	↑	XX	1	0	1	0	1	0	0	0	A8h
	1	1	↑	XX			vreg2_van[5:0]						15
Vreg2b voltage Control	0	1	↑	XX	1	0	1	0	1	0	0	1	A9h
	1	1	↑	XX			vreg2_vbn[5:0]						25
Frame Rate	0	1	↑	XX	1	0	1	0	0	0	1	1	E8h
	1	1	↑	XX	0	DINV[2:0]			RTN1[4:0]				11
	1	1	↑	XX	RTN2[7:0]								40
SPI 2data	0	1	↑	XX	1	1	1	0	1	0	0	1	E9h

control	1	1	↑	XX					2data_en	2data_mdt			00
Charge Pump Frequent Control	0	1	↑	XX	1	1	1	0	1	1	0	0	ECh
	1	1	↑	XX		avdd_clk_ad[2:0]				avee_clk_ad[2:0]			33
	1	1	↑	XX		chp_sou_clk_ad[2:0]				vcl_clk_ad[2:0]			22
	1	1	↑	XX	vgh_clk_ad[3:0]				vgl_clk_ad[3:0]				88
Inner register enable 1	0	1	↑	XX	1	1	1	1	1	1	1	0	FEh
Inner register enable 2	0	1	↑	XX	1	1	1	0	1	1	1	1	EFh
SET_GAMMA1	0	1	↑	XX	1	1	1	1	0	0	0	0	F0h
	1	1	↑	XX	0	0	0	0	0	0	dig2gam_dig2j0_n[1:0]		02
	1	1	↑	XX	0	0	0	0	0	0	dig2gam_dig2j1_n[1:0]		00
	1	1	↑	XX	0	0	0	0	dig2gam_vr0_n[3:0]				00
	1	1	↑	XX	0	0	dig2gam_vr1_n[5:0]						00
	1	1	↑	XX	0	0	dig2gam_vr2_n[5:0]						03
	1	1	↑	XX	0	0	0	dig2gam_vr4_n[4:0]					08
SET_GAMMA2	0	1	↑	XX	1	1	1	1	0	0	0	1	F1h
	1	1	↑	XX	0	0	0	0	0	0	dig2gam_dig2j0_p[1:0]		01
	1	1	↑	XX	0	0	0	0	0	0	dig2gam_dig2j1_p[1:0]		00
	1	1	↑	XX	0	0	0	0	dig2gam_vr0_p[3:0]				00
	1	1	↑	XX	0	0	dig2gam_vr1_p[5:0]						00
	1	1	↑	XX	0	0	dig2gam_vr2_p[5:0]						03
	1	1	↑	XX	0	0	0	dig2gam_vr4_p[4:0]					08
SET_GAMMA3	0	1	↑	XX	1	1	1	1	0	0	1	0	F2h
	1	1	↑	XX	0	0	0	dig2gam_vr6_n[4:0]					06
	1	1	↑	XX	0	0	0	0	dig2gam_vr13_n[3:0]				05
	1	1	↑	XX	0	dig2gam_vr20_n[6:0]							2b
	1	1	↑	XX	0	0	0	0	0	dig2gam_vr27_n[2:0]			04
	1	1	↑	XX	0	0	0	0	0	dig2gam_vr36_n[2:0]			04
	1	1	↑	XX	0	dig2gam_vr43_n[6:0]							41
SET_GAMMA4	0	1	↑	XX	1	1	1	1	0	0	1	1	F3h
	1	1	↑	XX	0	0	0	dig2gam_vr6_p[4:0]					0d
	1	1	↑	XX	0	0	0	0	dig2gam_vr13_p[3:0]				08
	1	1	↑	XX	0	dig2gam_vr20_p[6:0]							2e
	1	1	↑	XX	0	0	0	0	0	dig2gam_vr27_p[2:0]			04
	1	1	↑	XX	0	0	0	0	0	dig2gam_vr36_p[2:0]			05
	1	1	↑	XX	0	dig2gam_vr43_p[6:0]							3f
SET_GAMMA5	0	1	↑	XX	1	1	1	1	0	1	0	0	F4h
	1	1	↑	XX	0	0	0	0	dig2gam_vr50_n[3:0]				0c

	1	1	↑	XX	0	0	0	dig2gam_vr57_n[4:0]					17
	1	1	↑	XX	0	0	0	dig2gam_vr59_n[4:0]					18
	1	1	↑	XX	0	0	dig2gam_vr61_n[5:0]						13
	1	1	↑	XX	0	0	dig2gam_vr62_n[5:0]						17
	1	1	↑	XX	0	0	0	0	dig2gam_vr63_n[3:0]				0d
SET_GAMMA6	0	1	↑	XX	1	1	1	1	0	1	0	1	F5h
	1	1	↑	XX	0	0	0	0	dig2gam_vr50_p[3:0]				0c
	1	1	↑	XX	0	0	0	dig2gam_vr57_p[4:0]					18
	1	1	↑	XX	0	0	0	dig2gam_vr59_p[4:0]					14
	1	1	↑	XX	0	0	dig2gam_vr61_p[5:0]						14
	1	1	↑	XX	0	0	dig2gam_vr62_p[5:0]						18
	1	1	↑	XX	0	0	0	0	dig2gam_vr63_p[3:0]				0d

6.2. Description of Level 1 Command

6.2.1. Read display identification information (04h)

04h	Read display identification information 2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	0	1	0	0	04h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID2_1[7:0]								00
3rd Parameter	1	↑	1	XX	ID2_1[7:0]								93
4th Parameter	1	↑	1	XX	ID2_1[7:0]								06
Description	This read byte returns 24 bits display identification information. The 1st parameter is dummy data. The 2nd parameter (ID2_1 [7:0]): LCD module's manufacturer ID. The 3rd parameter (ID2_2 [7:0]): LCD module/driver version ID. The 4th parameter (ID2_3 [7:0]): LCD module/driver ID.												
Restriction													

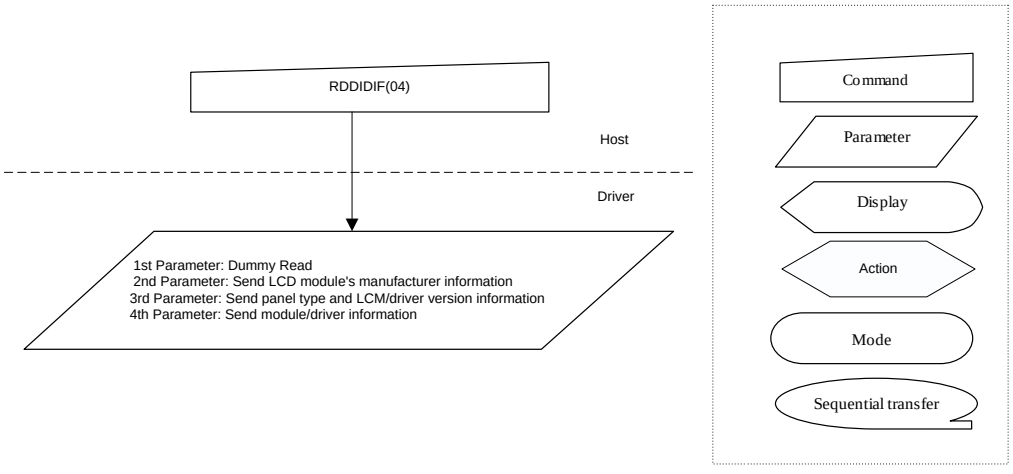
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	See description
SW Reset	See description
HW Reset	See description

Flow Chart



6.2.2. Read Display Status (09h)

09h	Read Display Status												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	0	0	1	0	0	1	09h
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	D[31:25]							X	00
3rd Parameter	1	↑	1	XX	0	D[22:20]			D[19:16]				61
4th Parameter	1	↑	1	XX	0	0	0	0	0	D[10:8]			00
5th Parameter	1	↑	1	XX	D[7:5]			0	0	0	0	0	00

Description

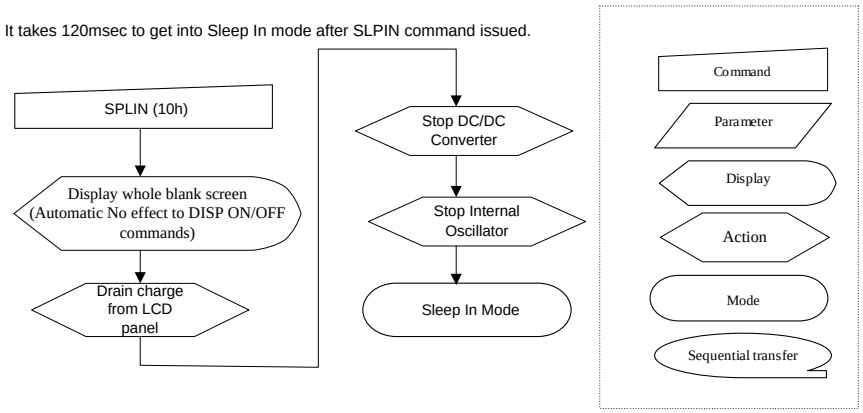
This command indicates the current status of the display as described in the table below:

Bit	Description	Value	Status
D31	Booster voltage status	O	Booster OFF
		1	Booster ON
D30	Row address order	O	Top to Bottom (When MADCTL B7='0')
		1	Bottom to Top (When MADCTL B7='1')
D29	Column address order	O	Left to Right (When MADCTL B6='0').
		1	Right to Left (When MADCTL B6='1').
D28	Row/column exchange	O	Normal Mode (When MADCTL B5='0').
		1	Reverse Mode (When MADCTL B5='1').
D27	Vertical refresh	O	LCD Refresh Top to BoUom (When MADCTL B4='0')
		1	LCD Refresh BoUom to Top (When MADCTL B4='1').
D26	RGB/BGR order	O	RGB (When MADCTL B3='0')
		1	BGR (When MADCTL B3='1')
D25	Horizontal refresh order	O	LCD Refresh Left to Right (When MADCTL B2='0')
		1	LCD Refresh Right to Left (When MADCTL B2='1')
D24	Not used	O	-
D23	Not used	O	-
D22	Interface color pixel format definition	101	16-bit/pixel
D21		110	18-bit/pixel
D20			
D19	Idle mode ON/OFF	O	Idle Mode OFF
		1	Idle Mode ON
D18	Partial mode ON/OFF	O	Partial Mode OFF

				1	Partial Mode ON
		D17	Sleep IN/OUT	O	Sleep IN Mode
				1	Sleep OUT Mode
		D16	Display normal mode ON/OFF	O	Display Normal Mode OFF.
				1	Display Normal Mode ON.
		D15	Vertical scrolling status	O	Scroll OFF
		D14	Not used	O	-
		D13	Inversion status	O	Not defined
		D12	All pixel ON	O	Not defined
		D11	All pixel OFF	O	Not defined
		D10	Display ON/OFF	O	
				1	Display is ON
		D9	Tearing effect line ON/OFF	O	Tearing Effect Line OFF
				1	Tearing Effect ON
		D5	Tearing effect line mode	0	Mode 1, V-Blanking only
				1	Mode 2, both H-Blanking and V-Blanking
		D4	Not used	O	-
		D3	Not used	O	-
		D2	Not used	O	-
		D1	Not used	O	-
		D0	Not used	O	-
Restriction					
Register Availability					

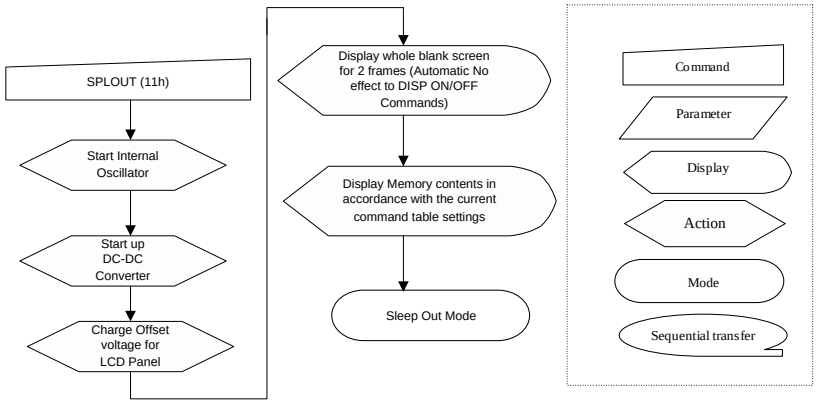
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

6.2.3. Enter Sleep Mode (10h)

<table>
<tr><td>10h</td><td colspan="13">Enter Sleep Mode</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>10h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command causes the LCD module to enter the minimum power consumption mode. In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped
 
MCU interface and memory are still working and the memory keeps its contents.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next to command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep IN Mode</td></tr><tr><td>SW Reset</td><td>Sleep IN Mode</td></tr><tr><td>HW Reset</td><td>Sleep IN Mode</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">  </td></tr>
</table>

6.2.4. Sleep Out Mode (11h)

<table>
<tr><td>11h</td><td colspan="13">Sleep Out Mode</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>11h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command turns off sleep mode.
the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits stabilize. The display module loads all display supplier’s factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep IN Mode</td></tr><tr><td>SW Reset</td><td>Sleep IN Mode</td></tr><tr><td>HW Reset</td><td>Sleep IN Mode</td></tr></table></td></tr>
</table>

Flow Chart	

SPLOUT (11h)
Start Internal Oscillator
Start up DC-DC Converter
Charge Offset voltage for LCD Panel
Display whole blank screen for 2 frames (Automatic No effect to DISP ON/OFF Commands)
Display Memory contents in accordance with the current command table settings
Sleep Out Mode
Command
Parameter
Display
Action
Mode
Sequential transfer

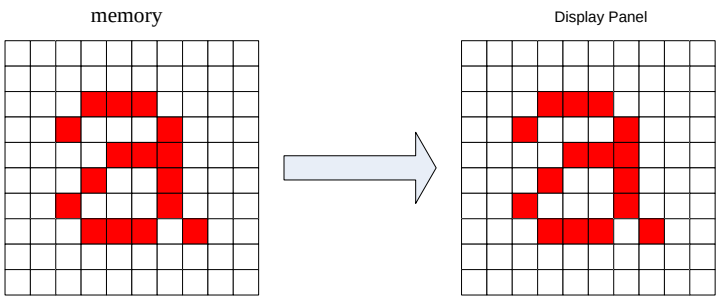
6.2.5. Partial Mode ON (12h)

<table>
<tr><td>12h</td><td colspan="13">Partial Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>12h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command turns on partial mode The partial mode window is described by the Partial Area command (30H).
To leave Partial mode, the Normal Display Mode On command (13H) should be written.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Partial mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>SW Reset</td><td>Normal Display Mode</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area (30h)</td></tr>
</table>

6.2.6. Normal Display Mode ON (13h)

<table>
<tr><td>13h</td><td colspan="13">Normal Display Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>13h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command returns the display to normal mode.
Normal display mode on means Partial mode off.
Exit from NORON by the Partial mode On command (12h)
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Normal Display mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>SW Reset</td><td>Normal Display Mode</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13">See Partial Area (30h)</td></tr>
</table>

6.2.7. Display Inversion OFF (20h)

20h	Display Inversion OFF												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	0	0	0	20h
Parameter	No Parameter												
Description	This command is used to recover from display inversion mode. This command makes no change of the content of frame memory. This command doesn't change any other status.  X = Don't care												
Restriction	This command has no effect when module already is inversion OFF mode.												

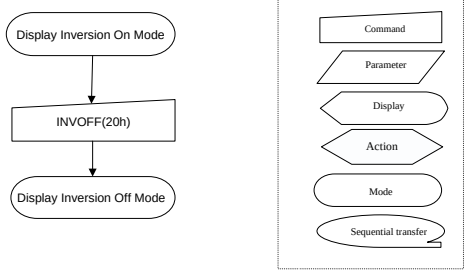
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

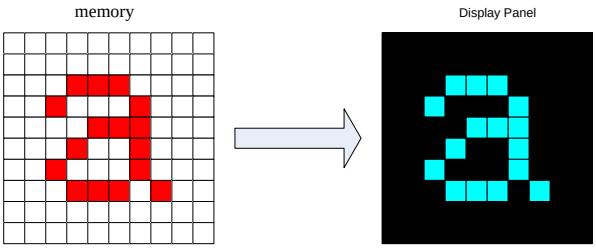
Default

Status	Default Value
Power On Sequence	Display Inversion OFF
SW Reset	Display Inversion OFF
HW Reset	Display Inversion OFF

Flow Chart



6.2.8. Display Inversion ON (21h)

21h	Display Inversion ON												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	0	0	0	1	21h
Parameter	No Parameter												
Description	This command is used to enter into display inversion mode. This command makes no change of the content of frame memory. Every bit is inverted from the frame memory to the display. This command doesn't change any other status. To exit Display inversion mode, the Display inversion OFF command (20h) should be written..  X = Don't care												
Restriction	This command has no effect when module already is inversion ON mode.												

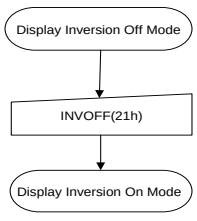
Register Availability

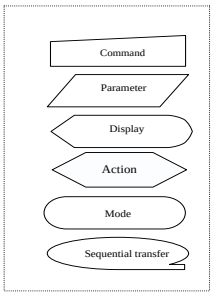
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

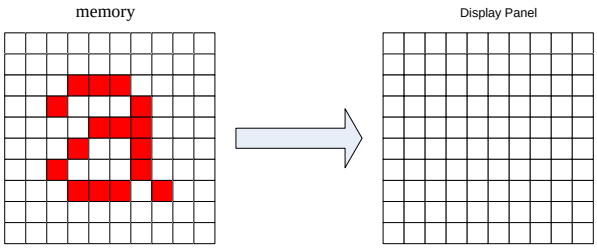
Status	Default Value
Power On Sequence	Display Inversion OFF
SW Reset	Display Inversion OFF
HW Reset	Display Inversion OFF

Flow Chart





6.2.9. Display OFF (28h)

28h	Display OFF												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	0	0	28h
Parameter	No Parameter												
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display.  X = Don't care												
Restriction	This command has no effect when module is already in display off mode.												

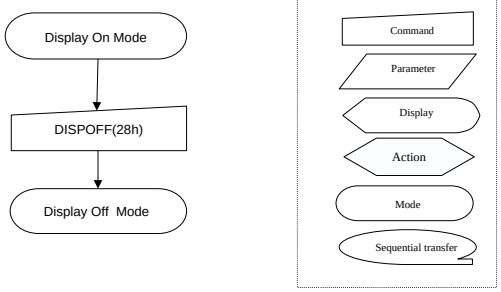
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

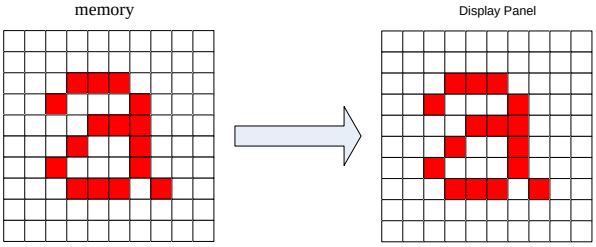
Default

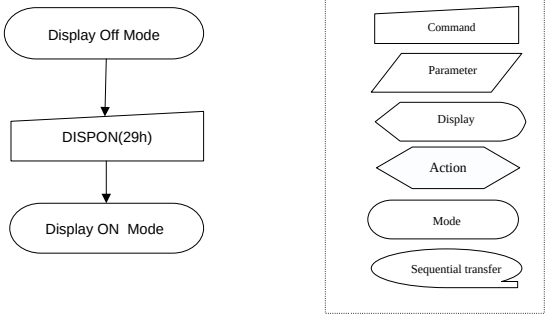
Status	Default Value
Power On Sequence	Display OFF
SW Reset	Display OFF
HW Reset	Display OFF

Flow Chart

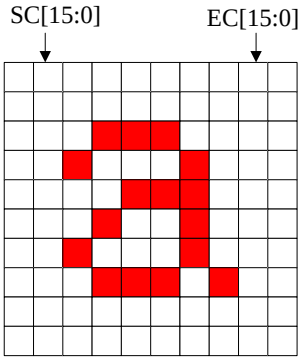


6.2.10. Display ON (29h)

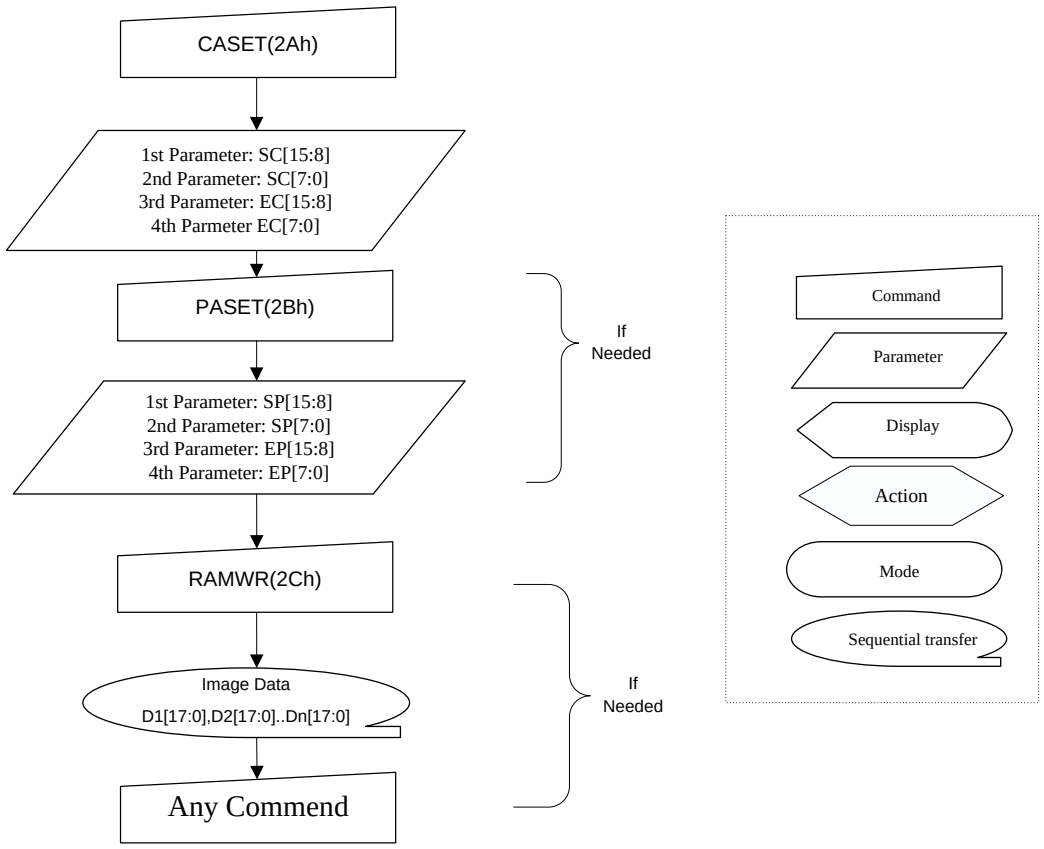
<table>
<tr><td>29h</td><td colspan="13">Display ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>29h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.
This command makes no change of contents of frame memory.
This command does not change any other status.
 

X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in display on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13"><table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Display OFF</td></tr>
<tr><td>SW Reset</td><td>Display OFF</td></tr>
<tr><td>HW Reset</td><td>Display OFF</td></tr>
</table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

6.2.11. Column Address Set (2Ah)

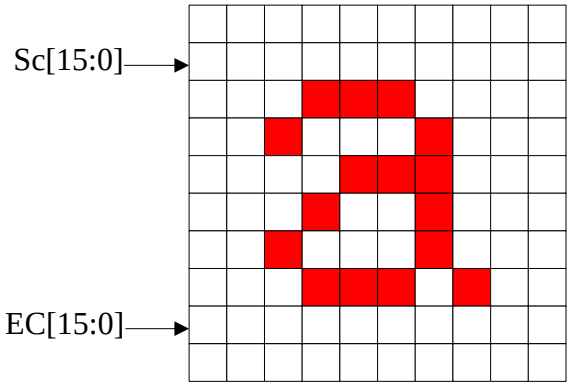
<table>
<tr><td>2Ah</td><td colspan="13">Column Address Set</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>2Ah</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>SC15</td><td>SC14</td><td>SC13</td><td>SC12</td><td>SC11</td><td>SC10</td><td>SC9</td><td>SC8</td><td rowspan="2">Note1</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>SC7</td><td>SC6</td><td>SC5</td><td>SC4</td><td>SC3</td><td>SC2</td><td>SC1</td><td>SC0</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>EC15</td><td>EC14</td><td>EC13</td><td>EC12</td><td>EC11</td><td>EC10</td><td>EC9</td><td>EC8</td><td rowspan="2">Note1</td></tr>
<tr><td>4th Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>EC7</td><td>EC6</td><td>EC5</td><td>EC4</td><td>EC3</td><td>EC2</td><td>EC1</td><td>EC0</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to define area of frame memory where MCU can access. This command makes no change on the
other driver status. The values of SC [15:0] and EC [15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory..
 

X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">SC [15:0] always must be equal to or less than EC [15:0].
Note 1: When SC [15:0] or EC [15:0] is greater than 00EFh (When MADCTL’s B5 = 0) or 013Fh
(When MADCTL’s B5 = 1), data of out of range will be ignored</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th colspan="2">Default Value</th></tr><tr><td>Power On Sequence</td><td>SC [15:0]=0000h</td><td>EC [15:0]=00EFh</td></tr><tr><td rowspan="2">SW Reset</td><td rowspan="2">SC [15:0]=0000h</td><td>If MADCTL’s B5 = 0: EC [15:0]=00EFh</td></tr><tr><td>If MADCTL’s B5 = 1: EC [15:0]=013Fh</td></tr><tr><td>HW Reset</td><td>SC [15:0]=0000h</td><td>EC [15:0]=00EFh</td></tr></table></td></tr>
</table>

Flow Chart	

CASET(2Ah)
1st Parameter: SC[15:8]
2nd Parameter: SC[7:0]
3rd Parameter: EC[15:8]
4th Parmeter EC[7:0]
PASET(2Bh)
1st Parameter: SP[15:8]
2nd Parameter: SP[7:0]
3rd Parameter: EP[15:8]
4th Parameter: EP[7:0]
RAMWR(2Ch)
Image Data
D1[17:0],D2[17:0]..Dn[17:0]
Any Commend
If Needed
If Needed
Command
Parameter
Display
Action
Mode
Sequential transfer

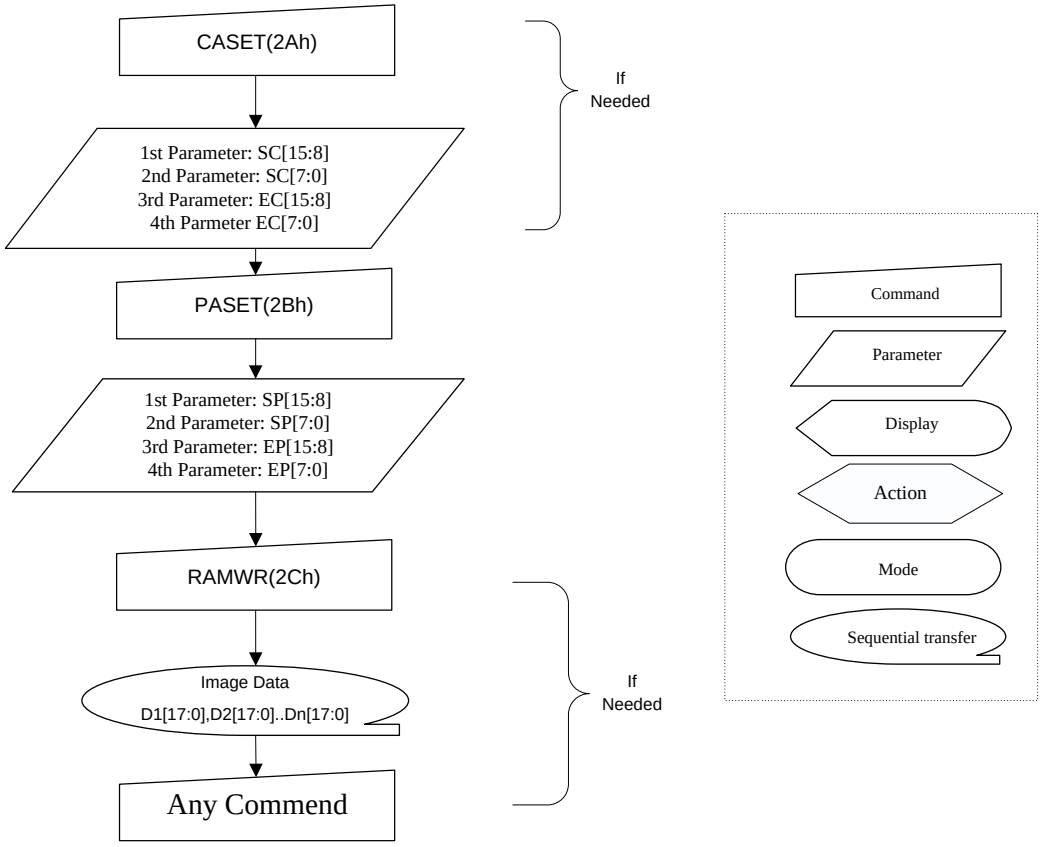
6.2.12. Row Address Set (2Bh)

<table>
<tr><td>2Bh</td><td colspan="13">Row Address Set</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>2Bh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>SP15</td><td>SP14</td><td>SP13</td><td>SP12</td><td>SP11</td><td>SP10</td><td>SP9</td><td>SP8</td><td rowspan="2">Note1</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>SP7</td><td>SP6</td><td>SP5</td><td>SP4</td><td>SP3</td><td>SP2</td><td>SP1</td><td>SP0</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>EP15</td><td>EP14</td><td>EP13</td><td>EP12</td><td>EP11</td><td>EP10</td><td>EP9</td><td>EP8</td><td rowspan="2">Note1</td></tr>
<tr><td>4th Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>EP7</td><td>EP6</td><td>EP5</td><td>EP4</td><td>EP3</td><td>EP2</td><td>EP1</td><td>EP0</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to define area of frame memory where MCU can access. This command makes no change on the
other driver status. The values of SP [15:0] and EP [15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.
 

X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="13">SP [15:0] always must be equal to or less than EP [15:0]
Note 1: When SP [15:0] or EP [15:0] is greater than 013Fh (When MADCTL’s B5 = 0) or 00EFh (When MADCTL’s B5 = 1), data of out of range will be ignored.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th colspan="2">Default Value</th></tr><tr><td>Power On Sequence</td><td>SP [15:0]=0000h</td><td>EP [15:0]=013Fh</td></tr><tr><td rowspan="2">SW Reset</td><td rowspan="2">SP [15:0]=0000h</td><td>If MADCTL’s B5 = 0: EP [15:0]=013Fh</td></tr><tr><td>If MADCTL’s B5 = 1: EP [15:0]=0EFh</td></tr></table></td></tr>
</table>

	HW Reset	SP [15:0]=0000h	EP [15:0]=013Fh

Flow Chart



6.2.13. Memory Write (2Ch)

2Ch	Memory Write												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch
1st Parameter	1	1	↑	D1 [17:0]									XX
:	1	1	↑	Dx [17:0]									XX
Nth Parameter	1	1	↑	Dn [17:0]									XX
Description	This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting.) Then D [17:0] isstored in frame memory and the column register and the page register incremented. Sending any other command can stop frame Write. X = Don't care.												
Restriction	In all color modes, there is no restriction on length of parameters.												

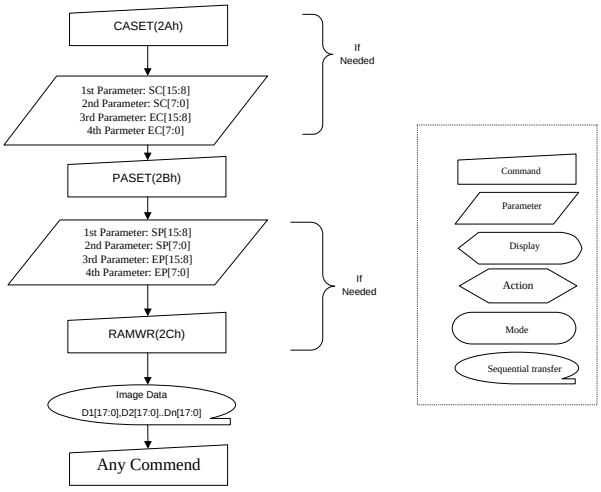
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

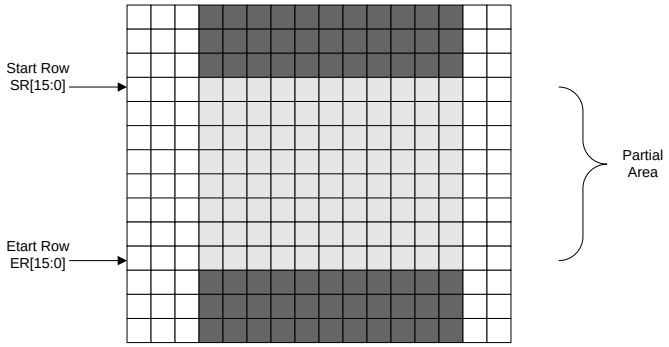
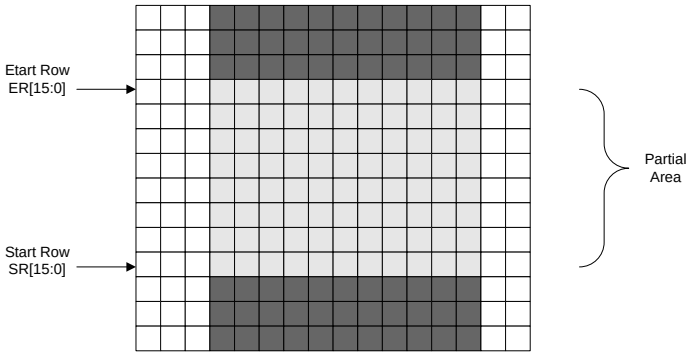
Default

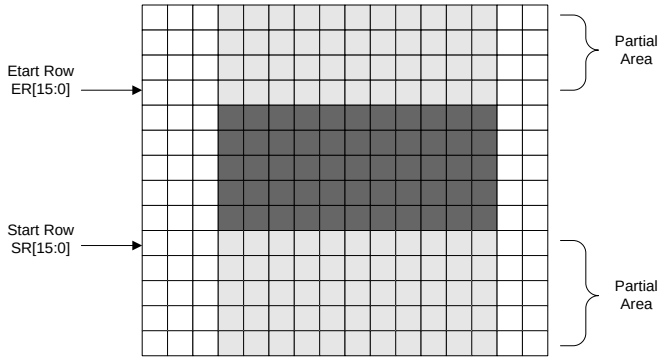
Status	Default Value
Power On Sequence	Contents of memory is set randomly
SW Reset	Contents of memory is not cleared
HW Reset	Contents of memory is not cleared

Flow Chart



6.2.14. Partial Area (30h)

30h	Partial Area												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
1st Parameter	1	1	↑	XX	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	00
2nd Parameter	1	1	↑	XX	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00
3rd Parameter	1	1	↑	XX	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	01
4th Parameter	1	1	↑	XX	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	3F
Description	This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. If End Row>Start Row when MADCTL B4=0:-  If End Row>Start Row when MADCTL B4=1:-  If End Row<Start Row when MADCTL B4=0:-													



If End Row = Start Row then the Partial Area will be one row deep.

X = Don't care.

Restriction: SR [15…0] and ER [15…0] cannot be 0000h nor exceed 013Fh.

Register Availability

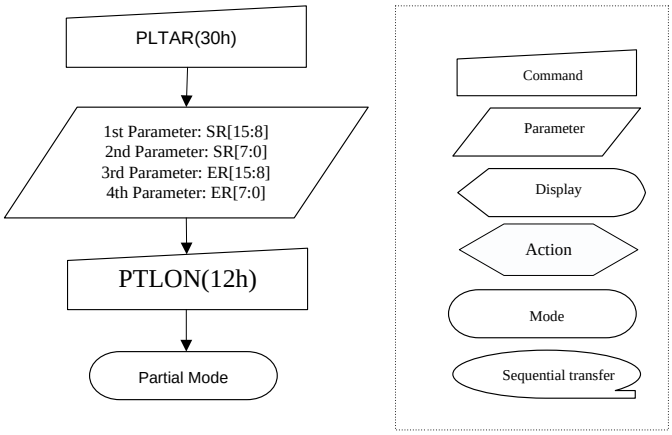
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

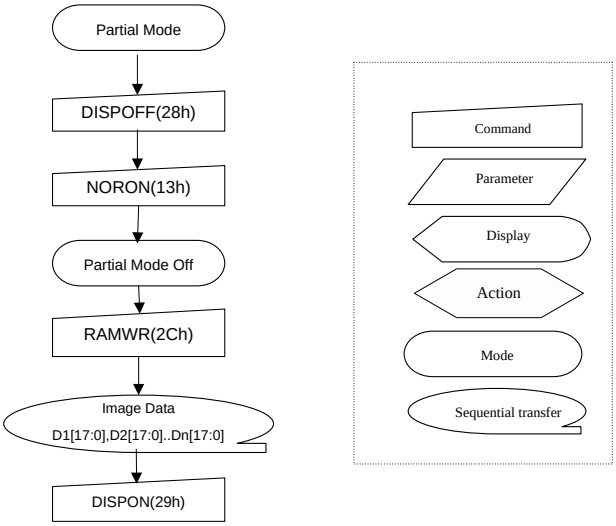
Status	Default Value	
	SR [15:0]	ER [15:0]
Power On Sequence	16'h0000h	16'h013Fh
SW Reset	16'h0000h	16'h013Fh
HW Reset	16'h0000h	16'h013Fh

Flow Chart

1. To Enter Partial Mode



2. To Leave Partial Mode



6.2.15. Vertical Scrolling Definition (33h)

33h	Vertical Scrolling Definition												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
1st Parameter	1	1	↑	XX	TFA [15:8]								00
2nd Parameter	1	1	↑	XX	TFA [7:0]								00
3rd Parameter	1	1	↑	XX	VSA [15:8]								01
4th Parameter	1	1	↑	XX	VSA [7:0]								40

Description

This command defines the Vertical Scrolling Area of the display.

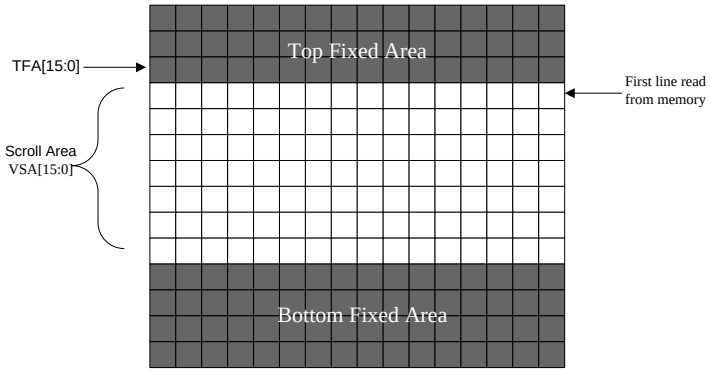
When MADCTL B4=0

The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).

The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame

Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears

immediately after the bottom most line of the Top Fixed Area.



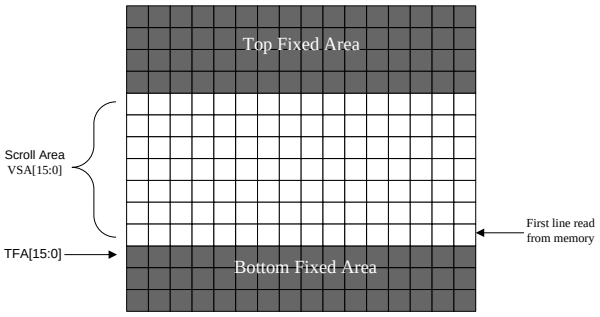
When MADCTL B4=1

The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).

The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame

Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears

immediately after the top most line of the Top Fixed Area.



X = Don't care.

Restriction

Register Availability

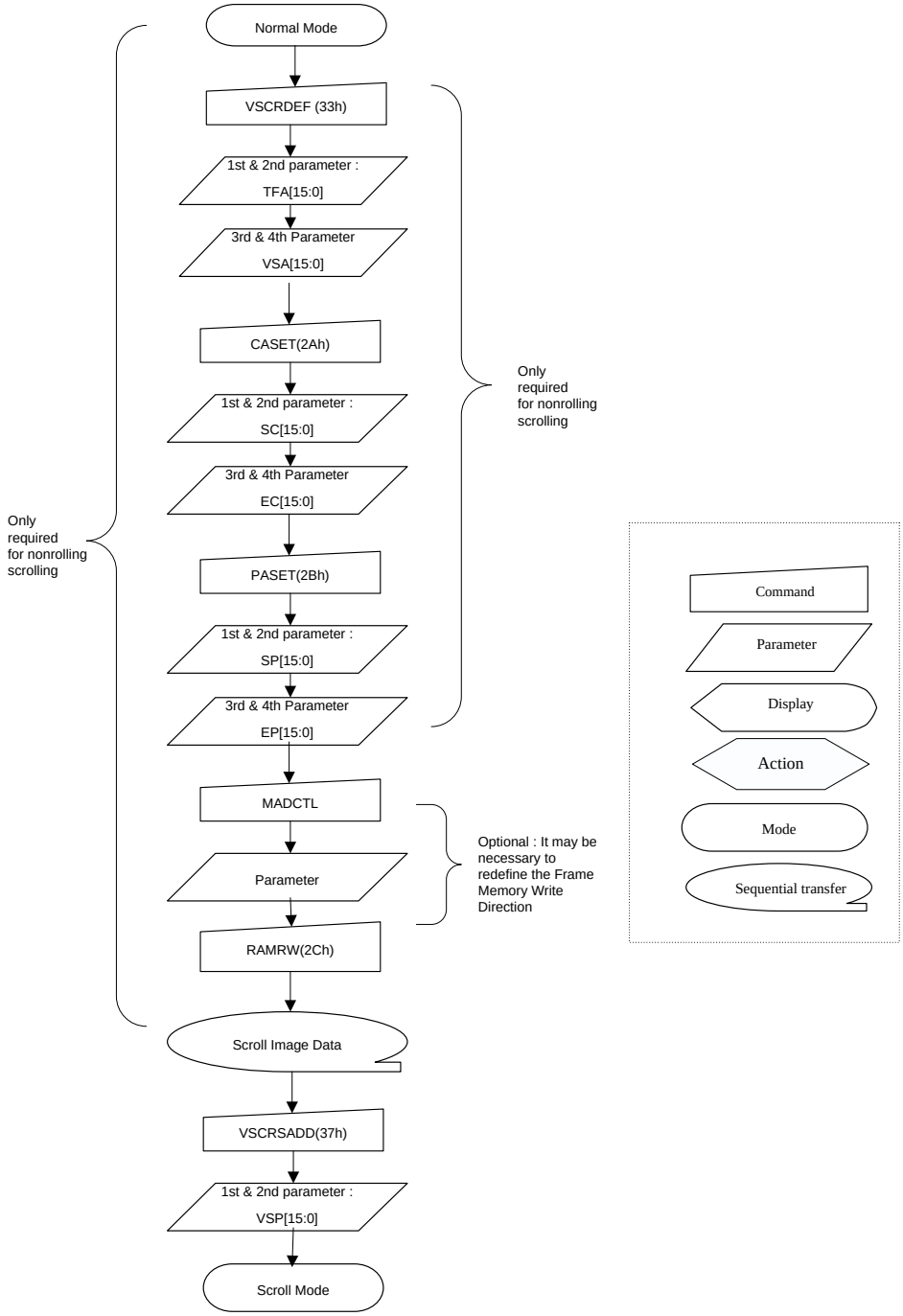
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	TFA [15:0]	VSA [15:0]
Power On Sequence	16'h0000h	16'h0140h
SW Reset	16'h0000h	16'h0140h
HW Reset	16'h0000h	16'h0140h

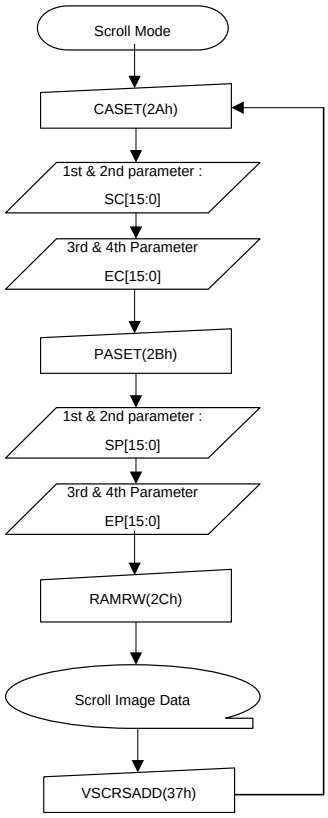
Flow Chart

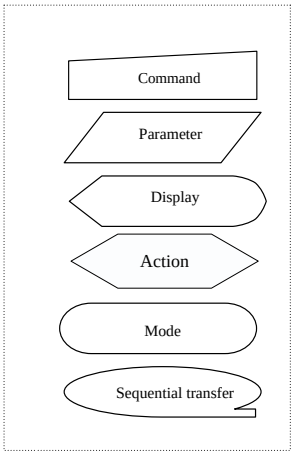
1. To enter Vertical Scroll Mode :



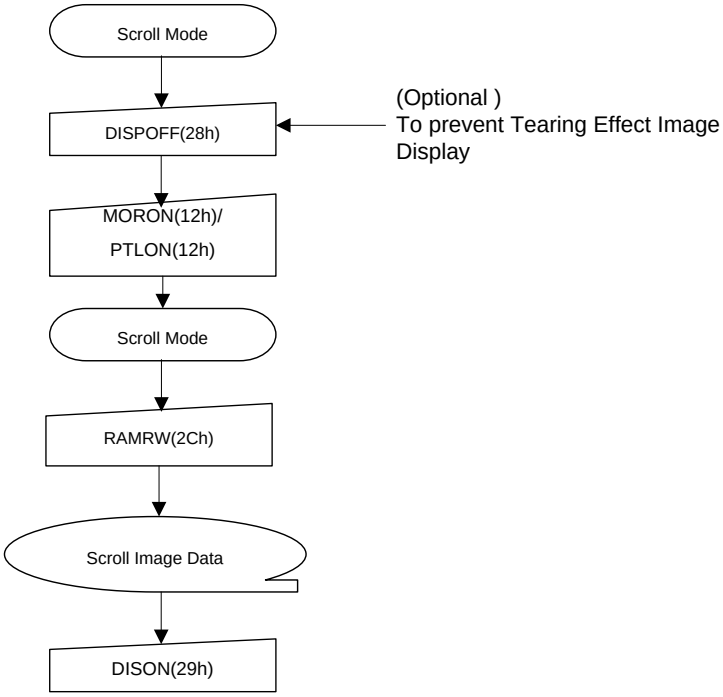
Note : The Frame Memory Window size ,must be defined correctly otherwise undesirable image will be displayed.

2.Continuous Scroll :



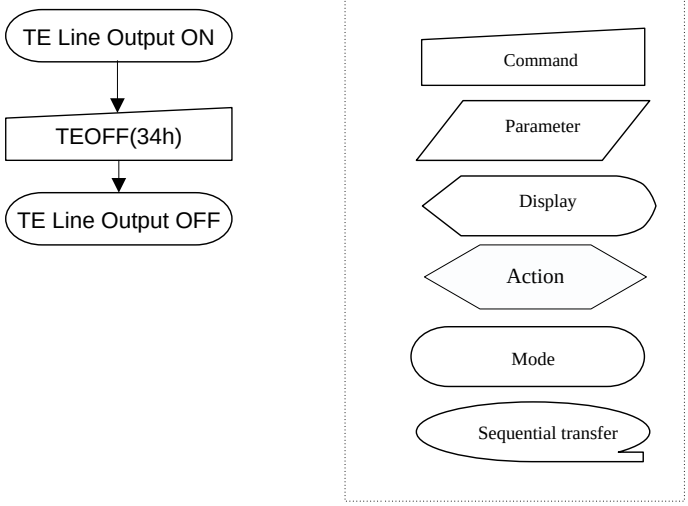


3.To Leave Vertical Scroll Mode:



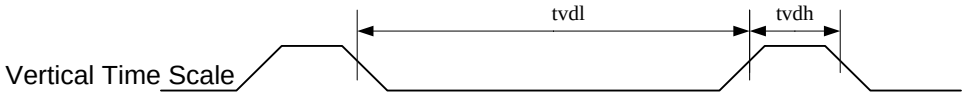
Note: Scroll Mode can be left by both the Normal Display Mode ON (13h) and Partial Mode ON (12h) commands.

6.2.16. Tearing Effect Line OFF (34h)

<table>
<tr><td>34h</td><td colspan="13">Tearing Effect Line OFF</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>34h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already OFF.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>SW Reset</td><td>OFF</td></tr><tr><td>HW Reset</td><td>OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

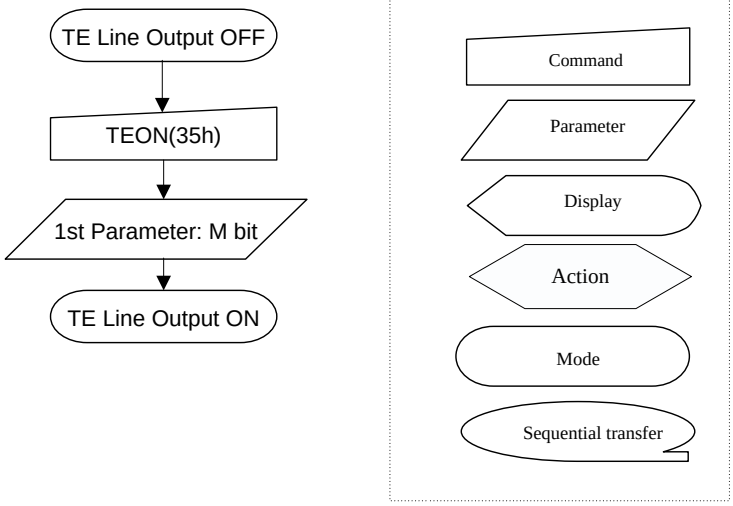
6.2.17. Tearing Effect Line ON (35h)

<table>
<tr><td>35h</td><td colspan="13">Tearing Effect Line ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>35h</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>M</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by
changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

When M=0:
The Tearing Effect Output line consists of V-Blanking information only:
 

When M=1:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:
 

Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when Tearing Effect output is already ON</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>SW Reset</td><td>OFF</td></tr><tr><td>HW Reset</td><td>OFF</td></tr></table></td></tr>
</table>

Flow Chart	

TE Line Output OFF
TEON(35h)
1st Parameter: M bit
TE Line Output ON
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.18. Memory Access Control(36h)

36h	Tearing Effect Line ON												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	0	36h
Parameter	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	0	0	00

Description

This command defines read/write scanning direction of frame memory.

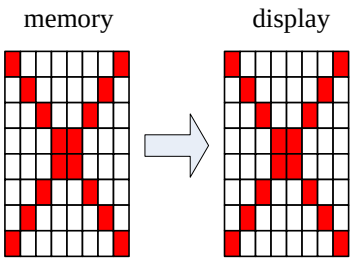
This command makes no change on the other driver status.

Bit	Name	Description
MY	Row Address Order	These 3 bits control MCU to memory write/read direction.
MX	Column Address Order	
MV	Row / Column Exchange	
ML	Vertical Refresh Order	LCD vertical refresh direction control.
BGR	RGB-BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)
MH	Horizontal Refresh ORDER	LCD horizontal refreshing direction control.

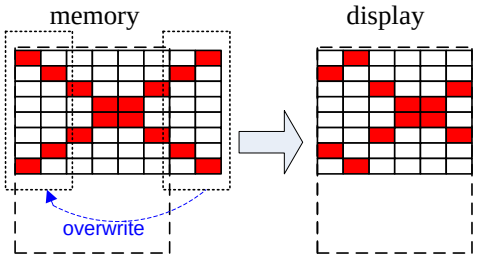
Note: When BGR bit is changed, the new setting is active immediately without update the content in Frame Memory again.

X = Don't care.

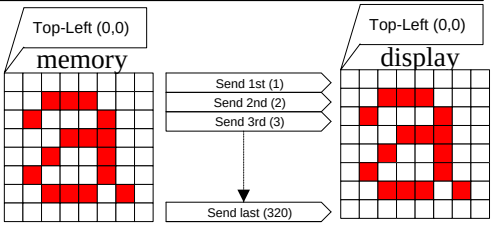
MV(Row / Column Exchange bit)="0"



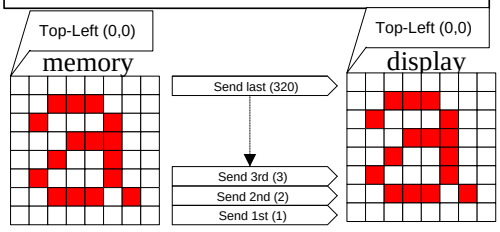
MV(Row / Column Exchange bit)="1"

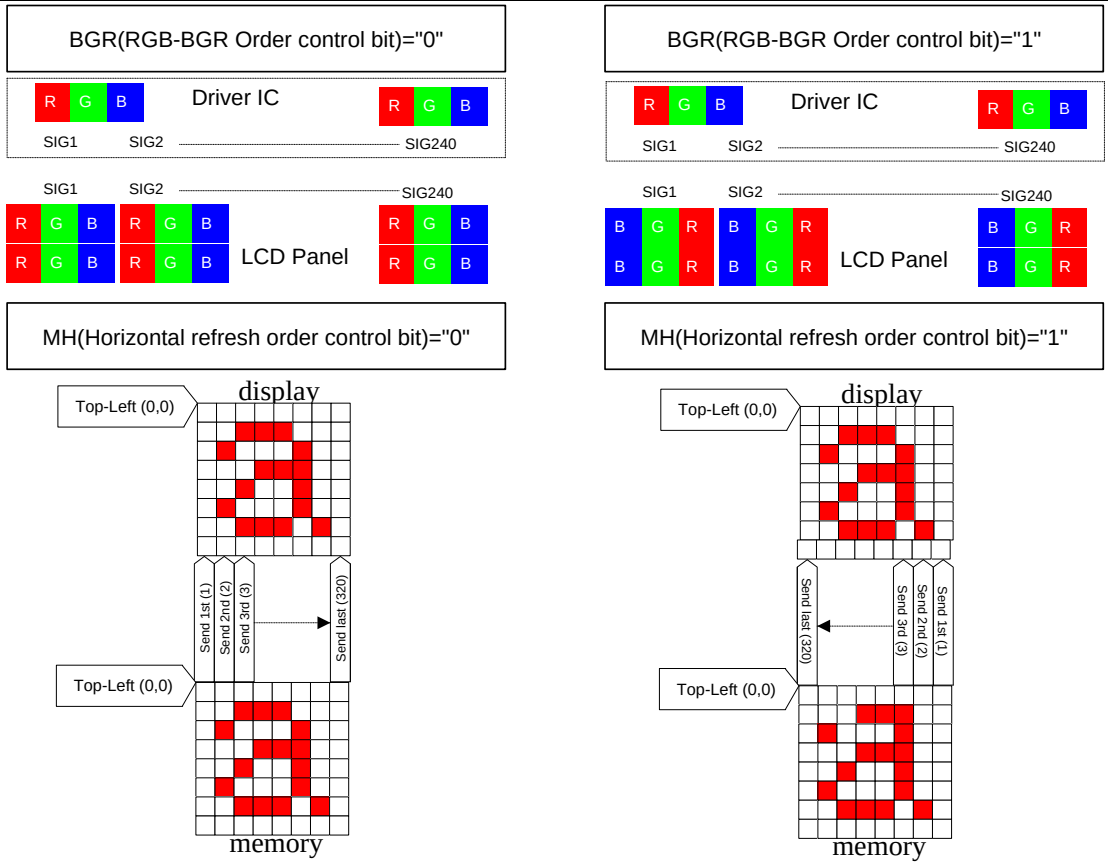


MV(Vertical refresh order bit)="0"



MV(Vertical refresh order bit)="1"





Note: Top-Left (0,0) means a physical memory location.

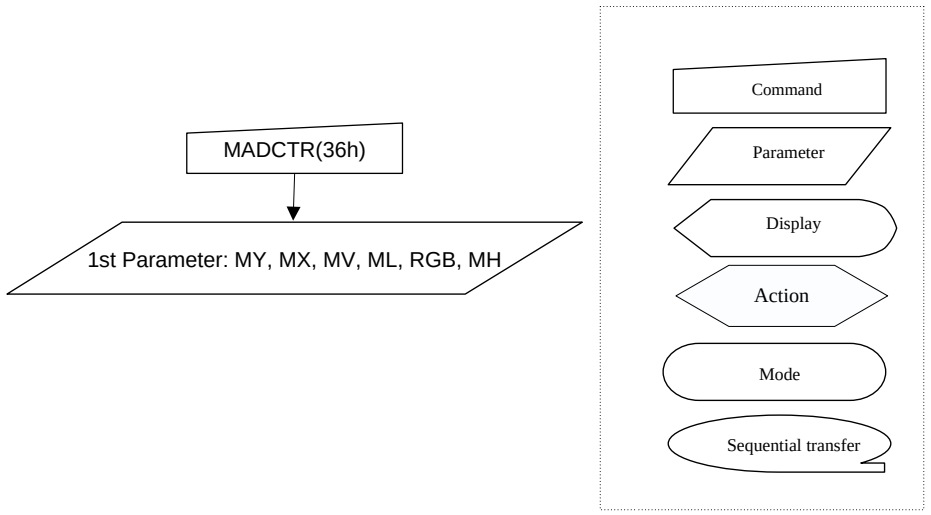
Restriction	This command has no effect when Tearing Effect output is already ON

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

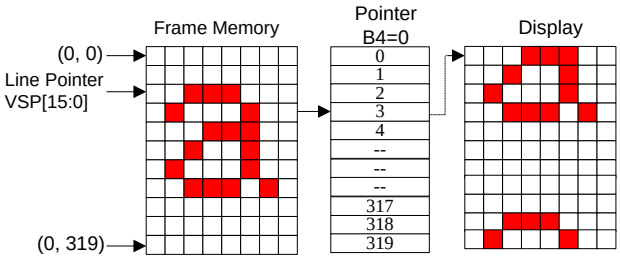
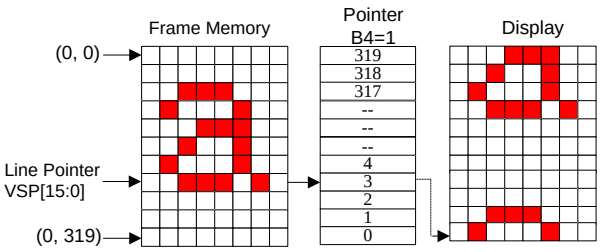
Default

Status	Default Value
Power On Sequence	8'h00h
SW Reset	No change
HW Reset	8'h00h

Flow Chart	

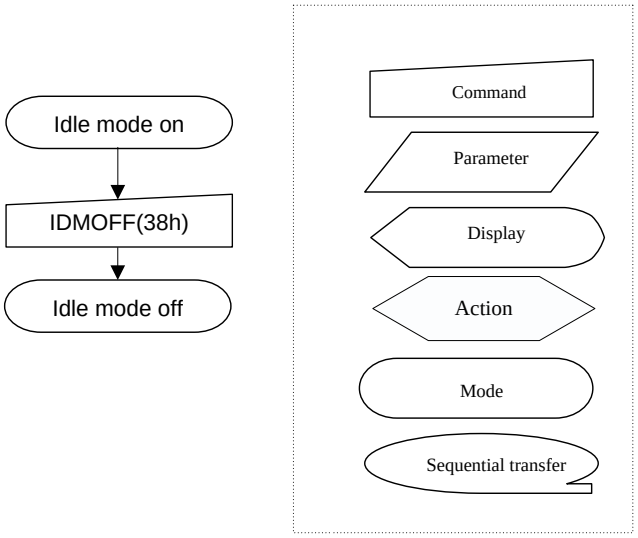
MADCTR(36h)
1st Parameter: MY, MX, MV, ML, RGB, MH
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.19. Vertical Scrolling Start Address (37h)

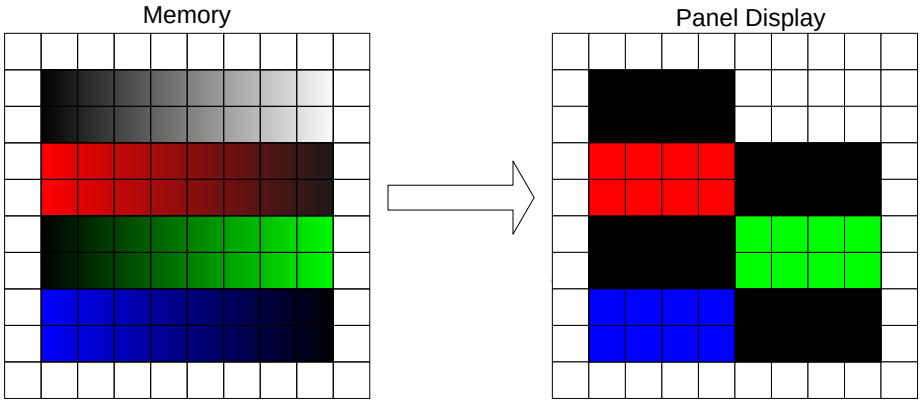
37h	VSCRSADD (Vertical Scrolling Start Address)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	1	1	1	37h
1st Parameter	1	1	↑	XX	VSP [15:8]								00
2nd Parameter	1	1	↑	XX	VSP [7:0]								00
Description	This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:- When MADCTL B4=0 Example: When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP='3'.  When MADCTL B4=1 Example: When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP='3'.  *Note: (1) When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer.* *(2) This command is ignored when the GC9306 enters Partial mode.* X = Don't care												
Restriction	This command has no effect when Tearing Effect output is already ON												

<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>VSP [15:0]</th></tr>
<tr><td>Power On Sequence</td><td>16’h0000h</td></tr>
<tr><td>SW Reset</td><td>16’h0000h</td></tr>
<tr><td>HW Reset</td><td>16’h0000h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

6.2.20. Idle Mode OFF (38h)

<table>
<tr><td>38h</td><td colspan="13">Idle Mode OFF</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>38h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to recover from Idle mode on.
In the idle off mode, LCD can display maximum 262,144 colors.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle mode OFF</td></tr><tr><td>SW Reset</td><td>Idle mode OFF</td></tr><tr><td>HW Reset</td><td>Idle mode OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

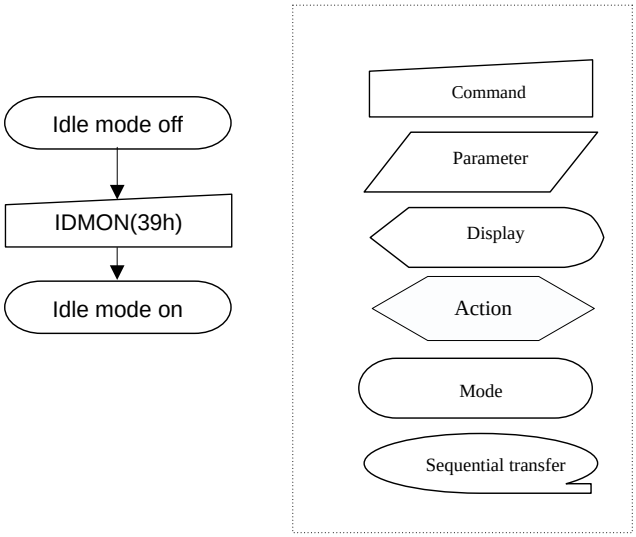
6.2.21. Idle Mode ON (39h)

<table>
<tr><td>39h</td><td colspan="13">Idle Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>39h</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to enter into Idle mode on.
In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.
 

<table><tr><td></td><td colspan="3">Memory Contents vs. Display Color</td></tr><tr><td></td><td>R5 R4 R3 R2 R1
R0</td><td>G5 G4 G3 G2 G1
G0</td><td>B5 B4 B3 B2 B1
B0</td></tr><tr><td>Black</td><td>0XXXXX</td><td>0XXXXX</td><td>0XXXXX</td></tr><tr><td>Blue</td><td>0XXXXX</td><td>0XXXXX</td><td>1XXXXX</td></tr><tr><td>Red</td><td>1XXXXX</td><td>0XXXXX</td><td>0XXXXX</td></tr><tr><td>Magenta</td><td>1XXXXX</td><td>0XXXXX</td><td>1XXXXX</td></tr><tr><td>Green</td><td>0XXXXX</td><td>1XXXXX</td><td>0XXXXX</td></tr><tr><td>Cyan</td><td>0XXXXX</td><td>1XXXXX</td><td>1XXXXX</td></tr><tr><td>Yellow</td><td>1XXXXX</td><td>1XXXXX</td><td>0XXXXX</td></tr><tr><td>White</td><td>1XXXXX</td><td>1XXXXX</td><td>1XXXXX</td></tr></table>X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
</table>

Register Availability

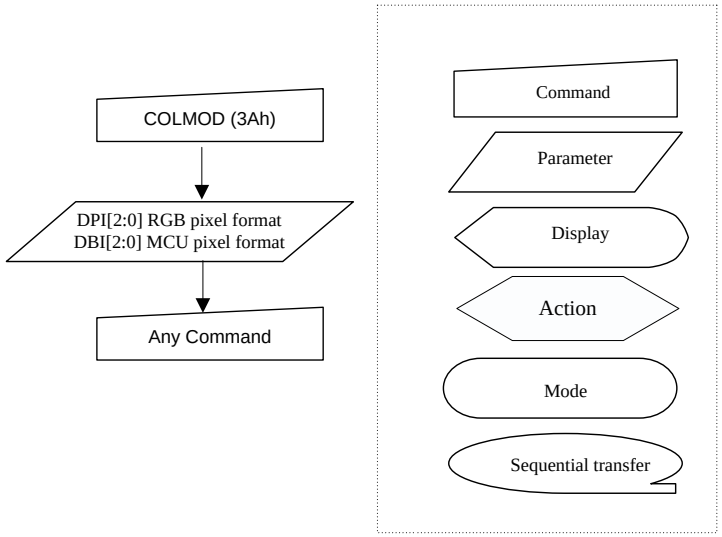
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

<table>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>Idle mode OFF</td></tr>
<tr><td>SW Reset</td><td>Idle mode OFF</td></tr>
<tr><td>HW Reset</td><td>Idle mode OFF</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>


</td></tr>
</table>

6.2.22. COLMOD: Pixel Format Set (3Ah)

<table>
<tr><td>3Ah</td><td colspan="13">Pixel Format Set</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>3Ah</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td colspan="3">DPI [2:0]</td><td>0</td><td colspan="3">DBI [2:0]</td><td>66</td></tr>
<tr><td>Description</td><td colspan="13">This command sets the pixel format for the RGB image data used by the interface. DPI [2:0] is the pixel format select of RGB interface and DBI [2:0] is the pixel format of MCU interface. If a particular interface, either RGB interface or MCU interface, is not used then the corresponding bits in the parameter are ignored. The pixel format is shown in the table below.
<table>
<tr><th colspan="3">DPI [2:0]</th><th>RGB Interface Format</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>18 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
</table>
<table>
<tr><th colspan="3">DBI [2:0]</th><th>MCU Interface Format</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>18 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Reserved</td></tr>
</table>
If using RGB Interface must selection serial interface.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="13">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr>
<tr><th>DPI [2:0]</th><th>DBI [2:0]</th></tr>
<tr><td>Power On Sequence</td><td>3’b110</td><td>3’b110</td></tr>
<tr><td>SW Reset</td><td>No Change</td><td>No Change</td></tr>
<tr><td>HW Reset</td><td>3’b110</td><td>3’b110</td></tr>
</table>
</td></tr>
</table>

Flow Chart	

COLMOD (3Ah)
DPI[2:0] RGB pixel format
DBI[2:0] MCU pixel format
Any Command
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.23. Write Memory Contiue (3Ch)

3Ch	write_memory_continue												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	D1[17..8]	0	0	1	1	1	1	0	0	3Ch
1st Parameter	1	1	↑	Dx[17..8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]	0003FF
Xth Parameter	1	1	↑	D1[17..8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]	0003FF
Nth Parameter	1	1	↑	Dn[17..8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]	0003FF
Description	This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command. **If set_address_mode B5 = 0:** Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If the number of pixels exceeds (EC –SC + 1) * (EP – SP + 1) the extra pixels are ignored. **If set_address_mode B5 = 1:** Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value and the page register equals the EP value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP –SP + 1) the extra pixels are ignored. Sending any other command can stop frame Write. Frame Memory Access and Interface setting (B3h), WEMODE=0 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored. Frame Memory Access and Interface setting (B3h), WEMODE=1 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.												
Restriction	A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write address. Otherwise, data written with write_memory_continue is written to undefined addresses.												

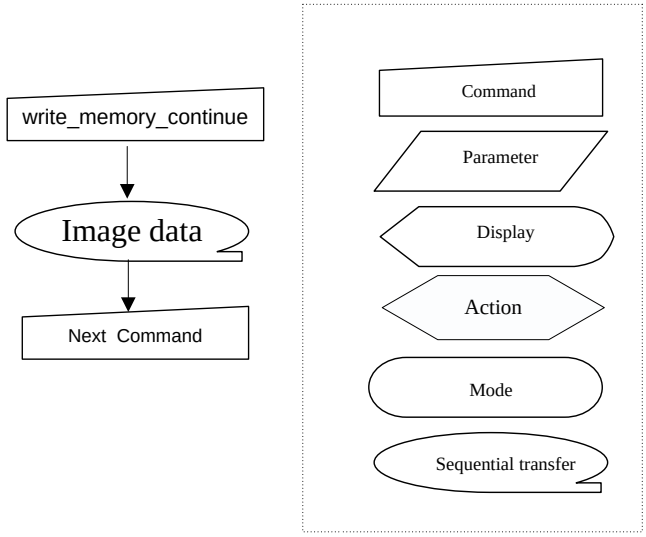
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

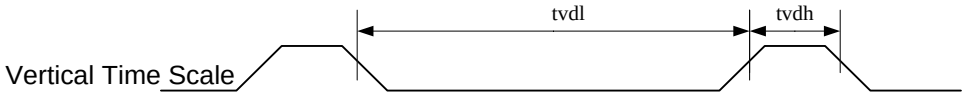
Default

Status	Default Value
Power On Sequence	Random value
SW Reset	No change
HW Reset	No change

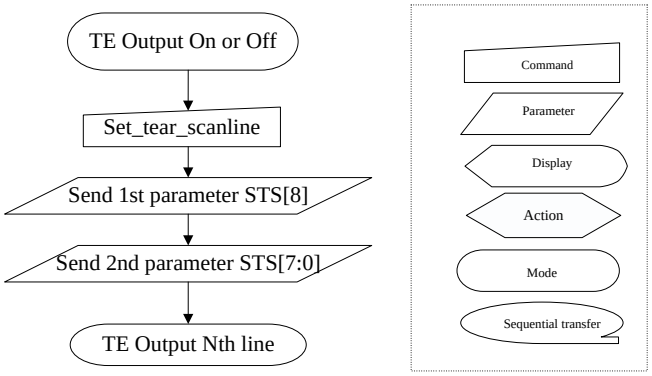
Flow Chart



6.2.24. Set_Tear_Scanline (44h)

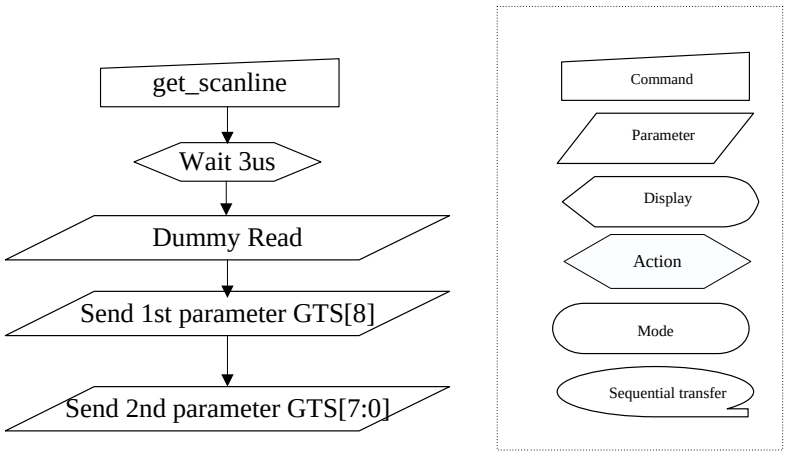
<table>
<tr><td>44h</td><td colspan="12">Set_Tear_Scanline</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>44h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>STS [8]</td><td>00</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>STS [7]</td><td>STS [6]</td><td>STS [5]</td><td>STS [4]</td><td>STS [3]</td><td>STS [2]</td><td>STS [1]</td><td>STS [0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="12">This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line equal the value of STS[8:0]
 

Note:that set_tear_scanline with STS is equivalent to set_tear_on with 8+GateN(N=1、2、3...320)
eg:when the STS[8:0]=8,the TE will output at the position of Gate1.
when the STS[8:0]=9,the TE will output at the position of Gate2.
when the STS[8:0]=10,the TE will output at the position of Gate3.
…….
The Tearing Effect Output line shall be active low when the display module is in Sleep mode.</td></tr>
<tr><td>Restriction</td><td colspan="12"></td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>STS [8:0]=0000h</td></tr><tr><td>SW Reset</td><td>STS [8:0]=0000h</td></tr><tr><td>HW Reset</td><td>STS [8:0]=0000h</td></tr></table></td></tr>
</table>

Flow Chart	

TE Output On or Off
Set_tear_scanline
Send 1st parameter STS[8]
Send 2nd parameter STS[7:0]
TE Output Nth line
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.25. Get_Scanline (45h)

<table>
<tr><td>45h</td><td colspan="13">Get_Scanline</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>45h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>GTS [8]</td><td>00</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>XX</td><td>GTS [7]</td><td>GTS [6]</td><td>GTS [5]</td><td>GTS [4]</td><td>GTS [3]</td><td>GTS [2]</td><td>GTS [1]</td><td>GTS [0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command returns the setting value of STS[8:0] .
When in Sleep Mode, the value returned by get_scanline is undefined.</td></tr>
<tr><td>Restriction</td><td colspan="13">None</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>GTS [9:0]=0000h</td></tr><tr><td>SW Reset</td><td>GTS [9:0]=0000h</td></tr><tr><td>HW Reset</td><td>GTS [9:0]=0000h</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="13"> 
</td></tr>
</table>

6.2.26. Write Display Brightness (51h)

51h	Write Display Brightness												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	1	0	1	0	0	0	1	51h
1st Parameter	1	1	↑	XX	DBV[7]	DBV[6]	DBV[5]	DBV[4]	DBV[3]	DBV[6]	DBV[5]	DBV[4]	00
Description	This command is used to adjust the brightness value of the display. It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.												
Restriction	None												

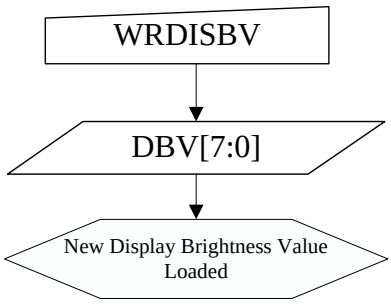
Register Availability

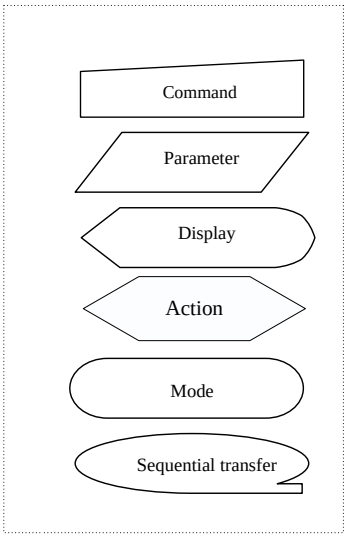
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	DBV [7:0]= 8'h00
SW Reset	DBV [7:0]= 8'h00
HW Reset	DBV [7:0]= 8'h00

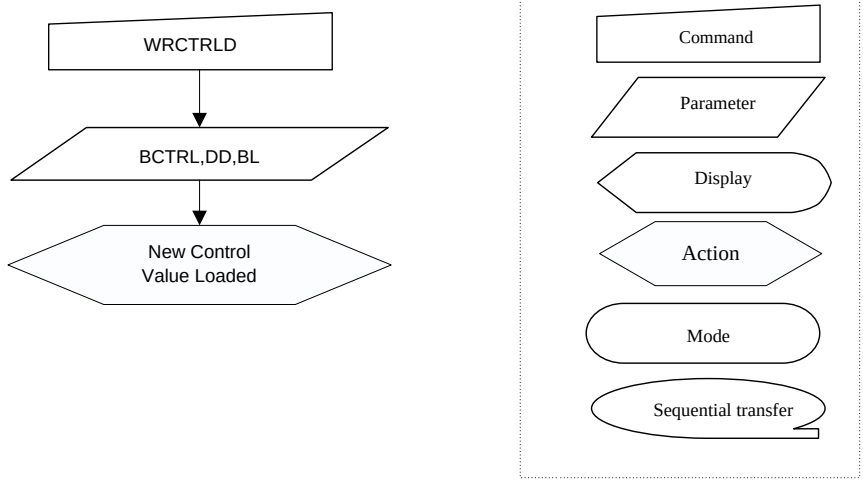
Flow Chart





6.2.27. Write CTRL Display (53h)

<table>
<tr><td>53h</td><td colspan="13">Write CTRL Display</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>53h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>0</td><td>BCTRL</td><td>0</td><td>DD</td><td>BL</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">This command is used to return brightness setting.
BCTRL: Brightness Control Block On/Off,
‘0’ = Off (Brightness registers are 00h)
‘1’ = On (Brightness registers are active, according to the DBV[7..0] parameters.)
DD: Display Dimming
‘0’ = Display Dimming is off
‘1’ = Display Dimming is on
BL: Backlight On/Off
‘0’ = Off (Completely turn off backlight circuit. Control lines must be low.)
‘1’ = On</td></tr>
<tr><td>Restriction</td><td colspan="13">The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter
(= more than 2 RDX cycle) on DBI.
Only 2nd parameter is sent on DSI (The 1st parameter is not sent).</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr><tr><th>BCTRL</th><th>DD</th><th>BL</th></tr><tr><td>Power On Sequence</td><td>1’b0</td><td>1’b0</td><td>1’b0</td></tr><tr><td>SW Reset</td><td>1’b0</td><td>1’b0</td><td>1’b0</td></tr><tr><td>HW Reset</td><td>1’b0</td><td>1’b0</td><td>1’b0</td></tr></table></td></tr>
</table>

Flow Chart	

WRCTRLD
BCTRL,DD,BL
New Control
Value Loaded
Command
Parameter
Display
Action
Mode
Sequential transfer

6.2.28. Read ID1 (DAh)

DCh	Read ID2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	1	0	0	DAh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID3 [7:0]								00h
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver version ID and the ID parameter range is from 80h to FFh. The ID3 can be programmed by MTP function. X = Don't care												
Restriction	None												

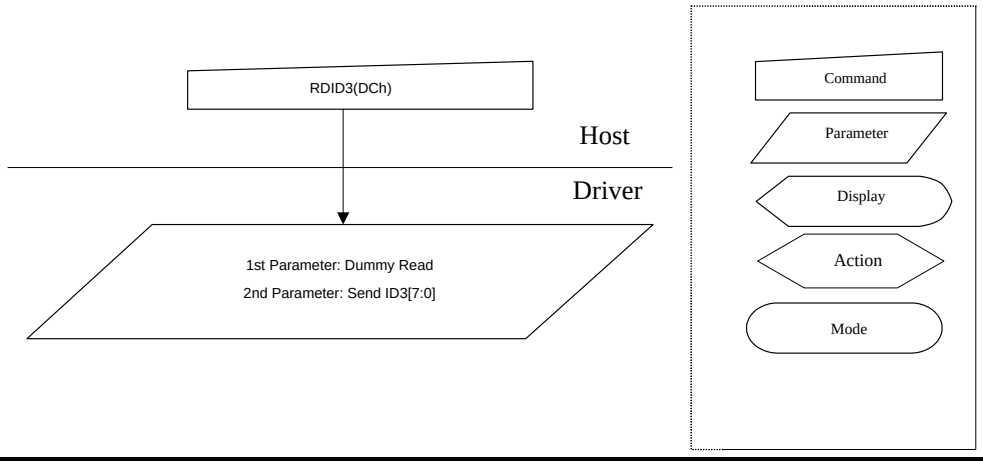
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before MTP program)	Default Value (After MTP program)
Power On Sequence	8'h04h	MTP value
SW Reset	8'h04h	MTP value
HW Reset	8'h04h	MTP value

Flow Chart



6.2.29. Read ID2 (DBh)

DCh	Read ID2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	1	0	0	DBh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID3 [7:0]								93h
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver version ID and the ID parameter range is from 80h to FFh. The ID3 can be programmed by MTP function. X = Don't care												
Restriction	None												

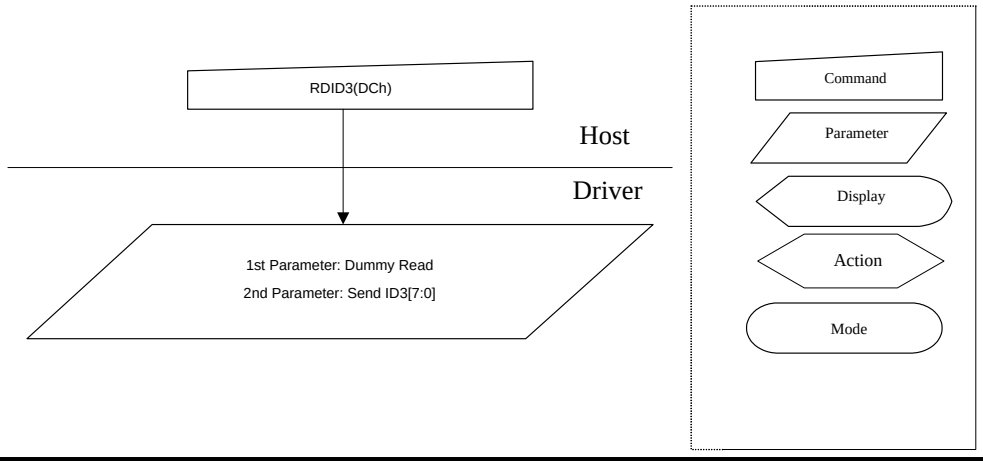
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before MTP program)	Default Value (After MTP program)
Power On Sequence	8'h04h	MTP value
SW Reset	8'h04h	MTP value
HW Reset	8'h04h	MTP value

Flow Chart



6.2.30. Read ID3 (DCh)

DCh	Read ID2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
1st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	XX	ID3 [7:0]								06
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver version ID and the ID parameter range is from 80h to FFh. The ID3 can be programmed by MTP function. X = Don't care												
Restriction	None												

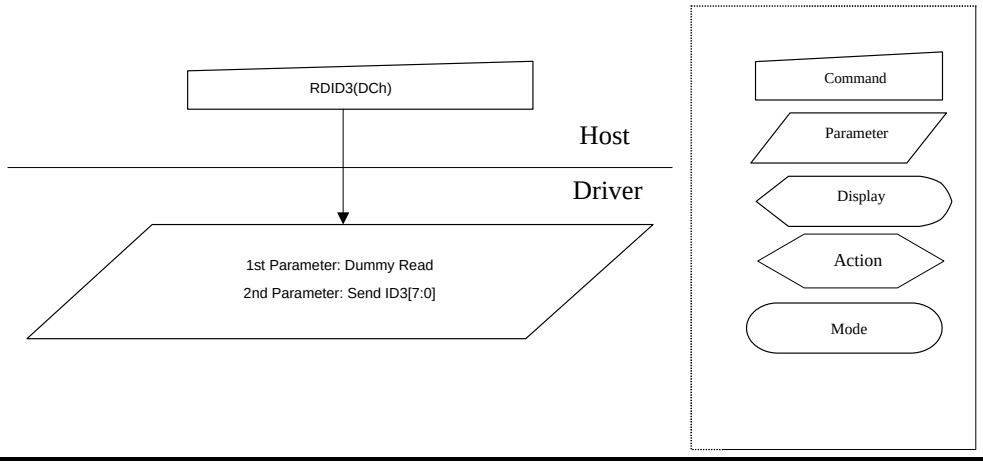
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before MTP program)	Default Value (After MTP program)
Power On Sequence	8'h06h	MTP value
SW Reset	8'h06h	MTP value
HW Reset	8'h06h	MTP value

Flow Chart



6.3. Description of Level 2 Command

6.3.1. RGB Interface Signal Control (B0h)

<table>
<tr><td>B0h</td><td colspan="13">RGB Interface Signal Control</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>B0h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>RCM[1]</td><td>RCM[0]</td><td>0</td><td>VSPL</td><td>HSPL</td><td>DPL</td><td>EPL</td><td>01</td></tr>
<tr><td>Description</td><td colspan="13">
Sets the operation status of the display interface. The setting becomes effective as soon as the command is received.
EPL: DE polarity (“0”= High enable for RGB interface, “1”= Low enable for RGB interface)
DPL: DOTCLK polarity set (“0”= data fetched at the rising time, “1”= data fetched at the falling time)
HSPL: HSYNC polarity (“0”= Low level sync clock, “1”= High level sync clock)
VSPL: VSYNC polarity (“0”= Low level sync clock, “1”= High level sync clock)
RCM [1:0]: RGB interface selection (refer to the RGB interface section).
<table>
<tr><th colspan="2">RCM[1:0]</th><th>RIM</th><th colspan="3">DPI[1:0]</th><th>RGB interface Mode</th><th>RGB Mode</th><th>Used Pins</th></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>18-bit RGB interface (262K colors)</td><td rowspan="3">DE Mode Valid data is determined by the DE signal</td><td>VSYNC,HSYNC,DE,DOTCLK,D[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>16-bit RGB interface (65K colors)</td><td>VSYNC,HSYNC,DE,DOTCLK,D[17:13] & D[11:1]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td colspan="3">-</td><td>6-bit RGB interface (262K colors)</td><td>VSYNC,HSYNC,DE,DOTCLK,D[5:0]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>18-bit RGB interface (262K colors)</td><td rowspan="3">SYNC Mode In SYNC mode, DE signal is ignored; blanking porch is determined by B5h command</td><td>VSYNC,HSYNC,DOTCLK,D[17:0]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>16-bit RGB interface (65K colors)</td><td>VSYNC,HSYNC,DOTCLK,D[17:13] & D[11:1]</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td colspan="3">-</td><td>6-bit RGB interface (262K colors)</td><td>VSYNC,HSYNC,DOTCLK,D[5:0]</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
</table>

Default

Status	Default Value				
	RCM[1:0]	VSPL	HSPL	DPL	EPL
Power On Sequence	2'b00	1'b0	1'b0	1'b0	1'b1
SW Reset	2'b00	1'b0	1'b0	1'b0	1'b1
HW Reset	2'b00	1'b0	1'b0	1'b0	1'b1

6.3.2. Blanking Porch Control (B5h)

B5h	Blanking Porch Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h
1st Parameter	1	1	↑	XX	0	VFP [6:0]							08
2nd Parameter	1	1	↑	XX	0	VBP [6:0]							02
3rd Parameter	1	1	↑	XX	0	0	0	X					XX
4th Parameter	1	1	↑	XX	0	0	0	HBP [4:0]					14

Description

Note: The Third parameter must write,but it is not valid.

VFP [6:0] / VBP [6:0]: The VFP [6:0] and VBP [6:0] bits specify the line number of vertical front and back porch period respectively.

VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch	VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch
0000000	Setting inhibited	1000000	64
0000001	Setting inhibited	1000001	65
0000010	2	1000010	66
0000011	3	1000011	67
0000100	4	1000100	68
0000101	5	1000101	69
: :	: :	: :	: :
0111101	61	1111101	125
0111110	62	1111110	109.5
0111111	63	1111111	127

Note: VFP + VBP ≦ 254 HSYNC signals

HBP [4:0]: HBP [4:0] bits specify the line number of horizontal back porch period respectively.

HBP [4:0]	Number of HSYNC of f ont/back porch
00000	Setting inhibited
00001	Setting inhibited
00010	2
00011	3
00100	4
00101	5
: :	: :
11101	30
11110	31
11111	32

<table>
<tr><td>Restriction</td><td>EXTC should be high to enable this command</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th colspan="3">Default Value</th></tr>
<tr><th>VFP [6:0]</th><th>VBP [6:0]</th><th>HBP [4:0]</th></tr>
<tr><td>Power On Sequence</td><td>7’h08</td><td>7’h02</td><td>5’h14</td></tr>
<tr><td>SW Reset</td><td>7’h08</td><td>7’h02</td><td>5’h14</td></tr>
<tr><td>HW Reset</td><td>7’h08</td><td>7’h02</td><td>5’h14</td></tr>
</table>
</td></tr>
</table>

6.3.3. Display Function Control (B6h)

B6h	Display Function Control												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	0	1	1	0	B6h
1st Parameter	1	1	↑	XX	X	X	X	X	X	X	X	X	XX
2nd Parameter	1	1	↑	XX	REV	GS	SS	SM	X				80
3rd Parameter	1	1	↑	XX	0	0	NL [5:0]						27

Description

note:the first parameter must write,but it is not valid.

SS: Select the shift direction of outputs from the source driver.

SS	Sourc Output Scan Direction
0	S1 → S720
1	S720 → S1

In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, and B dots to the source driver pins.

To assign R, G, B dots to the source driver pins from S1 to S720, set SS = 0.

To assign R, G, B dots to the source driver pins from S720 to S1, set SS = 1.

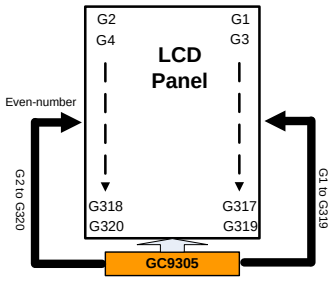
REV: Select whether the liquid crystal type is normally white type or normally black type.

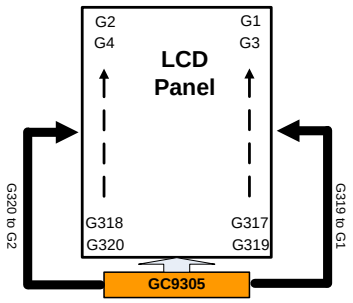
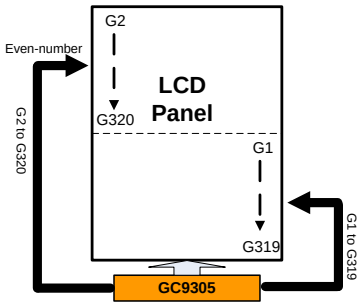
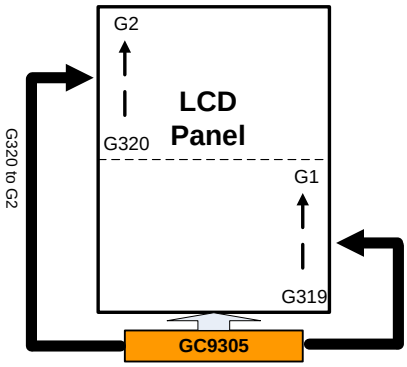
REV	Liquid crystal type
0	Normally black
1	Normally white

GS: Sets the direction of scan by the gate driver in the range determined by SCN [4:0] and NL [4:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.

GS	Gate Output Scan Direction
0	G1→G320
1	G320→G1

SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module

.SM	GS	Scan Direction	Gate Output Sequence
0	0		G1 G2 G3 G4 → G317 G318 G319 G320

0	1		G320 G319 G 318 G317 → G4 G3 G2 G1
1	0		G1 G3 →G317 G319 →G2 G4 → G318 G320
1	1		G320 G318 → G4 G2 → G319 G317 → G3 G1

NL [5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected

by the number of lines set by NL [5:0]. The number of lines must be the same or more than the number of lines necessary

for the size of the liquid crystal panel.

NL [5:0]						LCD Drive Line
0	0	0	0	0	0	Setting prohibited
0	0	0	0	0	1	16 lines
0	0	0	0	1	0	24 lines
0	0	0	0	1	1	32 lines
0	0	0	1	0	0	40 lines
0	0	0	1	0	1	48 lines
	0	0	1	1	0	56 lines
0	0	0	1	1	1	64 lines
0	0	1	0	0	0	72 lines

NL [5:0]						LCD Drive Line
0	1	0	1	0	1	176 lines
0	1	0	1	1	0	184 lines
0	1	0	1	1	1	192 lines
0	1	1	0	0	0	200 lines
0	1	1	0	0	1	208 lines
0	1	1	0	1	0	216 lines
0	1	1	0	1	1	224 lines
0	1	1	1	0	0	232 lines
0	1	1	1	0	1	240 lines

0	0	1	0	0	1	80 lines	0	1	1	1	1	0	248 lines
0	0	1	0	1	0	88 lines	0	1	1	1	1	1	256 lines
0	0	1	0	1	1	96 lines	1	0	0	0	0	0	264 lines
0	0	1	1	0	0	104 lines	1	0	0	0	0	1	272 lines
0	0	1	1	0	1	112 lines	1	0	0	0	1	0	280 lines
0	0	1	1	1	0	120 lines	1	0	0	0	1	1	288 lines
0	0	1	1	1	1	128 lines	1	0	0	1	0	0	296 lines
0	1	0	0	0	0	136 lines	1	0	0	1	0	1	304 lines
0	1	0	0	0	1	144 lines	1	0	0	1	1	0	312 lines
0	1	0	0	1	0	152 lines	1	0	0	1	1	1	320 lines
0	1	0	0	1	1	160 lines	Others						Setting prohibited
0	1	0	1	0	0	168 lines							

Restriction: EXTC should be high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value					
	-	REV	GS	SS	SM	NL[5:0]
Power On Sequence	-	1'b1	1'b0	1'b0	1'b0	6'h27
HW Reset	-	1'b1	1'b0	1'b0	1'b0	6'h27

6.3.4. Interface Control (F6h)

<table>
<tr><td>F6h</td><td colspan="13">Interface Control</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>F6h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>BGR_EOR</td><td>X</td><td>X</td><td>WE_MODE</td><td>01</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="2">MDT[1:0]</td><td>00</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>1</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="2">DM [1:0]</td><td>RM</td><td>RIM</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">
MDT [1:0]: Select the method of display data transferring.
WEMODE: Memory write control
WEMODE=0: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.
WEMODE=1: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.
DM [1:0]: Select the display operation mode.
<table>
<tr><th>DM[1]</th><th>DM[0]</th><th>Display Operation Mode</th></tr>
<tr><td>0</td><td>0</td><td>Internal clock operation</td></tr>
<tr><td>0</td><td>1</td><td>RGB Interface Mode</td></tr>
<tr><td>1</td><td>0</td><td>VSYNC interface Mode</td></tr>
<tr><td>1</td><td>1</td><td>Setting disabled</td></tr>
</table>
RM: Select the interface to access the GRAM.
Set RM to “1” when writing display data by the RGB interface.
<table>
<tr><th>RM</th><th>Interface for RAM Access</th></tr>
<tr><td>0</td><td>System interface/VSYNC interface</td></tr>
<tr><td>1</td><td>RGB interface</td></tr>
</table>
RIM: Specify the RGB interface mode when the RGB interface is used. These bits should be set before display operation through the RGB interface and should not be set during operation.
<table>
<tr><th>RIM</th><th>COLMOD [6:4]</th><th>RGB Interface Mode</th></tr>
<tr><td rowspan="2">0</td><td>110 (262K color)</td><td>18- bit RGB interface (1 transfer/pixel)</td></tr>
<tr><td>101 (65K color)</td><td>16- bit RGB interface (1 transfer/pixel)</td></tr>
<tr><td>1</td><td>(262K color)</td><td>6- bit RGB interface (3 transfer/pixel)</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="13">EXTC should be high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
</table>

Default

Status	Default Value					
	BGR_EOR	WE MODE	MDT[1:0]	DM [1:0]	RM	RIM
Power On Sequence	1'b0	1'b1	2'b00	2'b00	1'b0	1'b0
SW Reset	1'b0	1'b1	2'b00	2'b00	1'b0	1'b0
HW Reset	1'b0	1'b1	2'b00	2'b00	1'b0	1'b0

6.4. Description of Level 3 Command

6.4.1. Frame Rate (E8h)

<table>
<tr><td>E8h</td><td colspan="13">Frame Rate</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>E8h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="4">DINV[3:0]</td><td colspan="4">RTN1[3:0]</td><td>00</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="8">RTN2[7:0]</td><td>70</td></tr>
<tr><td>Description</td><td colspan="13">
DINV[3:0] : Set display inversion mode
<table>
<tr><th>DINV[3:0]</th><th>Inversion</th></tr>
<tr><td>0</td><td>column inversion</td></tr>
<tr><td>1</td><td>1 dot inversion</td></tr>
<tr><td>2</td><td>2 dot inversion</td></tr>
<tr><td>3</td><td>4 dot inversion</td></tr>
<tr><td>4</td><td>8 dot inversion</td></tr>
</table>
RTN1[3:0]/RTN2[7:0] :Set the frame rate when the internal resistor is used for oscillator circuit.
Frame Rate = 47.62KHz/(136*(RTN1+4)+RTN2)）
note: set rtn1 =1
<table>
<tr><th>rtn2[7:0]</th><th>TE(Hz)</th><th>rtn2[7:0]</th><th>TE(Hz)</th><th>rtn2[7:0]</th><th>TE(Hz)</th><th>rtn2[7:0]</th><th>TE Hz)</th></tr>
<tr><td>8'd00</td><td>70.0</td><td>8'd10</td><td>68.4</td><td>8'd20</td><td>66.9</td><td>8'd30</td><td>65.4</td></tr>
<tr><td>8'd01</td><td>69.9</td><td>8'd11</td><td>68.3</td><td>8'd21</td><td>66.8</td><td>8'd31</td><td>65.3</td></tr>
<tr><td>8'd02</td><td>69.8</td><td>8'd12</td><td>68.2</td><td>8'd22</td><td>66.7</td><td>8'd32</td><td>65.2</td></tr>
<tr><td>8'd03</td><td>69.7</td><td>8'd13</td><td>68.1</td><td>8'd23</td><td>66.6</td><td>8'd33</td><td>65.1</td></tr>
<tr><td>8'd04</td><td>69.6</td><td>8'd14</td><td>68.0</td><td>8'd24</td><td>66.5</td><td>8'd34</td><td>65.1</td></tr>
<tr><td>8'd05</td><td>69.5</td><td>8'd15</td><td>67.9</td><td>8'd25</td><td>66.4</td><td>8'd35</td><td>65.0</td></tr>
<tr><td>8'd06</td><td>69.4</td><td>8'd16</td><td>67.8</td><td>8'd26</td><td>66.3</td><td>8'd36</td><td>64.9</td></tr>
<tr><td>8'd07</td><td>69.3</td><td>8'd17</td><td>67.7</td><td>8'd27</td><td>66.2</td><td>8'd37</td><td>64.8</td></tr>
<tr><td>8'd08</td><td>69.2</td><td>8'd18</td><td>67.6</td><td>8'd28</td><td>66.1</td><td>8'd38</td><td>64.7</td></tr>
<tr><td>8'd09</td><td>69.1</td><td>8'd19</td><td>67.5</td><td>8'd29</td><td>66.0</td><td>8'd39</td><td>64.6</td></tr>
<tr><td>8'd0A</td><td>69.0</td><td>8'd1A</td><td>67.4</td><td>8'd2A</td><td>66.0</td><td>8'd3A</td><td>64.5</td></tr>
<tr><td>8'd0B</td><td>68.9</td><td>8'd1B</td><td>67.4</td><td>8'd2B</td><td>65.9</td><td>8'd3B</td><td>64.4</td></tr>
<tr><td>8'd0C</td><td>68.8</td><td>8'd1C</td><td>67.3</td><td>8'd2C</td><td>65.8</td><td>8'd3C</td><td>64.4</td></tr>
<tr><td>8'd0D</td><td>68.7</td><td>8'd1D</td><td>67.2</td><td>8'd2D</td><td>65.7</td><td>8'd3D</td><td>64.3</td></tr>
<tr><td>8'd0E</td><td>68.6</td><td>8'd1E</td><td>67.1</td><td>8'd2E</td><td>65.6</td><td>8'd3E</td><td>64.2</td></tr>
<tr><td>8'd0F</td><td>68.5</td><td>8'd1F</td><td>67.0</td><td>8'd2F</td><td>65.5</td><td>8'd3F</td><td>64.1</td></tr>
<tr><td>rtn2[7:0]</td><td>TE(Hz)</td><td>rtn2[7:0]</td><td>TE(Hz)</td><td>rtn2[7:0]</td><td>TE(Hz)</td><td>rtn2[7:0]</td><td>TE(Hz)</td></tr>
<tr><td>8'd40</td><td>64.0</td><td>8'd50</td><td>62.7</td><td>8'd60</td><td>61.4</td><td>8'd70</td><td>60.1</td></tr>
</table>
</td></tr>
</table>

	8'd41	63.9	8'd51	62.6	8'd61	61.3	8'd71	60.0
	8'd42	63.8	8'd52	62.5	8'd62	61.2	8'd72	60.0
	8'd44	63.7	8'd55	62.2	8'd66	60.9	8'd77	59.6
	8'd44	63.7	8'd54	62.3	8'd64	61.1	8'd74	59.8
	8'd45	63.6	8'd55	62.2	8'd65	61.0	8'd75	59.7
	8'd46	63.5	8'd56	62.2	8'd66	60.9	8'd76	59.7
	8'd47	63.4	8'd57	62.1	8'd67	60.8	8'd77	59.6
	8'd48	63.3	8'd58	62.0	8'd68	60.7	8'd78	59.5
	8'd49	63.2	8'd59	61.9	8'd69	60.7	8'd79	59.4
	8'd4A	63.2	8'd5A	61.8	8'd6A	60.6	8'd7A	59.4
	8'd4B	63.1	8'd5B	61.8	8'd6B	60.5	8'd7B	59.3
	8'd4C	63.0	8'd5C	61.7	8'd6C	60.4	8'd7C	59.2
	8'd4D	62.9	8'd5D	61.6	8'd6D	60.4	8'd7D	59.2
	8'd4E	62.8	8'd5E	61.5	8'd6E	60.3	8'd7E	59.1
	8'd4F	62.7	8'd5F	61.4	8'd6F	60.2	8'd7F	59.0
	rtn2[7:0]	TE(Hz)	rtn2[7:0]	TE(Hz)	rtn2[7:0]	TE(Hz)	rtn2[7:0]	TE(Hz)
	8'd80	58.9	8'd84	58.6				
	8'd81	58.9	8'd85	58.6				
	8'd82	58.8	8'd86	58.5				
	8'd83	58.4	8'd87	58.4				

note: set rtn2=0x40

rtn1[3:0]	TE(Hz)	rtn1[3:0]	TE(Hz)	rtn1[3:0]	TE(Hz)	rtn1[3:0]	TE(Hz)
8'd00	78.3	8'd04	41.3	8'd08	28.1	8'd0C	21.3
8'd01	64.0	8'd05	37.0	8'd09	26.0	8'd0D	20.0
8'd02	54.1	8'd06	33.4	8'd0A	24.2	8'd0E	19.0
8'd03	46.9	8'd07	30.5	8'd0B	22.6	8'd0F	18.0

Restriction	Inter_command should be set high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	DINV[3:0]	RTN1[3:0]	RTN2[7:0]
Power On Sequence	4'h1	4'h1	8'h40
SW Reset	4'h1	4'h1	8'h40
HW Reset	4'h1	4'h1	8'h40

6.4.2. SPI 2DATA control(E9h)

<table>
<tr><td>E9h</td><td colspan="13">SPI 2DATA control</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>E9h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>2data_en</td><td colspan="3">2data_mdt[2:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="13">2DATA_EN: Set 2_data_line mode in 3-wire/4-wire SPI.
2DATA_MDT[2:0] Set pixel data format in 2_data_line mode.

<table><tr><th>2DATA_MDT[2:0]</th><th>Data Format</th></tr><tr><td>000</td><td>65K color 1pi le/transition</td></tr><tr><td>001</td><td>262K color 1pixle/transition</td></tr><tr><td>010</td><td>262K color 2/3pixle/transition</td></tr><tr><td>100</td><td>4M color 1pixle/transition</td></tr><tr><td>110</td><td>4M color 2/3pixle/transition</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><th>2DATA_EN</th><th>2DATA_MDT[2:0]</th></tr><tr><td>Power On Sequence</td><td>1’b0</td><td>3’b000</td></tr><tr><td>SW Reset</td><td>1’b0</td><td>3’b000</td></tr><tr><td>HW Reset</td><td>1’b0</td><td>3’b000</td></tr></table></td></tr>
</table>

6.4.3. Power Control 1 (A3h)

<table>
<tr><td>A3h</td><td colspan="12">Power Control 1</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>A3h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>1</td><td>XX</td><td>X</td><td>X</td><td>X</td><td>X</td><td>0</td><td>0</td><td>VCIRE</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="12">VCIRE: Select the external reference voltage Vci or internal reference voltage VCIR.
<table>
<tr><td>VCIRE=0</td><td>Internal reference voltage 2.5V (default)</td></tr>
<tr><td>VCIRE =1</td><td>External reference voltag Vci</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">Inter_command should be set high to enable this command</td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><td rowspan="2">Status</td><td>Default Value</td></tr>
<tr><td>VCIRE</td></tr>
<tr><td>Power On Sequence</td><td>1’b0</td></tr>
<tr><td>SW Reset</td><td>1’b0</td></tr>
<tr><td>HW Reset</td><td>1’b0</td></tr>
</table></td></tr>
</table>

6.4.4. Power Control 2 (A6h)

A6h	Power Control 2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	0	0	1	1	0	A6h
1st Parameter	1	1	↑	XX	X	X	Vreg1_vap[5:0]						2a

Description

Set the voltage level value to output the VREG1A OUT level, which is a reference level for the grayscale voltage level.

vap[5:0]	vreg1a(V)	vap[5:0]	Vreg1a(V)	Vap[5:0]	Vreg1a(V)
6'h00	3.900	6'h16	5.000	6'h2c	6.100
6'h01	3.950	6'h17	5.050	6'h2d	6.150
6'h02	4.000	6'h18	5.100	6'h2e	6.200
6'h03	4.050	6'h19	5.150	6'h2f	6.250
6'h04	4.100	6'h1a	5.200	6'h30	6.300
6'h05	4.150	6'h1b	5.250	6'h31	6.350
6'h06	4.200	6'h1c	5.300	6'h32	6.400
6'h07	4.250	6'h1d	5.350	6'h33	6.450
6'h08	4.300	6'h1e	5.400	6'h34	6.500
6'h09	4.350	6'h1f	5.450	6'h35	6.550
6'h0a	4.400	6'h20	5.500	6'h36	6.600
6'h0b	4.450	6'h21	5.550	6'h37	6.650
6'h0c	4.500	6'h22	5.600	6'h38	6.700
6'h0d	4.550	6'h23	5.650	6'h39	6.750
6'h0e	4.600	6'h24	5.700	6'h3a	6.800
6'h0f	4.650	6'h25	5.750	6'h3b	6.850
6'h10	4.700	6'h26	5.800	6'h3c	6.900
6'h11	4.750	6'h27	5.850	6'h3d	6.950
6'h12	4.800	6'h28	5.900	6'h3e	7.000
6'h13	4.850	6'h29	5.950	6'h3f	7.050
6'h14	4.900	6'h2a	6.000		
6'h15	4.950	6'h2b	6.050		

Restriction: Inter_command should be set high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
	vap[5:0]
Power On Sequence	6'h2a
SW Reset	6'h2a
HW Reset	6'h2a

6.4.5. Power Control 3 (A7h)

A7h	Power Control 3												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	0	0	1	1	1	A7h
1st Parameter	1	1	↑	XX	X	X	Vreg1_vbp[5:0]						25

Description

Set the voltage level value to output the VREG1B OUT level, which is a reference level for the grayscale voltage level

vbp[5:0]	vreg1b(V)	vbp[5:0]	Vreg1b(V)	Vbp[5:0]	Vreg1b(V)
6'h00	0.400	6'h16	1.200	6'h2c	1.750
6'h01	0.450	6'h17	1.220	6'h2d	1.800
6'h02	0.500	6'h18	1.240	6'h2e	1.850
6'h03	0.550	6'h19	1.260	6'h2f	1.900
6'h04	0.600	6'h1a	1.280	6'h30	1.950
6'h05	0.650	6'h1b	1.300	6'h31	2.000
6'h06	0.700	6'h1c	1.320	6'h32	2.050
6'h07	0.750	6'h1d	1.340	6'h33	2.100
6'h08	0.800	6'h1e	1.360	6'h34	2.150
6'h09	0.850	6'h1f	1.380	6'h35	2.200
6'h0a	0.900	6'h20	1.400	6'h36	2.250
6'h0b	0.950	6'h21	1.420	6'h37	2.300
6'h0c	1.000	6'h22	1.440	6'h38	2.350
6'h0d	1.020	6'h23	1.460	6'h39	2.400
6'h0e	1.040	6'h24	1.480	6'h3a	2.450
6'h0f	1.060	6'h25	1.500	6'h3b	2.500
6'h10	1.080	6'h26	1.520	6'h3c	1.750
6'h11	1.100	6'h27	1.540	6'h3d	1.800
6'h12	1.120	6'h28	1.560	6'h3e	1.850
6'h13	1.140	6'h29	1.580	6'h3f	1.900
6'h14	1.160	6'h2a	1.600		
6'h15	1.180	6'h2b	1.620		

Restriction: Inter_command should be set high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

<table>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>vbp[5:0]</th></tr>
<tr><td>Power On Sequence</td><td>6’h25</td></tr>
<tr><td>SW Reset</td><td>6’h25</td></tr>
<tr><td>HW Reset</td><td>6’h25</td></tr>
</table>
</td></tr>
</table>

6.4.6. Power Control 4 (A8h)

<table>
<tr><td>A8h</td><td colspan="13">Power Control 4</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>A8h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td>X</td><td colspan="5">Vreg2_van[5:0]</td><td>15</td></tr>
<tr><td>Description</td><td colspan="13">Set the voltage level value to output the VREG2A OUT level, which is a reference level for the grayscale voltage level.
<table>
<tr><th>van[5:0]</th><th>Vreg2a</th><th>van[5:0]</th><th>Vreg2a</th><th>Van[5:0]</th><th>Vreg2a</th></tr>
<tr><td>6' 00</td><td>-1.950</td><td>6'h16</td><td>-3.050</td><td>6'h2c</td><td>-4.150</td></tr>
<tr><td>6'h01</td><td>-2.000</td><td>6'h17</td><td>-3.100</td><td>6'h2d</td><td>-4.200</td></tr>
<tr><td>6'h02</td><td>-2.050</td><td>6'h18</td><td>-3.150</td><td>6'h2e</td><td>-4.250</td></tr>
<tr><td>6'h03</td><td>-2.100</td><td>6'h19</td><td>-3.200</td><td>6'h2f</td><td>-4.300</td></tr>
<tr><td>6'h04</td><td>-2.150</td><td>6'h1a</td><td>-3.250</td><td>6'h30</td><td>-4.350</td></tr>
<tr><td>6'h05</td><td>-2.200</td><td>6'h1b</td><td>-3.300</td><td>6'h31</td><td>-4.400</td></tr>
<tr><td>6'h06</td><td>-2.250</td><td>6'h1c</td><td>-3.350</td><td>6'h32</td><td>-4.450</td></tr>
<tr><td>6'h07</td><td>-2.300</td><td>6'h1d</td><td>-3.400</td><td>6'h33</td><td>-4.500</td></tr>
<tr><td>6'h08</td><td>-2.350</td><td>6'h1e</td><td>-3.450</td><td>6'h34</td><td>-4.550</td></tr>
<tr><td>6'h09</td><td>-2.400</td><td>6'h1f</td><td>-3.500</td><td>6'h35</td><td>-4.600</td></tr>
<tr><td>6'h0a</td><td>-2.450</td><td>6'h20</td><td>-3.550</td><td>6'h36</td><td>-4.650</td></tr>
<tr><td>6'h0b</td><td>-2.500</td><td>6'h21</td><td>-3.600</td><td>6'h37</td><td>-4.700</td></tr>
<tr><td>6'h0c</td><td>-2.550</td><td>6'h22</td><td>-3.650</td><td>6'h38</td><td>-4.750</td></tr>
<tr><td>6'h0d</td><td>-2.600</td><td>6'h23</td><td>-3.700</td><td>6'h39</td><td>-4.800</td></tr>
<tr><td>6'h0e</td><td>-2.650</td><td>6'h24</td><td>-3.750</td><td>6'h3a</td><td>-4.850</td></tr>
<tr><td>6'h0f</td><td>-2.700</td><td>6'h25</td><td>-3.800</td><td>6'h3b</td><td>-4.900</td></tr>
<tr><td>6'h10</td><td>-2.750</td><td>6'h26</td><td>-3.850</td><td>6'h3c</td><td>-4.950</td></tr>
<tr><td>6'h11</td><td>-2.800</td><td>6'h27</td><td>-3.900</td><td>6'h3d</td><td>-5.000</td></tr>
<tr><td>6'h12</td><td>-2.850</td><td>6'h28</td><td>-3.950</td><td>6'h3e</td><td>-5.050</td></tr>
<tr><td>6'h13</td><td>-2.900</td><td>6'h29</td><td>-4.000</td><td>6'h3f</td><td>-5.100</td></tr>
<tr><td>6'h14</td><td>-2.950</td><td>6'h2a</td><td>-4.050</td><td></td><td></td></tr>
<tr><td>6'h15</td><td>-3.000</td><td>6'h2b</td><td>-4.100</td><td></td><td></td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
</table>

<table>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>van[5:0]</th></tr>
<tr><td>Power On Sequence</td><td>6’h15</td></tr>
<tr><td>SW Reset</td><td>6’h15</td></tr>
<tr><td>HW Reset</td><td>6’h15</td></tr>
</table>
</td></tr>
</table>

6.4.7. Power Control 5 (A9h)

<table>
<tr><td>A9h</td><td colspan="13">Power Control 5</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>A9h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>X</td><td>X</td><td colspan="6">Vreg2_vbp[5:0]</td><td>25</td></tr>
<tr><td>Description</td><td colspan="13">Set the voltage level value to output the VREG2B OUT level, which is a reference level for the grayscale voltage level.
<table>
<tr><th>vbn[5:0]</th><th>Vreg2b(V)</th><th>vbn[5:0]</th><th>Vreg2b(V)</th><th>Vbn[5:0]</th><th>Vreg2b(V)</th></tr>
<tr><td>6'h00</td><td>0.400</td><td>6'h16</td><td>1.200</td><td>6'h2c</td><td>1.640</td></tr>
<tr><td>6'h01</td><td>0.450</td><td>6'h17</td><td>1.220</td><td>6'h2d</td><td>1.660</td></tr>
<tr><td>6'h02</td><td>0.500</td><td>6'h18</td><td>1.240</td><td>6'h2e</td><td>1.680</td></tr>
<tr><td>6'h03</td><td>0.550</td><td>6'h19</td><td>1.260</td><td>6'h2f</td><td>1.700</td></tr>
<tr><td>6'h04</td><td>0.600</td><td>6'h1a</td><td>1.280</td><td>6'h30</td><td>1.750</td></tr>
<tr><td>6'h05</td><td>0.650</td><td>6'h1b</td><td>1.300</td><td>6'h31</td><td>1.800</td></tr>
<tr><td>6'h06</td><td>0.700</td><td>6'h1c</td><td>1.320</td><td>6'h32</td><td>1.850</td></tr>
<tr><td>6'h07</td><td>0.750</td><td>6'h1d</td><td>1.340</td><td>6'h33</td><td>1.900</td></tr>
<tr><td>6'h08</td><td>0.800</td><td>6'h1e</td><td>1.360</td><td>6'h34</td><td>1.950</td></tr>
<tr><td>6'h09</td><td>0.850</td><td>6'h1f</td><td>1.380</td><td>6'h35</td><td>2.000</td></tr>
<tr><td>6'h0a</td><td>0.900</td><td>6'h20</td><td>1.400</td><td>6'h36</td><td>2.050</td></tr>
<tr><td>6'h0b</td><td>0.950</td><td>6'h21</td><td>1.420</td><td>6'h37</td><td>2.100</td></tr>
<tr><td>6'h0c</td><td>1.000</td><td>6'h22</td><td>1.440</td><td>6'h38</td><td>2.150</td></tr>
<tr><td>6'h0d</td><td>1.020</td><td>6'h23</td><td>1.460</td><td>6'h39</td><td>2.200</td></tr>
<tr><td>6'h0e</td><td>1.040</td><td>6'h24</td><td>1.480</td><td>6'h3a</td><td>2.250</td></tr>
<tr><td>6'h0f</td><td>1.060</td><td>6'h25</td><td>1.500</td><td>6'h3b</td><td>2.300</td></tr>
<tr><td>6'h10</td><td>1.080</td><td>6'h26</td><td>1.520</td><td>6'h3c</td><td>2.350</td></tr>
<tr><td>6'h11</td><td>1.100</td><td>6'h27</td><td>1.540</td><td>6'h3d</td><td>2.400</td></tr>
<tr><td>6'h12</td><td>1.120</td><td>6'h28</td><td>1.560</td><td>6'h3e</td><td>2.450</td></tr>
<tr><td>6'h13</td><td>1.140</td><td>6'h29</td><td>1.580</td><td>6'h3f</td><td>2.500</td></tr>
<tr><td>6'h14</td><td>1.160</td><td>6'h2a</td><td>1.600</td><td></td><td></td></tr>
<tr><td>6'h15</td><td>1.180</td><td>6'h2b</td><td>1.620</td><td></td><td></td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
</table>

Default

Status	Default Value
	vbn[5:0]
Power On Sequence	6'h25
SW Reset	6'h25
HW Reset	6'h25

6.4.8. Power Control 6 (ECh)

<table>
<tr><td>ECh</td><td colspan="13">Power Control 6</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>ECh</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="3">avdd_clk_ad[2:0]</td><td></td><td colspan="3">avee_clk_ad[2:0]</td><td>33</td></tr>
<tr><td>2st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="3">chp_sou_clk_ad[2:0]</td><td></td><td colspan="3">vcl_clk_ad[2:0]</td><td>22</td></tr>
<tr><td>3st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td colspan="4">vgh_clk_ad[3:0]</td><td colspan="4">vgl_clk_ad[3:0]</td><td>88</td></tr>
<tr><td>Description</td><td colspan="13">Set the ChargePump frequence output(Fosc is equal to RC oscillator)
<table>
<tr><th>chp_sou_clk_ad[2:0]</th><th>sou_clk (Mhz)</th><th>vcl_clk_ad[2:0]</th><th>vcl_clk(Mhz)</th><th>avee_clk_ad[2:0]</th><th>avee_clk(Mhz)</th><th>avdd_clk_ad[2:0]</th><th>avdd_clk(Mhz)</th></tr>
<tr><td>3'h00</td><td>Fosc*(3/4)</td><td>3'h00</td><td>Fosc*(3/4)</td><td>3'h00</td><td>Fosc*(2/4)</td><td>3'h00</td><td>Fosc*(2/4)</td></tr>
<tr><td>3'h01</td><td>Fosc*(4/4)</td><td>3'h01</td><td>Fosc*(4/4)</td><td>3'h01</td><td>Fosc*(3/4)</td><td>3'h01</td><td>Fosc*(3/4)</td></tr>
<tr><td>3'h02</td><td>Fosc*(5/4)</td><td>3'h02</td><td>Fosc*(5/4)</td><td>3'h02</td><td>Fosc*(4/4)</td><td>3'h02</td><td>Fosc*(4/4)</td></tr>
<tr><td>3'h03</td><td>Fosc*(6/4)</td><td>3'h03</td><td>Fosc*(6/4)</td><td>3'h03</td><td>Fosc*(5/4)</td><td>3'h03</td><td>Fosc*(5/4)</td></tr>
<tr><td>3'h04</td><td>Fosc*(7/4)</td><td>3'h04</td><td>Fosc*(7/4)</td><td>3'h04</td><td>Fosc*(6/4)</td><td>3'h04</td><td>Fosc*(6/4)</td></tr>
<tr><td>3'h05</td><td>Fosc*(8/4)</td><td>3'h05</td><td>Fosc*(8/4)</td><td>3'h05</td><td>Fosc*(7/4)</td><td>3'h05</td><td>Fosc*(7/4)</td></tr>
<tr><td>3'h06</td><td>Fosc*(9/4)</td><td>3'h06</td><td>Fosc*(9/4)</td><td>3'h06</td><td>Fosc*(8/4)</td><td>3'h06</td><td>Fosc*(8/4)</td></tr>
<tr><td>3'h07</td><td>Fosc*(10/4)</td><td>3'h07</td><td>Fosc*(10/4)</td><td>3'h07</td><td>Fosc*(9/4)</td><td>3'h07</td><td>Fosc*(9/4)</td></tr>
<tr><th>vgh_clk_ad[3:0]</th><th>vgh_clk (Mhz)</th><th>vgh_clk_ad[3:0]</th><th>vgh_clk (Mhz)</th><th>vgl_clk_ad[3:0]</th><th>vgl_clk (Mhz)</th><th>vgl_clk_ad[3:0]</th><th>vgl_clk(Mhz)</th></tr>
<tr><td>4'h00</td><td>Fosc*(5/4)</td><td>4'h08</td><td>Fosc*(20/4)</td><td>4'h00</td><td>Fosc*(5/4)</td><td>4'h08</td><td>Fosc*(20/4)</td></tr>
<tr><td>4'h01</td><td>Fosc*(6/4)</td><td>4'h09</td><td>Fosc*(22/4)</td><td>4'h01</td><td>Fosc*(6/4)</td><td>4'h09</td><td>Fosc*(22/4)</td></tr>
<tr><td>4'h02</td><td>Fosc*(8/4)</td><td>4'h0a</td><td>Fosc*(24/4)</td><td>4'h02</td><td>Fosc*(8/4)</td><td>4'h0a</td><td>Fosc*(24/4)</td></tr>
<tr><td>4'h03</td><td>Fosc*(10/4)</td><td>4'h0b</td><td>Fosc*(26/4)</td><td>4'h03</td><td>Fosc*(10/4)</td><td>4'h0b</td><td>Fosc*(26/4)</td></tr>
<tr><td>4'h04</td><td>Fosc*(12/4)</td><td>4'h0c</td><td>Fosc*(28/4)</td><td>4'h04</td><td>Fosc*(12/4)</td><td>4'h0c</td><td>Fosc*(28/4)</td></tr>
<tr><td>4'h05</td><td>Fosc*(14/4)</td><td>4'h0d</td><td>Fosc*(30/4)</td><td>4'h05</td><td>Fosc*(14/4)</td><td>4'h0d</td><td>Fosc*(30/4)</td></tr>
<tr><td>4'h06</td><td>Fosc*(16/4)</td><td>4'h0e</td><td>Fosc*(40/4)</td><td>4'h06</td><td>Fosc*(16/4)</td><td>4'h0e</td><td>Fosc*(40/4)</td></tr>
<tr><td>4'h07</td><td>Fosc*(18/4)</td><td>4'h0f</td><td>Fosc*(50/4)</td><td>4'h07</td><td>Fosc*(18/4)</td><td>4'h0f</td><td>Fosc*(50/4)</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
</table>

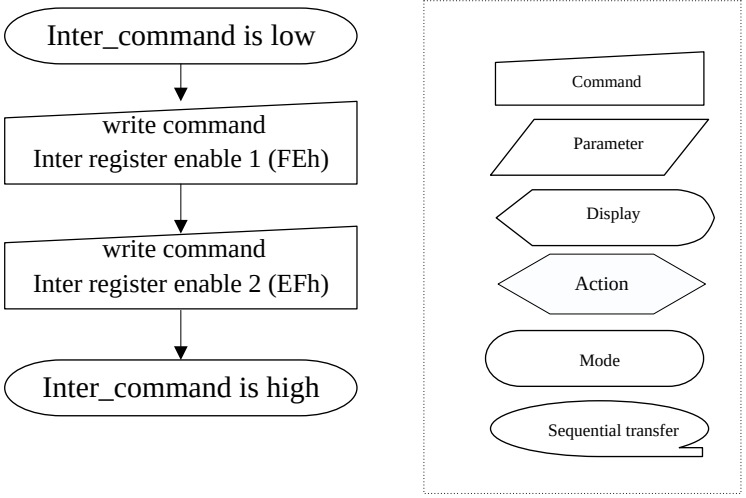
Default

Status	Default Value					
	avdd_clk_ad[2:0]	avee_clk_ad[2:0]	chp_sou_clk_ad[2:0]	vcl_clk_ad[2:0]	vgh_clk_ad[3:0]	vgl_clk_ad[3:0]
Power On Sequence	3'h3	3'h3	3'h2	3'h2	4'h8	4'h8
SW Reset	3'h3	3'h3	3'h2	3'h2	4'h8	4'h8
HW Reset	3'h3	3'h3	3'h2	3'h2	4'h8	4'h8

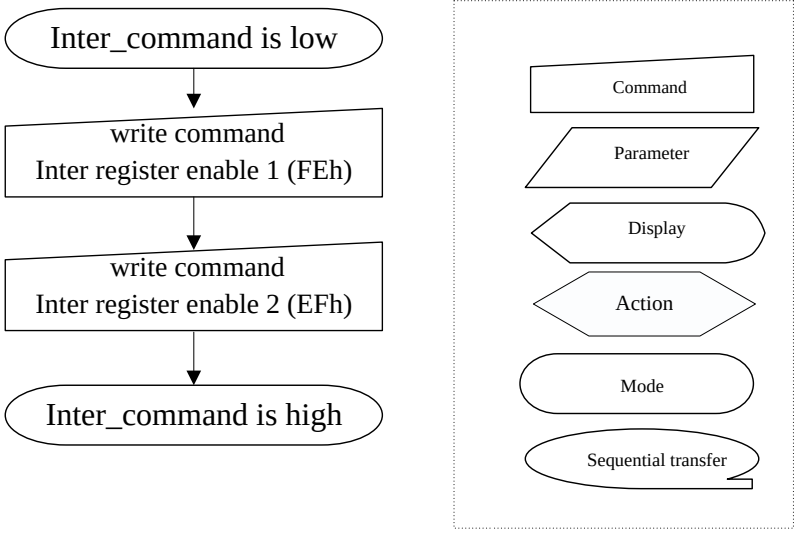
6.4.9. Power Control 7(A4h)

<table>
<tr><td>A4h</td><td colspan="13">Power Control 7</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>A4h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>0</td><td>1</td><td>0</td><td>0</td><td colspan="4">vdd_ad[3:0]</td><td>44</td></tr>
<tr><td>Description</td><td colspan="13">vdd_ad: Set the voltage level value to output the VCORE level,
<table>
<tr><th>vdd_ad[3:0]</th><th>VCORE(V)</th><th>vdd_ad[3:0]</th><th>VCORE(V)</th></tr>
<tr><td>4'h00</td><td>1.483</td><td>4'h08</td><td>1.994</td></tr>
<tr><td>4'h01</td><td>1.545</td><td>4'h09</td><td>2.109</td></tr>
<tr><td>4'h02</td><td>1.590</td><td>4'h0a</td><td>2.193</td></tr>
<tr><td>4'h03</td><td>1.638</td><td>4'h0b</td><td>2.286</td></tr>
<tr><td>4'h04</td><td>1.714</td><td>4'h0c</td><td>2.385</td></tr>
<tr><td>4'h05</td><td>1.279</td><td>4'h0d</td><td>1.713</td></tr>
<tr><td>4'h06</td><td>1.859</td><td>4'h0e</td><td>1.713</td></tr>
<tr><td>4'h07</td><td>1.925</td><td>4'h0f</td><td>1.713</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13">
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>vdd_ad[3:0]</th></tr>
<tr><td>Power On Sequence</td><td>4’b4</td></tr>
<tr><td>SW Reset</td><td>4’b4</td></tr>
<tr><td>HW Reset</td><td>4’b4</td></tr>
</table></td></tr>
</table>

6.4.10. Inter Register Enable1(FEh)

<table>
<tr><td>FEh</td><td colspan="13">Inter register enable 1</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>FEh</td></tr>
<tr><td>Parameter</td><td colspan="13">No Parameter</td></tr>
<tr><td>Description</td><td colspan="13">This command is used for Inter_command controlling.
To set Inter_command high ,you should write Inter register enable 1 (FEh) and Inter register enable 2 (EFh) continuously.
Once Inter_command is set high, only hardware or software reset can turn it to low.
 
</td></tr>
<tr><td>Restriction</td><td colspan="13"></td></tr>
<tr><td>Register Availability</td><td colspan="13"><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="13"></td></tr>
</table>

6.4.11. Inter Register Enable2(EFh)

EFh	Inter register enable 2												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	0	1	1	1	1	EFh
Parameter	No Parameter												
Description	This command is used for Inter_command controlling. To set Inter_command high ,you should write Inter register enable 1 (FEh) and Inter register enable 2 (EFh) continuously. Once Inter_command is set high, only hardware or software reset can turn it to low. 												
Restriction													
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default	

6.4.12. SET_GAMMA1 (F0h)

<table>
<tr><td>F0h</td><td colspan="13">SET_GAMMA1</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D17-8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>XX</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>F0h</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td></td><td></td><td></td><td></td><td colspan="2">dig2gam_dig2j0_n[1:0]</td><td>02</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td></td><td></td><td></td><td></td><td colspan="2">dig2gam_dig2j1_n[1:0]</td><td>00</td></tr>
<tr><td>3st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td></td><td></td><td colspan="5">dig2gam_vr0_n[3:0]</td><td>00</td></tr>
<tr><td>4nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td colspan="6">dig2gam_vr1_n[5:0]</td><td>00</td></tr>
<tr><td>5st Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td colspan="6">dig2gam_vr2_n[5:0]</td><td>03</td></tr>
<tr><td>6nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td></td><td></td><td></td><td colspan="6">dig2gam_vr4_n[4:0]</td><td>08</td></tr>
<tr><td>Description</td><td colspan="13">dig2gam_dig2j0_n[1:0]: γ gradient adjustment register for negative polarity
dig2gam_dig2j1_n[1:0]: γ gradient adjustment register for negative polarity
dig2gam_vr0_n[3:0]: γ gradient adjustment register for negative polarity
dig2gam_vr1_n[5:0]: γ gradient adjustment register for negative polarity
dig2gam_vr2_n[5:0]: γ gradient adjustment register for negative polarity
dig2gam_vr4_n[4:0]: γ gradient adjustment register for negative polarity</td></tr>
<tr><td>Restriction</td><td colspan="13">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="13"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Id e Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th rowspan="2">Status</th><th colspan="6">Default Value</th></tr><tr><th>dig2gam_dig2j0_n[1:0]</th><th>dig2gam_dig2j1_n[1:0]</th><th>dig2gam_vr0_n[3:0]</th><th>dig2gam_vr1_n[5:0]</th><th>dig2gam_vr2_n[5:0]</th><th>dig2gam_vr4_n[4:0]</th></tr><tr><td>Power On Sequence</td><td>2’h02</td><td>2’h00</td><td>4’h00</td><td>6’h00</td><td>6’h03</td><td>5’h08</td></tr><tr><td>SW Reset</td><td>2’h02</td><td>2’h00</td><td>4’h00</td><td>6’h00</td><td>6’h03</td><td>5’h08</td></tr><tr><td>HW Reset</td><td>2’h02</td><td>2’h00</td><td>4’h00</td><td>6’h00</td><td>6’h03</td><td>5’h08</td></tr></table></td></tr>
</table>

6.4.13. SET_GAMMA2 (F1h)

F1h	SET_GAMMA1												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	0	0	1	F1h
1st Parameter	1	1	↑	XX							dig2gam_dig2j0_p[1:0]		01
2nd Parameter	1	1	↑	XX							dig2gam_dig2j1_p[1:0]		00
3st Parameter	1	1	↑	XX					dig2gam_vr0_p[3:0]				00
4nd Parameter	1	1	↑	XX			dig2gam_vr1_p[5:0]						00
5st Parameter	1	1	↑	XX			dig2gam_vr2_p[5:0]						03
6nd Parameter	1	1	↑	XX				dig2gam_vr4_p[4:0]					08
Description	dig2gam_dig2j0_p[1:0]: γ gradient adjustment register for positive polarity dig2gam_dig2j1_p[1:0]: γ gradient adjustment register for positive polarity dig2gam_vr0_p[3:0]: γ gradient adjustment register for positive polarity dig2gam_vr1_p[5:0]: γ gradient adjustment register for positive polarity dig2gam_vr2_p[5:0]: γ gradient adjustment register for positive polarity dig2gam_vr4_p[4:0]: γ gradient adjustment register for positive polarity												
Restriction	Inter_command should be set high to enable this command												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mo e On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value					
	dig2gam_dig2j0_p[1:0]	dig2gam_dig2j1_p[1:0]	dig2gam_vr0_p[3:0]	dig2gam_vr1_p[5:0]	dig2gam_vr2_p[5:0]	dig2gam_vr4_p[4:0]
Power On Sequence	2'h01	2'h00	4'h00	6'h00	6'h03	5'h08
SW Reset	2'h01	2'h00	4'h00	6'h00	6'h03	5'h08
HW Reset	2'h01	2'h00	4'h00	6'h00	6'h03	5'h08

6.4.14. SET_GAMMA3 (F2h)

F2h	SET_GAMMA3												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	0	1	0	F2h
1st Parameter	1	1	↑	XX				dig2gam_vr6_n[4:0]					06
2nd Parameter	1	1	↑	XX					dig2gam_vr13_n[3:0]				05
3st Parameter	1	1	↑	XX		dig2gam_vr20_n[6:0]							2b
4nd Parameter	1	1	↑	XX						dig2gam_vr27_n[2:0]			04
5st Parameter	1	1	↑	XX						dig2gam_vr36_n[2:0]			04
6nd Parameter	1	1	↑	XX		dig2gam_vr43_n[6:0]							41
Description	dig2gam_vr6_n[4:0]: γ gradient adjustment register for negative polarity dig2gam_vr13_n[3:0]: γ gradient adjustment register for negative polarity dig2gam_vr20_n[6:0]: γ gradient adjustment register for negative polarity dig2gam_vr27_n[2:0]: γ gradient adjustment register for negative polarity dig2gam_vr36_n[2:0]: γ gradient adjustment register for negative polarity dig2gam_vr43_n[6:0]: γ gradient adjustment register for negative polarity												
Restriction	Inter_command should be set high to enable this command												

Register Availability

Status	Availability
Normal Mode On, Idle M de Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value					
	dig2gam_vr6_n[4:0]	dig2gam_vr13_n[3:0]	dig2gam_vr20_n[6:0]	dig2gam_vr27_n[2:0]	dig2gam_vr36_n[2:0]	dig2gam_vr43_n[6:0]
Power On Sequence	5'h06	4'h05	7'h2b	3'h04	3'h04	7'h41
SW Reset	5'h06	4'h05	7'h2b	3'h04	3'h04	7'h41
HW Reset	5'h06	4'h05	7'h2b	3'h04	3'h04	7'h41

6.4.15. SET_GAMMA4 (F3h)

F3h	SET_GAMMA4												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	0	1	1	F3h
1st Parameter	1	1	↑	XX				dig2gam_vr6_p[4:0]					0d
2nd Parameter	1	1	↑	XX					dig2gam_vr13_p[3:0]				08
3st Parameter	1	1	↑	XX		dig2gam_vr20_p[6:0]							2e
4nd Parameter	1	1	↑	XX						dig2gam_vr27_p[2:0]			04
5st Parameter	1	1	↑	XX						dig2gam_vr36_p[2:0]			05
6nd Parameter	1	1	↑	XX		dig2gam_vr43_p[6:0]							3f
Description	dig2gam_vr6_p[4:0]: γ gradient adjustment register for positive polarity dig2gam_vr13_p[3:0]: γ gradient adjustment register for positive polarity dig2gam_vr20_p[6:0]: γ gradient adjustment register for positive polarity dig2gam_vr27_p[2:0]: γ gradient adjustment register for positive polarity dig2gam_vr36_p[2:0]: γ gradient adjustment register for positive polarity dig2gam_vr43_p[6:0]: γ gradient adjustment register for positive polarity												
Restriction	Inter_command should be set high to enable this command												

Register Availability

Status	Avail bility
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value					
	dig2gam_vr6_p[4:0]	dig2gam_vr13_p[3:0]	dig2gam_vr20_p[6:0]	dig2gam_vr27_p[2:0]	dig2gam_vr36_p[2:0]	dig2gam_vr43_p[6:0]
Power On Sequence	5'h0d	4'h08	7'h2e	3'h04	3'h05	7'h3f
SW Reset	5'h0d	4'h08	7'h2e	3'h04	3'h05	7'h3f
HW Reset	5'h0d	4'h08	7'h2e	3'h04	3'h05	7'h3f

6.4.16. SET_GAMMA5 (F4h)

F4h	SET_GAMMA5												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	1	0	0	F4h
1st Parameter	1	1	↑	XX					dig2gam_vr50_n[3:0]				0c
2nd Parameter	1	1	↑	XX				dig2gam_vr57_n[4:0]					17
3st Parameter	1	1	↑	XX				dig2gam_vr59_n[4:0]					18
4nd Parameter	1	1	↑	XX			dig2gam_vr61_n[5:0]						13
5st Parameter	1	1	↑	XX			dig2gam_vr62_n[5:0]						17
6nd Parameter	1	1	↑	XX					dig2gam_vr63_n[3:0]				0d
Description	dig2gam_vr50_n[3:0]: γ gradient adjustment register for negative polarity dig2gam_vr57_n[4:0]: γ gradient adjustment register for negative polarity dig2gam_vr59_n[4:0]: γ gradient adjustment register for negative polarity dig2gam_vr61_n[5:0]: γ gradient adjustment register for negative polarity dig2gam_vr62_n[5:0]: γ gradient adjustment register for negative polarity dig2gam_vr63_n[3:0]: γ gradient adjustment register for negative polarity												
Restriction	Inter_command should be set high to enable this command												

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value					
	dig2gam_vr50_n[3:0]	dig2gam_vr57_n[4:0]	dig2gam_vr59_n[4:0]	dig2gam_vr61_n[5:0]	dig2gam_vr62_n[5:0]	dig2gam_vr63_n[3:0]
Power On Sequence	4'h0c	5'h17	5'h18	6'h13	6'h17	4'h0d
SW Reset	4'h0c	5'h17	5'h18	6'h13	6'h17	4'h0d
HW Reset	4'h0c	5'h17	5'h18	6'h13	6'h17	4'h0d

6.4.17. SET_GAMMA6 (F5h)

F5h	SET_GAMMA6												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	1	1	0	1	0	1	F5h
1st Parameter	1	1	↑	XX					dig2gam_vr50_p[3:0]				0c
2nd Parameter	1	1	↑	XX				dig2gam_vr57_p[4:0]					18
3st Parameter	1	1	↑	XX				dig2gam_vr59_p[4:0]					14
4nd Parameter	1	1	↑	XX			dig2gam_vr61_p[5:0]						14
5st Parameter	1	1	↑	XX			dig2gam_vr62_p[5:0]						18
6nd Parameter	1	1	↑	XX					dig2gam_vr63_p[3:0]				0d
Description	dig2gam_vr50_p[3:0]: γ amplitude adjustment register for positive polarity dig2gam_vr57_p[4:0]: γ amplitude adjustment register for positive polarity dig2gam_vr59_p[4:0]: γ amplitude adjustment register for positive polarity dig2gam_vr61_p[5:0]: γ amplitude adjustment register for positive polarity dig2gam_vr62_p[5:0]: γ amplitude adjustment register for positive polarity dig2gam_vr63_p[3:0]: γ amplitude adjustment register for positive polarity												
Restriction	Inter_command should be set high to enable this command												

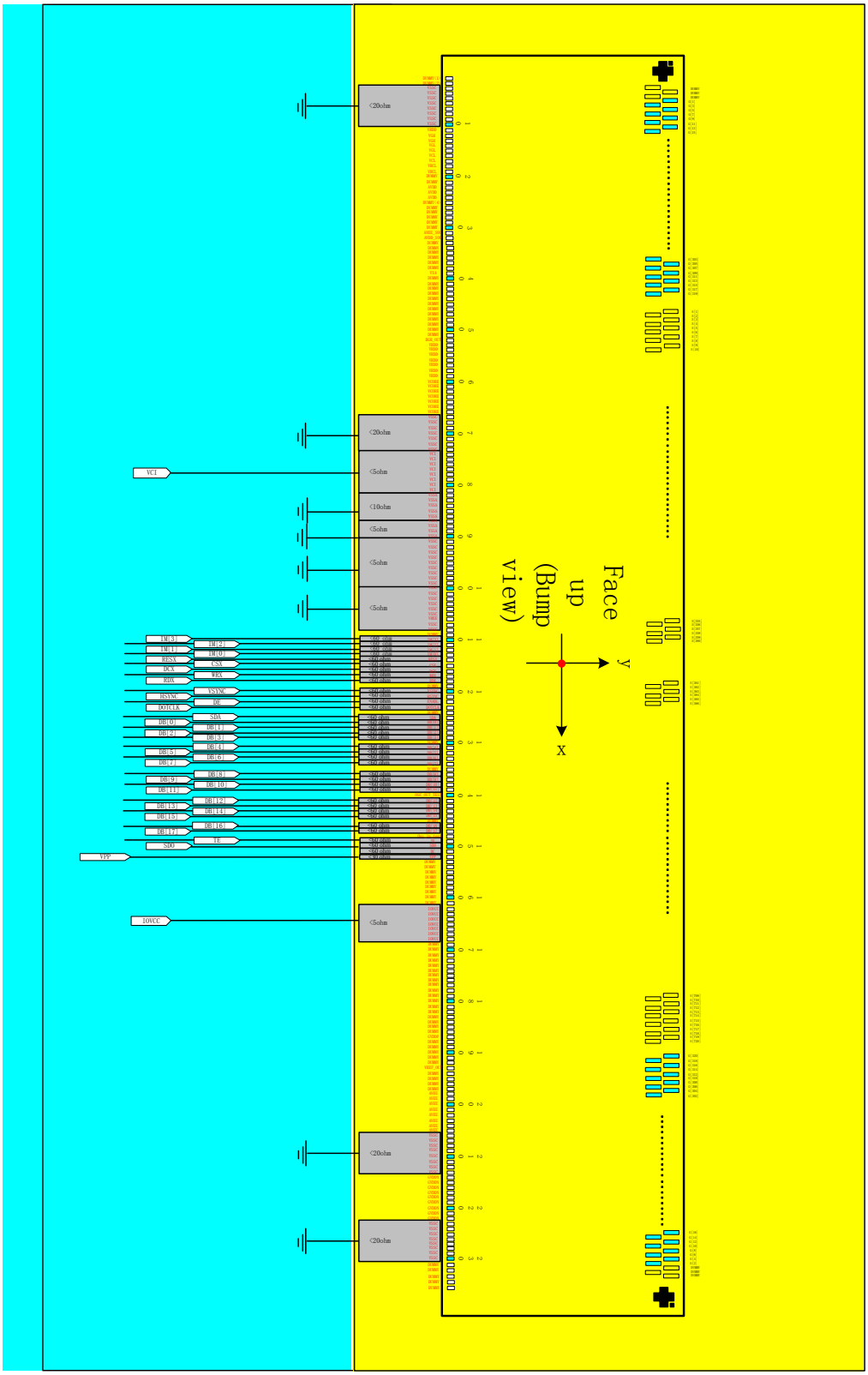
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value					
	dig2gam_vr50_p[3:0]	dig2gam_vr57_p[4:0]	dig2gam_vr59_p[4:0]	dig2gam_vr61_p[5:0]	dig2gam_vr62_p[5:0]	dig2gam_vr63_p[3:0]
Power On Sequence	4'h0c	5'h18	5'h14	6'h14	6'h18	4'h0d
SW Reset	4'h0c	5'h18	5'h14	6'h14	6'h18	4'h0d
HW Reset	4'h0c	5'h18	5'h14	6'h14	6'h18	4'h0d

7. Application



8. Electrical Characteristics

8.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When GC9306 is used out of the absolute maximum ratings, GC9306 may be permanently damaged. To use GC9306 within the following electrical characteristics limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, GC9306 will malfunction and cause poor reliability.

Table43.

Item	Symbol	Unit	Value
Supply voltage	VCI	V	-0.3~+4.6
Supply voltage(Logic)	IOVCC	V	-0.3~+4.6
Supply voltage(Digital)	VCORE	V	-0.3~+2.0
Driver supply voltage	VGH-VGL	V	-0.3~+32.0
Logic input voltage range	VIN	V	-0.3~IOVCC+0.3
Logic output voltage range	VO	V	-0.3~IOVCC+0.3
Operation temperature	Topr	℃	-40~+85
Storage temperature	Tstg	℃	-55~+110

Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

8.2. DC Characteristics

General DC Characteristics

Table44.

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
Power and Operation Voltage							
Analog Operating Voltage	VCI	V	Operating voltage	2.5	2.8	3.3	Note2
Logic Operating Voltage	IOVCC	V	I/O supply voltage	1.65	2.8	3.3	Note2
Digital Operating voltage	VCORE	V	Digital supply voltage	-	1.34	-	Note2
Gate Driver High Voltage	VGH	V	-	10.0	-	12.0	Note3
Gate Driver Low Voltage	VGL	V	-	-11.0	-	-9.0	Note3
Driver Supply Voltage	-	V	|VGH-VGL|	19	-	23	Note3
Input and Output							
Logic High Level Input Voltage	VIH	V	-	0.7*IOVCC	-	IOVCC	Note1,2,3
Logic Low Level Input Voltage	VIL	V	-	VSSC	-	0.3*IOVCC	Note1,2,3
Logic High Level Output Voltage	VOH	V	IOL=-1.0mA	0.8*IOVCC	-	IOVCC	Note1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	VSSC	-	0.2*IOVCC	Note1,2,3
Logic High Level Input Current	IIH	uA	-	-	-	1	Note1,2,3
Logic Low Level Input Current	IIL	uA	-	-1	-	-	Note1,2,3
Logic Input Leakage Current	ILEA	uA	VIN=IOVCC or VSSC	-0.1	-	+0.1	Note1,2,3
Source Driver							
Source Output Range	Vsout	V	-	VREG2	-	VREG1	Note4

Note 1: IOVCC=1.65 to 3.3V, VCI=2.5 to 3.3V, AGND=VSS=0V, Ta=-30 to 70 (to +85 no damage)℃

Note2: Please supply digital IOVCC voltage equal or less than analog VCI voltage.

Note3: CSX, RDX, WRX, D[17:0], D/CX, RESX, TE, DOTCLK, VSYNC, HSYNC, DE, SDA, SCL, IM3, IM2, IM1,IM0, and Test pins.

Note4: When the measurements are performed with LCD module. Measurement Points are like Note3.

Note5: VCI=2.6V

Note6: VCI=3.3V

Note7: The Max. Value is between with Note 4 measure point and Gamma setting value

8.3. AC Characteristics

8.3.1. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-Ⅰ)

Figure90.

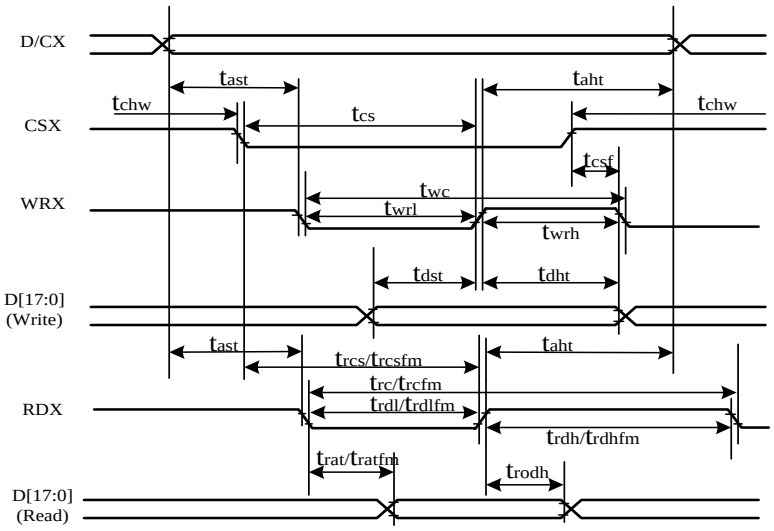


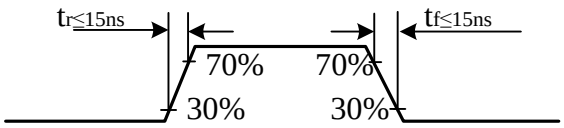
Table45.

Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time(Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time(Write)	15	-	ns	
	trcs	Chip Select setup time(Read ID)	45	-	ns	
	trcsfm	Chip Select setup time(Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write Cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX(FM)	trcfm	Read Cycle (FM)	380	-	ns	
	trdhfm	Read Control H duration(FM)	180	-	ns	
	trdlfm	Read Control L duration(FM)	200	-	ns	
RDX(ID)	trc	Read Cycle (ID)	160	-	ns	
	trdh	Read Control H pulse duration	90	-	ns	
	trdl	Read Control L pulse duration	70	-	ns	
D[17:0],D[15:0],D[8:0],	tdst	Write data setup time	10	-	ns	For maximum CL=30pF
	tdht	Write data hold time	10	-	ns	For minimum CL=8pF

D[7:0]	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

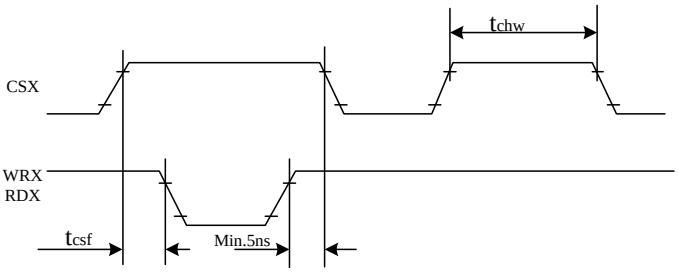
Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V

Figure91.



CSX timings :

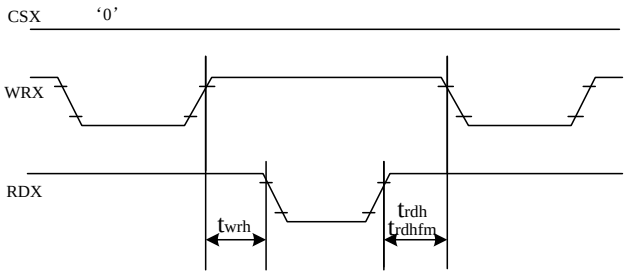
Figure92.



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Write to read or read to write timings:

Figure92.



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

8.3.2. Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-Ⅱ)

Figure93.

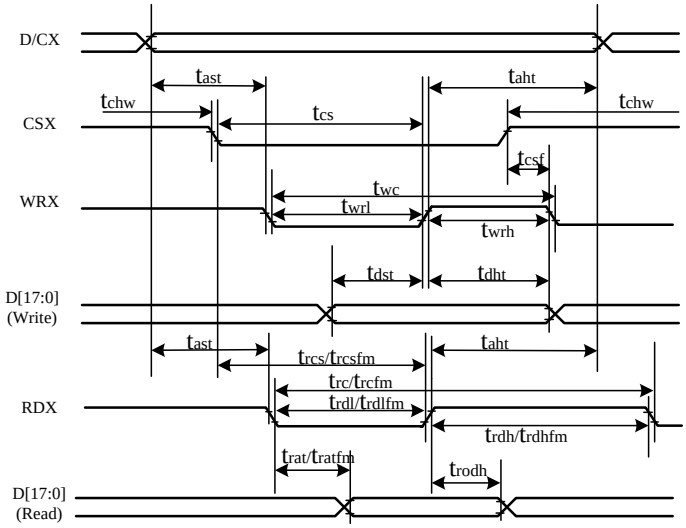


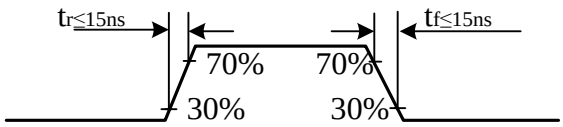
Table46.

Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time(Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time(Write)	15	-	ns	
	trcs	Chip Select setup time(Read ID)	45	-	ns	
	trcsfm	Chip Select setup time(Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write Cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX(FM)	trcfm	Read Cycle (FM)	380	-	ns	
	trdhfm	Read Control H duration(FM)	180	-	ns	
	trdlfm	Read Control L duration(FM)	200	-	ns	
RDX(ID)	trc	Read Cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	70	-	ns	
D[17:0],D[17:10]&D[8:1],D[17:10],D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	

	trod	Read output disable time	20	80	ns	

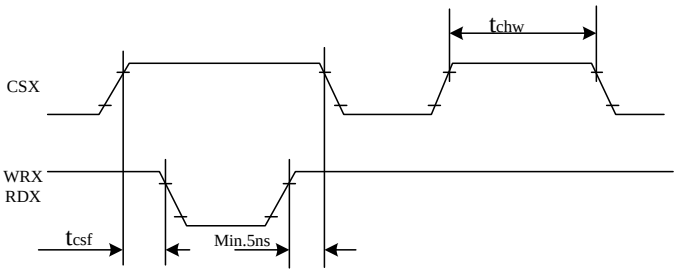
Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V.

Figure94.



CSX timings :

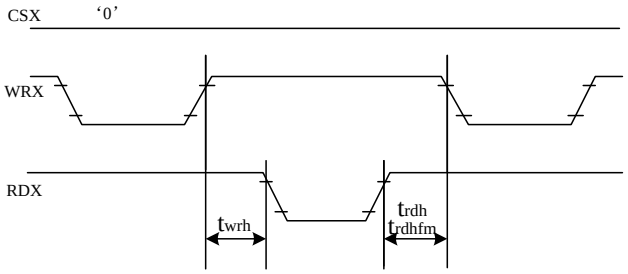
Figure95.



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Write to read or read to write timings:

Figure96.



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

8.3.3. Display Serial Interface Timing Characteristics (3-line SPI system)

Figure97.

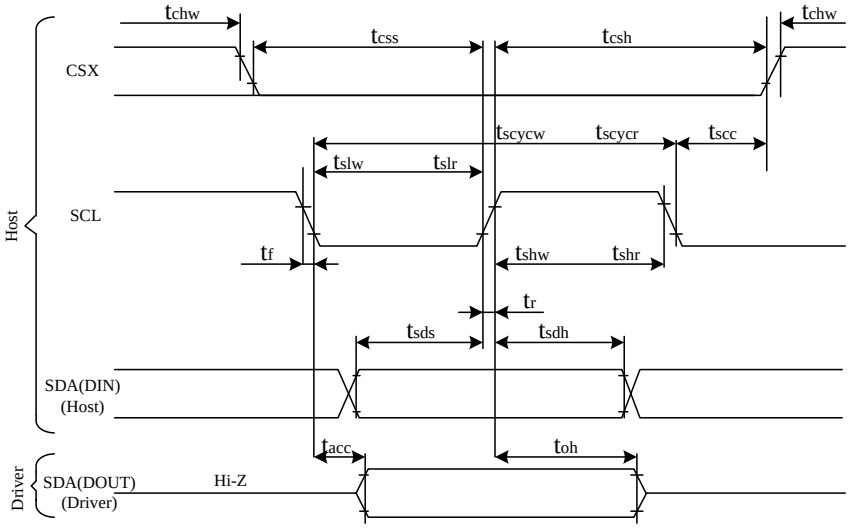
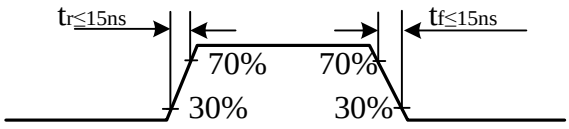


Table47.

Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	10	-	ns	
	tshw	SCL "H" Pulse Width (Write)	5	-	ns	
	tslw	SCL "L" Pulse Width (Write)	5	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA/SDI (Input)	tsds	Data setup time (Write)	5	-	ns	
	tsdh	Data hold time (Write)	5	-	ns	
SDA/SD0(Outp)	tacc	Access time (Read)	10	-	ns	
CSX	tscc	SCL-CSX	10	-	ns	
	tchw	CSX "H" Pulse Width	10	-	ns	
	tcss	CSX-SCL Time	20	-	ns	
	tcsh		40	-	ns	

Note: Ta = 25 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, VSSA=VSSC=0V

Figure98.



8.3.4. Display Serial Interface Timing Characteristics (4-line SPI system)

Figure98.

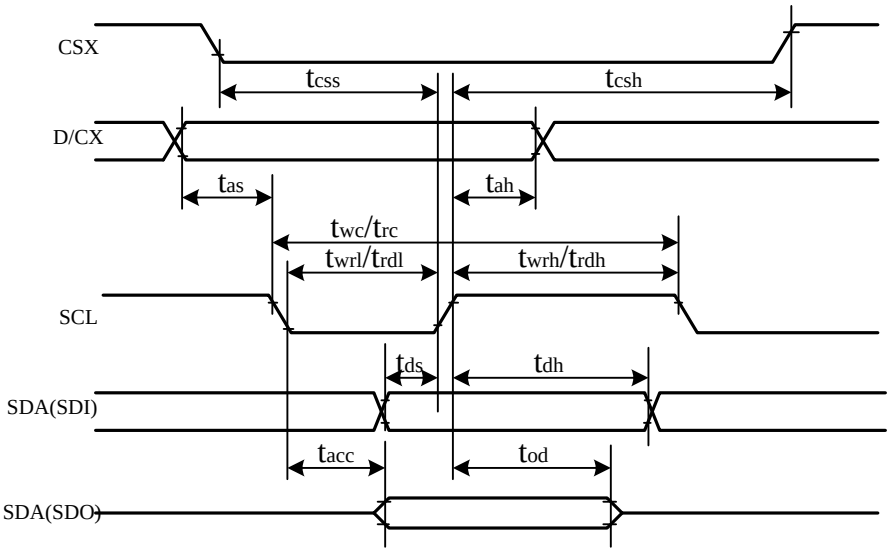
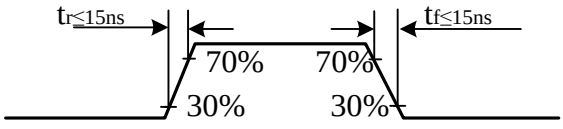


Table48.

Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	20	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial Clock Cycle (Write)	10	-	ns	
	twrh	SCL "H" Pulse Width (Write)	5	-	ns	
	twrl	SCL "L" Pulse Width (Write)	5	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL "H" Pulse Width (Read)	60	-	ns	
	trdl	SCL "L" Pulse Width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA/SDI (Input)	tds	Data setup time (Write)	5	-	ns	
	tdh	Data hold time (Write)	5	-	ns	
SDA/SD0 (Output)	tacc	Access time (Read)	10	-	ns	

Note: Ta = 25 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

Figure99.



8.3.5. Parallel 18/16/6-bit RGB Interface Timing Characteristics

Figure100.

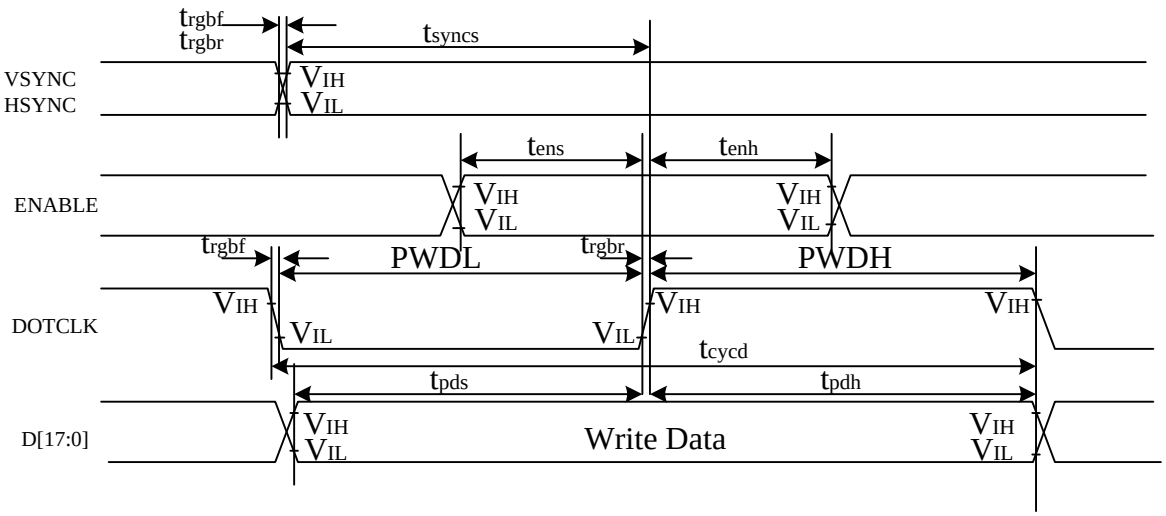
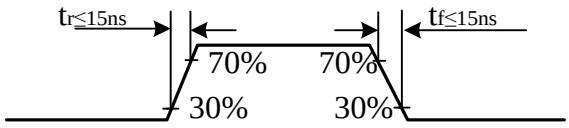


Table49.

Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/HSYNC	tsyncs	VSYNC/HSYNC setup time	15	-	ns	
	tsynch	VSYNC/HSYNC hold time	15	-	ns	
DE	tens	DE setup time	15	-	ns	
	tenh	DE hold time	15	-	ns	
D[17:0]	tpos	Data setup time	15	-	ns	18/16-bit bus RGB interface mode
	tpdh	Date hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	tcycd	DOTCLK cycle time	100	-	ns	
	trgbr,trgbf	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC/HSYNC	tsyncs	VSYNC/HSYNC setup time	15	-	ns	
	tsynch	VSYNC/HSYNC hold time	15	-	ns	
DE	tens	DE setup time	15	-	ns	
	tenh	DE hold time	15	-	ns	
D[17:0]	tpos	Data setup time	15	-	ns	6-bit bus RGB interface mode
	tpdh	Date hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	tcycd	DOTCLK cycle time	100	-	ns	
	trgbr,trgbf	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

Figure101.



9. Revision History

Version No.	Date	Page	Description
V1.00	2016-11-16	All	New Created
V1.01	2016-11-30	190/191	Table47 table48 modified