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(54) **INTEGRATED CIRCUIT INTERFACE WITH LOCKING SIGNAL**

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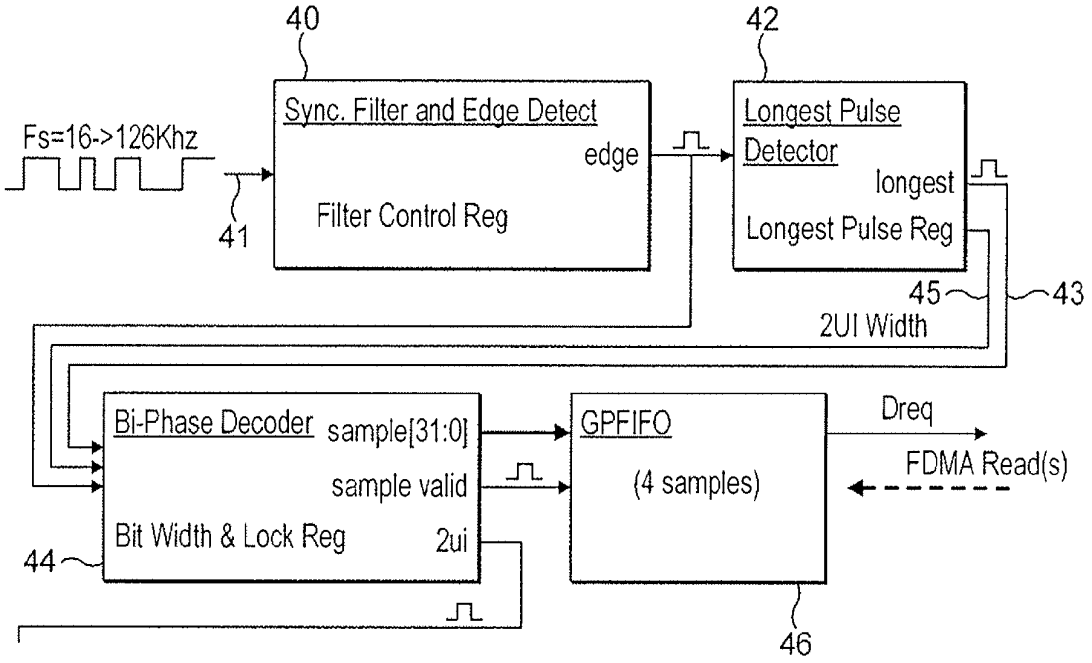
(57) **ABSTRACT**

An integrated circuit for recovering a position and clock period from an input bi-phase encoded digital signal, such as an SPDIF signal, has a longest interval detector arranged to count the intervals between phase changes of the input digital signal to derive the longest interval between the phase changes. The longest interval indicates the position and period length of a preamble portion of sub-frames of the signal. A store arranged to store the longest interval between phase changes and an output provides a signal indicating the position of the longest interval between phase changes and an indication of the clock period of the input digital signal. The longest interval detector includes a pair of counters for even and odd phase transitions and counts in multiple intervals such that a clock period of 2UI can be recovered directly from the longest pulse of 6UI present in the preamble X of an SPDIF signal.



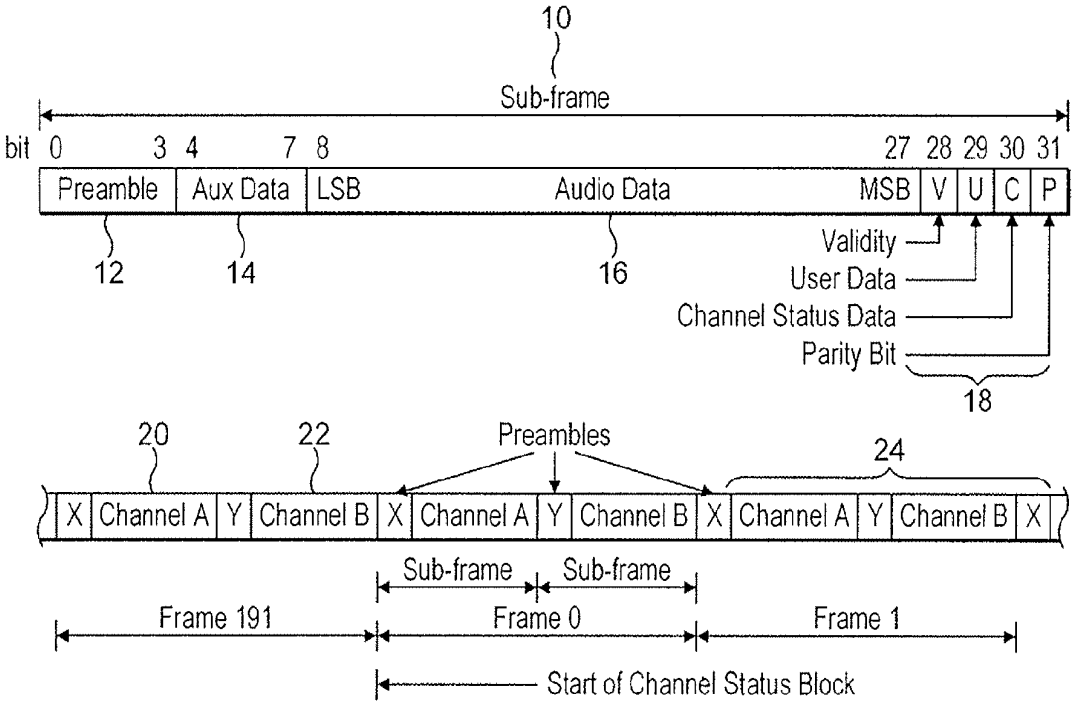

10
Sub-frame
bit 0 3 4 7 8 27 28 29 30 31
Preamble
Aux Data
LSB
Audio Data
MSB
V
U
C
P
12
14
16
Validity
User Data
Channel Status Data
Parity Bit
18
20
22
Preambles
24
X
Channel A
Y
Channel B
Sub-frame
Sub-frame
Frame 191
Frame 0
Frame 1
Start of Channel Status Block

FIG. 1

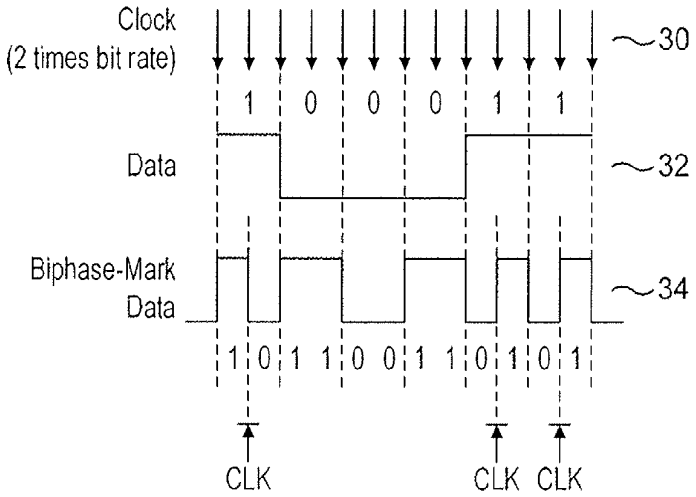

Clock
(2 times bit rate)
30
1 0 0 0 1 1
Data
32
Biphase-Mark
Data
34
1 0 1 1 0 0 1 1 0 1 0 1
CLK
CLK
CLK

FIG. 2

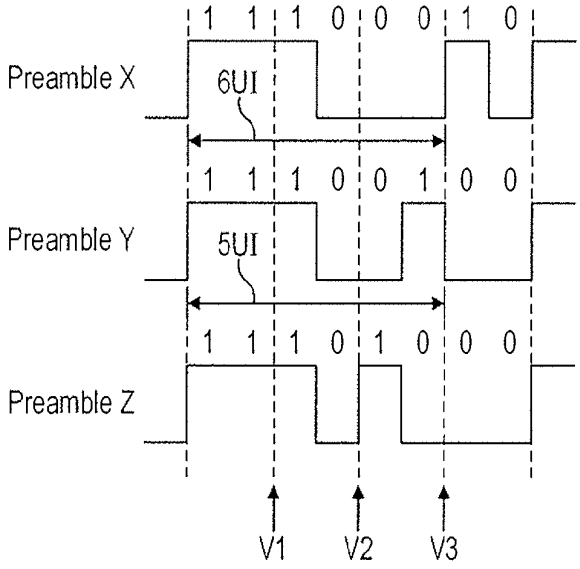

1 1 1 0 0 0 1 0
Preamble X
6UI
1 1 1 0 0 1 0 0
Preamble Y
5UI
1 1 1 0 1 0 0 0
Preamble Z
V1
V2
V3

FIG. 3

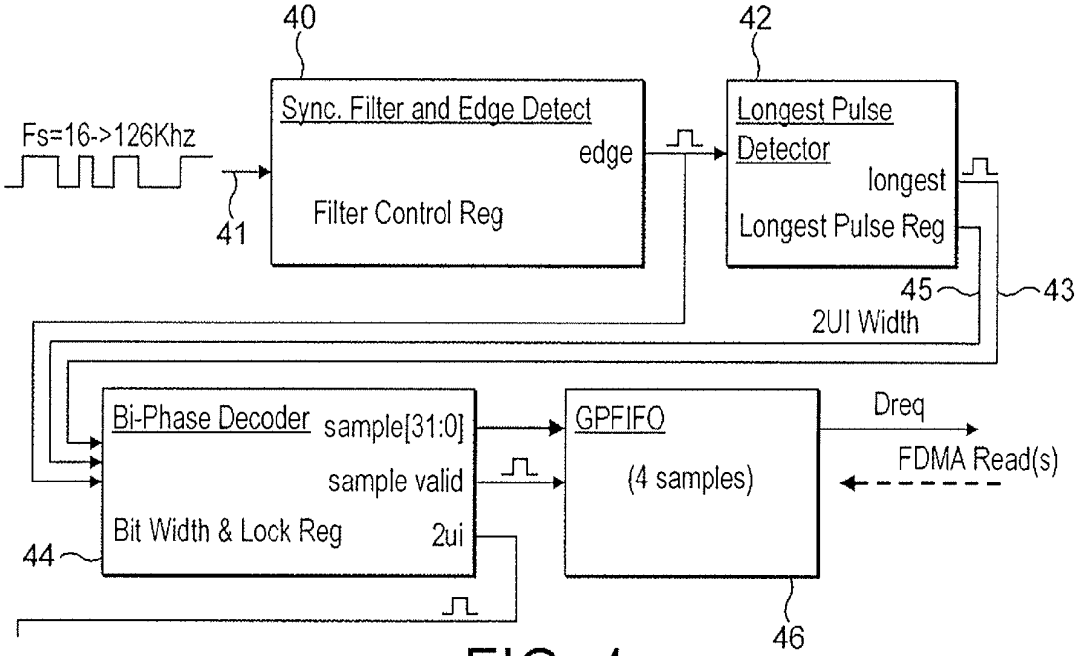

40
42
Fs=16->126Khz
Sync. Filter and Edge Detect
edge
Filter Control Reg
41
Longest Pulse Detector
longest
Longest Pulse Reg
45
43
2UI Width
Bi-Phase Decoder
sample[31:0]
sample valid
Bit Width & Lock Reg
2ui
44
GPFIFO
(4 samples)
Dreq
FDMA Read(s)
46

FIG. 4

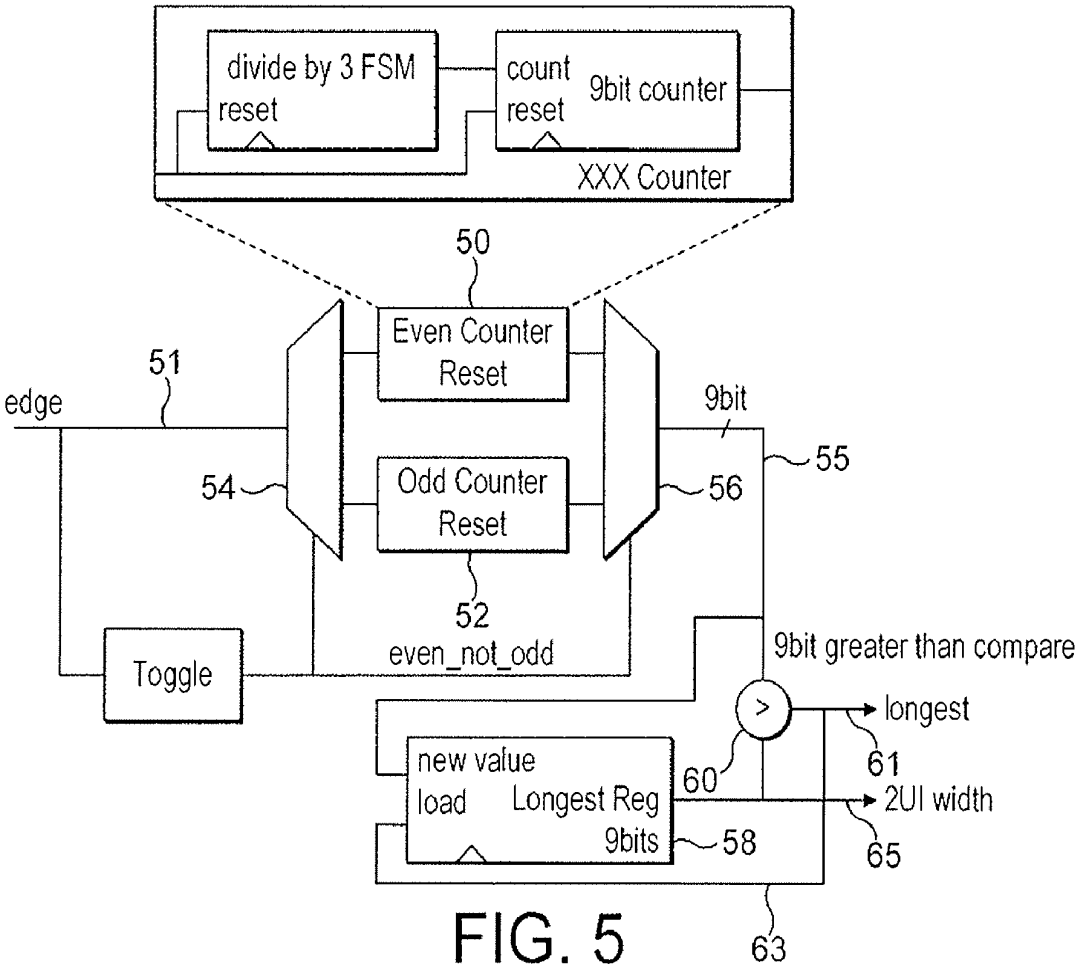

divide by 3 FSM
reset
count
reset
9bit counter
XXX Counter
50
Even Counter
Reset
51
edge
9bit
55
54
Odd Counter
Reset
56
52
even_not_odd
Toggle
9bit greater than compare
>
longest
61
new value
load
Longest Reg
9bits
58
60
2UI width
65
63

FIG. 5

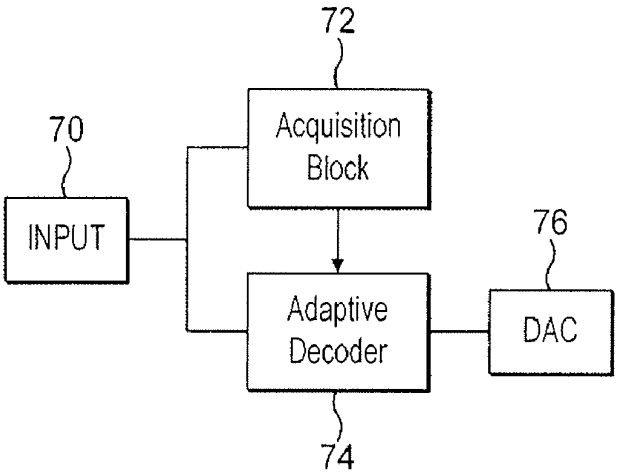

72
70
Acquisition
Block
INPUT
76
Adaptive
Decoder
DAC
74

FIG. 6

INTEGRATED CIRCUIT INTERFACE WITH LOCKING SIGNAL

RELATED APPLICATION

[0001] This application claims priority of European Patent Application 06252736.1 filed May 25, 2006, incorporated herein in its entirety by this reference.

FIELD OF THE INVENTION

[0002] The present invention relates to a semiconductor integrated circuit providing an interface to receive and lock to an incoming digital data signal. The invention is particularly applicable to an interface of the type which may handle digital data having a wide frequency range, as occurs in consumer electronics device interfaces such as for DVD players/recorders.

BACKGROUND OF THE INVENTION

[0003] In electronics devices, particularly consumer electronics audio/video players and recorders, there is a need to exchange digital data between devices. This is so that audio or video data can be exchanged for processing. For example, an audio amplifier typically has a digital input to receive an output from a DVD player. To provide such an interface various standards are known, one such being the known Sony Philips Digital InterFace format (SPDIF).

[0004] The SPDIF format is used for digital exchange of audio data between devices. The format is well known and is briefly described later for completeness. In brief, the format comprises a structure of 32 bit sub-frames with two such sub-frames (left and right audio) comprising a frame of data. The frequency of data can vary over a wide range (16 kHz-192 kHz), the higher the frequency, the better the quality of the audio signal. The signal is bi-phase encoded so that the clock signal and data signal are encoded on a single line. There is a need to recover the clock signal from the data signal. There is also a need to identify the start of each data frame and sub-frame. We have appreciated that the characteristics of a data signal of differing possible frequencies can be used to determine and lock on the start of data frames and determine the unit interval on frequency of the signal. The invention is defined in the claims to which reference is now directed.

[0005] The invention makes use of the appreciation that the preamble section (a header) of a digital data frame or sub-frame can include certain characteristic markers by which the start of a sub-frame or frame can be determined, as well as the frequency of the signal. In the embodiment, the particular characteristic is the fact that the preamble of a sub-frame includes a pulse (in the sense of the time between the successive signal edges) that is longer than any such pulse in the data signal. This allows the position of the preamble and the frequency of the clock signal to be quickly determined. The preferred embodiment of the invention relates to the SPDIF format of digital audio signal. In this format the preamble includes a portion which violates the normal bi-phase coding rules and, in consequence, has a gap between the successive edges that is 6 unit intervals (UI) in contrast to the longest gap of 4 unit intervals (UI) in the data portion of the data stream. The embodiment therefore includes a longest pulse detector that determines whenever there is a longer gap between edges than preceding bits. At this point, the output of the longest pulse detector is asserted, indicating to a signal decoder the position of the frames and sub-frames and the clock frequency.

[0006] The invention allows very fast locking of the position a and frequency of a binary phase encoded signal with a characteristic preamble or header. The embodiment counts for a period long enough that at least one sub-frame header would be seen (in the case of SPDIF this is 128 bits). The longest pulse received in that time is known to be a specific position in the preamble that is 6UI. By counting every third period the clock period of 2UI can be rapidly recovered.

[0007] The invention may apply to formats other than SPDIF, but is particularly applicable to digital signals having a given format, but wide possible range of signal frequency.

BRIEF DESCRIPTION OF THE FIGURES

[0008] An embodiment of the invention will now be described by way of example only and with reference to the figures in which:

[0009] FIG. **1** shows the format of SPDIF frames;

[0010] FIG. **2** shows the effect of bi-phase coding of a signal;

[0011] FIG. **3** shows the format of the preamble portion of an SPDIF signal;

[0012] FIG. **4** shows an acquisition block of a semiconductor integrated circuit embodying the invention;

[0013] FIG. **5** shows a longest pulse detector of a semiconductor integrated circuit embodying the invention; and

[0014] FIG. **6** shows an electronic device embodying the invention.

DESCRIPTION OF A PREFERRED EMBODIMENT

[0015] The preferred embodiment is a semiconductor integrated circuit for acquisition of a SPDIF format digital audio signal. As already described, the invention is applicable to other formats of signal, but is particularly useful for bi-phase coded digital signals that may have any of a range of frequencies, as is the case for SPDIF format.

[0016] The SPDIF format of digital audio signals will first be described by way of background with reference to FIGS. **1** to **3**. The frame and sub-frame format of the SPDIF signal is shown in FIG. **1** and comprises a preamble section **12**, auxiliary data section **14** and audio data section **16**, the whole assembled comprising a sub-frame **10** which also includes various parity and status bits **18**. The sub-frames are assembled in a sequence of alternating types shown as Channel A **20** and Channel B **22**. These provide left and right audio data respectively and are alternated with one another. A pair of sub-frames of Channel A and Channel B together comprises a frame of data **24**. The frames themselves are assembled into a sequence of 192 frames, with a given preamble identified as preamble **12** repeated every 192 frames.

[0017] The preamble **12** of each sub-frame is a type of header which provides a marker for the start of each sub-frame. In SPDIF, there are two main types of preamble: type

X associated with each Channel A sub-frame and type Y associated with each Channel B sub-frame.

[0018] Prior to describing the preamble X and preamble Y, the bi-phase coding of data will be described with reference to FIG. **2**. Bi-phase coding involves modulating a data signal with a clock signal so that data and clock are coded together and transportable on a single bit bus. As shown in FIG. **2**, a clock signal **30** (at two times the bit rate of the data signal) is coded onto a data signal **32**. The coding is performed so that an edge (that is a change of signal state) within a bit indicates a "1" in the data signal, the absence of an edge within a bit indicates a "0" in the data signal. Thus, the first bit of data is "1" and so the bi-phase mark data has a transition change at the position marked as "CLK". The second, third and fourth bits in the data signal are "0" and so the bi-phase mark data continues in a sequence with no edges within each bit. The fifth and sixth bits are both "1" and so these have edges as shown by the positions "CLK". In this way the clock and data signals are coded together.

[0019] The Unit Interval (UI) in bi-phase coded data is the space between transitions. In the signal shown there are two UIs for each data bit (the clock rate being twice the data rate).

[0020] The system needs to recover an accurate clock signal from the bi-phase coded signal. After bi-phase coding there can be narrow and wide UIs and the system needs to identify edges of bits to find clock edges in the signal. A known solution to recover the clock signal uses a Phase Locked Loop (PLL) to analyse the digital signal over many repeated cycles until a lock or the data signal itself is formed. A PLL typically takes of the order 20 ms to settle, and decoding cannot start until the clock has settled. The embodiment, however, uses a property of the preamble of the sub-frames to allow the signal to be acquired using a smaller integrated circuit and in a shorter time than the known PLL.

[0021] The structure of the three different preamble signals X, Y and Z is shown in FIG. **3**. These preamble signals use bi-phase coding violation as a mechanism to indicate the start of a sub-frame. Consider first the preamble X. In normal bi-phase coding, the bit sequence continues as 101010 etc, with a transition within each bit to indicate a "1" and the absence of a transition within each bit to indicate a "0". The preamble X starts with a high bit without any intra-bit transition. At the end of the first bit period, indicated as time VI, the signal does not drop to zero. The signal violates the bi-phase coding rule. Similarly, after two bit periods, at time V**2**, the signal does not change and so the bi-phase rule is violated.

[0022] The same situation occurs for preamble Y which violates the bi-phase coding at times V**1** and V**2**. Preamble Z violates the rules at times V**1** and V**3**. The bi-phase encoder inserts these violations to help the preamble stand out from the data. A consequence of the bi-phase violations is the length of the "pulse" within the preambles is longer than that within the data itself. The first pulse, that is the period from one rising clock edge to another in preamble X is 6UI. The first pulse in preamble Y is 5UI. The pulse is thus the time period between rising clock edges and is longer than any pulse in the data signal. Referring back to FIG. **2**, it can be seen that the longest period between rising clock edges is 4UI.

[0023] The embodiment comprises a "longest pulse" detector which detects the presence of this longer than normal period between rising clock edges which then instructs the circuit that the preamble has been located. At this point, the circuit can immediately begin decoding the signal.

[0024] The acquisition block of a circuit embodying the invention is shown in FIG. **4**. The block comprises a filter control register **40**, a bit width and lock register **44** and GDFIFO **46** which can be implemented in known fashion. The additional feature in the block is the longest pulse register **42**. The circuit operates as follows. An incoming signal **41**, which may have frequency in a wide range, is first processed by the filter control register **40**. This produces a pulse for each edge detection in the incoming signal. The pulses are then sent to the longest pulse detector. This asserts an output on a line, line **43**, whenever a pulse in the received signal **41** is longer than a previous pulse. In addition, the longest pulse register **42** outputs a frequency indication signal on a line, line **45**, indicating the 2UI period of the incoming signal, thereby indicating the signal frequency. The bit width and lock register **44** implements a bi-phase decoder and this recovers the data signal from the clock signal for input to a GPFIFO **46** for subsequent processing.

[0025] There are various possible implementations of the longest pulse detector, the preferred implementation being shown in FIG. **5**. The longest pulse detector comprises two counters **50**, **52** termed "even", counter **50** and "odd" counter **52**. These are arranged to alternately start counting in multiples of the UI period as alternate clock edges of the input signal. The reason for having two such counters in this arrangement is to ensure that the longest gap is not missed. If one refers back to FIG. **3**, it can be seen that starting a count on the first rising clock edge will count 6UI as the pulse length, but starting on any other clock edge would give a shorter pulse length such that the long pulse, and hence the preamble, would not be detected. The input bi-phase signal could be inverted such that the longest pulse is between two falling clock edges, rather than between two rising clock edges. Using two counters ensures that the longest pulse in either situation will be found. The input edge signal on input line **51** is therefore provided to a first multiplexer **54** which is toggled every edge signal to provide the input edge signal alternately to a reset input of "even" counter **50** and "odd" counter **52**. These counters count in any integer multiple of the UI period. In the present example the count period is every third cycle, effectively dividing by three, as shown by the divide by 3 FSM unit in FIG. **5**. The advantage of this is to derive the clock signal without requiring subsequent division, as the 6UI pulse divided by three gives 2UI, which is the clock period. It is a neat arrangement to perform the division by simply counting in multiples of UI, rather than requiring further hardware to perform the division.

[0026] A second multiplexer **56** takes the output of each counter as a counter output line **55** and provides this to a longest value register **58**. This register loads the new value at a new value input each time a longest pulse is detected. This is done by comparing the previous value for the longest pulse stored in the register with the current value using comparator **60**. If the current value is longer than the previous value then an output is asserted on line **61** to the bi-phase decoder (FIG. **4**). Simultaneously, the comparator output is taken on line **63** to the longest value register **58** and

presented at a load input causing the current longest pulse value to be stored in the register. The longest pulse register also outputs the pulse width on line **65**. Recalling that the preferred embodiment counts in a clock divided by 3, the longest pulse value output is the 2UI width (the clock period) as required by later blocks. This is a matter of design choice and the counters could count in UI units and thus output the value 6UI (as shown in the preamble X signal) which can be divided later. The implementation of counting in a multiple of UI, in this case 3UI, allows a clock period to be directly recovered, rather than requiring further hardware for subsequent division. The 2UI period is then supplied to an adaptive decoder which then derives an accurate clock signal. Adaptive decoders are well known and need not be describer here. The decoder simply needs to approximate frequency (because the input frequency could be any of a broad range of frequencies) and can then operate to recover a more accurate clock. The period of time during which the pulse lengths need to be counted in the SPDIF signal can be seen by referring back to FIG. **1**. The preamble X repeats every 4 sub-frames. Each sub-frame is 32 bits in length, and so the counter needs to count at least 4×32=128 bits to ensure that the longest pulse will have occurred in that time period. In other signals this period may differ. In general, a longest pulse detector needs to count for the duration of the repeat period of the characteristic longest pulse in the signal to be analysed.

[**0027**] Once the longest pulse has been recovered and the position and 2UI period provided to the adaptive decoder, the longest pulse detector no longer operates and is removed from the signal path by a simple gate arrangement (not shown). This ensure that no further "longest pulses" are provided to the adaptive decoder as these could be glitches in the signal and, when operational, the adaptive decoder no longer requires further indications of the clock period.

[**0028**] A device such as an audio amplifier or the like embodying the invention is shown in FIG. **6**. An input **70** provides the bi-phase signal to the acquisition block **72** (as already described) which provides the position and clock period signal to an adaptive decoder **74** which then provides an accurate clock to the DAC **76**. Other circuitry (not shown) for processing and amplifying the signal is also provided.

[**0029**] While there have been described above the principles of the present invention in conjunction with specific circuit designs and methods of operation, it is to be clearly understood that the foregoing description is made only by way of example and not as a limitation to the scope of the invention. Particularly, it is recognized that the teachings of the foregoing disclosure will suggest other modifications to those persons skilled in the relevant art. Such modifications may involve other features which are already known per se and which may be used instead of or in addition to features already described herein. Although claims have been formulated in this application to particular combinations of features, it should be understood that the scope of the disclosure herein also includes any novel feature or any novel combination of features disclosed either explicitly or implicitly or any generalization or modification thereof which would be apparent to persons skilled in the relevant art, whether or not such relates to the same invention as presently claimed in any claim and whether or not it mitigates any or all of the same technical problems as confronted by the present invention. The applicant hereby reserves the right to formulate new claims to such features and/or combinations of such features during the prosecution of the present application or of any further application derived therefrom.

1. An integrated circuit for recovering a position and clock period from an input digital signal of the type having a marker period between phase changes that is longer than other periods between phase changes in the digital signal, comprising:

a longest interval detector arranged to count the intervals between phase changes of the input digital signal to derive the longest interval between the phase changes;

a store arranged to store the longest interval between phase changes;

an output arranged to provide a signal indicating the position of the longest interval between phase changes and an indication of the clock period of the input digital signal.

2. An integrated circuit according to claim 1, wherein the longest interval detector is arranged to detect the longest interval between phase changes in a first direction and the longest interval between phase changes in a second direction.

3. An integrated circuit according to claim 1, wherein the longest interval detector is arranged to count in multiple unit intervals such that the indication of the clock period is effectively a division of the longest interval.

4. An integrated circuit according to claim 3, wherein the longest interval detector is arranged to detect the longest interval between phase changes in a first direction and the longest interval between phase changes in a second direction.

5. An integrated circuit according to claim 2 wherein the longest interval detector comprises a first counter arranged to detect the longest interval between phase changes in the first direction and a second counter arranged to detect the longest interval between phase changes in the second direction.

6. An integrated circuit according to claim 3, wherein the longest interval detector comprises a first counter arranged to detect the longest interval between phase changes in the first direction and a second counter arranged to detect the longest interval between phase changes in the second direction.

7. An integrated circuit according to claim 4, wherein the longest interval detector comprises a first counter arranged to detect the longest interval between phase changes in the first direction and a second counter arranged to detect the longest interval between phase changes in the second direction.

8. An integrated circuit according to claim 1, wherein the input digital signal is a bi-phase encoded signal of clock period 2UI, the longest interval is 6UI and the longest interval detector is arranged to count in multiples of 3 such that the clock period of 2UI is directly recovered from the longest interval.

9. An integrated circuit according to claim 2, wherein the input digital signal is a bi-phase encoded signal of clock period 2UI, the longest interval is 6UI and the longest

interval detector is arranged to count in multiples of 3 such that the clock period of 2UI is directly recovered from the longest interval.

10. An integrated circuit according to claim 3, wherein the input digital signal is a bi-phase encoded signal of clock period 2UI, the longest interval is 6UI and the longest interval detector is arranged to count in multiples of 3 such that the clock period of 2UI is directly recovered from the longest interval.

11. An integrated circuit according to claim 7, wherein the input digital signal is a bi-phase encoded signal of clock period 2UI, the longest interval is 6UI and the longest interval detector is arranged to count in multiples of 3 such that the clock period of 2UI is directly recovered from the longest interval.

12. An integrated circuit according to claim 1, wherein the digital signal is a bi-phase encoded signal and the longest interval detector is arranged to detect a longest interval that violates bi-phase encoding rules in a header of the signal.

13. An integrated circuit according to claim 2, wherein the digital signal is a bi-phase encoded signal and the longest interval detector is arranged to detect a longest interval that violates bi-phase encoding rules in a header of the signal.

14. An integrated circuit according to claim 3, wherein the digital signal is a bi-phase encoded signal and the longest interval detector is arranged to detect a longest interval that violates bi-phase encoding rules in a header of the signal.

15. An integrated circuit according to claim 1, wherein the input digital signal is an SPDIF signal and the longest interval detector is arranged to detect the longest period in the preamble.

16. An integrated circuit according to claim 11, wherein the input digital signal is an SPDIF signal and the longest interval detector is arranged to detect the longest period in the preamble.

17. An integrated circuit according to claim 12, wherein the input digital signal is an SPDIF signal and the longest interval detector is arranged to detect the longest period in the preamble.

18. A device for decoding a digital signal of the type comprising a clock and data signal, the device comprising an input, a decoder, a digital to analogue converter and an integrated circuit, comprising:

a longest interval detector arranged to count the intervals between phase changes of the input digital signal to derive the longest interval between the phase changes;

a store arranged to store the longest interval between phase changes;

an output arranged to provide to the decoder a signal indicating the position of the longest interval between phase changes and an indication of the clock period of the input digital signal.

19. An audio amplifier for decoding an audio digital signal of the type comprising a clock and data signal, the amplifier comprising an input, a decoder, a digital to analogue converter and an integrated circuit, comprising:

a longest interval detector arranged to count the intervals between phase changes of the input digital signal to derive the longest interval between the phase changes;

a store arranged to store the longest interval between phase changes;

an output arranged to provide to the decoder a signal indicating the position of the longest interval between phase changes and an indication of the clock period of the input digital signal.

20. A DVD player and/or recorder for decoding a digital signal of the type comprising a clock and data signal, comprising a decoder, a digital to analogue converter and an integrated circuit comprising:

a longest interval detector arranged to count the intervals between phase changes of the input digital signal to derive the longest interval between the phase changes;

a store arranged to store the longest interval between phase changes;

an output arranged to provide to the decoder a signal indicating the position of the longest interval between phase changes and an indication of the clock period of the input digital signal.

* * * * *