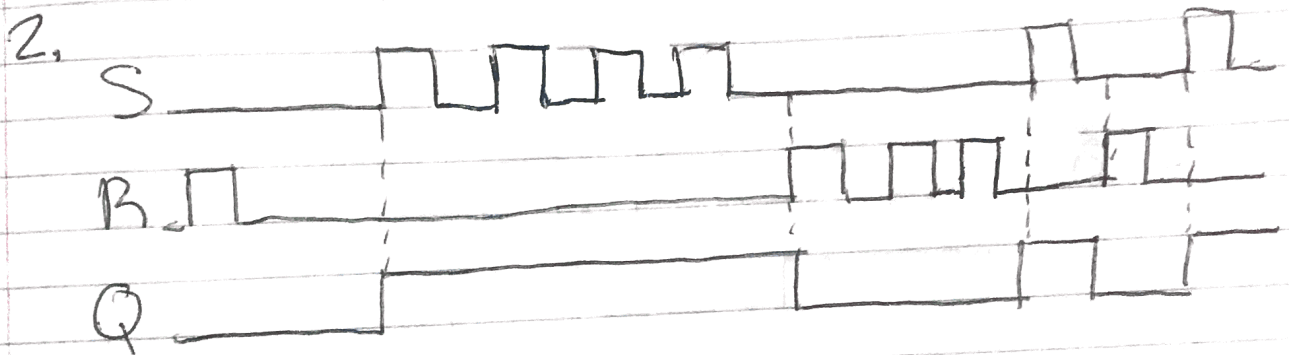
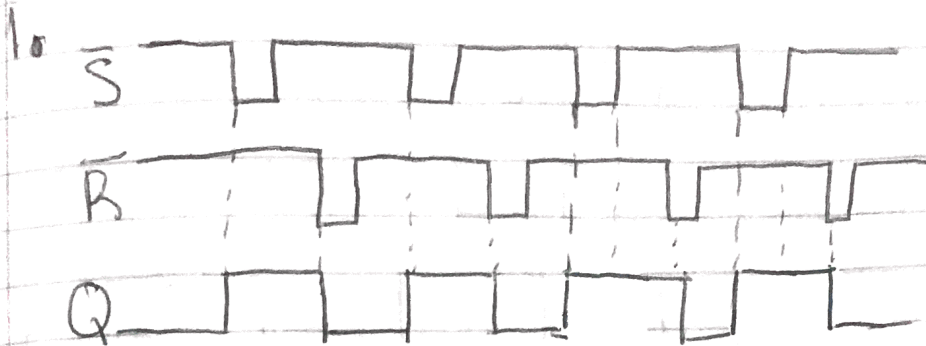
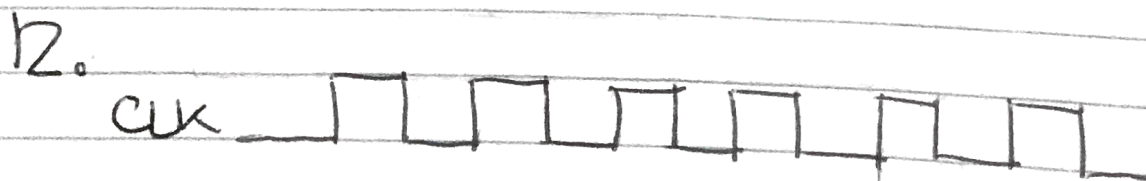
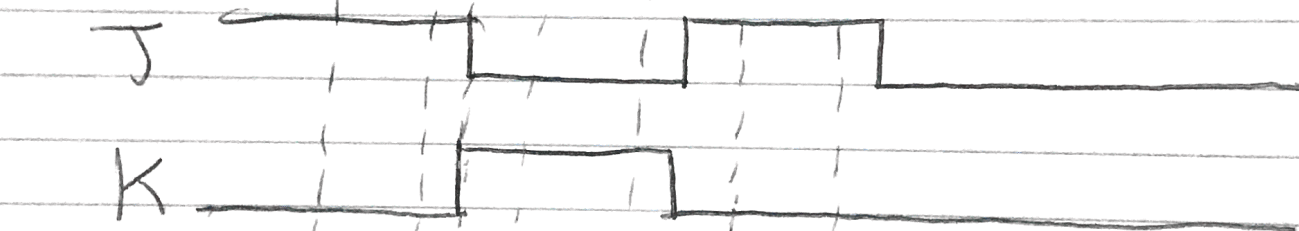


# Chapter 7 - Homework #5

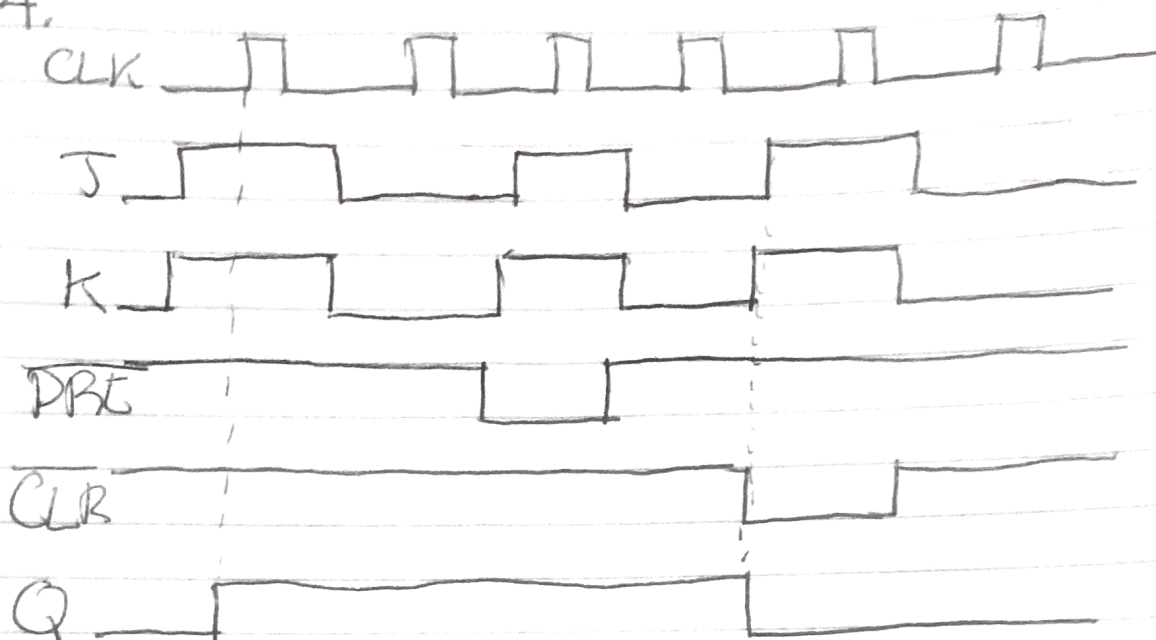


7. D Clock Q  $\bar{Q}$

1	↑	1	0	→ Set
0	↑	0	1	→ Reset



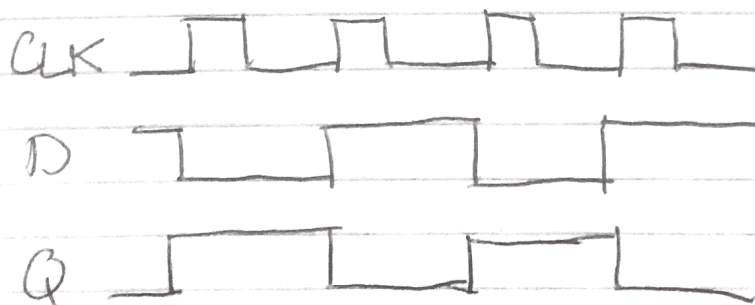
14.



21,  $t_w = 67 \text{ ns}$

$$f_{\max} = \frac{1}{67 \times 10^{-9} \text{ s}} = 0.0149 \times 10^9 \text{ Hz} = \boxed{14.9 \text{ MHz}}$$

25.



Since D has half the frequency of the clock signal, this is a divide by 2 frequency divider.