

Homework 5 Solutions for Computer Logic and Circuit Design: PHYS306/COSC330

Dr. Jordan Hanson - Whittier College Dept. of Physics and Astronomy

April 26, 2020

1 7-1: Latches

- Exercise 1: The active-LOW SR latch begins in the RESET state, and is SET, RESET, ...

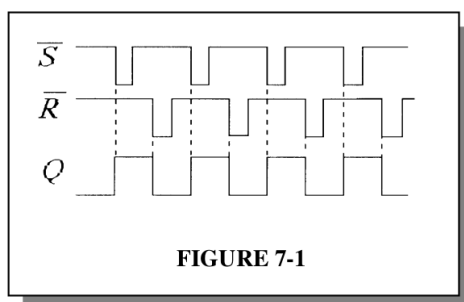


Figure 1: Solution to exercise 1.

- Exercise 2: The SR latch is now active-HIGH. Whenever it's in the SET state and S goes high again, there is no change in the state.

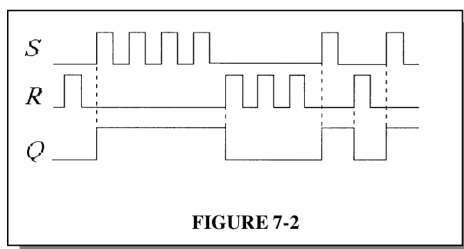


Figure 2: Solution to exercise 2.

- Exercise 4: The key here is that once the latch is SET, it stays set regardless of EN.

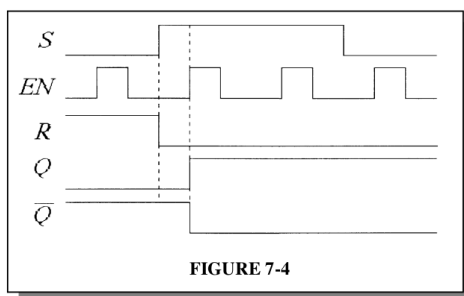


Figure 3: Solution to exercise 4.

- Exercise 7: For Q to be HIGH we need to enable and SET the latch. Once it's set it stays SET until enabled and RESET.

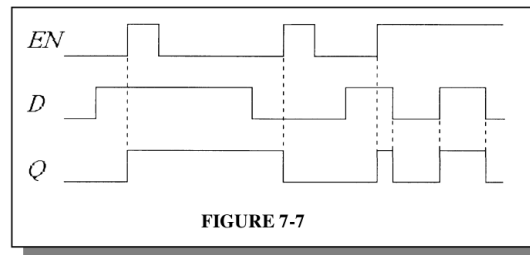


Figure 4: Solution to exercise 7.

2 7-2: Flip-flops

- Exercise 8: The pulse-transition-detector inside each means these are synchronous devices, but (a) triggers on the negative edges and (b) triggers on positive edges of the clock. Each device is SET, RESET, and SET again, however, these transitions line up with the negative or positive edges of CLK.

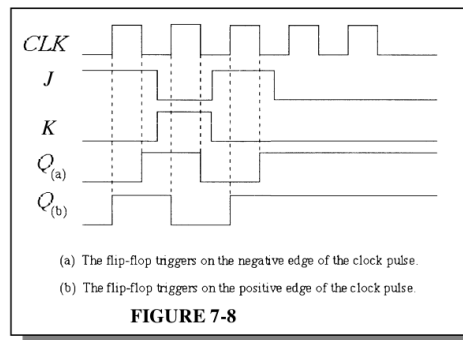


Figure 5: Solution to exercise 8.

- Exercise 12: The D flip-flop is positive edge triggered, and Q follows D only on the right pos edged signals.

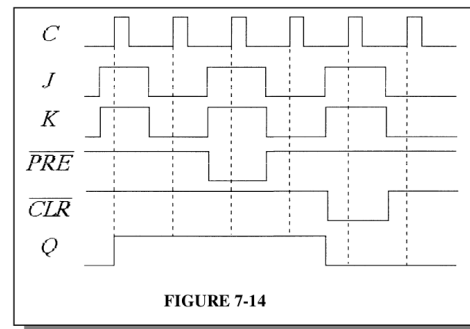
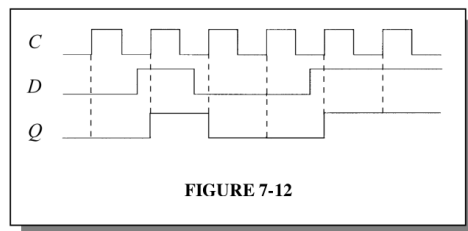


Figure 6: (Left) Solution to exercise 12. (Right) Solution to exercise 14.

- Exercise 14: The J and K inputs act together, alternatively toggling and indicating no-change. However, when the preset signal is active-LOW, the JK flip-flop is SET, and when the clear signal is active-LOW, the unit is RESET.

3 7-3: Flip-flop operating characteristics

- Adding the two numbers gives the minimum period of 67 ns. Inverting the number gives the frequency: $1/(67 \text{ ns}) = 0.0149 \text{ GHz} = 14.9 \text{ MHz}$.

4 7-4: Flip-flop Applications

1. Exercise 25: Because the flip-flop has to wait until the next posedge to go HIGH after the \bar{Q} output RESETs it, the Q output remains high for a clock cycle and low for a subsequent clock cycle. Thus, this is a frequency divider (by 2).

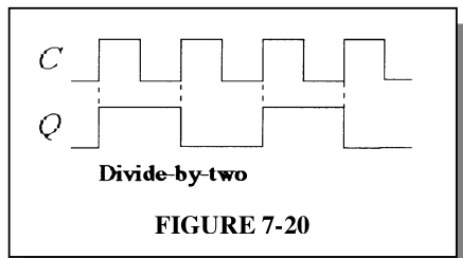


Figure 7: The solution to exercise 25.