

Study Guide for Midterm 1

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1 Chapter 1 - Introductory Concepts

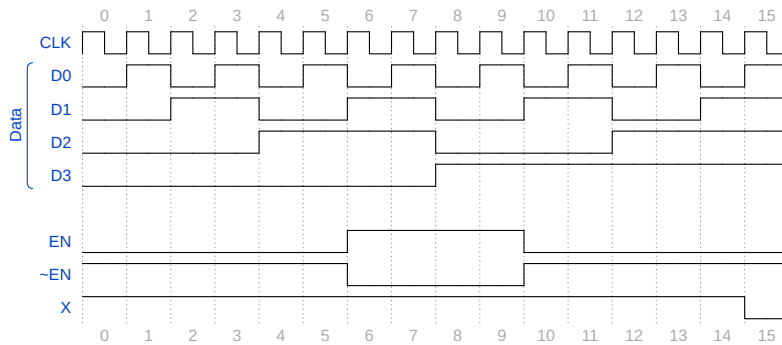


Figure 1: A timing diagram including a clock signal (CLK), a 4-bit parallel data stream (D0-D3), and enable/disable signals (EN/ \sim EN).

1. Consider Fig. 1. (a) What is the duty cycle of each D_i signal? (b) Consider the bitstreams of D_i . What does the sequence of numbers represent?
 - All duty cycles are 50%
 - This is a 4-bit counter
2. (a) Imagine that D_i signals enter a NAND gate, along with the \sim EN signal. Draw the resulting timing diagram.

See Fig. 1, with the output X.

3. Suppose D_i represents parallel data with a clock frequency of 4 MHz. (a) What is the total bitrate (bits per second)? (b) What would be the bit rate if the system was serial instead of parallel?
 - 16 Mbps (16 MHz)
 - 4 Mbps (4 MHz)

2 Chapter 2 - Number Systems, Operations, and Codes

1. Convert to binary: (a) 1024 (decimal) (b) 0xB BBB (hex) (c) -2048 (decimal)
 - 0100 0000 0000
 - 1011 1011 1011 1011
 - 2's complement: 1000 0000 0000 ... ends up the same representation unless you add leading 0's. Also correct to use a sign bit.
2. Convert to hex: (a) 65535 (decimal) (b) 1000100010001000 (binary)
 - 0xFFFF
 - 0x8888
3. Convert to *octal*, in which **the base is 8**: 1024 (decimal)
 - 0o2000

4. Consider the gray code angular encoder in Fig. 2. (a) If the shaft rotates 180 degrees, how many bit changes occur? (b) If it rotates 180 degrees, and the initial gray code is 0000, what is the final gray code? (c) With 4-bit gray code, how many distinct angles can the shaft encode? What is 360 degrees divided by this number (i.e. the angular precision)? (d) What would be the angular precision of an 8 bit encoder?
- 7 bit changes
 - 0100 (7 in gray code)
 - 16, 22.5 degrees
 - 1.4 degrees

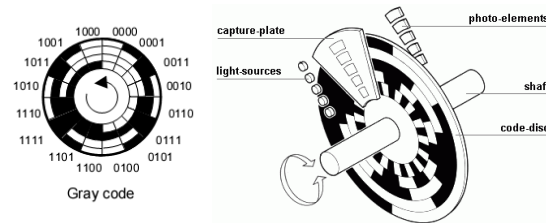


Figure 2: A gray code shaft encoder, or angular encoder, reports the angular position of an object digitally, using the gray code.

3 Chapter 3 - Logic Gates

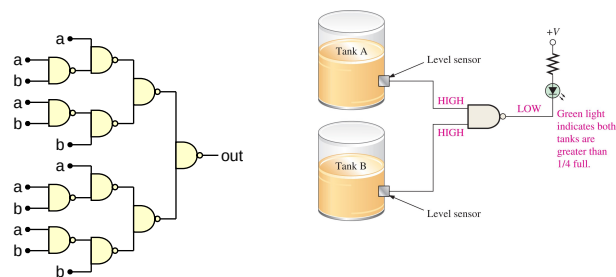
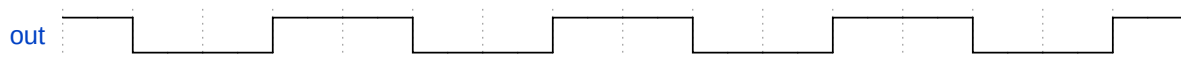


Figure 3: (Left) A logic gate combination. (Right) A liquid tank-level system built from a NAND gate.

1. Generate the simplified logic expression and truth table for Fig. 3, left. What do you call this type of gate?
 - $out = (\bar{a} + b)(a + \bar{b})$
 - XNOR gate
2. Suppose signals D_0 and D_1 in Fig. 1 are connected to a and b in Fig. 3, left. Generate the timing diagram for out .



3. **Creative design:** A liquid tank system is depicted in Fig. 3. The sensors are HIGH when the liquid is above the level (green ON). (a) Create a red LED system that activates when both tanks are *below* the level, and draw it below. (b) Create a yellow LED system that activates when one tank is below and one tank is above the level. (c) Add a third tank with more liquid, and two pipes guiding liquid to tank A and B. Each pipe should have a valve. Add logic that opens the correct valve so as to fill only the low tank until it is no longer below the level.

- An OR gate with a pull-up resistor connected in series with a red LED. If S1 and S2 are LOW, then the red LED will light. Could also be a NOR gate on the high side of the LED.
- S1 and S2 input to a XOR gate. Output connected to a resistor and yellow LED in series to GND.
- Sensors open valve when they receive a HIGH, and there is an inverter between S1 and its value, and an inverter between S2 and its valve.

4 Chapter 4 - Boolean Algebra and Logic Simplification

- Suppose an investment firm holds stock shares in four different stocks within a portfolio, labled A through D. The companies corresponding to stocks A through D are labeled *inactive* or *active* by the firm, based on information about their productivity. The firm notices that the portfolio output is *on* (rising) under the following conditions:
 - All four companies are inactive, or ...
 - Companies A through C are inactive, while company D is active, or ...
 - All companies are active, or ...
 - Companies A through C are active, while company D is inactive.

(a) Develop a S-SOP expression for X , the portfolio's state (on or off) based on the data above. (b) Use a domain-4 Karnaugh map to simplify the S-SOP expression. (c) Which stock appears to be irrelevant to the state of the portfolio?

- $X = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + ABCD + ABC\bar{D}$
- $X = \bar{A}\bar{B}\bar{C} + ABC$. The Karnaugh map has two 1's in the upper left, and two 1's in the lower right, forming two S-SOP terms.
- The D stock is irrelevant to the state of X .

- A circuit contains three main branches leading to one output. The output is observed to fail under the following conditions below. (a) Use the domain-3 Karnaugh map to determine the conditions under which it does succeed, and write an S-SOP expression for the circuit. (b) Draw the circuit using gates.

- A: false, B: false, C: false
- A: false, B: true, C: false
- A: true, B: true, C: false
- A: true, B: false, C: false
- A: false, B: true, C: true
- A: true, B: true, C: true
- The domain-3 Karnaugh map has two true states: upper right corner and lower-right corner. $X = \bar{B}C$.
- B goes into an inverter, then an AND, along with C.

5 Chapter 5 - Combinatorial Logic Analysis

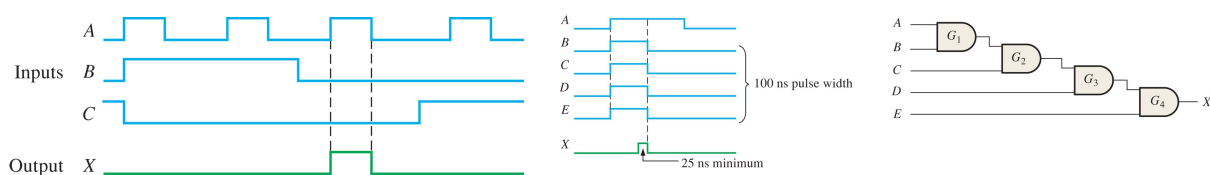


Figure 4: Diagrams for Sec. 5. (Left) Inputs are ABC, and the output is X. (Right) The inputs are ABCDE, and the output is X.

- For the input waveforms shown in Fig. 4 (left), what logic circuit will generate the output waveform?

$X = A\bar{B}\bar{C}$ (Two inverters: one for B, one for C. One 3-input AND gate.)

- Bonus:** Assuming a propagation delay of 10 ns through each gate in Fig. 4, determine if the *desired* output waveform X will be generated. The desired output is a pulse with a minimum width of 25 ns.

Yes, the waveform will be wide enough given the propagation delays in the gates.