Thursday Reading Assessment: Chapter 7

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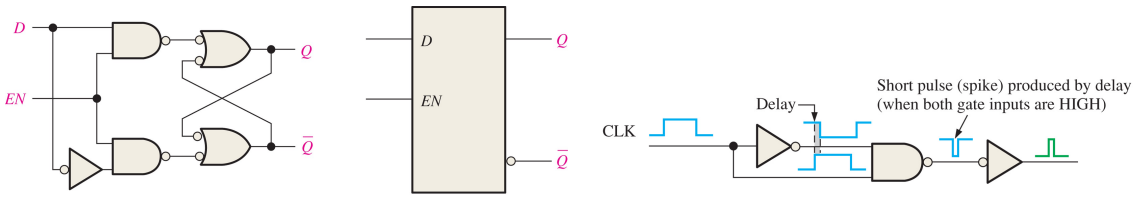

Figure 1: (Left) A gated D-latch system expressed in terms of NAND gates. (Right) A pulse transition detector.

1 Latches, Flip-Flops, and Timers: Gated D-latch

1. (a) Produce the full truth table of the circuit in Fig. 1 (left) for the inputs EN and D, and the outputs Q and $\bar{Q}$. Remember to write NC for "No Change." (b) Create a timing diagram that enables the D-latch and passes the bitstream 10101010 from D to Q, and then disables the D-latch. What is the final state of the D-latch?

2 Latches, Flip-Flops, and Timers: Pulse Transition Detector

1. (a) Produce the truth table for the **pulse transition detector** in Fig. 1 (right). Assume the input states are constant values. (b) If there is a 5 ns propagation delay in the initial inverter, what is the final pulse width? (c) Introduce logic components to make the final pulse width 15 ns.