Study Guide for Midterm 1

Dr. Jordan Hanson - Whittier College Dept. of Physics and Astronomy

March 24, 2020

1 Chapter 1 - Introductory Concepts

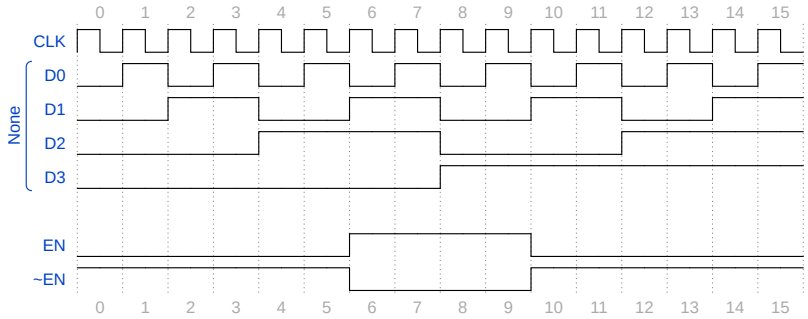

Figure 1: A timing diagram including a clock signal (CLK), a 4-bit parallel data stream (D0-D3), and enable/disable signals (EN/∼EN).

1. Consider Fig. 1. (a) What is the duty cycle of each $D_{\rm i}$ signal? (b) Consider the bitstreams of $D_{\rm i}$. What does the sequence of numbers represent?

2. (a) Imagine that D_i signals enter a NAND gate, along with the ∼EN signal. Draw the resulting timing diagram.

3. Suppose D_i represents parallel data with a clock frequency of 4 MHz. (a) What is the total bitrate (bits per second)? (b) What would be the bit rate if the system was serial instead of parallel?

2 Chapter 2 - Number Systems, Operations, and Codes

1. Convert to binary: (a) 1024 (decimal) (b) 0xBBBB (hex) (c) -2048 (decimal)

2. Convert to hex: (a) 65535 (decimal) (b) 1000100010001000 (binary)

3. Convert to *octal*, in which **the base is 8**: 1024 (decimal).

4. Consider the gray code angular encoder in Fig. 2. (a) If the shaft rotates 180 degrees, how many bit changes occur? (b) If it rotates 180 degrees, and the initial gray code is 0000, what is the final gray code? (c) With 4-bit gray code, how many distinct angles can the shaft encode? What is 360 degrees divided by this number (i.e. the angular precision)? (d) What would be the angular precision of an 8 bit encoder?

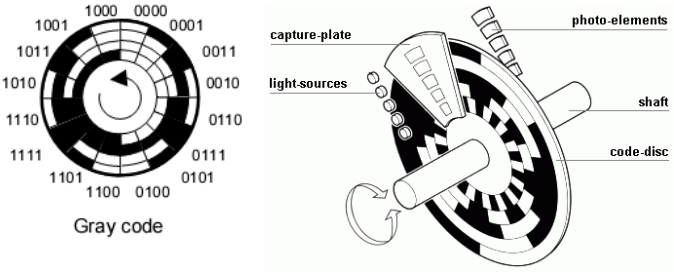

Figure 2: A gray code shaft encoder, or angular encoder, reports the angular position of an object digitally, using the gray code.

3 Chapter 3 - Logic Gates

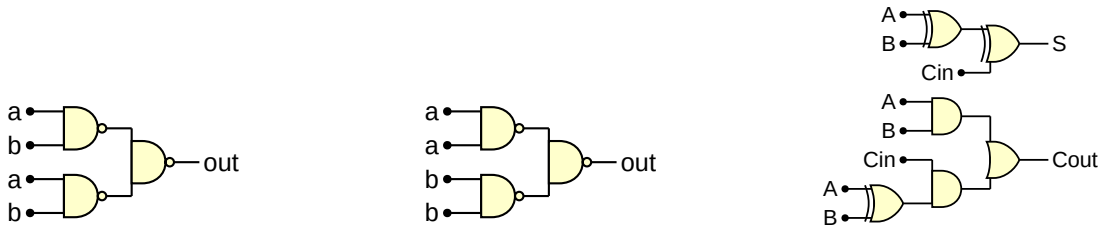

Figure 3: Examples of logic gate combinations.

1. Generate the truth tables for the gate diagrams in Fig. 3. Pay attention to the domain.

2. Identify the actions of the gate combinations in the previous problem from the truth tables. (a) Fig. 3, left:_____ (b) Fig. 3, middle:_____ (c) Fig. 3, right:_____.

3. Suppose the signals in Fig. 4 are fed into the circuit in Fig. 3, right. Fill in the S and Cout signals in Fig. 4.

4. Imagine a system for an electronic door lock which requires two electronic keys (two signals), S1 and S2. The circuit has a red LED, a yellow LED, and a green LED. The system unlocks when the output LOCK signal is LOW, caused by a LOW S1 and a LOW S2. The red LED is activated when S1 and S2 are both HIGH. The yellow LED is activated when S1 and S2 are different. The green LED is activated when the system is unlocked. *By default, S1 and S2 are HIGH.* Draw the solution below.

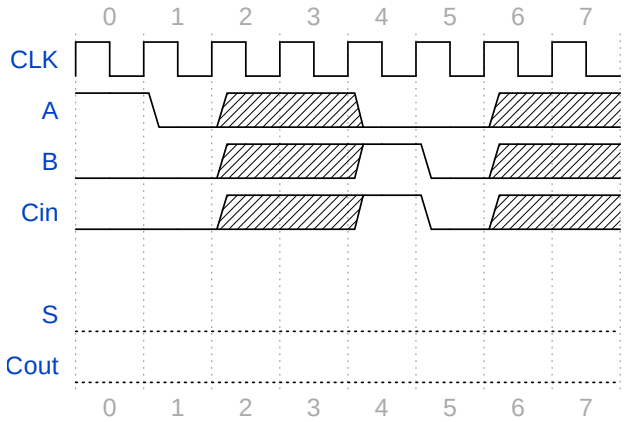

Figure 4: An example timing diagram for Fig. 3, right. The shaded regions indicate "don't care" conditions, or times when the data is not relevant.

4 Chapter 4 - Boolean Algebra and Logic Simplification

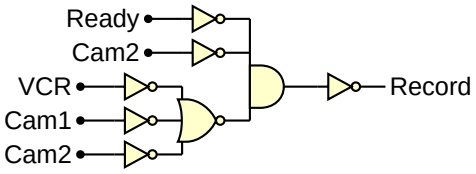

Figure 5: A gate combination triggering a signal named "record."

1. Consider the circuit in Fig. 5. (a) Write a logic expression for *Record*. (b) Simplify the expression to as minimal a form as possible. (c) Are any signals or gates unnecessary?

2. Consider again the logic expression that represents the circuit in Fig. 5. (a) Write the corresponding domain-4 Karnaugh map. (b) Use the Karnaugh map to produce the S-POS expression and truth table.

5 Chapter 5 - Combinatorial Logic Analysis

1. (a) Draw the circuit corresponding to the timing diagram in Fig. 6. (b) Create the Karnaugh map. (c) Using the Karnaugh map, write the simplest expression for this logic function and re-draw the circuit.

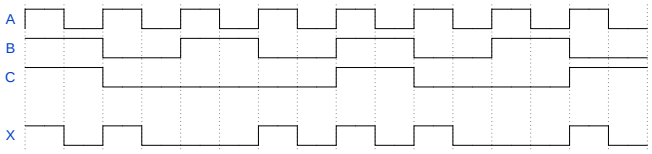

Figure 6: Timing diagram for Sec. 5.