

1 Chapter 1 - Introductory Concepts

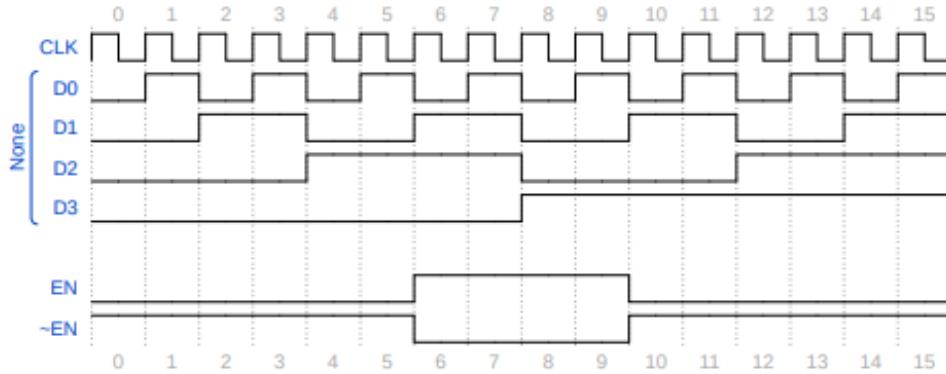


Figure 1: A timing diagram including a clock signal (CLK), a 4-bit parallel data stream (D0-D3), and enable/disable signals (EN/~EN).

$$0 \rightarrow 15 = 16$$

1. Consider Fig. 1.

(a) What is the duty cycle of each Di signal?

$$D0: 8/16 = 0.5 \times 100 = \mathbf{50\% \text{ duty cycle}}$$

$$D1: 8/16 = 0.5 \times 100 = \mathbf{50\% \text{ duty cycle}}$$

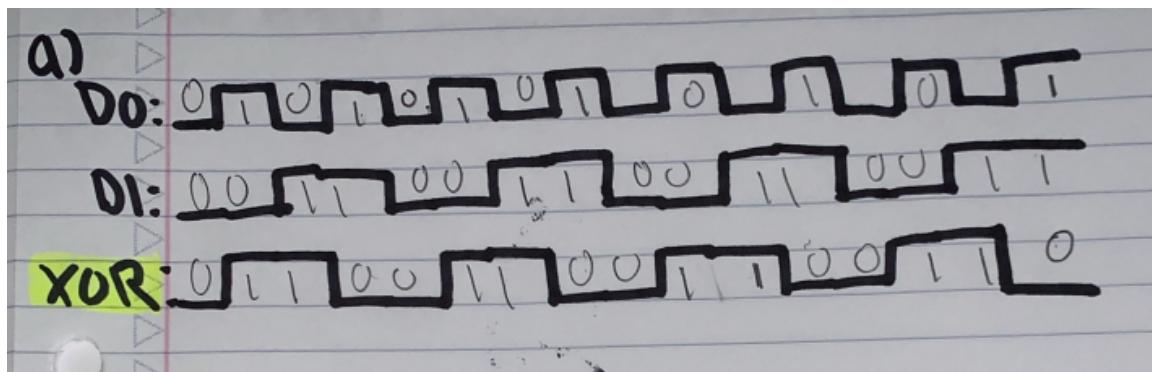
$$D2: 8/16 = 0.5 \times 100 = \mathbf{50\% \text{ duty cycle}}$$

$$D3: 8/16 = 0.5 \times 100 = \mathbf{50\% \text{ duty cycle}}$$

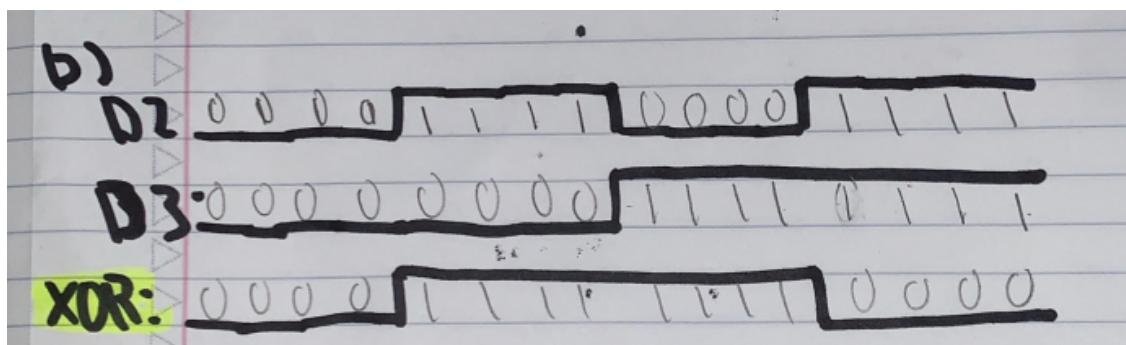
(b) Consider the bitstreams of Di. What does the sequence of numbers represent?

The sequence of numbers seems to be that of the binary counting sequence. It reminds me of a 4 input truth table similar to examples from class.

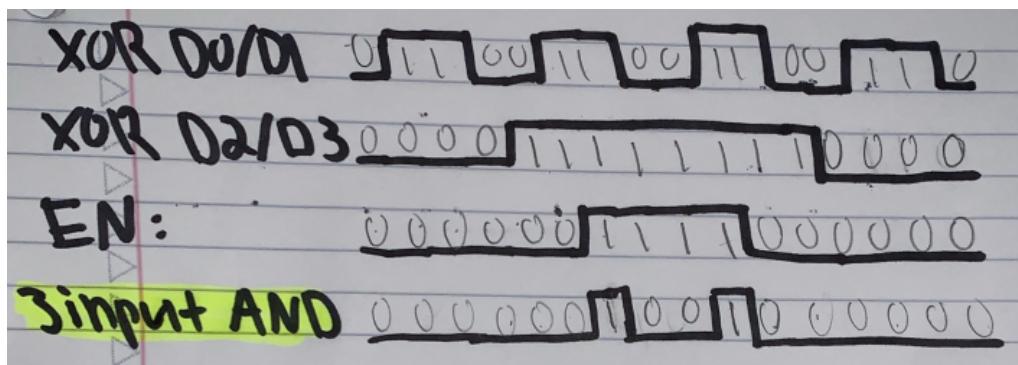
2. (a) Create the timing diagram representing the output of an XOR gate with D0 and D1 as inputs.



(b) Do the same for D2 and D3.



(c) Finally, create the timing diagram representing the output of a 3-input AND gate with the XOR gates from parts (a) and (b), and the EN signal as inputs.



3. Suppose D_i represents parallel data with a clock frequency of 4 MHz. (a) What is the total bitrate (bits per second)?

$D_0 \rightarrow D_3 = 4$ Data lines

4MHz x 4 = 16 Mbps

(b) What would be the bit rate if the system was serial instead of parallel?

4MHz=4Mbps

It would be 4Mbps if it was serially.

2 Chapter 2 - Number Systems, Operations, and Codes

1. Convert to binary:

(a) 1024 **0100 0000 0000**

(b) 0xB BBBB

$B = 11 \rightarrow 1011 1011 1011 1011$

(c) -2048 -1000 0000 0000

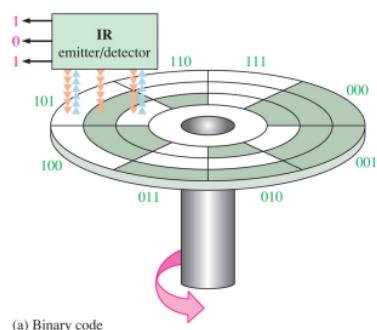
2. Convert to hex:

(a) 65535 **FFFF**

(b) 1000100010001000 **8888**

3. Design problem. Consider the angular shaft encoder in Fig. 2. The IR emitter/detector detects IR light reflected from white sectors, while the dark sectors absorb the light. The sectors are encoded in binary.

For example, starting from inner sectors and reading outward, dark-dark-light is translated to state 001 by the detector. If the shaft rotates 45 degrees, the detector records a state change.



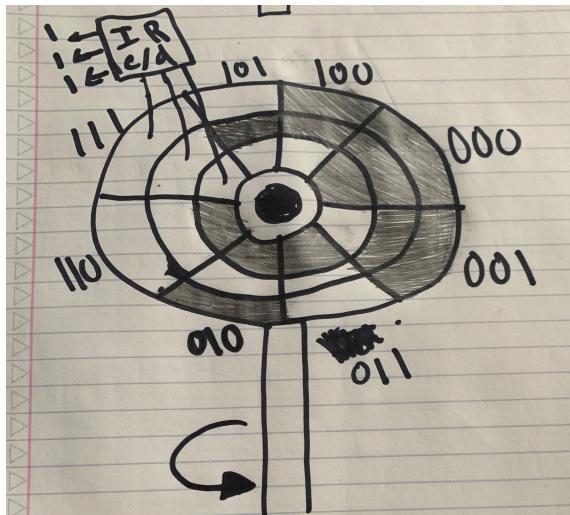
(a) If the initial state is 000 and the shaft rotates 360 degrees, how many bit changes occur?

There will be 8 state changes. Each state change represents a bit change.

(b) How many bit changes would occur if the shaft position was encoded in gray code?

There would still be 8 state changes.

(c) Draw the correct face of the shaft encoder, encoded in 3-bit gray code instead of binary¹



(d) If 45 degrees is the angular precision with 3-bit gray code, what is the angular precision with 8 bit gray code?

$$2^8 = 256$$

$$360/256 = 1.406 \text{ degrees per state}$$

3 Chapter 3 - Logic Gates

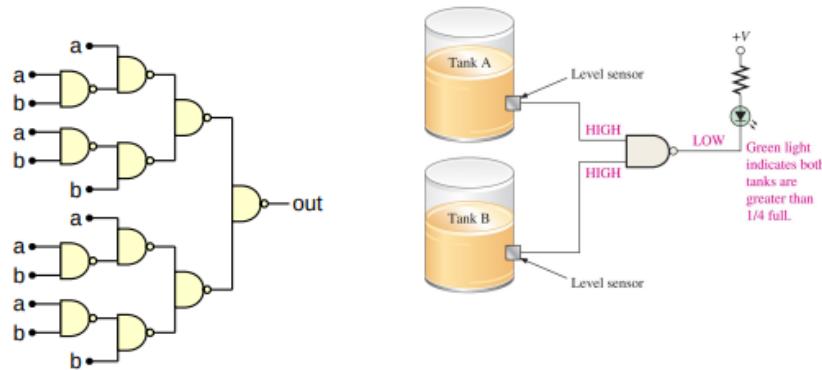


Figure 3: (Left) A logic gate combination. (Right) A liquid tank-level system built from a NAND gate.

1. Generate the simplified logic expression and truth table for Fig. 3, left. What do you call this type of gate?

$$AB = A + B$$

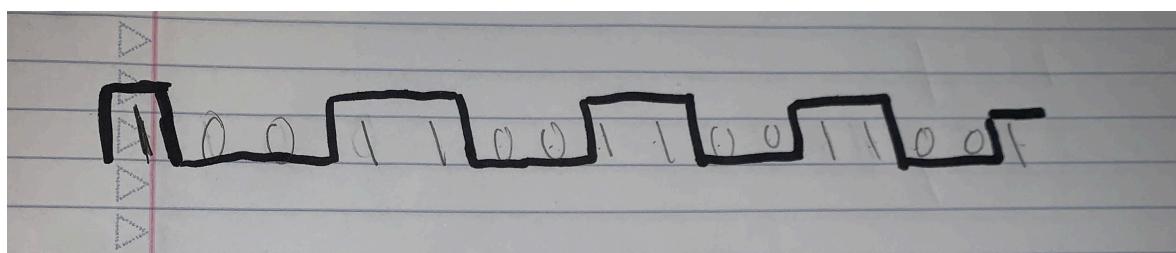
This is a NAND gate

2. Suppose signals D0 and D1 in Fig. 1 are connected to a and b in Fig. 3, left. Generate the timing diagram.

D0 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1

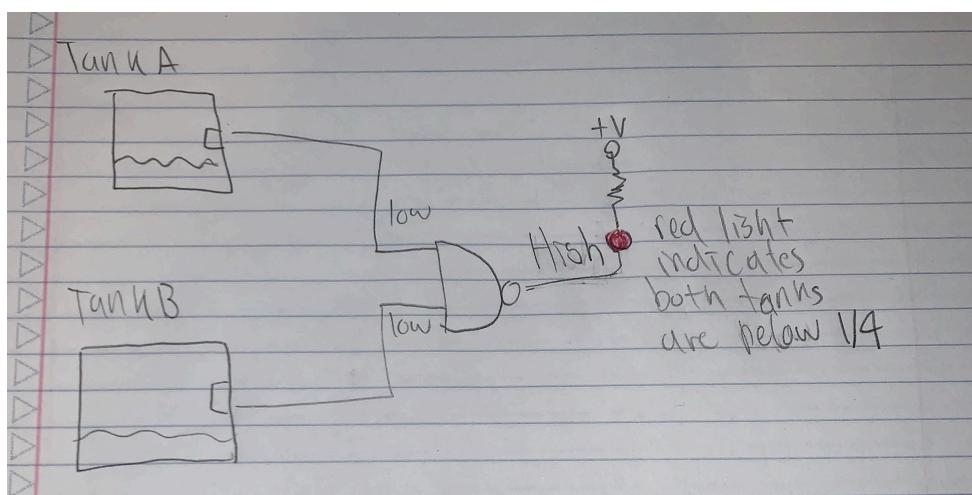
D1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1

Output 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1

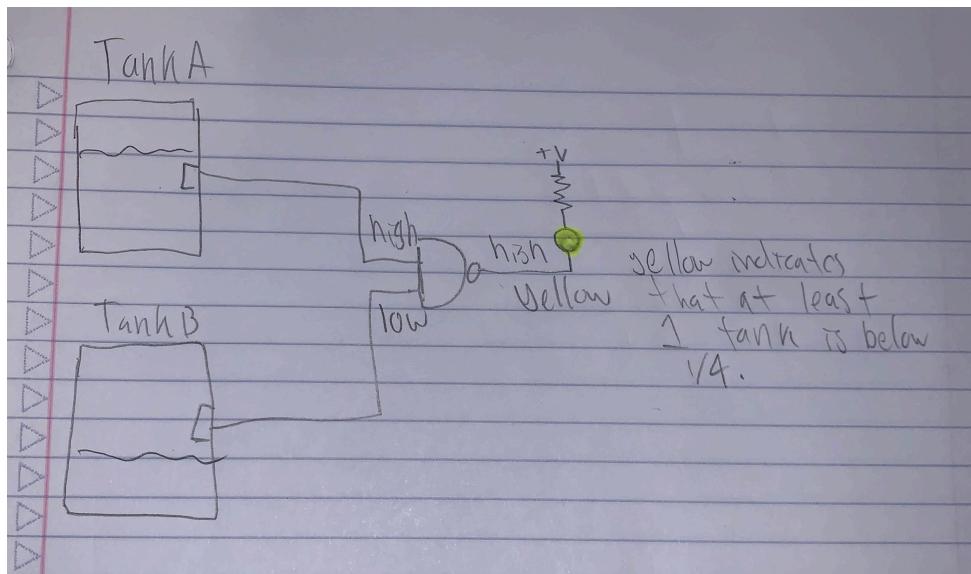


3. Design problem. A liquid tank system is depicted in Fig. 3 (right). The sensors are HIGH when the liquid is above the level.

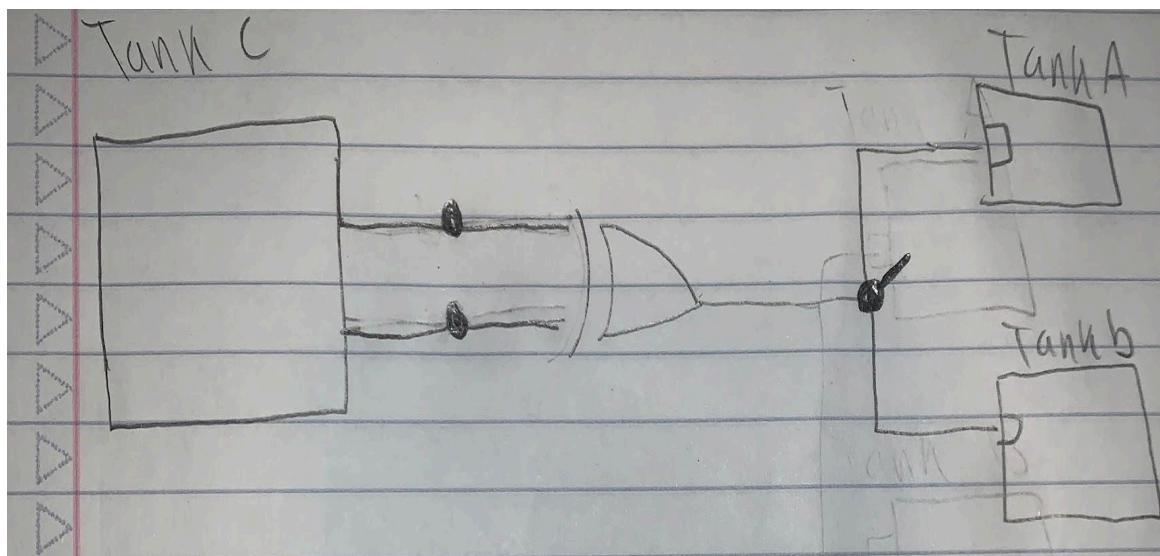
(a) Create and display a red LED system that activates when both tanks are below the level.



(b) Create and display a yellow LED system that activates when one tank is below and one tank is above the level.



(c) Add a third tank with two pipes guiding liquid to tanks A and B. Each pipe should have a valve. Add logic that opens the correct valve so as to fill only the low tank until it is no longer below the level.



4 Chapter 4 - Boolean Algebra and Logic Simplification

1. Suppose an investment firm manages a portfolio with shares in four stocks, labeled A through D. The companies corresponding to stocks A through D are labeled inactive or active by the firm, based on

productivity information. The firm notices that returns (profits) for the portfolio increase under the following conditions:

- All four companies are active, or ...
 - Companies A and B are inactive, while companies C and D are active, or ...
 - Company A is inactive, while companies B, C, and D are active, or ...
 - Company B is inactive, while companies A, C, and D are active.

(a) Develop a S-SOP expression for X , the portfolio's state. If profit is increasing, label the output ON, and label it OFF if profit is decreasing.

(b) Use a domain-4 Karnaugh map to simplify the S-SOP expression.

(c) Based on your analysis, which stock or stocks should be eliminated from the portfolio?

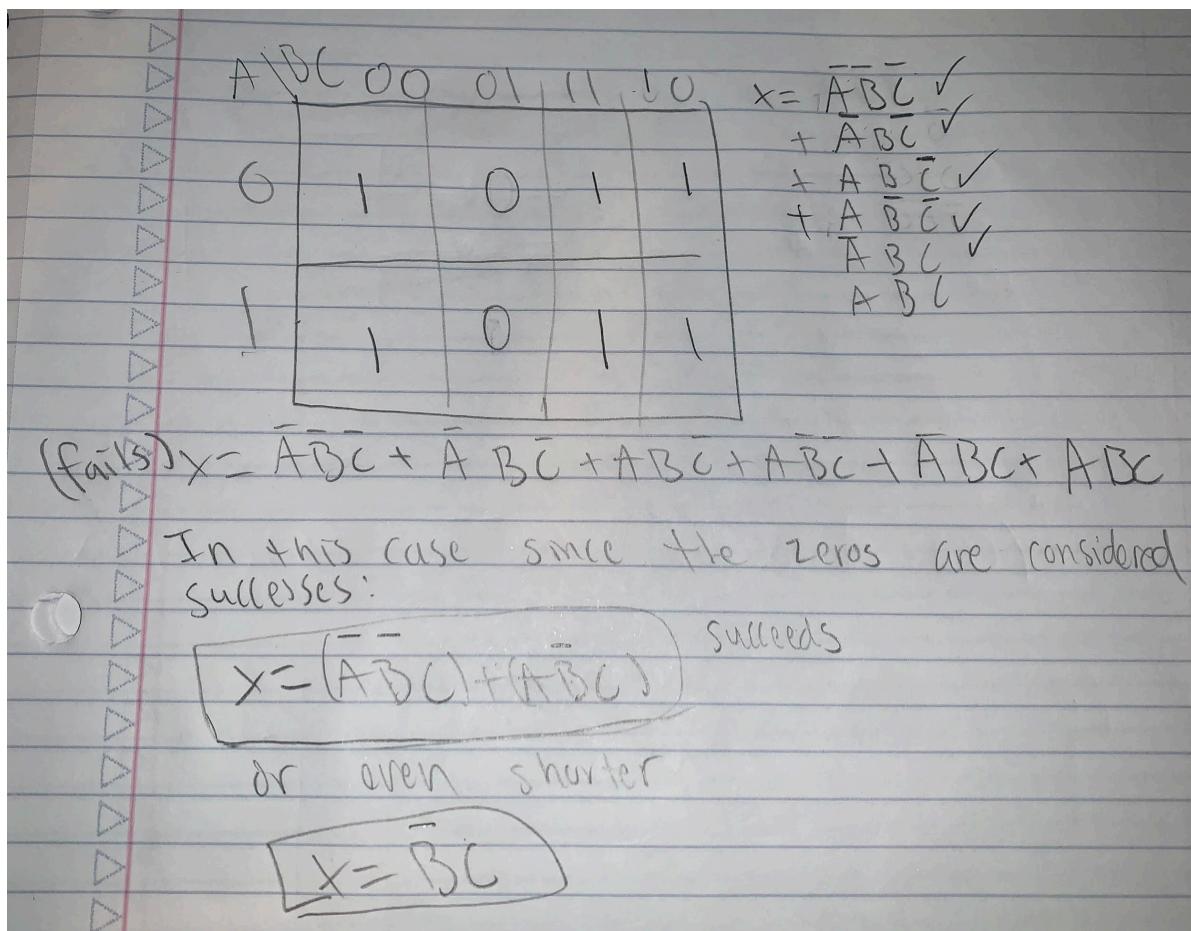
AB should be removed because they do not affect the portfolio

2. A circuit contains three main branches leading to one output. The output is observed to fail under the following conditions below.

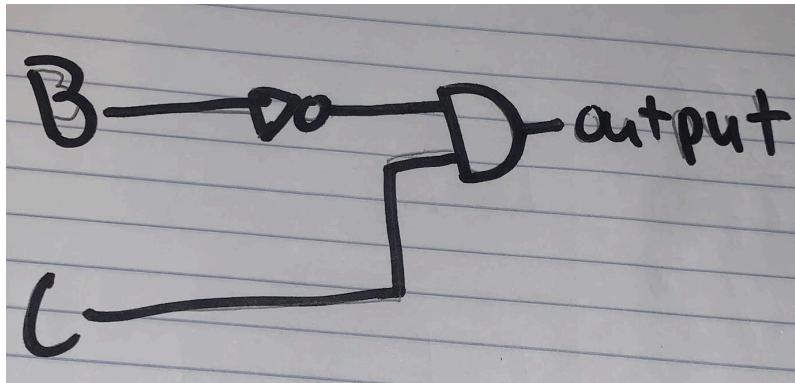
- A: false, B: false, C: false
 - A: false, B: true, C: false

- A: true, B: true, C: false
- A: true, B: false, C: false
- A: false, B: true, C: true
- A: true, B: true, C: true

(a) Use the domain-3 Karnaugh map to determine the conditions under which it does succeed, and write an S-SOP expression for the circuit.

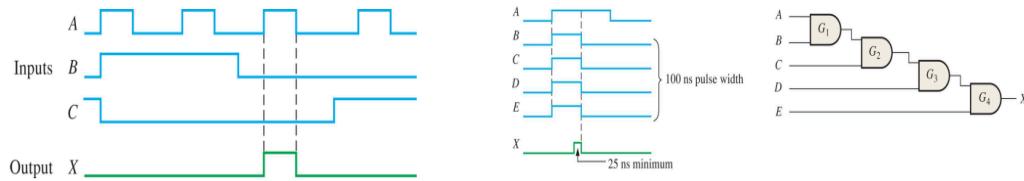


(b) Draw the circuit using gates.

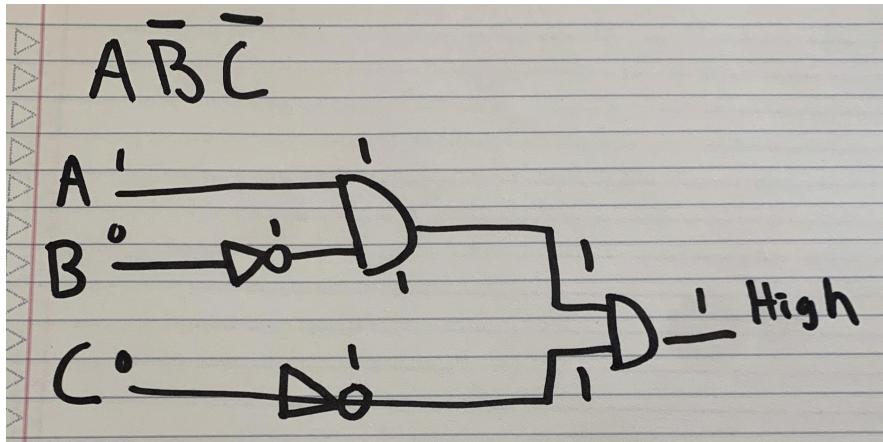


5 Chapter 5 - Combinatorial Logic Analysis

Figure 4: Diagrams for Sec. 5. (Left) Inputs are ABC, and the output is X. (Right) The inputs are ABCDE, and the output is X.



1. For the input waveforms shown in Fig. 4 (left), what logic circuit will generate the output waveform?



2. Bonus: Assuming a propagation delay of 10 ns through each gate in Fig. 4, determine if the desired output waveform X will be generated. The desired output is a pulse with a minimum width of 25 ns.

It cannot. The minimum width must be at least 40ns

$$10\text{ns} \times 4 \text{ gate} = 40\text{ns}$$