Thursday Reading Assessment: Chapter 3-1 through 3-6

Prof. Jordan C. Hanson

February 8, 2024

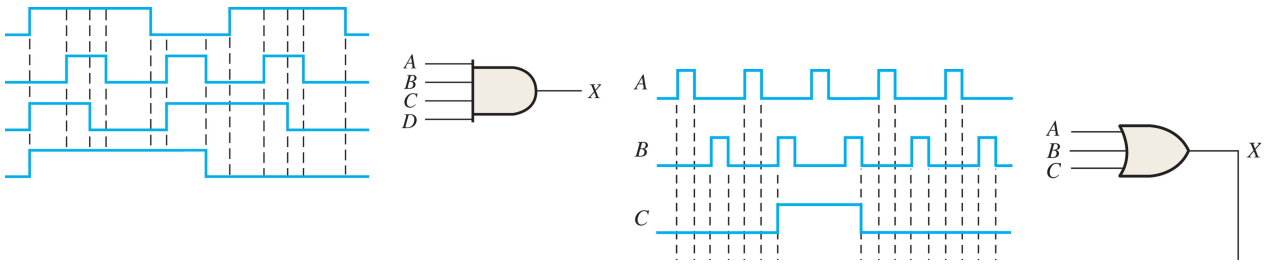

Figure 1: (Left) A timing diagram as input to a 4-input AND gate. (Right) A timing diagram as input to a 3-input OR gate.

1 Logic Gates: AND, OR, NOT

1. Draw the output timing diagram for the 4-input AND gate in Fig. 1 (left).

2. (a) Draw the output timing diagram for the 3-input OR gate in Fig. 1 (right). (b) Add the inverted output to your diagram, as if the output was split off into a NOT gate.

2 Logic Gates: NAND, OR, NOT

1. (a) If both Tank A and B levels in Fig. 2 (left) are below the level sensors, will the green LED be on or off? (b) If both Tank A and B levels in Fig. 2 (right) are above the level sensors, will the red LED be on or off? (c) Write the truth table for the gates in Fig. 2 (left and right).

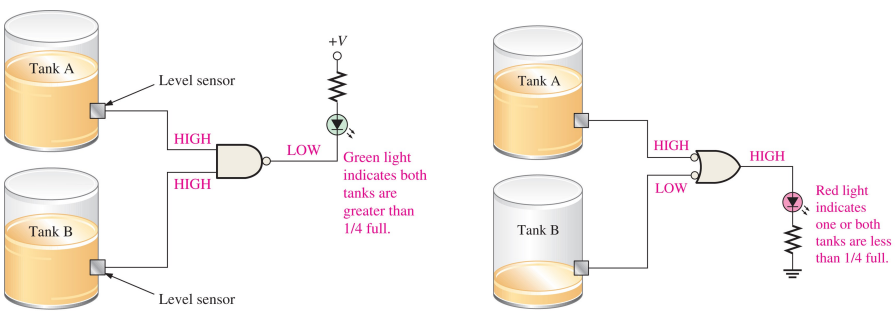

Figure 2: (Left) A timing diagram as input to a 4-input AND gate. (Right) A timing diagram as input to a 3-input OR gate.