6.1

1 a) For max. freq., our period has to min.. But we can't have the period to be less than the delay, otherwise will fail.

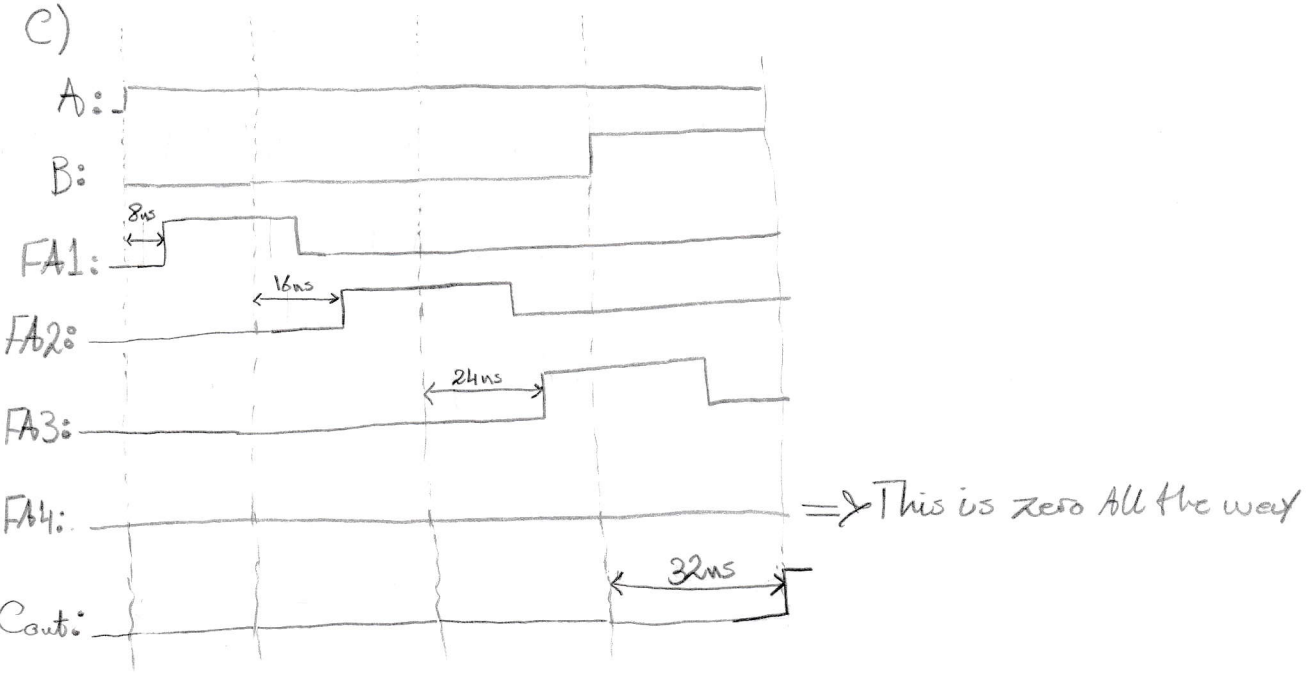
$\therefore P_{min.} = \text{total delay} = 32\,ns$

$\therefore f_{max.} = \frac{1}{P} = \frac{1}{32ns} = 31.25\,MHz.$

b) Delay = 2*(4-bit adder delay) = 2x32ns = 64ns = Pmin

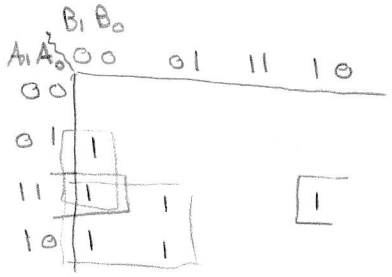
$\therefore f_{max.} = \frac{1}{64ns} = 15.625\,MHz$

c)



*Note: the Carry in is connect to the ground which must have a value of zero, but the Fig. says otherwise which doesn't make sense. My solution is based as if the carry in in the first adder is zero rather than one.

6.2 a) $A > B$

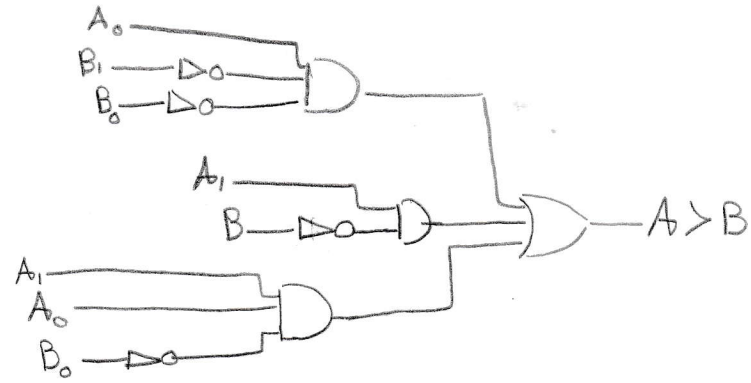


$A_1\ A_0\ B_1\ B_0$: $0\ 1\ 0\ 0 \Rightarrow A_0 \bar{B}_0 \bar{B}_1$

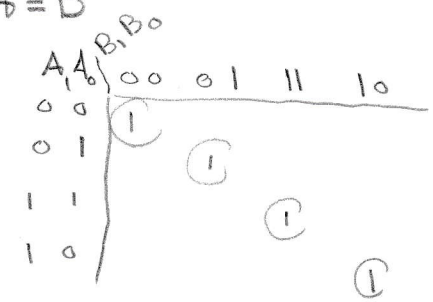
$A_1\ A_0\ B_1\ B_0$: $1\ 1\ 0\ 0$, $1\ 1\ 0\ 1$, $1\ 0\ 0\ 0$, $1\ 0\ 0\ 1$ $\Rightarrow A_1 \bar{B}_1$

$A_1\ A_0\ B_1\ B_0$: $1\ 1\ 0\ 0$, $1\ 1\ 1\ 0$ $\Rightarrow A_0 A_1 \bar{B}_0$

$\therefore$ SOP: $A_0 \bar{B}_0 \bar{B}_1 + A_1 \bar{B}_1 + A_0 A_1 \bar{B}_0$



b) $A = B$

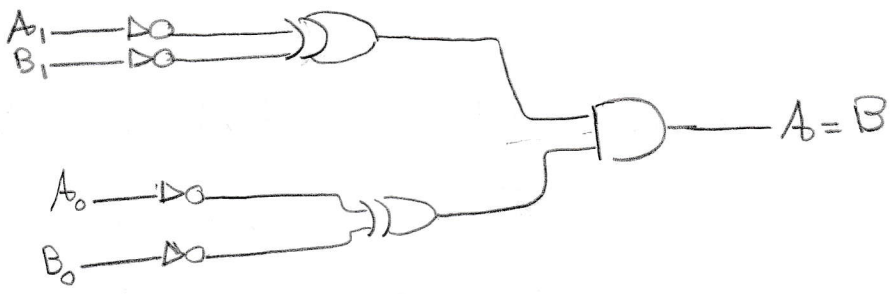


$\Rightarrow \bar{A}_1 \bar{A}_0 \bar{B}_1 \bar{B}_0 + \bar{A}_1 A_0 \bar{B}_1 B_0 + A_1 A_0 B_1 B_0 + A_1 \bar{A}_0 B_1 \bar{B}_0$

$\bar{A}_1 \bar{B}_1 (\bar{A}_0 \bar{B}_0 + A_0 B_0) + A_1 B_1 (A_0 B_0 + \bar{A}_0 \bar{B}_0)$

$(\bar{A}_1 \bar{B}_1 + A_1 B_1)\ (A_0 B_0 + \bar{A}_0 \bar{B}_0)$

$\Rightarrow (\overline{A_1 \oplus B_1})\ (\overline{A_0 \oplus B_0})$

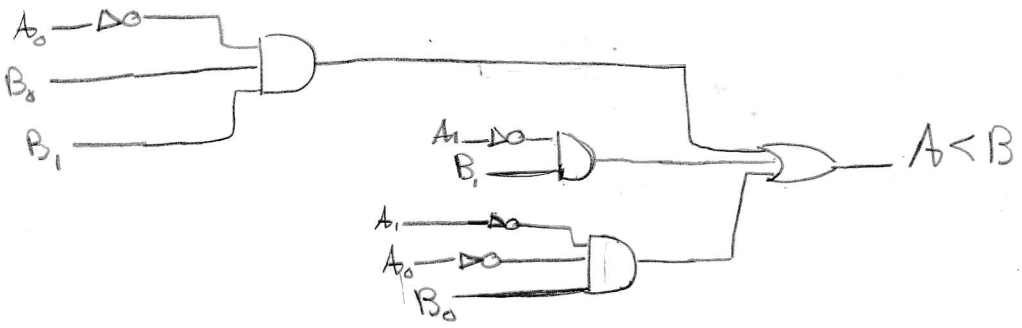


* Note: it would be simpler if we change the XOR to XNOR for part (d).

c) $A<B$ which, logically, is the same as $B>A$.

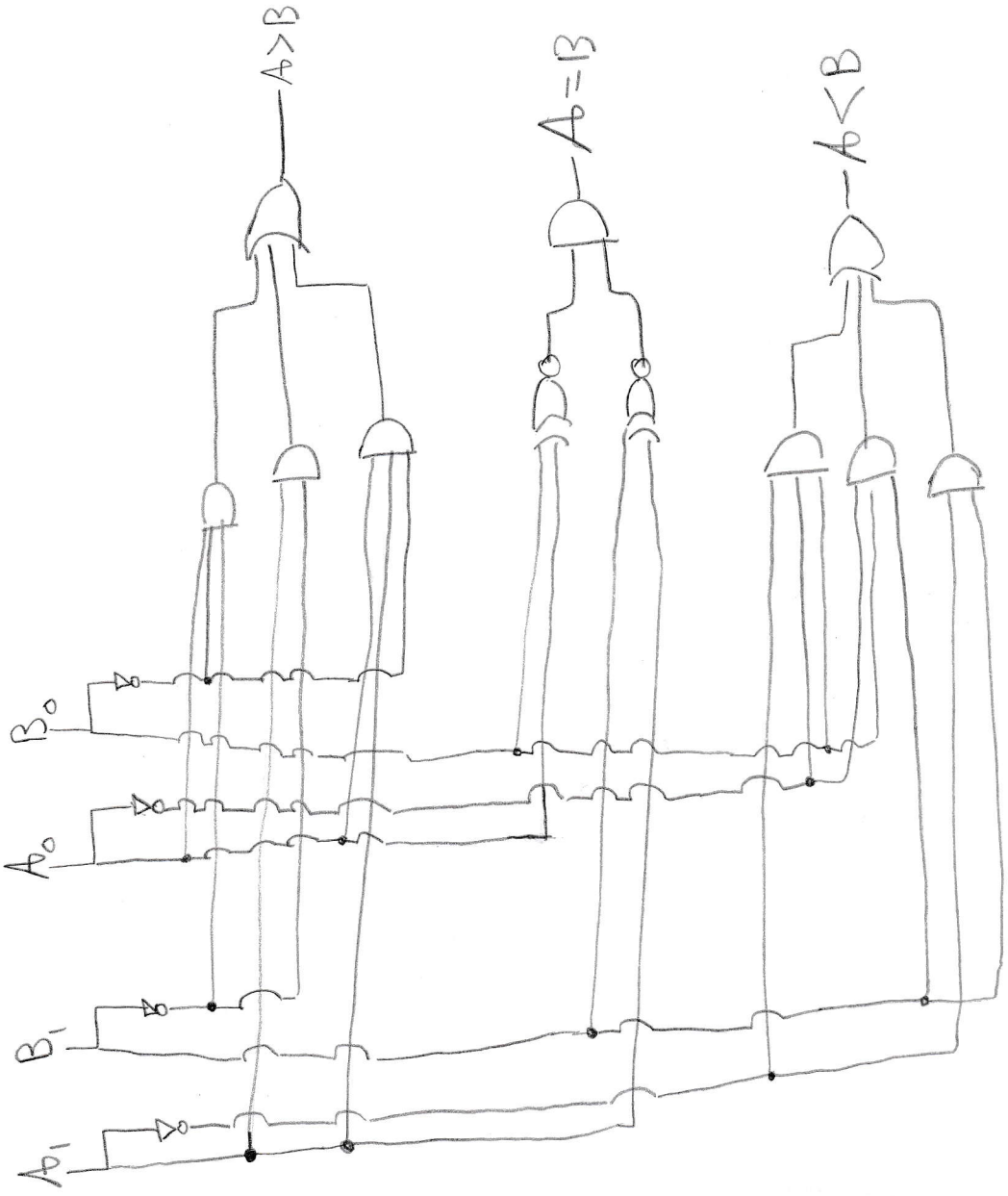
From this logic, we can take our expression in Part (a) and invert its terms as follows:

$$\overline{A_0 \bar{B}_0 \bar{B}_1} + \overline{A_1 \bar{B}_1} + \overline{A_0 A_1 \bar{B}_0} = \bar{A}_0 B_0 B_1 + \bar{A}_1 B_1 + \bar{A}_0 \bar{A}_1 B_0$$



d) In Page 4

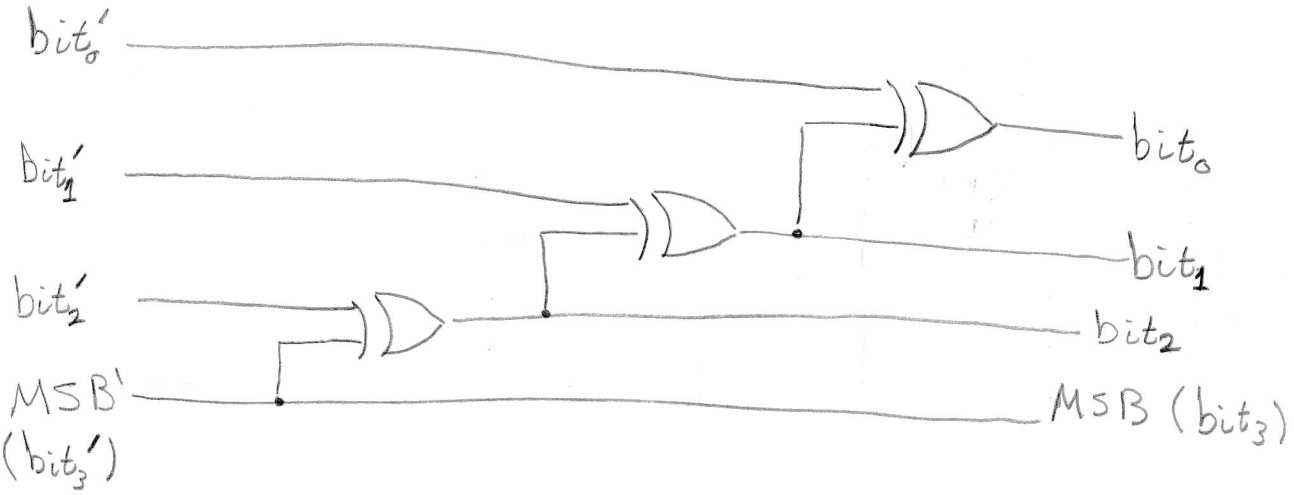
P4



6.3 The logic goes as follows:

The MSB will be the same. Then the third (gray) bit will be XORed with the MSB to give the third binary bit. The second binary bit, however, will carry the previous result and XOR it with the second gray bit as follows:

* Note: Prime symbols is used to indicate gray bits (bit').



6.4 For 4-bit binary, we need 15 hex-bit (not including the "0"), and 16 in total.

Note: Check the truth table which was made via Word Office "attached"

Boolean: $b_3 = h_8 + h_9 + h_{10} + h_{11} + h_{12} + h_{13} + h_{14} + h_{15}$

$b_0 = h_1 + h_3 + h_5 + h_7 + h_9 + h_{11} + h_{13} + h_{15}$

$b_1 = h_2 + h_3 + h_6 + h_7 + h_{10} + h_{11} + h_{14} + h_{15}$

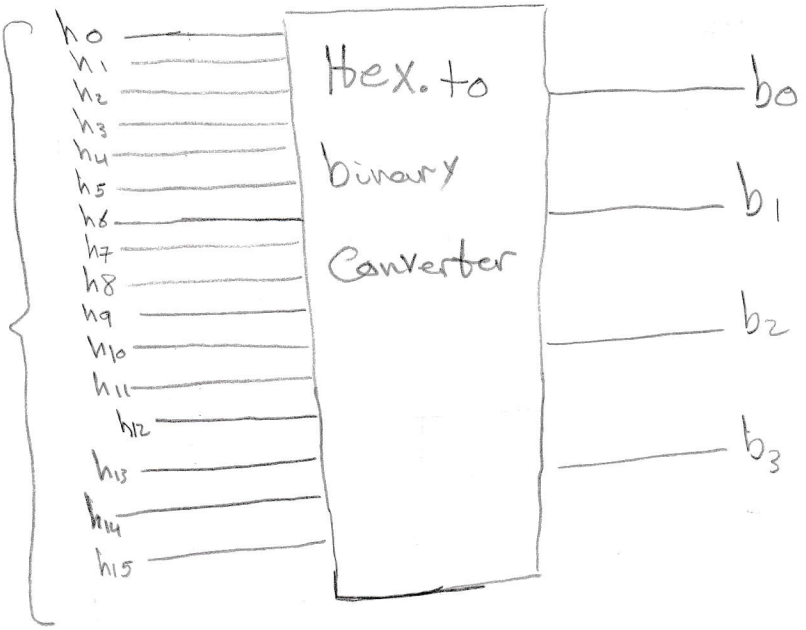
$b_2 = h_4 + h_5 + h_6 + h_7 + h_{12} + h_{13} + h_{14} + h_{15}$

6-4
Continued

Hex	b3	b2	b1	b0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
A=10	1	0	1	0
B=11	1	0	1	1
C=12	1	1	0	0
D=13	1	1	0	1
E=14	1	1	1	0
F=15	1	1	1	1

a) The logic circuit is done via wavedrom.

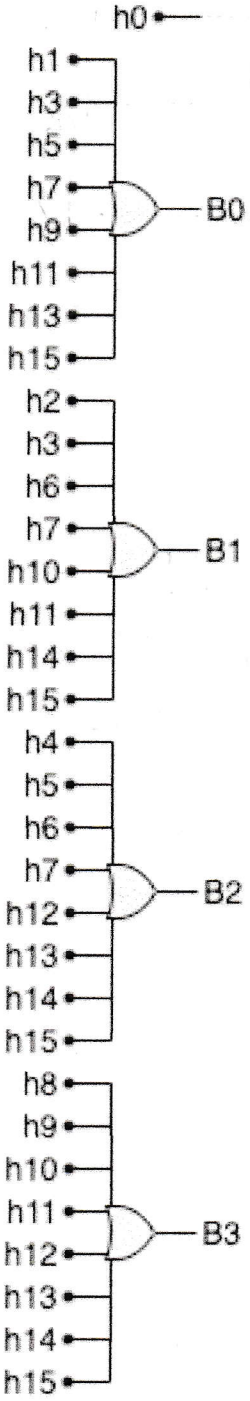
b)



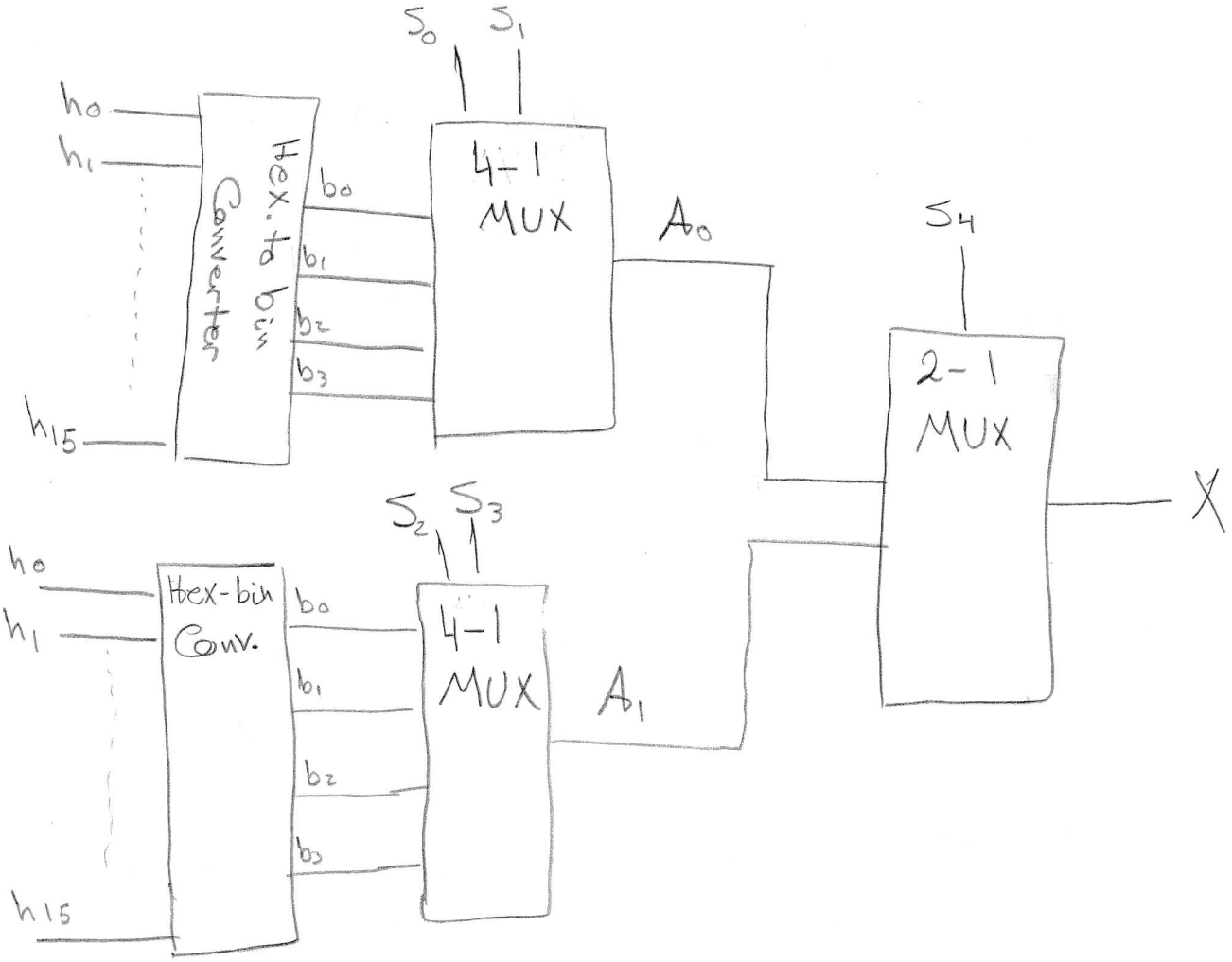
Note: h0 does not go through any gate; thus, it can be pulled out of the decoder.

a) Part 'a': the logic inside Hex-to-bin converter

P7

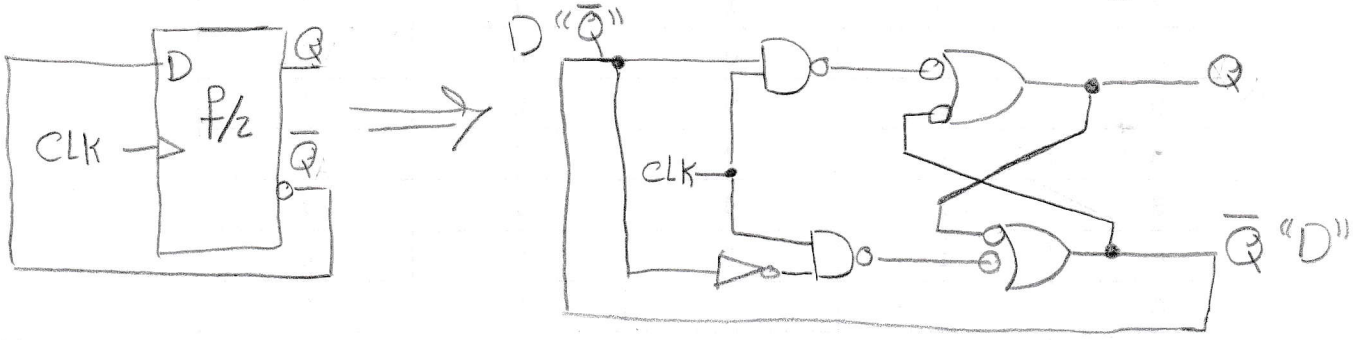


C) This part is very vague, it asks to connect 2 converters which produce 8 input to the MUX. But also, it asks to connect them to 2-1 MUX which, by definition, has 2 inputs only. I came up with a solution that satisfies the above statement, but i don't understant behind it.



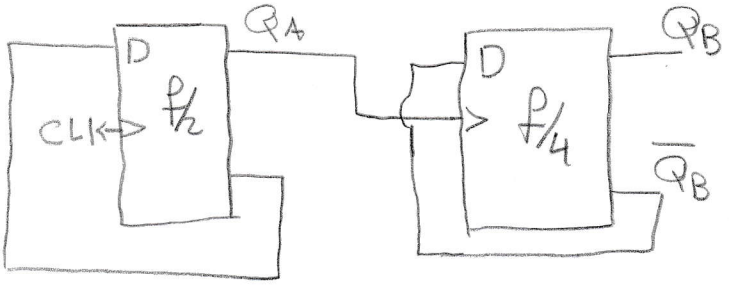
7.1 A frequency divider is basically a 'D' flip-flop with a clock signal. The frequency divided $= 2^n$, where 'n' is the number of flip-flops. $\overline{Q}$ must connect to input 'D'.

a) frequency divided (fd) $= 2^1$, meaning a single flip-flop.

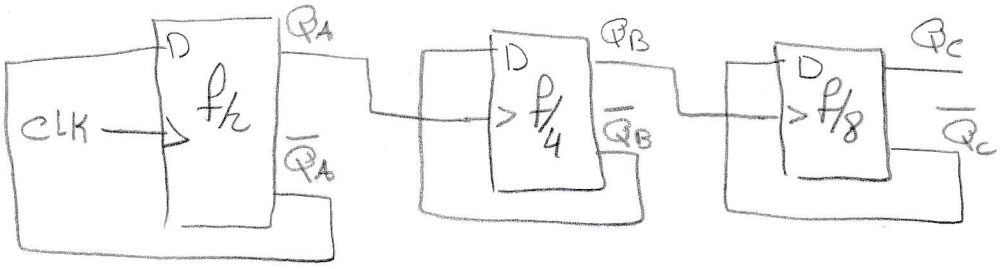


Note: I'll use the sympol from now on for convenience.

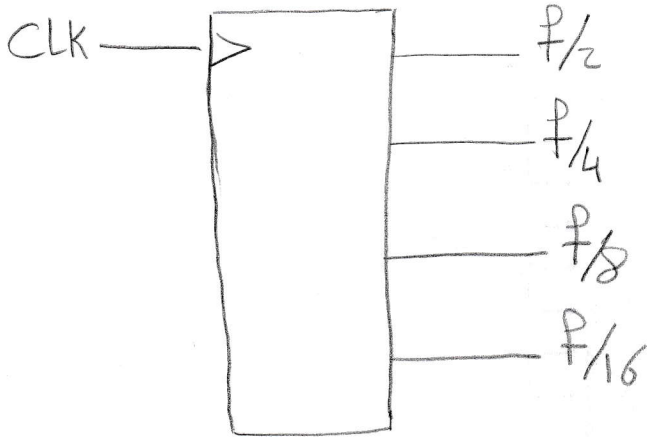
fd $= 4 = 2^2$, two devices.



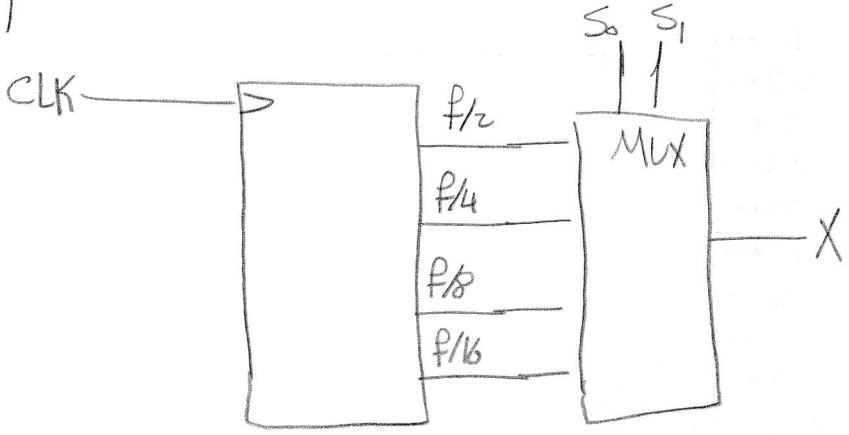
fd $= 8 = 2^3$, three devices.



b)



c)

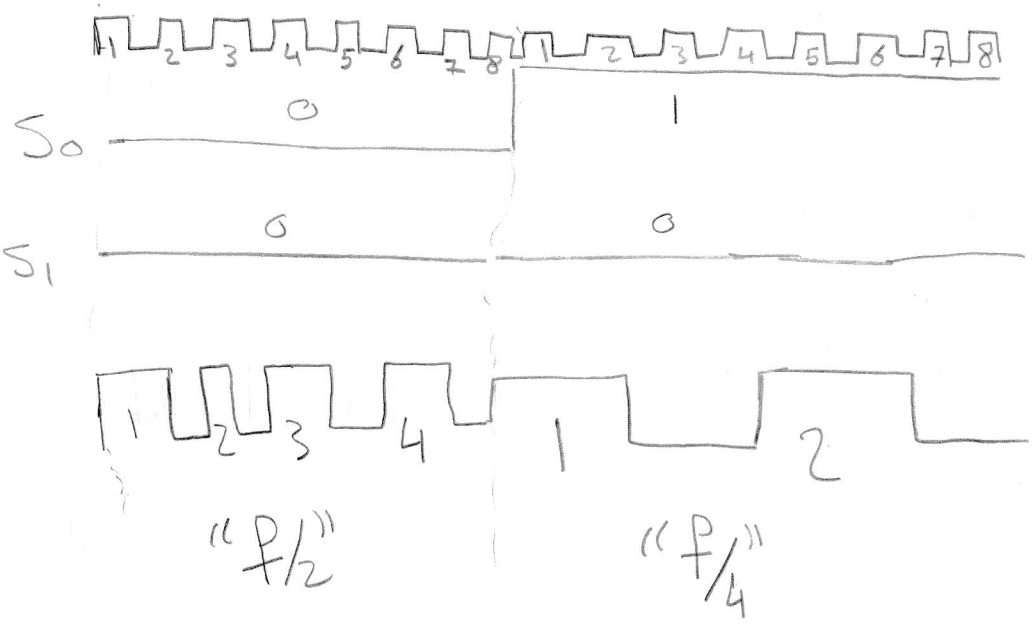


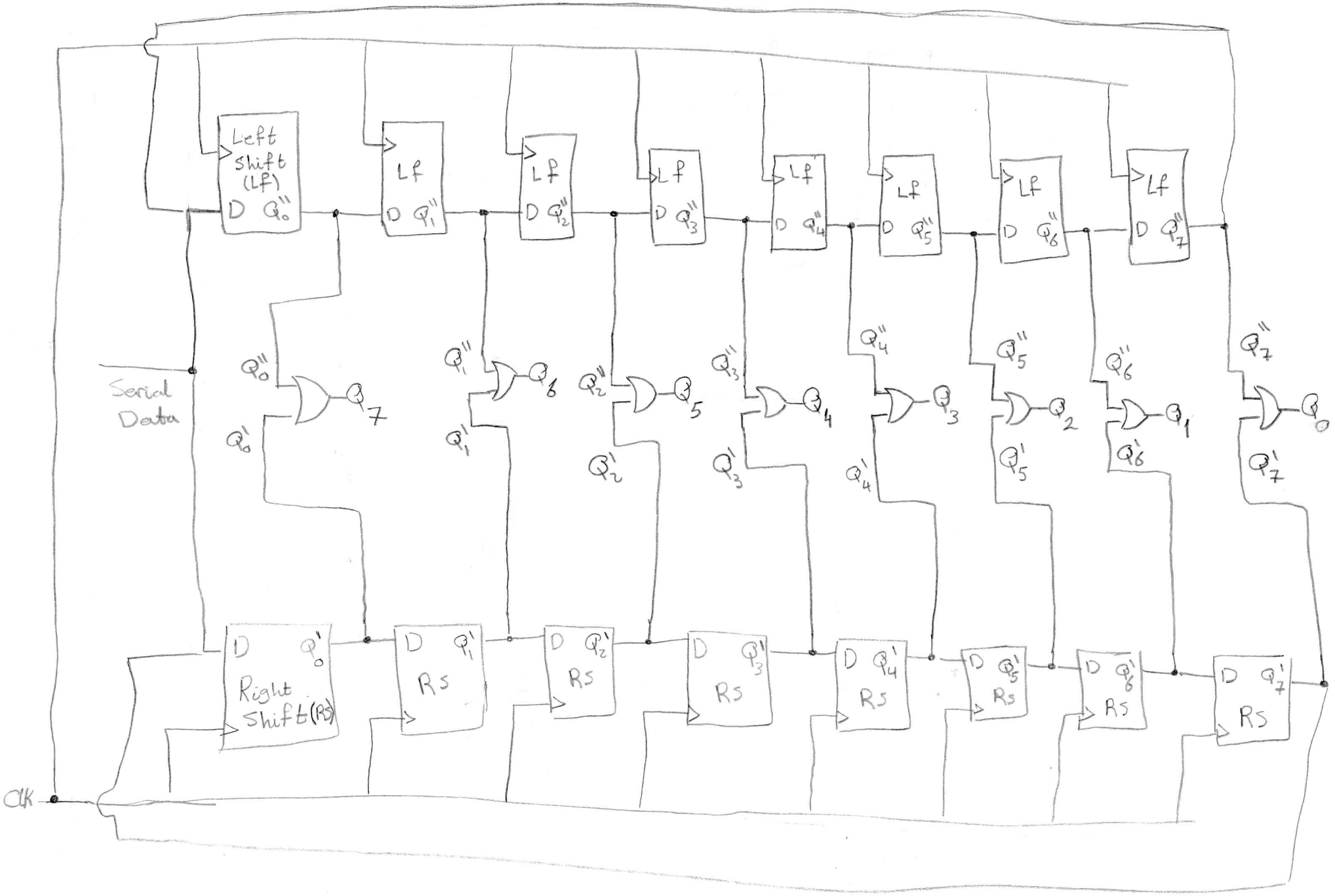
d) TRuth Table:

S_1	S_0	f/2	f/4	f/8	f/16
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

*Note: I'll choose f/2 & f/4 for timing diagram.

d)




Left Shift (Lf)
Lf
Lf
Lf
Lf
Lf
Lf
Lf
Serial Data
Right Shift (Rs)
Rs
Rs
Rs
Rs
Rs
Rs
Rs
CLK

8-9.2 This solution needs some elaboration.

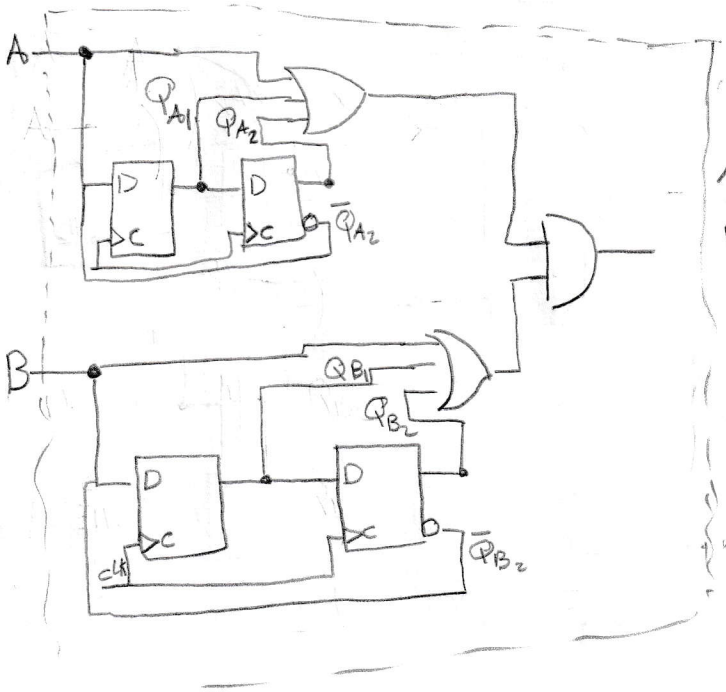
- First of all, the condition, "Any two of the four channels is true". This satisfied by the following boleam expression:

$$X(\text{output}) = AB + AC + AD + BC + BD + CD \quad \text{— Eq.1}$$

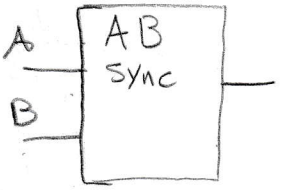
- For the condition, "True within 100 ns". It's better to use a logic diagram for further clarification as follows:

- Note: for simplicty, I'm assuming that after two John. counters, the delay (window) will be 100 ns. This means if z was our input, then Q_{2z} is nothing but z itself after 100 ns.

* Logic diagram that satisfies the conditions:



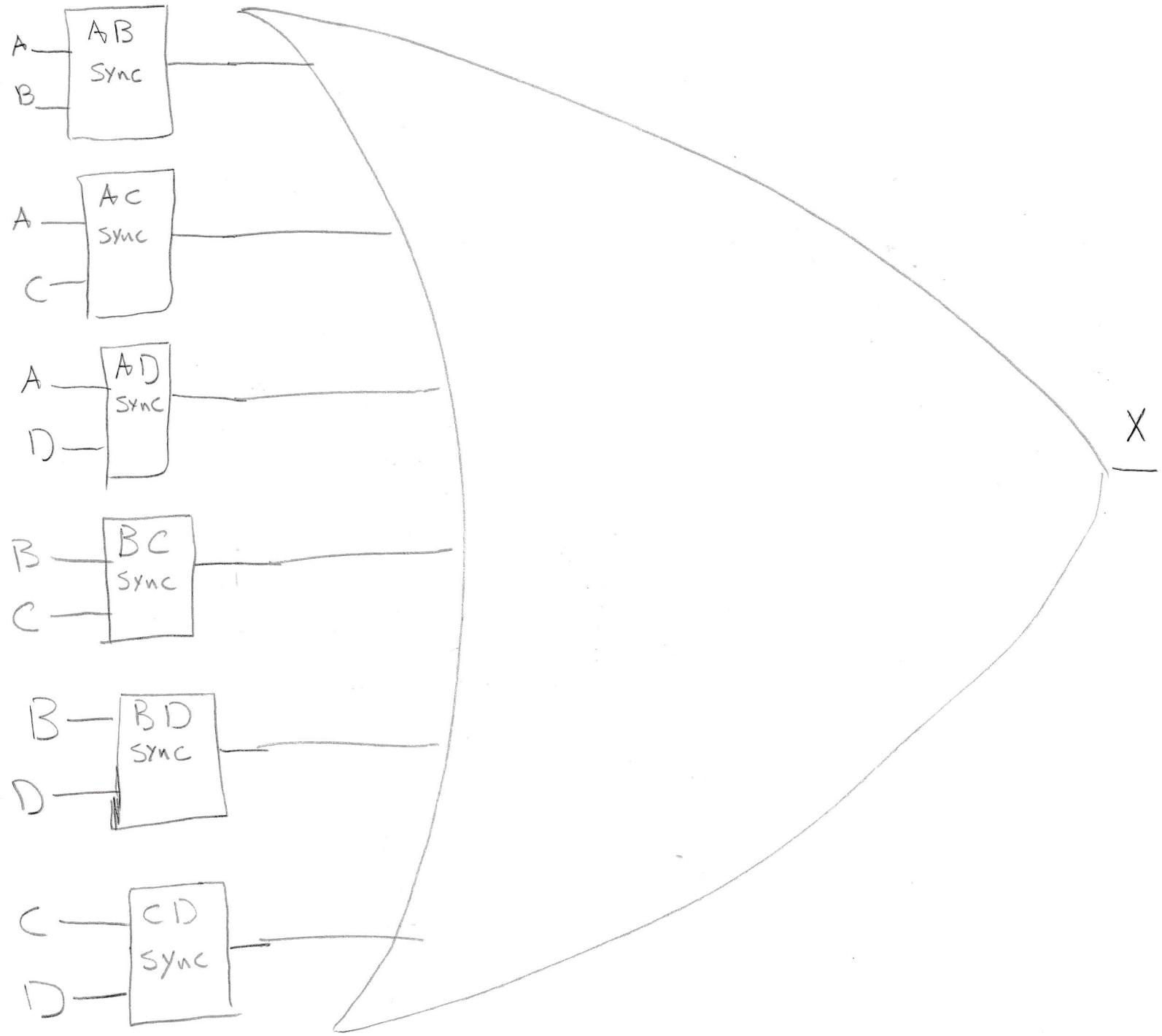
I'll sympolize this circuit as follows:



, we will repeat this sympolic circuit for each term in Eq.1

Continue on page 14 Please

Finally, putting all this together to obtain:



Happy Thanks Giving