CHAPTER 15

Integrated Circuit Technologies

CHAPTER OUTLINE

Before beginning this chapter, Section 3–8 should be covered.

CHAPTER OBJECTIVES

- Determine the noise margin of a device from data sheet parameters
- Calculate the power dissipation of a device
- Explain how propagation delay time affects the frequency of operation or speed of a circuit
- Interpret the speed-power product as a measure of performance
- Use data sheets to obtain information about a specific device
- Explain what the fan-out of a gate means
- Describe how basic TTL and CMOS gates operate at the component level
- Recognize the difference between TTL totem-pole outputs and TTL open-collector outputs and understand the limitations and uses of each
- Connect circuits in a wired-AND configuration
- Describe the operation of tri-state circuits
- Properly terminate unused gate inputs
- Compare the performance of TTL and CMOS families
- Handle CMOS devices without risk of damage due to electrostatic discharge
- State the advantages of ECL
- Describe the PMOS and NMOS circuits
- Describe an E^2CMOS cell

KEY TERMS

Key terms are in order of appearance in the chapter.

- TTL
- CMOS
- Noise immunity
- Noise margin
- Power dissipation
- Propagation delay time
- Fan-out
- Unit load
- Current sourcing
- Current sinking
- Pull-up resistor
- Tri-state
- Totem pole
- Open-collector
- ECL
- E^2CMOS

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INTRODUCTION

This chapter is intended to be used as a "floating" chapter. That is, all or portions of this chapter can be covered at any selected points throughout the book or completely omitted, depending on the course objectives. Section 3–8 should be covered before beginning this chapter.

In Chapter 3 (Section 3–8) you learned about basic integrated circuit logic gates. This chapter provides an introduction to the circuit technology used to implement those gates, as well as other types of IC devices.

Two major IC technologies, CMOS and bipolar (TTL), are covered and their operating parameters are defined. Also, the operational characteristics of various families within these circuit technologies are compared. Other circuit technologies are also introduced. It

is important to keep in mind that the particular circuit technology used to implement a logic gate has no effect on the logic operation of the gate. In terms of its truth table operation, a certain type of gate that is implemented with CMOS is the same as that type of gate implemented with TTL. The only differences in the gates are the electrical characteristics such as power dissipation, switching speed, and noise immunity.

15–1 Basic Operational Characteristics and Parameters

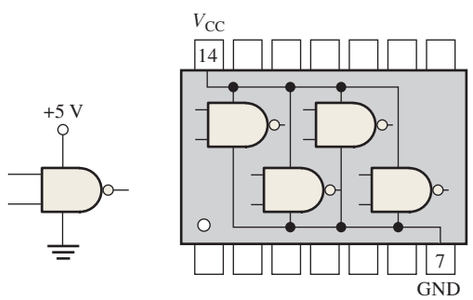
When you work with digital ICs, you should be familiar not only with their logical operation but also with such operational properties as voltage levels, noise immunity, power dissipation, fan-out, and propagation delay time. In this section, the practical aspects of these properties are discussed.

After completing this section, you should be able to

- Determine the power and ground connections
- Describe the logic levels for CMOS and TTL
- Discuss noise immunity
- Determine the power dissipation of a logic circuit
- Define the propagation delay time of a logic gate
- Discuss speed-power product and explain its significance
- Discuss loading and fan-out of TTL and CMOS

DC Supply Voltage

The nominal value of the dc supply voltage for **TTL** (transistor-transistor logic) devices is +5 V. TTL is also designated T^2L. **CMOS** (complementary metal-oxide semiconductor) devices are available in different supply voltage categories: +5 V, +3.3 V, 2.5 V, and 1.8 V. Although omitted from logic diagrams for simplicity, the dc supply voltage is connected to the V_{CC} pin of an IC package, and ground is connected to the GND pin. Both voltage and ground are distributed internally to all elements within the package, as illustrated in Figure 15–1 for a 14-pin package.



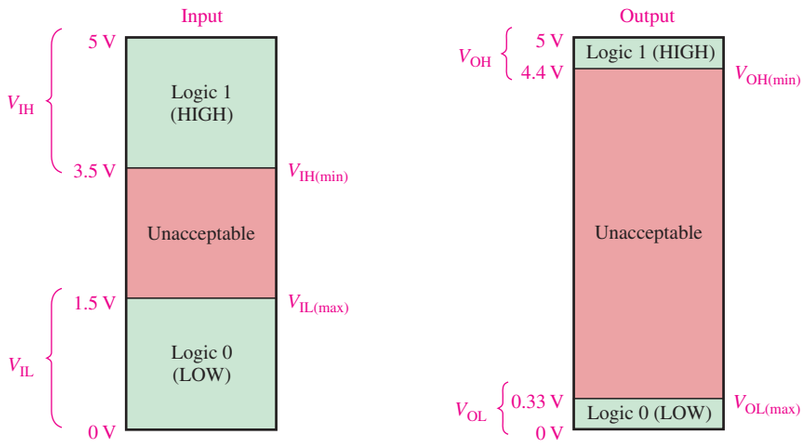
(a) Single gate (b) IC dual in-line package

FIGURE 15–1 Example of V_{CC} and ground connection and distribution in an IC package. Other pin connections are omitted for simplicity.

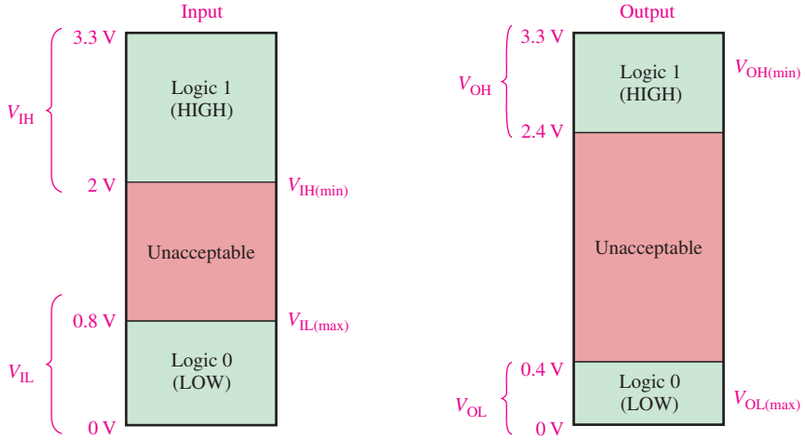
CMOS Logic Levels

Logic levels were discussed briefly in Chapter 1. There are four different logic-level specifications: V_{IL}, V_{IH}, V_{OL}, and V_{OH}. For CMOS circuits, the ranges of input voltages (V_{IL}) that can represent an acceptable LOW (logic 0) are from 0 V to 1.5 V for the +5 V logic and 0 V to 0.8 V for the 3.3 V logic. The ranges of input voltages (V_{IH}) that can represent an

acceptable HIGH (logic 1) are from 3.5 V to 5 V for the 5 V logic and 2 V to 3.3 V for the 3.3 V logic, as indicated in Figure 15–2. The ranges of values from 1.5 V to 3.5 V for 5 V logic and 0.8 V to 2 V for 3.3 V logic are regions of unpredictable performance, and values in these ranges are unacceptable. When an input voltage is in one of these ranges, it can be interpreted as either a HIGH or a LOW by the logic circuit. Therefore, CMOS gates cannot be operated reliably when the input voltages are in these unacceptable ranges.



(a) +5 V CMOS



(b) +3.3 V CMOS

FIGURE 15–2 Input and output logic levels for CMOS.

The ranges of CMOS output voltages (V_{OL} and V_{OH}) for both 5 V and 3.3 V logic are also shown in Figure 15–2. Notice that the minimum HIGH output voltage, $V_{OH(min)}$, is greater than the minimum HIGH input voltage, $V_{IH(min)}$. Also, notice that the maximum LOW output voltage, $V_{OL(max)}$, is less than the maximum LOW input voltage, $V_{IL(max)}$.

TTL Logic Levels

The input and output logic levels for TTL are given in Figure 15–3. Just as for CMOS, there are four different logic level specifications: V_{IL}, V_{IH}, V_{OL}, and V_{OH}.

Noise Immunity

Noise is unwanted voltage that is induced in electrical circuits and can present a threat to the proper operation of the circuit. Wires and other conductors within a system can pick up stray high-frequency electromagnetic radiation from adjacent conductors in which currents

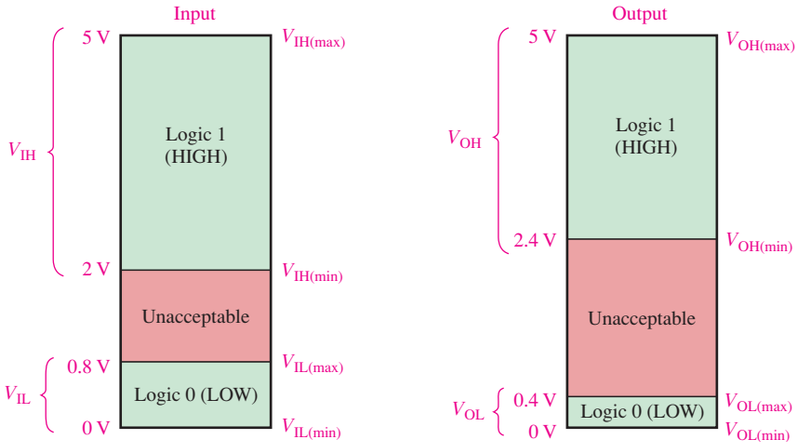


FIGURE 15–3 Input and output logic levels for TTL.

are changing rapidly or from many other sources external to the system. Also, power-line voltage fluctuation is a form of low-frequency noise.

In order not to be adversely affected by noise, a logic circuit must have a certain amount of **noise immunity.** This is the ability to tolerate a certain amount of unwanted voltage fluctuation on its inputs without changing its output state. For example, if noise voltage causes the input of a 5 V CMOS gate to drop below 3.5 V in the HIGH state, the input is in the unacceptable region and operation is unpredictable (see Figure 15–2). Thus, the gate may interpret the fluctuation below 3.5 V as a LOW level, as illustrated in Figure 15–4(a). Similarly, if noise causes a gate input to go above 1.5 V in the LOW state, an uncertain condition is created, as illustrated in part (b).

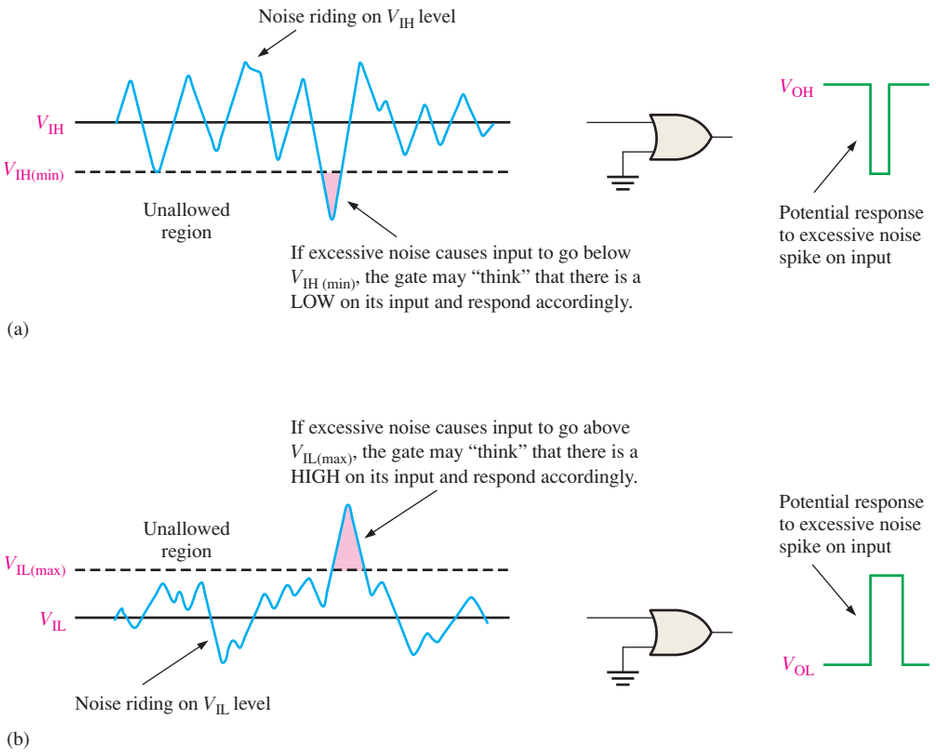


FIGURE 15–4 Illustration of the effects of input noise on gate operation.

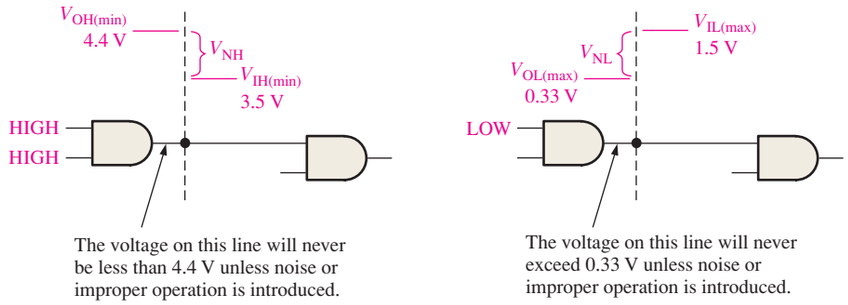
Noise Margin

A measure of a circuit's noise immunity is called the **noise margin,** which is expressed in volts. There are two values of noise margin specified for a given logic circuit: the HIGH-level noise margin (V_{NH}) and the LOW-level noise margin (V_{NL}). These parameters are defined by the following equations:

$$V_{NH} = V_{OH(min)} = V_{IH(min)} \quad \text{Equation 15–1}$$

$$V_{NL} = V_{IL(max)} = V_{OL(max)} \quad \text{Equation 15–2}$$

Sometimes you will see the noise margin expressed as a percentage of V_{CC}. From the equations, V_{NH} is the difference between the lowest possible HIGH output from a driving gate ($V_{OH(min)}$) and the lowest possible HIGH input that the load gate can tolerate ($V_{IH(min)}$). Noise margin, V_{NL}, is the difference between the maximum possible LOW input that a gate can tolerate ($V_{IL(max)}$) and the maximum possible LOW output of the driving gate ($V_{OL(max)}$). Noise margins are illustrated in Figure 15–5.



(a) HIGH-level noise margin (b) LOW-level noise margin

FIGURE 15–5 Illustration of noise margins. Values are for 5 V CMOS, but the principle applies to any logic family.

EXAMPLE 15–1

Determine the HIGH-level and LOW-level noise margins for CMOS and for TTL by using the information in Figures 15–2 and 15–3.

Solution

For 5 V CMOS,

$$V_{IH(min)} = 3.5 \text{ V}$$
$$V_{IL(max)} = 1.5 \text{ V}$$
$$V_{OH(min)} = 4.4 \text{ V}$$
$$V_{OL(max)} = 0.33 \text{ V}$$
$$V_{NH} = V_{OH(min)} - V_{IH(min)} = 4.4 \text{ V} - 3.5 \text{ V} = \mathbf{0.9\ V}$$
$$V_{NL} = V_{IL(max)} - V_{OL(max)} = 1.5 \text{ V} - 0.33 \text{ V} = \mathbf{1.17\ V}$$

For TTL,

$$V_{IH(min)} = 2 \text{ V}$$
$$V_{IL(max)} = 0.8 \text{ V}$$
$$V_{OH(min)} = 2.4 \text{ V}$$
$$V_{OL(max)} = 0.4 \text{ V}$$
$$V_{NH} = V_{OH(min)} - V_{IH(min)} = 2.4 \text{ V} - 2 \text{ V} = \mathbf{0.4\ V}$$
$$V_{NL} = V_{IL(max)} - V_{OL(max)} = 0.8 \text{ V} - 0.4 \text{ V} = \mathbf{0.4\ V}$$

A TTL gate is immune to up to 0.4 V of noise for both the HIGH and LOW input states.

Related Problem*

Based on the preceding noise margin calculations, which family of devices, 5 V CMOS or TTL, should be used in a high-noise environment?

*Answers are at the end of the chapter.

Power Dissipation

A logic gate draws current from the dc supply voltage source, as indicated in Figure 15–6. When the gate is in the HIGH output state, an amount of current designated by I_{CCH} is drawn; and in the LOW output state, a different amount of current, I_{CCL}, is drawn.

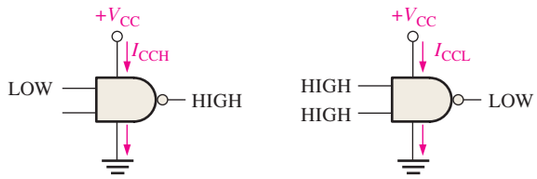


FIGURE 15–6 Currents from the dc supply. Conventional current direction is shown. Electron flow notation is opposite.

As an example, if I_{CCH} is specified as 1.5 mA when V_{CC} is 5 V and if the gate is in a static (nonchanging) HIGH output state, the **power dissipation** (P_D) of the gate is

$$P_D = V_{CC}I_{CCH} = (5\text{ V})(1.5\text{ mA}) = 7.5\text{ mW}$$

When a gate is pulsed, its output switches back and forth between HIGH and LOW, and the amount of supply current varies between I_{CCH} and I_{CCL}. The average power dissipation depends on the duty cycle and is usually specified for a duty cycle of 50%. When the duty cycle is 50%, the output is HIGH half the time and LOW the other half. The average supply current is therefore

$$I_{CC} = \frac{I_{CCH} + I_{CCL}}{2} \qquad \text{Equation 15–3}$$

The average power dissipation is

$$P_D = V_{CC}I_{CC} \qquad \text{Equation 15–4}$$

EXAMPLE 15–2

A certain gate draws 2 μA when its output is HIGH and 3.6 μA when its output is LOW. What is its average power dissipation if V_{CC} is 5 V and the gate is operated on a 50% duty cycle?

Solution

The average I_{CC} is

$$I_{CC} = \frac{I_{CCH} + I_{CCL}}{2} = \frac{2.0\,\mu\text{A} + 3.6\,\mu\text{A}}{2} = 2.8\,\mu\text{A}$$

The average power dissipation is

$$P_D = V_{CC}I_{CC} = (5\text{ V})(2.8\ \mu\text{A}) = \mathbf{14\ \mu W}$$

Related Problem

A certain IC gate has an $I_{CCH} = 1.5\ \mu$A and $I_{CCL} = 2.8\ \mu$A. Determine the average power dissipation for 50% duty cycle operation if V_{CC} is 5 V.

Power dissipation in a TTL circuit is essentially constant over its range of operating frequencies. Power dissipation in CMOS, however, is frequency dependent. It is extremely low under static (dc) conditions and increases as the frequency increases. These characteristics are shown in the general curves of Figure 15–7. For example, the power dissipation of a low-power Schottky (LS) TTL gate is a constant 2.2 mW. The power dissipation of an HCMOS gate is 2.75 μW under static conditions and 170 μW at 100 kHz.

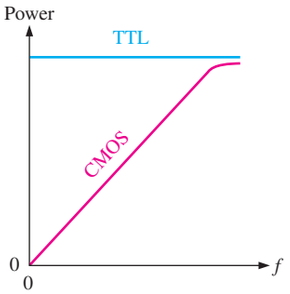


FIGURE 15–7 Power-versus-frequency curves for TTL and CMOS.

Propagation Delay Time

When a signal passes (propagates) through a logic circuit, it always experiences a time delay, as illustrated in Figure 15–8. A change in the output level always occurs a short time, called the **propagation delay time,** later than the change in the input level that caused it.

As mentioned in Chapter 3, there are two propagation delay times specified for logic gates:

- t_{PHL}: The time between a designated point on the input pulse and the corresponding point on the output pulse when the output is changing from HIGH to LOW.
- t_{PLH}: The time between a designated point on the input pulse and the corresponding point on the output pulse when the output is changing from LOW to HIGH.

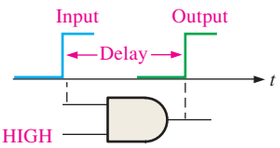


FIGURE 15–8 A basic illustration of propagation delay time.

These propagation delay times are illustrated in Figure 15–9, with the 50% points on the pulse edges used as references.

The propagation delay time of a gate limits the frequency at which it can be operated. The greater the propagation delay time, the lower the maximum frequency. Thus, a higher-speed circuit is one that has a smaller propagation delay time. For example, a gate with a delay of 3 ns is faster than one with a 10 ns delay.

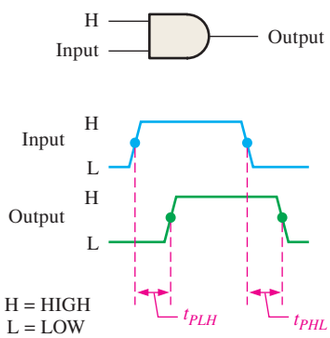


FIGURE 15–9 Propagation delay times.

Speed-Power Product

The speed-power product provides a basis for the comparison of logic circuits when *both* propagation delay time and power dissipation are important considerations in the selection of the type of logic to be used in a certain application. The lower the speed-power product, the better. The unit of speed-power product is the picojoule (pJ). For example, HCMOS has a speed-power product of 1.2 pJ at 100 kHz while LS TTL has a value of 22 pJ.

Loading and Fan-Out

When the output of a logic gate is connected to one or more inputs of other gates, a load on the driving gate is created, as shown in Figure 15–10. There is a limit to the number of load gate inputs that a given gate can drive. This limit is called the **fan-out** of the gate. Fan-out is expressed as **unit loads**. One gate input represents a unit load to a driving gate of the same logic family.

CMOS Loading

Loading in CMOS differs from that in TTL because the type of transistors used in CMOS logic present a predominantly capacitive load to the driving gate, as illustrated in Figure 15–11. In this case, the limitations are the charging and discharging times associated with the output

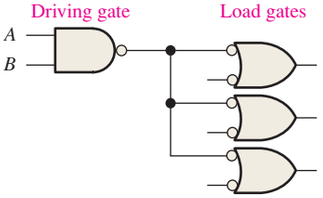


FIGURE 15–10 Loading a gate output with gate inputs.

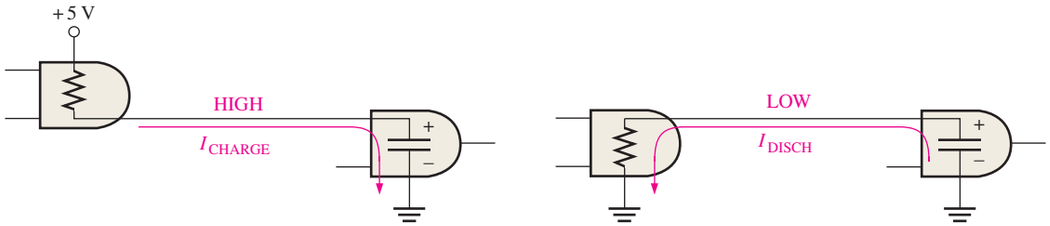


FIGURE 15–11 Capacitive loading of a CMOS gate.

resistance of the driving gate and the input capacitance of the load gates. When the output of the driving gate is HIGH, the input capacitance of the load gate is charging through the output resistance of the driving gate. When the output of the driving gate is LOW, the capacitance is discharging, as indicated in Figure 15–11.

When more load gate inputs are added to the driving gate output, the total capacitance increases because the input capacitances effectively appear in parallel. This increase in capacitance increases the charging and discharging times, thus reducing the maximum frequency at which the gate can be operated. Therefore, the fan-out of a CMOS gate depends on the frequency of operation. The fewer the load gate inputs, the greater the maximum frequency.

TTL Loading

A TTL driving gate sources current to a load gate input in the HIGH state (I_{IH}) and sinks current from the load gate in the LOW state (I_{IL}). **Current sourcing** and **current sinking** are illustrated in simplified form in Figure 15–12, where the resistors represent the internal input and output resistance of the gate for the two conditions.

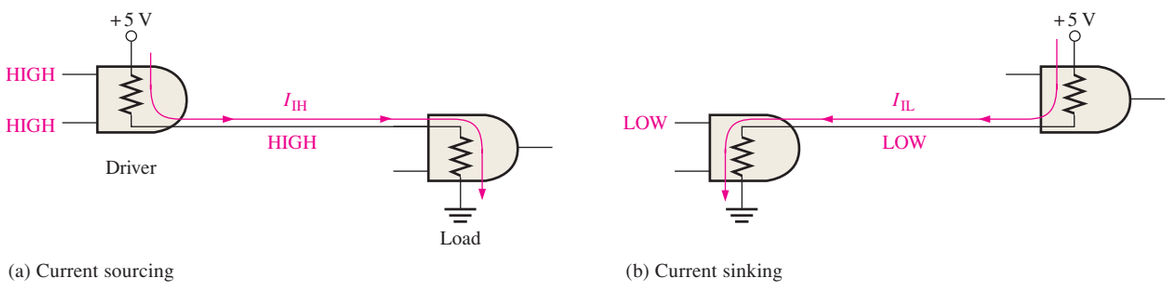


FIGURE 15–12 Basic illustration of current sourcing and current sinking in logic gates.

As more load gates are connected to the driving gate, the loading on the driving gate increases. The total source current increases with each load gate input that is added, as illustrated in Figure 15–13. As this current increases, the internal voltage drop of the driving gate

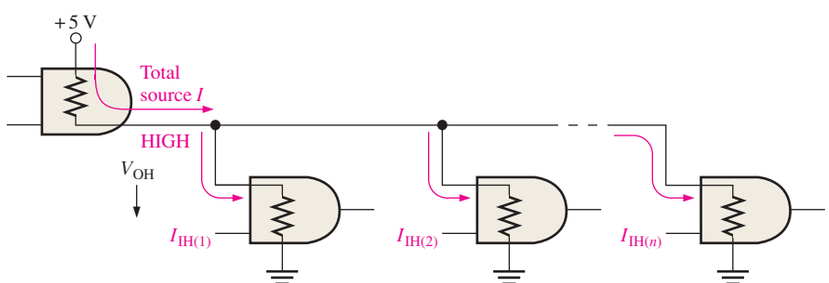


FIGURE 15–13 HIGH-state TTL loading.

increases, causing the output, V_{OH}, to decrease. If an excessive number of load gate inputs are connected, V_{OH} drops below $V_{OH(min)}$, and the HIGH-level noise margin is reduced, thus compromising the circuit operation. Also, as the total source current increases, the power dissipation of the driving gate increases.

The fan-out is the maximum number of load gate inputs that can be connected without adversely affecting the specified operational characteristics of the gate. For example, low-power Schottky (LS) TTL has a fan-out of 20 unit loads.

The total sink current also increases with each load gate input that is added, as shown in Figure 15–14. As this current increases, the internal voltage drop of the driving gate increases, causing V_{OL} to increase. If an excessive number of loads are added, V_{OL} exceeds $V_{OL(max)}$, and the LOW-level noise margin is reduced.

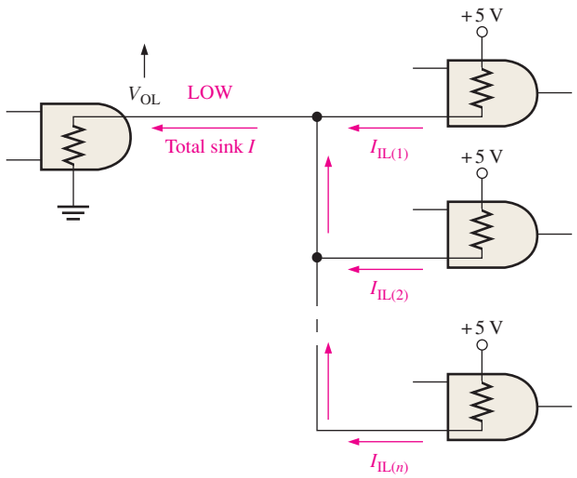


FIGURE 15–14 LOW-stage TTL loading.

In TTL, the current-sinking capability (LOW output state) is the limiting factor in determining the fan-out.

SECTION 15–1 CHECKUP

Answers are at the end of the chapter.

1. Define V_{IH}, V_{IL}, V_{OH}, and V_{OL}.
2. Is it better to have a lower value of noise margin or a higher value?
3. Gate *A* has a greater propagation delay time than gate *B*. Which gate can operate at a higher frequency?
4. How does excessive loading affect the noise margin of a gate?

15–2 CMOS Circuits

Basic internal CMOS circuitry and its operation are discussed in this section. The abbreviation CMOS stands for complementary metal-oxide semiconductor. The term *complementary* refers to the use of two types of transistors in the output circuit. An *n*-channel MOSFET (MOS field-effect transistor) and a *p*-channel MOSFET are used.

After completing this section, you should be able to

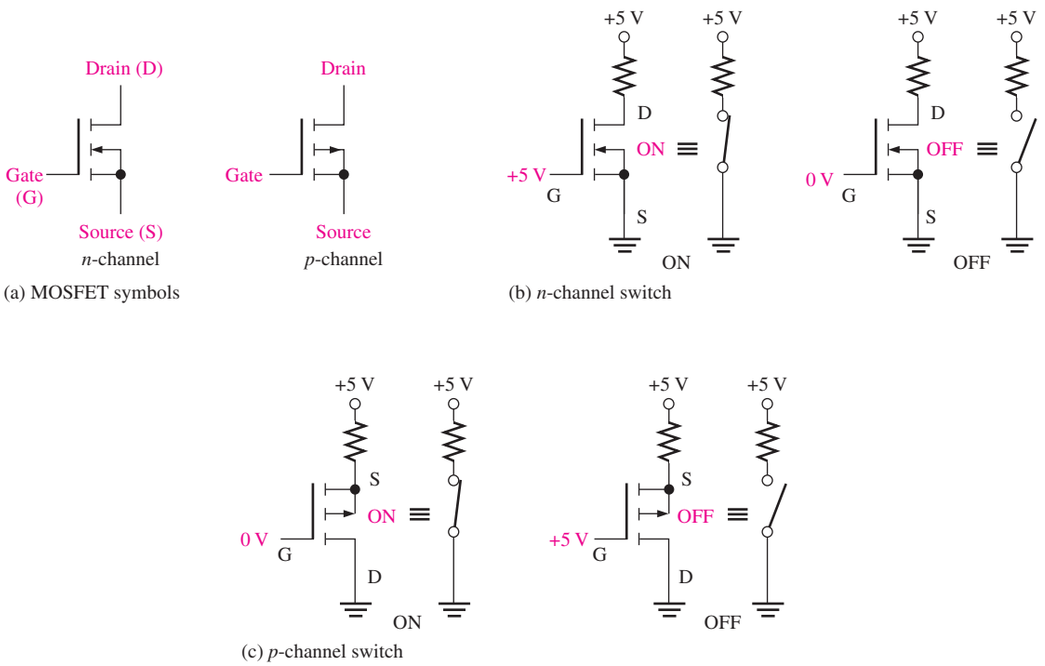
- Identify a MOSFET by its symbol
- Discuss the switching action of a MOSFET

- Describe the basic operation of a CMOS inverter circuit
- Describe the basic operation of CMOS NAND and NOR gates
- Explain the operation of a CMOS gate with an open-drain output
- Discuss the operation of tri-state CMOS gates
- List the precautions required when handling CMOS devices

The MOSFET

Metal-oxide semiconductor field-effect transistors (**MOSFETs**) are the active switching elements in CMOS circuits. These devices differ greatly in construction and internal operation from bipolar junction transistors used in bipolar (TTL) circuits, but the switching action is basically the same: they function ideally as open or closed switches, depending on the input.

Figure 15–15(a) shows the symbols for both *n*-channel and *p*-channel MOSFETs. As indicated, the three terminals of a MOSFET are **gate, drain,** and **source**. When the gate voltage of an *n*-channel MOSFET is more positive than the source, the MOSFET is on (*saturation*), and there is, ideally, a closed switch between the drain and the source. When the gate-to-source voltage is zero, the MOSFET is off (*cutoff*), and there is, ideally, an open switch between the drain and the source. This operation is illustrated in Figure 15–15(b). The *p*-channel MOSFET operates with opposite voltage polarities, as shown in part (c).



(a) MOSFET symbols

(b) *n*-channel switch

(c) *p*-channel switch

FIGURE 15–15 Basic symbols and switching action of MOSFETs.

Sometimes a simplified MOSFET symbol as shown in Figure 15–16 is used.

FIGURE 15–16 Simplified MOSFET symbol.

CMOS Inverter

Complementary MOS (CMOS) logic uses the MOSFET in complementary pairs as its basic element. A complementary pair uses both *p*-channel and *n*-channel enhancement MOSFETs, as shown in the inverter circuit in Figure 15–17.

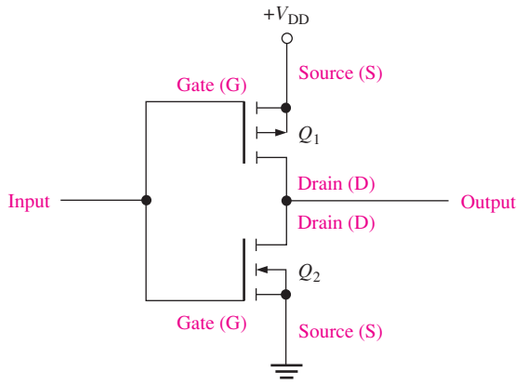
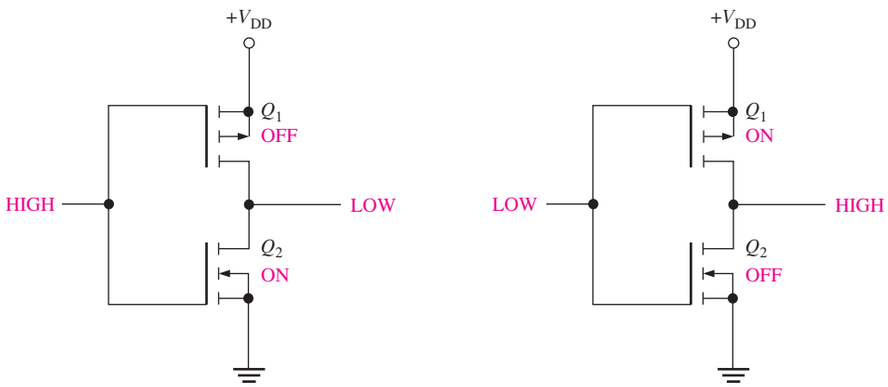


FIGURE 15–17 A CMOS inverter circuit.

When a HIGH is applied to the input, as shown in Figure 15–18(a), the *p*-channel MOSFET Q_1 is off and the *n*-channel MOSFET Q_2 is on. This condition connects the output to ground through the *on* resistance of Q_2, resulting in a LOW output. When a LOW is applied to the input, as shown in Figure 15–18(b), Q_1 is on and Q_2 is off. This condition connects the output to $+V_{DD}$ (dc supply voltage) through the *on* resistance of Q_1, resulting in a HIGH output.



(a) HIGH input, LOW output

(b) LOW input, HIGH output

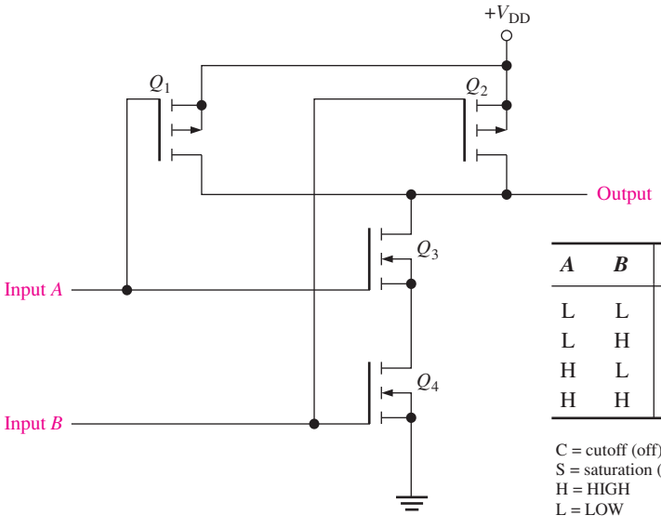
FIGURE 15–18 Operation of a CMOS inverter.

CMOS NAND Gate

Figure 15–19 shows a CMOS NAND gate with two inputs. Notice the arrangement of the complementary pairs (*n*-channel and *p*-channel MOSFETs).

The operation of a CMOS NAND gate is as follows:

- When both inputs are LOW, Q_1 and Q_2 are on, and Q_3 and Q_4 are off. The output is pulled HIGH through the *on* resistance of Q_1 and Q_2 in parallel.
- When input *A* is LOW and input *B* is HIGH, Q_1 and Q_4 are on, and Q_2 and Q_3 are off. The output is pulled HIGH through the low *on* resistance of Q_1.
- When input *A* is HIGH and input *B* is LOW, Q_1 and Q_4 are off, and Q_2 and Q_3 are on. The output is pulled HIGH through the low *on* resistance of Q_2.
- Finally, when both inputs are HIGH, Q_1 and Q_2 are off, and Q_3 and Q_4 are on. In this case, the output is pulled LOW through the *on* resistance of Q_3 and Q_4 in series to ground.



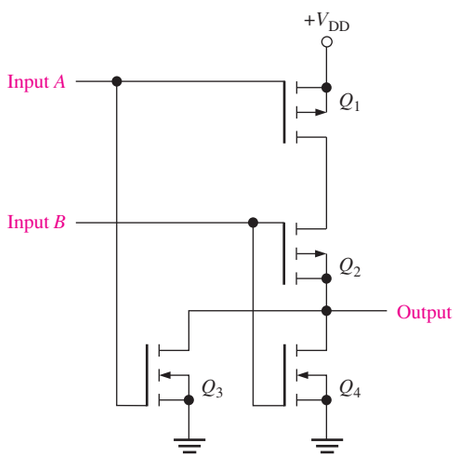
A	B	Q_1	Q_2	Q_3	Q_4	X
L	L	S	S	C	C	H
L	H	S	C	C	S	H
H	L	C	S	S	C	H
H	H	C	C	S	S	L

C = cutoff (off)
S = saturation (on)
H = HIGH
L = LOW

FIGURE 15–19 A CMOS NAND gate circuit.

CMOS NOR Gate

Figure 15–20 shows a CMOS NOR gate with two inputs. Notice the arrangement of the complementary pairs.



A	B	Q_1	Q_2	Q_3	Q_4	X
L	L	S	S	C	C	H
L	H	S	C	C	S	L
H	L	C	S	S	C	L
H	H	C	C	S	S	L

C = cutoff (off)
S = saturation (on)
H = HIGH
L = LOW

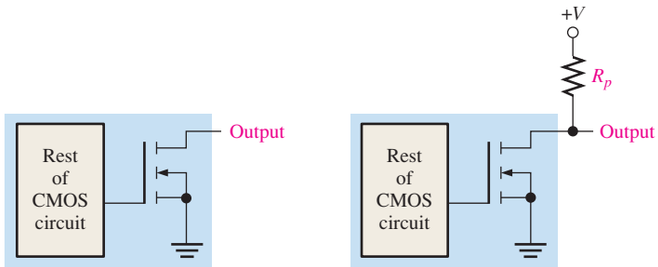
FIGURE 15–20 A CMOS NOR gate circuit.

The operation of a CMOS NOR gate is as follows:

- When both inputs are LOW, Q_1 and Q_2 are on, and Q_3 and Q_4 are off. As a result, the output is pulled HIGH through the *on* resistance of Q_1 and Q_2 in series.
- When input A is LOW and input B is HIGH, Q_1 and Q_4 are on, and Q_2 and Q_3 are off. The output is pulled LOW through the low *on* resistance of Q_4 to ground.
- When input A is HIGH and input B is LOW, Q_1 and Q_4 are off, and Q_2 and Q_3 are on. The output is pulled LOW through the *on* resistance of Q_3 to ground.
- When both inputs are HIGH, Q_1 and Q_2 are off, and Q_3 and Q_4 are on. The output is pulled LOW through the *on* resistance of Q_3 and Q_4 in parallel to ground.

Open-Drain Gates

The term *open-drain* means that the drain terminal of the output transistor is unconnected and must be connected externally to V_{DD} through a load. An open-drain gate is the CMOS counterpart of an open-collector TTL gate (discussed in Section 15–3). An open-drain output circuit is a single *n*-channel MOSFET as shown in Figure 15–21(a). An external **pull-up resistor** must be used, as shown in part (b), to produce a HIGH output state. Also, open-drain outputs can be connected in a wired-AND configuration, a concept that is discussed in Section 15–4 in relation to TTL.

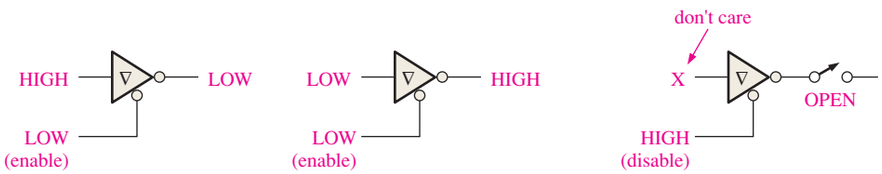


(a) Unconnected output (b) With pull-up resistor

FIGURE 15–21 Open-drain CMOS gates.

Tri-state CMOS Gates

Tri-state outputs are available in both CMOS and TTL logic. The **tri-state** output combines the advantages of the totem-pole and open-collector circuits. As you recall, the three output states are HIGH, LOW, and high-impedance (**high-Z**). When selected for normal logic-level operation, as determined by the state of the enable input, a tri-state circuit operates in the same way as a regular gate. When a tri-state circuit is selected for high-*Z* operation, the output is effectively disconnected from the rest of the circuit by the internal circuitry. Figure 15–22 illustrates the operation of a tri-state circuit. The inverted triangle (∇) designates a tri-state output.



(a) Enabled for normal logic operation (b) High-*Z* state

FIGURE 15–22 The three states of a tri-state circuit.

The circuitry in a tri-state CMOS gate, as shown in Figure 15–23, allows each of the output transistors Q_1 and Q_2 to be turned off at the same time, thus disconnecting the output from the rest of the circuit. When the enable input is LOW, the device is enabled for normal logic operation. When the enable input is HIGH, both Q_1 and Q_2 are off and the circuit is in the high-*Z* state.

Precautions for Handling CMOS

All CMOS devices are subject to damage from electrostatic discharge (ESD). Therefore, they must be handled with special care. Review the following precautions:

1. All CMOS devices are shipped in conductive foam to prevent electrostatic charge buildup. When they are removed from the foam, the pins should not be touched.
2. The devices should be placed with pins down on a grounded surface, such as a metal plate, when removed from protective material. Do not place CMOS devices in polystyrene foam or plastic trays.

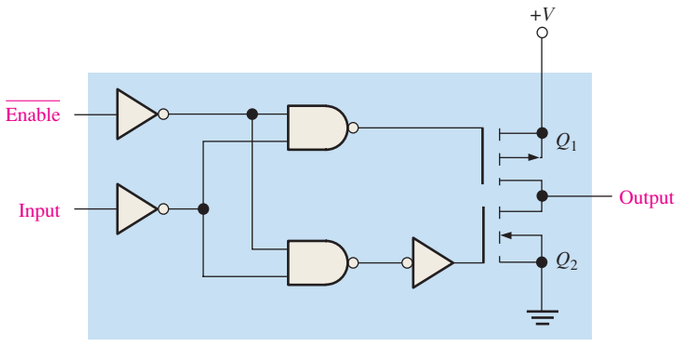


FIGURE 15–23 A tri-state CMOS inverter.

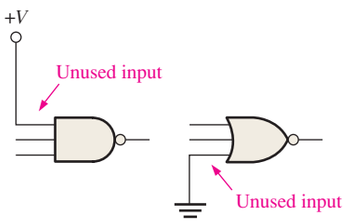


FIGURE 15–24 Handling unused CMOS inputs.

3. All tools, test equipment, and metal workbenches should be earth-grounded. A person working with CMOS devices should, in certain environments, have his or her wrist grounded with a length of cable and a large-value series resistor. The resistor prevents severe shock should the person come in contact with a voltage source.
4. Do not insert CMOS devices (or any other ICs) into sockets or PCBs with the power on.
5. All unused inputs should be connected to the supply voltage or ground as indicated in Figure 15–24. If left open, an input can acquire electrostatic charge and "float" to unpredicted levels.
6. After assembly on PCBs, protection should be provided by storing or shipping boards with their connectors in conductive foam. The CMOS input and output pins may also be protected with large-value resistors connected to ground.

SECTION 15–2 CHECKUP

1. What type of transistor is used in CMOS logic?
2. What is meant by the term *complementary MOS?*
3. Why must CMOS devices be handled with care?

15–3 TTL (Bipolar) Circuits

The internal circuit operation of TTL (bipolar) logic gates with totem-pole outputs is covered in this section. Also, the operation of TTL gates with open-collector outputs and the operation of tri-state gates are covered.

After completing this section, you should be able to

- Identify a bipolar junction transistor (BJT) by its symbol
- Describe the switching action of a BJT
- Describe the basic operation of a TTL inverter circuit
- Explain what a totem-pole output is
- Describe the basic operation of a TTL NAND gate
- Explain the operation and use a TTL gate with an open-collector output
- Explain the operation of a gate with a tri-state output

The Bipolar Junction Transistor

The bipolar junction transistor (**BJT**) is the active switching element used in all TTL circuits. Figure 15–25 shows the symbol for an *npn* BJT with its three terminals; **base, emitter,** and **collector**. A BJT has two **junctions,** the base-emitter junction and the base-collector junction.

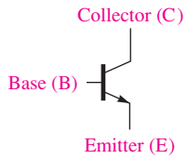
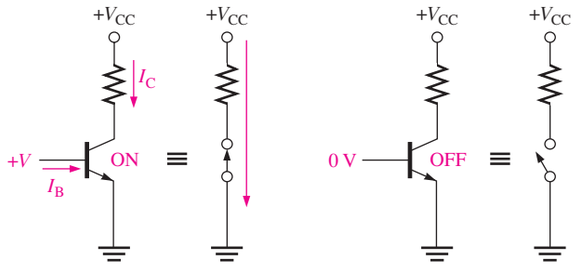


FIGURE 15–25 The symbol for a BJT.

The basic switching operation is as follows: When the base is approximately 0.7 V more positive than the emitter and when sufficient current is provided into the base, the **transistor** turns on and goes into saturation. In saturation, the transistor ideally acts like a closed switch between the collector and the emitter, as illustrated in Figure 15–26(a). When the base is less than 0.7 V more positive than the emitter, the transistor turns off and becomes an open switch between the collector and the emitter, as shown in part (b). To summarize in general terms, a HIGH on the base turns the transistor on and makes it a closed switch. A LOW on the base turns the transistor off and makes it an open switch. In TTL, some BJTs have multiple emitters.



(a) Saturated (ON) transistor and ideal switch equivalent

(b) OFF transistor and ideal switch equivalent

FIGURE 15–26 The ideal switching action of the BJT. Conventional current direction is shown. Electron flow notation is opposite.

TTL Inverter

The logic function of an inverter or any type of gate is always the same, regardless of the type of circuit technology that is used. Figure 15–27 shows a standard TTL circuit for an inverter. In this figure Q_1 is the input coupling transistor, and D_1 is the input clamp **diode**. Transistor Q_2 is called a *phase splitter,* and the combination of Q_3 and Q_4 forms the output circuit often referred to as a **totem-pole** arrangement.

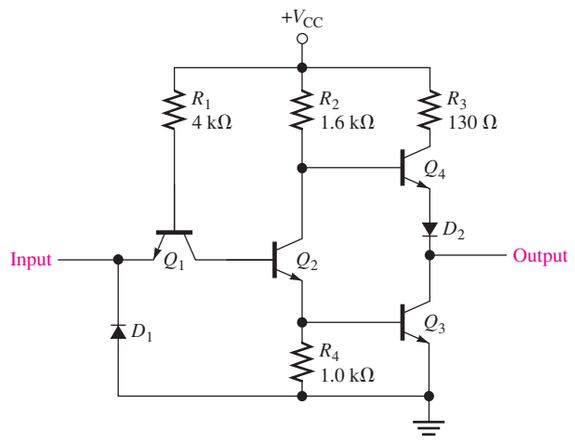


FIGURE 15–27 A standard TTL inverter circuit.

When the input is a HIGH, the base-emitter junction of Q_1 is **reverse-biased,** and the base-collector junction is **forward-biased**. This condition permits current through R_1 and

the base-collector junction of Q_1 into the base of Q_2, thus driving Q_2 into saturation. As a result, Q_3 is turned on by Q_2, and its collector voltage, which is the output, is near ground potential. Therefore, there is a LOW output for a HIGH input. At the same time, the collector of Q_2 is at a sufficiently low voltage level to keep Q_4 off.

When the input is LOW, the base-emitter junction of Q_1 is forward-biased, and the base-collector junction is reverse-biased. There is current through R_1 and the base-emitter junction of Q_1 to the LOW input. A LOW provides a path to ground for the current. There is no current into the base of Q_2, so it is off. The collector of Q_2 is HIGH, thus turning Q_4 on. A saturated Q_4 provides a low-resistance path from V_{CC} to the output; therefore, there is a HIGH on the output for a LOW on the input. At the same time, the emitter of Q_2 is at ground potential, keeping Q_3 off.

Diode D_1 in the TTL circuit prevents negative spikes of voltage on the input from damaging Q_1. Diode D_2 ensures that Q_4 will turn off when Q_2 is on (HIGH input). In this condition, the collector voltage of Q_2 is equal to the base-to-emitter voltage, V_{BE}, of Q_3 plus the collector-to-emitter voltage, V_{CE}, of Q_2. Diode D_2 provides an additional V_{BE} equivalent drop in series with the base-emitter junction of Q_4 to ensure its turn-off when Q_2 is on.

The operation of the TTL inverter for the two input states is illustrated in Figure 15–28. In the circuit in part (a), the base of Q_1 is 2.1 V above ground, so Q_2 and Q_3 are on. In the circuit in part (b), the base of Q_1 is about 0.7 V above ground—not enough to turn Q_2 and Q_3 on.

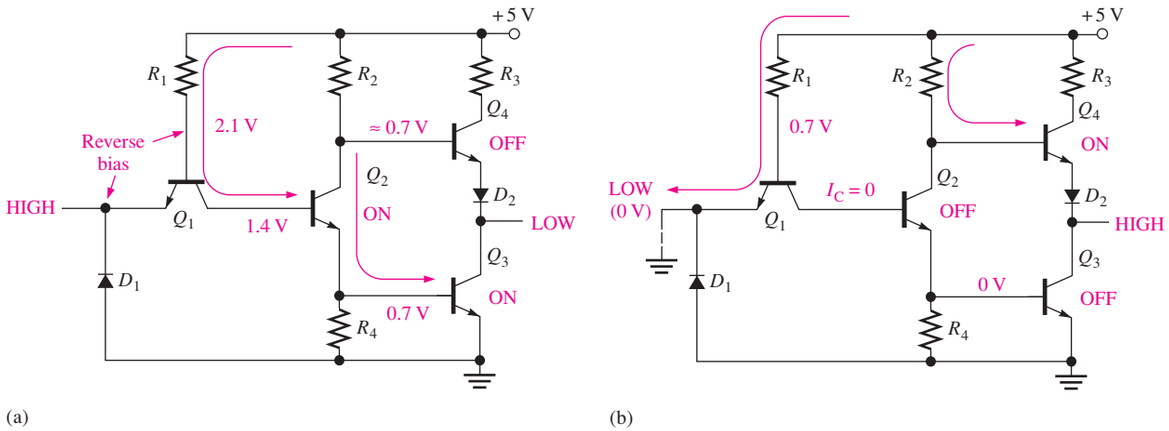


FIGURE 15–28 Operation of a TTL inverter.

TTL NAND Gate

A 2-input TTL NAND gate is shown in Figure 15–29. Basically, it is the same as the inverter circuit except for the additional input emitter of Q_1. In TTL technology, multiple-emitter transistors are used for the input devices. These multiple-emitter transistors can be compared to the diode arrangement, as shown in Figure 15–30.

Perhaps you can understand the operation of this circuit better by visualizing Q_1 in Figure 15–29 replaced by the diode arrangement in Figure 15–30. A LOW on either input A or input B forward-biases the corresponding diode and reverse-biases D_3 (Q_1 base-collector junction). This action keeps Q_2 off and results in a HIGH output in the same way as described for the TTL inverter. Of course, a LOW on both inputs will do the same thing.

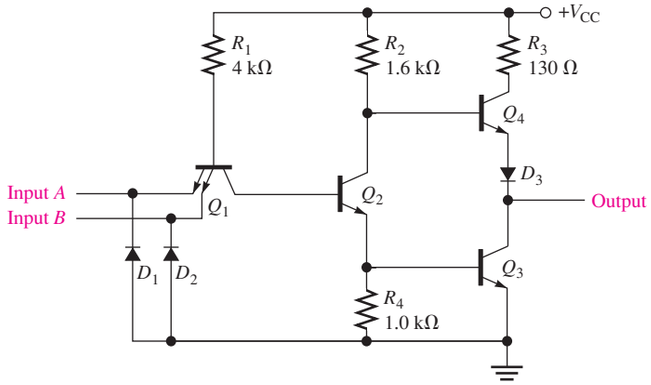


FIGURE 15–29 A TTL NAND gate circuit.

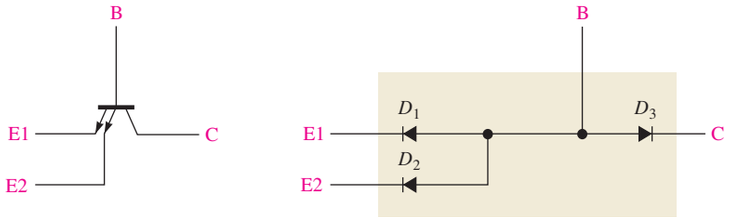
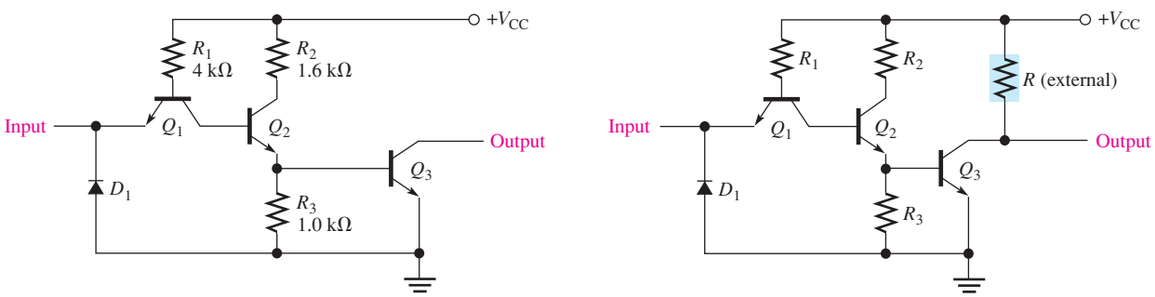


FIGURE 15–30 Diode equivalent of a TTL multiple-emitter transistor.

A HIGH on both inputs reverse-biases both input diodes and forward-biases D_3 (Q_1 base-collector junction). This action turns Q_2 on and results in a LOW output in the same way as described for the TTL inverter. You should recognize this operation as that of the NAND function: The output is LOW only if all inputs are HIGH.

Open-Collector Gates

In addition to the totem-pole output circuit; another type of output available in TTL integrated circuits is the **open-collector** output. This is comparable to the open-drain output of CMOS. A standard TTL inverter with an open-collector is shown in Figure 15–31(a). The other types of gates are also available with open-collector outputs.



(a) Open-collector inverter circuit

(b) With external pull-up resistor

FIGURE 15–31 TTL inverter with open-collector output.

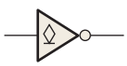


FIGURE 15–32 Open-collector symbol in an inverter.

Notice that the output is the collector of transistor Q_3 with nothing connected to it, hence the name *open collector.* In order to get the proper HIGH and LOW logic levels out of the circuit, an external pull-up resistor must be connected to V_{CC} from the collector of Q_3, as shown in Figure 15–31(b). When Q_3 is off, the output is pulled up to V_{CC} through the external resistor. When Q_3 is on, the output is connected to near-ground through the saturated transistor.

The ANSI/IEEE standard symbol that designates an open-collector output is shown in Figure 15–32 for an inverter and is the same for an open-drain output.

Tri-state TTL Gates

Figure 15–33 shows the basic circuit for a TTL tri-state inverter. When the enable input is LOW, Q_2 is off, and the output circuit operates as a normal totem-pole configuration, in which the output state depends on the input state. When the enable input is HIGH, Q_2 is on. There is thus a LOW on the second emitter of Q_1, causing Q_3 and Q_5 to turn off, and diode D_1 is forward biased, causing Q_4 also to turn off. When both totem-pole transistors are off, they are effectively open, and the output is completely disconnected from the internal circuitry, as illustrated in Figure 15–34.

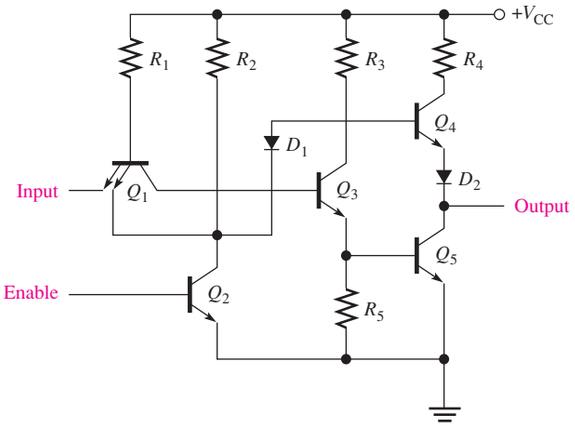


FIGURE 15–33 Basic tri-state inverter circuit.

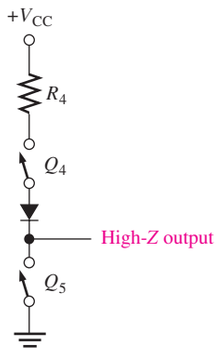


FIGURE 15–34 An equivalent circuit for the tri-state output in the high-Z state.

Schottky TTL

The basic or standard TTL NAND gate circuit was discussed earlier. It is a current-sinking type of logic that draws current from the load when in the LOW output state and sources negligible current to the load when in the HIGH output state. Most TTL logic is some form of Schottky TTL, which provides a faster switching time by incorporating *Schottky* diodes to prevent the transistors from going into saturation, thereby decreasing the time for a transistor to turn on or off. Figure 15–35 shows a Schottky gate circuit. Notice the symbols for the Schottky transistor and Schottky diodes. Schottky devices are designated by an *S* in their part number, such as 74S00. Other types of Schottky TTL are low-power Schottky designated by LS, advanced Schottky designated by AS, advanced low-power Schottky designated by ALS, and fast designated by F.

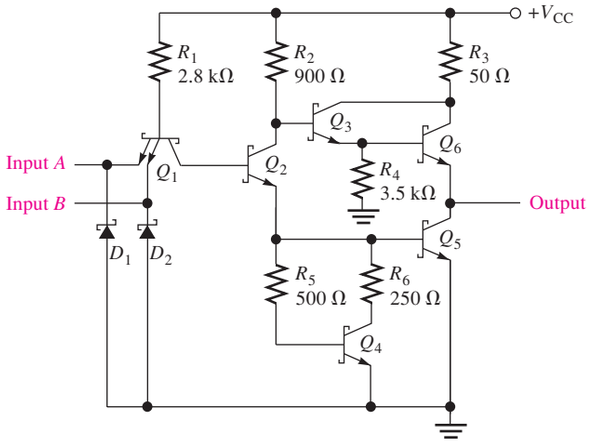


FIGURE 15–35 Schottky TTL NAND gate.

SECTION 15–3 CHECKUP

1. An *npn* BJT is on when the base is more negative than the emitter. (T or F)
2. In terms of switching action, what do the *on* and *off* states of a BJT represent?
3. What are the two major types of output circuits in TTL?
4. Explain how tri-state logic differs from normal, two-state logic.

15–4 Practical Considerations in the Use of TTL

Although CMOS is the more predominant IC technology in industry and commercial applications, TTL is still used but is on the decline. In educational applications, TTL is usually preferred because it does not have the handling restrictions that CMOS does due to ESD. Because of this, several practical considerations in the use and application of TTL circuits will be covered using standard TTL for illustration.

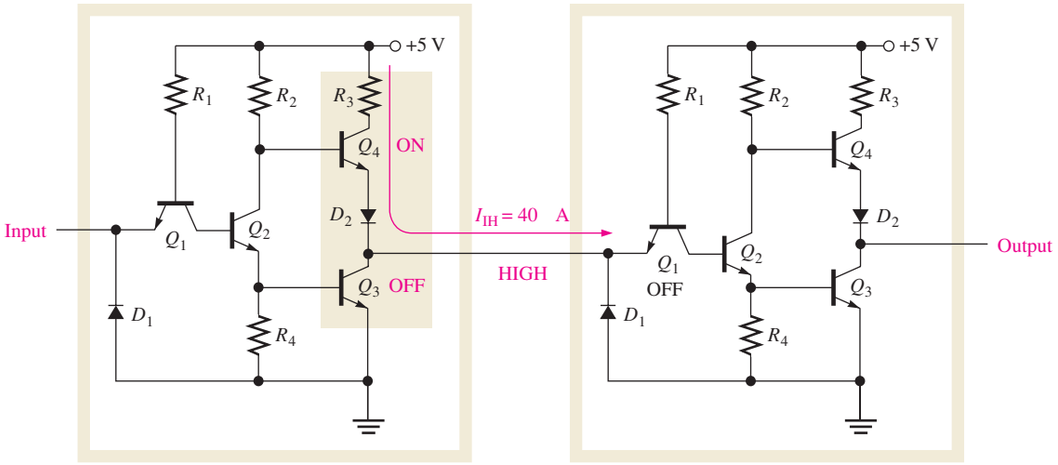
After completing this section, you should be able to

- Describe current sinking and current sourcing
- Use an open-collector circuit for wired-AND operation
- Describe the effects of connecting two or more totem-pole outputs
- Use open-collector gates to drive LEDs and lamps
- Explain what to do with unused TTL inputs

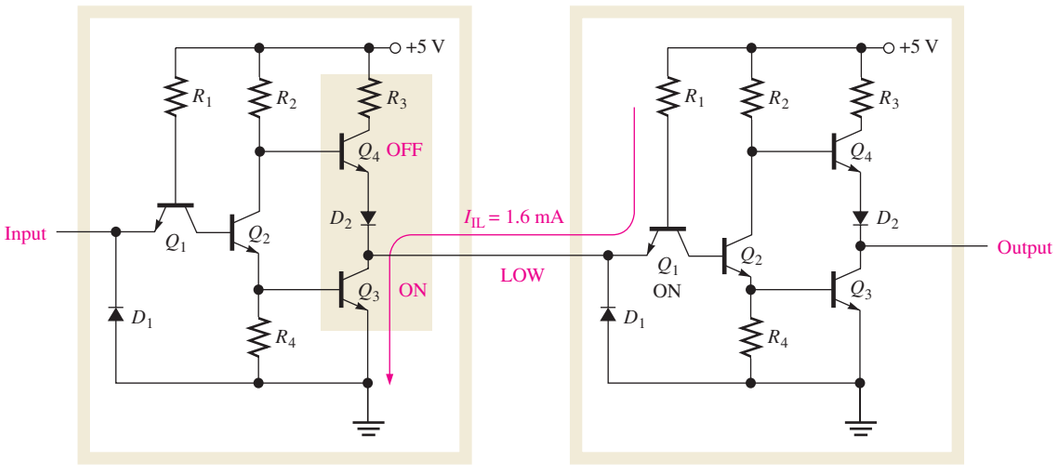
Current Sinking and Current Sourcing

The concepts of current sinking and current sourcing were introduced in Section 15–1. Now that you are familiar with the totem-pole-output circuit configuration used in TTL, let's look closer at the sinking and sourcing action.

Figure 15–36 shows a standard TTL inverter with a totem-pole output connected to the input of another TTL inverter. When the driving gate is in the HIGH output state, the driver is sourcing current to the load, as shown in Figure 15–36(a). The input to the load gate is



(a) Current sourcing (I_{IH} value is maximum)



(b) Current sinking (I_{IL} value is maximum)

FIGURE 15–36 Current sinking and sourcing action in TTL.

like a reverse-biased diode, so there is practically no current required by the load. Actually, since the input is nonideal, there is a maximum of 40 μA from the totem-pole output of the driver into the load gate input.

When the driving gate is in the LOW output state, the driver is sinking current from the load, as shown in Figure 15–36(b). This current is 1.6 mA maximum for standard TTL and is indicated on a **data sheet** with a negative value because it is *out* of the input.

EXAMPLE 15–3

When a standard TTL NAND gate drives five TTL inputs, how much current does the driver output source, and how much does it sink? (Refer to Figure 15–36.)

Solution

Total source current (in HIGH output state):

$$I_{IH(max)} = 40\ \mu\text{A per input}$$

$$I_{T(source)} = (5\ \text{inputs})(40\ \mu\text{A/input}) = 5(40\ \mu\text{A}) = 200\ \mu\text{A}$$

Total sink current (in LOW output state):

$$I_{IL(max)} = -1.6 \text{ mA per input}$$

$$I_{T(sink)} = (5 \text{ inputs})(-1.6 \text{ mA/input}) = 5(-1.6 \text{ mA}) = -8.0 \text{ mA}$$

Related Problem

Repeat the calculations for an LS TTL NAND gate that drives five inputs. Refer to a data sheet available at **www.ti.com**.

EXAMPLE 15–4

Refer to the data sheet available at **www.ti.com**, and determine the fan-out of the 7400 NAND gate.

Solution

According to the data sheet, the current parameters are as follows:

$$I_{IH(max)} = 40\ \mu\text{A} \qquad I_{OH(max)} = -400\ \mu\text{A}$$

$$I_{IL(max)} = -1.6 \text{ mA} \qquad I_{OL(max)} = 16 \text{ mA}$$

Fan-out for the HIGH output state is calculated as follows: Current $I_{OH(max)}$ is the maximum current that the gate can source to a load. Each load input requires an $I_{IH(max)}$ of 40 μA. The HIGH-state fan-out is

$$\left|\frac{I_{OH(max)}}{I_{IH(max)}}\right| = \frac{400\ \mu\text{A}}{40\ \mu\text{A}} = \textbf{10 unit loads}$$

For the LOW output state, fan-out is calculated as follows: $I_{OL(max)}$ is the maximum current that the gate can sink. Each load input produces an $I_{IL(max)}$ of -1.6 mA. The LOW-state fan-out is

$$\left|\frac{I_{OL(max)}}{I_{IL(max)}}\right| = \frac{16 \text{ mA}}{1.6 \text{ mA}} = \textbf{10 unit loads}$$

In this case both the HIGH-state fan-out and the LOW-state fan-out are the same.

Related Problem

Determine the fan-out for a 74LS00 NAND gate.

Using Open-Collector Gates for Wired-AND Operation

The outputs of open-collector gates can be wired together to form what is called a *wired-AND* configuration. Figure 15–37 illustrates how four inverters are connected to produce a 4-input negative-AND gate. A single external pull-up resistor, R_p, is required in all wired-AND circuits.

When one (or more) of the inverter inputs is HIGH, the output X is pulled LOW because an output transistor is on and acts as a closed switch to ground, as illustrated in Figure 15–38(a). In this case only one inverter has a HIGH input, but this is sufficient to pull the output LOW through the saturated output transistor Q_1 as indicated.

For the output X to be HIGH, *all* inverter inputs must be LOW so that all the open-collector output transistors are off, as indicated in Figure 15–38(b). When this condition exists, the output X is pulled HIGH through the pull-up resistor. Thus, the output X is HIGH only when *all* the inputs are LOW. Therefore, we have a negative-AND function, as expressed in the following equation:

$$X = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D}$$

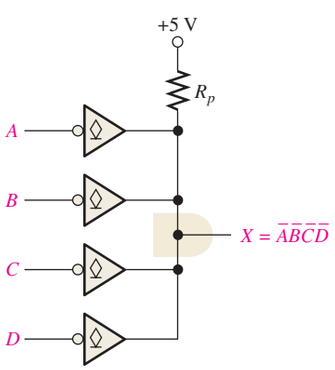
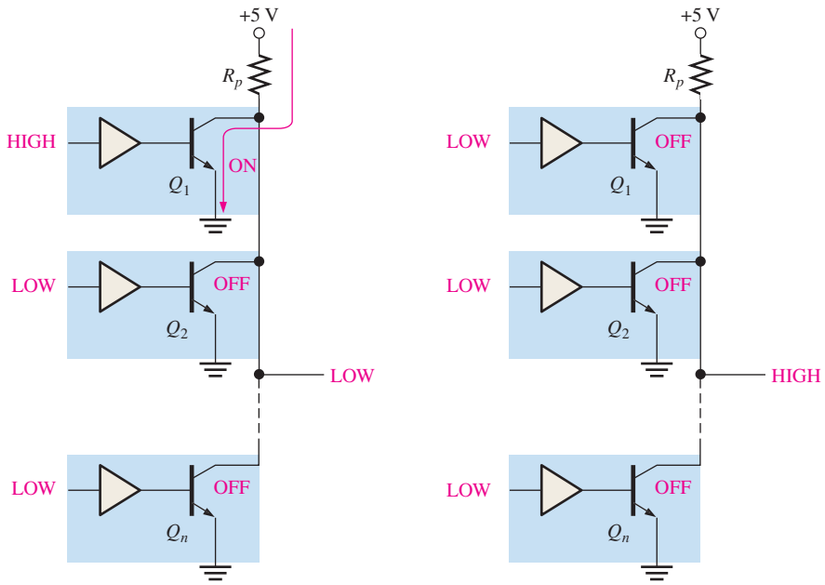


FIGURE 15–37 A wired-AND configuration of four inverters.



(a) When one or more output transistors are on, the output is LOW.

(b) When all output transistors are off, the output is HIGH.

FIGURE 15–38 Open-collector wired negative-AND operation with inverters.

EXAMPLE 15–5

Write the output expression for the wired-AND configuration of open-collector AND gates in Figure 15–39.

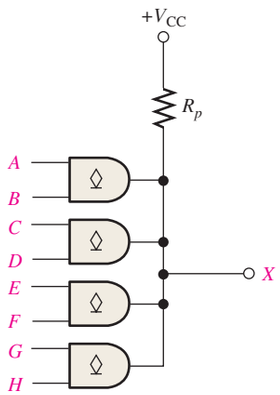


FIGURE 15–39

Solution

The output expression is

$$X = ABCDEFGH$$

The wired-AND connection of the four 2-input AND gates creates an 8-input AND gate.

Related Problem

Determine the output expression if NAND gates are used in Figure 15–39.

EXAMPLE 15–6

Three open-collector AND gates are connected in a wired-AND configuration as shown in Figure 15–40. Assume that the wired-AND circuit is driving four standard TTL inputs (−1.6 mA each).

(a) Write the logic expression for *X*.

(b) Determine the minimum value of R_p if $I_{OL(max)}$ for each gate is 30 mA and $V_{OL(max)}$ is 0.4 V.

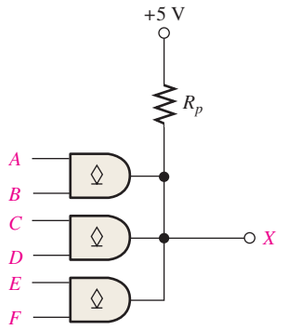


FIGURE 15–40

Solution

(a) $X = ABCDEF$

(b) $4(1.6\text{ mA}) = 6.4\text{ mA}$

$$I_{R_P} = I_{OL(max)} - 6.4\text{ mA} = 30\text{ mA} - 6.4\text{ mA} = 23.6\text{ mA}$$

$$R_P = \frac{V_{CC} - V_{OL(max)}}{I_{R_P}} = \frac{5\text{ V} - 0.4\text{ V}}{23.6\text{ mA}} = \mathbf{195\ \Omega}$$

Related Problem

Show the wired-AND circuit for a 10-input AND function using 74LS09 quad 2-input AND gates.

Connection of Totem-Pole Outputs

Totem-pole outputs cannot be connected together because such a connection might produce excessive current and result in damage to the devices. For example, in Figure 15–41, when Q_1 in device A and Q_2 in device B are both on, the output of device A is effectively shorted to ground through Q_2 of device B.

Open-Collector Buffer/Drivers

A TTL circuit with a totem-pole output is limited in the amount of current that it can sink in the LOW state ($I_{OL(max)}$) to 16 mA for standard TTL and 8 mA for LS TTL. In many special applications, a gate must drive external devices, such as LEDs, lamps, or relays, that may require more current than that.

Because of their higher voltage and current-handling capability, circuits with open-collector outputs are generally used for driving LEDs, lamps, or relays. However, totem-pole outputs can be used, as long as the output current required by the external device does not exceed the amount that the TTL driver can sink.

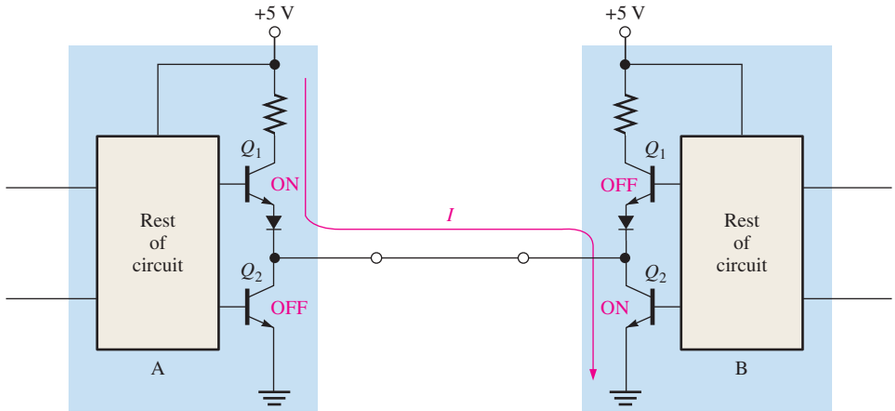
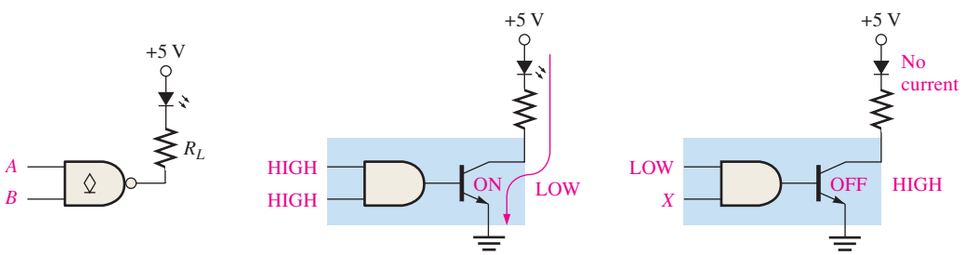
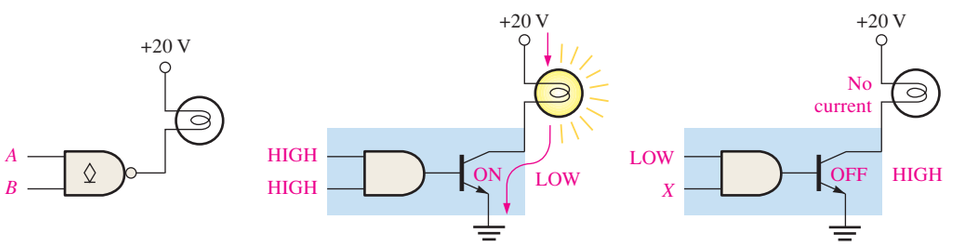


FIGURE 15–41 Totem-pole outputs wired together. Such a connection may cause excessive current through Q_1 of device A and Q_2 of device B and should never be used.

With an open-collector TTL gate, the collector of the output transistor is connected to an **LED** or incandescent lamp, as illustrated in Figure 15–42. In part (a) the limiting resistor, R_L, is used to keep the current below maximum LED current. When the output of the gate is LOW, the output transistor is sinking current, and the LED is on. The LED is off when the output transistor is off and the output is HIGH. A typical open-collector buffer gate can sink up to 40 mA. In part (b) of the figure, the lamp requires no limiting resistor because the filament is resistive. Typically, up to +30 V can be used on the open collector, depending on the particular logic family.



(a) Driving an LED



(b) Driving a low-current lamp

FIGURE 15–42 Some applications of open-collector drivers.

EXAMPLE 15–7

Determine the value of the limiting resistor, R_L, in the open-collector circuit of Figure 15–43 if the LED current is to be 20 mA. Assume a 1.5 V drop across the LED when it is forward-biased and a LOW-state output voltage of 0.1 V at the output of the gate.

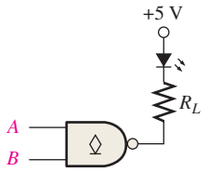


FIGURE 15–43

Solution

$$V_{R_L} = 5\text{ V} - 1.5\text{ V} - 0.1\text{ V} = 3.4\text{ V}$$

$$R_L = \frac{V_{R_L}}{I} = \frac{3.4\text{ V}}{20\text{ mA}} = \mathbf{170\ \Omega}$$

Related Problem

Determine the value of the limiting resistor, R_L, if the LED requires 35 mA.

Unused TTL Inputs

An unconnected input on a TTL gate acts as a HIGH because an open input results in a reverse-biased emitter junction on the input transistor, just as a HIGH level does. This effect is illustrated in Figure 15–44. However, because of noise sensitivity, it is best not to leave unused TTL inputs unconnected (open). There are several alternative ways to handle unused inputs.

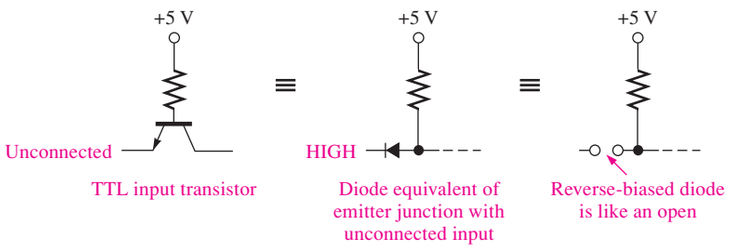


FIGURE 15–44 Comparison of an open TTL input and a HIGH-level input.

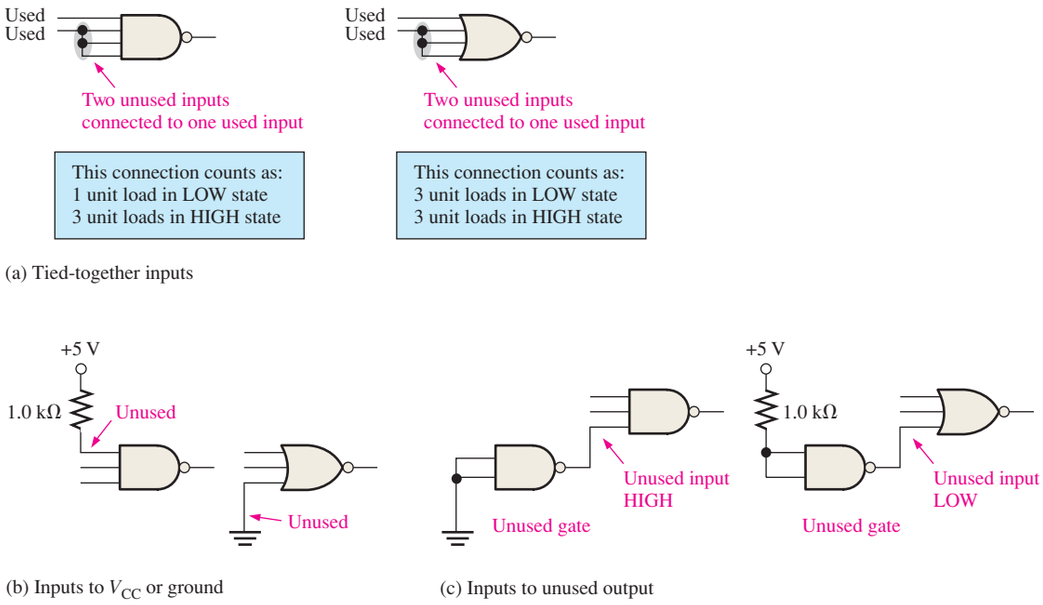
Tied-Together Inputs

The most common method for handling unused gate inputs is to connect them to a used input of the same gate. For AND gates and NAND gates, all tied-together inputs count as one unit load in the LOW state; but for OR gates and NOR gates, each input tied to another input counts as a separate unit load in the LOW state. In the HIGH state, each tied-together input counts as a separate load for all types of TTL gates. In Figure 15–45(a) are two examples of the connection of two unused inputs to a used input.

The AND and NAND gates present only a single unit load no matter how many inputs are tied together, whereas OR and NOR gates present a unit load for each tied-together input. This is because the NAND gate uses a multiple-emitter input transistor; so no matter how many inputs are LOW, the total LOW-state current is limited to a fixed value. The NOR gate uses a separate transistor for each input; therefore, the LOW-state current is the sum of the currents from all the tied-together inputs.

Inputs to V_{CC} or Ground

Unused inputs of AND and NAND gates can be connected to V_{CC} through a 1.0 kΩ resistor. This connection pulls the unused inputs to a HIGH level. Unused inputs of OR and NOR gates can be connected to ground. These methods are illustrated in Figure 15–45(b).



(a) Tied-together inputs

(b) Inputs to V_{CC} or ground

(c) Inputs to unused output

FIGURE 15–45 Methods for handling unused TTL inputs.

Inputs to Unused Output

A third method of terminating unused inputs may be appropriate in some cases when an unused gate or inverter is available. The unused gate output must be a constant HIGH for unused AND and NAND inputs and a constant LOW for unused OR and NOR inputs, as illustrated in Figure 15–45(c).

SECTION 15–4 CHECKUP

1. In what output state does a TTL circuit sink current from a load?
2. Why does a TTL circuit source less current into a TTL load than it sinks?
3. Why can TTL circuits with totem-pole outputs not be connected together?
4. What type of TTL circuit must be used for a wired-AND configuration?
5. Why type of TTL circuit would you use to drive a lamp?
6. An unconnected TTL input acts as a LOW. (T or F)

15–5 Comparison of CMOS and TTL Performance

In this section, the main operational and performance characteristics of selected CMOS series are compared with those of the major TTL series and with BiCMOS.

After completing this section, you should be able to

- Compare bipolar (TTL), BiMOS, and CMOS devices in terms of propagation delay, maximum clock frequency, power dissipation, and drive capability

In the past, the superior characteristic of TTL (bipolar) compared to CMOS was its relatively high speed and output current capability. These advantages of TTL have diminished to the point where CMOS is often equal or superior in many areas and has become the dominant IC technology, although TTL is still available and in use. One family of IC

logic devices, BiCMOS, combines CMOS logic with TTL output circuitry in an effort to combine the advantages of both.

Table 15–1 provides a comparison of the performance of several IC logic families.

TABLE 15–1

Comparison of selected performance parameters of several 74XX IC families.

	Bipolar (TTL)			BiCMOS	CMOS					
					5 V			3.3 V		
	F	LS	ALS	ABT	HC	AC	AHC	LV	LVC	ALVC
Speed										
Gate propagation delay, t_p (ns)	3.3	10	7	3.2	7	5	3.7	9	4.3	3
FF maximum clock freq. (MHz)	145	33	45	150	50	160	170	90	100	150
Power Dissipation Per Gate										
Bipolar: 50% dc (mW)	6	2.2	1.4							
CMOS: quiescent (μW)				17	2.75	0.55	2.75	1.6	0.8	0.8
Output Drive										
I_{OL} (mA)	20	8	8	64	4	24	8	12	24	24

SECTION 15–5 CHECKUP

1. What is a BiCMOS circuit?
2. In general, what is the main advantage of CMOS over bipolar (TTL)?

15–6 Emitter-Coupled Logic (ECL) Circuits

Emitter-coupled logic, like TTL, is a bipolar technology. The typical ECL circuit consists of a different amplifier input circuit, a bias circuit, and emitter-follower outputs. ECL is much faster than TTL because the transistors do not operate in saturation and is used in more specialized high-speed applications.

After completing this section, you should be able to

- Describe how ECL differs from TTL and CMOS
- Explain the advantages and disadvantages of ECL

An **ECL** OR/NOR gate is shown in Figure 15–46(a). The emitter-follower outputs provide the OR logic function and its NOR complement, as indicated by Figure 15–46(b).

Because of the low output impedance of the emitter-follower and the high input impedance of the differential amplifier input, high fan-out operation is possible. In this type of circuit, saturation is not possible. The lack of saturation results in higher power consumption and limited voltage swing (less than 1 V), but it permits high-frequency switching.

The V_{CC} pin is normally connected to ground, and the V_{EE} pin is connected to −5.2 V from the power supply for best operation. Notice that in Figure 15–46(c) the output varies from a LOW level of −1.75 V to a HIGH level of −0.9 V with respect to ground. In positive logic, a 1 is the HIGH level (less negative), and a 0 is the LOW level (more negative).

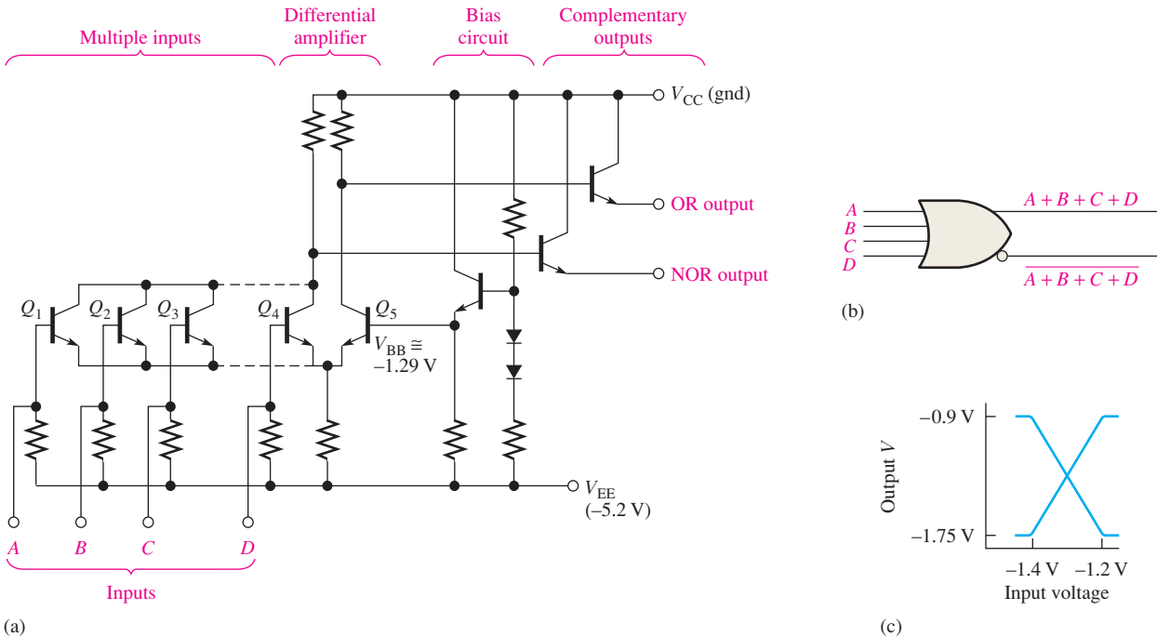


FIGURE 15–46 An ECL OR/NOR gate circuit.

Noise Margin

As you have learned, the noise margin of a gate is the measure of its immunity to undesired voltage fluctuations (noise). Typical ECL circuits have noise margins from about 0.2 V to 0.25 V. These are less than for TTL and make ECL less suitable in high-noise environments.

Comparison of ECL with TTL and CMOS

Table 15–2 shows a comparison of key performance parameters for F, AHC, and ECL.

TABLE 15–2

Comparison of ECL series performance parameters with F and AHC.

	Bipolar (TTL) F	CMOS AHC	Bipolar (ECL)
Speed			
Gate propagation delay, t_p (ns)	3.3	3.7	0.22–1
FF maximum clock freq. (MHz)	145	170	330–2800
Power Dissipation Per Gate			
Bipolar: 50% dc	6 mW		25 mW–73 mW
CMOS: quiescent		2.75 μW	

SECTION 15–6 CHECKUP

1. What is the primary advantage of ECL over TTL?
2. Name two disadvantages of ECL compared with TTL.

15–7 PMOS, NMOS, and E^{2}CMOS

The PMOS and NMOS circuits are used largely in LSI functions, such as long shift registers, large memories, and microprocessor products. Such use is a result of the low power consumption and very small chip area required for MOS transistors. E^{2}CMOS is used in reprogrammable PLDs.

After completing this section, you should be able to

- Describe a basic PMOS gate
- Describe a basic NMOS gate
- Describe a basic E^{2}CMOS cell

PMOS

One of the first high-density **MOS** circuit technologies to be produced was **PMOS**. It utilizes enhancement-mode *p*-channel MOS transistors to form the basic gate building blocks. Figure 15–47 shows a basic PMOS gate that produces the NOR function in positive logic.

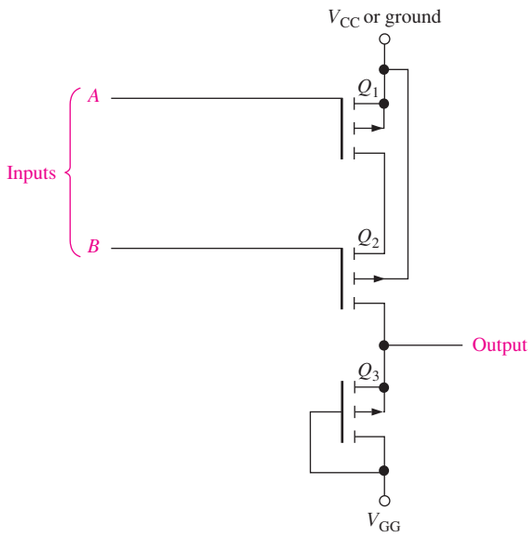


FIGURE 15–47 Basic PMOS gate.

The operation of the PMOS gate is as follows: The supply voltage V_{GG} is a negative voltage, and V_{CC} is a positive voltage or ground (0 V). Transistor Q_3 is permanently biased to create a constant drain-to-source resistance. Its sole purpose is to function as a current-limiting resistor. If a HIGH (V_{CC}) is applied to input *A* or *B*, then Q_1 or Q_2 is off, and the output is pulled down to a voltage near V_{GG}, which represents a LOW. When a LOW voltage (V_{GG}) is applied to both input *A* and input *B,* both Q_1 and Q_2 are turned on. This causes the output to go to a HIGH level (near V_{CC}). Since a LOW output occurs when either or both inputs are HIGH, and a HIGH output occurs only when all inputs are LOW, we have a NOR gate.

NMOS

The NMOS devices were developed as processing technology improved. The *n*-channel MOS transistor is used in NMOS circuits, as shown in Figure 15–48 for a NAND gate and a NOR gate.

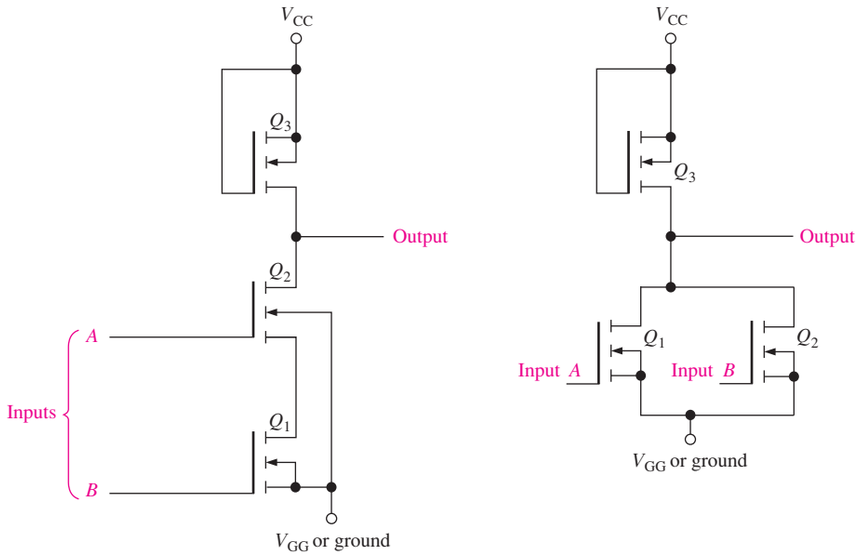


FIGURE 15–48 Two NMOS gates.

In Figure 15–48(a), Q_3 acts as a resistor to limit current. When a LOW (V_{GG} or ground) is applied to one or both inputs, then at least one of the transistors (Q_1 or Q_2) is off, and the output is pulled up to a HIGH level near V_{CC}. When HIGHs (V_{CC}) are applied to both A and B, both Q_1 and Q_2 conduct, and the output is LOW. This action, of course, identifies this circuit as a NAND gate.

In Figure 15–48(b), Q_3 again acts as a resistor. A HIGH on either input turns Q_1 or Q_2 on, pulling the output LOW. When both inputs are LOW, both transistors are off, and the output is pulled up to a HIGH level.

E^2CMOS

E^2CMOS (electrically erasable CMOS) technology is based on a combination of CMOS and NMOS technologies and is used in programmable devices such as PROMs and CPLDs. An E^2CMOS cell is built around a MOS transistor with a floating gate that is externally charged or discharged by a small programming current. A schematic of this type of cell is shown in Figure 15–49.

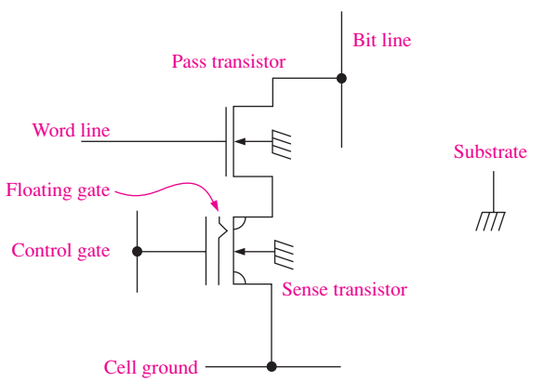


FIGURE 15–49 An E^2CMOS cell.

When the floating gate is charged to a positive potential by removing electrons, the sense transistor is turned on, storing a binary zero. When the floating gate is charged to a negative potential by placing electrons on it, the sense transistor is turned off, storing a binary 1. The control gate controls the potential of the floating gate. The pass transistor isolates the sense transistor from the array during read and write operations that use the word and bit lines.

The cell is programmed by applying a programming pulse to either the control gate or the bit line of a cell that has been selected by a voltage on the word line. During the programming cycle, the cell is first erased by applying a voltage to the control gate to make the floating gate negative. This leaves the sense transistor in the *off* state (storing a 1). A write pulse is applied to the bit line of a cell in which a 0 is to be stored. This will charge the floating gate to a point where the sense transistor is on (storing a 0). The bit stored in the cell is read by sensing presence or absence of a small cell current in the bit line. When a 1 is stored, there is no cell current because the sense transistor is off. When a 0 is stored, there is a small cell current because the sense transistor is on. Once a bit is stored in a cell, it will remain indefinitely unless the cell is erased or a new bit is written into the cell.

SECTION 15–7 CHECKUP

1. What is the main feature of NMOS and PMOS technology in integrated circuits?
2. What is the mechanism for charge storage in an E^2CMOS cell?

SUMMARY

- *Formulas:*

15–1 $V_{NH} = V_{OH(min)} - V_{IH(min)}$ High-level noise margin

15–2 $V_{NL} = V_{IL(max)} - V_{OL(max)}$ Low-level noise margin

15–3 $I_{CC} = \dfrac{I_{CCH} + I_{CCL}}{2}$ Average dc supply current

15–4 $P_D = V_{CC}I_{CC}$ Power dissipation

- Totem-pole outputs of TTL cannot be connected together.
- Open-collector and open-drain outputs can be connected for wired-AND.
- CMOS devices offer lower power dissipation than any of the TTL series.
- A TTL device is not as vulnerable to electrostatic discharge (ESD) as is a CMOS device.
- Because of ESD, CMOS devices must be handled with great care.
- ECL is the fastest type of logic circuit.
- E^2CMOS is used in PROMs and other PLDs.

KEY TERMS

Key terms and other bold terms in the chapter are defined in the end-of-book glossary.

CMOS Complementary metal-oxide semiconductor; a type of integrated logic circuit that uses *n*- and *p*-channel MOSFETs (metal-oxide semiconductor field-effect transistors).

Current sinking The action of a logic circuit in which it accepts current into its output from a load.

Current sourcing The action of a logic circuit in which it sends current from its output to a load.

ECL Emitter-coupled logic; a class of integrated logic circuits that are implemented with nonsaturating bipolar junction transistors.

E^2CMOS Electrically erasable CMOS; the IC technology used in programmable logic devices (PLDs).

Fan-out The number of equivalent gate inputs of the same family series that a logic gate can drive.

Noise immunity The ability of a logic circuit to reject unwanted signals (noise).

Noise margin The difference between the maximum LOW output of a gate and the maximum acceptable LOW input of an equivalent gate; also, the difference between the minimum HIGH output of a gate and the minimum HIGH input of an equivalent gate. Noise margin is sometimes expressed as a percentage of the dc supply voltage.

Open-collector A type of output for a TTL circuit in which the collector of the output transistor is left internally disconnected and is available for connection to an external load that requires relatively high current or voltage.

Power dissipation The product of the dc supply voltage and the dc supply current in an electronic circuit.

Propagation delay time The time interval between the occurrence of an input transition and the occurrence of the corresponding output transition in a logic circuit.

Pull-up resistor A resistor with one end connected to the dc supply voltage used to keep a given point in a logic circuit HIGH when in the inactive state.

Totem pole A type of output in TTL circuits.

Tri-state A type of output in logic circuits that exhibits three states: HIGH, LOW, and high *Z*.

TTL Transistor-transistor logic; a type of integrated circuit that uses bipolar junction transistors. Also called *bipolar*.

Unit load A measure of fan-out. One gate input represents a unit load to a driving gate.

TRUE/FALSE QUIZ

Answers are at the end of the chapter.

1. The dc supply voltage for TTL is typically +5 V.
2. The fan-out of a logic gate is the number of gates in an IC package.
3. CMOS uses MOSFETs.
4. BJT stands for binary junction transistor.
5. An open-collector gate must be connected to an external resistor.
6. CMOS is the dominant digital IC technology.
7. A totem-pole output means that two or more resistors are in series.
8. CMOS is subject to ESD.
9. A tri-state output can be HIGH, LOW or high-impedance.
10. Propagation delay is a measure of the speed of a logic gate.

SELF-TEST

Answers are at the end of the chapter.

1. When the frequency of the input signal to a CMOS gate is increased, the average power dissipation
   (a) decreases **(b)** increases
   (c) does not change **(d)** decreases exponentially
2. CMOS operates more reliably than TTL in a high-noise environment because of its
   (a) lower noise margin **(b)** input capacitance
   (c) higher noise margin **(d)** smaller power dissipation
3. Proper handling of a CMOS device is necessary because of its
   (a) fragile construction
   (b) high-noise immunity
   (c) susceptibility to electrostatic discharge
   (d) low power dissipation
4. Which of the following is not a TTL circuit?
   (a) 74F00 **(b)** 74AS00
   (c) 74HC00 **(d)** 74ALS00

5. An open TTL NOR gate input
(a) acts as a LOW **(b)** acts as a HIGH
(c) should be grounded **(d)** should be connected to V_{CC} through a resistor
(e) answers (b) and (c) **(f)** answers (a) and (c)

6. An LS TTL gate can drive a maximum of
(a) 20 unit loads **(b)** 10 unit loads
(c) 40 unit loads **(d)** unlimited unit loads

7. If two unused inputs of a LS TTL gate are connected to an input being driven by another LS TTL gate, the total number of remaining unit loads that can be driven by this gate is
(a) seven **(b)** eight
(c) seventeen **(d)** unlimited

8. The main advantage of ECL over TTL or CMOS is
(a) ECL is less expensive
(b) ECL consumes less power
(c) ECL is available in a greater variety of circuit types
(d) ECL is faster

9. ECL cannot be used in
(a) high-noise environments
(b) damp environments
(c) high-frequency applications

10. The basic mechanism for storing a data bit in an E^2CMOS cell is
(a) control gate **(b)** floating drain
(c) floating gate **(d)** cell current

PROBLEMS

Answers to odd-numbered problems are at the end of the book.

Section 15–1 Basic Operational Characteristics and Parameters

1. A certain logic gate has a $V_{OH(min)} = 2.2$ V, and it is driving a gate with a $V_{IH(min)} = 2.5$ V. Are these gates compatible for HIGH-state operation? Why?

2. A certain logic gate has a $V_{OL(max)} = 0.45$ V, and it is driving a gate with a $V_{IL(max)} = 0.75$ V. Are these gates compatible for LOW-state operation? Why?

3. A TTL gate has the following actual voltage level values: $V_{IH(min)} = 2.25$ V, $V_{IL(max)} = 0.65$ V. Assuming it is being driven by a gate with $V_{OH(min)} = 2.4$ V and $V_{OL(max)} = 0.4$ V, what are the HIGH- and LOW-level noise margins?

4. What is the maximum amplitude of noise spikes that can be tolerated on the inputs in both the HIGH state and the LOW state for the gate in Problem 3?

5. Voltage specifications for three types of logic gates are given in Table 15–3. Select the gate that you would use in a high-noise industrial environment.

TABLE 15–3

	$V_{OH(min)}$	$V_{OL(max)}$	$V_{IH(min)}$	$V_{IL(max)}$
Gate *A*	2.4 V	0.4 V	2 V	0.8 V
Gate *B*	3.5 V	0.2 V	2.5 V	0.6 V
Gate *C*	4.2 V	0.2 V	3.2 V	0.8 V

6. A certain gate draws a dc supply current from a +5 V source of 2 mA in the LOW state and 3.5 mA in the HIGH state. What is the power dissipation in the LOW state? What is the power dissipation in the HIGH state? Assuming a 50% duty cycle, what is the average power dissipation?

7. Each gate in the circuit of Figure 15–50 has a t_{PLH} and a t_{PHL} of 4 ns. If a positive-going pulse is applied to the input as indicated, how long will it take the output pulse to appear?

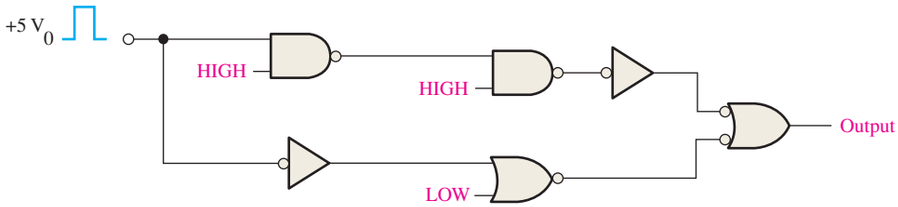


FIGURE 15–50

8. For a certain gate, $t_{PLH} = 3$ ns and $t_{PHL} = 2$ ns. What is the average propagation delay time?

9. Table 15–4 lists parameters for three types of gates. Basing your decision on the speed-power product, which one would you select for best performance?

TABLE 15–4

	t_{PLH}	t_{PHL}	P_D
Gate *A*	1 ns	1.2 ns	15 mW
Gate *B*	5 ns	4 ns	8 mW
Gate *C*	10 ns	10 ns	0.5 mW

10. Which gate in Table 15–4 would you select if you wanted the gate to operate at the highest possible frequency?

11. A standard TTL gate has a fan-out of 10 unit loads. Are any of the gates in Figure 15–51 overloaded? If so, which ones?

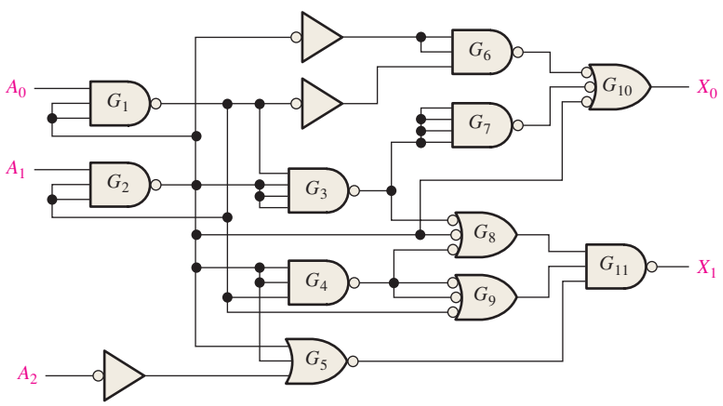


FIGURE 15–51

12. Which CMOS gate network in Figure 15–52 can operate at the highest frequency?

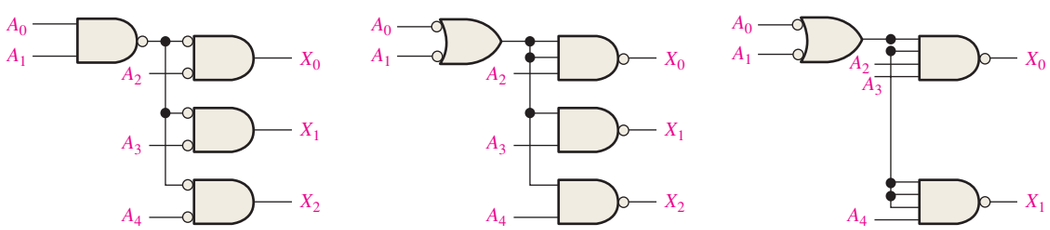


FIGURE 15–52

Section 15–2 CMOS Circuits

13. Determine the state (on or off) of each MOSFET in Figure 15–53.

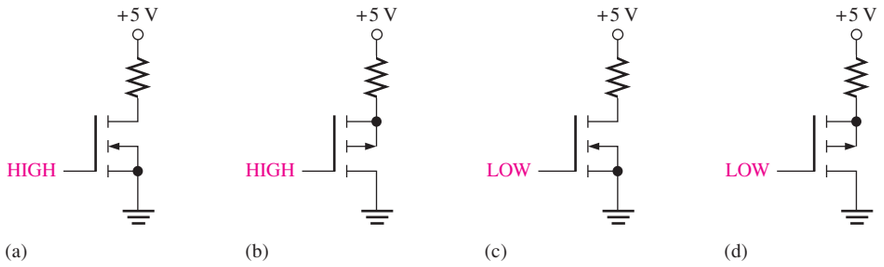


FIGURE 15–53

14. The CMOS gate network in Figure 15–54 is incomplete. Indicate the changes that should be made.

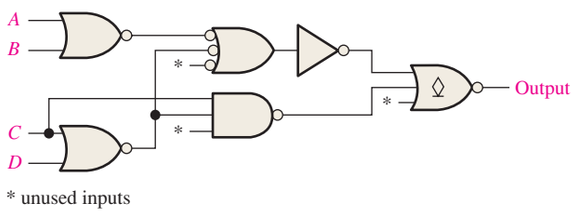


FIGURE 15–54

15. Devise a circuit, using appropriate CMOS logic gates and/or inverters, with which signals from four different sources can be connected to a common line at different times without interfering with each other.

Section 15–3 TTL (Bipolar) Circuits

16. Determine which BJTs in Figure 15–55 are off and which are on.

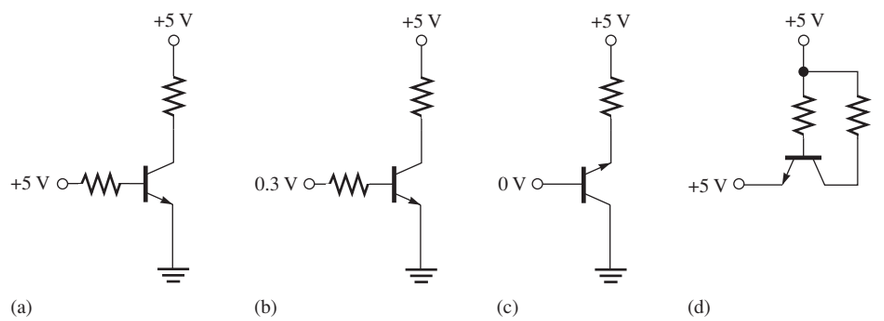


FIGURE 15–55

17. Determine the output state of each TTL gate in Figure 15–56.

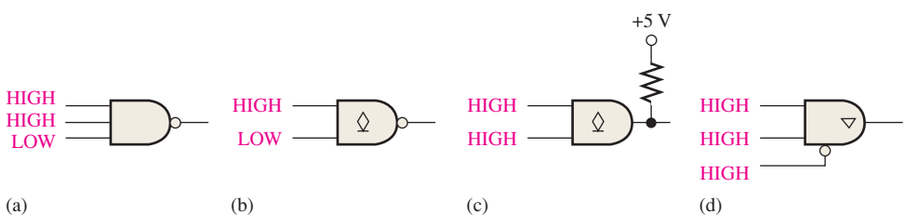


FIGURE 15–56

18. The TTL gate network in Figure 15–57 is incomplete. Indicate the changes that should be made.

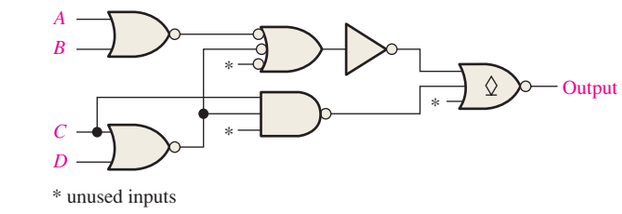


FIGURE 15–57

Section 15–4 Practical Considerations in the Use of TTL

19. Determine the output level of each TTL gate in Figure 15–58.

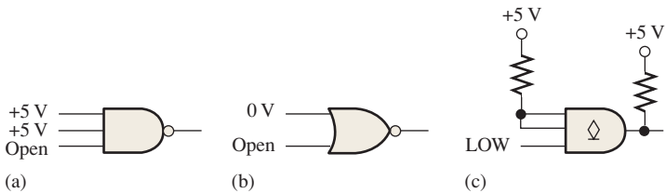


FIGURE 15–58

20. For each part of Figure 15–59, tell whether each driving gate is sourcing or sinking current. Specify the maximum current out of or into the output of the driving gate or gates in each case. All gates are standard TTL.

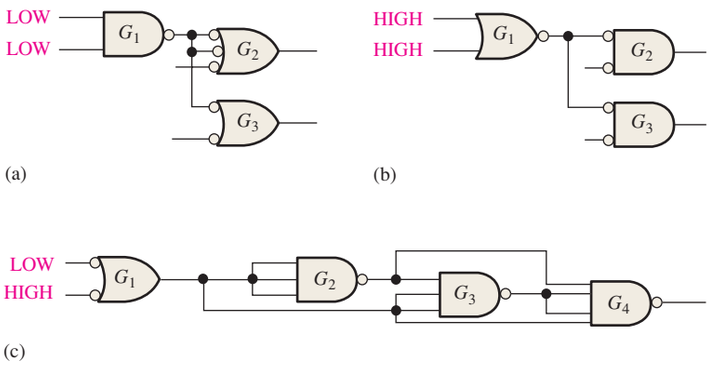


FIGURE 15–59

21. Use open-collector inverters to implement the following logic expressions:

(a) $X = \overline{A}\,\overline{B}\,\overline{C}$

(b) $X = A\overline{B}C\overline{D}$

(c) $X = ABC\overline{D}\,\overline{E}\,\overline{F}$

22. Write the logic expression for each of the circuits in Figure 15–60.

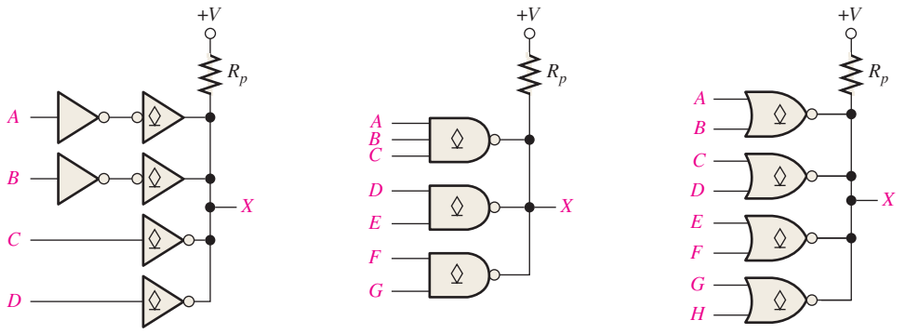


FIGURE 15–60

23. Determine the minimum value for the pull-up resistor in each circuit in Figure 15–60 if $I_{OL(max)} = 40$ mA and $V_{OL(max)} = 0.25$ V for each gate. Assume that 10 standard TTL unit loads are being driven from output X and the supply voltage is 5 V.

24. A certain relay requires 60 mA. Devise a way to use open-collector NAND gates with $I_{OL(max)} = 40$ mA to drive the relay.

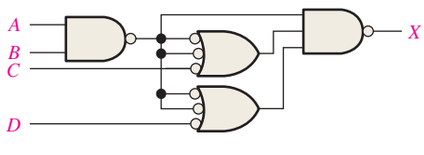
Section 15–5 Comparison of CMOS and TTL Performance

25. Select the IC family with the best speed-power product in Table 15–1.

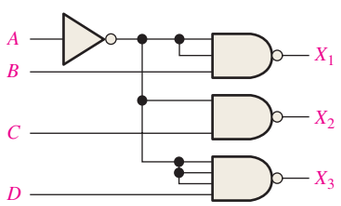
26. Determine from Table 15–1 the logic family that is most appropriate for each of the following requirements:

(a) shortest propagation delay time
(b) fastest flip-flop toggle rate
(c) lowest power dissipation
(d) best compromise between speed and power for a logic gate

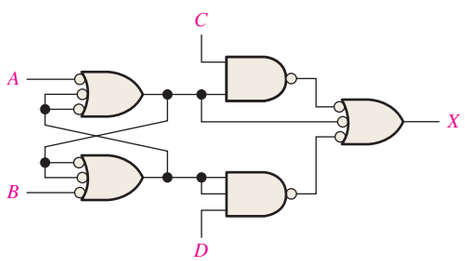
27. Determine the total propagation delay from each input to each output for each circuit in Figure 15–61.



(a) 74FXX gates



(b) 74HCXX gates



(c) 74AHCXX gates

FIGURE 15–61

28. One of the flip-flops in Figure 15–62 may have an erratic output. Which one is it if any and why?

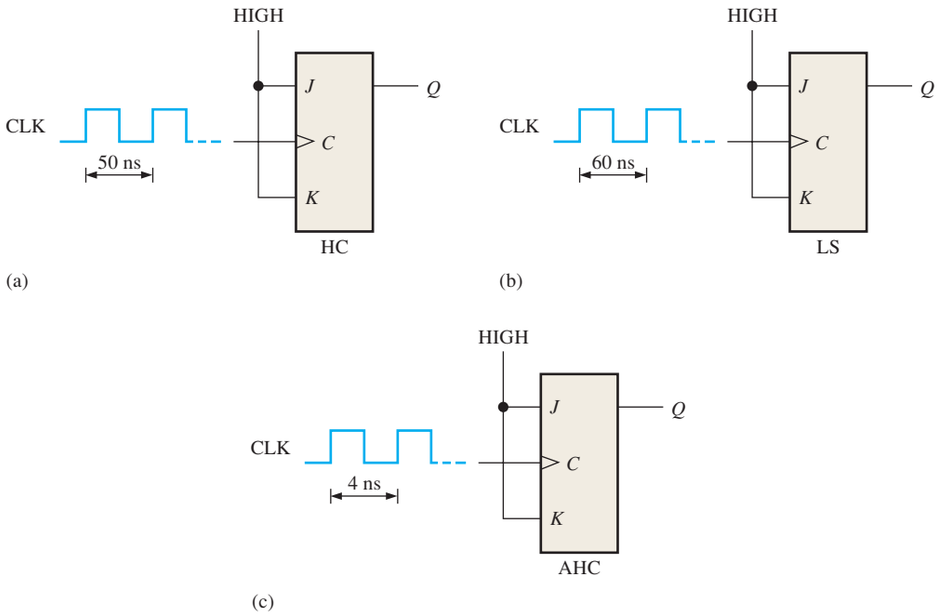


FIGURE 15–62

Section 15–6 Emitter-Coupled Logic (ECL) Circuits

29. What is the basic difference between ECL circuitry and TTL circuitry?

30. Select ECL, CMOS HC series, or the appropriate TTL series for each of the following requirements:

(a) highest speed
(b) lowest power
(c) best compromise between high speed and low power (speed-power product)

ANSWERS

SECTION CHECKUPS

Section 15–1 Basic Operational Characteristics and Parameters

1. V_{IH}: HIGH level input voltage: V_{IL}: LOW level input voltage; V_{OH}: HIGH level output voltage; V_{OL}: LOW level output voltage

2. A higher value of noise margin is better.

3. Gate *B* can operate at a higher frequency.

4. Excessive loading reduces the noise margin of a gate.

Section 15–2 CMOS Circuits

1. MOSFETs are used in CMOS logic.

2. A complementary output circuit consists of an *n*-channel and a *p*-channel MOSFET.

3. Because electrostatic discharge can damage CMOS devices

Section 15–3 TTL (Bipolar) Circuits

1. False, the *npn* BJT is off.

2. The *on* state of a BJT is a closed switch; the *off* state is an open switch.

3. Totem-pole and open-collector are types of TTL outputs.

4. Tri-state logic provides a high-impedance state, in which the output is disconnected from the rest of the circuit.

Section 15–4 Practical Considerations in the Use of TTL

1. Sink current occurs in a LOW output state.
2. Source current is less than sink current because a TTL load looks like a reverse-biased diode in the HIGH state.
3. The totem-pole transistors cannot handle the current when one output tries to go HIGH and the other is LOW.
4. Wired-AND must use open-collector.
5. Lamp driver must be open-collector.
6. False, an unconnected TTL input generally acts as a HIGH.

Section 15–5 Comparison of CMOS and TTL Performance

1. BiCMOS uses bipolar transistors for input and output circuitry and CMOS in between.
2. CMOS has lower power dissipation than bipolar.

Section 15–6 Emitter-Coupled Logic (ECL) Circuits

1. ECL is faster than TTL.
2. ECL has more power and less noise margin than TTL.

Section 15–7 PMOS, NMOS, and E^{2}CMOS

1. NMOS and PMOS are high density.
2. The floating gate is the mechanism for storing charge in an E^{2}CMOS cell.

RELATED PROBLEMS FOR EXAMPLES

15–1 CMOS

15–2 10.75 μW

15–3 $I_{T(source)} = 5(20\ \mu A) = 100\ \mu A$

$I_{T(sink)} = 5(-0.4\ mA) = -2.0\ mA$

15–4 Fan-out = 20 unit loads

15–5 $X = (\overline{AB})(\overline{CD})(\overline{EF})(\overline{GH}) = (\overline{A} + \overline{B})(\overline{C} + \overline{D})(\overline{E} + \overline{F})(\overline{G} + \overline{H})$

15–6 See Figure 15–63.

15–7 $R_L = 97\ \Omega$

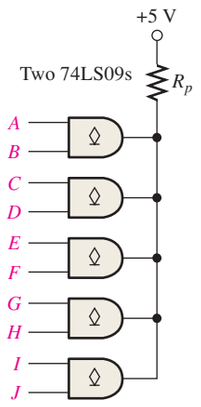


FIGURE 15–63

TRUE/FALSE QUIZ

1. T **2.** F **3.** T **4.** F **5.** T
6. T **7.** F **8.** T **9.** T **10.** T

SELF-TEST

1. (b) **2.** (c) **3.** (c) **4.** (c) **5.** (e)
6. (a) **7.** (c) **8.** (d) **9.** (a) **10.** (c)