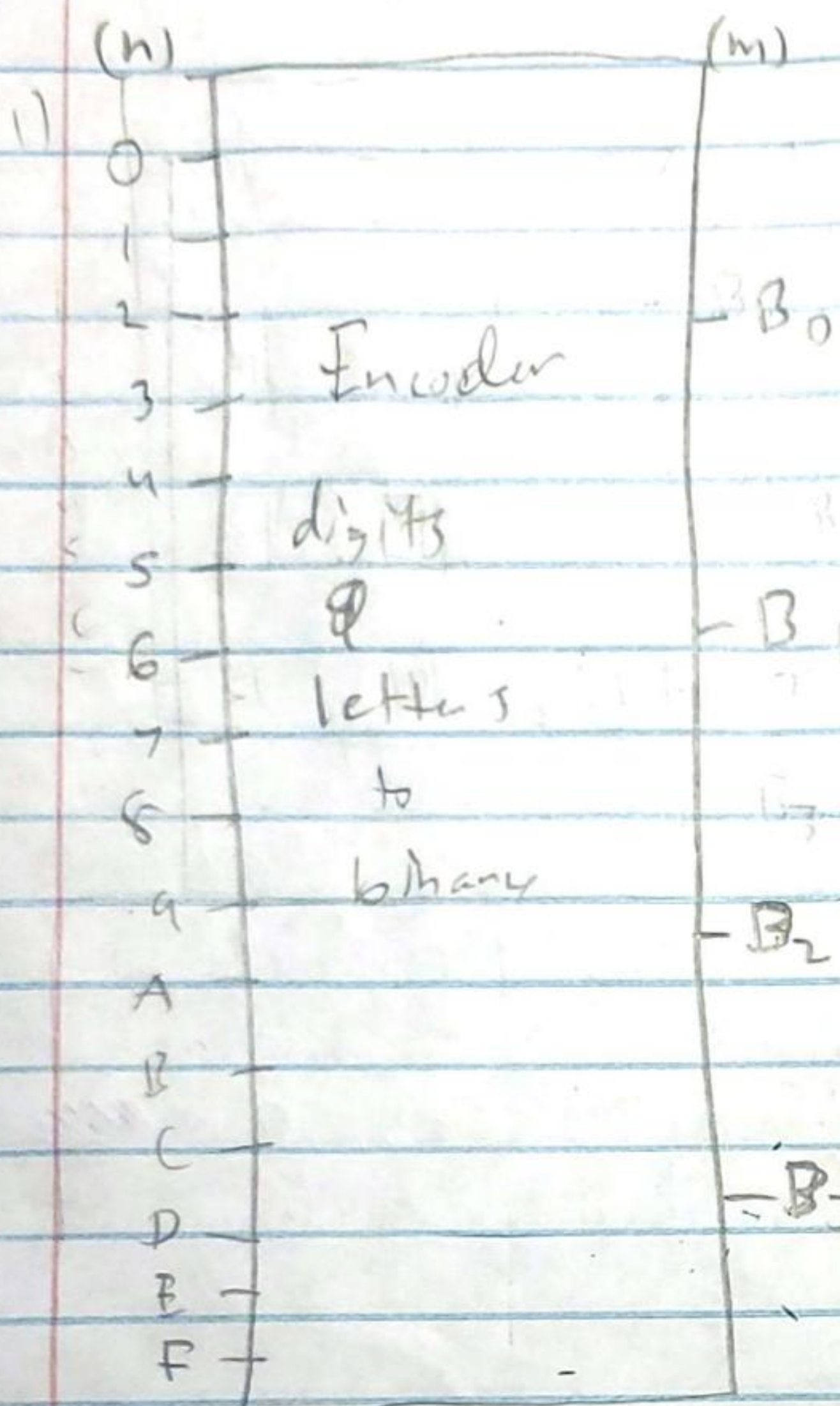


Midterm 2

13

5-1-20

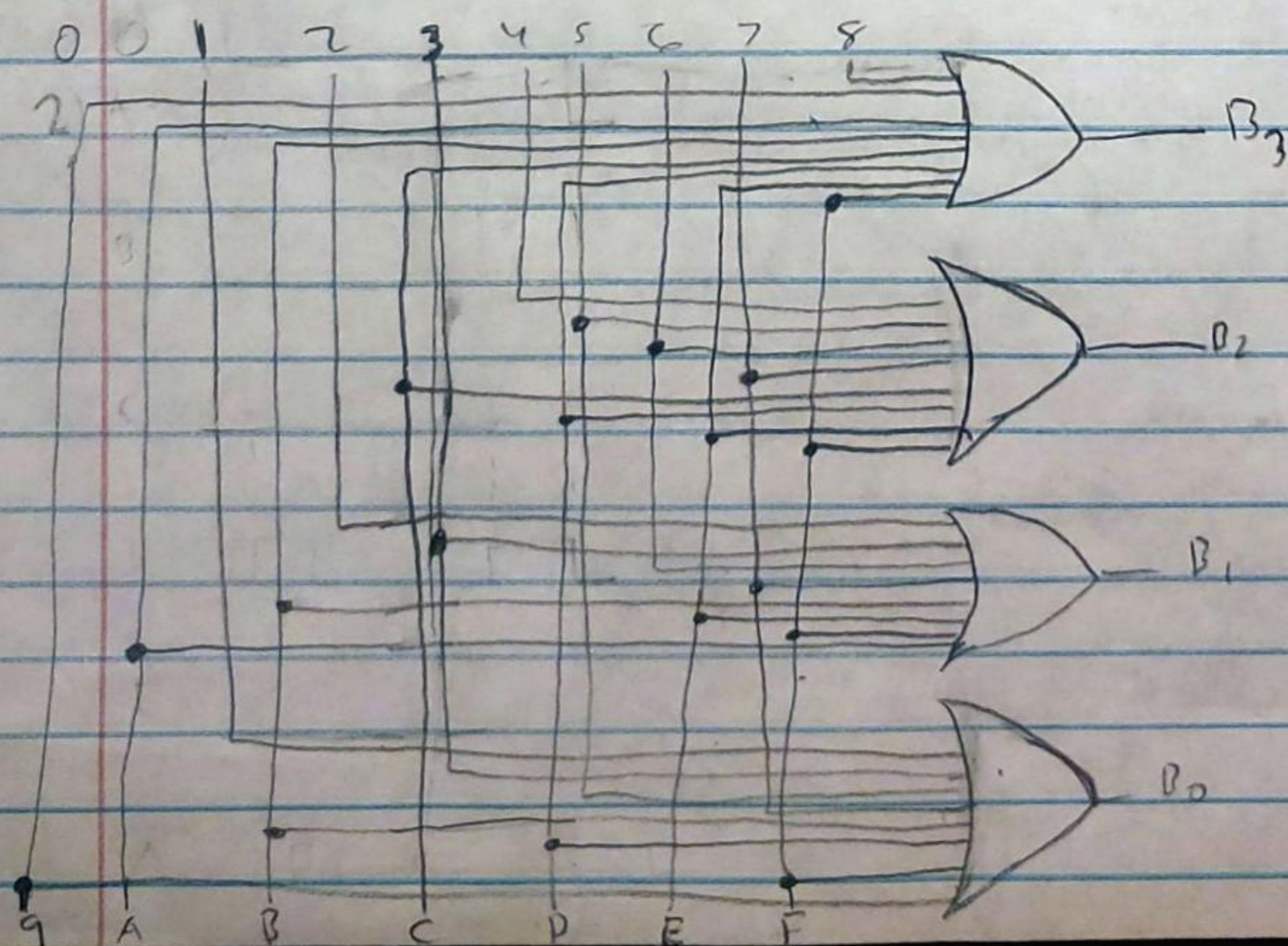
Ch. 5-



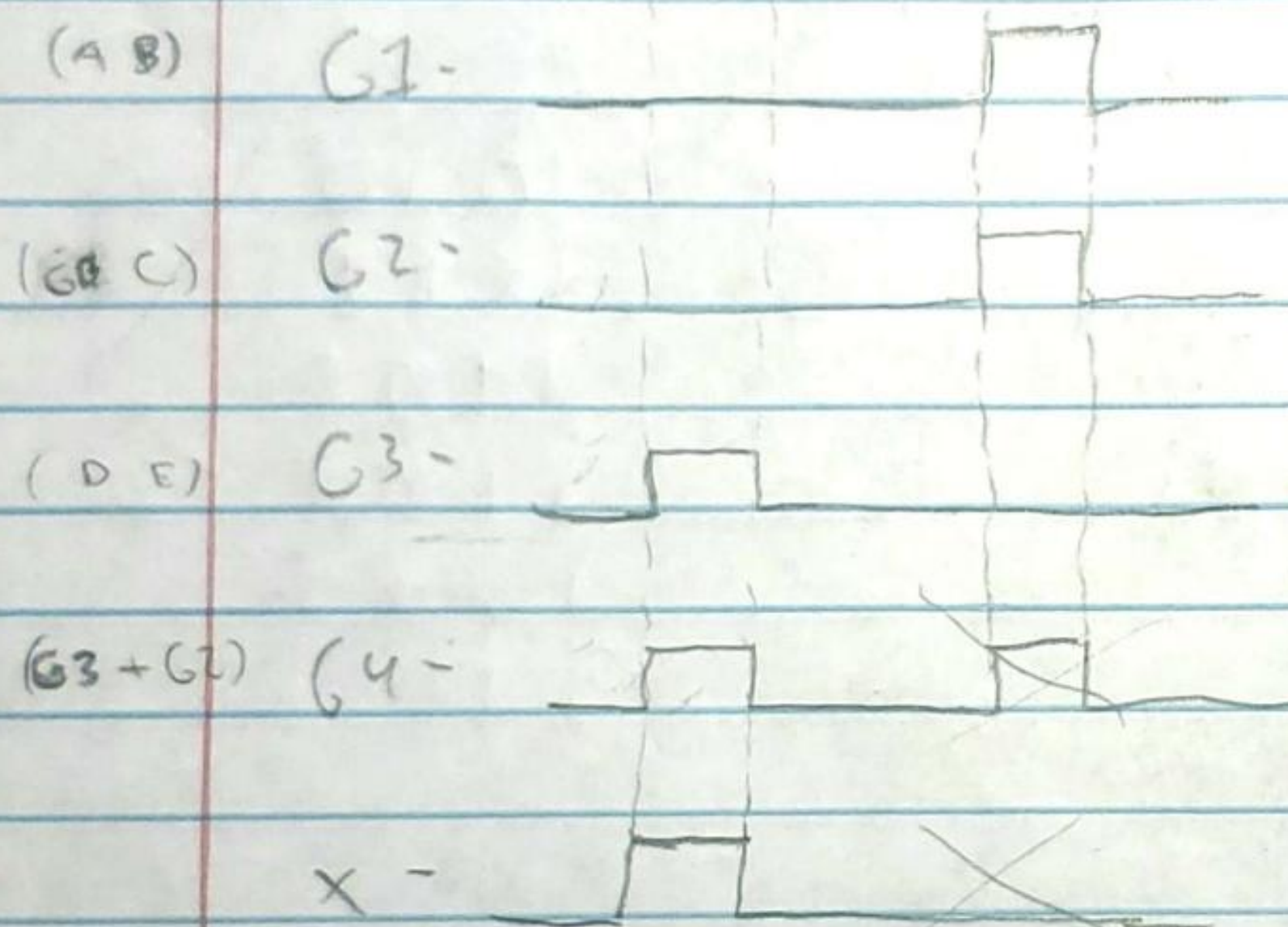
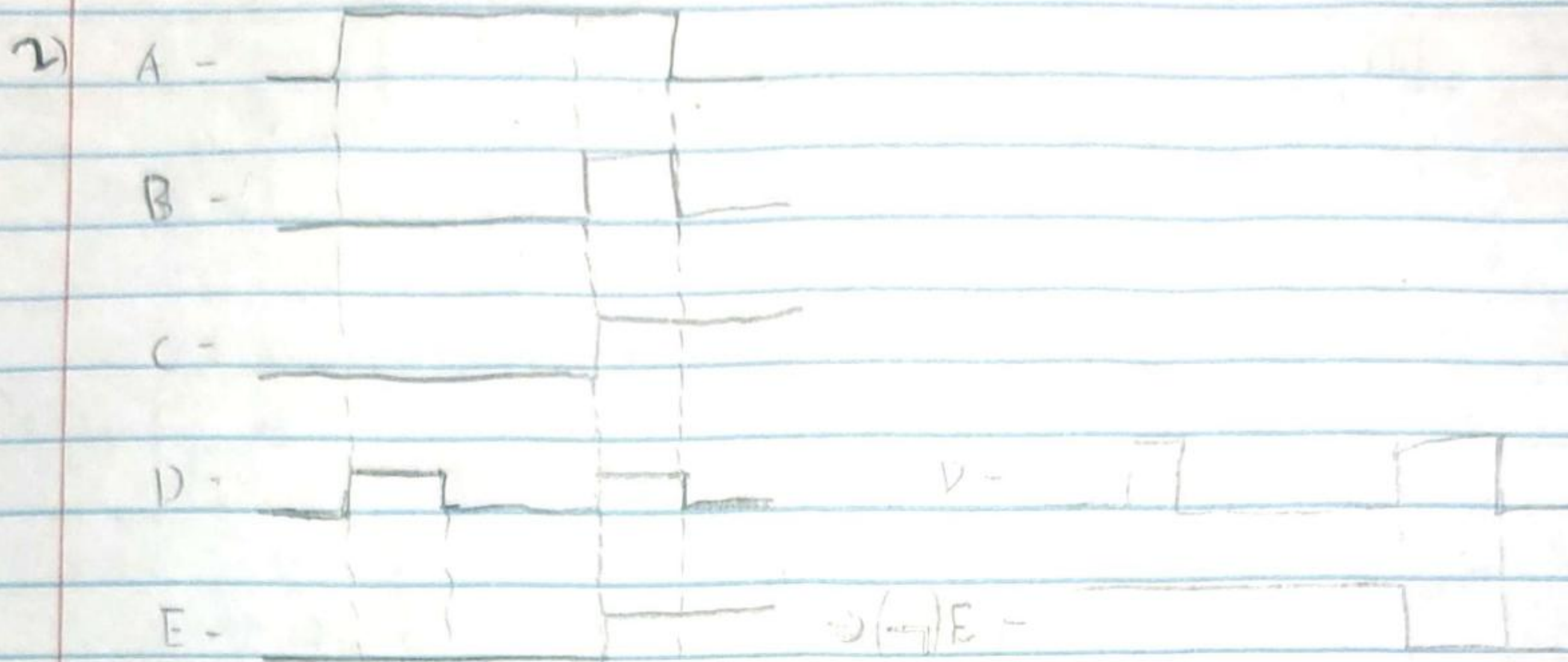
Decimal	F <sub>3</sub>	B <sub>3</sub> B <sub>2</sub> B <sub>1</sub> B <sub>0</sub>
0	1	0000
1	1	0001
2	1	0010
3	1	0011
4	1	0100
5	1	0101
6	1	0110
7	1	0111
8	1	1000
9	1	1001
(10) A	1	1010
(11) B	1	1011
(12) C	1	1100
(13) D	1	1101
(14) E	1	1110
(15) F	1	1111

base = 16

0 to F





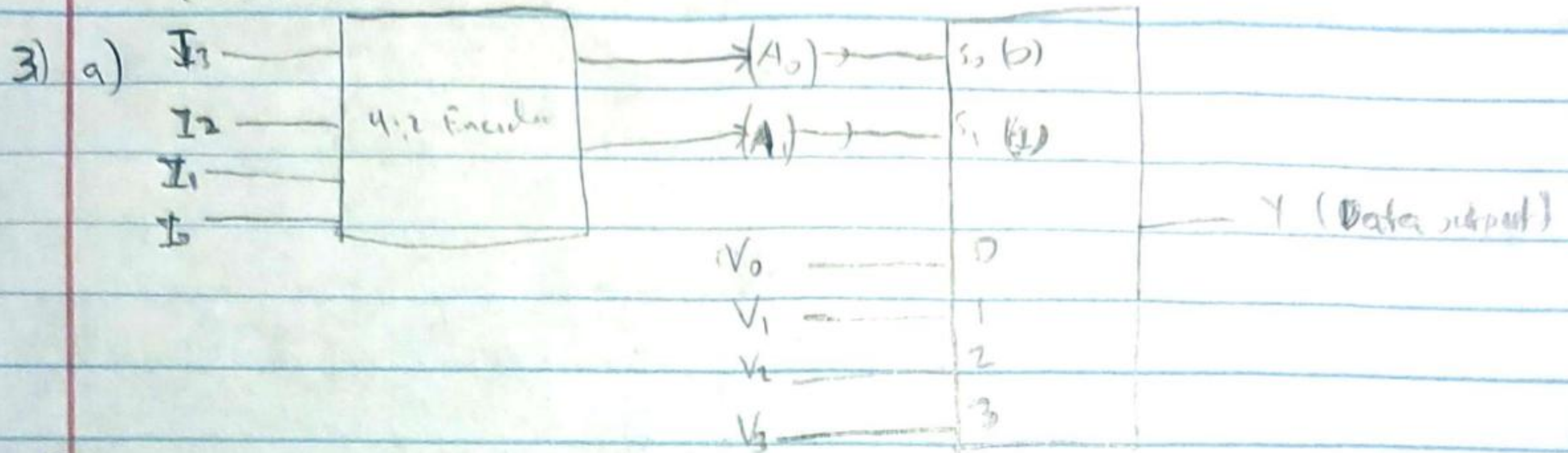


The faulty gate in this circuit is either G<sub>1</sub> or G<sub>2</sub>. Output ~~is~~ open.



## Ch. 6 (Review)

(Active-Low)

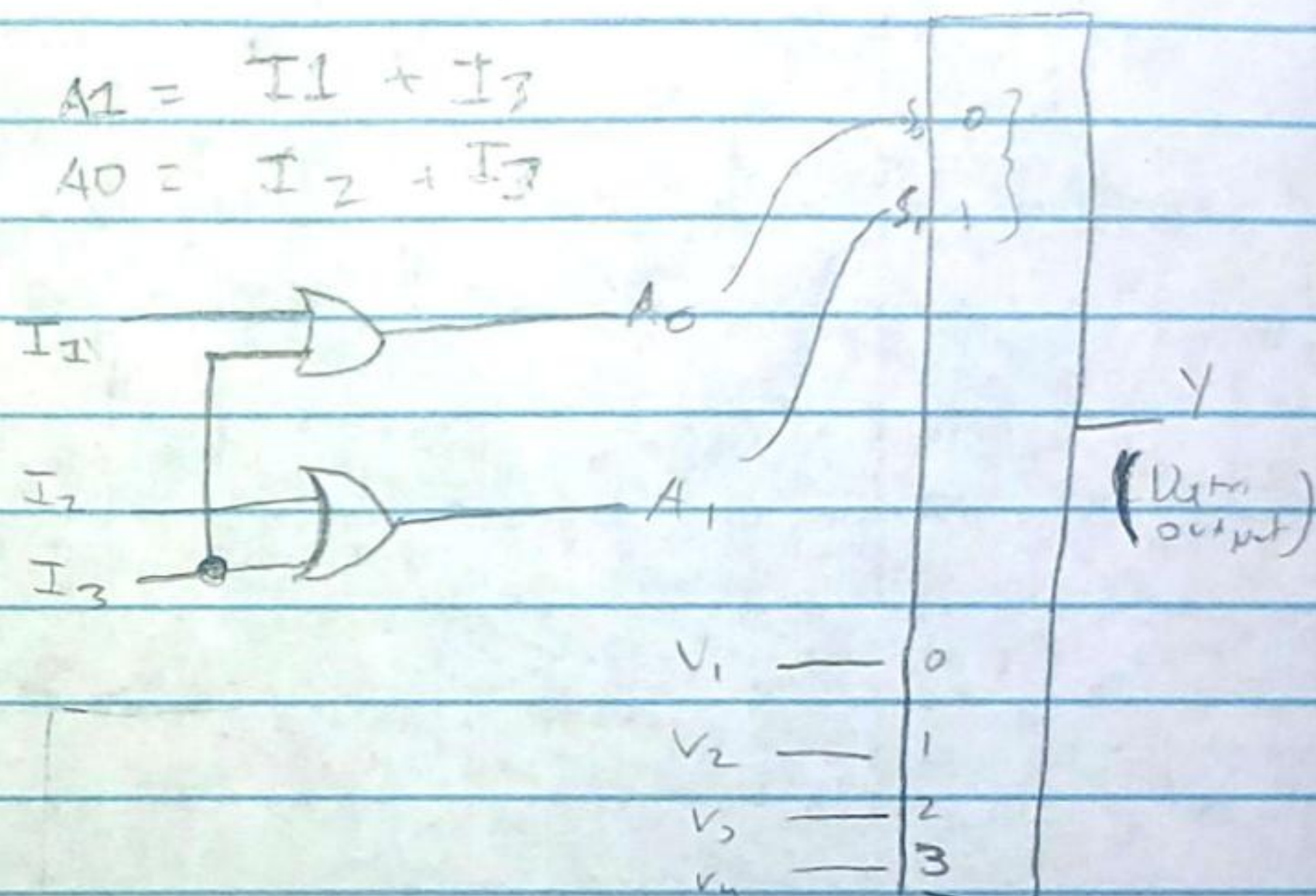


Encoder Logic

Inputs				Outputs	
$I_3$	$I_2$	$I_1$	$I_0$	$A_1$	$A_0$
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

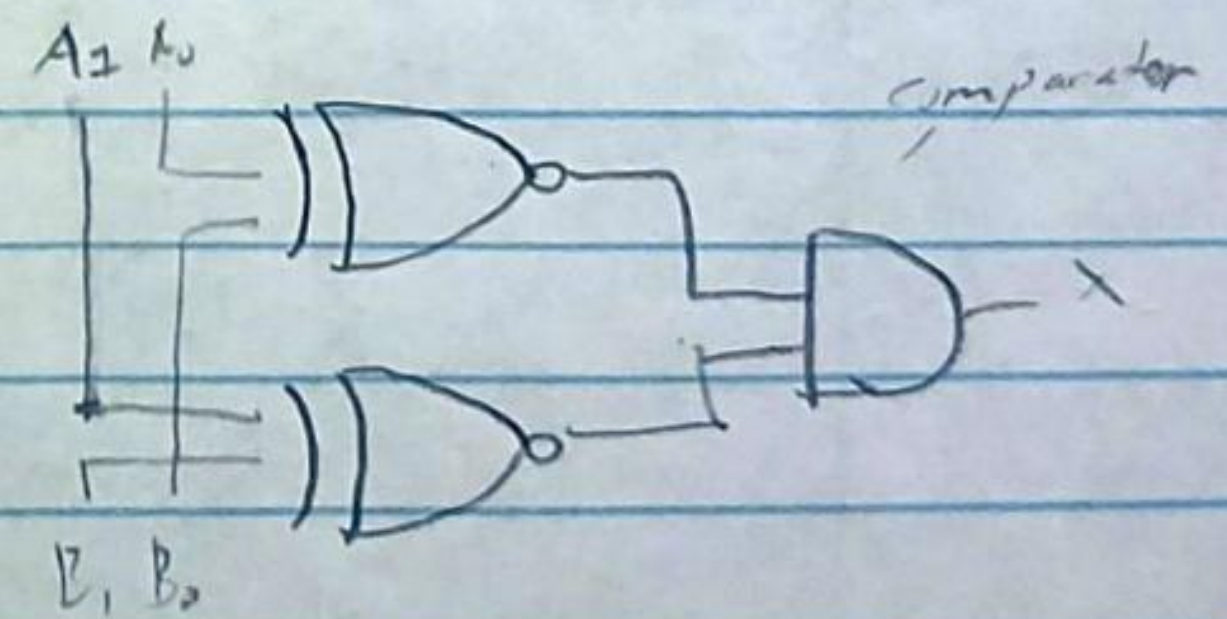
$$A_1 = I_1 + I_3$$

$$A_0 = I_2 + I_3$$



b) XNOR gate logic

A	B	X
0	0	1
1	0	0
0	1	0
1	1	1

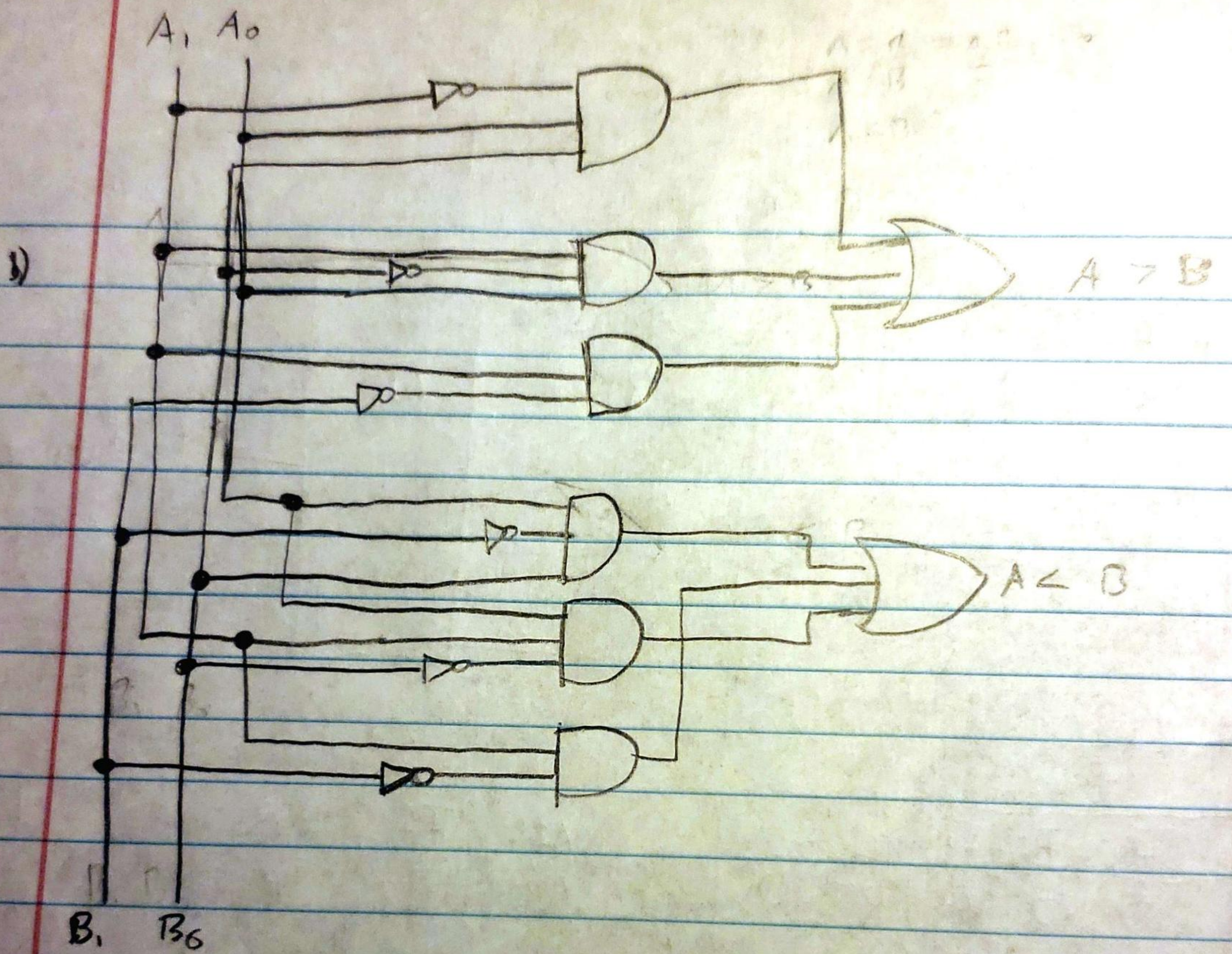


$$A < B: A_0 \overline{B}_0 B_1 + A_1 \overline{A}_0 \overline{B}_0 + A_1 B_1$$

$$A > B: \overline{A}_1 A_0 B_0 + A_1 A_0 \overline{B}_0 + A_1 \overline{B}_1$$

$$A = B: A_1 B_1 + A_0 B_0$$







Ch. 7

5) a)

CLK:

D:

Q<sub>0</sub>:

Q<sub>1</sub>:

Q<sub>2</sub>:

Q<sub>3</sub>:

Q<sub>3</sub>:

b)

Flip-flops stop working when inputs are equal to the output, because they must influence the output.

CLK:

D<sub>1</sub>:

Q<sub>0</sub>:

Q<sub>1</sub>:

Q<sub>2</sub>:

Q<sub>3</sub>:

1

0

1

0

— stored bits



