Study Guide for Midterm 2

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April 18, 2020

1 Chapter 5 - Combinatorial Logic Analysis

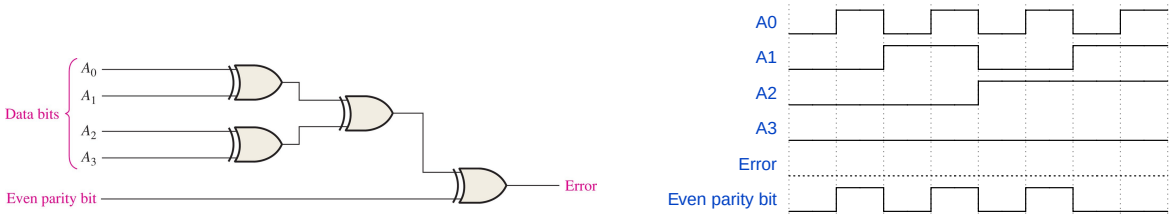


Figure 1: (Left) A circuit involving several XOR gates. (Right) An example timing diagram for the circuit at left.

1. Consider Fig. 1. (a) Generate the truth table for the output of the first three XOR gates, for all possible values of the 4-bit binar y input. What does this output represent numerically about the input $\vec{A}$? (b) Fill in the Error bit stream in Fig. 1.

2. In Fig. 2, (a) simplify the circuit via the Karnaugh map. (b) For the resulting domain-2 logic function, connect $A0$ and $A1$ from Fig. 1 (right) as inputs and produce the timing diagram assuming the same even parity bit stream.

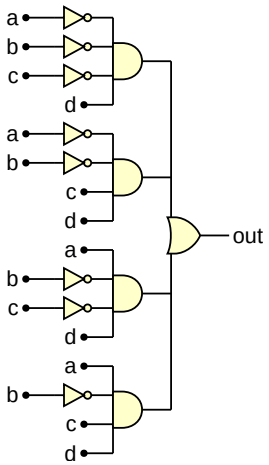


Figure 2: A domain-4 logic function.

2 Chapter 6 - Functions of Combinational Logic

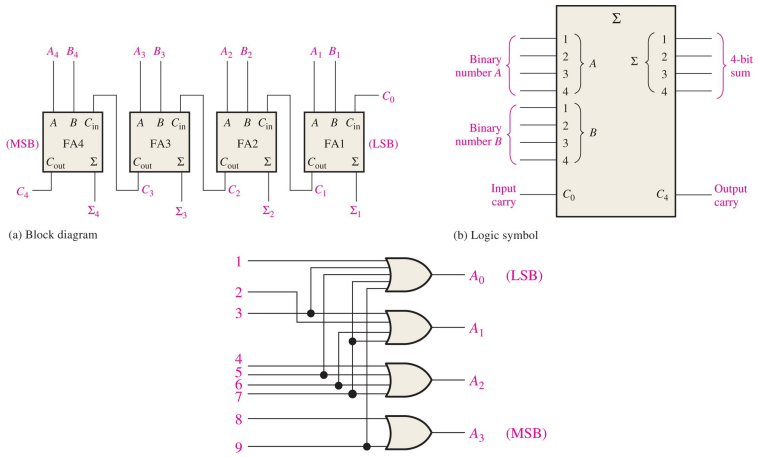


Figure 3: A 4-bit ripple carry adder (with logic symbol), and a 9-digit (zero ommitted) encoder.

1. Consider Fig. 3. (a) Design a circuit below that adds two numbers in binary corresponding to outputs from two separate encoders. (b) Demonstrate how your design would add 1 and 9. (c) Add a separate input line with XNOR gates that switches the system to subtraction in 2's complement form.

2. Using the basic logic in Fig. 4, plus inverters, (a) create a circuit that compares the *magnitude* of two 2-bit binary numbers. Assume that one or both of the numbers is a negative one, and that if a number is negative it is in *1's complement form.*

3. For the first four binary numbers (0, 1, 2, 3) show that the logic in Fig. 4 (right) converts binary to gray code.

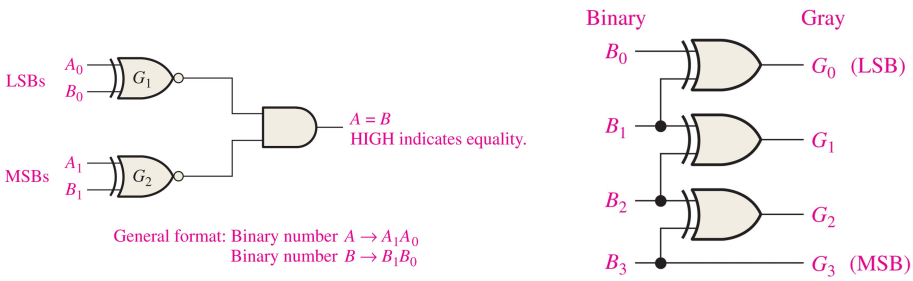
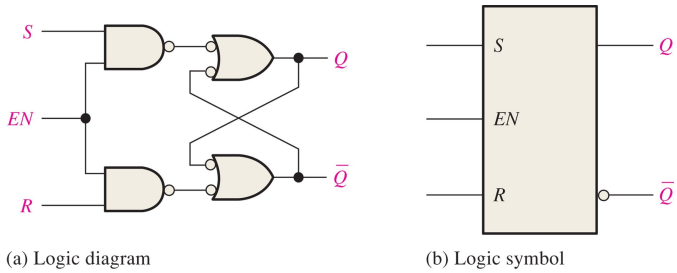


Figure 4: (Left) This is how a 2-bit comparator works. (Right) A binary to gray code converter.

3 Chapter 7 - Latches, Flip-flops, and Timers



(a) Logic diagram (b) Logic symbol

TABLE 7–3

Truth table for a positive edge-triggered J-K flip-flop.

Inputs			Outputs		
J	***K***	**CLK**	***Q***	$\overline{Q}$	**Comments**
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

↑ = clock transition LOW to HIGH
Q_0 = output level prior to clock transition

Figure 5: (Top) The gate-enabled SR latch. (Bottom) The truth table for the JK flip-flop.

1. Using the logic for the gate-enabled SR latch in Fig. 5 (top), develop a system that (a) activates a green LED when the circuit is enabled and in SET mode, (b) a yellow LED switch when the circuit is enabled and in RESET mode, and (c) a red LED when the circuit is not enabled.

2. The truth table for a positive clock-edge JK flip-flop is shown in Fig. 5 (bottom). Use such a device to design a circuit below that (a) powers two LEDs, and toggles between two states: one in which one LED is activated, and another in which the opposite LED is activated. The lights should switch on positive edges of the clock. (b) Add logic that holds LED1 on, and LED2 off, regardless of the outputs of the JK flip-flop (the equivalent of *preset* and *clear* functions of JK flip-flops).