Tuesday Reading Assessment: Chapter 3-1 through 3-3

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1 Basic Logic Gates

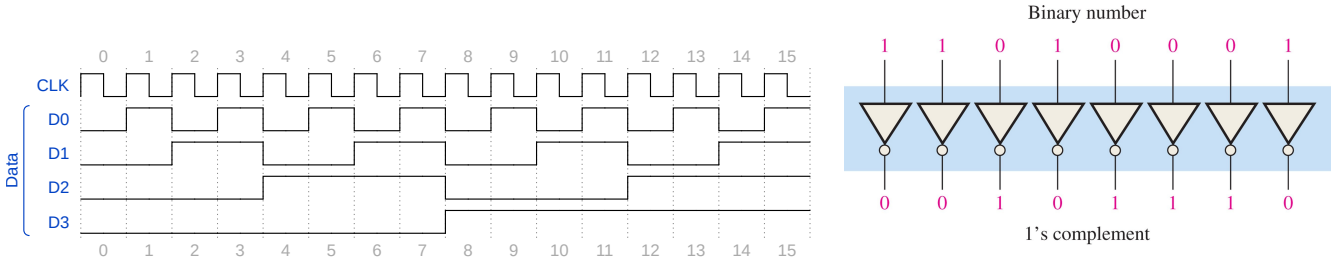

Figure 1: (Left) A timing diagram for a 4-bit parallel binary number. (Right) A simple logic circuit that computes the ones complement of a byte in parallel.

1. Consider Fig. 1, in which a 4-bit parallel data stream is shown (right), and a basic logic circuit is shown (left).
   - Describe in words what function or process is happening with the data bits D0-D3 in Fig. 1 (left).
   - Suppose D0-D4 were fed into the left-most gates in Fig. 1. Draw the timing diagram below.

2. Draw the output timing diagram for the 4-input AND gate below. *Hint: what should the truth table be for the 4-input AND?*

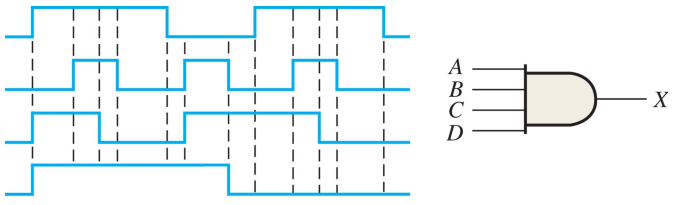

Figure 2: A timing diagram as input to a 4-input AND gate.