

Homework 6 Solutions for Computer Logic and Circuit Design: PHYS306/COSC330

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1 8-2: Types of Shift Register Data IO

- Exercise 6: see Figure 1.

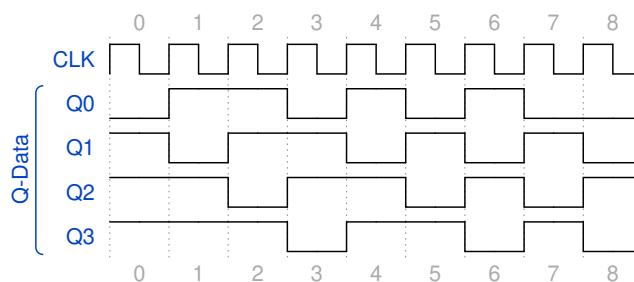


Figure 1: Solution to exercise 6.

- Exercise 8: see Figure 2.

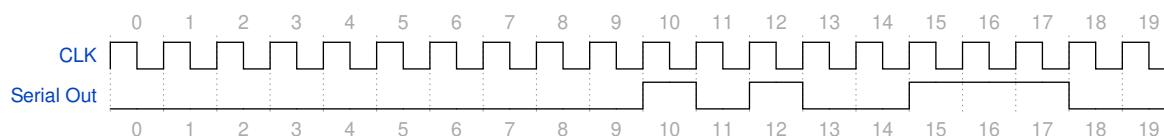


Figure 2: Solution to exercise 8.

- Exercise 10: 11011010, which is 218.
- Exercise 14: see Figure 3.

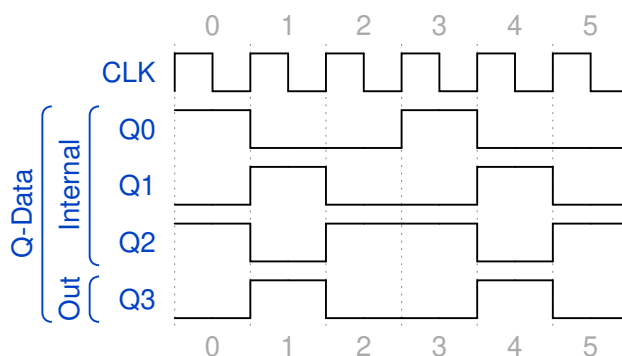


Figure 3: Solution to exercise 14.

2 8-3: Bidirectional Shift Registers

- Exercise 21: see Figure 4.

Initially (76)	01001100	
CLK 1	10011000	Shift left
CLK 2	01001100	Shift right
CLK 3	00100110	Shift right
CLK 4	00010011	Shift right
CLK 5	00100110	Shift left
CLK 6	01001100	Shift left
CLK 7	00100110	Shift right
CLK 8	01001100	Shift left
CLK 9	00100110	Shift right
CLK 10	01001100	Shift left
CLK 11	10011000	Shift left

Figure 4: Solution to exercise 21.

A 15-bit ring counter with stages **3**, **7**, and **12** SET and the remaining stages RESET.
See Figure 8-20.

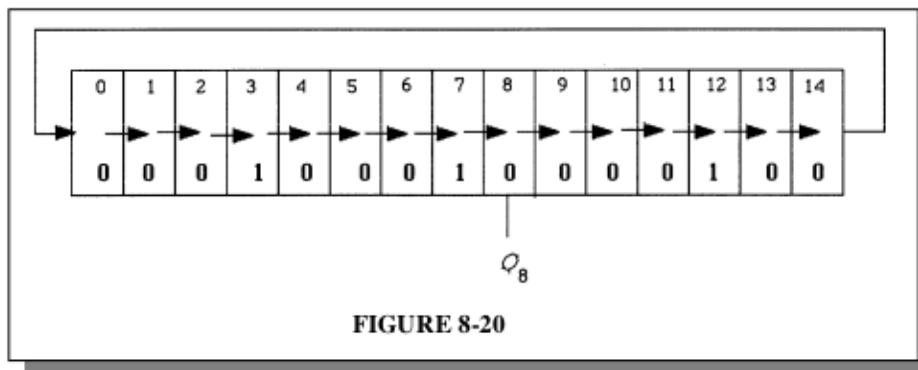


Figure 5: Solution to exercise 28.

3 8-4: Shift Register Counters

1. Exercise 28: see Figure 5.