1. Suppose an investment firm holds stock shares in four different stocks within a portfolio, labled A through D. The companies corresponding to stocks A through D are labeled *inactive* or *active* by the firm, based on information about their productivity. The firm notices that the portfolio output is *on* (rising) under the following conditions:

   - All four companies are inactive, or ... $\bar{A}\bar{B}\bar{C}\bar{D}$
   - Companies A through C are inactive, while company D is active, or ... $\bar{A}\bar{B}\bar{C}D$
   - All companies are active, or ... $ABCD$
   - Companies A through C are active, while company D is inactive. $ABC\bar{D}$

   (a) Develop a S-SOP expression for X, the portfolio's state (on or off) based on the data above. (b) Use a domain-4 Karnaugh map to simplify the S-SOP expression. (c) Which stock appears to be irrelevant to the state of the portfolio?

   a) $\bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + ABCD + ABC\bar{D}$

   b)

	CD	$\bar{C}\bar{D}$	$C\bar{D}$	$\bar{C}D$
AB	1	0	1	0
$\bar{A}\bar{B}$	0	1	0	1
$A\bar{B}$	0	0	0	0
$\bar{A}B$	0	0	0	0

   c) D

2. A circuit contains three main branches leading to one output. The output is observed to fail under the following conditions below. (a) Use the domain-3 Karnaugh map to determine the conditions under which it does succeed and write an S-SOP expression for the circuit. (b) Draw the circuit using gates.

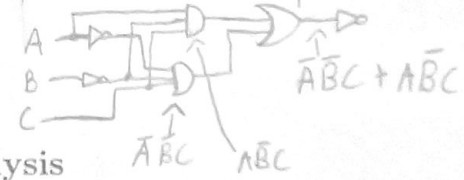
   - A: false, B: false, C: false $\bar{A}\bar{B}\bar{C}$
   - A: false, B: true, C: false $\bar{A}B\bar{C}$
   - A: true, B: true, C: false $AB\bar{C}$
   - A: true, B: false, C: false $A\bar{B}\bar{C}$
   - A: false, B: true, C: true $\bar{A}BC$
   - A: true, B: true, C: true ABC

   $\bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + AB\bar{C} + A\bar{B}\bar{C} + \bar{A}BC + ABC$

   a)

	BC	$B\bar{C}$	$\bar{B}\bar{C}$	$\bar{B}C$
A	1	1	1	0
$\bar{A}$	1	1	1	0

   b)



5 Chapter 5 - Combinatorial Logic Analysis

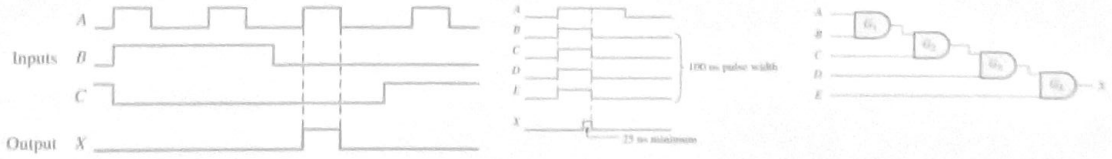
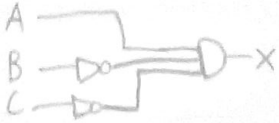


Figure 4: Diagrams for Sec. 5. (Left) Inputs are ABC, and the output is X. (Right) The inputs are ABCDE, and the output is X.

1. For the input waveforms shown in Fig. 4 (left), what logic circuit will generate the output waveform?

   $A\bar{B}\bar{C}$



2. **Bonus**: Assumming a propagation delay of 10 ns through each gate in Fig. 4, determine if the *desired* output waveform X will be generated. The desired output is a pulse with a minimum width of 25 ns.

   Yes, the total propagation delay should be 40ns. This would put the pulse width of output X at 60ns.