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Study Guide for Midterm 1

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1 Chapter 1 - Introductory Concepts

D_0 $T = 2$ $P_w = 1$

D_1 $T = 4$ $P_w = 2$

D_2 $T = 8$ $P_w = 4$

D_3 $T = 16$ $P_w = 8$

$\frac{1}{2} \times 100\% = 50\% = D_0$

$\frac{2}{4} \times 100\% = 50\% = D_1$

$\frac{4}{8} \times 100\% = 50\% = D_2$

$\frac{8}{16} \times 100\% = 50\% = D_3$

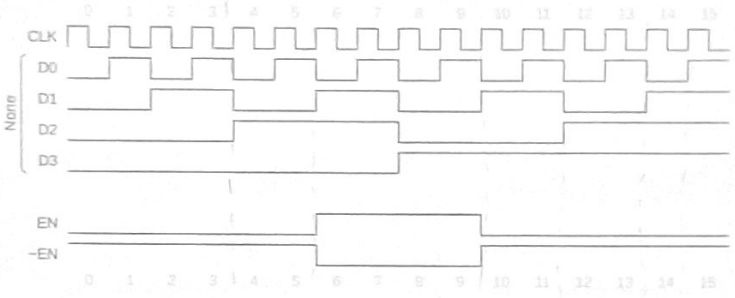


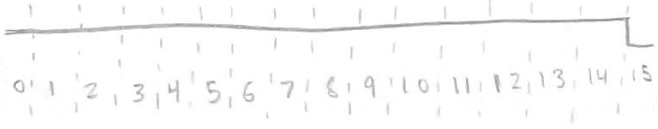
Figure 1: A timing diagram including a clock signal (CLK), a 4-bit parallel data stream (D0-D3), and enable/disable signals (EN/~EN).

1. Consider Fig. 1. (a) What is the duty cycle of each D_i signal? (b) Consider the bitstreams of D_i. What does the sequence of numbers represent?

a) $D_0 = 50\%$, $D_1 = 50\%$, $D_2 = 50\%$, $D_3 = 50\%$

b) $D_0 = 0101010101010101$ $D_1 = 0011001100110011$ $D_2 = 0000111100001111$ $D_3 = 0000000011111111$

2. (a) Imagine that D_i signals enter a NAND gate, along with the ~EN signal. Draw the resulting timing diagram.



$\overline{(D_i \sim EN)}$

3. Suppose D_i represents parallel data with a clock frequency of 4 MHz. (a) What is the total bitrate (bits per second)? (b) What would be the bit rate if the system was serial instead of parallel?

a) $f = 4\,MHz$ $T = \frac{1}{4 \times 10^6} = 2.5 \times 10^{-7} = 0.25\,\mu s \times 16\ cycles = 4\,\mu s$ $\frac{64\,bits}{4\,\mu s} = 16\,bits/\mu s$

b) $\frac{16\,bits}{4\,\mu s} = 4\,bits/\mu s = 4\,Mbs/s$ $= 16\,Mbs/s$

2 Chapter 2 - Number Systems, Operations, and Codes

1. Convert to binary: (a) 1024 (decimal) (b) 0xBBBB (hex) (c) -2048 (decimal)

a) 10000000000 b) 1011101110111011 c) 10000000000000 $=$ 1111111111110

2. Convert to hex: (a) 65535 (decimal) (b) 1000100010001000 (binary)

a) FFFF b) 8888

3. Convert to *octal*, in which **the base is 8**: 1024 (decimal).

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