Computer Logic and Digital Circuit Design: Midterm 1

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1 Chapter 1 - Introductory Concepts

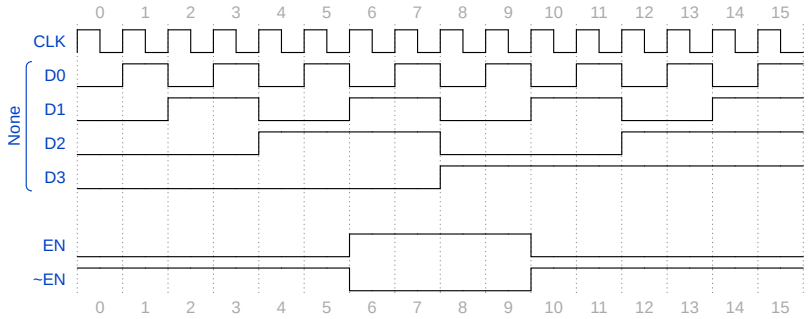
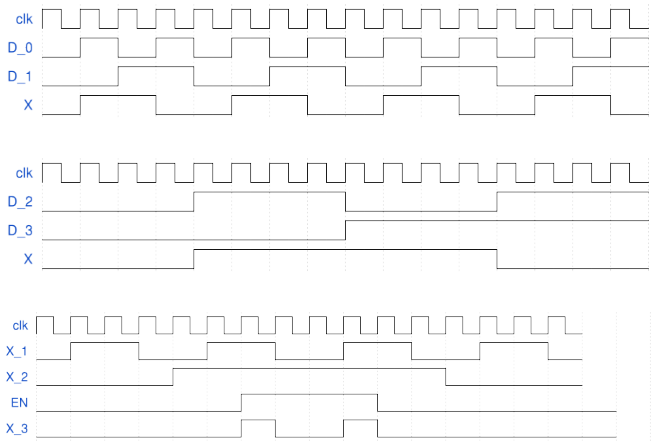


Figure 1: A timing diagram including a clock signal (CLK), a 4-bit parallel data stream (D0-D3), and enable/disable signals (EN/∼EN).

1. Consider Fig. 1. (a) What is the duty cycle of each $D_{\rm i}$ signal? (b) Consider the bitstreams of $D_{\rm i}$. What does the sequence of numbers represent?

   (a) 50%. (b) Binary counting.

2. (a) Create the timing diagram representing the output of an XOR gate with D_0 and D_1 as inputs. (b) Do the same for D_2 and D_3. (c) Finally, create the timing diagram representing the output of a 3-input AND gate with the XOR gates from parts (a) and (b), and the EN signal as inputs.



3. Suppose D_i represents parallel data with a clock frequency of 4 MHz. (a) What is the total bitrate (bits per second)? (b) What would be the bit rate if the system was serial instead of parallel?

   (a) 16 Mbps. This is because D_i represent 4 bit streams sent in parallel, so there are 4 bits per clock cycle, and the clock frequency is 4 MHz. (b) 4 Mbps. To send all the data, we need to send D_0 bits, then the D_1 bits, ... One could also argue that the effective rate is 1 Mbps, because to get all the data we have to wait four times as long because we get one bitstream at a time.

2 Chapter 2 - Number Systems, Operations, and Codes

1. Convert to binary: (a) 1024 (b) 0xBBBB (c) -2048

   (a) 100 0000 0000 (b) 1011 1011 1011 1011 (c) 1000 0000 0000 (2's complement form. When added to 2048 in binary, this result produces zero in a 12 bit system.

2. Convert to hex: (a) 65535 (b) 1000100010001000

   (a) 0xFFFF (b) 0x8888

3. **Design problem.** Consider the angular shaft encoder in Fig. 2. The IR emitter/detector detects IR light reflected from white sectors, while the dark sectors absorb the light. The sectors are encoded in binary. For example, starting from inner sectors and reading outward, dark-dark-light is translated to state 001 by the detector. If the shaft rotates 45 degrees, the detector records a state change. (a) If the initial state is 000 and the shaft rotates 360 degrees, how many bit changes occur? (b) How many bit changes would occur if the shaft position was encoded in gray code? (c) Draw the correct face of the shaft encoder, encoded in 3-bit gray code instead of binary[1] (c) If 45 degrees is the angular precision with 3-bit gray code, what is the angular precision with 8 bit gray code?

   (a) There are 8 state changes for every 360 degree rotation. Counting bit transitions for 0-7 in binary, we find a total of 11 bit changes. There are an additional three when rotating from 111 back to 000, making the total 14. (b) For gray code, the same accounting gives 8 bit changes. (b) See Fig. 2. (c) $360°/2^8 = 1.4$ *degrees.*

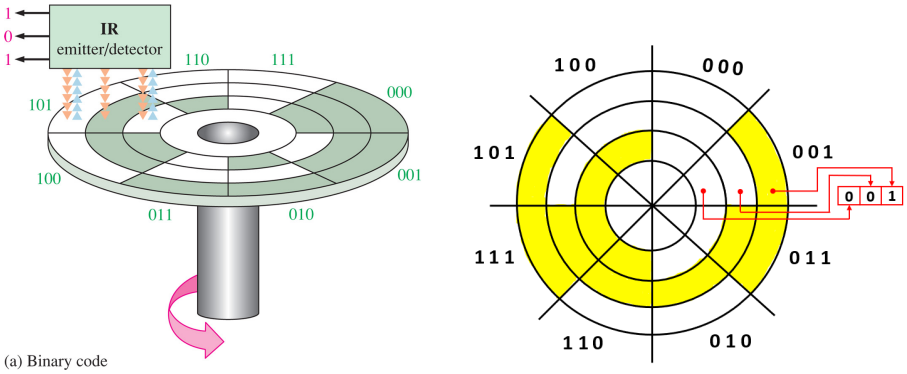


Figure 2: (Left) Binary version. (Right) Gray code version.

3 Chapter 3 - Logic Gates

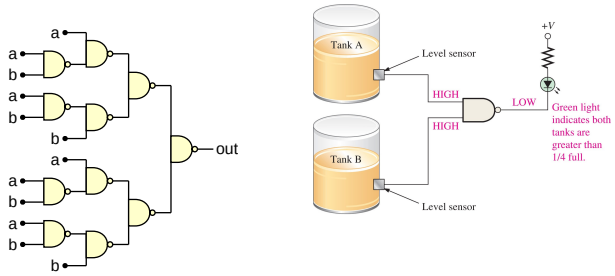
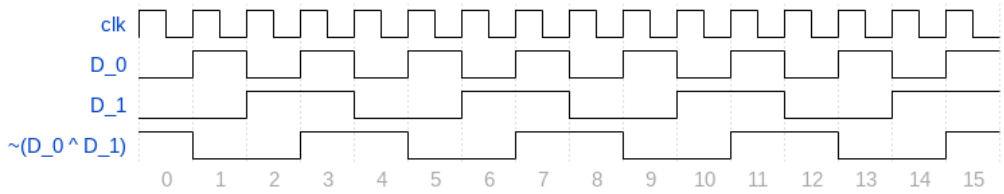


Figure 3: (Left) A logic gate combination. (Right) A liquid tank-level system built from a NAND gate.

1. Generate the simplified logic expression and truth table for Fig. 3, left. What do you call this type of gate?

   (a) $out = ab + \bar{a}\bar{b}$*, an XNOR gate. The truth table is 1 for the states 00 and 11, and 0 for 10 and 01.*

[1] Caution: I believe the figure in the textbook contains errors.



Exercise 3.2

2. Suppose signals D_0 and D_1 in Fig. 1 are connected to a and b in Fig. 3, left. Generate the timing diagram.

3. **Design problem.** A liquid tank system is depicted in Fig. 3 (right). The sensors are HIGH when the liquid is above the level. (a) Create and display a red LED system that activates when both tanks are *below* the level. (b) Create and display a yellow LED system that activates when one tank is below and one tank is above the level. (c) Add a third tank with two pipes guiding liquid to tanks A and B. Each pipe should have a valve. Add logic that opens the correct valve so as to fill only the low tank until it is no longer below the level.

   (a) Connect wires from sensors 1 and 2 to an OR gate. Connect the output of the OR gate to the low side of an LED in series with a blocking resistor. The high side of the LED should be connected to 5 Volts (V_{CC}). (b) Connect wires from sensors 1 and 2 to an XNOR gate. Connect the output of the XNOR gate to the low side of an LED in series with a blocking resistor. The high side of the LED should be connected to 5 Volts (V_{CC}). (c) Suppose the valves open when the receive a high signal. Connect wires from sensors 1 and 2 to inverters, then connect the inverters to the valve inputs. Valves will remain open until the tank sensors go high.

4 Chapter 4 - Boolean Algebra and Logic Simplification

1. Suppose an investment firm manages a portfolio with shares in four stocks, labled A through D. The companies corresponding to stocks A through D are labeled *inactive* or *active* by the firm, based on productivity information. The firm notices that returns (profits) for the portfolio increase under the following conditions:

   - All four companies are active, or ...
   - Companies A and B are inactive, while companies C and D are active, or ...
   - Company A is inactive, while companies B, C, and D are active, or ...
   - Company B is inactive, while companies A, C, and D are active.

   (a) Develop a S-SOP expression for X, the portfolio's state. If profit is increasing, label the output ON, and label it OFF if profit is decreasing. (b) Use a domain-4 Karnaugh map to simplify the S-SOP expression. (c) Based on your analysis, which stock or stocks should be eliminated from the portfolio?

   (a) $X = ABCD + \bar{A}\bar{B}CD + \bar{A}BCD + A\bar{B}CD$. (b) We find a column of states that form a group of 4. The expression simplifies to $X = CD$. (c) Eliminate stocks A and B.

2. A circuit contains three main branches leading to one output. The output is observed to **fail** under the following conditions below. (a) Use the domain-3 Karnaugh map to determine the conditions under which it does succeed, and write an S-SOP expression for the circuit. (b) Draw the circuit using gates.

   - A: false, B: false, C: false
   - A: false, B: true, C: false
   - A: true, B: true, C: false
   - A: true, B: false, C: false
   - A: false, B: true, C: true
   - A: true, B: true, C: true

   (a) $X = \bar{B}C$. (b)

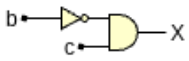


Figure 4: Exercisec 4.2

5 Chapter 5 - Combinatorial Logic Analysis

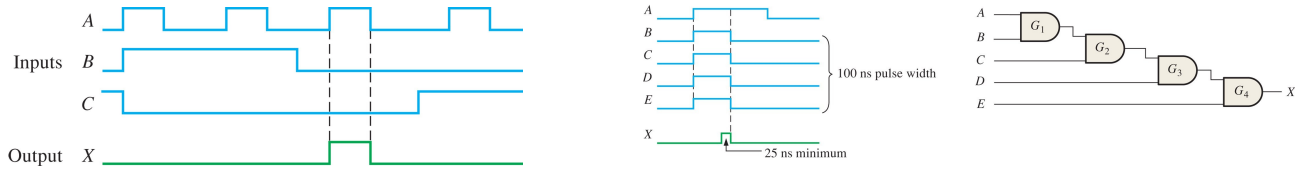


Figure 5: Diagrams for Sec. 5. (Left) Inputs are ABC, and the output is X. (Right) The inputs are ABCDE, and the output is X.

1. For the input waveforms shown in Fig. 5 (left), what logic circuit will generate the output waveform?

   Read the input states across the timing diagram. The truth table is nearly completed, with only the $ABC = 011$ *and* $ABC = 111$ *states left unprobed. The question asks for the logic circuit that will generate the given waveform, and the only true state is* $X = A\bar{B}\bar{C}$*. Treating the unprobed states as "don't cares" does not help with the Karnaugh map. The circuit is an AND gate with an inverter on the B and C inputs:*

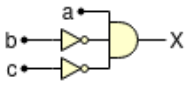


Figure 6: Exercise 5.1

2. **Bonus**: Assumming a propagation delay of 10 ns through each gate in Fig. 5, determine if the *desired* output waveform X will be generated. The desired output is a pulse with a minimum width of 25 ns.

   Accounting for delays and overlaps in timing, we find a final pulse width of 70 ns:

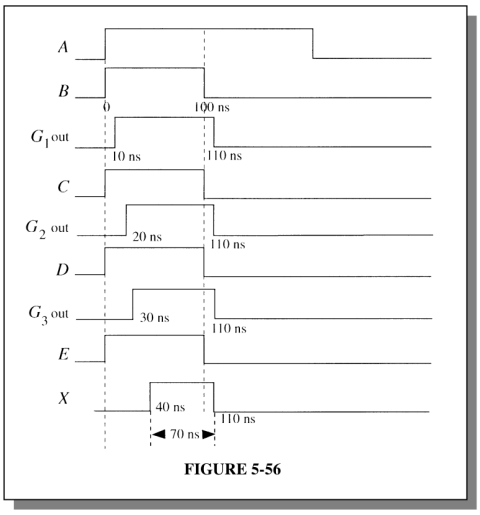


Figure 7: Bonus exercise.