Synopsis - Week 7 Integrated Project: Probing Fixed IC Gates with Oscilloscope, DC Power Supply, Breadboard, and Digital Voltmeter

Prof. Jordan C. Hanson

October 19, 2023

1 Reading the Specification Sheet of IC Gates

Today we will be working with the Texas Instruments SN74HC00N component. This is a 14-pin DIP package containing 4 NAND gates, each with 2 inputs and 1 output. The specification sheet is posted to the course Moodle page, under Week 7. Note the specification includes the functional block diagram (Fig. 1, left). Note that there are 4 gates, requiring 8 inputs and 4 outputs. There are two additional pins, $V_{\rm CC}$ (DC power), and GND (ground). Pairs of inputs are labelled 1A, 1B, 2A, 2B, ..., and outputs are labelled 1Y, 2Y, ...

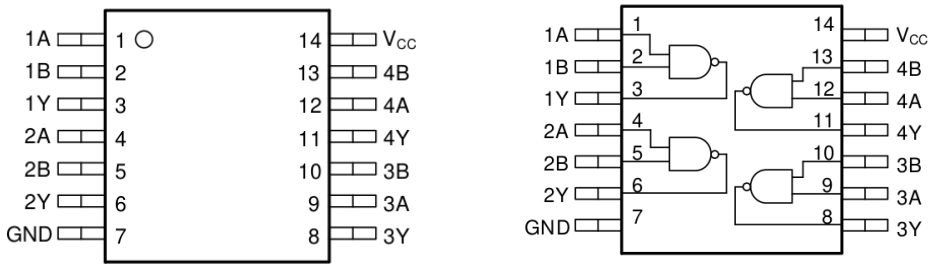

Figure 1: (Left) The pinout for the SN74HC00N 14-pin DIP. Note the locations of $V_{\rm CC}$ and GND relative to the notch at the top left. (Right) The functional block diagram of the SN74HC00N shows how the 4 NAND gates are internally connected. The gates are labelled A, B, C, and D, with Y indicating outputs.

Using the Table of Contents and tables within the specification sheet, answer the following questions.

- What is the maximum range for the supply voltage $V_{\rm CC}$?
- If the supply voltage is 3.3V to 5V, what is the minimum input HIGH voltage, $V_{\rm IH}$?
- If the supply voltage is 3.3V to 5V, what is the maximum input LOW voltage, $V_{\rm IL}$?
- What is the maximum propagation delay, $t_{\rm pd}$, for the commerical version of this component? What does this imply about the maximum clocking frequency for these gates?

2 Breadboard Setup, Connecting the IC Gates

Make sure that your lap table is powered, and that the DC power supply is connected. Switch on the power supply, and use the digital voltmeter to check that the voltage between the red and black (GND) terminals is 3.3 V. Use the red and black banana-plug cables to route power down to your breadboard. Use the red breadboard post for $V_{\rm CC}$, and the black post for GND. Use the DVM to check that the voltage between the posts is still 3.3V. Now turn off the DC power supply. Unscrew the red post cap until you find a hole through the post. Do the same for the black post. Slide jumper wires into these holes, and then screw the post down to hold the jumpers in place. Orient the posts away from you on the table. Note in Fig. 1 (left) the pinout of the DIP package for the IC gates contains a notch near pin 1. Straddle the counter across the center divide of the breadboard such that pin 1 is oriented away from you. The IC gates should be within range of the jumpers so that the hot jumper can bring $V_{\rm CC}$ to pin 14, and the GND jumper can bring GND to pin 7 (Fig. 2).

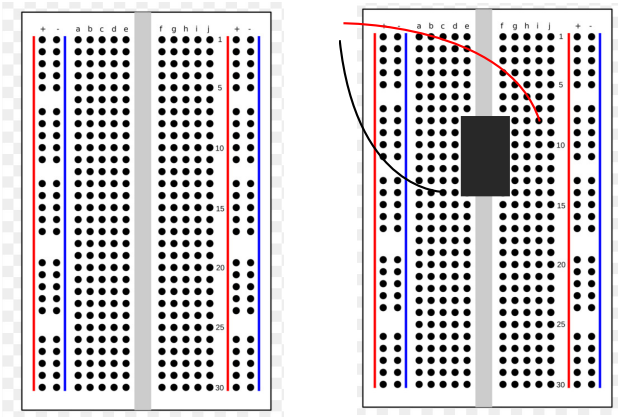

Figure 2: (Left) The basic breadboard layout. The rows of five pins are connected, but the connection does not persist across the center divide. Outer columns of five pins are also connected. (Right) Place the IC gates across the divide, and connect V_{CC} to pin 14 and GND to pin 7.

3 Generating a Clock Signal with the Oscilloscope Signal Generator

On the oscilloscope, there is a built-in signal generator. The button to activate it is named "wave gen." Press it to open the signal generator menu. If a message appears indicating the wave generator is not available, we will use a separate signal generator. Use the controls to create a square wave. For the clock frequency, use your response in Sec. 1. Connect a BNC coaxial cable from the signal output to the channel 1 scope input. Use the spec sheet to determine what CLK amplitude is appropriate. **Please ensure that the minimum voltage of CLK signal is 0V.** Adjust the scope trigger settings such that the scope displays the CLK signal on channel 1.

4 Wiring the IC Gates with CLK, Probing the Output

Our next job is to provide the CLK signal to the IC gates as an input signal. In the lab, there are special coaxial cables with BNC connectors on one side, and red/black leads on the other side. Connect the CLK signal to the BNC side, and use the leads with jumpers to deliver the CLK signal to the board. Connect the black CLK lead to GND (pin 7) with a jumper, and use two jumpers to connect the red CLK lead to pins 1 and 2 (Fig. 3, left). Finally, connect the scope probe BNC connector to scope channel 1. Connect the grounding clip of the scope probe to ground via a jumper. Then probe of the CLK signals on pin 1 or 2. Adjust the trigger controls until you are triggering on the CLK signal. Does this signal match your expected CLK settings? Next, we will probe pin 3, the output of the first NAND gate.

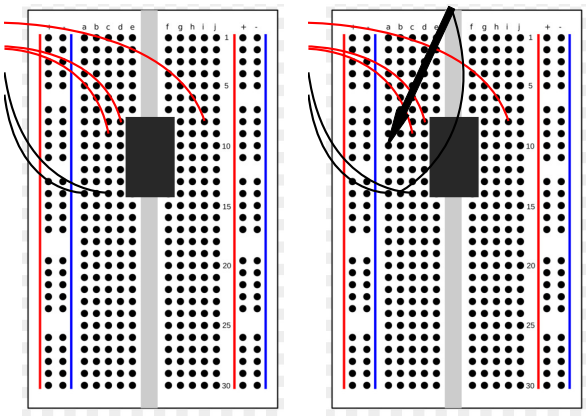

Figure 3: (Left) The CLK signal is connected to pin 10 and GND. The CLR signal is held LOW by connecting it to GND. (Right) The probe is connected to GND, and the tip passes the signal to the scope.

Input Pin	Input Pin	Output Pin
1	2	3
4	5	6
9	10	8
12	13	11

Table 1: Fill in the measured data for the truth tables of the 3 NAND gates.

5 Probing IC Gate Channels with Scope Probe

Use the probe tip to probe the pin 3 signal on the breadboard (Fig. 3, right). Adjust the trigger controls to display the signal. Now complete the following steps:

- Locate the Measurement section of the scope panel. Press the Measurement button to bring up a menu at the bottom of the screen.
- Add a measurement, and choose Frequency as the measurement. Is the measured frequency the same as the chosen CLK frequency? Does this match or not match expectations?
- What is the duty cycle of the signal? Does this match or not match expectations?
- Switch the CLK inputs to pins 4 and 5, and probe the output pin 6. Repeat the frequency and duty cycle measurements to confirm that they match expectations.

Notice that you can jump GND to input pins to hold inputs LOW, and you can jump V_{CC} to input pins to hold inputs HIGH. Using this technique and the DVM to probe output pins, determine the truth tables of the gates and record the data in Tab. 1. In the space below, draw the output timing diagram corresponding to the following scenario: pin 1 is held LOW (GND), pin 2 receives the CLK signal, and pin 3 is probed by the scope probe. Explain the features of the signal.