Andy P.
Cosc 330

Chapter 5 - Combinatorial Logic Analysis

1.

	A_3	A_2	A_1	A_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
A	1	0	1	0
B	1	0	1	1
C	1	1	0	0
D	1	1	0	1
E	1	1	1	0
F	1	1	1	1

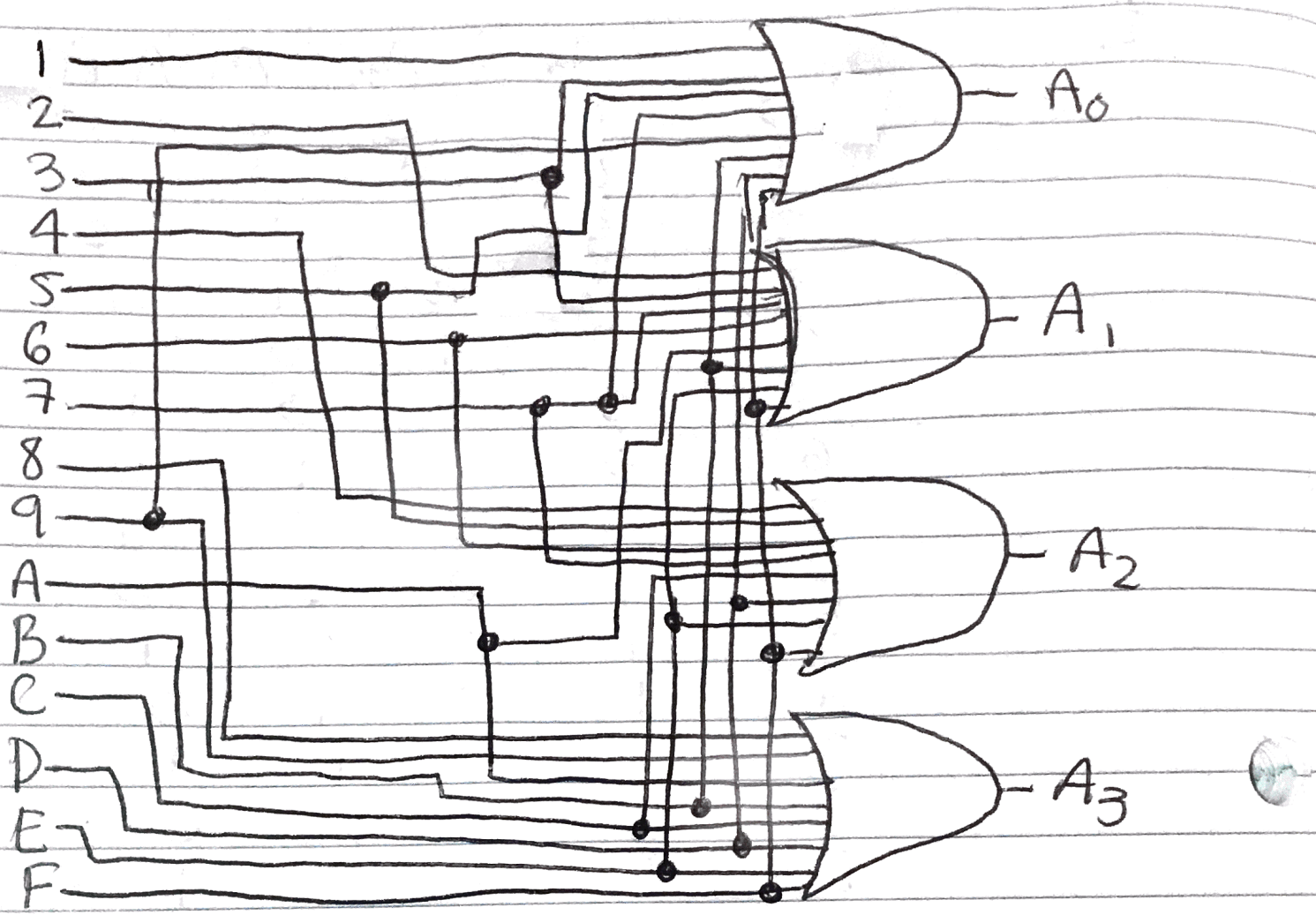
$A_3 = 8+9+A+B+C+D+E+F$

$A_2 = 4+5+6+7+C+D+E+F$

$A_1 = 2+3+6+7+A+B+E+F$

$A_0 = 1+3+5+7+9+B+D+F$

1 Continued)

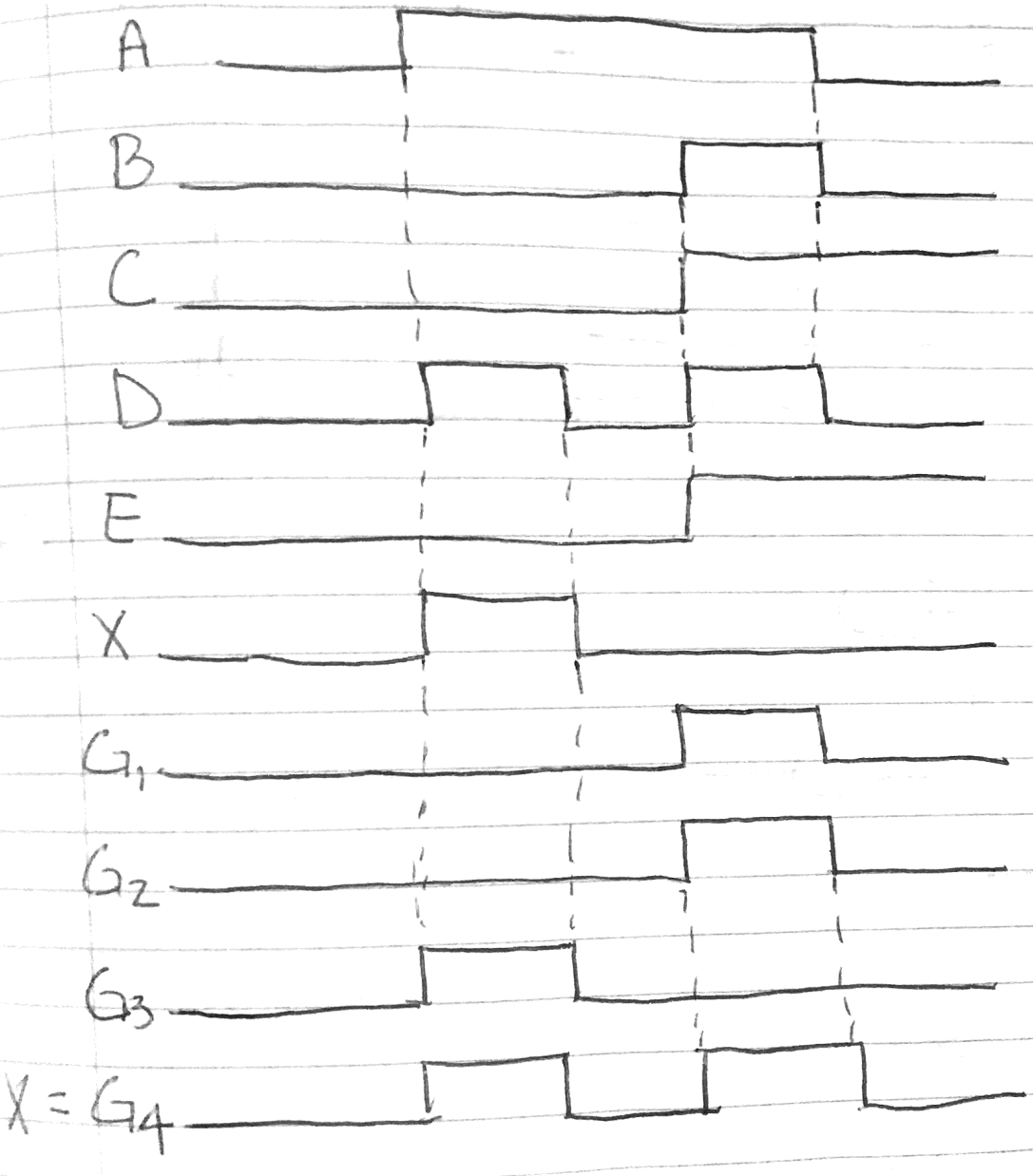


2. $G_1 = AB$

$G_2 = G_1 C$

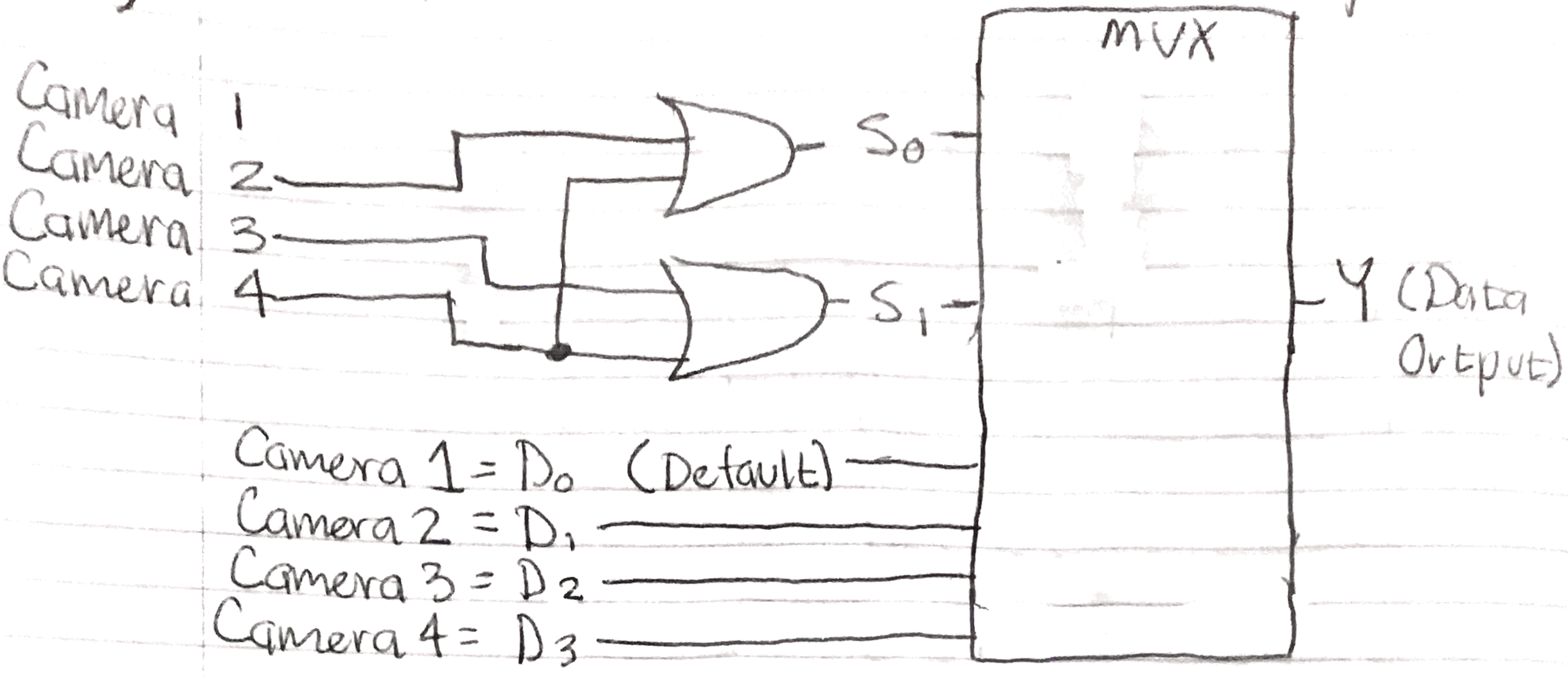
$G_3 = D\bar{E}$

$G_4 = G_2 + G_3$

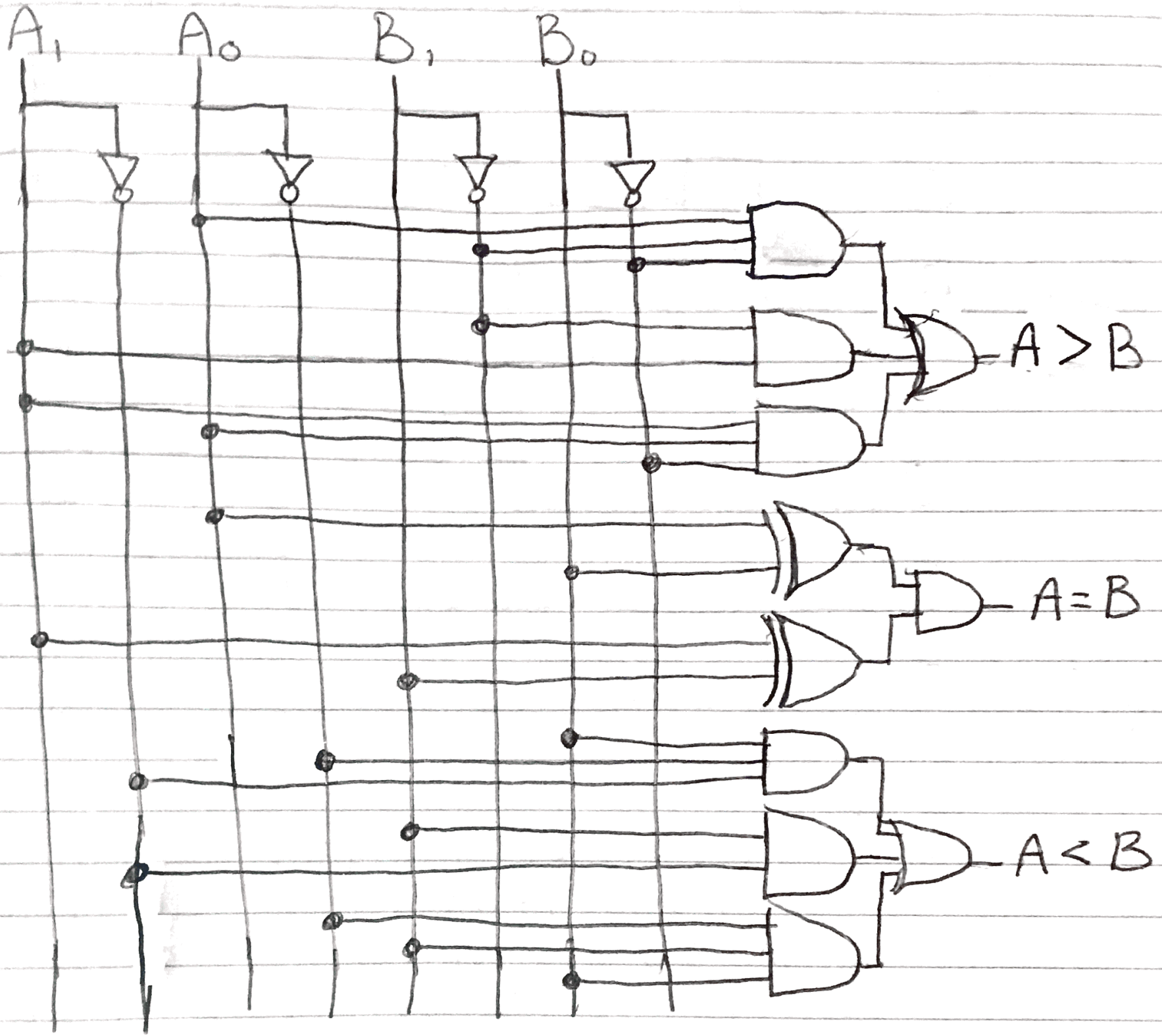


This shows that either G_1 or G_2 is faulty; one or both are stuck at a Low signal.

1) 2 Chapter 6 Fctns of Combinatorial Logic

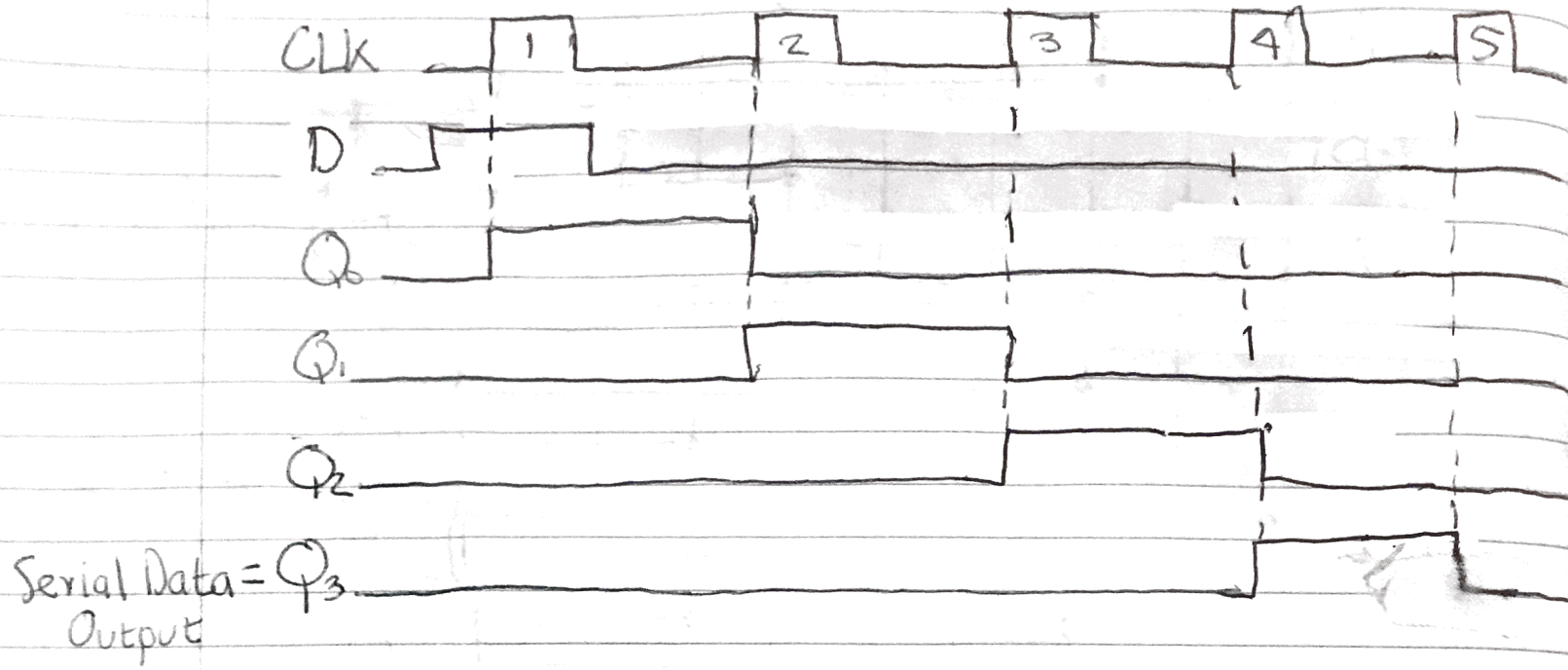


2)

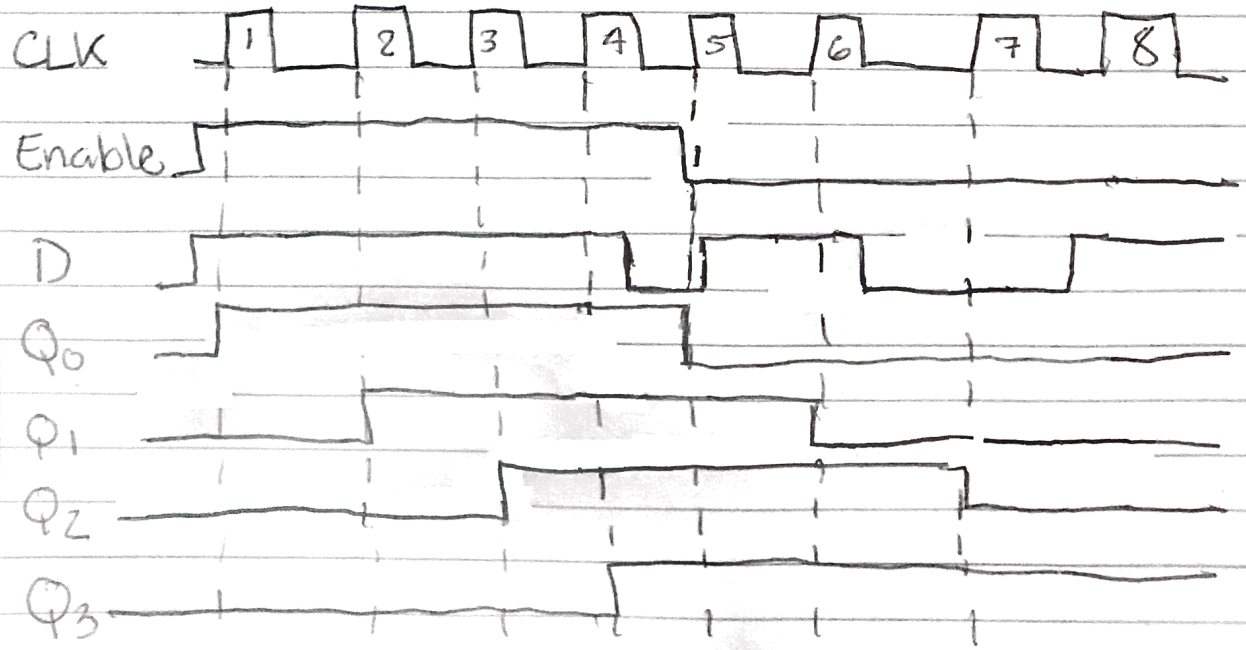


3 Chapter 7 - Latches, Flip-Flops, Timers

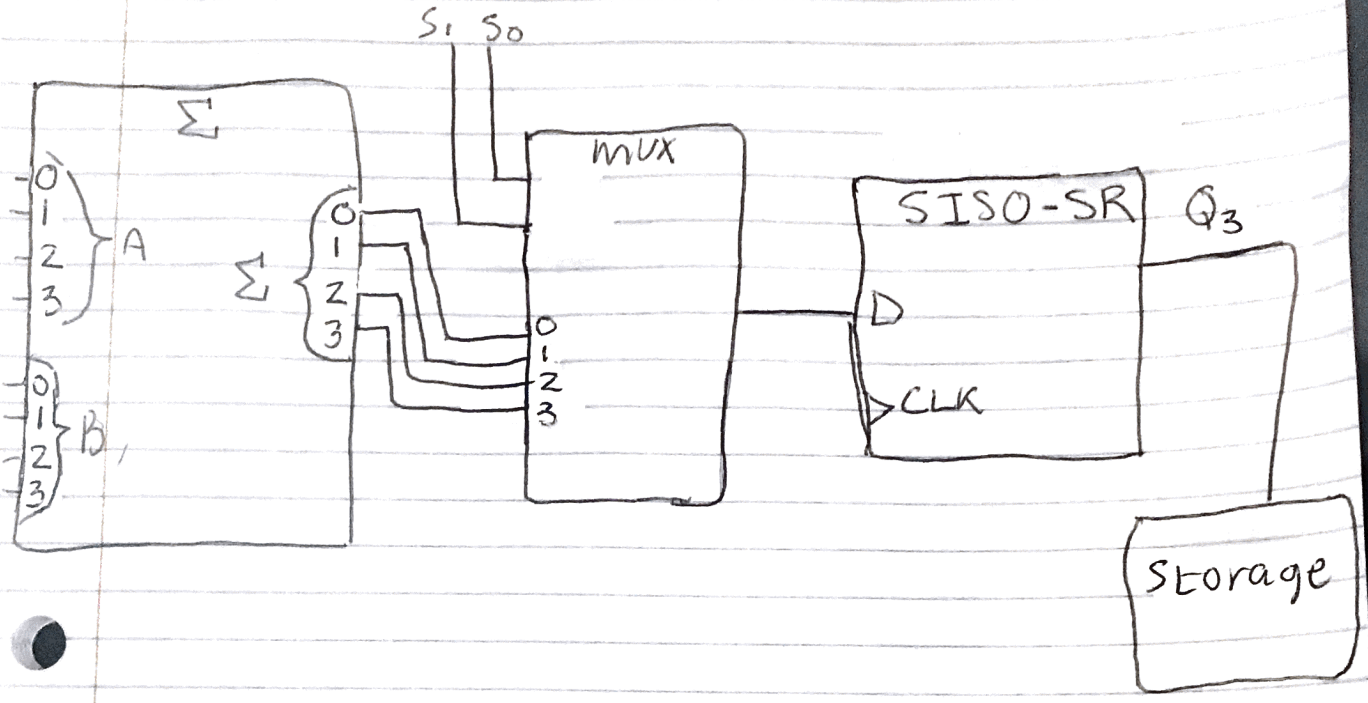
1. a)

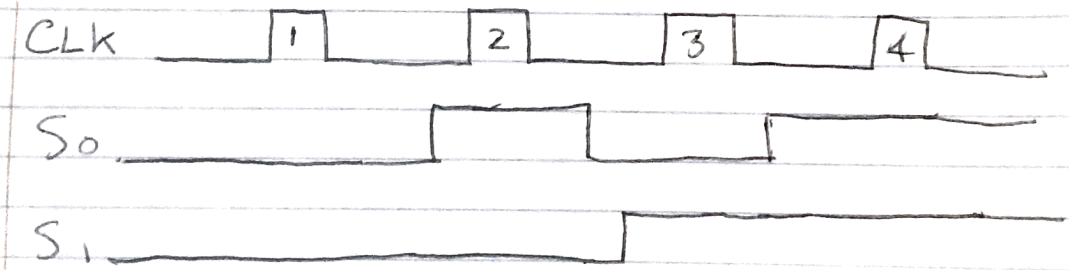


b) To Halt the Clock signal I will create an Enable input that will allow the clock signal to be read when the Enable signal is high. Binary #: 1111



2)


S1 S0
Σ
0
1
2
3
A
Σ
0
1
2
3
0
1
2
3
B
MUX
0
1
2
3
SISO-SR
Q3
D
CLK
Storage


CLK
1
2
3
4
S0
S1