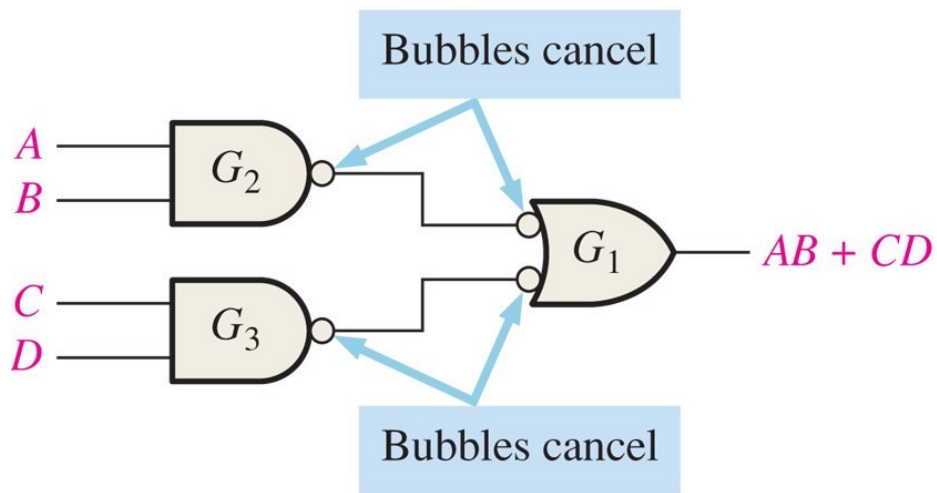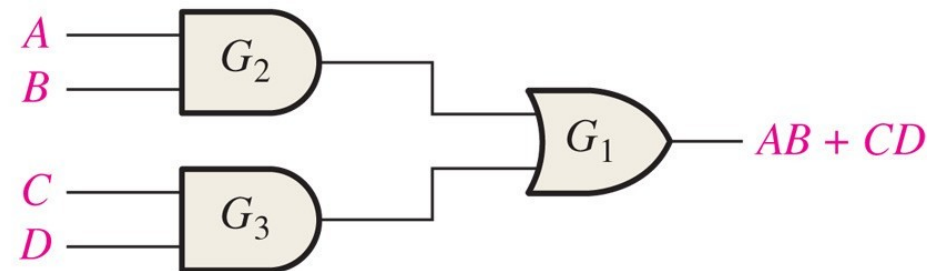(a) Original NAND logic diagram showing effective gate operation relative to the output expression

(b) Equivalent NAND/Negative-OR logic diagram

(c) AND-OR equivalent