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11/23

COSC 330 Midterm

Ch6

1.) a.) delay < clock cycle

$32ns < \tau \qquad F = \frac{1}{\tau}$

$F < \frac{1}{32ns}$

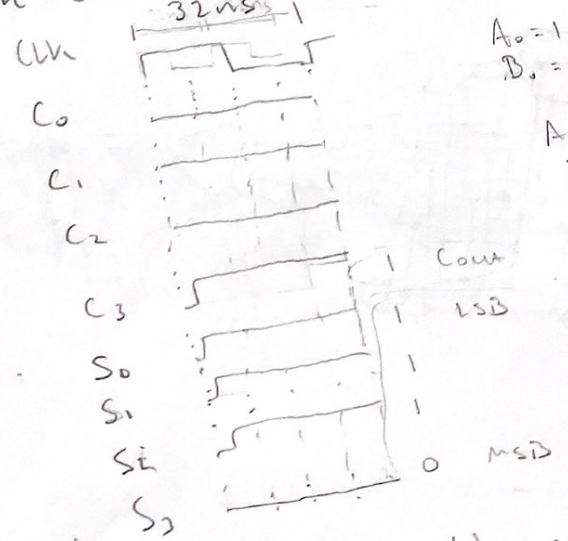
$f < \frac{1}{32 \times 10^{-9}}$ sec

$f < \frac{1}{32}$ GHz $= 0.03125$ GHz $= 31.25$ MHz

b.) $8 \times 8ns = 64ns$ delay

$F = \frac{1}{64}$ GHz $= 0.015625$ GHz $= 15.625$ MHz

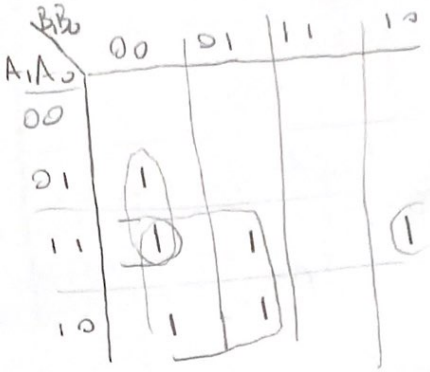
c.) The problem states that the total delay must be less than one clock period, so the entire addition happens in one clock cycle.



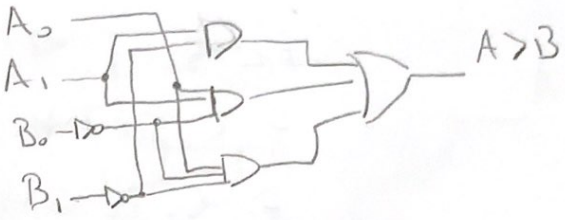
$A_0 = 1$ $A_1 = 1$
$B_0 = 0$ $B_0 = 0$
$A_2 = 1$ $A_3 = 1$
$B_2 = 0$ $B_3 = 1$

Sums will go high rather quickly as A,B inputs are constant, and the carries in this case do not change any of the sums. C_3 goes high almost immediately because A_3, B_3 both high in full-adder circuit.

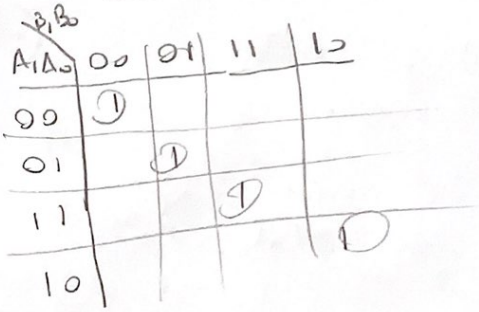
2) a) A>B



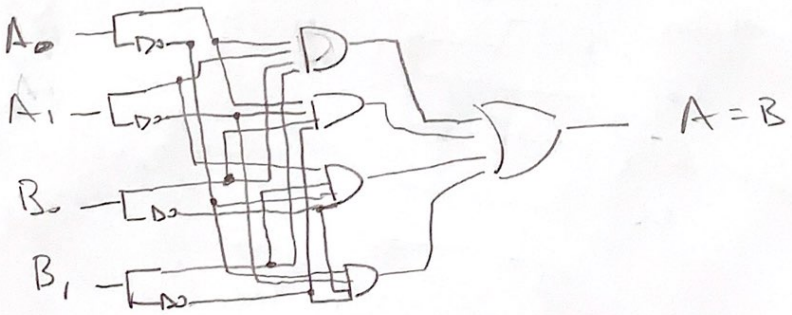
$$X = (A_1 \overline{B_1}) + (A_0 \overline{B_1} \overline{B_0}) + (A_1 A_0 \overline{B_0})$$



b.) A=B



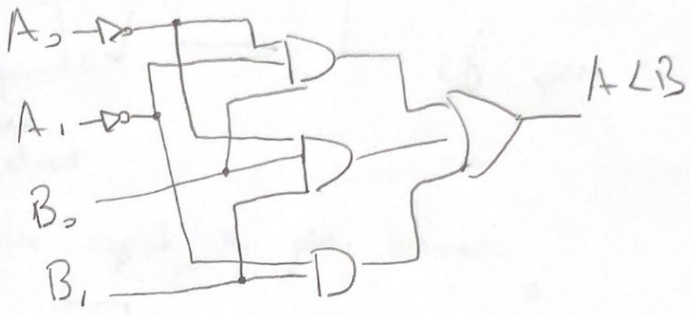
$$X = (\overline{A_1} \overline{A_0} \overline{B_1} \overline{B_0}) + (\overline{A_1} A_0 \overline{B_1} B_0) + (A_1 \overline{A_0} B_1 \overline{B_0}) + (A_1 A_0 B_1 B_0)$$



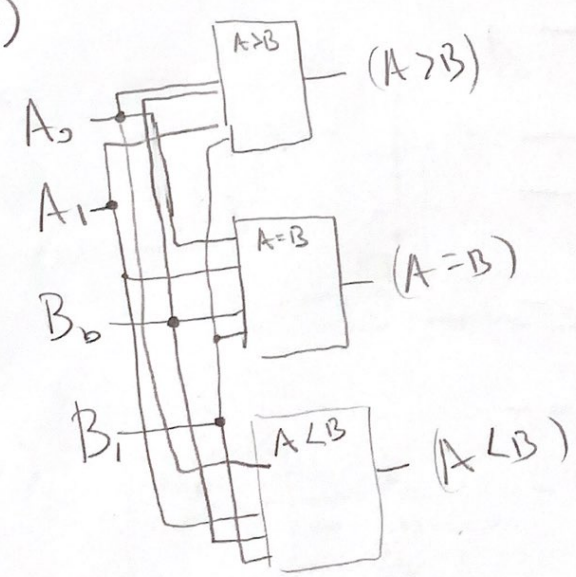
2.) c.) $A<B$

A_1A_0 \ B_1B_0	00	01	11	10
00		1	(1)	1
01				1
11				
10			(1)	

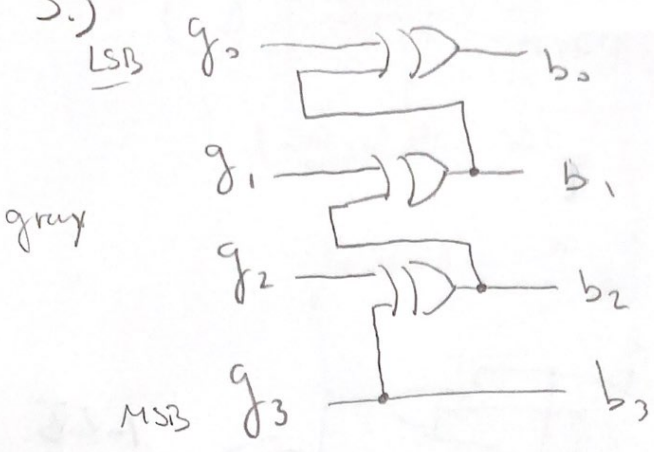
$$X = (B_1\bar{A}_1) + (B_0\bar{A}_1\bar{A}_0) + (B_1B_0\bar{A}_0)$$



d.)



3.)



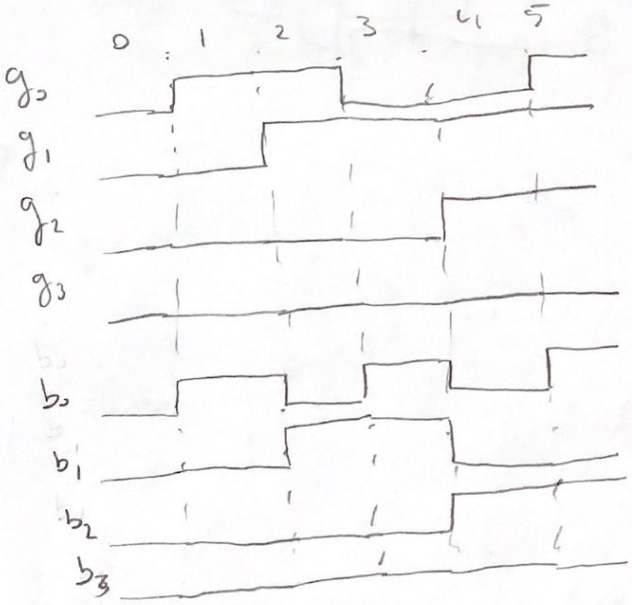
LSB

MSB

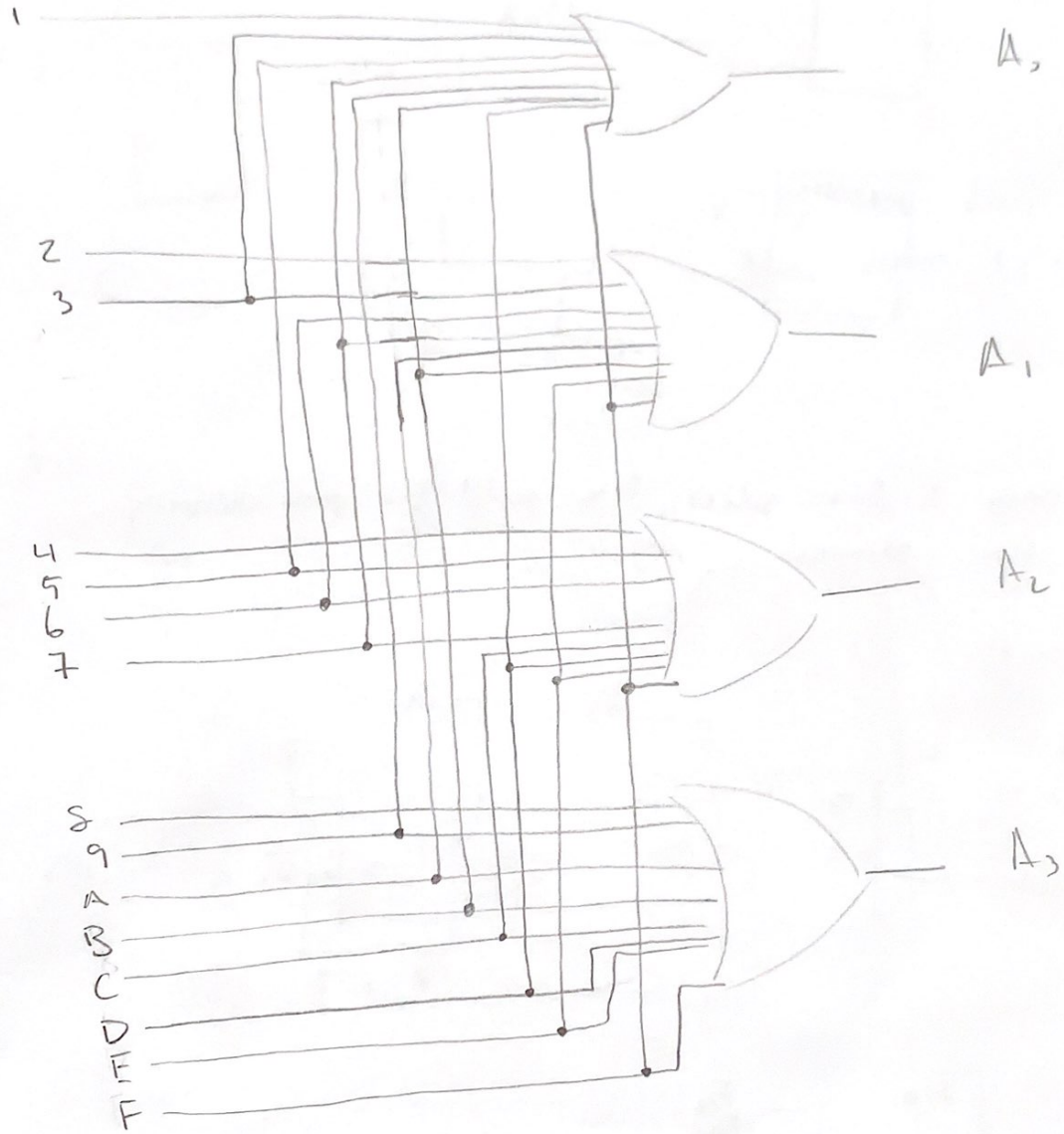
binary

XOR: addition (w/o carry)

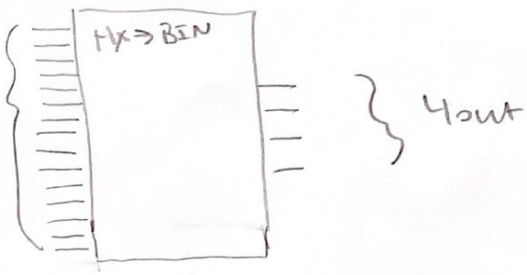
A	B	x
0	0	0
0	1	1
1	0	1
1	1	0



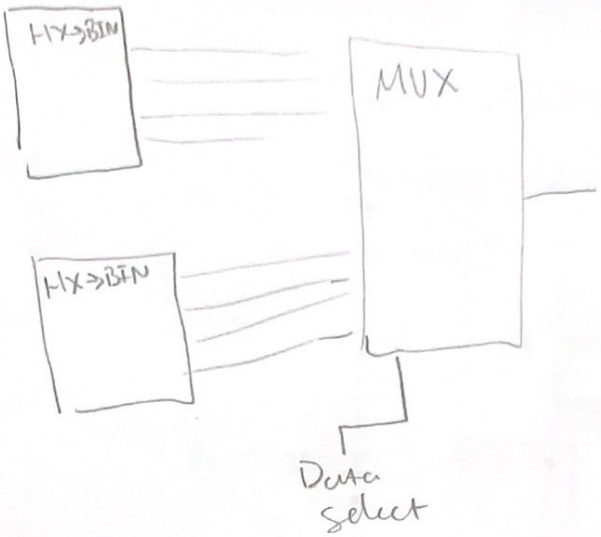
4.) a.)



b.)



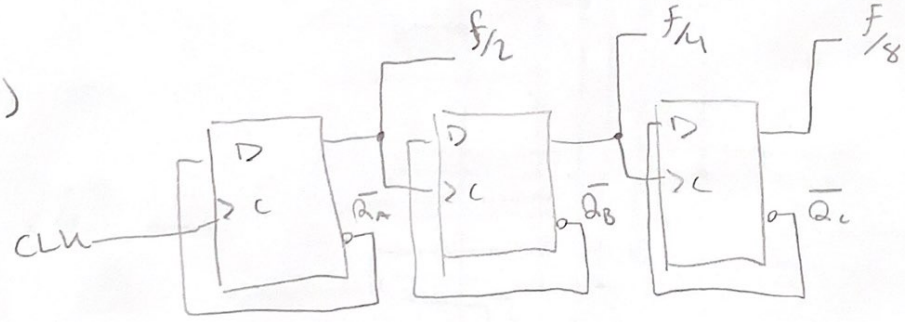
4.) c.)



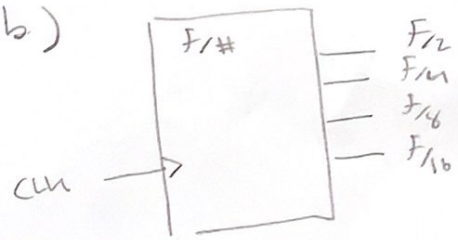
Only 1 data select line needed to pick between two states (1/0).

Ch 7

1.) a)



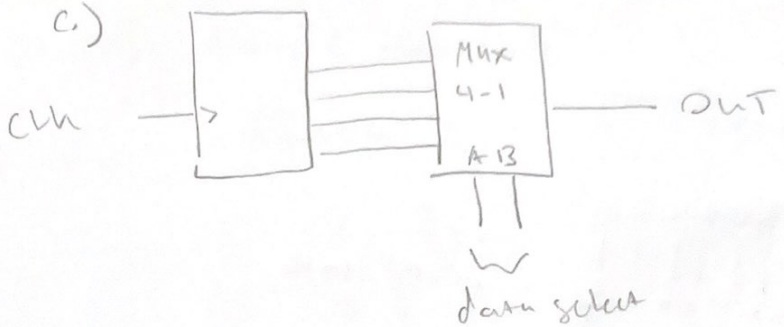
b.)



Ch 7

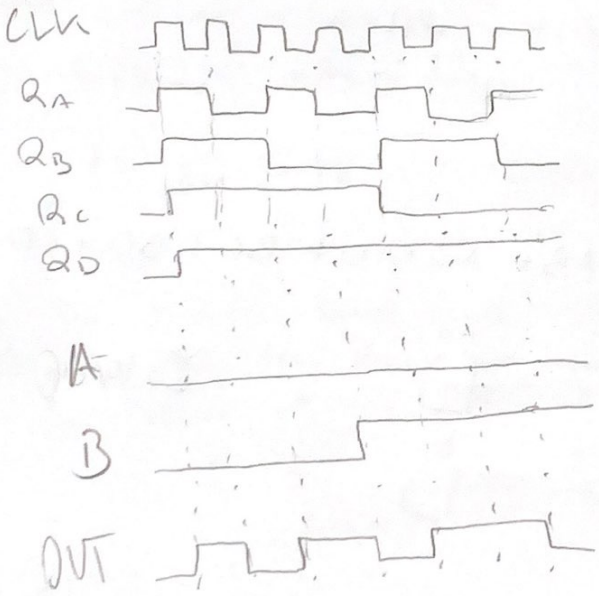
1.) cont

c.)



* Only two data select lines needed ($2^2 = 4$ options)

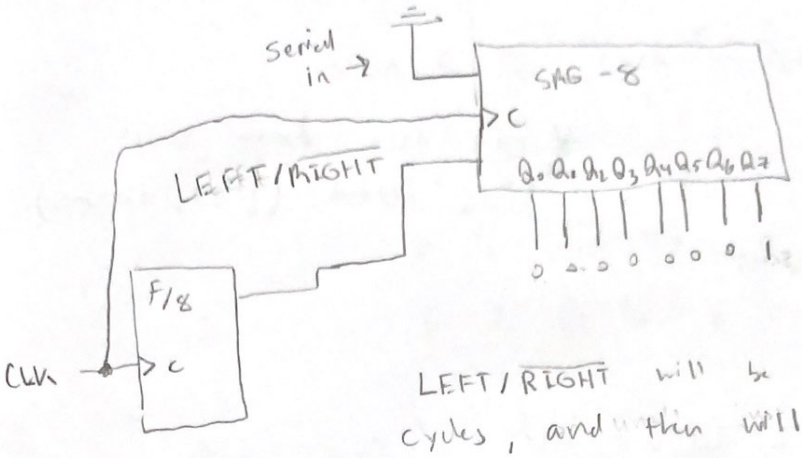
d.)



A	B	X
0	0	$f_{/2}$
0	1	$f_{/4}$
1	0	$f_{/8}$
1	1	$f_{/16}$

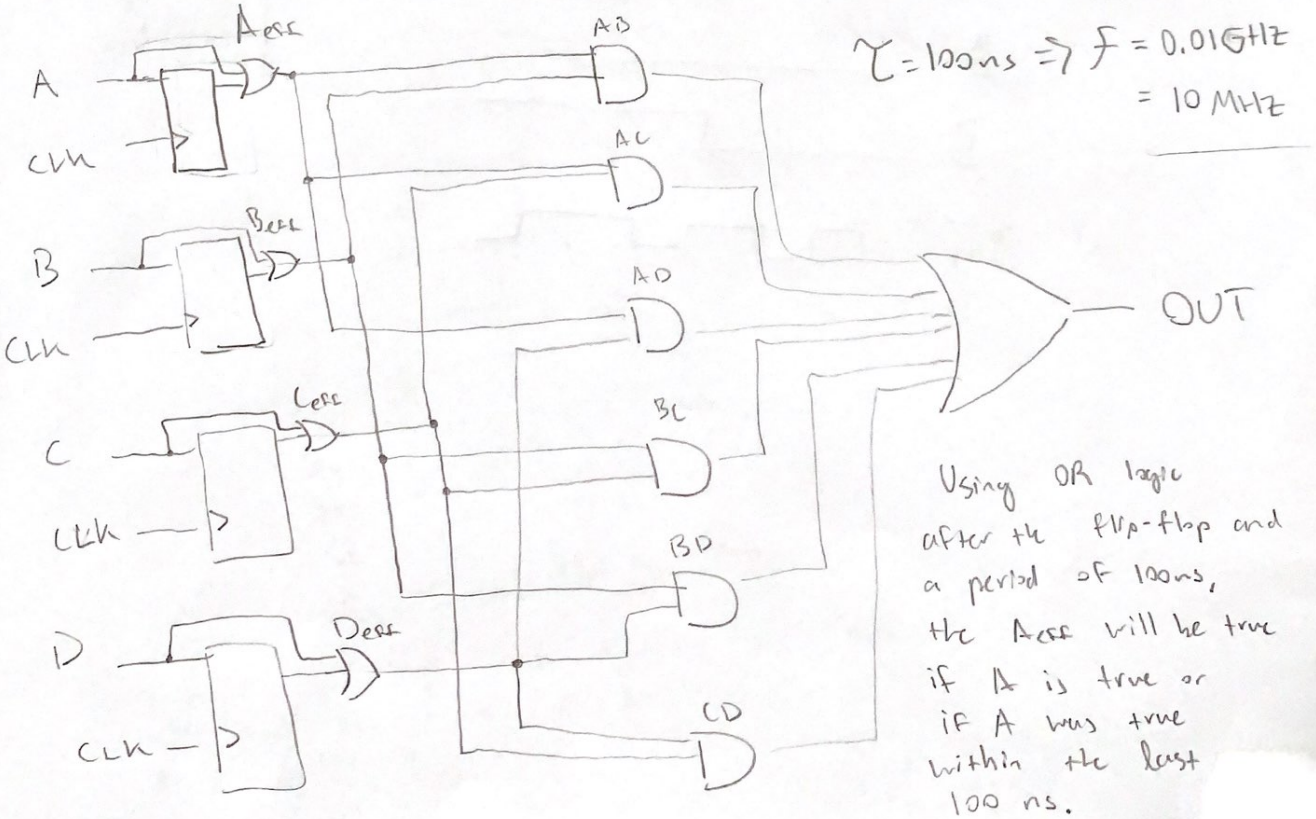
Ch 8/9

1.)



LEFT/$\overline{\text{RIGHT}}$ will be high for the first 8 cycles, and then will switch low for least 8.

2.) True IF $X = AB + AC + AD + BC + BD + CD$



$\tau = 100ns \Rightarrow f = 0.01GHz$
$= 10 MHz$

Using OR logic after the flip-flop and a period of 100ns, the Aeff will be true if A is true or if A was true within the least 100 ns.