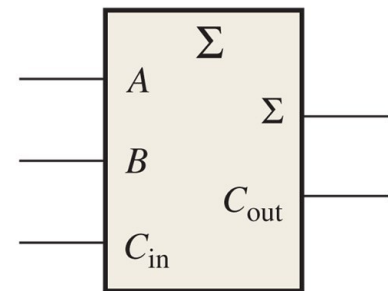


(a) Arrangement of two half-adders to form a full-adder



(b) Full-adder logic symbol