

Sackson Diamond

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## Midterm 2 for COSC330/PHYS306 - Fall 2021

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### 1 Chapter 6 - Functions of Combinational Logic

1. Consider Fig. 1, in which a 4-bit adder is depicted. Assuming a uniform worst-case delay of 8 ns from carry-in to carry-out for each stage, the total delay is 32 ns. (a) At what maximum frequency can this circuit perform additions, if the delay must be less than a clock period? (b) What would the result in (a) be if the adder was extended to 8 bits? (c) Create a timing diagram showing the addition of the numbers in Fig. 1. **Bonus:** include the timing delays, and indicate the clock period.

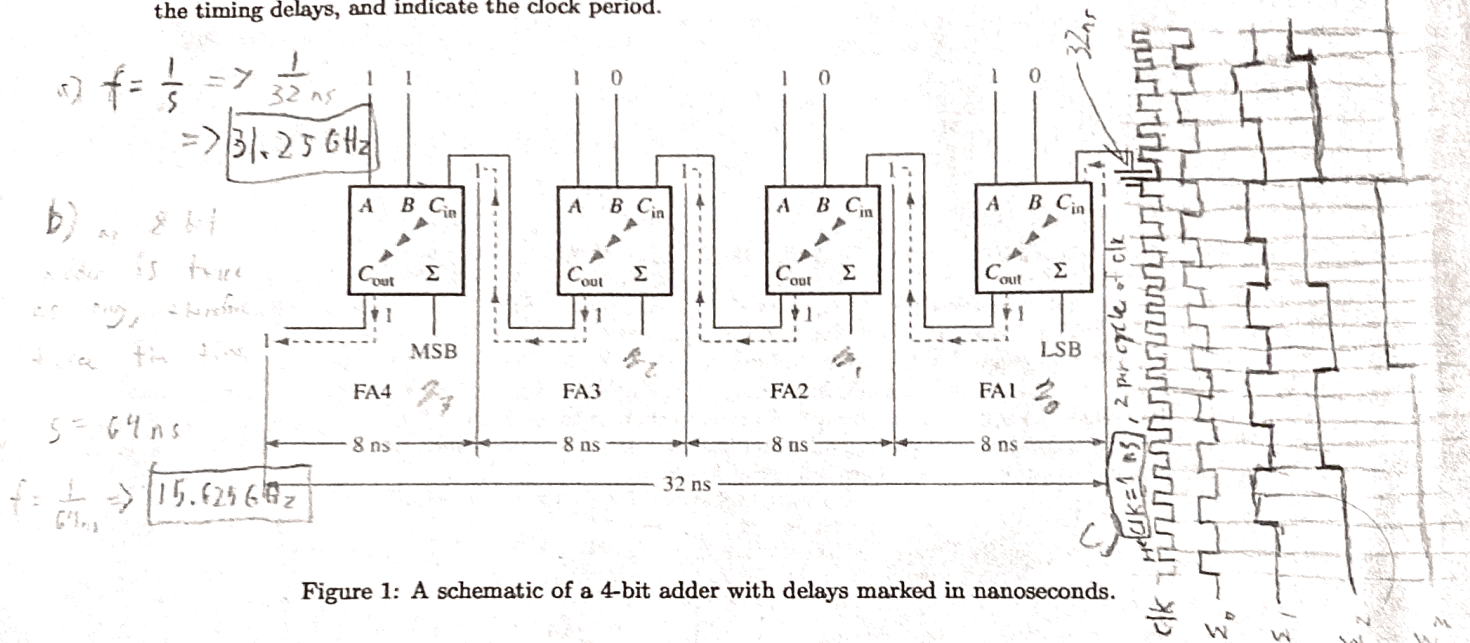
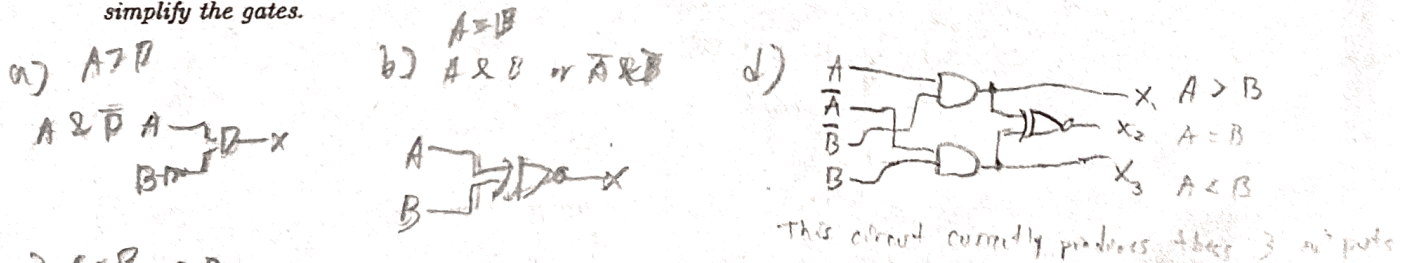
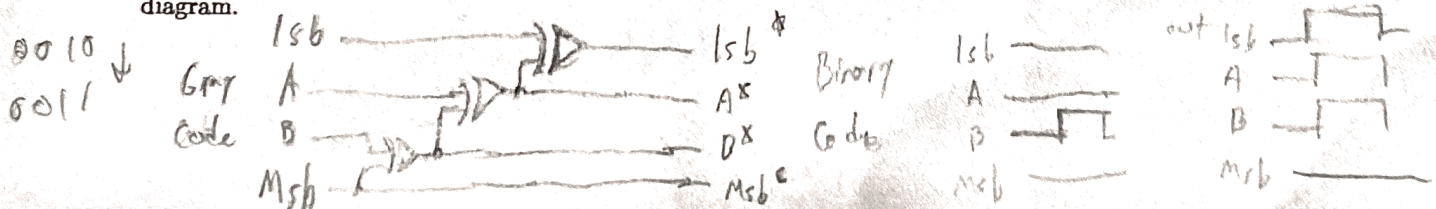


Figure 1: A schematic of a 4-bit adder with delays marked in nanoseconds.

2. Using AND, OR, XNOR, and inverter gates, (a) create a 2-bit comparator that yields True if  $A > B$ , (b) True if  $A = B$ , and (c) True if  $A < B$ . For each circuit, assume both  $A$  and  $B$  are 2-bit binary positive numbers. (d) Wrap this all into one circuit with three outputs and 4 inputs. *Hint: use Karnaugh maps for parts (a)-(c) to simplify the gates.*

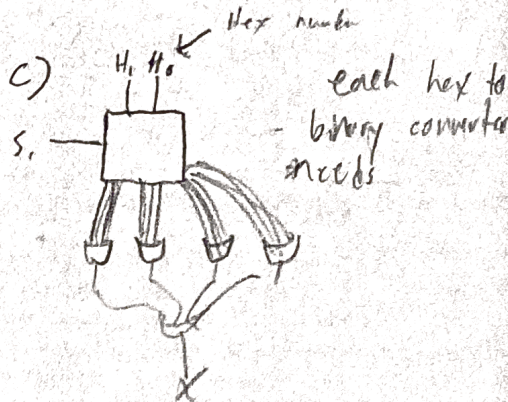


3. Generate the logic gates that convert 4-bit gray code to 4-bit binary code, and show that it works with a timing diagram.





- Add lines:  $\alpha$ )
- A,  $10 \rightarrow A_1, A_3$
- B,  $11 \rightarrow A_0, A_1, A_3$
- C,  $12 \rightarrow A_2, A_3$
- D,  $13 \rightarrow A_0, A_2, A_3$
- E,  $14 \rightarrow A_1, A_2, A_3$
- F,  $15 \rightarrow A_0, A_1, A_2, A_3$



b) It's the same circuit as Figure 2 with the addition of input lines for A-F, which follow the paths in part A.

1. Consider Fig. 3, in which a divide-by-four frequency divider is depicted with D flip-flops and a CLK signal. (a) Elaborate on this circuit to create a circuit that can divide the clock frequency by 2, 4, or 8. Show the flip-flops explicitly. (b) Develop a symbol for the 2-4-8-16 divider, with CLK signal input and four outputs (one each for  $f/2$ ,  $f/4$ ,  $f/8$ , and  $f/16$ , where  $f$  is the clock frequency). (c) Connect the symbol for the new part to a symbolic 4-to-1 multiplexer with the appropriate number of data select lines to form a clock division system. (d) Show with a timing diagram the output if the user changes the data select lines at least once. For parts (b)-(d), it is only necessary to show symbols rather than individual flip-flops.

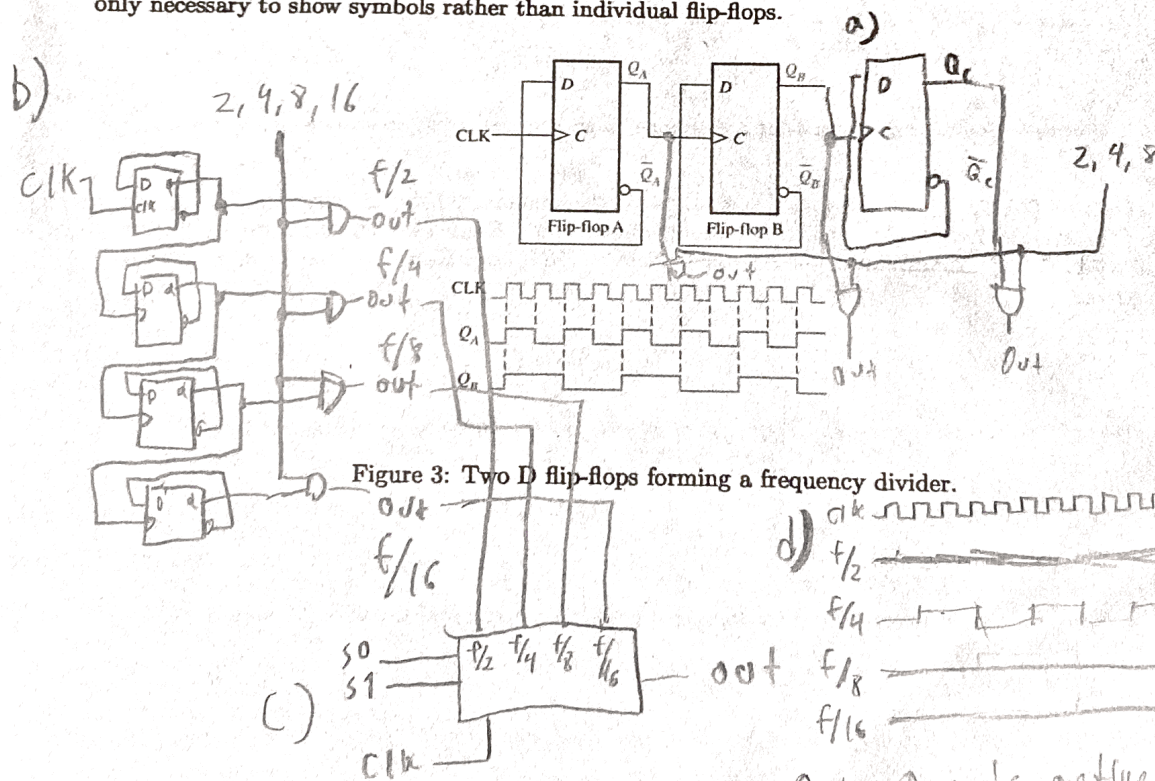






Figure 3: Two D flip-flops forming a frequency divider.


frequency divider.

d)  $f_{clk}$  

$f/2$  

$f/4$  

$f/8$  

$f/16$  

Only One is active if data selected  
is 01 =  $f/4$  output.



### 3 Chapters 8 and 9 - Shift Registers and Counters

1. Consider the timing diagram in Fig. 4. Using any combination of *shift registers* and supporting gates, create a circuit with 8-outputs that produces this timing diagram.

msb  
lsb  
S.I. = 1000 0000

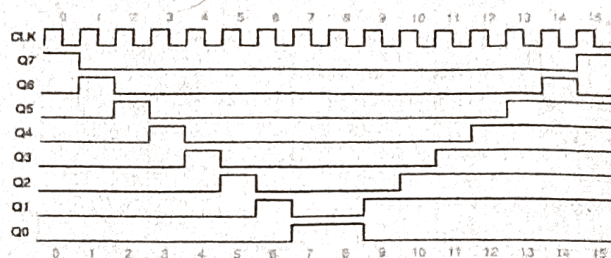
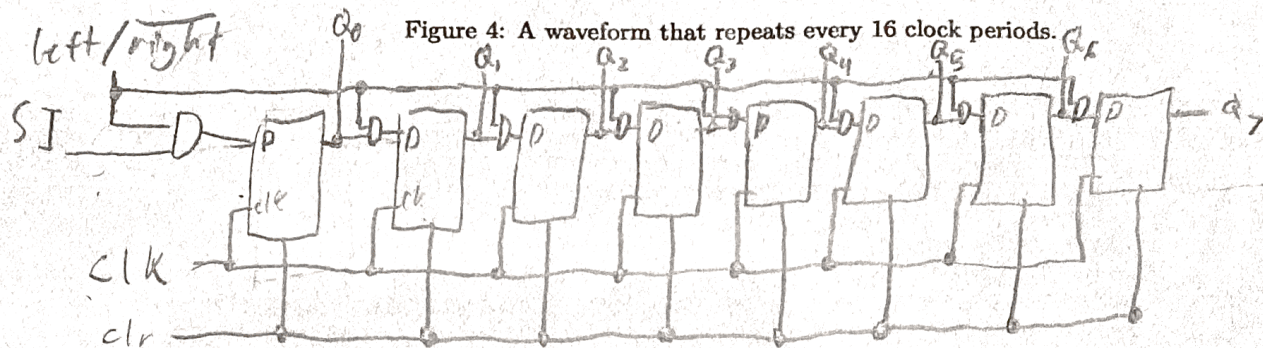


Figure 4: A waveform that repeats every 16 clock periods.



2. Consider Fig. 5, in which 4 and 5-bit Johnson counters are depicted. (a) Create a circuit based on Fig. 5 called a *combinatoric trigger*. Imagine four digital channels A, B, C, and D, as inputs. The output of the circuit should be True if *any two* of the four channels is True *within 100 ns of each other*. Develop any necessary logic symbols, and use the appropriate clock frequency. The Johnson counter(s) can have any number of bits.

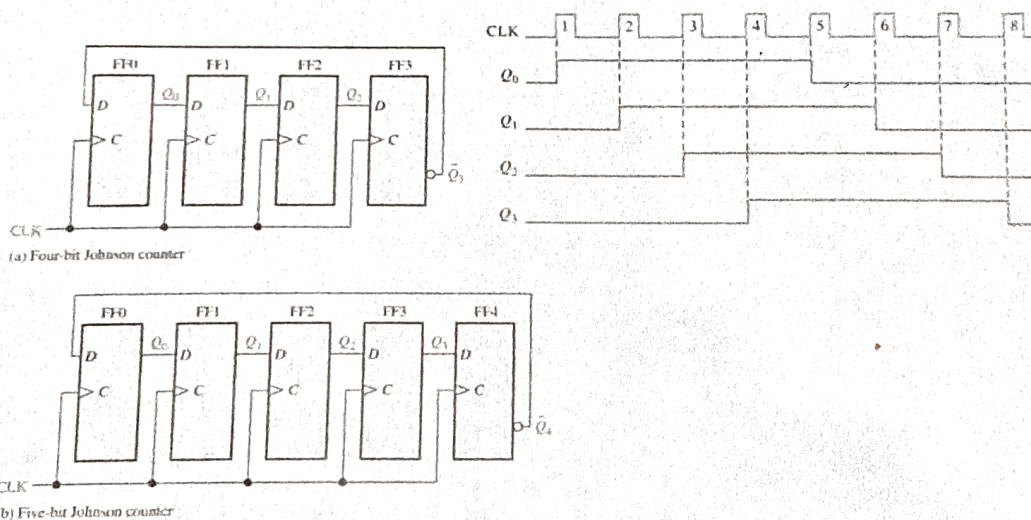


Figure 5: (Left) 4 and 5-bit Johnson counters. (Right) The timing diagram for the 4-bit case.

