Computer Logic and Digital Circuit Design (PHYS306/COSC330): Unit 3

Jordan Hanson

March 21, 2024

Whittier College Department of Physics and Astronomy

Summary

Unit 3 Summary

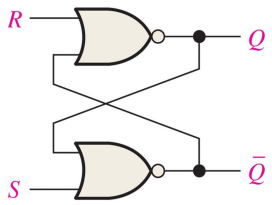
Reading: chapter 7

We now know how to generate and process digital data. We can do algebra, compare numbers, encode, decode, and multiplex. *How does memory work? How is information held in digital systems?*

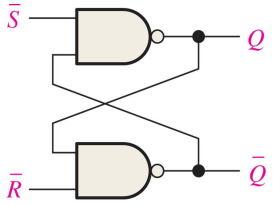
1. S-R latches
    - Basic latch, de-bounce
    - Gated latch
    - D-latch
2. Flip-flops
    - JK flip-flops
    - Synchronous vs. level-sensitive
3. Flip-flop applications

S-R Latches

S-R Latches



(a) Active-HIGH input S-R latch



(b) Active-LOW input $\bar{S}$-$\bar{R}$ latch

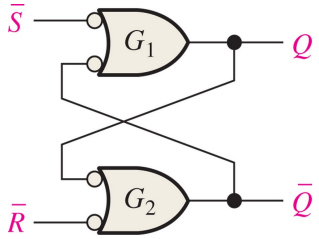


TABLE 7–1

Truth table for an active-LOW input $\bar{S}$-$\bar{R}$ latch.

Inputs		Outputs		
$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$	Comments
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1	1	Invalid condition

Figure 1: An S-R latch is a *multivibrator* that holds its state when SET, or RESET.

S-R Latches

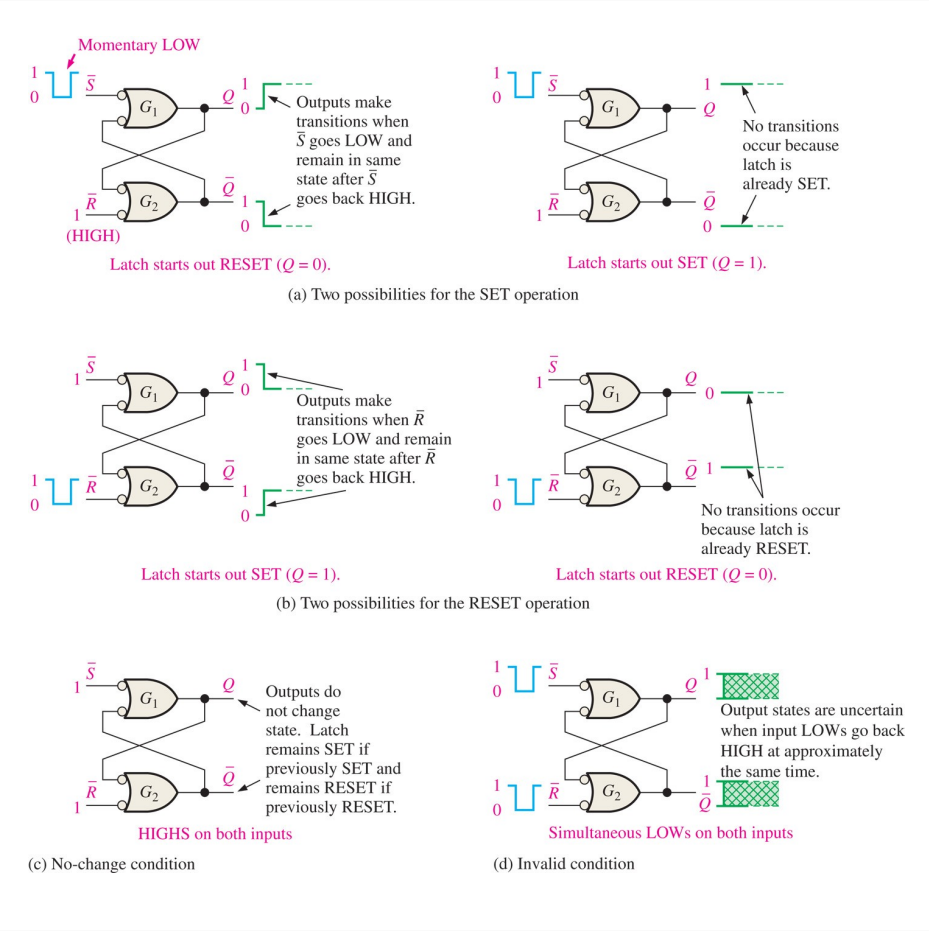


Figure 2: Summary of potential states of a basic S-R latch.

S-R Latches

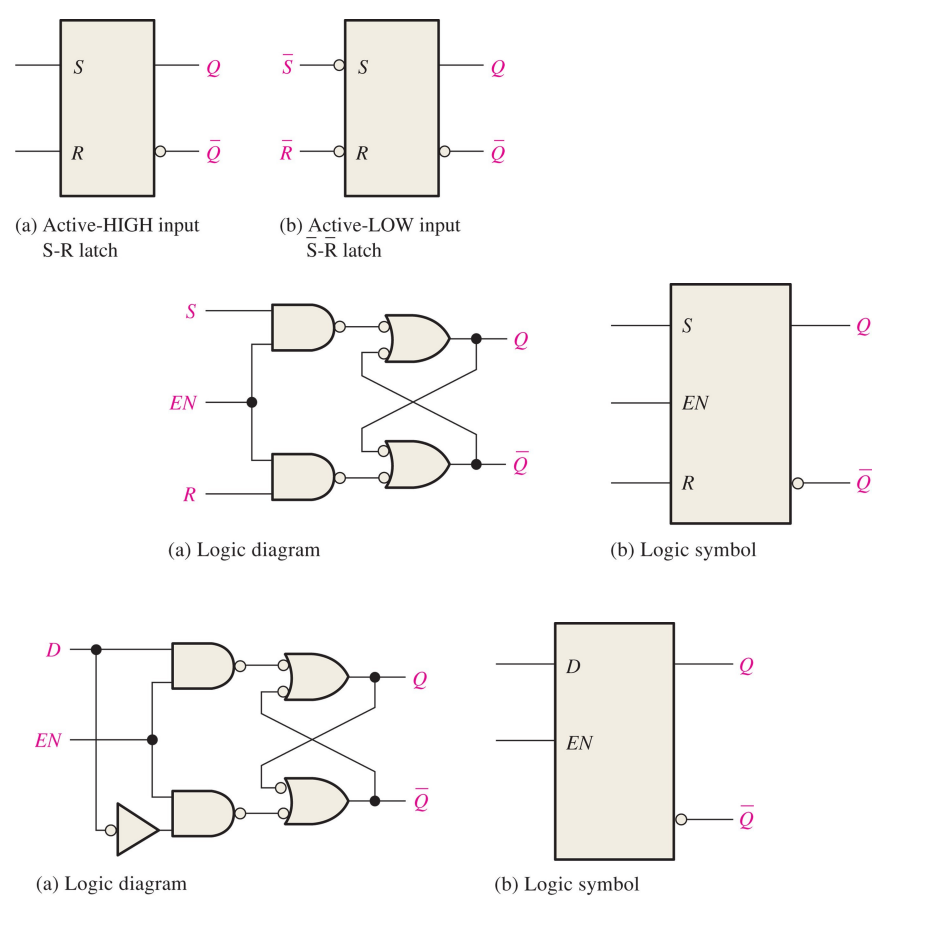


Figure 3: The basic, gate-enabled, and D-latch systems. For the latter two, both the gate and symbol are shown.

S-R Latches

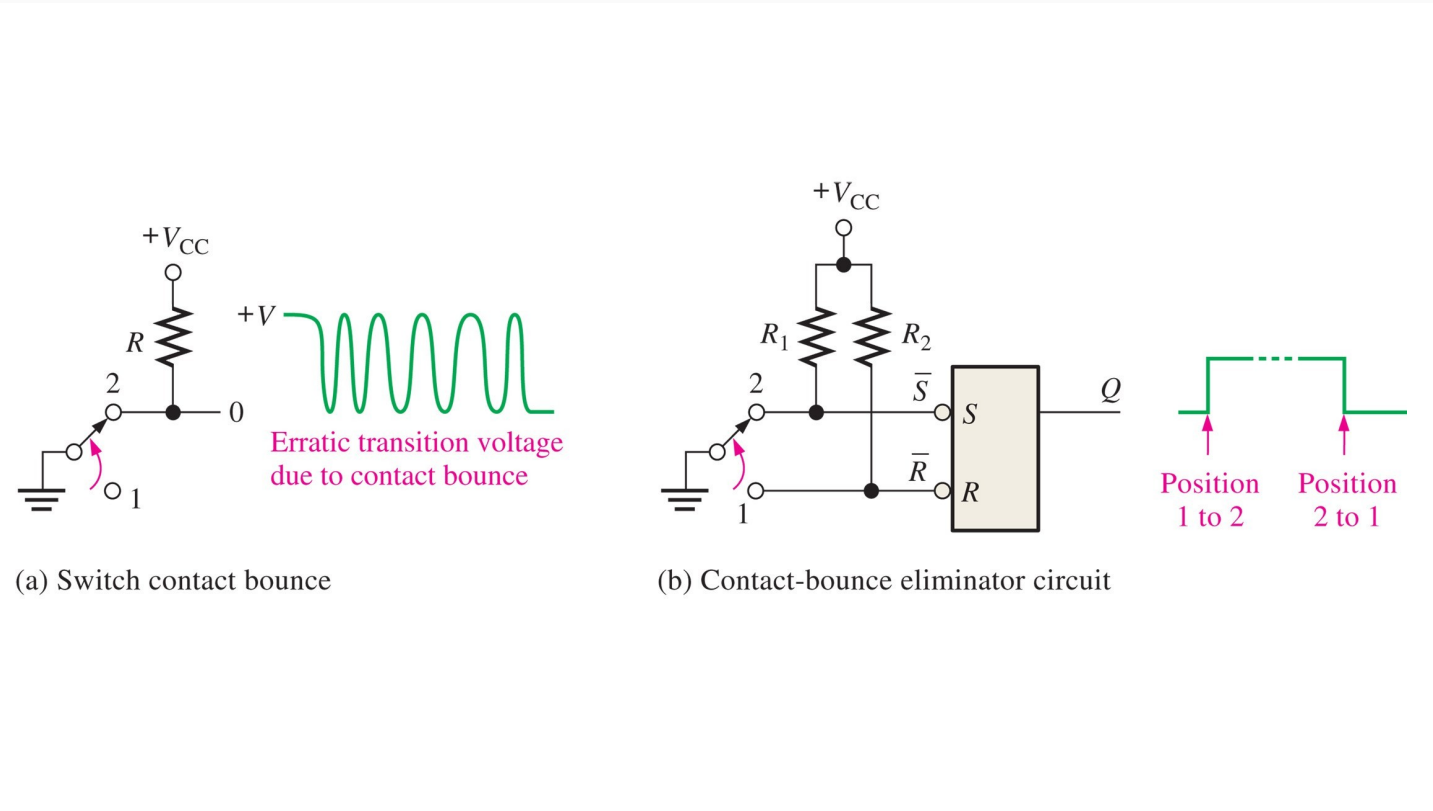


Figure 4: De-bouncing is important any time a mechanical switch is meant to interact with digital logic.

Flip Flops

Flip-Flops

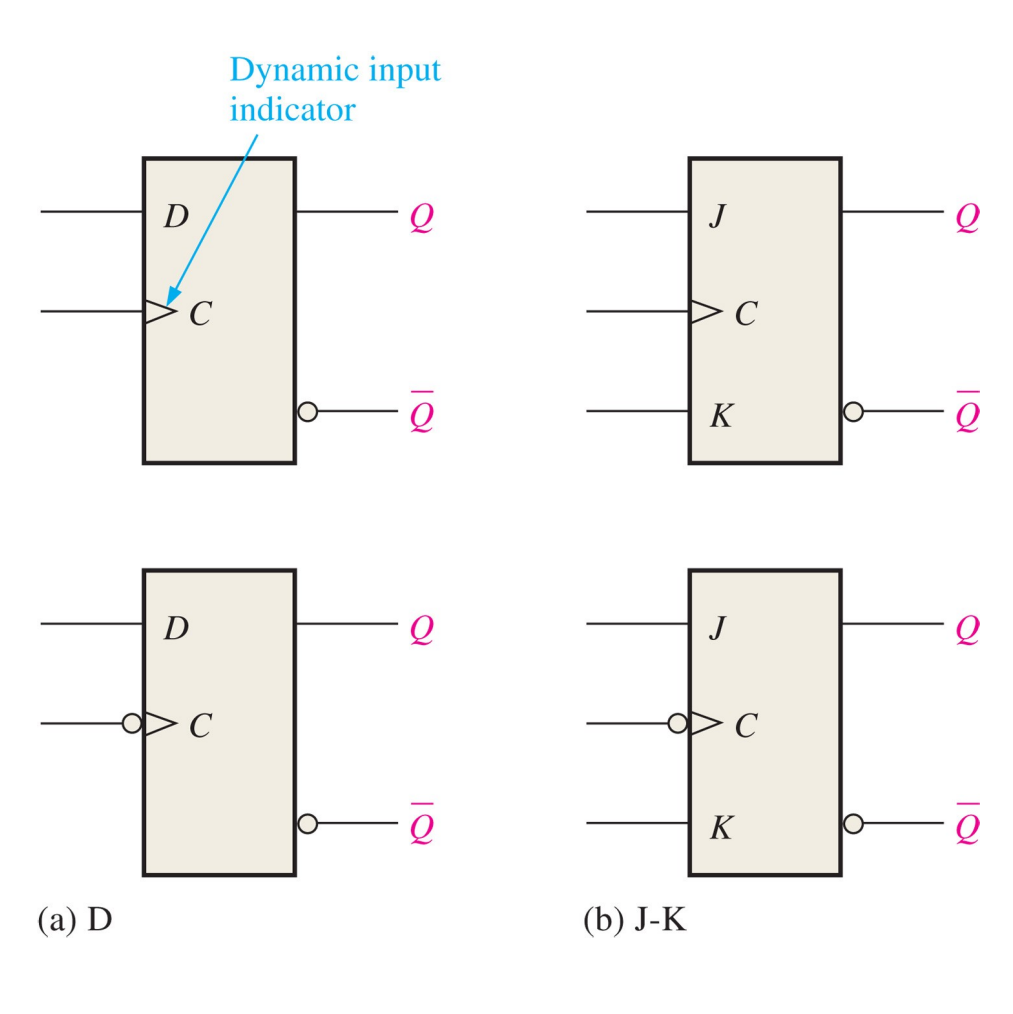
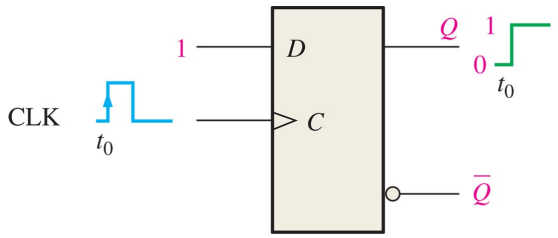
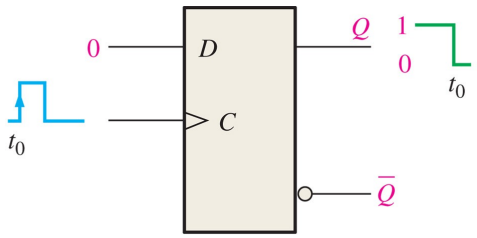


Figure 5: Four types of **synchronous** latches called flip-flops.

Flip-Flops



(a) $D = 1$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)



(b) $D = 0$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)

TABLE 7–2

Truth table for a positive edge-triggered D flip-flop.

Inputs		Outputs		
D	**CLK**	***Q***	$\overline{Q}$	**Comments**
0	↑	0	1	RESET
1	↑	1	0	SET

↑ = clock transition LOW to HIGH

Figure 6: The symbol and TT for the D-flip flop. The behavior is simular to a D-latch without enable, but only on positive edge of clock (posedge).

Flip-Flops

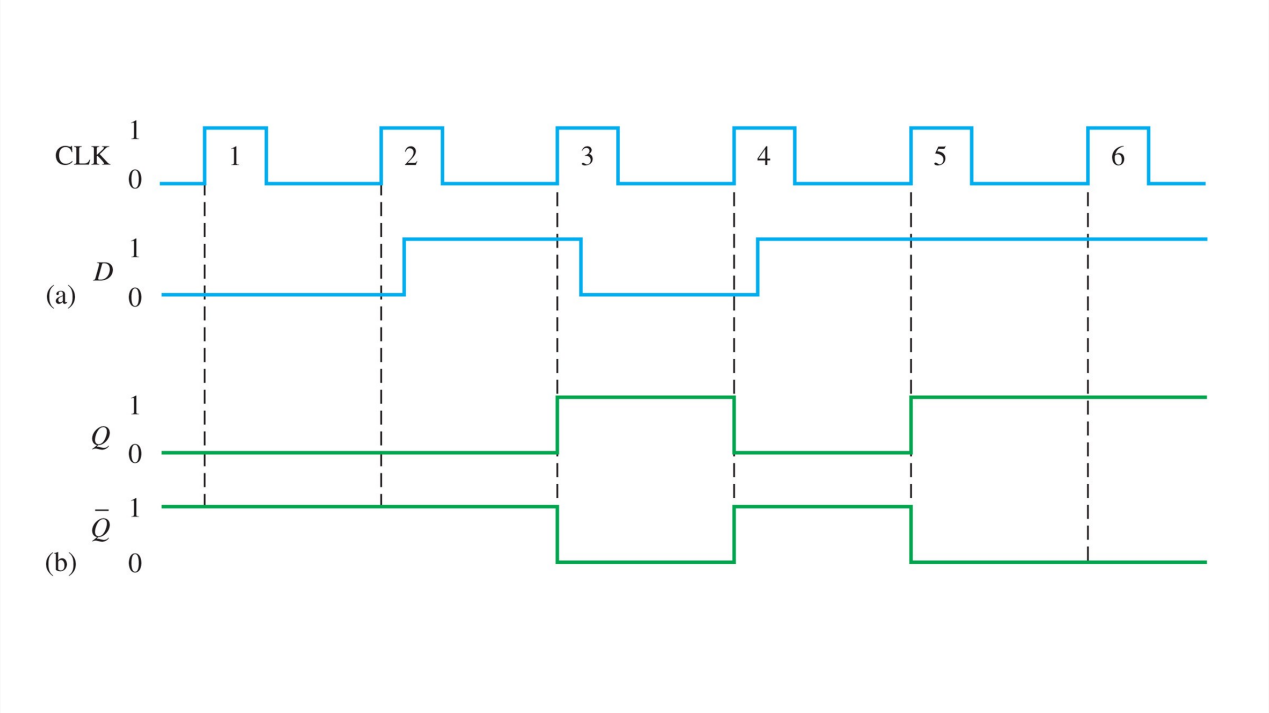


Figure 7: Example of D flip-flop behavior.

Flip-Flops

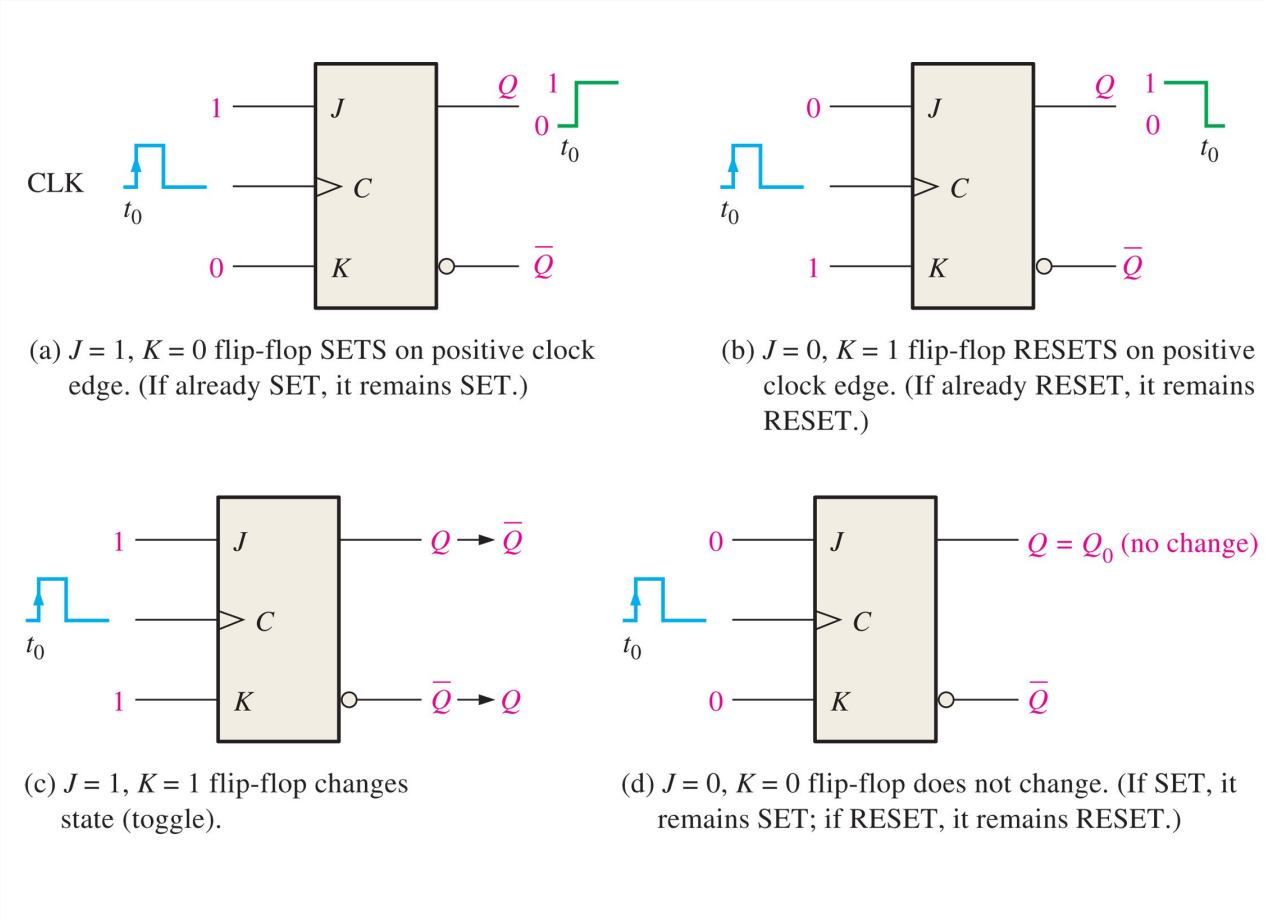


Figure 8: The JK flip flop, triggered on posedge. There are still the SET and RESET states, but the other two states differ from the SR latch.

Flip-Flops

TABLE 7–3

Truth table for a positive edge-triggered J-K flip-flop.

Inputs			Outputs		
J	K	CLK	Q	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

↑ = clock transition LOW to HIGH

Q_0 = output level prior to clock transition

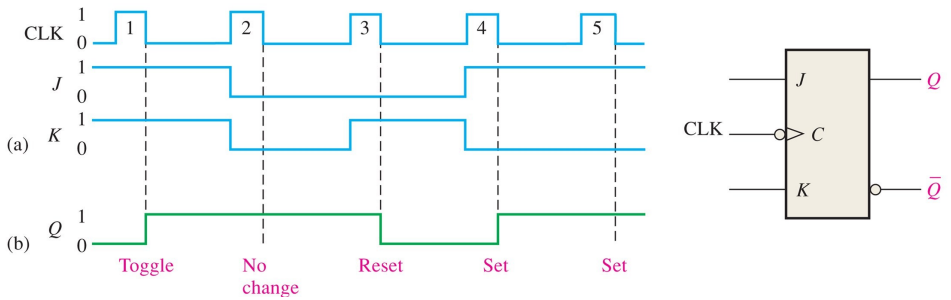


Figure 9: The TT for the JK flip flop, which is also **synchronous**. An example timing diagram is given for the JK as well.

Flip-Flops

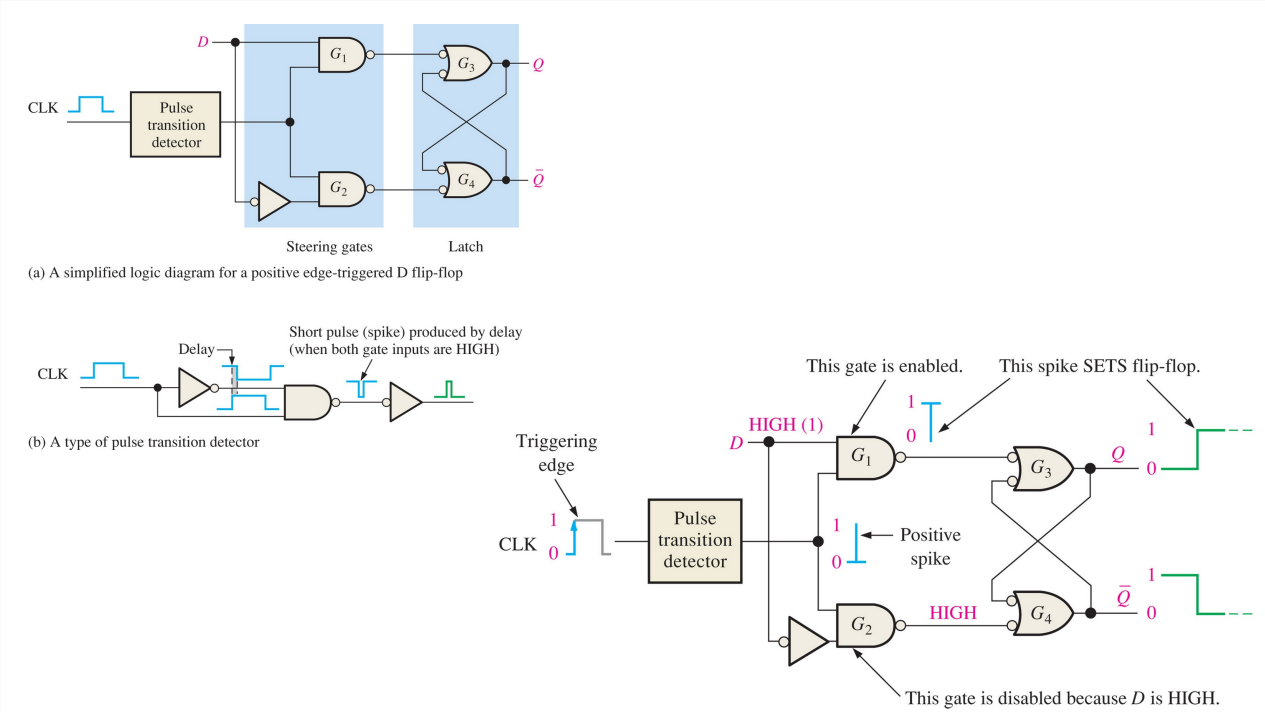


Figure 10: How does the posedge triggering work? Physically, it is based on *propagation delay*. The D flip-flop is pictured as an example, with spikes. *What counts as a spike?*

Flip-Flops

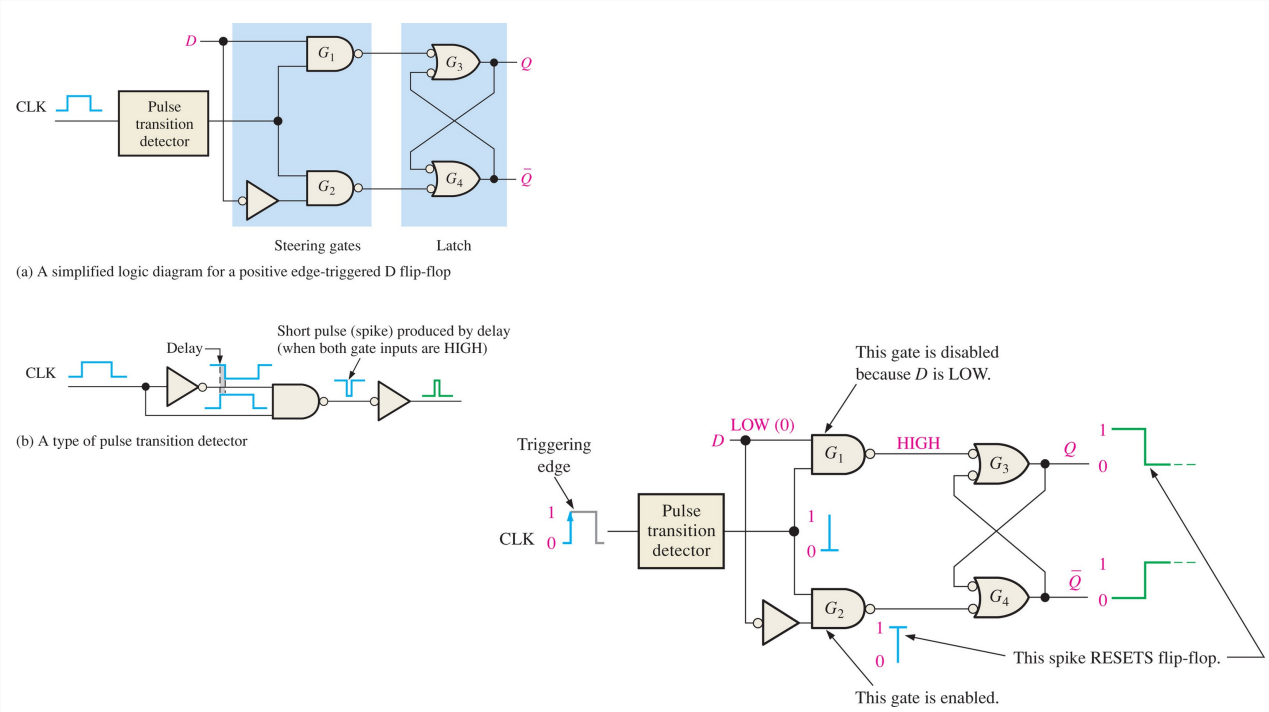


Figure 11: How does the posedge triggering work? Physically, it is based on *propagation delay*. The D flip-flop is pictured as an example, with spikes. *What counts as a spike?*

Flip-Flops

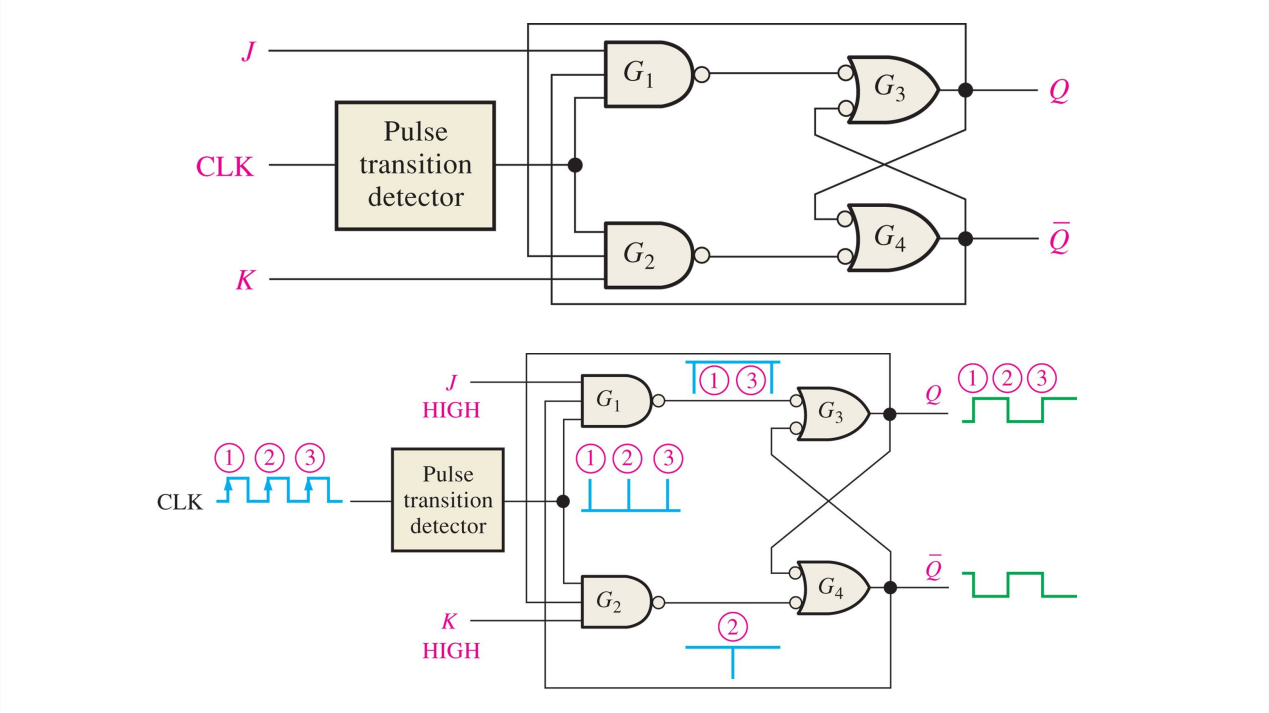


Figure 12: Circuit diagram with symbols for the JK flip flop, with posedge trigger. The JK flip-flop is in toggle mode.

Flip-Flops

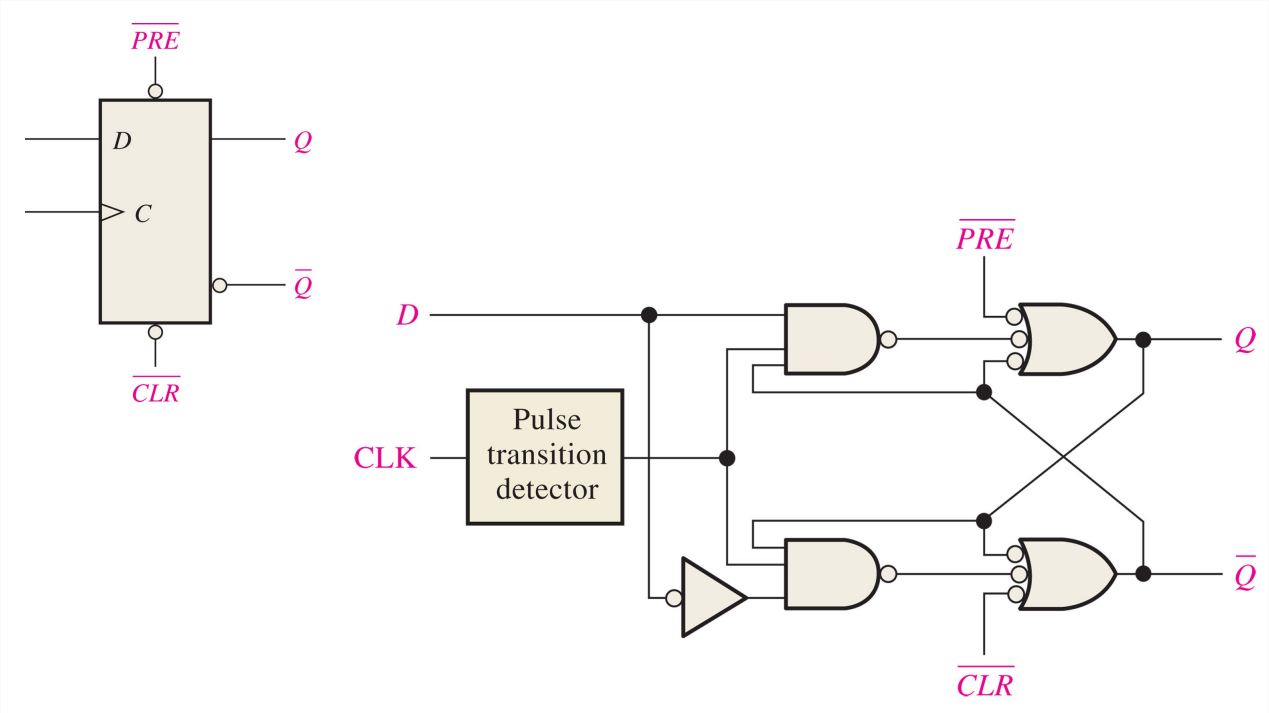
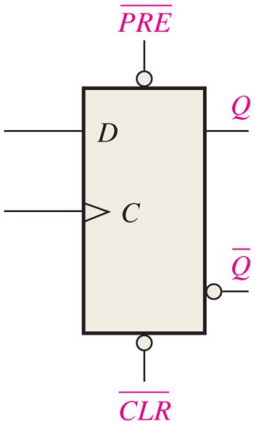
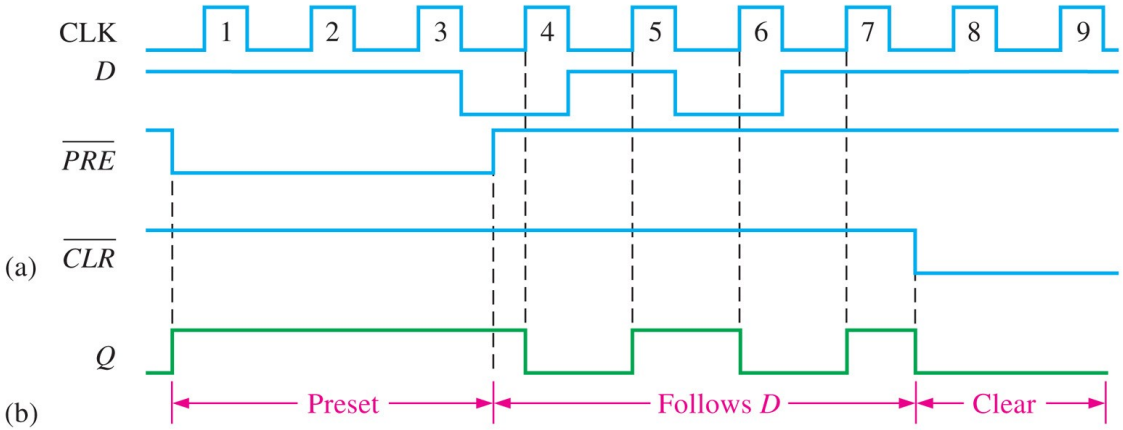


Figure 13: Addig two asynchronous features, preset and clear. These override the synchronous features due to the way they are used.

Flip-Flops


PRE
D
Q
C
Q
CLR


CLK
1
2
3
4
5
6
7
8
9
D
PRE
(a)
CLR
Q
(b)
Preset
Follows D
Clear

Flip Flop Applications

Flip Flop Applications

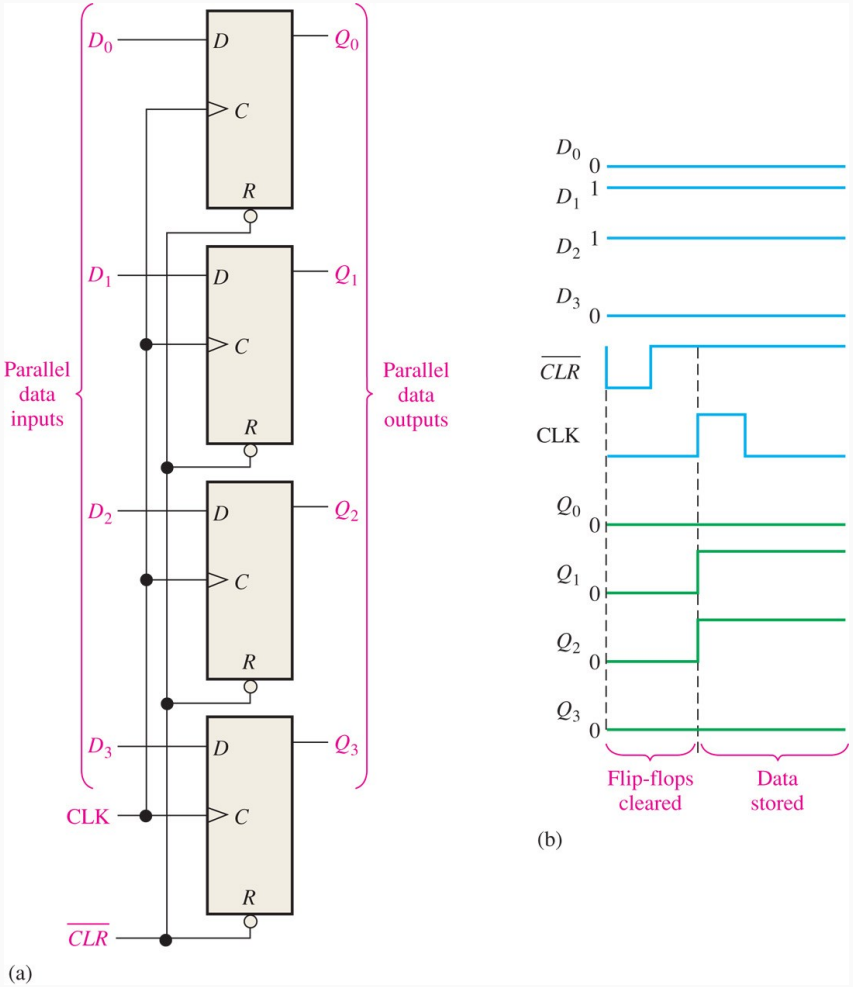


Figure 15: 4-bit parallel memory storage.

Flip Flop Applications

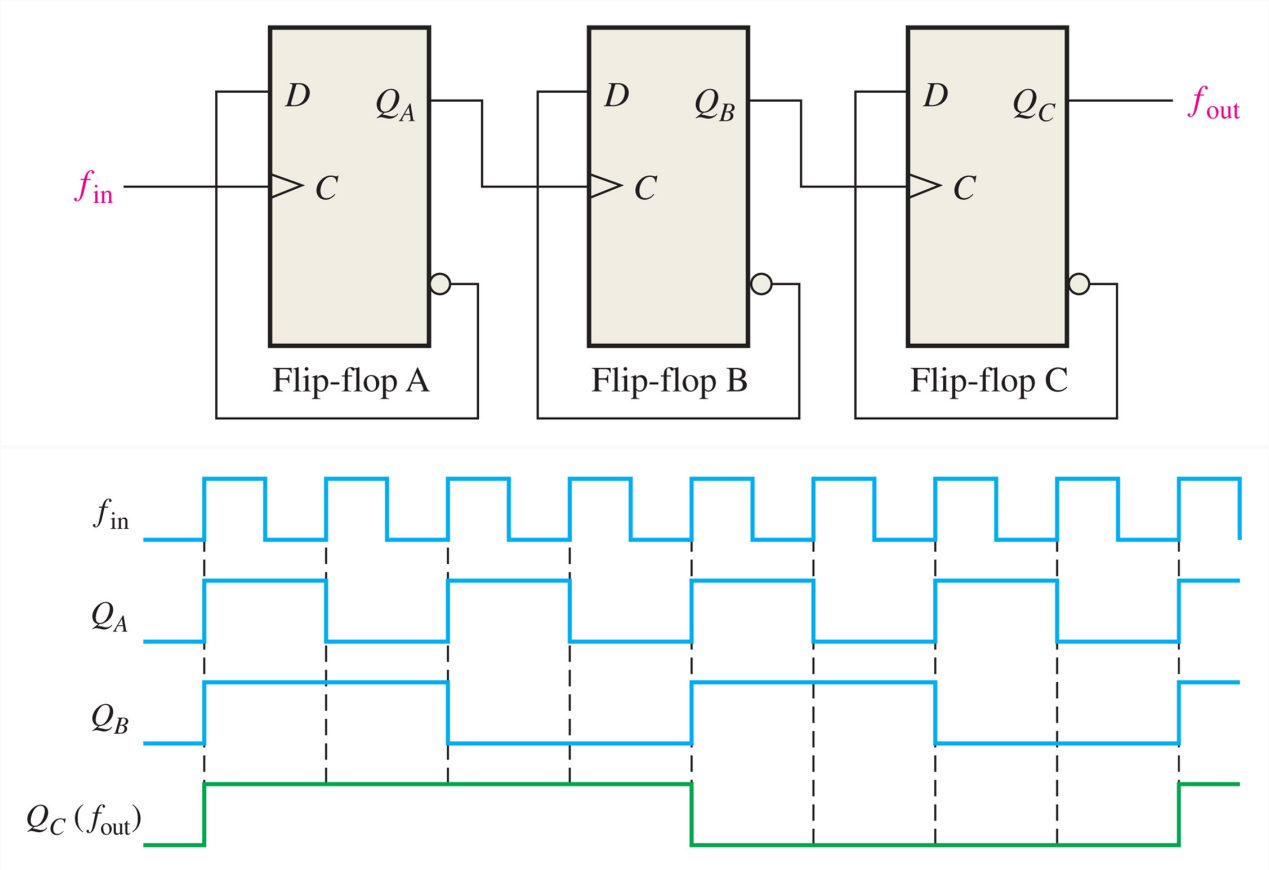


Figure 16: Frequency divider. What is the ratio $f_{\text{out}}/f_{\text{in}}$?

Flip Flop Applications

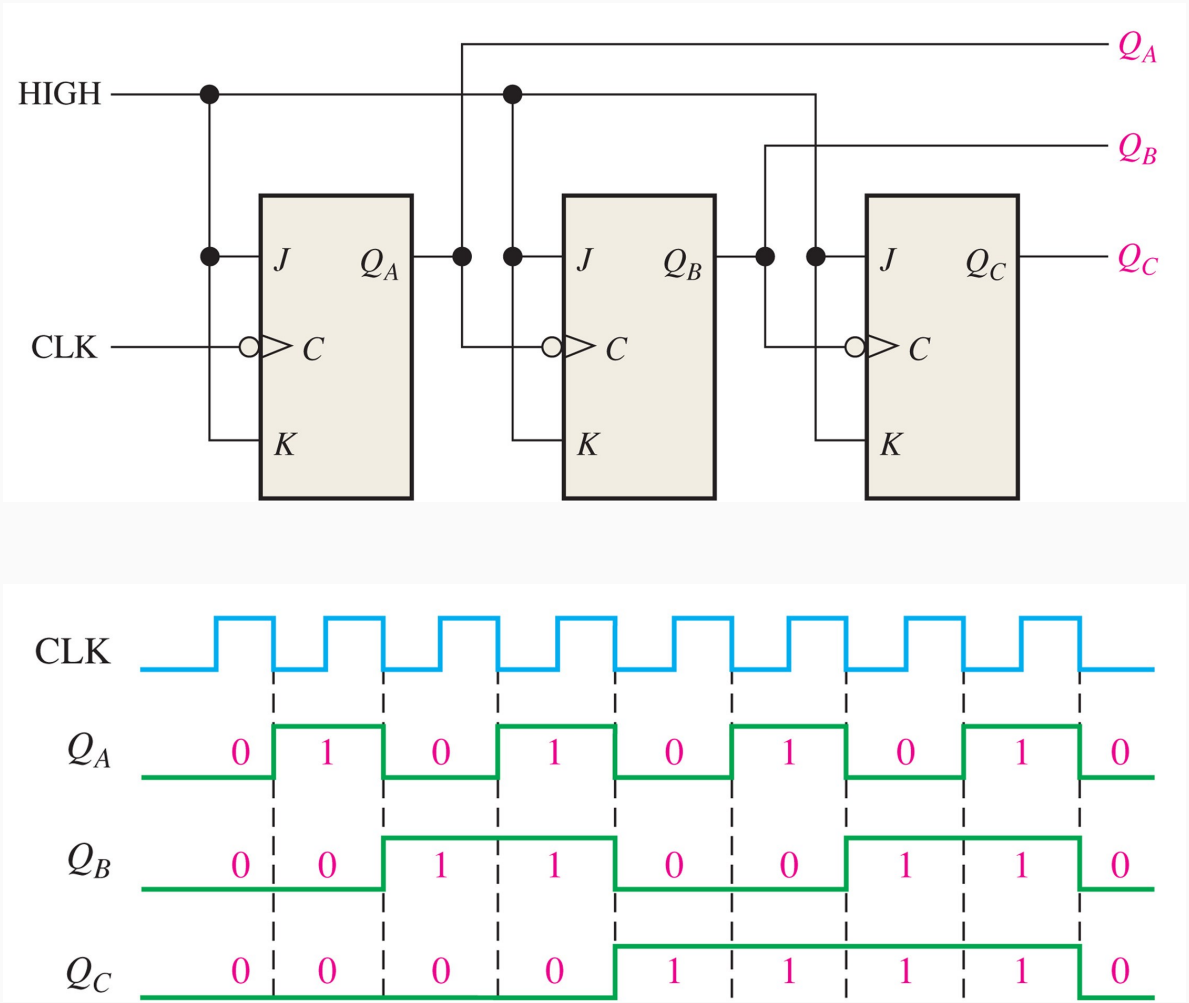


Figure 17: A 3-bit counter built from 3 JK flip-flops.

Conclusion

Unit 3 Summary

Reading: chapter 7

We now know how to generate and process digital data. We can do algebra, compare numbers, encode, decode, and multiplex. *How does memory work? How is information held in digital systems?*

1. S-R latches
    - Basic latch, de-bounce
    - Gated latch
    - D-latch
2. Flip-flops
    - JK flip-flops
    - Synchronous vs. level-sensitive
3. Flip-flop applications

Move the subject of timers to later date.