Computer Logic and Digital Circuit Design (PHYS306/COSC330): Unit 1

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Summary

Unit 1 Summary - Theoretical Logic Gates, and Operations

1. Logic Gates
    - Circuit diagram
    - Truth table
    - Timing diagram
    - Boolean logic
2. Boolean algebra I
3. Boolean algebra II
4. Dual logic symbols and logic diagrams

Karnaugh Maps

Karnaugh Maps

A **Karnaugh Map**, or K-map, is a *cell-array*, with 2^N cells, where N is the number of logical inputs.

AB \ C	0	1
00	000	001
01	010	011
11	110	111
10	100	101

AB \ C	0	1
00	$\overline{A}\ \overline{B}\ \overline{C}$	$\overline{A}\ \overline{B}\ C$
01	$\overline{A}\ B\ \overline{C}$	$\overline{A}\ \overline{B}\ C$
11	$A\ B\ \overline{C}$	$\overline{A}\ \overline{B}\ C$
10	$A\ \overline{B}\ \overline{C}$	$\overline{A}\ \overline{B}\ C$

Table 1: The 3-input Karnaugh map, or K-map, lists all possible outcomes of a logic operation for all possible input combinations. (Left) Bit sequence representation of all input combinations. (Right) Symbolic representation of all input combinations.

Karnaugh Maps

AB \ CD	00	01	11	10
00	0000	0001	0011	0010
01	0100	0101	0111	0110
11	1100	1101	1111	1110
10	1000	1001	1011	1010

AB \ CD	00	01	11	10
00	$\overline{A}\ \overline{B}\ \overline{C}\ \overline{D}$	$\overline{A}\ \overline{B}\ \overline{C}\ D$	$\overline{A}\ \overline{B}\ C\ D$	$\overline{A}\ \overline{B}\ C\ \overline{D}$
01	$\overline{A}\ B\ \overline{C}\ \overline{D}$	$\overline{A}\ B\ \overline{C}\ D$	$\overline{A}\ B\ C\ D$	$\overline{A}\ B\ C\ \overline{D}$
11	$A\ B\ \overline{C}\ \overline{D}$	$A\ B\ \overline{C}\ D$	$A\ B\ C\ D$	$A\ B\ C\ \overline{D}$
10	$A\ \overline{B}\ \overline{C}\ \overline{D}$	$A\ \overline{B}\ \overline{C}\ D$	$A\ \overline{B}\ C\ D$	$A\ \overline{B}\ C\ \overline{D}$

Table 2: The 4-input K-map, in the same notation as Tab. 1.

Karnaugh Maps

K-maps have several requirements for *adjacent cells*.

1. **Only one bit change** between adjacent cells.
2. Cells have *wrap-around* adjacency.
3. Diagonal cells are not adjacent.

Karnagh Maps: Mapping S-SOP expressions

A S-SOP expression may be mapped to a K-map:

AB \ CD	00	01	11	10
00	1	1		
01		1	1	
11		1		
10		1		

Table 3: The 4-input K-map, with an S-SOP mapped.

S-SOP expression that is being mapped:

$$\overline{A}\ \overline{B}\ \overline{C}\ \overline{D} + \overline{A}\ \overline{B}\ \overline{C}\ D + \overline{A}\ B\ \overline{C}\ D + A\ B\ \overline{C}\ D + A\ \overline{B}\ \overline{C}\ D + \overline{A}\ B\ C\ D$$

Karnagh Maps: Mapping S-SOP expressions

AB \ CD	00	01	11	10
00		1		
01		1		
11		1		
10		1		

Table 4: The 4-input K-map, with an S-SOP mapped.

SOP expression that is being mapped:

$\overline{A}\ \overline{B}\ \overline{C}\ D + \overline{A}\ B\ \overline{C}\ D + A\ B\ \overline{C}\ D + A\ \overline{B}\ \overline{C}\ D$

Karnagh Maps: Mapping non-standard SOP expressions

AB \ CD	00	01	11	10
00		1	1	
01		1	1	
11		1	1	
10		1	1	

Table 5: The 4-input K-map, with an S-SOP mapped.

S-SOP expression that is being mapped:

$\overline{A}\ \overline{B}\ \overline{C}\ D + \overline{A}\ B\ \overline{C}\ D + D$

(We must enumerate the non-standard term). We could convert to standard form, but this is faster.

Karnagh Maps: Mapping S-SOP expressions

S-SOP to K-map exercise:

AB \ CD	00	01	11	10
00				
01				
11				
10				

Table 6: Map the S-SOP expression below into the K-Map.

$\overline{A}\ \overline{B}\ \overline{C}\ \overline{D} + ABC$

Karnagh Maps: Mapping S-SOP expressions

S-SOP to K-map exercise:

AB \ CD	00	01	11	10
00				
01				
11				
10				

Table 7: Map the S-SOP expression below into the K-Map.

$\overline{A}\ \overline{B}\ \overline{C}\ \overline{D} + ABCD + \overline{A}\ \overline{B}\ C\ D$

Applied K-Maps: Logic Simplification

Applied K-Maps: Logic Simplification

The expression $\overline{A}\ \overline{B}\ \overline{C}\ D + \overline{A}\ B\ \overline{C}\ D + A\ B\ \overline{C}\ D + A\ \overline{B}\ \overline{C}\ D$ probably has a simpler form. How can we use the K-map to simplify?

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1. *Group the 1's in adjacent cells*
   - Group size must be equal to a power of 2
   - Groups must be as large as possible
2. *Read simplified terms from map*
   - One SOP term per group. **Exclude** contradictory variables.
   - **3-variable maps**: 1-cell groups have 3-variable products, 2-cell groups with 2-variable products, 4-cell groups with 1-variable products.
   - **4-variable maps**: 1-cell groups have 4-variable products, 2-cell groups with 3-variable products, 4-cell groups with 2-variable products, 8-cell groups with 1-variable products.

Applied K-Maps: Logic Simplification

K-map to simplified SOP (*work several examples*):

AB \ CD	00	01	11	10
00				
01				
11				
10				

Table 8: Place 1's in the K-map to find the corresponding SOP expression.

Applied K-Maps: Logic Simplification

K-map to simplified SOP (*use wrap-around adjacency*):

AB \ CD	00	01	11	10
00				
01				
11				
10				

Table 9: Place 1's in the K-map to find the corresponding SOP expression.

Applied K-Maps: Logic Simplification

Simplify: $\overline{B}\ \overline{C}\ \overline{D} + \overline{A}\ B\ \overline{C}\ \overline{D} + A\ B\ \overline{C}\ \overline{D} + \overline{A}\ \overline{B}\ C\ D + A\ \overline{B}\ C\ D + \overline{A}\ \overline{B}\ C\ \overline{D} + \overline{A}\ B\ C\ \overline{D} + A\ B\ C\ \overline{D} + A\ \overline{B}\ C\ \overline{D}$

AB \ CD	00	01	11	10
00				
01				
11				
10				

Table 10: Place 1's in the K-map to find the corresponding SOP expression. *The final expression has only two terms. Build the truth table from the final expression, and check against original expression.*

Applied K-Maps: Logic Simplification

TT to minimal SOP *(work several examples).*

A	B	C	D	X
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

AB \ CD	00	01	11	10
00				
01				
11				
10				

Table 11: The minimal SOP may be derived from a TT via the K-map.

Applied K-Maps: Logic Simplification

TT to minimal SOP *(utilize **don't care** conditions).*

A	B	C	D	X
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

AB \ CD	00	01	11	10
00				
01				
11				
10				

Table 12: The minimal SOP may be derived from a TT via the K-map.

Combinatorial Logic and Dual Logic Symbols

Combinatorial Logic and Dual Logic Symbols

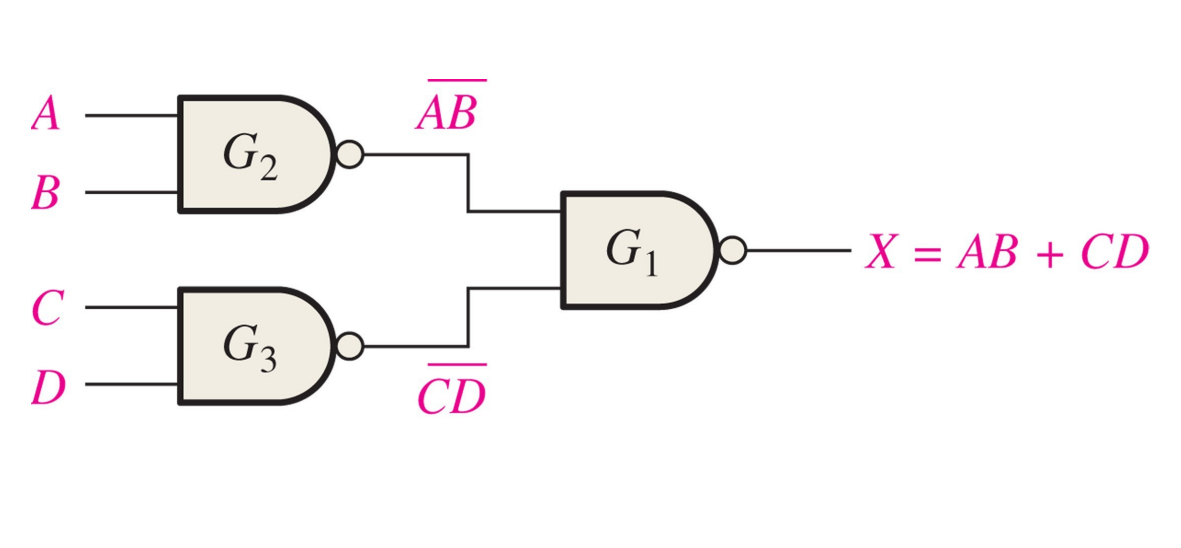


Figure 1: An example of a combinatorical logic circuit involving inverters. What if we arranged the circuit without single inverters?

Hint: move the last bubble backwards one step.

Combinatorial Logic and Dual Logic Symbols

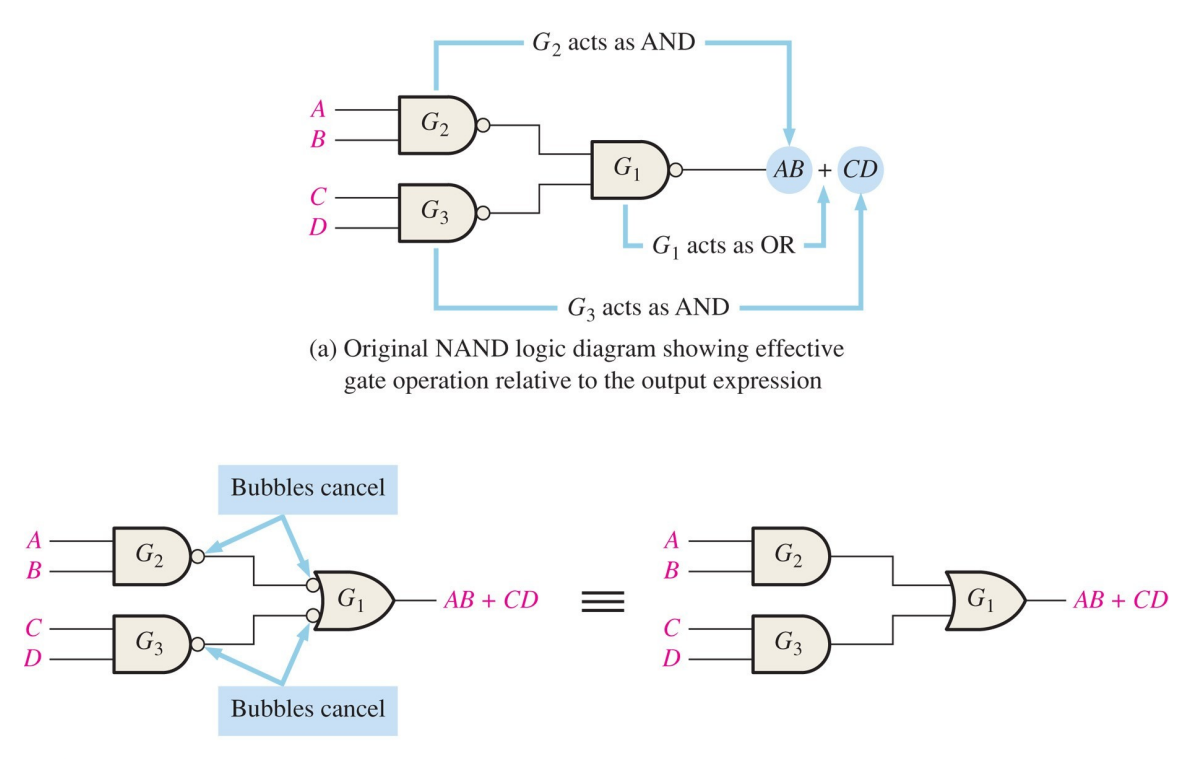
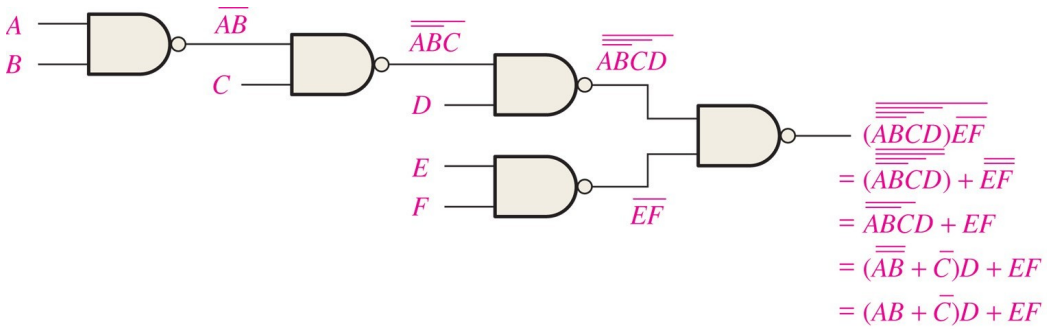
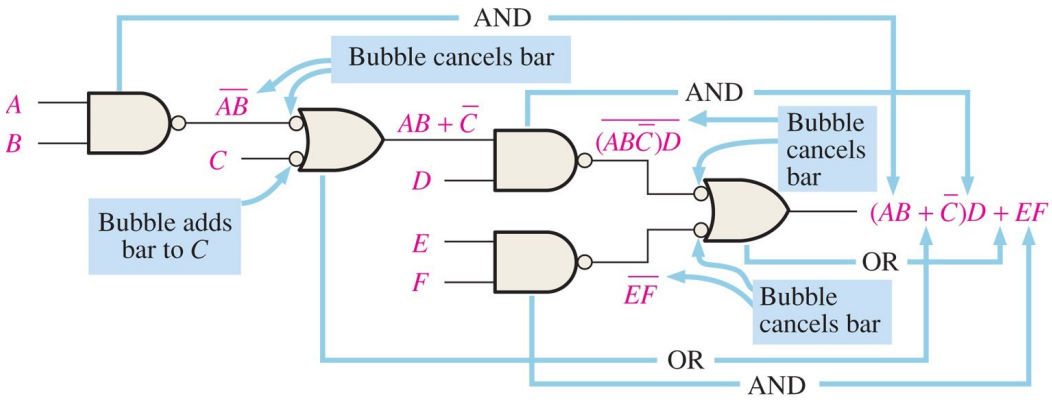


Figure 2: The solution to Fig. 1.

Combinatorial Logic and Dual Logic Symbols



(a) Several Boolean steps are required to arrive at final output expression.



(b) Output expression can be obtained directly from the function of each gate symbol in the diagram.

Figure 3: Notice how the active LOW states mid-circuit are simplifying the interpretation of the circuit.

Combinatorial Logic and Dual Logic Symbols

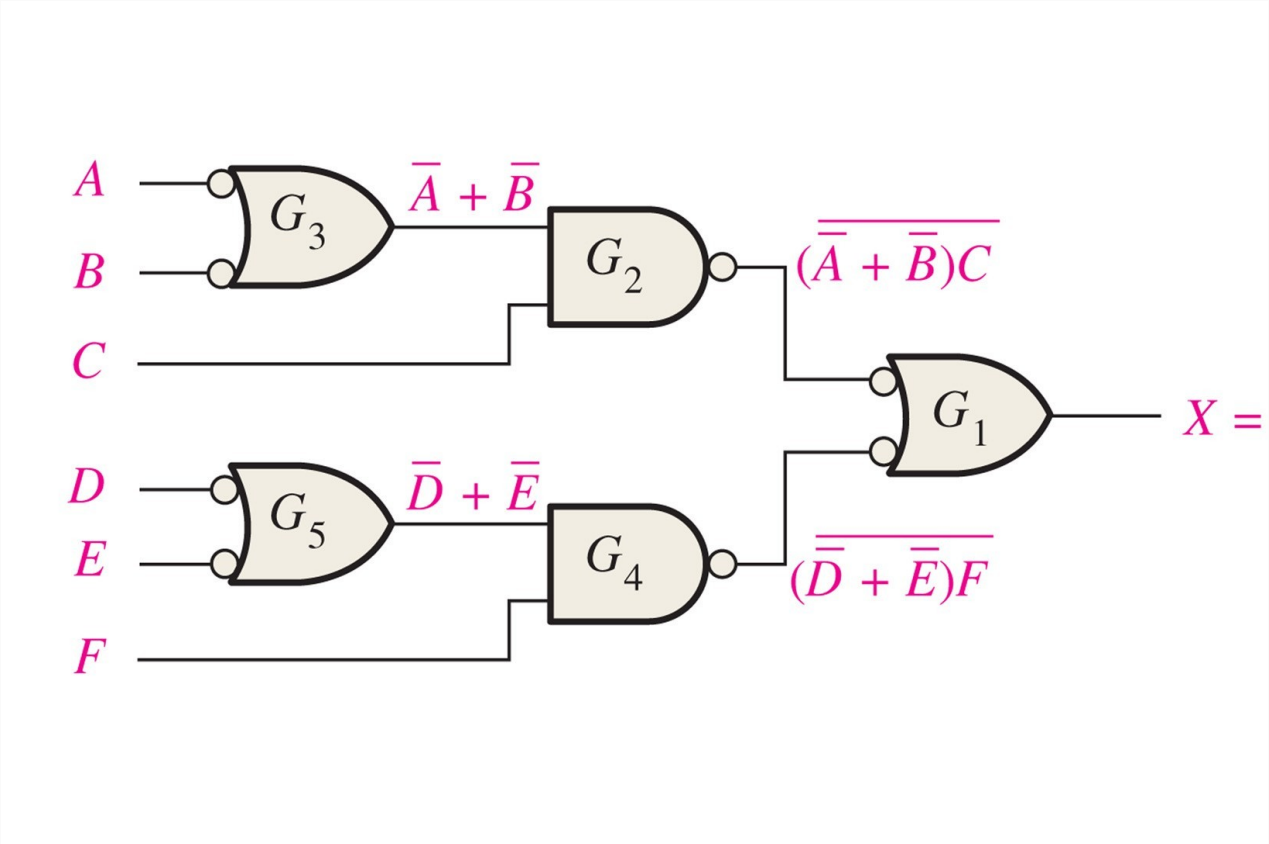


Figure 4: Solve for X.

Combinatorial Logic and Dual Logic Symbols

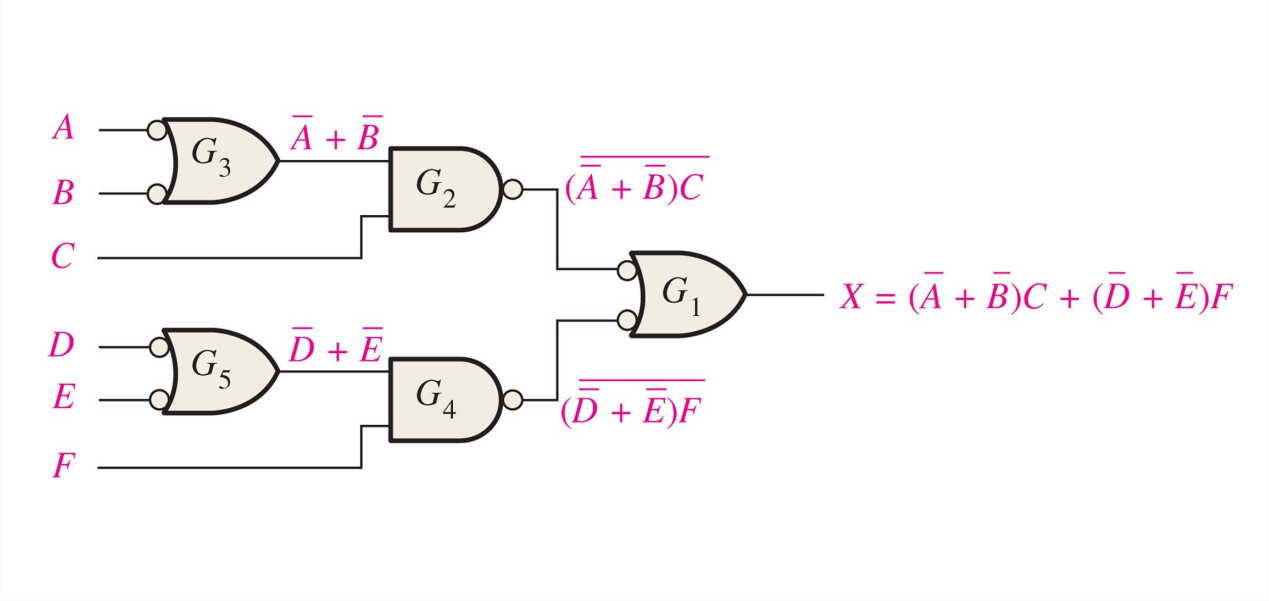


Figure 5: Answer for Fig. 4.

Conclusion

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