CARLOS MARTIN

Study Guide for Midterm 1

Dr. Jordan Hanson - Whittier College Dept. of Physics and Astronomy

March 24, 2020

1 Chapter 1 - Introductory Concepts

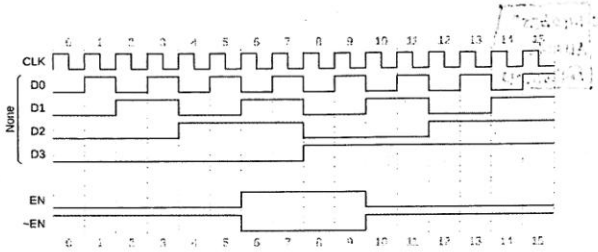


Figure 1: A timing diagram including a clock signal (CLK), a 4-bit parallel data stream (D0-D3), and enable/disable signals (EN/∼EN).

1. Consider Fig. 1. (a) What is the duty cycle of each D_i signal? (b) Consider the bitstreams of D_i. What does the sequence of numbers represent?

1a.) D_0 DUTY CYCLE $\left(\frac{T_{on}}{T}\right)\times 100\% = \left(\frac{1}{2}\right)\times 100\% =$ 50%, SIMILARLY $D_1 = \frac{2}{4}\times 100\% =$ 50%, $D_2 = \frac{4}{8}\times 100\% =$ 50%, $D_3 = \frac{8}{16}\times 100\% =$ 50%

1b.) D_0 = 0101010101010101 , D_1 = 0011001100110011 , D_2 = 0000111100001111 , D_3 = 0000000011111111

2. (a) Imagine that D_i signals enter a NAND gate. along with the ∼EN signal. Draw the resulting timing diagram.

NAND = ONLY LOW AT 15.

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

3. Suppose D_i represents parallel data with a clock frequency of 4 MHz. (a) What is the total bitrate (bits per second)? (b) What would be the bit rate if the system was serial instead of parallel?

3a.) $\frac{1}{4MHz} = .25\mu s$, EACH LINE IS 16 BITS SO $16\times 4 = 64$ BITS. $\frac{64}{(.25)(16)} = \frac{16\text{ BITS}}{\mu s}\times\frac{1\times 10^6\,\mu s}{s} =$ 16 MEGABITS PER SECOND

3b.) 4x LONGER SO $\frac{64\text{ BITS}}{16\,\mu s} = \frac{4\text{ BITS}}{\mu s}\times\frac{1\times 10^6\,\mu s}{s} =$ 4 MEGABITS PER SECOND.

2 Chapter 2 - Number Systems, Operations, and Codes

1. Convert to binary: (a) 1024 (decimal) (b) 0xBBBB (hex) (c) -2048 (decimal).

a.) 1024 IS 2^{10} IN BIN SO 10000000000

b) WE CAN WRITE BBBB AS ONE B 4 TIMES SO 1011 1011 1011 1011

c) WE WRITE 2048 IN BIN FIRST SO 100000000000 → TAKE COMP AND ADD ONE GETS US 100000000000

2. Convert to hex: (a) 65535 (decimal) (b) 1000100010001000 (binary)

a.) 16^3 BIGGEST POWER $16^3\ 16^2\ 16^1\ 16^0$ 15 15 15 15 $= 16^3(15) + 16^2(15) + 16^1(15) + 15 = 65535$ SO FFFF

b.) 1000 1000 1000 1000 (8 8 8 8) = 8888

3. Convert to *octal*, in which the base is 8: 1024 (decimal).

1024 = 10 000 000 000 IN BINARY

2 0 0 0 = 2000

CHUNKS OF 3 FOR OCTAL.

4. Consider the gray code angular encoder in Fig. 2. (a) If the shaft rotates 180 degrees, how many bit changes occur? (b) If it rotates 180 degrees, and the initial gray code is 0000, what is the final gray code? (c) With 4-bit gray code, how many distinct angles can the shaft encode? What is 360 degrees divided by this number (i.e. the angular precision)? (d) What would be the angular precision of an 8 bit encoder?

a.) $16/2 =$ 8 TOTAL BIT CHANGES

b.) 1100

c.) 2^4 OPTIONS = 16 ANGLES so $\frac{360^\circ}{16} =$ 22.5° ANGLE PRECISION

D.) $2^8 = 256$ so $\frac{360^\circ}{256} =$ 1.40625° ANGLE PRECISION

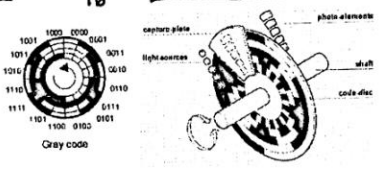


Figure 2: A gray code shaft encoder, or angular encoder, reports the angular position of an object digitally, using the gray code.

3 Chapter 3 - Logic Gates

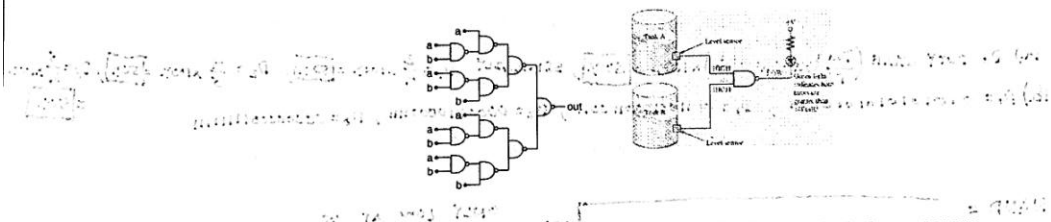
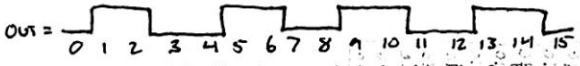


Figure 3: (Left) A logic gate combination. (Right) A liquid tank-level system built from a NAND gate.

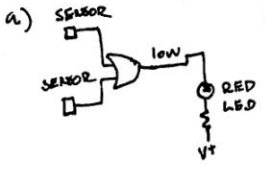
1. Generate the simplified logic expression and truth table for Fig. 3, left. What do you call this type of gate?

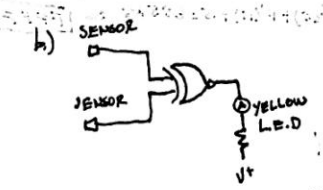
ATTACHMENT FOR LOGIC EXPRESSION. IT IS $\bar{B}A + \bar{A}B$ SO ITS AN XOR GATE.

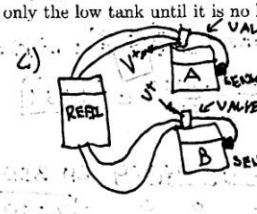
2. Suppose signals D_0 and D_1 in Fig. 1 are connected to a and b in Fig. 3, left. Generate the timing diagram for *out*.



3. **Creative design**: A liquid tank system is depicted in Fig. 3. The sensors are HIGH when the liquid is above the level (green ON). (a) Create a red LED system that activates when both tanks are *below* the level, and draw it below. (b) Create a yellow LED system that activates when one tank is below and one tank is above the level. (c) Add a third tank with more liquid, and two pipes guiding liquid to tank A and B. Each pipe should have a valve. Add logic that opens the correct valve so as to fill only the low tank until it is no longer below the level.







WHEN THERE IS A VOLTAGE DIFF, THE VALVE WILL OPEN, AS SOON ASS THE TANK IS FILLED IT WILL PRODUCE A HIGH AND THE VALVE WILL SHUT.

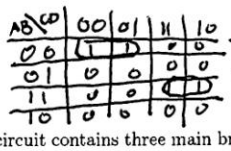
4 Chapter 4 - Boolean Algebra and Logic Simplification

1. Suppose an investment firm holds stock shares in four different stocks within a portfolio, labled A through D. The companies corresponding to stocks A through D are labeled *inactive* or *active* by the firm, based on information about their productivity. The firm notices that the portfolio output is *on* (rising) under the following conditions:

   - All four companies are inactive. or ...
   - Companies A through C are inactive, while company D is active, or ...
   - All companies are active, or ...
   - Companies A through C are active, while company D is inactive.

   (a) Develop a S-SOP expression for X, the portfolio's state (on or off) based on the data above. (b) Use a domain-4 Karnaugh map to simplify the S-SOP expression. (c) Which stock appears to be irrelevant to the state of the portfolio?

   a.) $\bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C}D + ABCD + ABC\bar{D}$

   B) 

   → $\bar{A}\bar{B}A\bar{B}\bar{C}\bar{D}\bar{C}D = \bar{A}\bar{B}\bar{C}$

   → $AB\,ABCD\bar{C}\bar{D} = ABC$

   so SIMPLIFIED S-SOP IS $\bar{A}\bar{B}\bar{C} + ABC$

   C) D IS IRRELEVANT.

2. A circuit contains three main branches leading to one output. The output is observed to fail under the following conditions below. (a) Use the domain-3 Karnaugh map to determine the conditions under which it does succeed, and write an S-SOP expression for the circuit. (b) Draw the circuit using gates.

   - A: false, B: false, C: false
   - A: false, B: true, C: false
   - A: true, B: true, C: false
   - A: true, B: false, C: false
   - A: false, B: true, C: true
   - A: true, B: true, C: true

   a)

AB\C	0	1
00	1	0
01	1	1
11	1	1
10	1	0

   SUCCEEDS WHEN:

   ① A FAILS, B FAILS, C SUCCEEDS

   ② A SUCCEEDS, B FAILS, C SUCCEEDS.

   S-SOP = $\bar{A}\bar{B}C + A\bar{B}\bar{C}$

   b) IS ON ATTACHMENT.

5 Chapter 5 - Combinatorial Logic Analysis

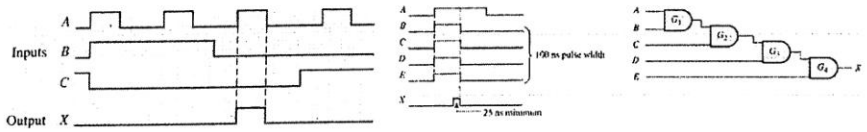


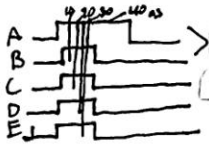
Figure 4: Diagrams for Sec. 5. (Left) Inputs are ABC. and the output is X. (Right) The inputs are ABCDE. and the output is X.

1. For the input waveforms shown in Fig. 4 (left), what logic circuit will generate the output waveform?

2. **Bonus**: Assumming a propagation delay of 10 ns through each gate in Fig. 4, determine if the *desired* output waveform X will be generated. The desired output is a pulse with a minimum width of 25 ns.

IF EACH "AND" TERM TAKES 10 ns, THE MINIMUM PULSE WIDTH IS 60ns > 25 ns SO THE DESIRED OUTPUT WONT BE GENERATED.

EX:



AB TAKES 10 ns THEN ABC TAKES 10 ns, THEN ABCD TAKES 10 ns, THEN ABCDE TAKES 10 ns, ADDED THATS 40 ns AND THE PULSE WIDTH IS 100 ns SO 100 − 40 ns = 60 ns > 25 ns.

POPULAR
INVESTMENTS

CHAPTER 3 #1 ATTACHMENT

$$\overline{((\overline{AB})A)((\overline{AB})B)}\,\overline{((\overline{AB})A)((\overline{AB})B)}$$

$$= \overline{((\overline{AB})A)} + \overline{((\overline{AB})B)} + \overline{((\overline{AB})A)} + \overline{((\overline{AB})B)}$$

$$= \overline{((\bar{A}+\bar{B})A)} + \overline{((\bar{A}+\bar{B})B)} + \overline{((\bar{A}+\bar{B})A)} + \overline{((\bar{A}+\bar{B})B)}$$

$$= \overline{(\bar{A}+\bar{B})+\bar{A}} + \overline{(\bar{A}+\bar{B})+\bar{B}} + \overline{(\bar{A}+\bar{B})+\bar{A}} + \overline{(\bar{A}+\bar{B})+\bar{B}}$$

$$= \overline{(AB)+\bar{A}} + \overline{(AB)+\bar{B}} + \overline{(AB)+\bar{A}} + \overline{(AB)+\bar{B}}$$

$$= (\overline{AB})A + (\overline{AB})B + (\overline{AB})A + (\overline{AB})B$$

$$= (\bar{A}+\bar{B})A + (\bar{A}+\bar{B})B$$

$$= \boxed{\bar{B}A + \bar{A}B} \quad \text{WHICH IS AN X-OR}$$

CHAPTER 4 #2b ATTACHMENT