# Synopsis - Week 7 Integrated Project: fixed IC gates and counters, gates and counters in programmable logic

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## 1 Finite Impulse Response (FIR) Filter

A finite impulse response (FIR) filter takes digitized data as the input, and returns modified data of the same shape as the output. Let $n$ represent the number of samples of digitized data. Let $x[n]$ represent the vector of digitized input data, and $y[n]$ represent the digitized output data. Let $z^{-1}$ represent an operation that selects the prior sample, or the $n-1$ sample relative to sample $n$. Let the coefficients $b_n$ multiply the samples $x[n]$ as they pass through an amplifier. Finally, let $\Sigma$ represent an adder that sums to inputs and produces one output. A generalized circuit diagram for the FIR filter is shown in Fig. 1, and the formula relating the input to the output is given in Eq. **??**.

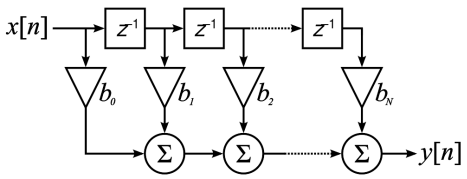


Figure 1: A generalized circuit diagram for the FIR filter.

$$y[n] = \sum_{i=0}^{N} b_i x[n-i] \tag{1}$$

In this lab, we are going to create a PYNQ overlay that will implement Eq. 1 in the SoC PL layer.

## 2 Comparing fixed IC gates and counters to programmable logic

1. Things