Tuesday Reading Assessment: Chapters 3, 4-1 and 4-2

Prof. Jordan C. Hanson

February 13, 2024

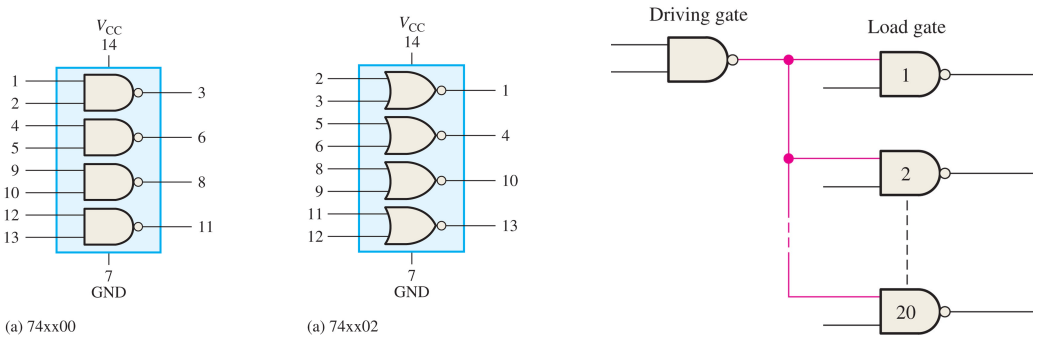

Figure 1: (Left) A 74xx00 gate, a quad NAND package IC. (Middle) A 74xx02 gate, a quad NOR package IC.

1 Logic Gates and Logic Functions

1. Figure 1 (left) contains a diagram of a quad-NAND IC package, the 74xx00 class. (a) Create and draw a system of NAND gates that is equivalent to a 2-input AND gate. (b) Determine a system of connections of outputs to inputs for the 74xx00 IC that will yield one AND gate. (c) Do the same for an OR gate.

2. Repeat the previous exercise with the 74xx02 in Fig. 1 (middle), a quad-NOR gate.

2 Electrical Characteristics

1. Suppose for all individual gates in Fig. 1 the $I_{\mathrm{CCH}} = 10\ \mu\mathrm{A}$, $I_{\mathrm{CCL}} = 100\ \mu\mathrm{A}$, and $V_{\mathrm{CC}} = 5$ V. (a) What is the power dissipation of your AND gate made from NAND gates? *Hint:* $P_{\mathrm{D}} = V_{\mathrm{CC}}(I_{\mathrm{CCH}} + I_{\mathrm{CCL}})/2$. (b) If the *propagation delay time* t_{P} is 5 ns per NAND gate, what is the **speed power product**, $P_{\mathrm{D}}t_{\mathrm{P}}$, for the AND gate in pJ? (c) What is the *fan-out* of your AND and OR gate designs from NANDs? That is, how many gates are driven by the output current of a single gate (see Fig. 1 (right)).