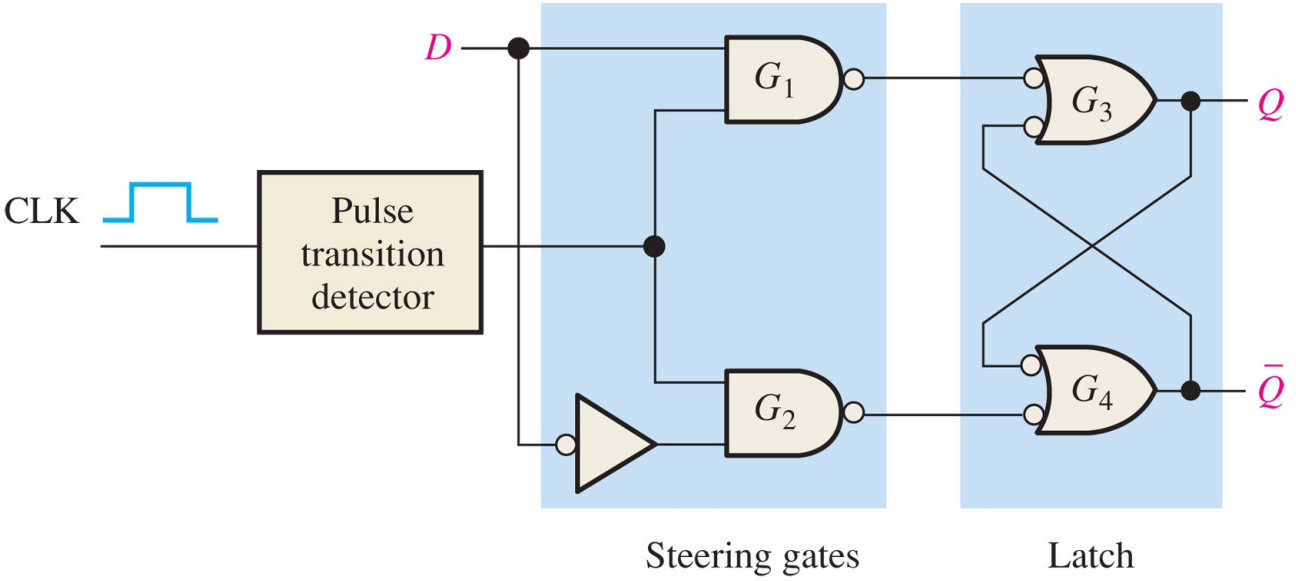
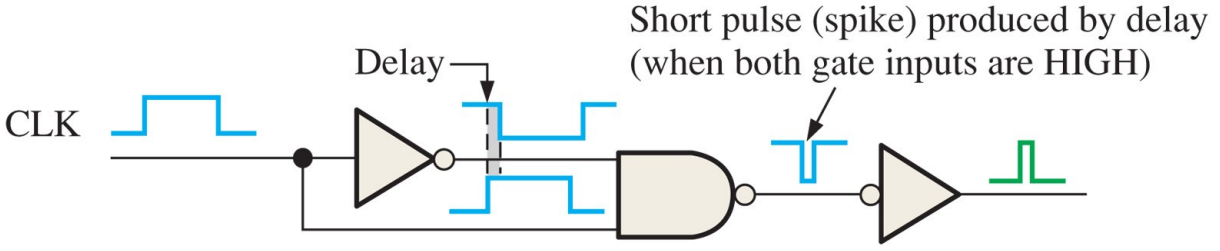


(a) A simplified logic diagram for a positive edge-triggered D flip-flop



(b) A type of pulse transition detector

A D Flip-flop with positive edge triggering.

- The pulse transition detector is responsible for the positive edge trigger
- CLK pulse passes through inverter with intrinsic delay, and another wire
- Both fed into effective AND gate, producing narrow pulse centered on CLK rising edge