Section 1

① (A) n (delay of in to out)

4 (8 ns)

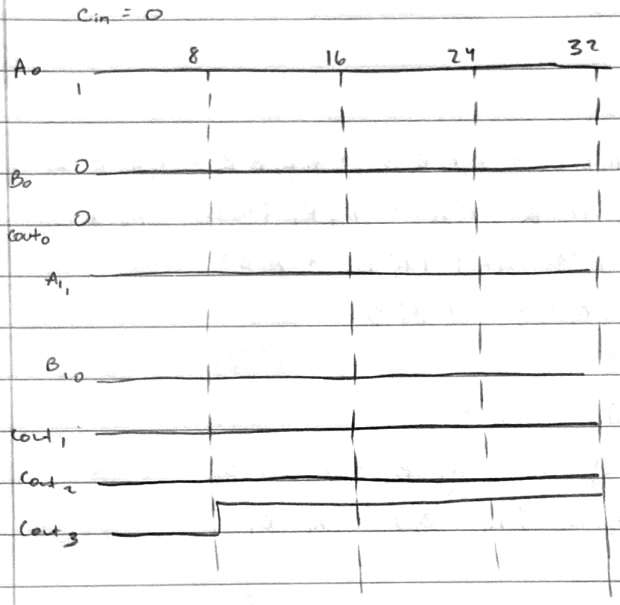
32 ns => $f_{max} = \frac{1}{32ns} = 31.25$ MHz

(B) a w/ 8 bit extended

8 (8ns)

64 ns => $f_{max} = \frac{1}{64ns} = 15.62$ MHz

(C) Timing Diagram

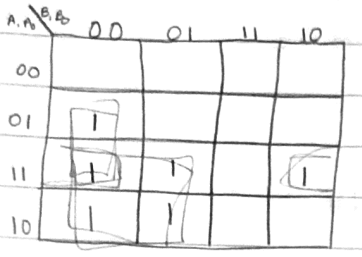


② For 2-bit:

A A_1 A_0	B B_1 B_0	A > B	A = B	A < B
0 0	0 0	0	1	0
0 0	0 1	0	0	1
0 0	1 0	0	0	1
0 0	1 1	0	0	1
0 1	0 0	1	0	0
0 1	0 1	0	1	0
0 1	1 0	0	0	1
0 1	1 1	0	0	1
1 0	0 0	1	0	0
1 0	0 1	1	0	0
1 0	1 0	0	1	0
1 0	1 1	0	0	1
1 1	0 0	1	0	0
1 1	0 1	1	0	0
1 1	1 0	1	0	0
1 1	1 1	0	1	0

For $A > B$

$f(A, B) = \Sigma(4, 8, 9, 12, 13, 14)$

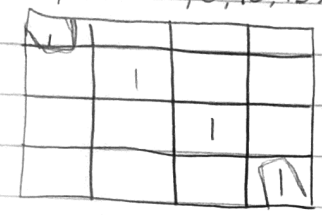


$A_0 B_1' B_0' + A_1 B_1' + A_1 A_0 B_0'$

$A_0 B_0' (A_0 + A_1) + A_1 B_1'$

For $A = B$

$f(A, B) = \Sigma(0, 5, 10, 15)$



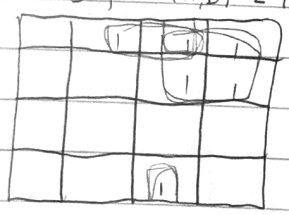
$A_1' A_0' B_1' B_0' + A_1' A_0 B_1' B_0 + A_1 A_0 B_1 B_0 + A_1 A_0' B_1 B_0'$

$A_1' B_1' (A_0' B_0' + A_0 B_0) + A_1 B_1 (A_0 B_0 + A_0' B_0')$

$(A_0' B_0' + A_0 B_0)(A_1' B_1' + A_1 B_1)$

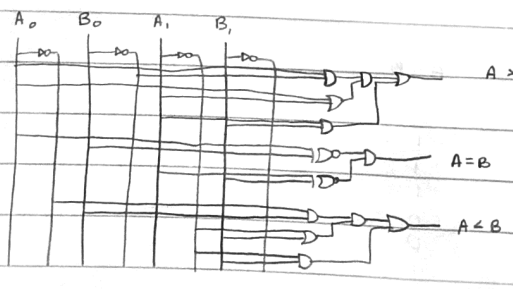
$(A_0 \odot B_0)' + (A_1 \odot B_1)'$

For $A < B$, $f(A, B) \Sigma(1, 2, 3, 6, 7, 11)$



$A_1' A_0' B_0 + A_1' B_1 + A_0' B_1 B_0$

$A_0' B_0 (A_1' + B_1) + A_1' B_1$

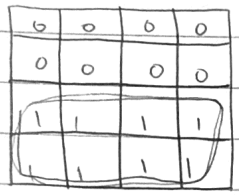


Section 1

③ Gray code input — Binary code output

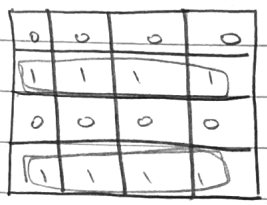
G_3	G_2	G_1	G_0	B_3	B_2	B_1	B_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
1	0	0	0	1	1	1	1
1	0	0	1	1	1	1	0
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	0	1	0	1	1
1	1	1	1	1	0	1	0

For B3



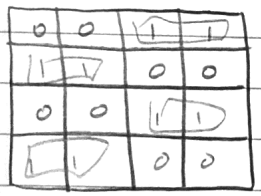
$B_3 = G_3$

For B_2



$B_2 = G_3 \oplus G_2$

For B_1



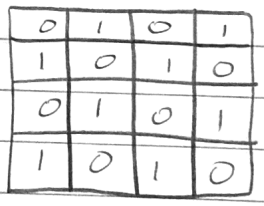
$G_1 G_2' G_3' + G_3 G_2 G_1' + G_3 G_2 G_1 + G_3 G_2' G_1'$

$G_1 G_2' G_3' + G_1 G_2 G_3 + G_1' G_2 G_3' + G_1' G_2' G_3$

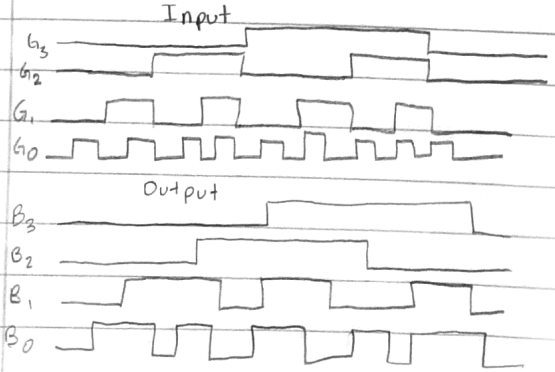
$G_1 (G_2' G_3' + G_2 G_3) + G_1' (G_2 G_3' + G_2 G_3')$

$G_1 (G_1' \oplus G_3') + G_1' (G_2 \oplus G_3) = B_1$

For B_0



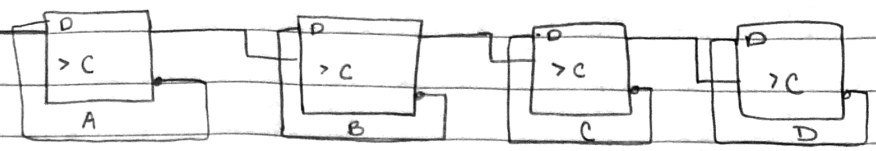
$B_0 = G_0 \oplus G_1 \oplus G_2 \oplus G_3$



Bidirectional register

Section 2

① 1) Ⓐ CLK



Section 3

①

CLK	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	S_1	S_0
0	1	0	0	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	1	0
2	0	0	1	0	0	0	0	0	1	0
3	0	0	0	1	0	0	0	0	1	0
4	0	0	0	0	1	0	0	0	1	0
5	0	0	0	0	0	1	0	0	1	0
6	0	0	0	0	0	0	1	0	1	0
7	0	0	0	0	0	0	0	1	1	0
8	0	0	0	0	0	0	0	1	0	1
9	0	0	0	0	0	0	1	0	0	1
10	0	0	0	0	0	1	0	0	0	1
11	0	0	0	0	1	0	0	0	0	1
12	0	0	0	1	0	0	0	0	0	1
13	0	0	1	0	0	0	0	0	0	1
14	0	1	0	0	0	0	0	0	0	1
15	1	0	0	0	0	0	0	0	0	1

The circuit has 8 outputs therefore it requires 8 flip flops