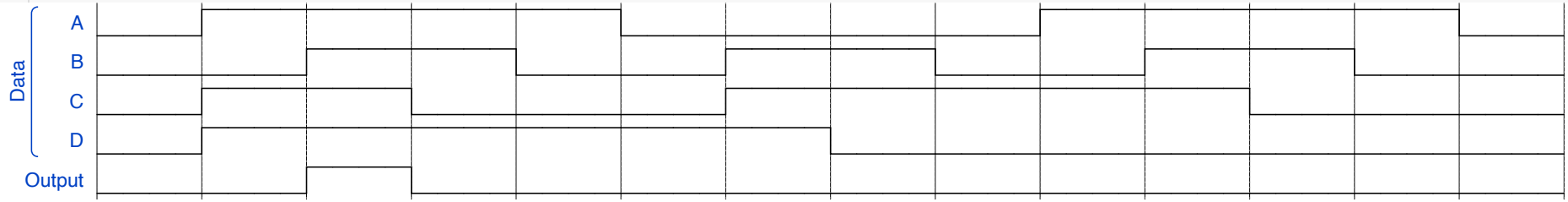
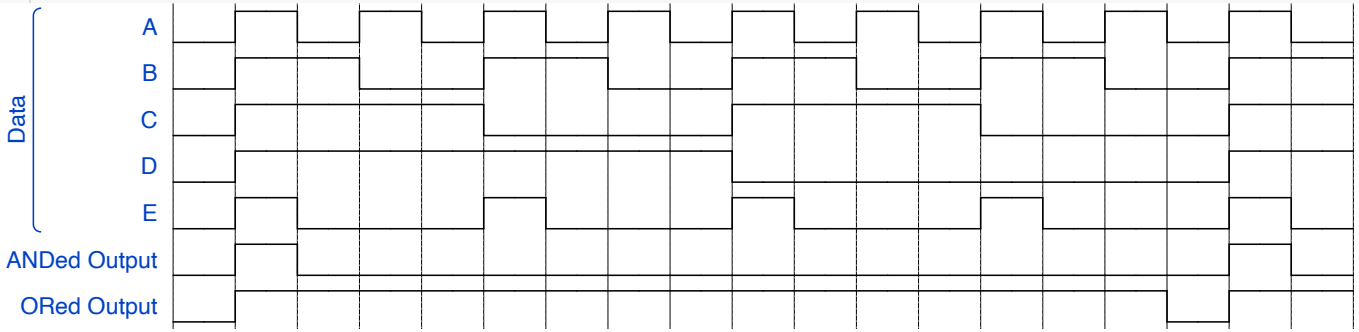
```
{ "signal" : [
  ["Data",
  { "name": "A",               "wave": "lh...l...h...l" },
  { "name": "B",            "wave": "l.h.l.h.l.h.l." },
  { "name": "C",         "wave": "lh.l..h....l.." },
  { "name": "D",     "wave": "lh.....l......" },
   ],
  { "name": "Output",   "wave": "l.hl.........." },
],
  "config" : { "hscale" : 2 }
}
```



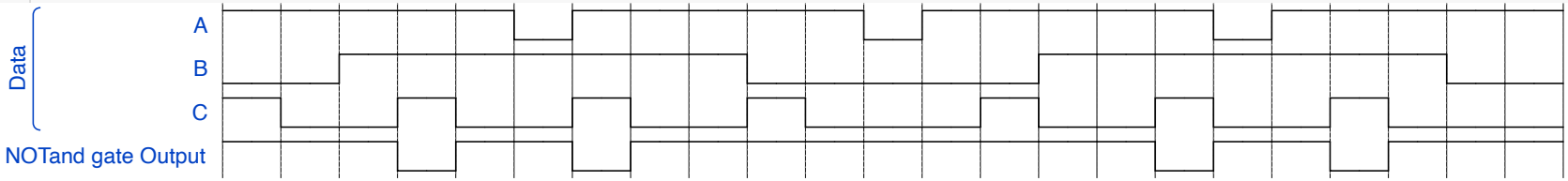
AND Truth Table

Inputs (A B C D)	AND Output (X)
000	0
001	0
010	0
011	0
100	0
101	0
110	0
111	0
1000	0
1001	0
1010	0
1011	0
1100	0
1101	0
1110	0
1111	1

```
{ "signal" : [
  ["Data",
   { "name": "A",               "wave": "lhlhlhlhlhlhlhlhlhl" },
   { "name": "B",            "wave": "lh.l.h.l.h.l.h.l.h." },
   { "name": "C",         "wave": "lh...l...h...l...h." },
   { "name": "D",     "wave": "lh.......l.......h." },
   { "name": "E",   "wave": "lhl..hl..hl..hl..hl" },
    ],
   { "name": "ANDed Output",    "wave": "lhl.............hl" },
    { "name": "ORed Output",    "wave": "lh.............lh." },
],
  "config" : { "hscale" : 1 }
}
```



```
{ "signal" : [
  ["Data",
  { "name": "A",               "wave": "h....lh....lh....lh...." },
  { "name": "B",           "wave": "l.h......l....h......l." },
  { "name": "C",        "wave": "hl.hl.hl.hl..hl.hl.hl.." },
   ],
  { "name": "NOTand gate Output",   "wave": "h..lh.lh........lh.lh.." },
],
  "config" : { "hscale" : 1 }
   }
```



NAND Truth Table

Inputs (A B C)	N And Output ("X")
000	1
001	1
010	1
011	1
100	1
101	1
110	1
111	0