Tuesday Reading Assessment: Chapters 6, 7

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1 Functions of Combinational Logic: Multiplexer

1. (a) Draw a diagram of the gate logic describing the 4-to-1 multiplexer, using basic AND, OR, and inverter gates. The design should include the correct number of data-select lines, four inputs, and one output. (b) Suppose that the data lines are called D_i, the data select lines are S_i, and the output line is D_{out}. If the S_i represent binary counting between 0-3, with 1 μs per clock step, how often can one send a bit of data to D_{out} using the D_0 line? (c) How long would it take to send four bits of data, one on each D_i?

2 Functions of Combinational Logic: Demultiplexer

1. (a) Draw a diagram of the gate logic describing the 1-to-4 demultiplexer, using basic AND, OR, and inverter gates. The design should include the correct number of data-select lines, one input, and four outputs. (b) Suppose that the data input line is called D_{in}, the data output lines are D_i the data select lines are S_i. The S_i represent binary counting between 0-3, with 1 μs per clock step. Create a timing diagram showing the behavior of D_{in}, S_i, and D_i.