

 This work is protected by
US copyright laws and is for
instructors' use only.

Online Instructor's Manual
for

Digital Fundamentals

Eleventh Edition

Thomas L. Floyd

PEARSON

Boston Columbus Indianapolis New York San Francisco Hoboken

Amsterdam Cape Town Dubai London Madrid Milan Munich Paris Montreal Toronto

Delhi Mexico City Sao Paulo Sydney Hong Kong Seoul Singapore Taipei Tokyo



This work is protected by United States copyright laws and is provided solely for the use of instructors in teaching their courses and assessing student learning. Dissemination or sale of any part of this work (including on the World Wide Web) will destroy the integrity of the work and is not permitted. The work and materials from it should never be made available to students except by instructors using the accompanying text in their classes. All recipients of this work are expected to abide by these restrictions and to honor the intended pedagogical purposes and the needs of other instructors who rely on these materials.

Copyright © 2015 Pearson Education, Inc., publishing as Prentice Hall, Hoboken, New Jersey and Columbus, Ohio. All rights reserved. Manufactured in the United States of America. This publication is protected by Copyright, and permission should be obtained from the publisher prior to any prohibited reproduction, storage in a retrieval system, or transmission in any form or by any means, electronic, mechanical, photocopying, recording, or likewise. To obtain permission(s) to use material from this work, please submit a written request to Pearson Education, Inc., Permissions Department, 221 River Street, Hoboken, New Jersey.

Many of the designations by manufacturers and seller to distinguish their products are claimed as trademarks. Where those designations appear in this book, and the publisher was aware of a trademark claim, the designations have been printed in initial caps or all caps.

10 9 8 7 6 5 4 3 2 1



ISBN-13: 978-0-13-273795-1
ISBN-10: 0-13-273795-7

CONTENTS

PART 1: PROBLEM SOLUTIONS	1
CHAPTER 1 Introductory Concepts.....	2
CHAPTER 2 Number Systems, Operations, and Codes	8
CHAPTER 3 Logic Gates	24
CHAPTER 4 Boolean Algebra and Logic Simplification.....	37
CHAPTER 5 Combinational Logic Analysis.....	66
CHAPTER 6 Functions of Combinational Logic.....	120
CHAPTER 7 Latches, Flip-Flops, and Timers	135
CHAPTER 8 Shift Registers	135
CHAPTER 9 Counters	152
CHAPTER 10 Programmable Logic	181
CHAPTER 11 Data Storage.....	190
CHAPTER 12 Signal Conversion and Processing	200
CHAPTER 13 Data Transmission.....	208
CHAPTER 14 Data Processing and Control.....	218
CHAPTER 15 Integrated Circuit Technologies.....	224
PART 2: APPLIED LOGIC SOLUTIONS	231
CHAPTER 4	232
CHAPTER 5	236
CHAPTER 6	239
CHAPTER 7	244
CHAPTER 8	247
CHAPTER 9	248
CHAPTER 10	249
PART 3: LABORATORY SOLUTIONS FOR <i>EXPERIMENTS IN DIGITAL FUNDAMENTALS</i> by David Buchla and Doug Joksch	251
PART 4: MULTISIM PROBLEM SOLUTIONS	303

PART 1

Problem Solutions

CHAPTER 1

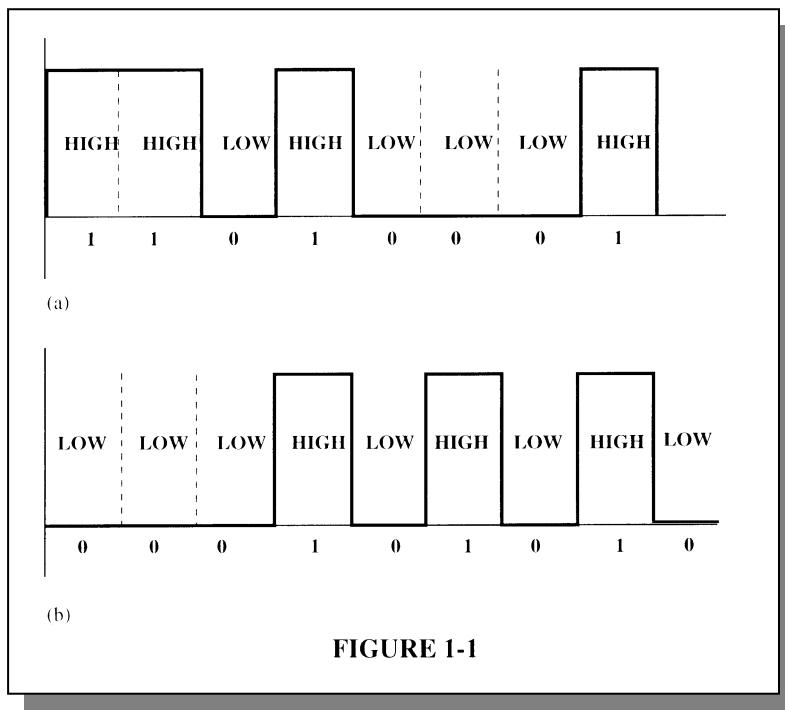
INTRODUCTORY CONCEPTS

Section 1-1 Digital and Analog Quantities

1. Digital data can be transmitted and stored more efficiently and reliably than analog data. Also, digital circuits are simpler to implement and there is a greater immunity to noisy environments.
2. Pressure is an analog quantity.
3. A clock, a thermometer, and a speedometer can have either an analog or a digital output.

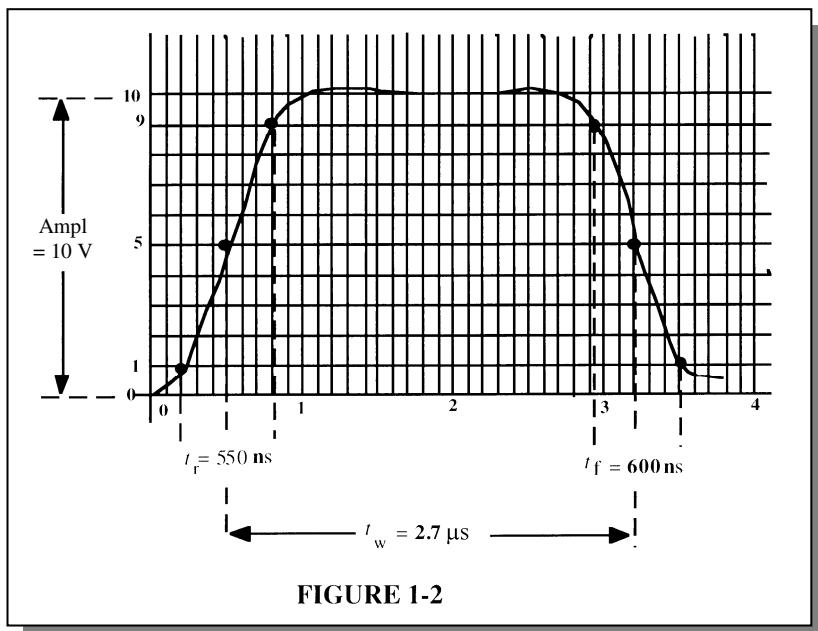
Section 1-2 Binary Digits, Logic Levels, and Digital Waveforms

4. In positive logic, a 1 is represented by a HIGH level and a 0 by a LOW level. In negative logic, a 1 is represented by a LOW level, and a 0 by a HIGH level.
5. HIGH = 1; LOW = 0. See Figure 1-1.

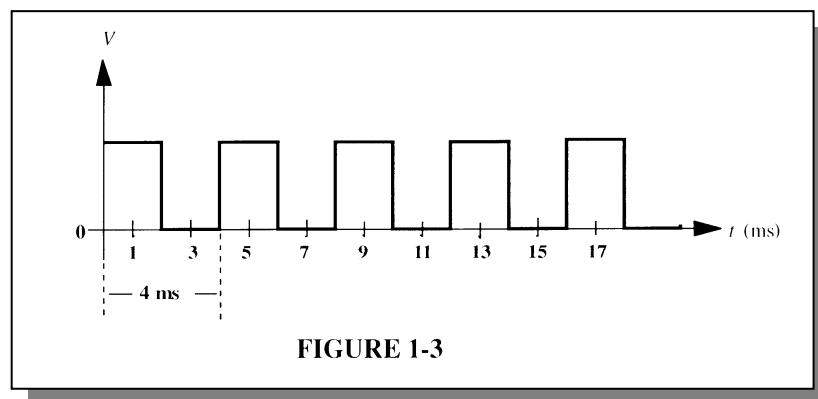


6. A 1 is a HIGH and a 0 is a LOW:
 - (a) HIGH, LOW, HIGH, HIGH, HIGH, LOW, HIGH
 - (b) HIGH, HIGH, HIGH, LOW, HIGH, LOW, LOW, HIGH

7. See Figure 1-2.



8. $T = 4 \text{ ms}$. See Figure 1-3.



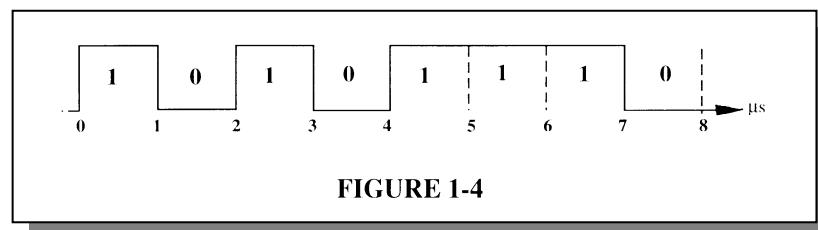
$$9. f = \frac{1}{T} = \frac{1}{4 \text{ ms}} = 0.25 \text{ kHz} = 250 \text{ Hz}$$

10. The waveform in Figure 1-61 is **periodic** because it repeats at a fixed interval.

11. $t_w = 2 \text{ ms}; T = 4 \text{ ms}$

$$\% \text{ duty cycle} = \left(\frac{t_w}{T} \right) 100 = \left(\frac{2 \text{ ms}}{4 \text{ ms}} \right) 100 = 50\%$$

12. See Figure 1-4.



Chapter 1

13. Each bit time = 1 μ s

$$\text{Serial transfer time} = (8 \text{ bits})(1 \mu\text{s}/\text{bit}) = 8 \mu\text{s}$$

Parallel transfer time = 1 bit time = 1 μ s

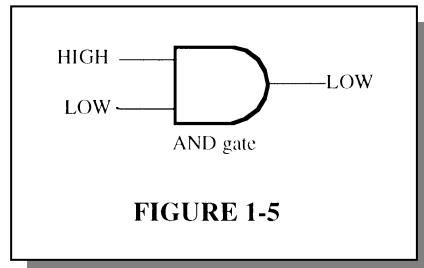
14. $T = \frac{1}{f} = \frac{1}{3.5 \text{ GHz}} = 0.286 \text{ ns}$

Section 1-3 Basic Logic Functions

15. $L_{\text{ON}} = \text{SW1} + \text{SW2} + \text{SW1} \cdot \text{SW2}$

16. An AND gate produces a HIGH output only when *all* of its inputs are HIGH.

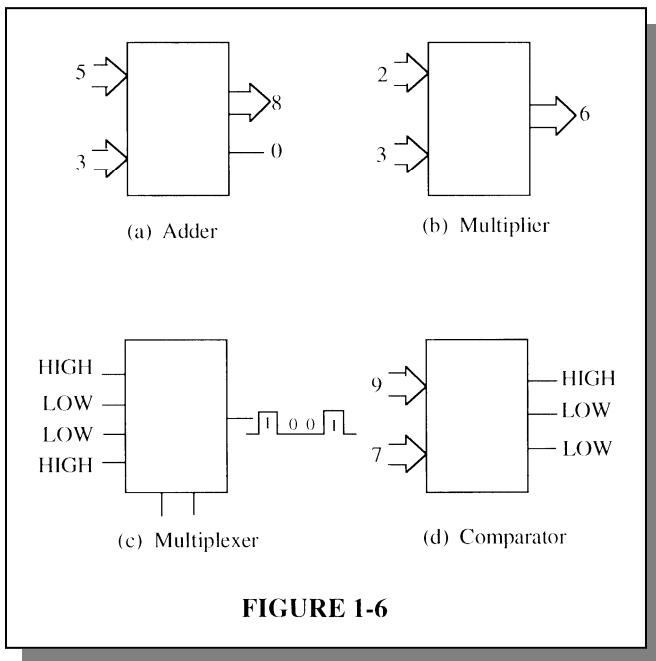
17. AND gate. See Figure 1-5.



18. An OR gate produces a HIGH output when *either or both* inputs are HIGH. An exclusive-OR gate produces a HIGH if one input is HIGH and the other LOW.

Section 1-4 Combinational and Sequential Logic Functions

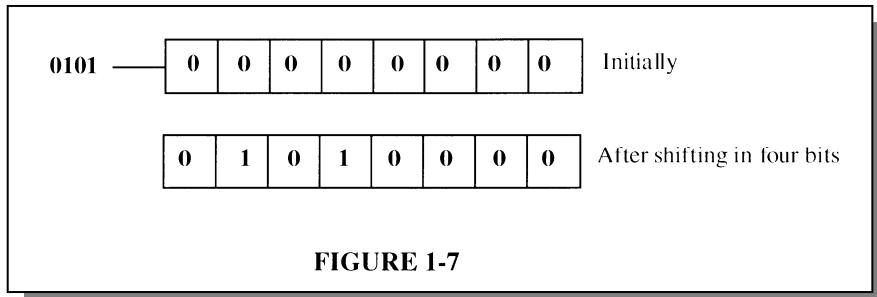
19. See Figure 1-6.



20. $T = \frac{1}{10 \text{ kHz}} = 100 \mu\text{s}$

$$\text{Pulses counted} = \frac{100 \text{ ms}}{100 \mu\text{s}} = 1000$$

21. See Figure 1-7.



Section 1-5 Introduction to Programmable Logic

22. The following do not describe PLDs: VHDL, AHDL
23. (a) SPLD: Simple Programmable Logic Device
 (b) CPLD: Complex Programmable Logic Device
 (c) HDL: Hardware Description Language
 (d) FPGA: Field-Programmable Gate Array
 (e) GAL: Generic Array Logic
24. (a) Design entry: The step in a programmable logic design flow where a description of the circuit is entered in either schematic (graphic) form or in text form using an HDL.
 (b) Simulation: The step in a design flow where the entered design is simulated based on defined input waveforms.
 (c) Compilation: A program process that controls the design flow process and translates a design source code to object code for testing and downloading.
 (d) Download: The process in which the design is transferred from software to hardware.
25. Place-and-route or fitting is the process where the logic structures described by the netlist are mapped into the actual structure of the specific target device. This results in an output called a bitstream.

Section 1-6 Fixed-Function Logic Devices

26. Circuits with complexities of from 100 to 10,000 equivalent gates are classified as large scale integration (LSI).
27. The pins of an SMT are soldered to the pads on the surface of a pc board, whereas the pins of a DIP feed through and are soldered to the opposite side. Pin spacing on SMTs is less than on DIPs and therefore SMT packages are physically smaller and require less surface area on a pc board.

Chapter 1

- 28.** See Figure 1-8.

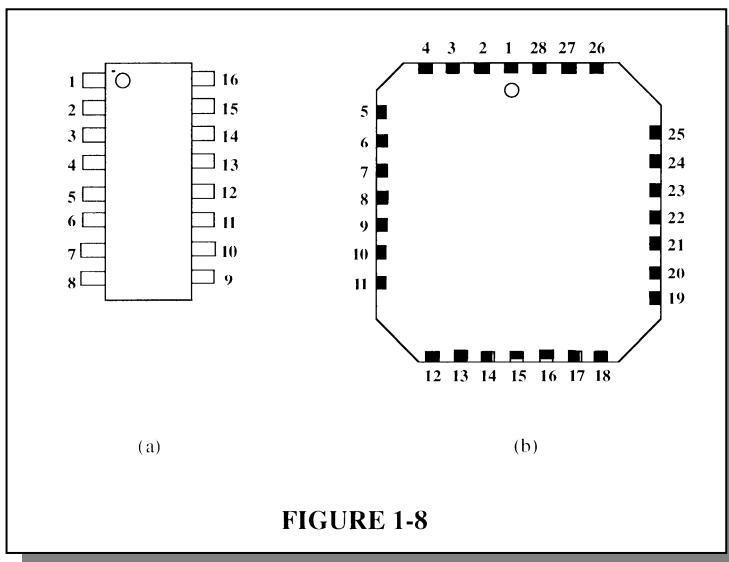


FIGURE 1-8

Section 1-7 Test and Measurement Instruments

- 29.** Amplitude = top of pulse minus base line

$$V = 8 \text{ V} - 1 \text{ V} = 7 \text{ V}$$

- 30.** Amplitude = (3 div)(2 V /div) = **6 V**.

- 31.** $T = (4 \text{ div})(2 \text{ ms/div}) = 8 \text{ ms}$

$$f = \frac{1}{T} = \frac{1}{8 \text{ ms}} = \mathbf{125 \text{ Hz}}$$

- 32.** Record length = (Acquisition time)(sample rate) = (2 ms) 12 Msamples/s = **24 ksamples**

Section 1-8 Introduction to Trouble Shooting

- 33.** Troubleshooting is the process of recognizing, isolating, and correcting a fault or failure in a system.
- 34.** In the half-splitting method, a point half way between the input and output is checked for the presence or absence of a signal.
- 35.** In the signal-tracing method, a signal is tracked as it progresses through a system until a point is found where the signal disappears or is incorrect.
- 36.** In signal substitution, a generated signal replaces the normal input signal of a system or portion of a system. In signal injection a generated signal is injected into the system at a point where the normal signal has been determined to be faulty or missing.
- 37.** When a failure is reported, determine when and how it failed and what are the symptoms.

- 38.** No output signal can be caused by no dc power, no input signal, or a short or open that prevents the signal from getting to the output.
- 39.** An incorrect output can be caused by an incorrect dc supply voltage, improper ground, incorrect component value, or a faulty component.
- 40.** Some types of obvious things that you look for when a system fails are visible faults such as shorted wires, solder splashes, wire clippings, bad or open connections, burned components, Also look for a signal that is incorrect in terms of amplitude shape, or frequency or the absence of a signal.
- 41.** To isolate a fault in a system, apply half-splitting or signal tracing.
- 42.** Two common troubleshooting instruments are the oscilloscope and the DMM.
- 43.** When a fault has been isolated to a particular circuit board, the options are to repair the board or replace the board with a known good board.

CHAPTER 2

NUMBER SYSTEMS, OPERATIONS, AND CODES

Section 2-1 Decimal Numbers

1. (a) $1386 = 1 \times 10^3 + 3 \times 10^2 + 8 \times 10^1 + 6 \times 10^0$
 $= 1 \times 1000 + 3 \times 100 + 8 \times 10 + 6 \times 1$
The digit 6 has a weight of $10^0 = 1$

(b) $54,692 = 5 \times 10^4 + 4 \times 10^3 + 6 \times 10^2 + 9 \times 10^1 + 2 \times 10^0$
 $= 5 \times 10,000 + 4 \times 1000 + 6 \times 100 + 9 \times 10 + 2 \times 1$
The digit 6 has a weight of $10^2 = 100$

(c) $671,920 = 6 \times 10^5 + 7 \times 10^4 + 1 \times 10^3 + 9 \times 10^2 + 2 \times 10^1 + 0 \times 10^0$
 $= 6 \times 100,000 + 7 \times 10,000 + 1 \times 1000 + 9 \times 100 + 2 \times 10 + 0 \times 1$
The digit 6 has a weight of $10^5 = 100,000$

2. (a) $10 = 10^1$ (b) $100 = 10^2$
(c) $10,000 = 10^4$ (d) $1,000,000 = 10^6$

3. (a) $471 = 4 \times 10^2 + 7 \times 10^1 + 1 \times 10^0$
 $= 4 \times 100 + 7 \times 10 + 1 \times 1$
 $= 400 + 70 + 1$

(b) $9,356 = 9 \times 10^3 + 3 \times 10^2 + 5 \times 10^1 + 6 \times 10^0$
 $= 9 \times 1000 + 3 \times 100 + 5 \times 10 + 6 \times 1$
 $= 9,000 + 300 + 50 + 6$

(c) $125,000 = 1 \times 10^5 + 2 \times 10^4 + 5 \times 10^3$
 $= 1 \times 100,000 + 2 \times 10,000 + 5 \times 1000$
 $= 100,000 + 20,000 + 5,000$

4. The highest four-digit decimal number is 9999.

Section 2-2 Binary Numbers

5. (a) $11 = 1 \times 2^1 + 1 \times 2^0 = 2 + 1 = 3$
(b) $100 = 1 \times 2^2 + 0 \times 2^1 + 0 \times 2^0 = 4$
(c) $111 = 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 = 4 + 2 + 1 = 7$
(d) $1000 = 1 \times 2^3 + 0 \times 2^2 + 0 \times 2^1 + 0 \times 2^0 = 8$
(e) $1001 = 1 \times 2^3 + 0 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 = 8 + 1 = 9$
(f) $1100 = 1 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 0 \times 2^0 = 8 + 4 = 12$
(g) $1011 = 1 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 = 8 + 2 + 1 = 11$
(h) $1111 = 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 = 8 + 4 + 2 + 1 = 15$

- 6.**
- (a) $1110 = 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 = 8 + 4 + 2 = 14$
 - (b) $1010 = 1 \times 2^3 + 1 \times 2^1 = 8 + 2 = 10$
 - (c) $11100 = 1 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 = 16 + 8 + 4 = 28$
 - (d) $10000 = 1 \times 2^4 = 16$
 - (e) $10101 = 1 \times 2^4 + 1 \times 2^2 + 1 \times 2^0 = 16 + 4 + 1 = 21$
 - (f) $11101 = 1 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^0 = 16 + 8 + 4 + 1 = 29$
 - (g) $10111 = 1 \times 2^4 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 = 16 + 4 + 2 + 1 = 23$
 - (h) $11111 = 1 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 = 16 + 8 + 4 + 2 + 1 = 31$
- 7.**
- (a) $110011.11 = 1 \times 2^5 + 1 \times 2^4 + 1 \times 2^1 + 1 \times 2^0 + 1 \times 2^{-1} + 1 \times 2^{-2}$
 $= 32 + 16 + 2 + 1 + 0.5 + 0.25 = 51.75$
 - (b) $101010.01 = 1 \times 2^5 + 1 \times 2^3 + 1 \times 2^1 + 1 \times 2^{-2} = 32 + 8 + 2 + 0.25$
 $= 42.25$
 - (c) $1000001.111 = 1 \times 2^6 + 1 \times 2^0 + 1 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3}$
 $= 64 + 1 + 0.5 + 0.25 + 0.125 = 65.875$
 - (d) $1111000.101 = 1 \times 2^6 + 1 \times 2^5 + 1 \times 2^4 + 1 \times 2^3 + 1 \times 2^{-1} + 1 \times 2^{-3}$
 $= 64 + 32 + 16 + 8 + 0.5 + 0.125 = 120.625$
 - (e) $1011100.10101 = 1 \times 2^6 + 1 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^{-1} + 1 \times 2^{-3} + 1 \times 2^{-5}$
 $= 64 + 16 + 8 + 4 + 0.5 + 0.125 + 0.03125$
 $= 92.65625$
 - (f) $1110001.0001 = 1 \times 2^6 + 1 \times 2^5 + 1 \times 2^4 + 1 \times 2^0 + 1 \times 2^{-4}$
 $= 64 + 32 + 16 + 1 + 0.0625 = 113.0625$
 - (g) $1011010.1010 = 1 \times 2^6 + 1 \times 2^4 + 1 \times 2^3 + 1 \times 2^1 + 1 \times 2^{-1} + 1 \times 2^{-3}$
 $= 64 + 16 + 8 + 2 + 0.5 + 0.125 = 90.625$
 - (h) $1111111.11111 = 1 \times 2^6 + 1 \times 2^5 + 1 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1$
 $+ 1 \times 2^0 + 1 \times 2^{-1} + 1 \times 2^{-2} + 1 \times 2^{-3} + 1 \times 2^{-4} + 1 \times 2^{-5}$
 $= 64 + 32 + 16 + 8 + 4 + 2 + 1 + 0.5 + 0.25 + 0.125 + 0.0625 + 0.03125$
 $= 127.96875$
- 8.**
- | | |
|-------------------------|-------------------------|
| (a) $2^2 - 1 = 3$ | (b) $2^3 - 1 = 7$ |
| (c) $2^4 - 1 = 15$ | (d) $2^5 - 1 = 31$ |
| (e) $2^6 - 1 = 63$ | (f) $2^7 - 1 = 127$ |
| (g) $2^8 - 1 = 255$ | (h) $2^9 - 1 = 511$ |
| (i) $2^{10} - 1 = 1023$ | (j) $2^{11} - 1 = 2047$ |
- 9.**
- (a) $(2^4 - 1) < 17 < (2^5 - 1)$; 5 bits
 - (b) $(2^5 - 1) < 35 < (2^6 - 1)$; 6 bits
 - (c) $(2^5 - 1) < 49 < (2^6 - 1)$; 6 bits
 - (d) $(2^6 - 1) < 68 < (2^7 - 1)$; 7 bits
 - (e) $(2^6 - 1) < 81 < (2^7 - 1)$; 7 bits
 - (f) $(2^6 - 1) < 114 < (2^7 - 1)$; 7 bits
 - (g) $(2^7 - 1) < 132 < (2^8 - 1)$; 8 bits
 - (h) $(2^7 - 1) < 205 < (2^8 - 1)$; 8 bits

Chapter 2

- 10.** (a) 0 through 7:
000, 001, 010, 011, 100, 101, 110, 111
(b) 8 through 15:
1000, 1001, 1010, 1011, 1100, 1101, 1110, 1111
(c) 16 through 31:
10000, 10001, 10010, 10011, 10100, 10101, 10110, 10111, 11000, 11001, 11010,
11011, 11100, 11101, 11110, 11111
(d) 32 through 63:
100000, 100001, 100010, 100011, 100100, 100101, 100110, 100111, 10100, 101001,
101010, 101011, 101100, 101101, 101110, 101111, 110000, 110001, 110010, 110011,
110100, 110101, 110110, 110111, 111000, 111001, 111010, 111011, 111100, 111101,
111110, 111111
(e) 64 through 75:
1000000, 1000001, 1000010, 1000011, 1000100, 1000101, 1000110, 1000111,
1001000, 1001001, 1001010, 1001011

Section 2-3 Decimal-to-Binary Conversion

- 11.** (a) $10 = 8 + 2 = 2^3 + 2^1 = 1010$
(b) $17 = 16 + 1 = 2^4 + 2^0 = 10001$
(c) $24 = 16 + 8 = 2^4 + 2^3 = 11000$
(d) $48 = 32 + 16 = 2^5 + 2^4 = 110000$
(e) $61 = 32 + 16 + 8 + 4 + 1 = 2^5 + 2^4 + 2^3 + 2^2 + 2^0 = 111101$
(f) $93 = 64 + 16 + 8 + 4 + 1 = 2^6 + 2^4 + 2^3 + 2^2 + 2^0 = 1011101$
(g) $125 = 64 + 32 + 16 + 8 + 4 + 1 = 2^6 + 2^5 + 2^4 + 2^3 + 2^2 + 2^0 = 1111101$
(h) $186 = 128 + 32 + 16 + 8 + 2 = 2^7 + 2^5 + 2^4 + 2^3 + 2^1 = 10111010$
- 12.** (a) $0.32 \cong 0.00 + 0.25 + 0.0625 + 0.0 + 0.0 + 0.0078125 = 0.0101001$
(b) $0.246 \cong 0.0 + 0.0 + 0.125 + 0.0625 + 0.03125 + 0.015625 = 0.001111$
(c) $0.0981 \cong 0.0 + 0.0 + 0.0 + 0.0625 + 0.03125 + 0.0 + 0.0 + 0.00390625 = 0.0001101$

- 13.** (a) $\frac{15}{2} = 7, R = 1$ (LSB) (b) $\frac{21}{2} = 10, R = 1$ (LSB) (c) $\frac{28}{2} = 14, R = 0$ (LSB)
- $\frac{7}{2} = 3, R = 1$ $\frac{10}{2} = 5, R = 0$ $\frac{14}{2} = 7, R = 0$
- $\frac{3}{2} = 1, R = 1$ $\frac{5}{2} = 2, R = 1$ $\frac{7}{2} = 3, R = 1$
- $\frac{1}{2} = 0, R = 1$ (MSB) $\frac{2}{2} = 1, R = 0$ $\frac{3}{2} = 1, R = 1$
- $\frac{1}{2} = 0, R = 1$ (MSB) $\frac{1}{2} = 0, R = 1$ (MSB)
- (d) $\frac{34}{2} = 17, R = 0$ (LSB) (e) $\frac{40}{2} = 20, R = 0$ (LSB) (f) $\frac{59}{2} = 29, R = 1$ (LSB)
- $\frac{17}{2} = 8, R = 1$ $\frac{20}{2} = 10, R = 0$ $\frac{29}{2} = 14, R = 1$
- $\frac{8}{2} = 4, R = 0$ $\frac{10}{2} = 5, R = 0$ $\frac{14}{2} = 7, R = 0$
- $\frac{4}{2} = 2, R = 0$ $\frac{5}{2} = 2, R = 1$ $\frac{7}{2} = 3, R = 1$
- $\frac{2}{2} = 1, R = 0$ $\frac{2}{2} = 1, R = 0$ $\frac{3}{2} = 1, R = 1$
- $\frac{1}{2} = 0, R = 1$ (MSB) $\frac{1}{2} = 0, R = 1$ (MSB) $\frac{1}{2} = 0, R = 1$ (MSB)
- (g) $\frac{65}{2} = 32, R = 1$ (LSB) (h) $\frac{73}{2} = 36, R = 1$ (LSB)
- $\frac{32}{2} = 16, R = 0$ $\frac{36}{2} = 18, R = 0$
- $\frac{16}{2} = 8, R = 0$ $\frac{18}{2} = 9, R = 0$
- $\frac{8}{2} = 4, R = 0$ $\frac{9}{2} = 4, R = 1$
- $\frac{4}{2} = 2, R = 0$ $\frac{4}{2} = 2, R = 0$
- $\frac{2}{2} = 1, R = 0$ $\frac{2}{2} = 1, R = 0$
- $\frac{1}{2} = 0, R = 1$ (MSB) $\frac{1}{2} = 0, R = 1$ (MSB)

Chapter 2

- 14.** (a) $0.98 \times 2 = 1.96$ 1 (MSB)
 $0.96 \times 2 = 1.92$ 1
 $0.92 \times 2 = 1.84$ 1
 $0.84 \times 2 = 1.68$ 1
 $0.68 \times 2 = 1.36$ 1
 $0.36 \times 2 = 0.72$ 0
 continue if more accuracy is desired
 0.111110
- (b) $0.347 \times 2 = 0.694$ 0 (MSB)
 $0.694 \times 2 = 1.388$ 1
 $0.388 \times 2 = 0.776$ 0
 $0.776 \times 2 = 1.552$ 1
 $0.552 \times 2 = 1.104$ 1
 $0.104 \times 2 = 0.208$ 0
 $0.208 \times 2 = 0.416$ 0
 continue if more accuracy is desired
 0.0101100
- (c) $0.9028 \times 2 = 1.8056$ 1 (MSB)
 $0.8056 \times 2 = 1.6112$ 1
 $0.6112 \times 2 = 1.2224$ 1
 $0.2224 \times 2 = 0.4448$ 0
 $0.4448 \times 2 = 0.8896$ 0
 $0.8896 \times 2 = 1.7792$ 1
 $0.7792 \times 2 = 1.5584$ 1
 continue if more accuracy is desired
 0.1110011

Section 2-4 Binary Arithmetic

- | | | | | | |
|----------------|--|-----|--|-----|---|
| 15. (a) | $\begin{array}{r} 11 \\ + 01 \\ \hline 100 \end{array}$ | (b) | $\begin{array}{r} 10 \\ + 10 \\ \hline 100 \end{array}$ | (c) | $\begin{array}{r} 101 \\ + 011 \\ \hline 1000 \end{array}$ |
| (d) | $\begin{array}{r} 111 \\ + 110 \\ \hline 1101 \end{array}$ | (e) | $\begin{array}{r} 1001 \\ + 0101 \\ \hline 1110 \end{array}$ | (f) | $\begin{array}{r} 1101 \\ + 1011 \\ \hline 11000 \end{array}$ |
| 16. (a) | $\begin{array}{r} 11 \\ - 01 \\ \hline 10 \end{array}$ | (b) | $\begin{array}{r} 101 \\ - 100 \\ \hline 001 \end{array}$ | (c) | $\begin{array}{r} 110 \\ - 101 \\ \hline 001 \end{array}$ |
| (d) | $\begin{array}{r} 1110 \\ - 0011 \\ \hline 1011 \end{array}$ | (e) | $\begin{array}{r} 1100 \\ - 1001 \\ \hline 0011 \end{array}$ | (f) | $\begin{array}{r} 11010 \\ - 10111 \\ \hline 00011 \end{array}$ |

17. (a) $\begin{array}{r} 11 \\ \times 11 \\ \hline 11 \end{array}$	(b) $\begin{array}{r} 100 \\ \times 10 \\ \hline 000 \end{array}$	(c) $\begin{array}{r} 111 \\ \times 101 \\ \hline 111 \end{array}$	(d) $\begin{array}{r} 1001 \\ \times 110 \\ \hline 0000 \end{array}$
$\begin{array}{r} 11 \\ \times 11 \\ \hline 100 \\ \hline 1001 \end{array}$	$\begin{array}{r} 100 \\ \times 100 \\ \hline 1000 \\ \hline 1000 \end{array}$	$\begin{array}{r} 000 \\ \times 111 \\ \hline 111 \\ \hline 1001 \end{array}$	$\begin{array}{r} 1001 \\ \times 1001 \\ \hline 110110 \end{array}$
(e) $\begin{array}{r} 1101 \\ \times 1101 \\ \hline 1101 \\ 0000 \\ \hline 1101 \\ 1101 \\ \hline 10101001 \end{array}$	(f) $\begin{array}{r} 1110 \\ \times 1101 \\ \hline 1110 \\ 0000 \\ \hline 1110 \\ 1110 \\ \hline 10110110 \end{array}$		

18. (a) $\frac{100}{10} = 010$ (b) $\frac{1001}{0011} = 0011$ (c) $\frac{1100}{0100} = 0011$

Section 2-5 Complements of Binary Numbers

- 19.** Zero is represented in 1's complement as all 0's (for +0) or all 1's (for -0).
- 20.** Zero is represented by all 0's only in 2's complement.
- 21.** (a) The 1's complement of 101 is 010.
 (b) The 1's complement of 110 is 001.
 (c) The 1's complement of 1010 is 0101.
 (d) The 1's complement of 1101011 is 00101000.
 (e) The 1's complement of 1110101 is 0001010.
 (f) The 1's complement of 00001 is 11110.
- 22.** Take the 1's complement and add 1:

(a) $01 + 1 = 10$	(b) $000 + 1 = 001$
(c) $0110 + 1 = 0111$	(d) $0010 + 1 = 0011$
(e) $00011 + 1 = 00100$	(f) $01100 + 1 = 01101$
(g) $01001111 + 1 = 01010000$	(h) $11000010 + 1 = 11000011$

Section 2-6 Signed Numbers

- 23.** (a) Magnitude of 29 = 0011101
 $+ 29 = 00011101$
- (b) Magnitude of 85 = 1010101
 $-85 = 11010101$
- (c) Magnitude of $100_{10} = 1100100$
 $+100 = 01100100$
- (d) Magnitude of 123 = 1111011
 $-123 = 11111011$

Chapter 2

- 24.** (a) Magnitude of $34 = 0100010$
 $-34 = 11011101$
- (b) Magnitude of $57 = 0111001$
 $+57 = 00111001$
- (c) Magnitude of $99 = 1100011$
 $-99 = 10011100$
- (d) Magnitude of $115 = 1110011$
 $+115 = 01110011$
- 25.** (a) Magnitude of $12 = 1100$
 $+12 = 00001100$
- (b) Magnitude of $68 = 1000100$
 $-68 = 10111100$
- (c) Magnitude of $101_{10} = 1100101$
 $+101_{10} = 01100101$
- (d) Magnitude of $125 = 1111101$
 $-125 = 10000011$
- 26.** (a) $10011001 = -25$ (b) $01110100 = +116$ (c) $10111111 = -63$
- 27.** (a) $10011001 = -(01100110) = -102$
(b) $01110100 = +(1110100) = +116$
(c) $10111111 = -(1000000) = -64$
- 28.** (a) $10011001 = -(1100111) = -103$
(b) $01110100 = +(1110100) = +116$
(c) $10111111 = -(1000001) = -65$
- 29.** (a) $0111110000101011 \rightarrow \text{sign} = 0$
 $1.11110000101011 \times 2^{14} \rightarrow \text{exponent} = 127 + 14 + 141 = 10001101$
Mantissa = $11110000101011000000000000$
010001101111100001010110000000000
- (b) $100110000011000 \rightarrow \text{sign} = 1$
 $1.10000011000 \times 2^{11} \rightarrow \text{exponent} = 127 + 11 = 138 = 10001010$
Mantissa = $1100000110000000000000000000$
11000101011000001100000000000000
- 30.** (a) $11000000101001001110001000000000$
Sign = 1
Exponent = $10000001 = 129 - 127 = 2$
Mantissa = $1.01001001110001 \times 2^2 = 101.001001110001$
 $-101.001001110001 = -\mathbf{5.15258789}$
- (b) $0110011001000011110100100000000$
Sign = 0
Exponent = $11001100 = 204 - 127 = 77$
Mantissa = 1.100001111101001
1.100001111101001 $\times 2^{77}$

Section 2-7 Arithmetic Operations with Signed Numbers

- 31.** (a) $33 = 00100001$ 00100001
 $15 = 00001111$ $\underline{+ 00001111}$
 00110000
- (b) $56 = 00111000$ 00111000
 $27 = 00011011$ $\underline{+ 11100101}$
 $-27 = 11100101$
 00011101
- (c) $46 = 00101110$ 11010010
 $-46 = 11010010$ $\underline{+ 00011001}$
 $25 = 00011001$ 11101011
- (d) $110_{10} = 01101110$ 10010010
 $-110_{10} = 10010010$ $\underline{+ 10101100}$
 $84 = 01010100$
 $-84 = 10101100$
 100111110
- 32.** (a) 00010110
 $\underline{+ 00110011}$
 01001001
- (b) 01110000
 $\underline{+ 10101111}$
 1000111111
- 33.** (a) 10001100
 $\underline{+ 00111001}$
 11000101
- (b) 11011001
 $\underline{+ 11100111}$
 11000000
- 34.** (a) 00110011
 $\underline{- 00010000}$
 00110011
- (b) 01100101
 $\underline{- 11101000}$
 01100101
- 01100101
 $\underline{+ 00011000}$
 01111101
- 35.** 01101010
 $\times \underline{11110001}$
 01101010
 $\underline{01101010}$
 100111110
 $\underline{01101010}$
 1011100110
 $\underline{01101010}$
 11000110110

Changing to 2's complement with sign: 100111001010

36.
$$\begin{array}{r} 01000100 \\ 00011001 \\ \hline 68 \end{array} = 00000010$$

$$\frac{68}{25} = 2, \text{ remainder of } 18$$

Section 2-8 Hexadecimal Numbers

- 37.** (a) $38_{16} = 0011\ 1000$
(b) $59_{16} = 0101\ 1001$
(c) $A14_{16} = 1010\ 0001\ 0100$
(d) $5C8_{16} = 0101\ 1100\ 1000$
(e) $4100_{16} = 0100\ 0001\ 0000\ 0000$
(f) $FB17_{16} = 1111\ 1011\ 0001\ 0111$
(g) $8A9D_{16} = 1000\ 1010\ 1001\ 1101$

Chapter 2

- 38.** (a) $1110 = E_{16}$
 (b) $10 = 2_{16}$
 (c) $0001\ 0111 = 17_{16}$
 (d) $1010\ 0110 = A6_{16}$
 (e) $0011\ 1111\ 0000 = 3F0_{16}$
 (f) $1001\ 1000\ 0010 = 982_{16}$
- 39.** (a) $23_{16} = 2 \times 16^1 + 3 \times 16^0 = 32 + 3 = 35$
 (b) $92_{16} = 9 \times 16^1 + 2 \times 16^0 = 144 + 2 = 146$
 (c) $1A_{16} = 1 \times 16^1 + 10 \times 16^0 = 16 + 10 = 26$
 (d) $8D_{16} = 8 \times 16^1 + 13 \times 16^0 = 128 + 13 = 141$
 (e) $F3_{16} = 15 \times 16^1 + 3 \times 16^0 = 240 + 3 = 243$
 (f) $EB_{16} = 14 \times 16^1 + 11 \times 16^0 = 224 + 11 = 235$
 (g) $5C2_{16} = 5 \times 16^2 + 12 \times 16^1 + 2 \times 16^0 = 1280 + 192 + 2 = 1474$
 (h) $700_{16} = 7 \times 16^2 = 1792$
- 40.** (a) $\frac{8}{16} = 0$, remainder = 8
 hexadecimal number = 8_{16}
- (b) $\frac{14}{16} = 0$, remainder = 14 = E_{16}
 hexadecimal number = E_{16}
- (c) $\frac{33}{16} = 2$, remainder = 1 (LSD)
 $\frac{2}{16} = 0$, remainder = 2
 hexadecimal number = 21_{16}
- (d) $\frac{52}{16} = 3$, remainder = 4 (LSD)
 $\frac{3}{16} = 0$, remainder = 3
 hexadecimal number = 34_{16}
- (e) $\frac{284}{16} = 17$, remainder = 12 = C_{16} (LSD)
 $\frac{17}{16} = 1$, remainder = 1
 $\frac{1}{16} = 0$, remainder = 1
 hexadecimal number = $11C_{16}$
- (f) $\frac{2890}{16} = 180$, remainder = 10 = A_{16} (LSD)
 $\frac{180}{16} = 11$, remainder = 4
 $\frac{11}{16} = 0$, remainder = 11 = B_{16}
 hexadecimal number = $B4A_{16}$
- (g) $\frac{4019}{16} = 251$, remainder = 3 (LSD)
 $\frac{251}{16} = 15$, remainder = 11 = B_{16}
 $\frac{15}{16} = 0$, remainder = 15 = F_{16}
 hexadecimal number = $FB3_{16}$
- (h) $\frac{6500}{16} = 406$, remainder = 4 (LSD)
 $\frac{406}{16} = 25$, remainder = 6
 $\frac{25}{16} = 1$, remainder = 9
 $\frac{1}{16} = 0$, remainder = 1
 hexadecimal number = 1964_{16}
- 41.** (a) $37_{16} + 29_{16} = 60_{16}$
 (b) $A0_{16} + 6B_{16} = 10B_{16}$
 (c) $FF_{16} + BB_{16} = 1BA_{16}$

- 42.** (a) $51_{16} - 40_{16} = 11_{16}$
 (b) $C8_{16} - 3A_{16} = 8E_{16}$
 (c) $FD_{16} - 88_{16} = 75_{16}$

Section 2-9 Octal Numbers

- 43.** (a) $12_8 = 1 \times 8^1 + 2 \times 8^0 = 8 + 2 = 10$
 (b) $27_8 = 2 \times 8^1 + 7 \times 8^0 = 16 + 7 = 23$
 (c) $56_8 = 5 \times 8^1 + 6 \times 8^0 = 40 + 6 = 46$
 (d) $64_8 = 6 \times 8^1 + 4 \times 8^0 = 48 + 4 = 52$
 (e) $103_8 = 1 \times 8^2 + 3 \times 8^0 = 64 + 3 = 67$
 (f) $557_8 = 5 \times 8^2 + 5 \times 8^1 + 7 \times 8^0 = 320 + 40 + 7 = 367$
 (g) $163_8 = 1 \times 8^2 + 6 \times 8^1 + 3 \times 8^0 = 64 + 48 + 3 = 115$
 (h) $1024_8 = 1 \times 8^3 + 2 \times 8^1 + 4 \times 8^0 = 512 + 16 + 4 = 532$
 (i) $7765_8 = 7 \times 8^3 + 7 \times 8^2 + 6 \times 8^1 + 5 \times 8^0 = 3584 + 448 + 48 + 5 = 4085$

- 44.** (a) $\frac{15}{8} = 1$, remainder = 7 (LSD)
 $\frac{1}{8} = 0$, remainder = 1
 octal number = 17_8
- (b) $\frac{27}{8} = 3$, remainder = 3 (LSD)
 $\frac{3}{8} = 0$, remainder = 3
 octal number = 33_8
- (c) $\frac{46}{8} = 5$, remainder = 6 (LSD)
 $\frac{5}{8} = 0$, remainder = 5
 octal number = 56_8
- (d) $\frac{70}{8} = 8$, remainder = 6 (LSD)
 $\frac{8}{8} = 1$, remainder = 0
 $\frac{1}{8} = 0$, remainder = 1
 octal number = 106_8
- (e) $\frac{100}{8} = 12$, remainder = 4 (LSD)
 $\frac{12}{8} = 1$, remainder = 4
 $\frac{1}{8} = 0$, remainder = 1
 octal number = 144_8
- (f) $\frac{142}{8} = 17$, remainder = 6 (LSD)
 $\frac{17}{8} = 2$, remainder = 1
 $\frac{2}{8} = 0$, remainder = 2
 octal number = 216_8
- (g) $\frac{219}{8} = 27$, remainder = 3 (LSD)
 $\frac{27}{8} = 3$, remainder = 3
 $\frac{3}{8} = 0$, remainder = 3
 octal number = 333_8
- (h) $\frac{435}{8} = 54$, remainder = 3 (LSD)
 $\frac{54}{8} = 6$, remainder = 6
 $\frac{6}{8} = 0$, remainder = 6
 octal number = 663_8

- 45.** (a) $13_8 = 001\ 011$
 (b) $57_8 = 101\ 111$
 (c) $101_8 = 001\ 000\ 001$
 (d) $321_8 = 011\ 010\ 001$
 (e) $540_8 = 101\ 100\ 000$
 (f) $4653_8 = 100\ 110\ 101\ 011$
 (g) $13271_8 = 001\ 011\ 010\ 111\ 001$
 (h) $45600_8 = 100\ 101\ 110\ 000\ 000$
 (i) $100213_8 = 001\ 000\ 000\ 010\ 001\ 011$

- 46.** (a) $111 = 7_8$
 (b) $010 = 2_8$
 (c) $110\ 111 = 67_8$
 (d) $101\ 010 = 52_8$
 (e) $001\ 100 = 14_8$
 (f) $001\ 011\ 110 = 136_8$
 (g) $101\ 100\ 011\ 001 = 5431_8$
 (h) $010\ 110\ 000\ 011 = 2603_8$
 (i) $111\ 111\ 101\ 111\ 000 = 77570_8$

Section 2-10 Binary Coded Decimal (BCD)

- 47.** (a) $10 = 0001\ 0000$
 (b) $13 = 0001\ 0011$
 (c) $18 = 0001\ 1000$
 (d) $21 = 0010\ 0001$
 (e) $25 = 0010\ 0101$
 (f) $36 = 0011\ 0110$
 (g) $44 = 0100\ 0100$
 (h) $57 = 0101\ 0111$
 (i) $69 = 0110\ 1001$
 (j) $98 = 1001\ 1000$
 (k) $125 = 0001\ 0010\ 0101$
 (l) $156 = 0001\ 0101\ 0110$

- 48.** (a) $10 = 1010_2$ 4 bits binary, 8 bits BCD
 (b) $13 = 1101_2$ 4 bits binary, 8 bits BCD
 (c) $18 = 10010_2$ 5 bits binary, 8 bits BCD
 (d) $21 = 10101_2$ 5 bits binary, 8 bits BCD
 (e) $25 = 11001_2$ 5 bits binary, 8 bits BCD
 (f) $36 = 100100_2$ 6 bits binary, 8 bits BCD
 (g) $44 = 101100_2$ 6 bits binary, 8 bits BCD
 (h) $57 = 111001_2$ 6 bits binary, 8 bits BCD
 (i) $69 = 1000101_2$ 7 bits binary, 8 bits BCD
 (j) $98 = 1100010_2$ 7 bits binary, 8 bits BCD
 (k) $125 = 1111101_2$ 7 bits binary, 12 bits BCD
 (l) $156 = 10011100_2$ 8 bits binary, 12 bits BCD

- 49.** (a) $104 = 0001\ 0000\ 0100$
 (b) $128 = 0001\ 0010\ 1000$
 (c) $132 = 0001\ 0011\ 0010$
 (d) $150 = 0001\ 0101\ 0000$
 (e) $186 = 0001\ 1000\ 0110$
 (f) $210 = 0010\ 0001\ 0000$
 (g) $359 = 0011\ 0101\ 1001$
 (h) $547 = 0101\ 0100\ 0111$
 (i) $1051 = 0001\ 0000\ 0101\ 0001$

- 50.** (a) $0001 = 1$ (b) $0110 = 6$
 (c) $1001 = 9$ (d) $0001\ 1000 = 18$
 (e) $0001\ 1001 = 19$ (f) $0011\ 0010 = 32$
 (g) $0100\ 0101 = 45$ (h) $1001\ 1000 = 98$
 (i) $1000\ 0111\ 0000 = 870$

- 51.** (a) $1000\ 0000 = 80$
 (b) $0010\ 0011\ 0111 = 237$
 (c) $0011\ 0100\ 0110 = 346$
 (d) $0100\ 0010\ 0001 = 421$
 (e) $0111\ 0101\ 0100 = 754$
 (f) $1000\ 0000\ 0000 = 800$
 (g) $1001\ 0111\ 1000 = 978$
 (h) $0001\ 0110\ 1000\ 0011 = 1683$
 (i) $1001\ 0000\ 0001\ 1000 = 9018$
 (j) $0110\ 0110\ 0110\ 0111 = 6667$

- 52.** (a)
$$\begin{array}{r} 0010 \\ + 0001 \\ \hline 0011 \end{array}$$
 (b)
$$\begin{array}{r} 0101 \\ + 0011 \\ \hline 1000 \end{array}$$
 (c)
$$\begin{array}{r} 0111 \\ + 0010 \\ \hline 1001 \end{array}$$

 (d)
$$\begin{array}{r} 1000 \\ + 0001 \\ \hline 1001 \end{array}$$
 (e)
$$\begin{array}{r} 00011000 \\ + 00010001 \\ \hline 00101001 \end{array}$$
 (f)
$$\begin{array}{r} 01100100 \\ + 00110011 \\ \hline 10010111 \end{array}$$

 (g)
$$\begin{array}{r} 01000000 \\ + 01000111 \\ \hline 10000111 \end{array}$$
 (h)
$$\begin{array}{r} 10000101 \\ + 01000111 \\ \hline 10000111 \end{array}$$

Chapter 2

53. (a)

$$\begin{array}{r}
 1000 \\
 + 0110 \\
 \hline
 1110 \quad \text{invalid}
 \end{array}$$

(b)

$$\begin{array}{r}
 0111 \\
 + 0101 \\
 \hline
 1100 \quad \text{invalid}
 \end{array}$$

(c)

$$\begin{array}{r}
 1001 \\
 + 1000 \\
 \hline
 10001 \quad \text{invalid}
 \end{array}$$

(d)

$$\begin{array}{r}
 1001 \\
 + 0111 \\
 \hline
 10000 \quad \text{invalid}
 \end{array}$$

(e)

$$\begin{array}{r}
 00100101 \\
 + 00100111 \\
 \hline
 01001100 \quad \text{invalid}
 \end{array}$$

(f)

$$\begin{array}{r}
 01010001 \\
 + 01011000 \\
 \hline
 10101001 \quad \text{invalid}
 \end{array}$$

(g)

$$\begin{array}{r}
 10011000 \\
 + 10010111 \\
 \hline
 100101111 \quad \text{invalid}
 \end{array}$$

(h)

$$\begin{array}{r}
 010101100001 \\
 + 011100001000 \\
 \hline
 110001101001 \quad \text{invalid}
 \end{array}$$

54. (a)
$$\begin{array}{r} 4 + 3 \\ 0100 \\ + 0011 \\ \hline 0111 \end{array}$$

(b)
$$\begin{array}{r} 5 + 2 \\ 0101 \\ + 0010 \\ \hline 0111 \end{array}$$

(c)
$$\begin{array}{r} 6 + 4 \\ 0110 \\ + 0100 \\ \hline 1010 \\ + 0110 \\ \hline 00010000 \end{array}$$

(d)
$$\begin{array}{r} 17 + 12 \\ 00010111 \\ + 00100010 \\ \hline 00101001 \end{array}$$

(e)
$$\begin{array}{r} 28 + 23 \\ 00101000 \\ + 00100011 \\ \hline 01001011 \\ + 0110 \\ \hline 01010001 \end{array}$$

(f)
$$\begin{array}{r} 65 + 58 \\ 01100101 \\ + 01011000 \\ \hline 10111101 \\ + 01100110 \\ \hline 000100100011 \end{array}$$

(g)
$$\begin{array}{r} 113 + 101 \\ 000100010011 \\ + 000100000001 \\ \hline 001000010100 \end{array}$$

(h)
$$\begin{array}{r} 295 + 157 \\ 001010010101 \\ + 000101010111 \\ \hline 00111101100 \\ + 01100110 \\ \hline 010001010010 \end{array}$$

Section 2-11 Digital Codes

55. The Gray code makes only one bit change at a time when going from one number in the sequence to the next number.

Gray for $1111_2 = 1000$

Gray for $0000_2 = 0000$

56. (a)
$$\begin{array}{r} 1 + 1 + 0 + 1 + 1 \\ 1 \ 0 \ 1 \ 1 \ 0 \end{array} \text{ Binary}$$

(b)
$$\begin{array}{r} 1 + 0 + 0 + 1 + 0 + 1 + 0 \\ 1 \ 1 \ 0 \ 1 \ 1 \ 1 \ 1 \end{array} \text{ Binary}$$

(c)
$$\begin{array}{r} 1 + 1 + 1 + 1 + 0 + 1 + 1 + 1 + 0 + 1 + 1 + 1 + 0 \\ 1 \ 0 \ 0 \ 0 \ 1 \ 1 \ 0 \ 0 \ 1 \ 1 \ 0 \ 0 \ 1 \end{array} \text{ Binary}$$

$$\begin{array}{r} \text{Gray} \\ \text{Gray} \end{array}$$

57. (a)
$$\begin{array}{r} 1 \ 0 \ 1 \ 0 \\ 1 \ 1 \ 0 \ 0 \end{array} \text{ Gray}$$

(b)
$$\begin{array}{r} 0 \ 0 \ 0 \ 1 \ 0 \\ 0 \ 0 \ 0 \ 1 \ 1 \end{array} \text{ Gray}$$

(c)
$$\begin{array}{r} 1 \ 1 \ 0 \ 0 \ 0 \ 0 \ 1 \ 0 \ 0 \ 0 \ 1 \\ 1 \ 0 \ 0 \ 0 \ 0 \ 0 \ 1 \ 1 \ 1 \ 1 \ 0 \end{array} \text{ Gray}$$

$$\begin{array}{r} \text{Gray} \\ \text{Binary} \end{array}$$

58. (a) $1 \rightarrow 00110001$

(b) $3 \rightarrow 00110011$

(c) $6 \rightarrow 00110110$

(d) $10 \rightarrow 0011000100110000$

(e) $18 \rightarrow 0011000100111000$

(f) $29 \rightarrow 0011001000111001$

(g) $56 \rightarrow 0011010100110110$

(h) $75 \rightarrow 0011011100110101$

(i) $107 \rightarrow 001100010011000000110111$

Chapter 2

- 59.** (a) $0011000 \rightarrow \text{CAN}$ (b) $1001010 \rightarrow \mathbf{J}$
(c) $0111101 \rightarrow =$ (d) $0100011 \rightarrow \#$
(e) $0111110 \rightarrow >$ (f) $1000010 \rightarrow \mathbf{B}$
- 60.** $1001000 \ 1100101 \ 1101100 \ 1101100 \ 1101111 \ 0101110 \ 0100000$
H e i l o . #
 $1001000 \ 1101111 \ 1110111 \ 0100000 \ 1100001 \ 1110010 \ 1100101$
H o w # a r e
 $0100000 \ 1111001 \ 1101111 \ 1110101 \ 0111111$
y o u ?
- 61.** $1001000 \ 1100101 \ 1101100 \ 1101100 \ 1101111 \ 0101110 \ 0100000$
48 **65** **6C** **6C** **6F** **2E** **20**
 $1001000 \ 1101111 \ 1110111 \ 0100000 \ 1100001 \ 1110010 \ 1100101$
48 **6F** **77** **20** **61** **72** **65**
 $0100000 \ 1111001 \ 1101111 \ 1110101 \ 0111111$
20 **79** **6F** **75** **3F**
- 62.** 30 INPUT A, B
- | | | |
|----|---------|-----------|
| 3 | 0110011 | 33_{16} |
| 0 | 0110000 | 30_{16} |
| SP | 0100000 | 20_{16} |
| I | 1001001 | 49_{16} |
| N | 1001110 | $4E_{16}$ |
| P | 1010000 | 50_{16} |
| U | 1010101 | 55_{16} |
| T | 1010100 | 54_{16} |
| SP | 0100000 | 20_{16} |
| A | 1000001 | 41_{16} |
| , | 0101100 | $2C_{16}$ |
| B | 1000010 | 42_{16} |

Section 2-12 Error Codes

- 63.** Code (b) 011101010 has five 1s, so it is in error.
- 64.** Codes (a) 11110110 and (c) 010101010101010 are in error because they have an even number of 1s.
- 65.** (a) 1 10100100 (b) 0 00001001 (c) 1 11111110

$$\begin{array}{r} \textbf{66. (a)} \quad \quad \quad 1100 \\ \quad \quad \quad + 1011 \\ \hline \quad \quad \quad 0111 \end{array}$$

$$\begin{array}{r}
 (b) \quad \quad \quad 1111 \\
 + 0100 \\
 \hline
 1011
 \end{array}$$

$$\begin{array}{r}
 (c) \quad 100011100 \\
 + \quad 10011001 \\
 \hline
 110000101
 \end{array}$$

$$67. \quad (a) \quad \begin{array}{r} 1100 \\ + 0111 \\ \hline 1011 \end{array}$$

$$\begin{array}{r} \text{(b)} \quad \quad \quad 1111 \\ \quad \quad \quad + 1011 \\ \hline \quad \quad \quad 0100 \end{array}$$

$$\begin{array}{r}
 (c) \quad 100011100 \\
 + \quad 110000101 \\
 \hline
 010011001
 \end{array}$$

In each case, you get the other number.

$$\begin{array}{r}
 \text{68.} \quad 101100100000 \\
 - 1010 \downarrow \downarrow \downarrow \downarrow \\
 \underline{1001} \\
 - 1010 \downarrow \downarrow \downarrow \downarrow \\
 \underline{1100} \\
 - 1010 \downarrow \downarrow \downarrow \downarrow \\
 \underline{1100} \\
 - 1010 \downarrow \downarrow \downarrow \downarrow \\
 \underline{1100} \\
 - 1010 \downarrow \downarrow \downarrow \downarrow \\
 \underline{1100} \\
 - 1010 \downarrow \downarrow \downarrow \downarrow \\
 \underline{1100} \\
 \text{Remainder} = 0110
 \end{array}$$

```

      101100100110
    - 1010
    -----
      1001
      1010
    - 1100
    -----
      1101
      1010
    - 1111
      1010
    - 1010
      1010
    - 0000
    -----

```

Remainder = 0110

Append remainder to data. CRC is 101100100110.

- 69.** Error in MSB of transmitted CRC:

```

001100100110
 1010 | |
1001 | |
1010 | |
    1100 |
  1010 | |
    1101 |
  1010 | |
    1110 |
  1010 | |
    1000 |
  1010 | |
    1011 |
1010 | |
    10
  
```

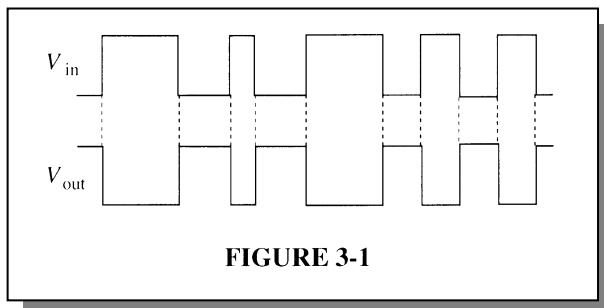
Remainder is 10, indicating an error.

CHAPTER 3

LOGIC GATES

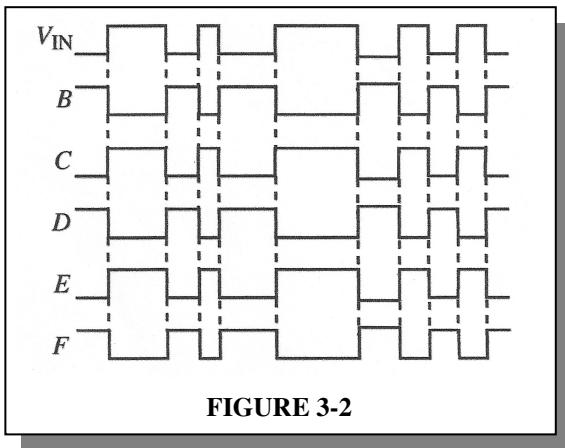
Section 3-1 The Inverter

1. See Figure 3-1.



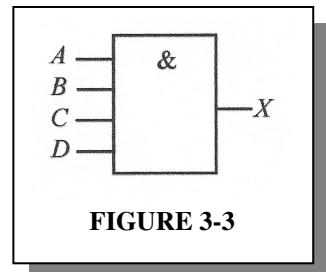
2. B: LOW, C: HIGH, D: LOW, E: HIGH, F: LOW

3. See Figure 3-2.



Section 3-2 The AND Gate

4. See Figure 3-3.



5. See Figure 3-4.

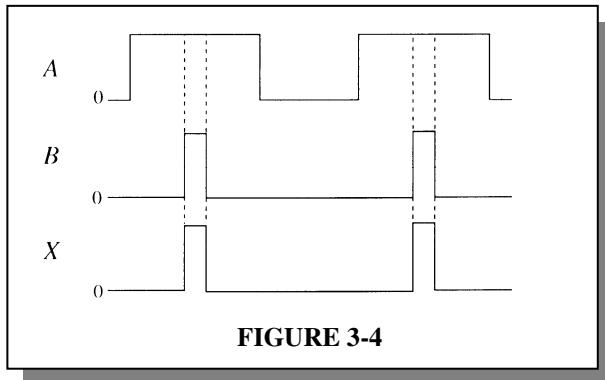


FIGURE 3-4

6. See Figure 3-5.

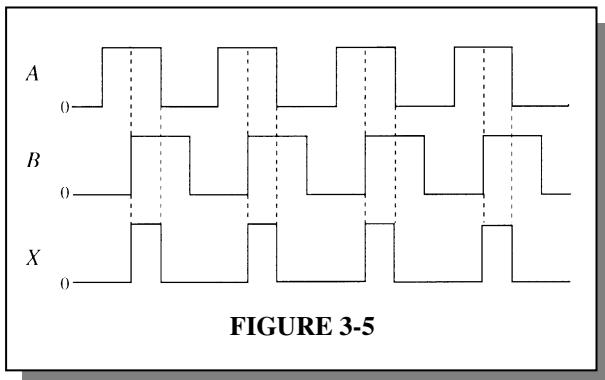


FIGURE 3-5

7. See Figure 3-6.

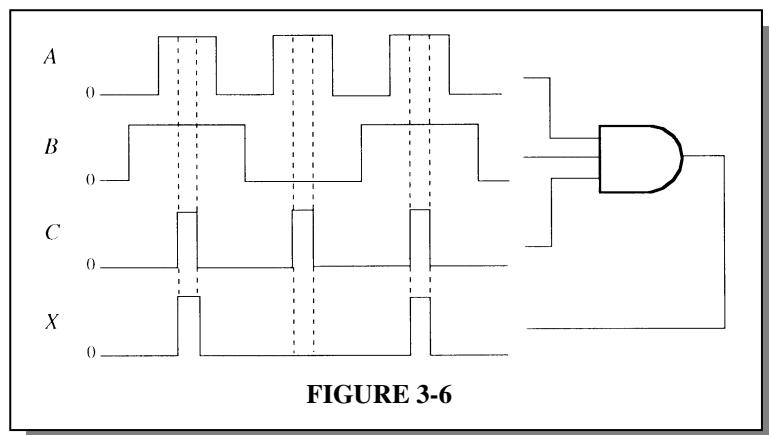
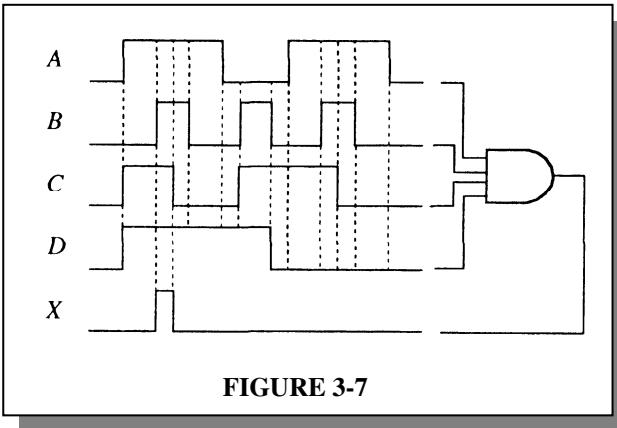


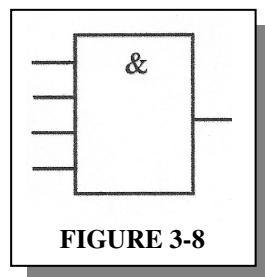
FIGURE 3-6

Chapter 3

8. See Figure 3-7.



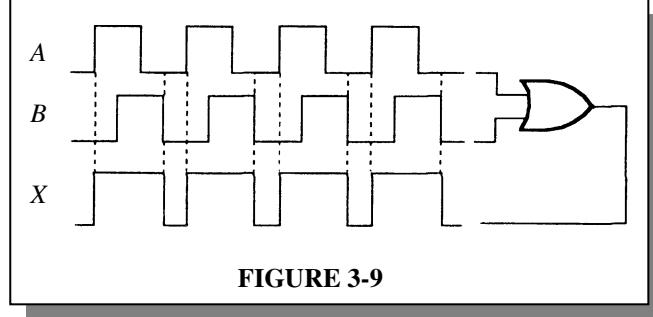
9. See Figure 3-8



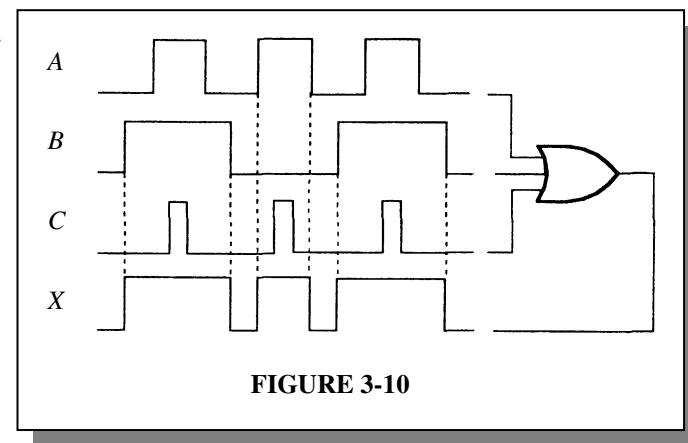
10. $X = A + B + C + D + E$

Section 3-3 The OR Gate

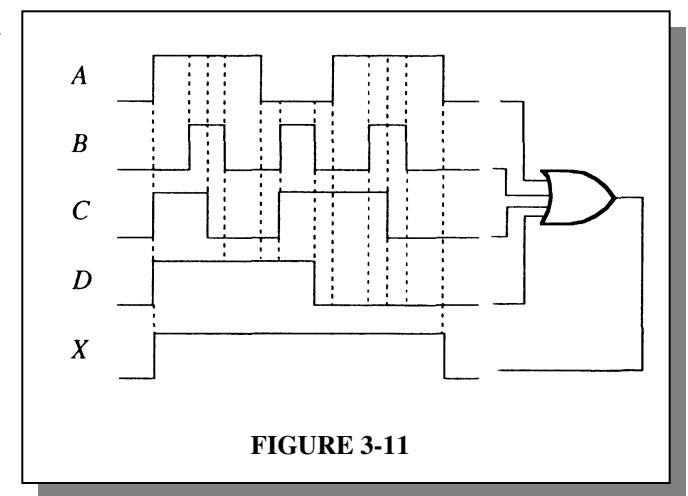
11. See Figure 3-9.



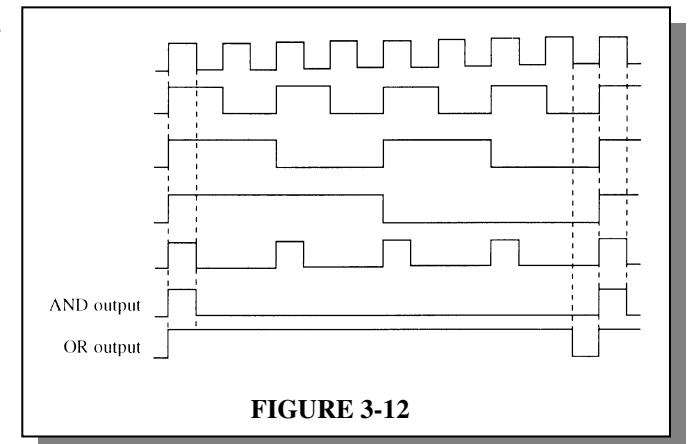
12. See Figure 3-10.



13. See Figure 3-11.



14. See Figure 3-12.



Chapter 3

15. See Figure 3-13.

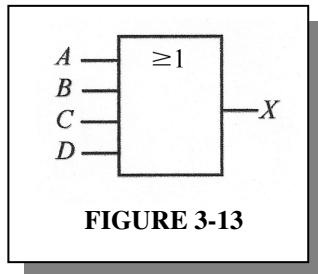


FIGURE 3-13

16.

A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	0	1
1	1	0	1
1	1	1	1

Section 3-4 The NAND Gate

17. See Figure 3-14.

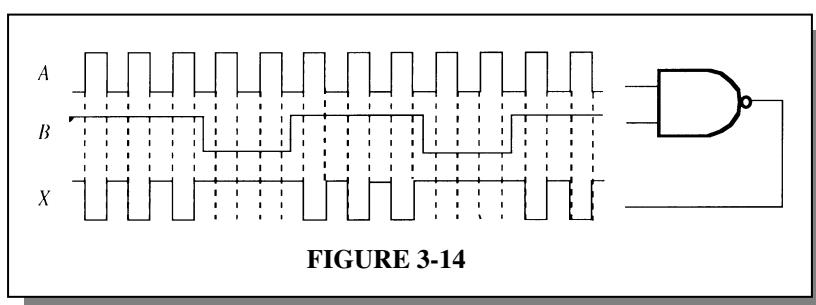


FIGURE 3-14

18. See Figure 3-15.

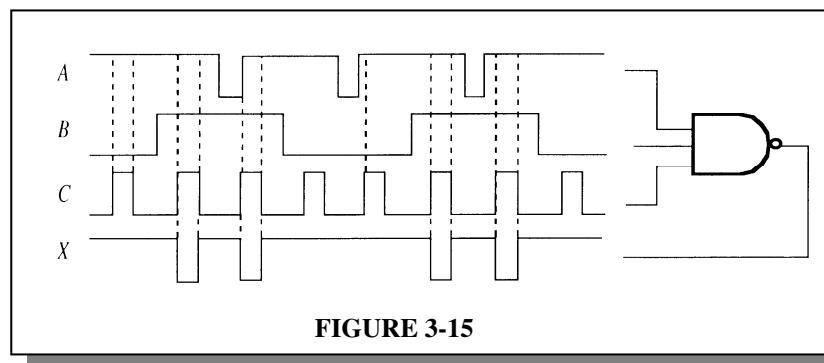
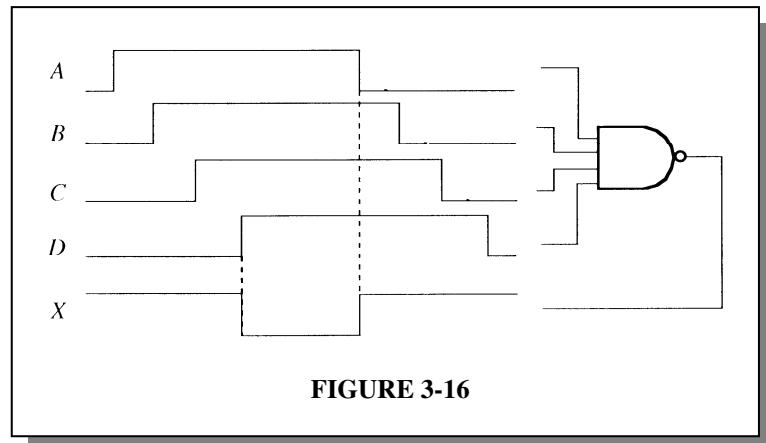
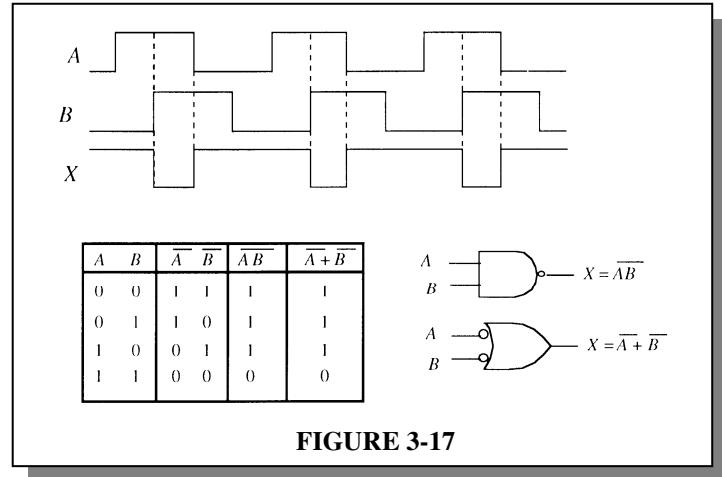


FIGURE 3-15

19. See Figure 3-16.

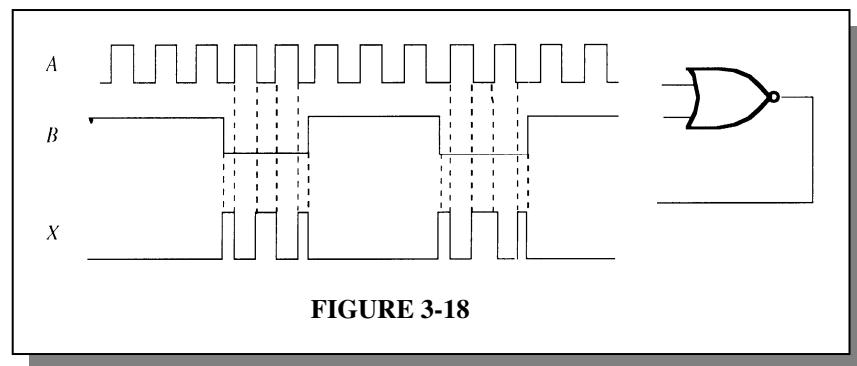


20. See Figure 3-17.



Section 3-5 The NOR Gate

21. See Figure 3-18.



Chapter 3

22. See Figure 3-19.

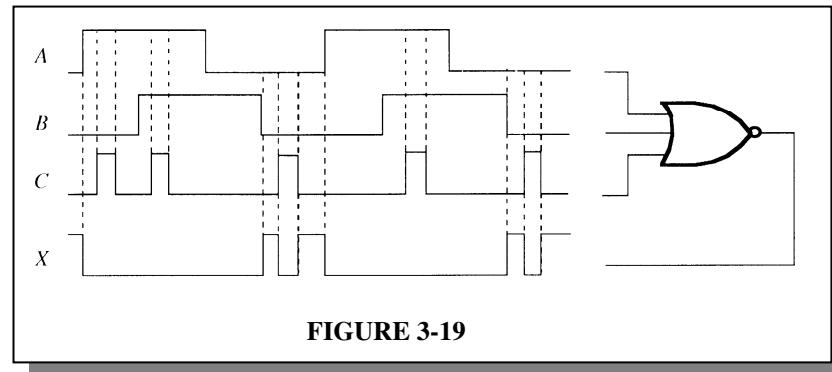


FIGURE 3-19

23. See Figure 3-20.

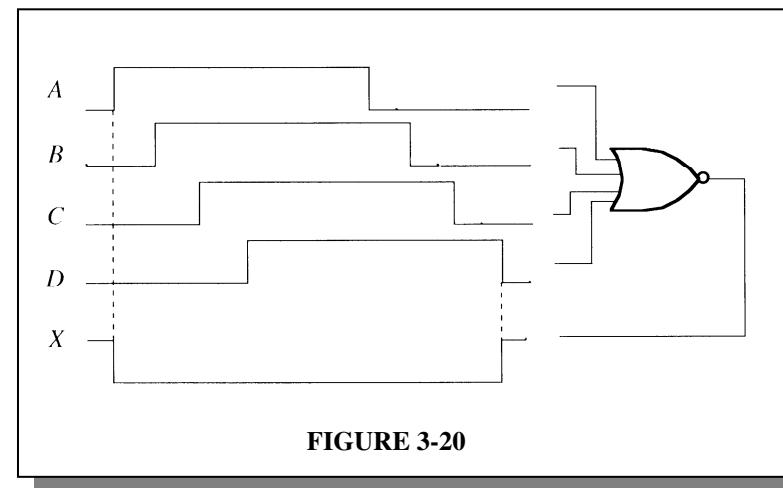


FIGURE 3-20

24. See Figure 3-21.

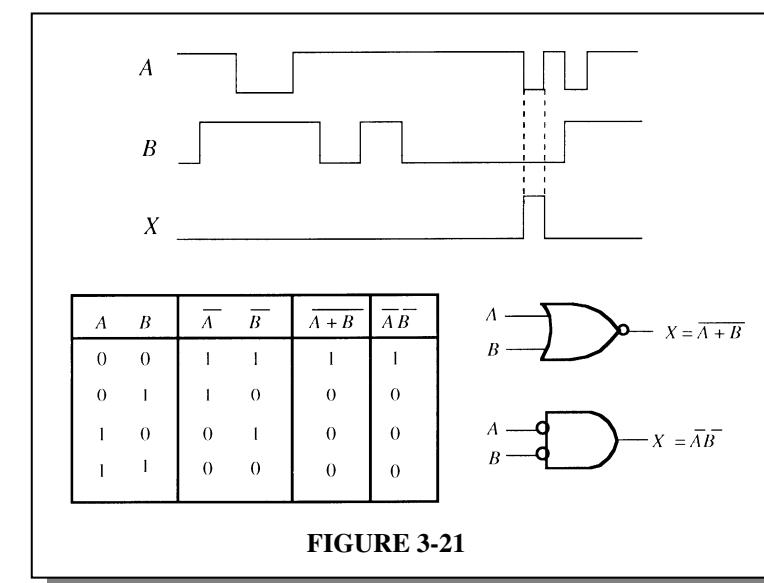


FIGURE 3-21

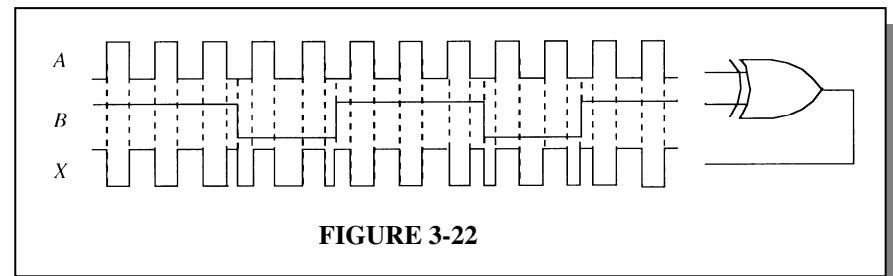
Section 3-6 The Exclusive-OR and Exclusive-NOR Gates

25. The output of the XOR gate is HIGH only when one input is HIGH. The output of the OR gate is HIGH any time one or more inputs are HIGH.

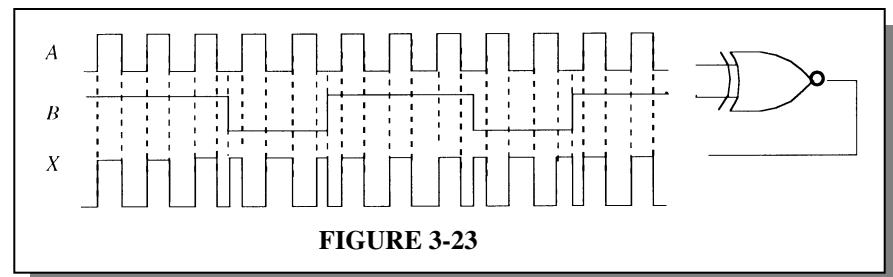
$$\text{XOR} = A\bar{B} + \bar{A}B$$

$$\text{OR} = A + B$$

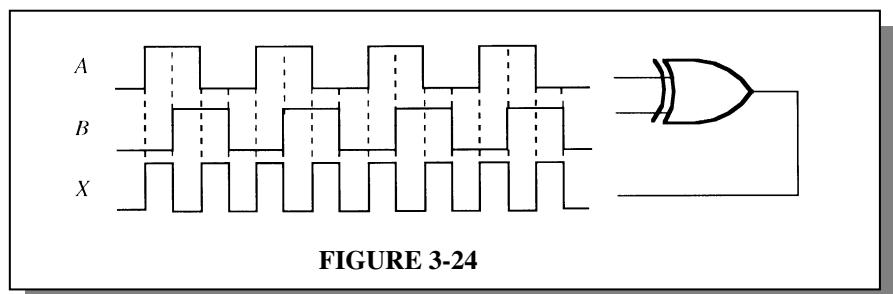
26. See Figure 3-22.



27. See Figure 3-23.



28. See Figure 3-24.



Section 3-7 Programmable Logic

29. $X_1 = \overline{AB}$

$$X_2 = \overline{A}\overline{B}$$

$$X_3 = A\overline{B}$$

Chapter 3

30. $X_1 = \overline{ABC}$

Row 1: blow A, B, \overline{B}, C , and \overline{C} column fuses

Row 2: blow $A, \overline{A}, \overline{B}, C$, and \overline{C} column fuses

Row 3: blow $A, \overline{A}, B, \overline{B}$, and \overline{C} column fuses

$X_2 = ABC\overline{C}$

Row 4: blow $\overline{A}, B, \overline{B}, C$, and \overline{C} column fuses

Row 5: blow $A, \overline{A}, \overline{B}, C$, and \overline{C} column fuses

Row 6: blow $A, \overline{A}, B, \overline{B}$, and C column fuses

$X_3 = \overline{ABC}$

Row 7: blow A, B, \overline{B}, C , and \overline{C} column fuses

Row 8: blow $A, \overline{A}, \overline{B}, C$, and \overline{C} column fuses

Row 9: blow $A, \overline{A}, B, \overline{B}$, and C column fuses

31. entity 4InputAND is

```
port (A, B, C, D: in bit; X: out bit);
```

```
end entity 4InputAND;
```

```
architecture Function of 4InputAND is
```

```
begin
```

```
    X <= A and B and C and D;
```

```
end architecture 4InputAND;
```

32. entity 5InputNOR is

```
port (A, B, C, D, E: in bit; X: out bit);
```

```
end entity 5InputNOR;
```

```
architecture Function of 5InputNOR is
```

```
begin
```

```
    X <= not(A or B or C or D or E);
```

```
end architecture 5InputNOR;
```

Section 3-8 Fixed Function Logic

33. The power dissipation of CMOS increases with frequency.

34. (a) $P = \left(\frac{I_{CCH} + I_{CCL}}{2} \right) V_{CC} = \left(\frac{1.6 \text{ mA} + 4.4 \text{ mA}}{2} \right) 5.5 \text{ V} = 16.5 \text{ mW}$
 (b) $V_{OH(\min)} = 2.7 \text{ V}$
 (c) $t_{PLH} = T_{PHL} = 15 \text{ ns}$
 (d) $V_{OL} = 0.4 \text{ V (max)}$
 (e) @ $V_{CC} = 2 \text{ V}$, $t_{PHL} = t_{PLH} = 75 \text{ ns}$; @ $V_{CC} = 6 \text{ V}$, $t_{PHL} = t_{PLH} = 73 \text{ ns}$

35. See Figure 3-25.

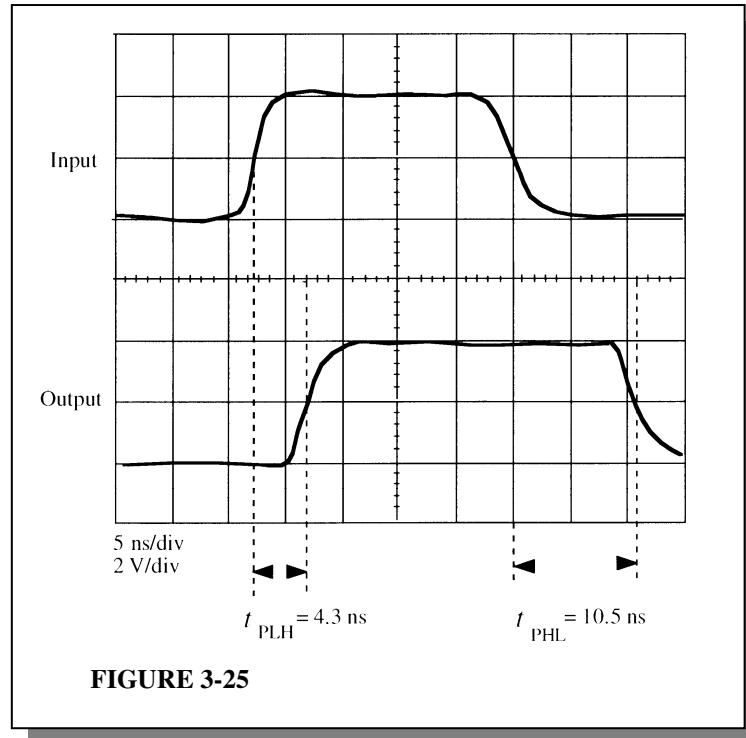


FIGURE 3-25

36. Gate A can be operated at the highest frequency because it has shorter propagation delay times than Gate B.
 37. $P_D = V_{CC}I_C = (5 \text{ V})(4 \text{ mA}) = 20 \text{ mW}$
 38. $I_{CCH} = 4 \text{ mA}; P_D = (5 \text{ V})(4 \text{ mA}) = 20 \text{ mW}$

Chapter 3

Section 3-9 Troubleshooting

- 39.** (a) NAND gate OK
(b) AND gate faulty
(c) NAND gate faulty
(d) NOR gate OK
(e) XOR gate faulty
(f) XOR gate OK
- 40.** (a) NAND gate faulty. Input A open
(b) NOR gate faulty. Input B shorted to ground.
(c) NADN gate OK
(d) XOR gate faulty. Input A open.
- 41.** (a) The gate does not respond to pulses on either input when the other input is HIGH. It is unlikely that both inputs are open. The most probable fault is that the output is stuck in the LOW state (shorted to ground, perhaps) although it could be open.
(b) Pin 4 input or pin 6 output internally open.
- 42.** The timer input to the AND gate is open. Check for 30-second HIGH level on this input when ignition is turned on.
- 43.** An open seat-belt input to the AND gate will act like a constant HIGH just as if the seat belt were unbuckled.
- 44.** Two possibilities: An input stuck LOW or the output stuck HIGH.

Special Design Problems

- 45.** Add an inverter to the Enable input line of the AND gate as shown in Figure 3-26.

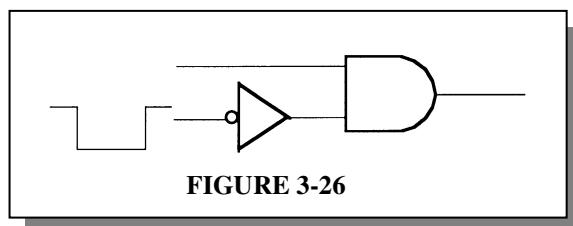


FIGURE 3-26

46. See Figure 3-27.

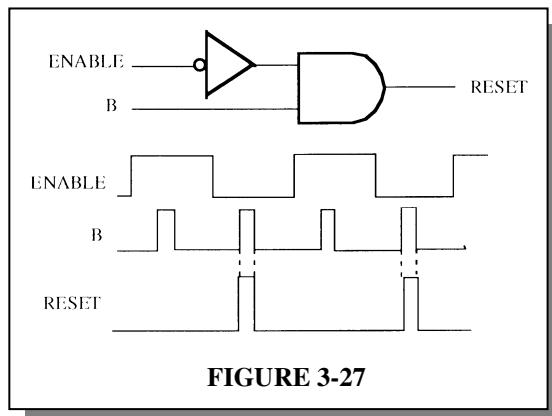


FIGURE 3-27

47. See Figure 3-28.

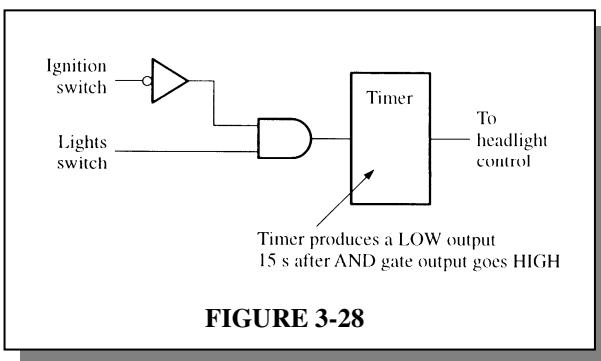


FIGURE 3-28

48. See Figure 3-29.

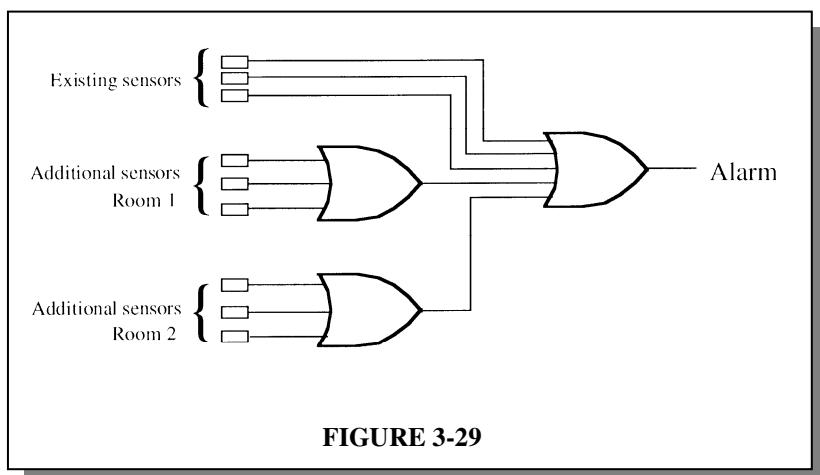
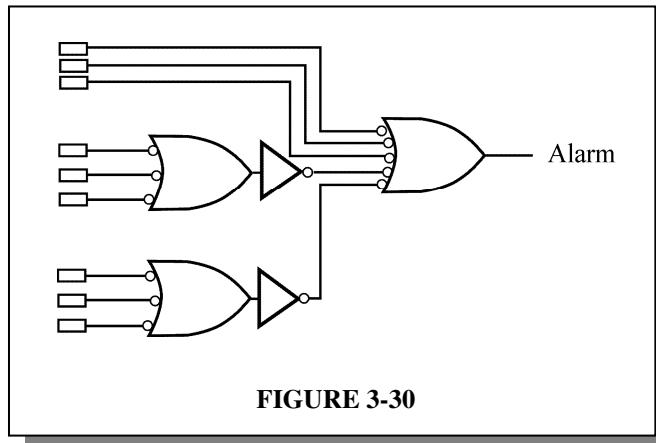


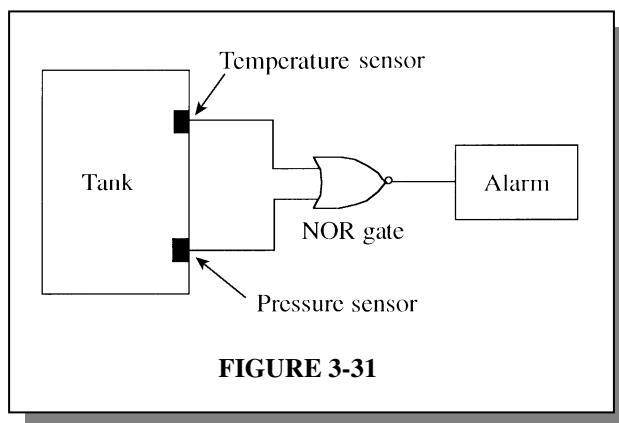
FIGURE 3-29

Chapter 3

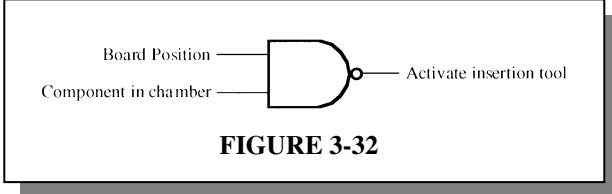
49. See Figure 3-30.



50. See Figure 3-31.



51. See Figure 3-32.



Multisim Troubleshooting Practice

52. Input B of AND gate U1 shorted to ground.
53. Input B of NAND gate shorted to V_{CC} .
54. Input A of NOR gate shorted to ground.
55. Input B of XOR gate shorted to V_{CC} .

CHAPTER 4

BOOLEAN ALGEBRA AND LOGIC SIMPLIFICATION

Section 4-1 Boolean Operations and Expressions

1. $X = A + B + C + D$

This is an OR configuration.

2. $Y = ABCDE$

3. $X = \overline{A} + \overline{B} + \overline{C}$

4. (a) $0 + 0 + 1 = 1$ (b) $1 + 1 + 1 = 1$

(c) $1 \cdot 0 \cdot 0 = 1$

(d) $1 \cdot 1 \cdot 1 = 1$

(e) $1 \cdot 0 \cdot 1 = 0$

(f) $1 \cdot 1 + 0 \cdot 1 \cdot 1 = 1 + 0 = 1$

5. (a) $AB = 1$ when $A = 1, B = 1$

(b) $\overline{ABC} = 1$ when $A = 1, B = 0, C = 1$

(c) $A + B = 0$ when $A = 0, B = 0$

(d) $\overline{A} + \overline{B} + \overline{C} = 0$ when $A = 1, B = 0, C = 1$

(e) $\overline{A} + \overline{B} + C = 0$ when $A = 1, B = 1, C = 0$

(f) $\overline{A} + B = 0$ when $A = 1, B = 0$

(g) $A\overline{B}\overline{C} = 1$ when $A = 1, B = 0, C = 0$

6. (a) $X = (A + B)C + B$

A	B	C	$A + B$	$(A + B)C$	X
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	1	0	1
0	1	1	1	1	1
1	0	0	1	0	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	1	1

(b) $X = (\overline{A} + \overline{B})C$

A	B	C	$\overline{A} + \overline{B}$	X
0	0	0	1	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	0	0
1	0	1	0	0
1	1	0	0	0
1	1	1	0	0

Chapter 4

(c) $X = A\bar{B}C + AB$

A	B	C	$A\bar{B}C$	AB	X
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	0	0
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	1	0	1
1	1	0	0	1	1
1	1	1	0	1	1

(d) $X = (A + B)(\bar{A} + B)$

A	B	$A + B$	$\bar{A} + B$	X
0	0	0	1	0
0	1	1	1	1
1	0	1	0	0
1	1	1	1	1

(e) $X = (A + BC)(\bar{B} + \bar{C})$

A	B	C	$A + BC$	$\bar{B} + \bar{C}$	X
0	0	0	0	1	0
0	0	1	0	1	0
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	1	1
1	0	1	1	1	1
1	1	0	1	1	1
1	1	1	1	0	0

Section 4-2 Laws and Rules of Boolean Algebra

7. (a) Commutative law of addition
 (b) Commutative law of multiplication
 (c) Distributive law
8. Refer to Table 4-1 in the textbook.

- (a) Rule 9: $\overline{\overline{A}} = A$
 (b) Rule 8: $\overline{AA} = 0$ (applied to 1st and 3rd terms)
 (c) Rule 5: $A + A = A$
 (d) Rule 6: $A + \overline{A} = 1$
 (e) Rule 10: $A + AB = A$
 (f) Rule 11: $A + \overline{AB} = A + B$ (applied to 1st and 3rd terms)

Section 4-3 DeMorgan's Theorems

9.

- (a) $\overline{\overline{A+B}} = \overline{\overline{A}\overline{B}} = \overline{AB}$
- (b) $\overline{\overline{AB}} = \overline{A} + \overline{\overline{B}} = A + \overline{B}$
- (c) $\overline{\overline{A+B+C}} = \overline{\overline{ABC}}$
- (d) $\overline{\overline{ABC}} = \overline{A} + \overline{\overline{B}} + \overline{\overline{C}}$
- (e) $\overline{\overline{A(B+C)}} = \overline{\overline{A}} + \overline{\overline{(B+C)}} = \overline{A} + \overline{B}\overline{C}$
- (f) $\overline{\overline{AB} + \overline{CD}} = \overline{\overline{A} + \overline{B}} + \overline{\overline{C} + \overline{D}}$
- (g) $\overline{\overline{AB} + \overline{CD}} = (\overline{AB})(\overline{CD}) = (\overline{A} + \overline{B})(\overline{C} + \overline{D})$
- (h) $\overline{\overline{(A+B)(C+D)}} = \overline{\overline{A} + \overline{B}} + \overline{\overline{C} + \overline{D}} = \overline{AB} + \overline{CD}$

10.

- (a) $\overline{\overline{AB}(C+\overline{D})} = \overline{\overline{AB}} + \overline{\overline{(C+\overline{D})}} = \overline{A} + \overline{B} + \overline{CD}$
- (b) $\overline{\overline{AB(CD+EF)}} = \overline{\overline{AB}} + \overline{\overline{(CD+EF)}} = \overline{A} + \overline{B} + \overline{\overline{(CD)}}\overline{\overline{(EF)}}$
 $= \overline{A} + \overline{B} + (\overline{C} + \overline{D})(\overline{E} + \overline{F})$
- (c) $\overline{\overline{(A+\overline{B}+C+\overline{D})}} + \overline{\overline{ABCD}} = \overline{ABC}\overline{D} + \overline{A} + \overline{B} + \overline{C} + \overline{D}$
- (d) $\overline{\overline{(A+B+C+D)(ABCD)}} = \overline{\overline{(AB}\overline{CD)}}(\overline{A} + \overline{B} + \overline{C} + \overline{D})$
 $= \overline{\overline{AB}\overline{CD}} + \overline{\overline{A} + \overline{B} + \overline{C} + \overline{D}} = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{ABC}\overline{D}$
- (e) $\overline{\overline{AB(CD+\overline{EF})}}\overline{\overline{(AB+CD)}} = \overline{\overline{AB}} + \overline{\overline{(CD+\overline{EF})}} + \overline{\overline{(AB+CD)}}$
 $= AB + (\overline{CD})(\overline{EF}) + (\overline{AB})(\overline{CD})$
 $= AB + (\overline{C} + \overline{D})(E + \overline{F}) + ABCD$

11.

- (a) $\overline{\overline{(ABC)}\overline{\overline{(EFG)}}} + \overline{\overline{(HIJ)}\overline{\overline{(KLM)}}} = \overline{\overline{ABC}} + \overline{\overline{EFG}} + \overline{\overline{HIJ}} + \overline{\overline{KLM}}$
 $= \overline{\overline{ABC}} + \overline{\overline{EFG}} + \overline{\overline{HIJ}} + \overline{\overline{KLM}} = (\overline{ABC})(\overline{EFG})(\overline{HIJ})(\overline{KLM})$
 $= (\overline{A} + \overline{B} + \overline{C})(\overline{E} + \overline{F} + \overline{G})(\overline{H} + \overline{I} + \overline{J})(\overline{K} + \overline{L} + \overline{M})$
- (b) $\overline{\overline{(A+B\overline{C}+CD)}} + \overline{\overline{BC}} = \overline{A}(\overline{B}\overline{C})(\overline{CD}) + BC = \overline{A}(\overline{B}\overline{C})(\overline{CD}) + BC$
 $= \overline{ABC}(\overline{C} + \overline{D}) + BC = \overline{ABC} + \overline{ABC}\overline{D} + BC = \overline{ABC}(1 + \overline{D}) + BC$
 $= \overline{ABC} + BC$
- (c) $\overline{\overline{(A+B)(C+D)}}\overline{\overline{(E+F)(G+H)}}$
 $= (\overline{A} + \overline{B})(\overline{C} + \overline{D})(\overline{E} + \overline{F})(\overline{G} + \overline{H}) = \overline{ABC}\overline{D}\overline{E}\overline{F}\overline{GH}$

Chapter 4

Section 4-4 Boolean Analysis of Logic Circuits

12. (a) $AB = X$
 (b) $\overline{A} = X$
 (c) $A + B = X$
 (d) $A + B + C = X$

13. See Figure 4-1.

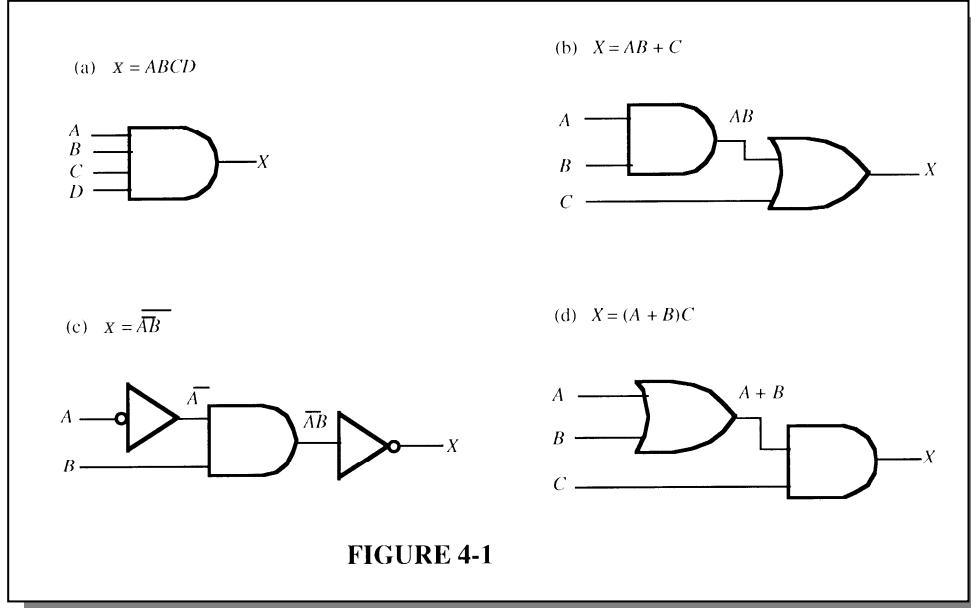


FIGURE 4-1

14. See Figure 4-2.

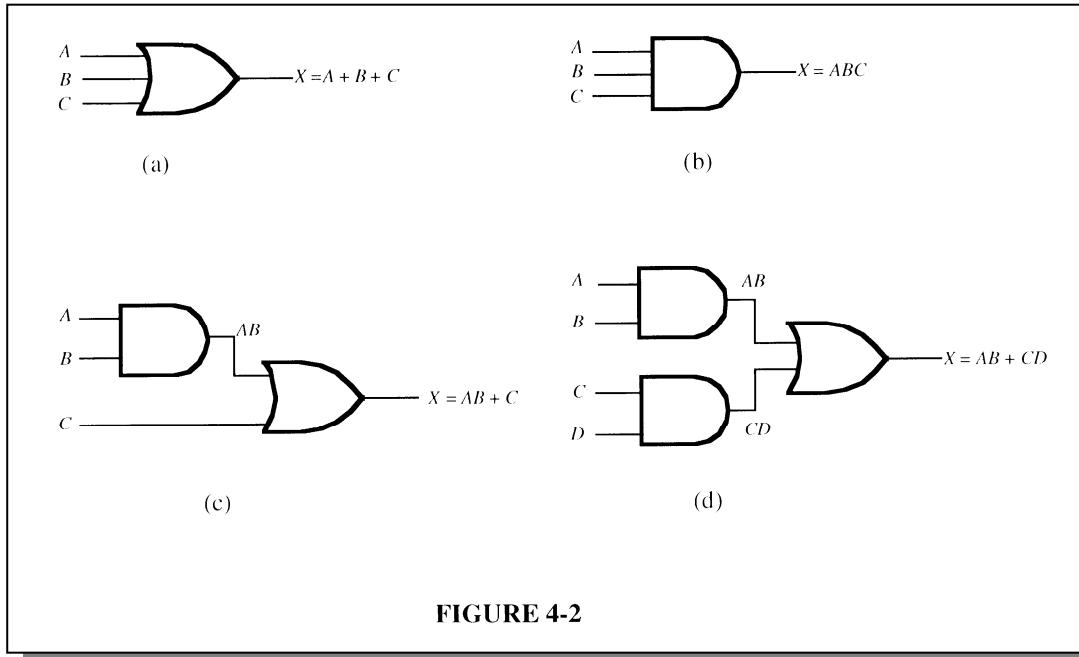


FIGURE 4-2

15. See Figure 4-3.

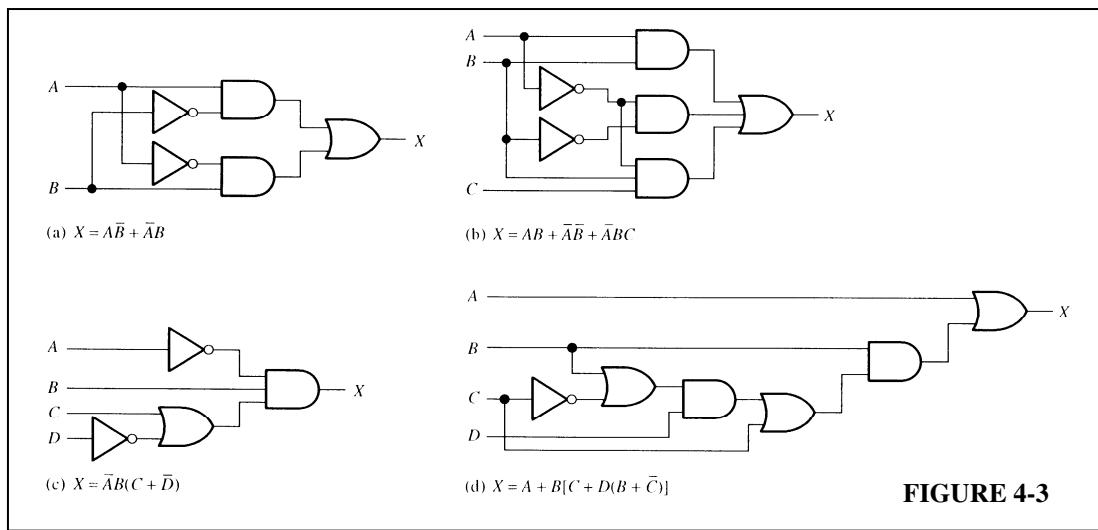


FIGURE 4-3

16. (a) See Figure 4-4(a).
 (b) See Figure 4-4(b).

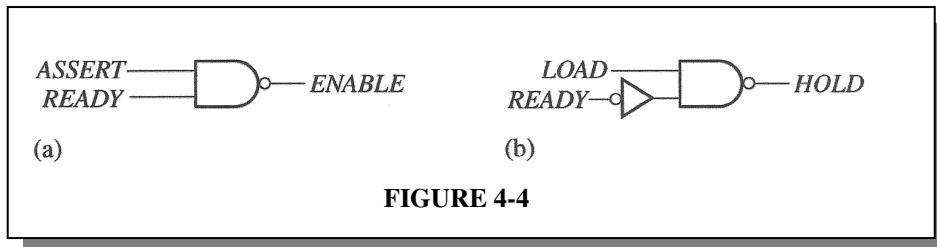


FIGURE 4-4

17. See Tables 4-1 and 402

Table 4-1

INPUTS			OUTPUT
<i>VCR</i>	<i>CAMI</i>	<i>RDY</i>	<i>RECORD</i>
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Table 4-2

INPUTS			OUTPUT
<i>RTS</i>	<i>ENABLE</i>	<i>BUSY</i>	<i>SEND</i>
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

Chapter 4

18. (a) $X = A + B$

A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

(b) $X = AB$

A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

(c) $X = AB + BC$

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

(d) $X = (A + B)C$

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

(e) $X = (A + B)(\bar{B} + C)$

A	B	C	$A + B$	$\bar{B} + C$	X
0	0	0	0	1	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	1	1	1
1	0	0	1	1	1
1	0	1	1	1	1
1	1	0	1	0	0
1	1	1	1	1	1

Section 4-5 Simplification Using Boolean Algebra

19. (a) $A(A + B) = AA + BB = A + AB = A(1 + B) = A$

(b) $A(\bar{A} + AB) = A\bar{A} + AAB = 0 + AB = AB$

(c) $BC + \bar{B}C = C(B + \bar{B}) = C(1) = C$

(d) $A(A + \bar{A}B) = AA + A\bar{A}B = A + (0)B = A + 0 = A$

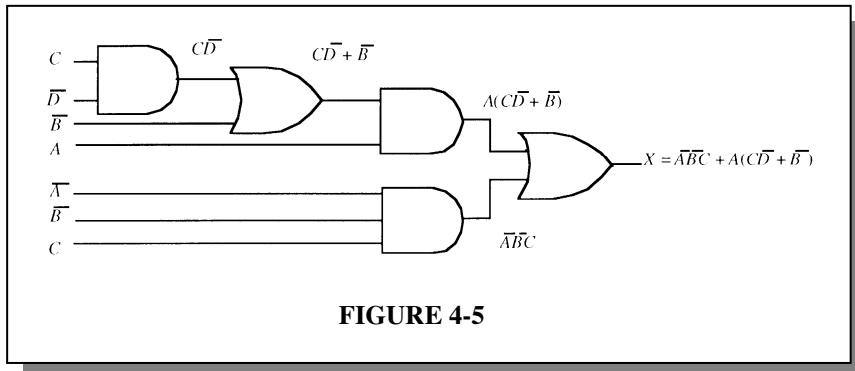
(e) $\bar{A}\bar{B}C + \bar{A}BC + \bar{A}\bar{B}C = \bar{A}\bar{B}C + \bar{A}C(B + \bar{B}) = \bar{A}\bar{B}C + \bar{A}C(1)$
 $= \bar{A}\bar{B}C + \bar{A}C = C(\bar{A} + \bar{A}B) = C(\bar{A} + \bar{B}) = \bar{A}C + \bar{B}C$

- 20.** (a)
$$\begin{aligned} (A + \bar{B})(A + C) &= AA + AC + A\bar{B} + \bar{B}C = A + AC + A\bar{B} + \bar{B}C \\ &= A(1 + C + \bar{B}) + \bar{B}C = A(1) + \bar{B}C = \mathbf{A} + \bar{\mathbf{B}}\mathbf{C} \end{aligned}$$
- (b)
$$\begin{aligned} \bar{A}\bar{B} + \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D}\bar{E} &= \bar{A}\bar{B}(1 + \bar{C} + \bar{C}\bar{D} + \bar{C}\bar{D}\bar{E}) = \bar{A}\bar{B}(1) \\ &= \bar{\mathbf{A}}\mathbf{B} \end{aligned}$$
- (c)
$$\begin{aligned} AB + \bar{A}\bar{B}\bar{C} + A &= AB + (\bar{A} + \bar{B})C + A = AB + \bar{A}\bar{C} + \bar{B}C + A \\ A(B + 1) + \bar{A}\bar{C} + \bar{B}C &= A + \bar{A}\bar{C} + \bar{B}C = A + C + \bar{B}C = A + C(1 + \bar{B}) \\ &= \mathbf{A} + \mathbf{C} \end{aligned}$$
- (d)
$$\begin{aligned} (A + \bar{A})(AB + A\bar{B}\bar{C}) &= AAB + AAB\bar{C} + \bar{A}AB + \bar{A}ABC \\ &= AB + A\bar{B}\bar{C} + 0 + 0 = AB(1 + \bar{C}) = \mathbf{AB} \end{aligned}$$
- (e)
$$\begin{aligned} AB + (\bar{A} + \bar{B})C + AB &= AB + \bar{A}\bar{C} + \bar{B}C + AB = AB + (\bar{A} + \bar{B})C \\ &= AB + \bar{A}\bar{B}\bar{C} = \mathbf{AB} + \mathbf{C} \end{aligned}$$
- 21.** (a)
$$\begin{aligned} BD + B(D + E) + \bar{D}(D + F) &= BD + BD + BE + \bar{D}D + \bar{D}F \\ &= BD + BE + 0 + \bar{D}F = \mathbf{BD} + \mathbf{BE} + \bar{\mathbf{D}}\mathbf{F} \end{aligned}$$
- (b)
$$\begin{aligned} \bar{A}\bar{B}\bar{C} + (\bar{A} + \bar{B} + \bar{C}) + \bar{A}\bar{B}\bar{C}\bar{D} &= \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C}\bar{D} = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C}\bar{D} \\ &= \bar{A}\bar{B}(C + \bar{C}\bar{D}) = \bar{A}\bar{B}(C + D) = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{D} \end{aligned}$$
- (c)
$$\begin{aligned} (B + BC)(B + \bar{B}C)(B + D) &= B(1 + C)(B + C)(B + D) \\ &= B(B + C)(B + D) = (BB + BC)(B + D) = (B + BC)(B + D) \\ &= B(1 + C)(B + D) = B(B + D) = BB + BD = B + BD = B(1 + D) = \mathbf{B} \end{aligned}$$
- (d)
$$\begin{aligned} ABCD + AB(\bar{C}\bar{D}) + (\bar{A}\bar{B})CD &= ABCD + AB(\bar{C} + \bar{D}) + (\bar{A} + \bar{B})CD \\ &= ABCD + AB\bar{C} + AB\bar{D} + \bar{A}CD + \bar{B}CD \\ &= CD(AB + \bar{A} + \bar{B}) + AB\bar{C} + AB\bar{D} = CD(B + \bar{A} + \bar{B}) + AB\bar{C} + AB\bar{D} \\ &= CD(1 + \bar{A}) + AB\bar{C} + AB\bar{D} = CD + AB\bar{C} + AB\bar{D} = CD + AB(\bar{C}\bar{D}) = \mathbf{CD} + \mathbf{AB} \end{aligned}$$
- (e)
$$\begin{aligned} ABC[AB + \bar{C}(BC + AC)] &= ABABC + ABC\bar{C}(BC + AC) \\ &= ABC + 0(BC + AC) = \mathbf{ABC} \end{aligned}$$

Chapter 4

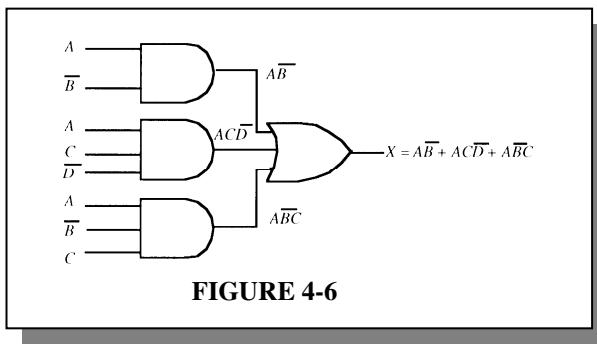
22. First develop the Boolean expression for the output of each gate network and simplify.

(a) See Figure 4-5.



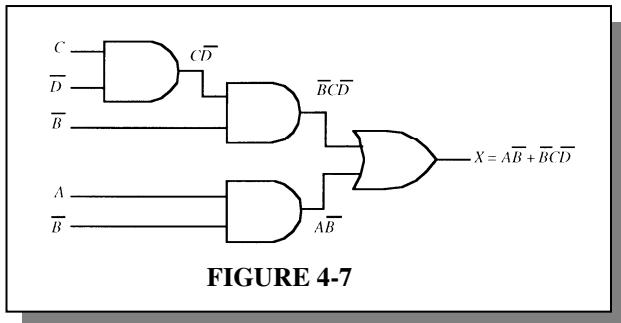
$$\begin{aligned} X &= \overline{ABC} + A(\overline{CD} + \overline{B}) = \overline{ABC} + A\overline{C}\overline{D} + A\overline{B} = \overline{B}(A + \overline{AC}) + A\overline{CD} \\ &= \overline{B}(A + C) + A\overline{CD} = \overline{AB} + \overline{BC} + A\overline{CD} \end{aligned}$$

(b) See Figure 4-6.



$$X = \overline{AB} + A\overline{CD} + \overline{ABC} = \overline{AB}(1+C) + A\overline{CD} = \overline{AB} + A\overline{CD}$$

(c) See Figure 4-7.



$$X = \overline{AB} + \overline{BCD} \quad \text{No further simplification is possible.}$$

- (d) See Figure 4-8.

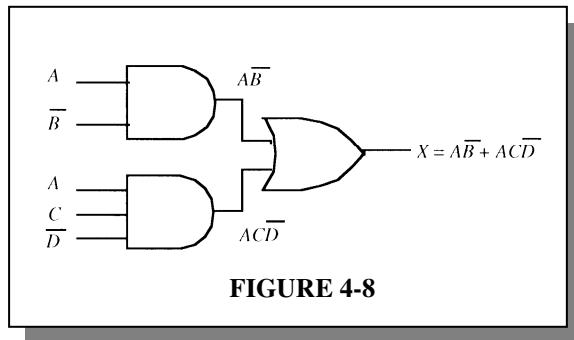


FIGURE 4-8

$X = AB̄ + AC̄D$ No further simplification is possible.

Section 4-6 Standard Forms of Boolean Expressions

- 23.** (a) $(A + B)(C + \bar{B}) = AC + BC + B\bar{B} + A\bar{B} = AC + BC + A\bar{B}$
 (b) $(A + \bar{B}C)C = AC + \bar{B}CC = AC + \bar{B}C$
 (c) $(A + C)(AB + AC) = AAB + AAC + ABC + ACC = AB + AC + ABC + ACC$
 $= (AB + AC)(1 + C) = AB + AC$
- 24.** (a) $AB + CD(A\bar{B} + CD) = AB + A\bar{B}CD + CD\bar{C}D = AB + A\bar{B}CD + CD$
 $= AB(A\bar{B} + 1)CD = AB + CD$
 (b) $AB(\bar{B}\bar{C} + BD) = A\bar{B}\bar{B}\bar{C} + ABB\bar{D} = 0 + ABD = ABD$
 (c) $A + B[AC + (B + \bar{C})D] = A + ABC + (B + \bar{C})BD$
 $= A + ABC + BD + B\bar{C}D = A(1 + BC) + BD + B\bar{C}D = A + BD(1 + \bar{C})$
 $= A + BD$
- 25.** (a) The domain is A, B, C
 The standard SOP is: $\bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C} + ABC + \bar{A}\bar{B}C$
 (b) The domain is A, B, C
 The standard SOP is: $ABC + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}$
 (c) The domain is A, B, C
 The standard SOP is: $ABC + A\bar{B}\bar{C} + A\bar{B}C$
- 26.** (a) $AB + CD = ABCD + ABC\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}BCD + A\bar{B}CD$
 (b) $ABD = ABCD + A\bar{B}\bar{C}D$
 (c) $A + BD = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D}$
 $+ ABC\bar{D} + ABCD + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}CD$
- 27.** (a) $\bar{A}\bar{B}C + A\bar{B}\bar{C} + ABC + \bar{A}\bar{B}C : 101 + 100 + 111 + 011$
 (b) $ABC + A\bar{B}\bar{C} + \bar{A}\bar{B}C : 111 + 101 + 001$
 (c) $ABC + A\bar{B}\bar{C} + A\bar{B}C : 111 + 110 + 101$

Chapter 4

- 28.** (a) $ABCD + ABC\bar{D} + AB\bar{C}D + A\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}\bar{D}$:
 $1111 + 1110 + 1101 + 1100 + 0011 + 0111 + 1011$
- (b) $ABCD + AB\bar{C}D$: $1111 + 1101$
- (c) $A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D + A\bar{B}CD + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}D$
 $+ ABC\bar{D} + ABCD + \bar{ABC}\bar{D} + \bar{ABC}D$:
 $1000 + 1001 + 1010 + 1011 + 1100 + 1101 + 1110 + 1111 + 0101 + 0111$
- 29.** (a) $(A + B + C)(A + B + \bar{C})(A + \bar{B} + C)(\bar{A} + \bar{B} + C)$
(b) $(A + B + C)(A + \bar{B} + C)(A + \bar{B} + \bar{C})(\bar{A} + B + C)(\bar{A} + \bar{B} + C)$
(c) $(A + B + C)(A + B + \bar{C})(A + \bar{B} + C)(A + \bar{B} + \bar{C})(\bar{A} + B + C)$
- 30.** (a) $(A + B + C + D)(A + B + C + \bar{D})(A + B + \bar{C} + D)(A + \bar{B} + C + D)(A + \bar{B} + C + \bar{D})$
 $(A + \bar{B} + \bar{C} + D)(\bar{A} + B + C + D)(\bar{A} + B + C + \bar{D})(\bar{A} + B + \bar{C} + D)$
- (b) $(A + B + C + D)(A + B + C + \bar{D})(A + B + \bar{C} + D)(A + B + \bar{C} + \bar{D})$
 $(A + \bar{B} + C + D)(A + \bar{B} + C + \bar{D})(A + \bar{B} + \bar{C} + D)(A + \bar{B} + \bar{C} + \bar{D})(\bar{A} + B + C + D)$
 $(\bar{A} + B + C + \bar{D})(\bar{A} + B + \bar{C} + D)(\bar{A} + B + \bar{C} + \bar{D})(\bar{A} + \bar{B} + C + D)(\bar{A} + \bar{B} + \bar{C} + D)$
- (c) $(A + B + C + D)(A + B + C + \bar{D})(A + B + \bar{C} + D)(A + B + \bar{C} + \bar{D})$
 $(A + \bar{B} + C + D)(A + \bar{B} + \bar{C} + D)$

Section 4-7 Boolean Expressions and Truth Tables

- 31.** (a)

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

- (b)

X	Y	Z	Q
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

32. (a)

A	B	C	D	X
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

(b)

W	X	Y	Z	Q
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

33. (a) $\overline{AB} + A\overline{B}\overline{C} + \overline{A}\overline{C} + A\overline{B}C = \overline{ABC} + \overline{ABC} + A\overline{B}\overline{C} + \overline{ABC} + A\overline{B}\overline{C} + A\overline{B}C$

$$\begin{aligned}
 \text{(b)} \quad & \overline{X} + Y\overline{Z} + WZ + X\overline{YZ} = \overline{W}\overline{X}\overline{Y}\overline{Z} + \overline{W}\overline{X}\overline{Y}Z + \overline{W}\overline{X}Y\overline{Z} + \overline{W}\overline{X}YZ \\
 & + \overline{WX}\overline{YZ} + \overline{WX}Y\overline{Z} + W\overline{X}\overline{Y}\overline{Z} + W\overline{X}\overline{Y}Z \\
 & + W\overline{X}\overline{Y}\overline{Z} + W\overline{X}YZ + WX\overline{YZ} + WXY\overline{Z} + WXYZ
 \end{aligned}$$

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

W	X	Y	Z	Q
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Chapter 4

34. (a)

A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

(b)

A	B	C	D	X
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

35. (a)

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

(b)

A	B	C	D	X
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

36. (a) $X = \overline{A}\overline{B}C + A\overline{B}\overline{C} + A\overline{B}C + ABC$

$$X = (A + B + C)(A + \overline{B} + C)(A + \overline{B} + \overline{C})(\overline{A} + \overline{B} + C)$$

(b) $X = A\overline{B}\overline{C} + A\overline{B}C + ABC$

$$X = (A + B + C)(A + B + \overline{C})(A + \overline{B} + C)(A + \overline{B} + \overline{C})(\overline{A} + B + C)$$

(c) $X = \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}D + \overline{A}\overline{B}CD + \overline{A}\overline{B}C\overline{D} + \overline{A}\overline{B}CD + \overline{A}\overline{B}C\overline{D} + ABC\overline{D}$

$$X = (A + B + \overline{C} + D)(A + \overline{B} + C + D)(A + \overline{B} + \overline{C} + \overline{D})(\overline{A} + B + C + D)(\overline{A} + B + \overline{C} + D)$$

$$(\overline{A} + B + \overline{C} + \overline{D})(\overline{A} + \overline{B} + C + \overline{D})(\overline{A} + \overline{B} + \overline{C} + D)(\overline{A} + \overline{B} + \overline{C} + \overline{D})$$

$$\begin{aligned}
 (d) \quad X &= \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}D + \overline{A}\overline{B}CD + A\overline{B}\overline{C}D + A\overline{B}\overline{C}\overline{D} + ABCD \\
 X &= (A+B+C+D)(A+B+C+\overline{D})(A+B+\overline{C}+\overline{D})(A+\overline{B}+\overline{C}+D)(\overline{A}+B+C+D) \\
 &\quad (\overline{A}+B+C+\overline{D})(\overline{A}+B+\overline{C}+D)(\overline{A}+\overline{B}+C+\overline{D})(\overline{A}+\overline{B}+\overline{C}+D)
 \end{aligned}$$

Section 4-8 The Karnaugh Map

37. See Figure 4-9.

38. See Figure 4-10.

39. See Figure 4-11.

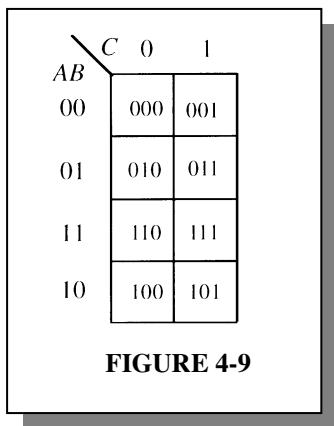


FIGURE 4-9

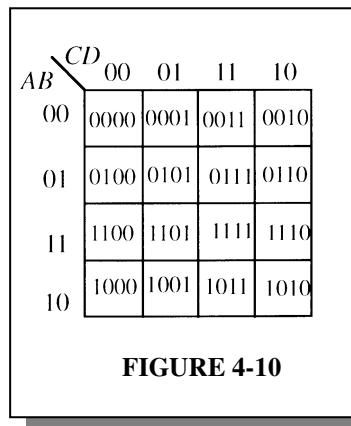


FIGURE 4-10

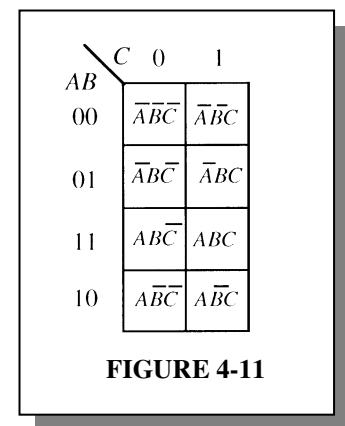


FIGURE 4-11

Section 4-9 Karnaugh Map SOP Minimization

40. See Figure 4-12.

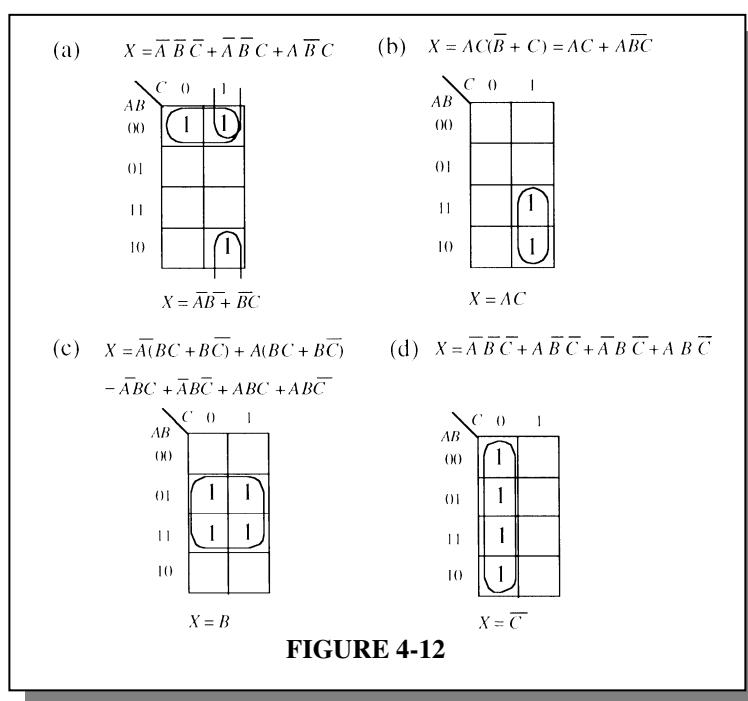
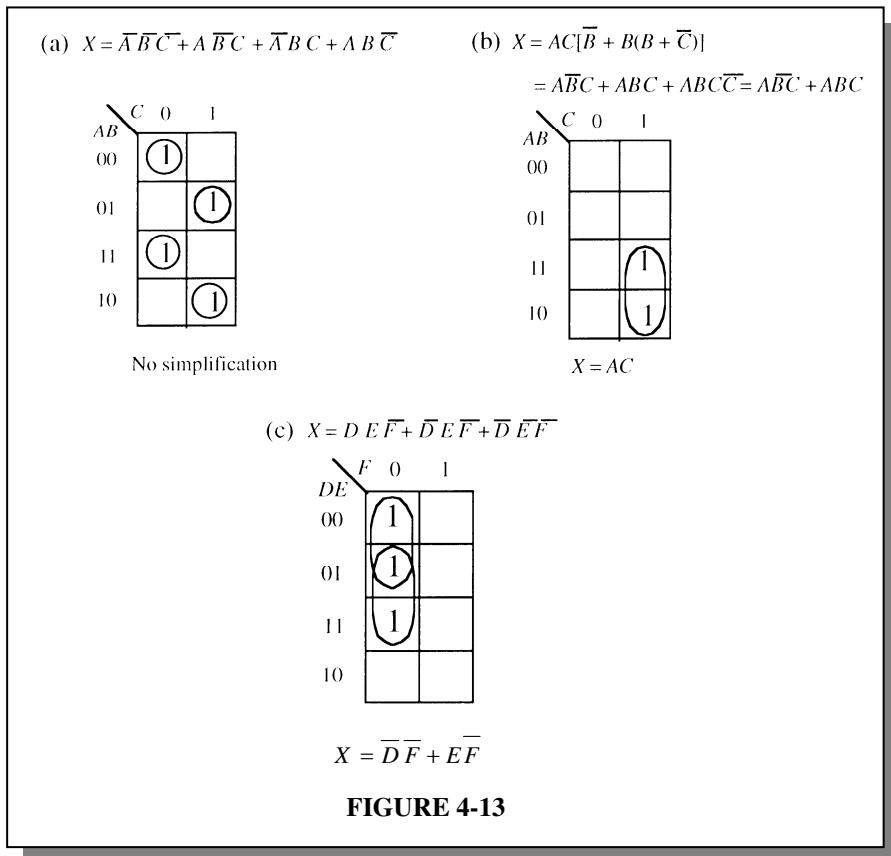


FIGURE 4-12

Chapter 4

41. See Figure 4-13.



42. (a) $AB + A\overline{B}C + ABC = AB(C + \overline{C}) + \overline{A}\overline{B}C + ABC$
 $= ABC + A\overline{B}\overline{C} + \overline{A}\overline{B}C + ABC$
 $= ABC + A\overline{B}\overline{C} + A\overline{B}C$
- (b) $A + BC = A(B + \overline{B})(C + \overline{C}) + (\overline{A} + A)BC = (AB + A\overline{B})(C + \overline{C}) + (\overline{A} + A)BC$
 $= ABC + A\overline{B}\overline{C} + A\overline{B}C + \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}C + ABC$
 $= ABC + A\overline{B}\overline{C} + A\overline{B}C + \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}C$
- (c) $A\overline{B}\overline{C}D + A\overline{C}\overline{D} + B\overline{C}D + \overline{A}\overline{B}CD$
 $= A\overline{B}\overline{C}D + A(B + \overline{B})CD + (A + \overline{A})B\overline{C}D + \overline{A}\overline{B}CD =$
 $= A\overline{B}\overline{C}D + ABCD + A\overline{B}CD + B\overline{C}D + \overline{A}\overline{B}CD + \overline{A}\overline{B}CD$
- (d) $A\overline{B} + A\overline{B}\overline{C}D + CD + B\overline{C}D + ABCD$
 $= A\overline{B}(C + \overline{C})(D + \overline{D}) + A\overline{B}\overline{C}D + (A + \overline{A})(B + \overline{B})CD + (A + \overline{A})B\overline{C}D + ABCD$
 $= A\overline{B}\overline{C}\overline{D} + A\overline{B}\overline{C}D + ABC\overline{D} + ABCD + A\overline{B}\overline{C}D + A\overline{B}CD + A\overline{B}CD + A\overline{B}CD$
 $+ A\overline{B}CD + A\overline{B}CD + A\overline{B}CD + ABCD$
 $= A\overline{B}\overline{C}\overline{D} + A\overline{B}\overline{C}D + ABC\overline{D} + ABCD + A\overline{B}\overline{C}D + A\overline{B}CD + A\overline{B}CD + A\overline{B}CD$
 $= A\overline{B}\overline{C}D + A\overline{B}\overline{C}D + A\overline{B}CD + A\overline{B}CD + A\overline{B}CD + A\overline{B}CD + A\overline{B}CD + ABCD + ABCD$

43. See Figure 4-14.

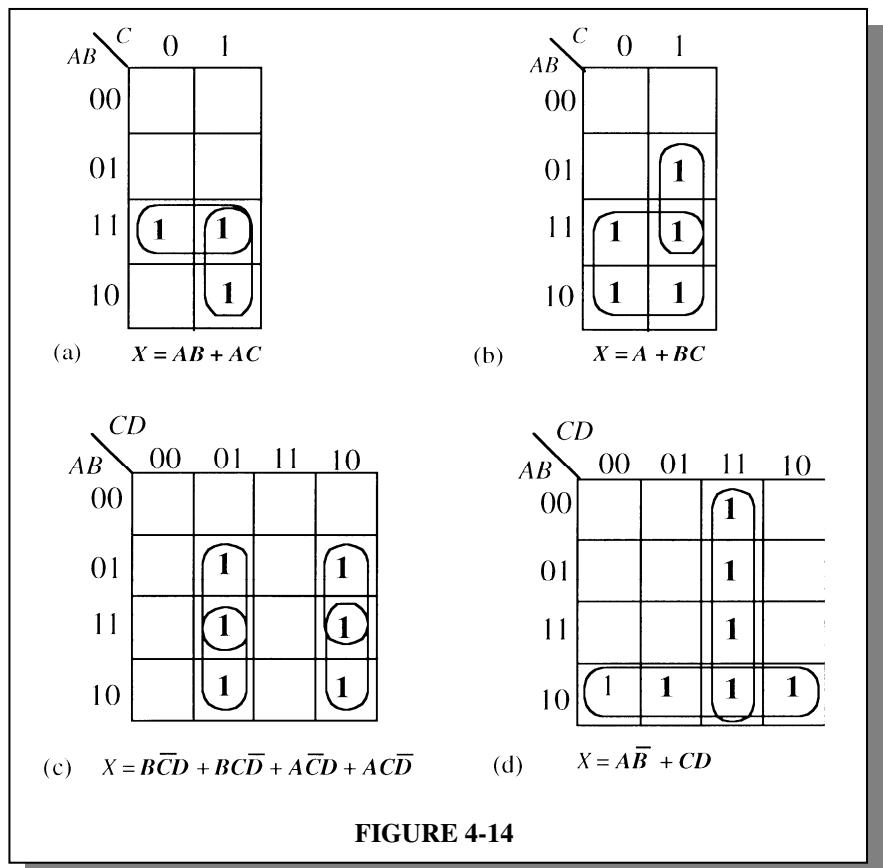


FIGURE 4-14

44. See Figure 4-15.

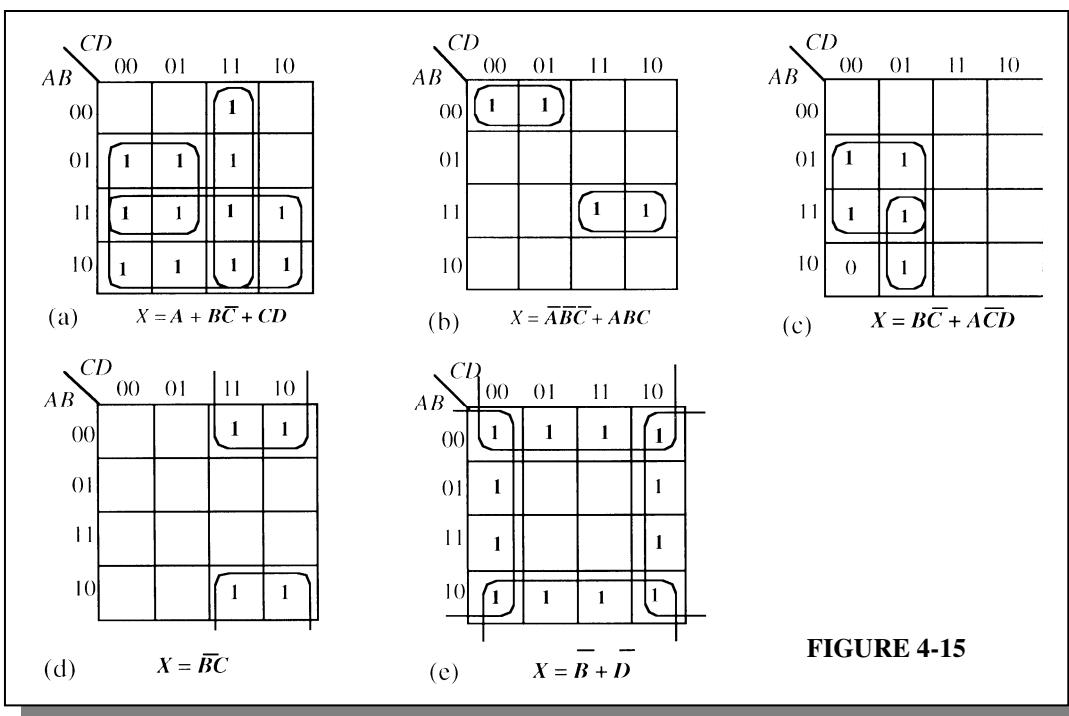
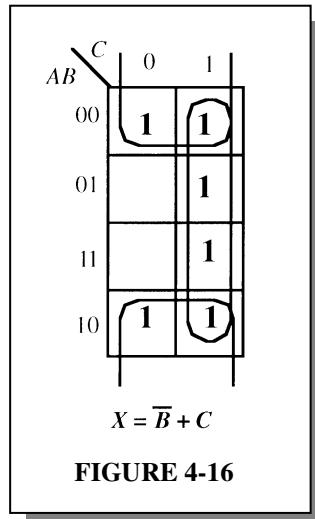


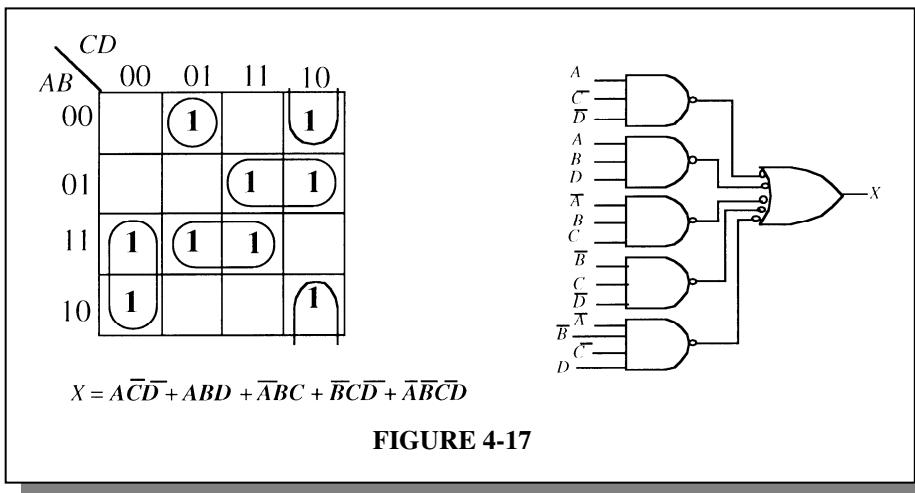
FIGURE 4-15

Chapter 4

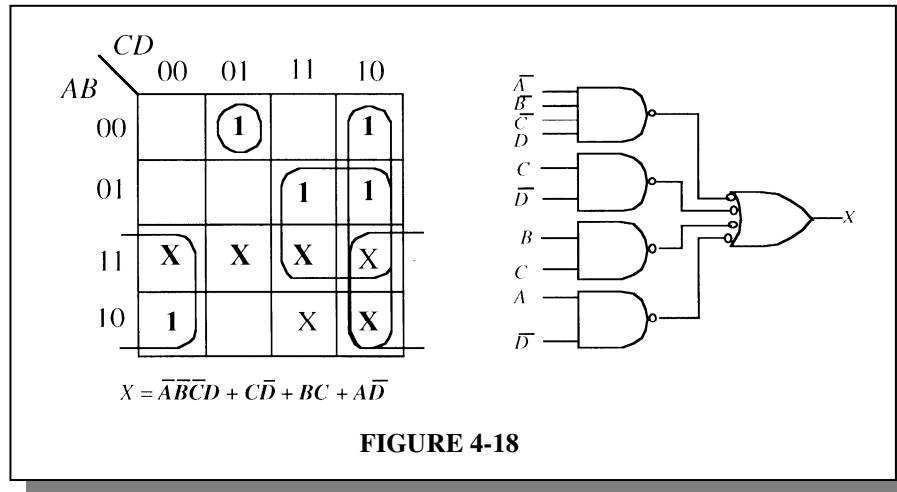
45. Plot the 1's from Figure 4-11 in the text on the map as shown in Figure 4-16 and simplify.



46. Plot the 1's from Figure 4-12 in the text on the map as shown in Figure 4-17 and simplify.



47. See Figure 4-18.



Section 4-10 Karnaugh Map POS Minimization

48. (a) $(A + B + C)(\bar{A} + \bar{B} + \bar{C})(A + \bar{B} + C)$

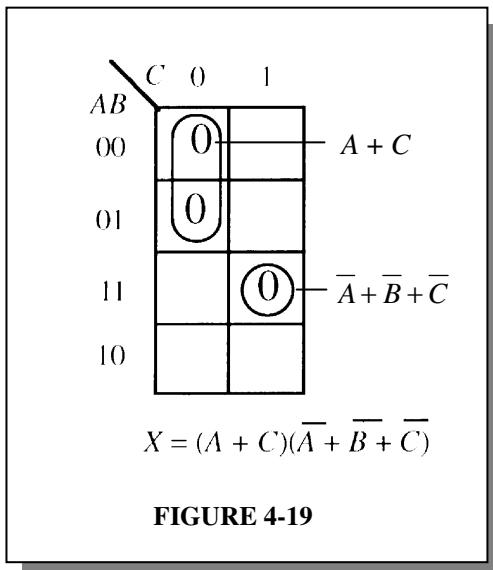


FIGURE 4-19

$$\begin{aligned}
 (b) \quad & (X + \bar{Y})(\bar{X} + Z)(X + \bar{Y} + \bar{Z})(\bar{X} + \bar{Y} + \bar{Z}) \\
 &= (X + \bar{Y} + Z)(X + \bar{Y} + \bar{Z})(\bar{X} + \bar{Y} + Z)(\bar{X} + Y + Z) \\
 &\quad \cancel{(X + \bar{Y} + \bar{Z})} \quad \cancel{(\bar{X} + \bar{Y} + Z)}
 \end{aligned}$$

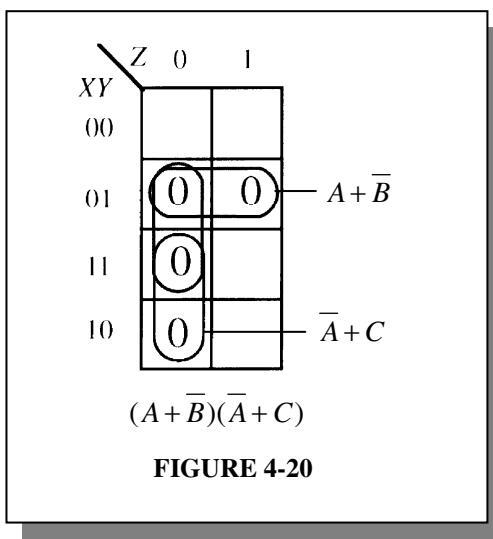


FIGURE 4-20

Chapter 4

$$\begin{aligned}
 (c) \quad & A(B + \bar{C})(\bar{A} + C)(A + \bar{B} + C)(\bar{A} + B + \bar{C}) \\
 & = (A + B + C)(A + \bar{B} + C)(A + \bar{B} + \bar{C})(A + B + \bar{C}) \\
 & \quad \cancel{(A + B + C)} (\bar{A} + B + \bar{C})(\bar{A} + B + C)(\bar{A} + \bar{B} + C) \\
 & \quad \cancel{(A + \bar{B} + C)} \cancel{(\bar{A} + B + \bar{C})}
 \end{aligned}$$

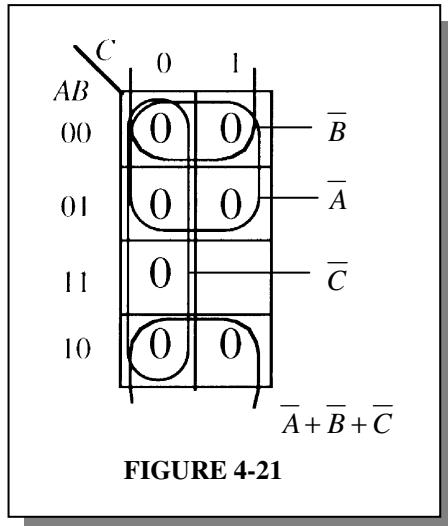


FIGURE 4-21

49. (a) $(A + \bar{B} + C + \bar{D})(\bar{A} + B + \bar{C} + D)(A + \bar{B} + \bar{C} + \bar{D})$

0101	1010	1111
------	------	------

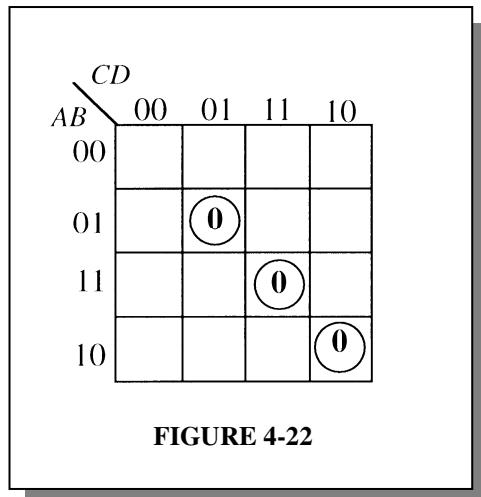
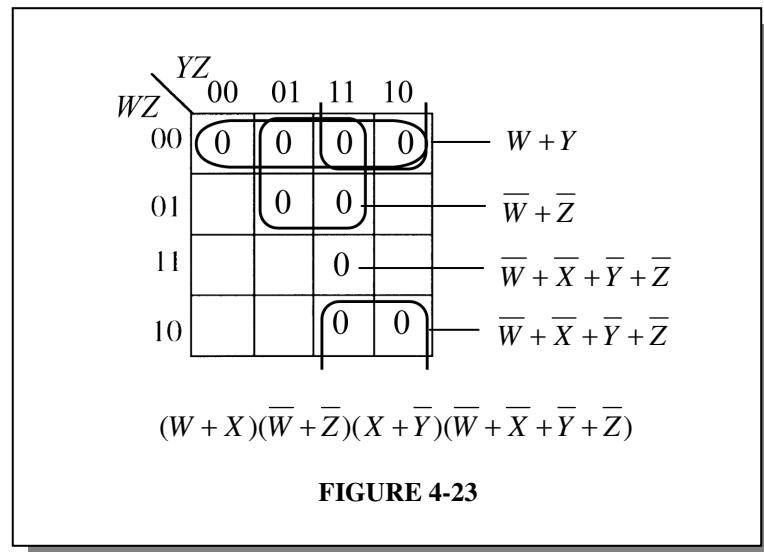


FIGURE 4-22

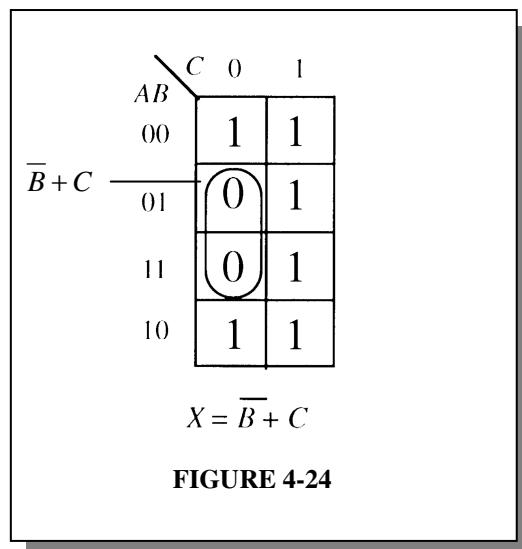
No reduction

$$\begin{aligned}
 (b) \quad & (X + \bar{Y})(W + \bar{Z})(\bar{X} + \bar{Y} + \bar{Z})(W + X + Y + Z) \\
 & = (W + X + \bar{Y} + Z)(\bar{W} + X + \bar{Y} + \bar{Z})(W + X + \bar{Y} + \bar{Z})(\bar{W} + X + \bar{Y} + Z) \\
 & (\bar{W} + \bar{X} + \bar{Y} + \bar{Z})(W + \bar{X} + Y + \bar{Z}) \cancel{(W + X + \bar{Y} + Z)} (W + X + Y + \bar{Z}) \\
 & (\bar{W} + \bar{X} + \bar{Y} + \bar{Z}) \cancel{(W + \bar{X} + \bar{Y} + Z)} (W + X + Y + Z)
 \end{aligned}$$



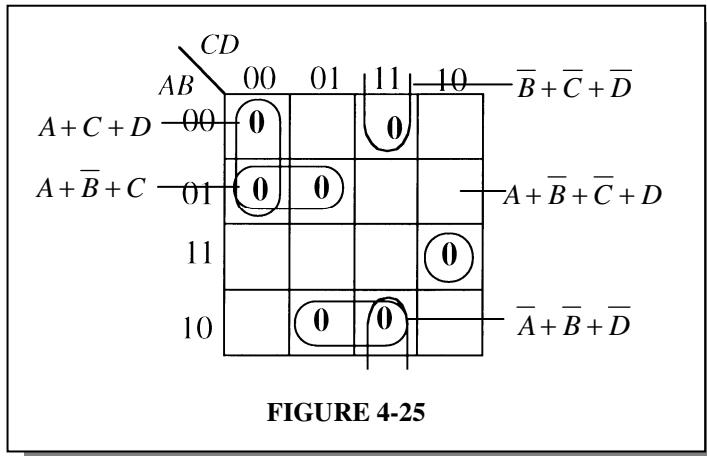
50. From Table 4-17.

$$SOP = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}\bar{C} + A\bar{B}C + ABC$$



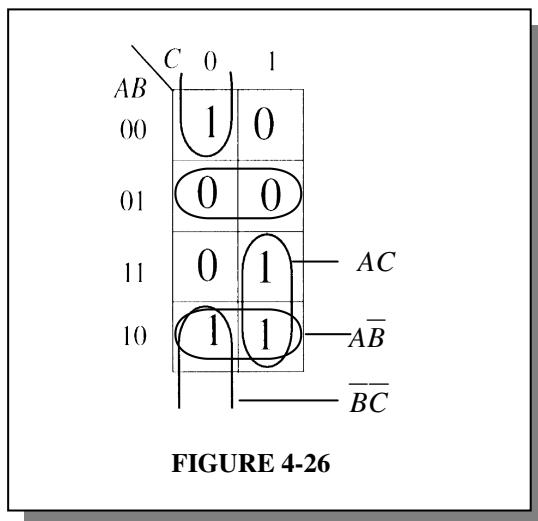
Chapter 4

51. From Table 4-17.



$$(\bar{A} + B + \bar{D})(A + C + D)(A + \bar{B} + C)(B + \bar{C} + \bar{D})(A + \bar{B} + \bar{C} + D)$$

52. (a) $(A + \bar{B})(A + \bar{C})(\bar{A} + B + \bar{D})(\bar{A} + \bar{B} + C)$
 $(A + \bar{B} + \bar{C})(A + \bar{B} + C) \cancel{(A + \bar{B} + C)} (A + B + \bar{C})(\bar{A} + \bar{B} + C)$



$$AC + A\bar{B} + \bar{B}\bar{C}$$

Section 4-11 The Quine-McCluskey Method

53. $X = ABC + \overline{A}\overline{B}C + A\overline{B}\overline{C} + A\overline{B}C + \overline{A}BC$

ABC	X	Minterm
000	0	
001	1	m_1
010	0	
011	1	m_3
100	0	
101	1	m_5
110	1	m_6
111	1	m_7

Minterms 1, 3, 5, 6, 7

54. $X = \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}\overline{C}D + \overline{A}\overline{B}CD + ABC\overline{D} + \overline{ABC}\overline{D} + A\overline{B}\overline{C}D$

$ABCD$	X	Minterm
0000	1	m_0
0001	1	m_1
0010	0	
0011	0	
0100	0	
0101	1	m_5
0110	1	m_6
0111	0	
1000	0	
1001	1	m_9
1010	0	
1011	0	
1100	1	m_{12}
1101	0	
1110	0	
1111	0	

55.

Number of 1s	Minterm	ABCD
0	m_0	0000
1	m_1	0001
2	m_5	0101
	m_6	0110
	m_9	1001
	m_{12}	1100

Chapter 4

56.

Number of 1s	Minterm	ABCD	First Level
0	m_0	0000	$(m_0, m_1) 000X$
1	m_1	0001 ✓	$(m_1, m_5) 0X01$
2	m_5	0101 ✓	
	m_6	0110	
	m_9	1001 ✓	$(m_1, m_9) X001$
	m_{12}	1100	

57.

First Level	Number of 1s	Second Level
$(m_0, m_1) 000X$		$(m_0, m_1) 000X$
$(m_1, m_5) 0X01$	1	$(m_1, m_5, m_9) XX01$
$(m_1, m_9) X001$		

58.

Prime Implicants	m_0	m_1	m_5	m_6	m_9	m_{12}
$\overline{A}\overline{B}\overline{C} (m_0m_1)$	✓	✓				✓
$\overline{C}\overline{D} (m_0m_5m_9)$			✓	✓		
$\overline{A}\overline{B}\overline{C}\overline{D} (m_6)$					✓	
$A\overline{B}\overline{C}\overline{D} (m_{12})$						✓

59. $X = \overline{C}\overline{D} + \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}\overline{C}\overline{D} + A\overline{B}\overline{C}\overline{D}$

Section 4-12 Boolean Expressions with VHDL

60. entity AND_OR is
 port (A, B, C, D, E, F, G, H, I: **in** bit; X: **out** bit);
 end entity AND_OR;
 architecture Logic of AND_OR is
 begin
 X <= (A and B and C) or (D and E and F) or (G and H and I);
 end architecture Logic;

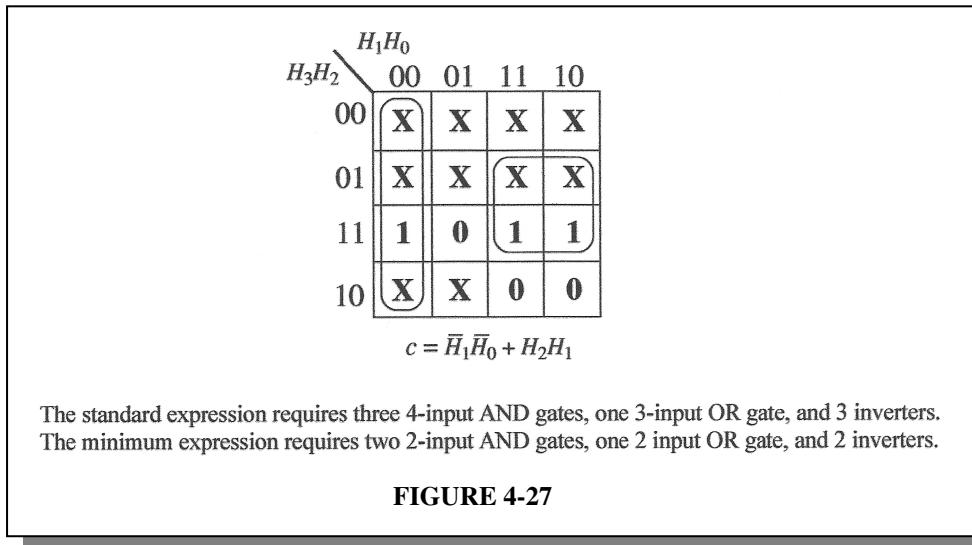
61. The VHDL program:

```
entity SOP is
    port (A, B, C: in bit; X: out bit);
end entity SOP;
architecture Logic of SOP is
begin
    Y <= (A and not B and C) or (not A and not B and C) or
        (A and not B and not C) or (not A and B and C);
end architecture Logic;
```

Applied Logic

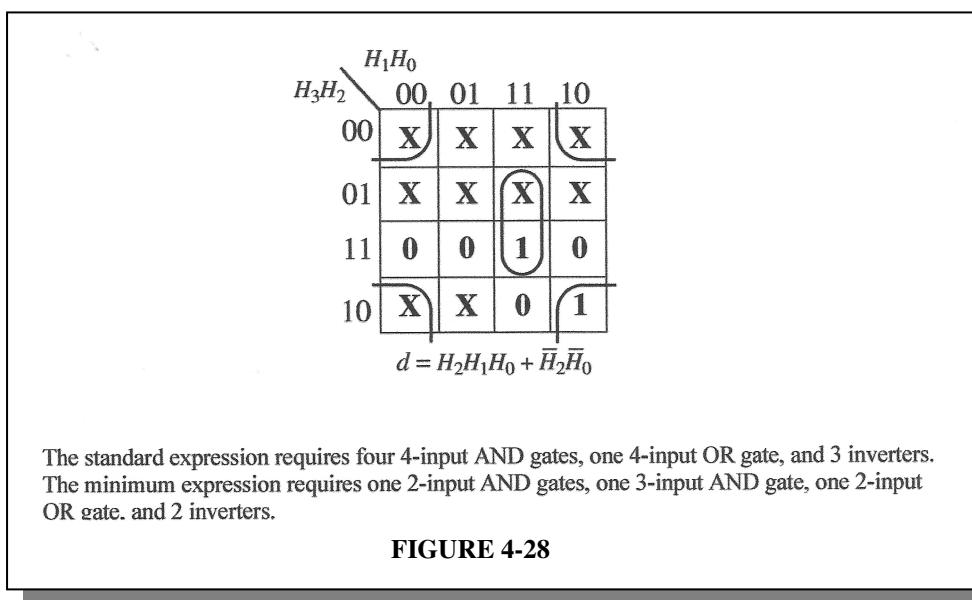
62. An LED Display is more suitable for low-light conditions because LEDs emit light and LCDs do not.
63. The purpose of the invalid code detector is to detect the codes 1010, 1011, 1100, 1101, 1110, and 1111 to activate the display for letters.
64. The standard SOP expression for segment c is:

$$c = H_3 \bar{H}_2 H_1 H_0 + H_3 \bar{H}_2 \bar{H}_1 H_0 + H_3 H_2 \bar{H}_1 H_0$$
 This expression is minimized in Figure 4-27.



65. The standard SOP expression for segment d is:

$$d = H_3 \bar{H}_2 H_1 H_0 + H_3 H_2 \bar{H}_1 H_0 + H_3 H_2 \bar{H}_1 H_0 + H_3 H_2 H_1 \bar{H}_0$$
 This expression is minimized in Figure 4-28.



Chapter 4

The standard SOP expression for segment e is:

$$e = H_3 \overline{H}_2 H_1 H_0 + H_3 \overline{H}_2 H_1 \overline{H}_0 + H_3 H_2 \overline{H}_1 \overline{H}_0 + H_3 H_2 H_1 \overline{H}_0$$

This expression is minimized in Figure 4-29.

$H_3 H_2$	$H_1 H_0$	00	01	11	10
$H_3 H_2$	00	X	X	X	X
00	01	X	X	(X)	X
01	11	0	0	(1)	0
11	10	X	X	0	0

$$e = H_2 H_1 H_0$$

The standard expression requires five 4-input AND gates, one 5-input OR gate, and 3 inverters.
The minimum expression requires one 3-input AND gate.

FIGURE 4-29

The standard SOP expression for segment f is:

$$f = H_3 \overline{H}_2 H_1 \overline{H}_0 + H_3 \overline{H}_2 H_1 H_0 + H_3 H_2 \overline{H}_1 \overline{H}_0 + H_3 H_2 H_1 \overline{H}_0$$

This expression is minimized in Figure 4-30.

$H_3 H_2$	$H_1 H_0$	00	01	11	10
$H_3 H_2$	00	X	X	X	X
00	01	X	(X)	(X)	X
01	11	0	(1)	(1)	0
11	10	X	X	0	0

$$f = H_2 H_0$$

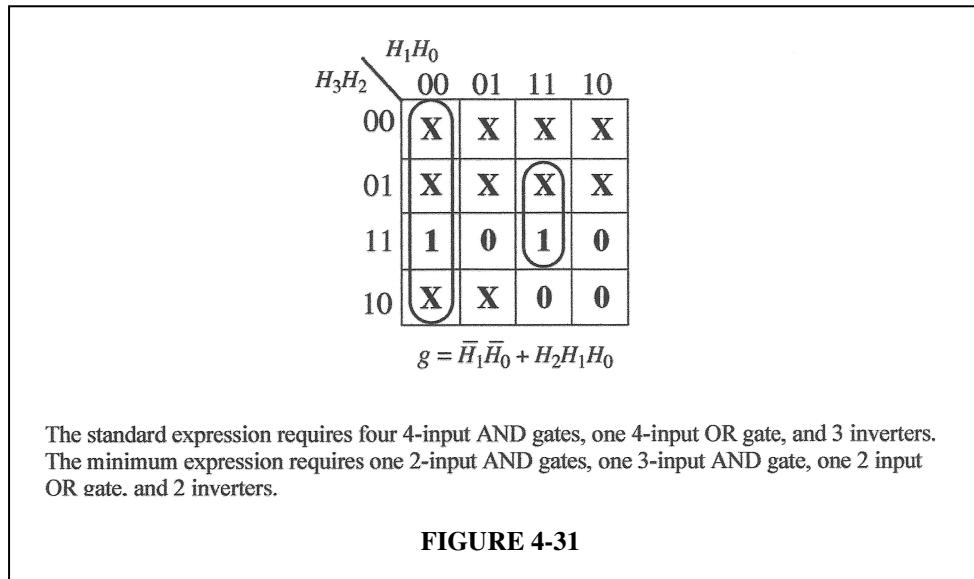
The standard expression requires four 4-input AND gates, one 4-input OR gate, and 3 inverters.
The minimum expression requires one 2-input AND gate.

FIGURE 4-30

The standard SOP expression for segment g is:

$$g = H_3 \bar{H}_2 H_1 \bar{H}_0 + H_3 \bar{H}_2 H_1 H_0 + H_3 H_2 \bar{H}_1 H_0 + H_3 H_2 H_1 \bar{H}_0$$

This expression is minimized in Figure 4-31.



Special Design Problems

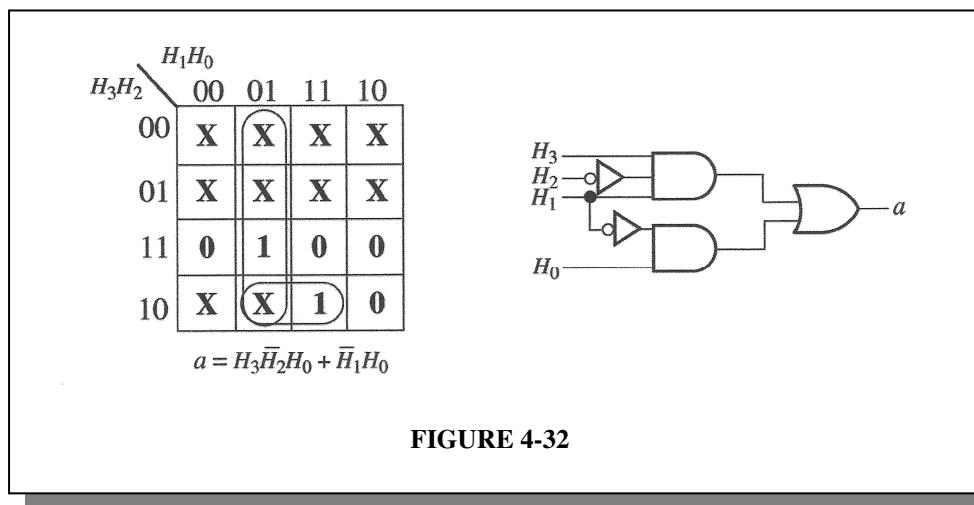
66. Connect the OR gate output for each segment to an inverter and then use the inverter output to drive the segment with a HIGH.

67. See Figure 4-27. $F = 1111$

The expression for segment a to include the letter F is:

$$a = H_3 \bar{H}_2 H_1 \bar{H}_0 + H_3 H_2 \bar{H}_1 \bar{H}_0 + H_3 H_2 H_1 \bar{H}_0 + H_3 H_2 H_1 H_0$$

The expression is minimized in Figure 4-32.



Chapter 4

68. See Figure 4-33. Segment *b* is used for letters *A* and *d*.

$$b = H_3 \bar{H}_2 H_2 H_1 \bar{H}_0 + H_3 H_2 \bar{H}_1 H_0$$

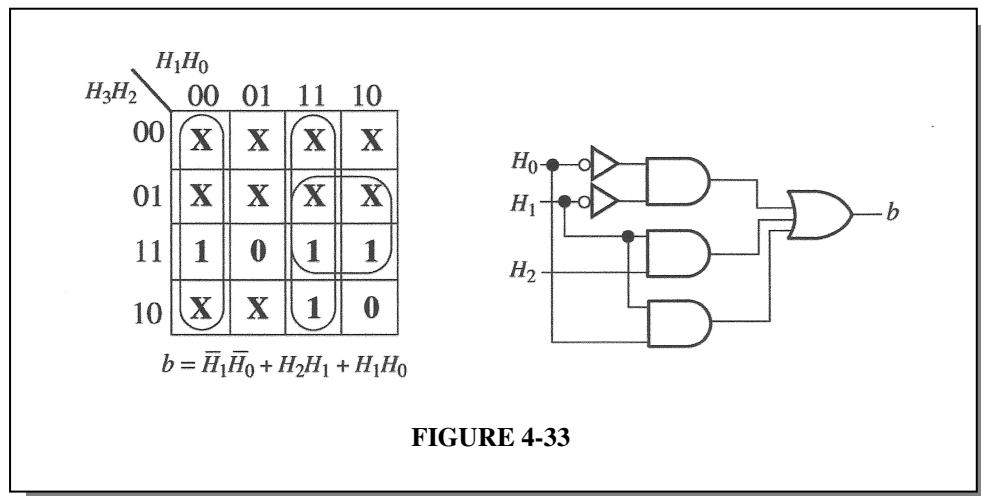


FIGURE 4-33

See Figure 4-34. Segment *c* is used for letters *A*, *b*, and *d*.

$$c = H_3 \bar{H}_2 H_2 H_1 \bar{H}_0 + H_3 \bar{H}_2 H_1 H_0 + H_3 H_2 \bar{H}_1 H_0$$

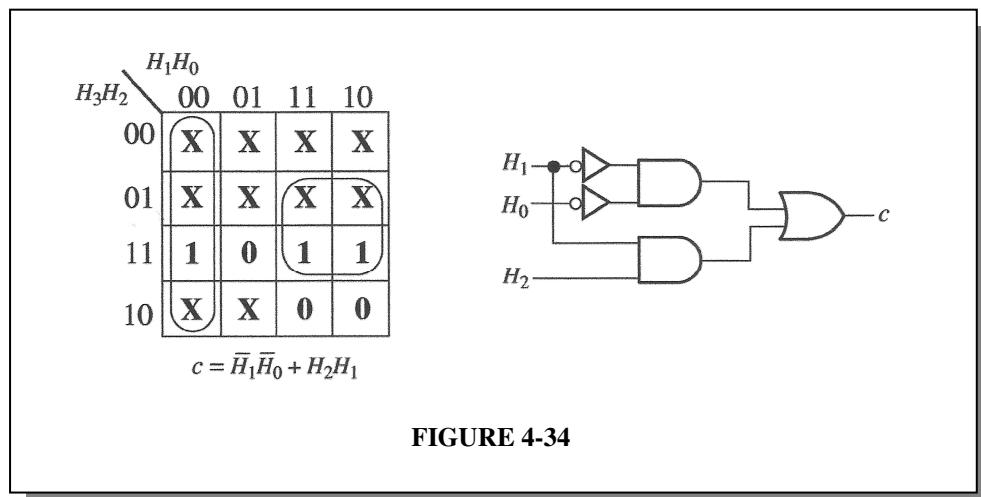
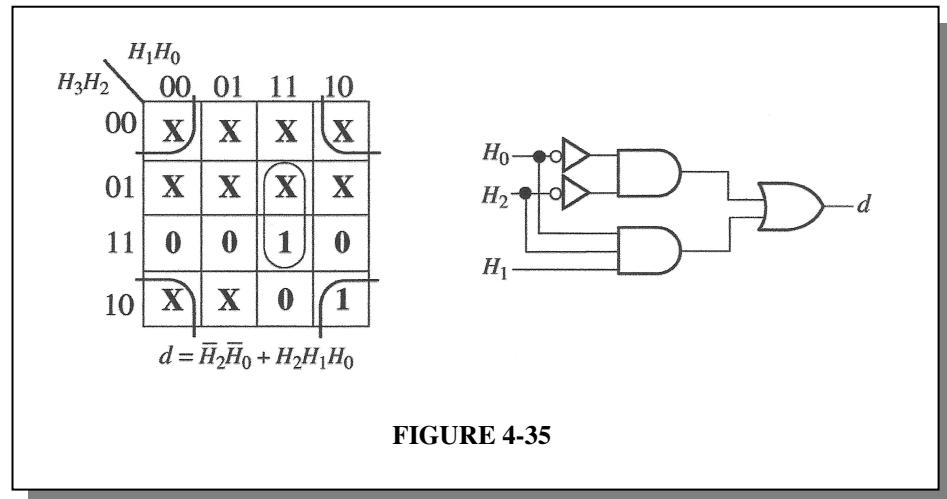


FIGURE 4-34

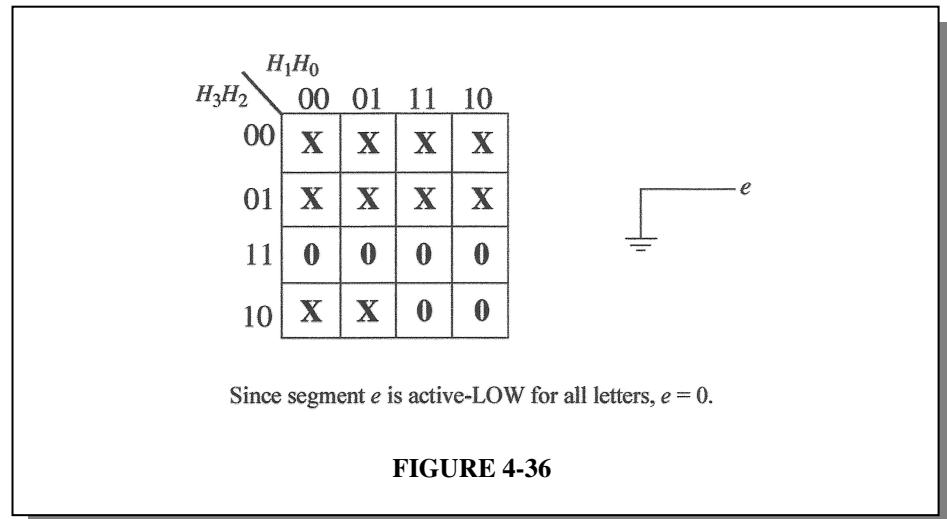
See Figure 4-35. Segment *d* is used for *b*, *c*, *d*, and *e*.

$$d = H_3 \bar{H}_2 H_2 \bar{H}_1 \bar{H}_0 + H_3 H_2 \bar{H}_2 \bar{H}_1 \bar{H}_0 + H_3 H_2 \bar{H}_1 \bar{H}_0 + H_3 H_2 H_1 \bar{H}_0$$



See Figure 4-36. Segment *e* is used for *A*, *b*, *C*, *d*, *E*, and *F*.

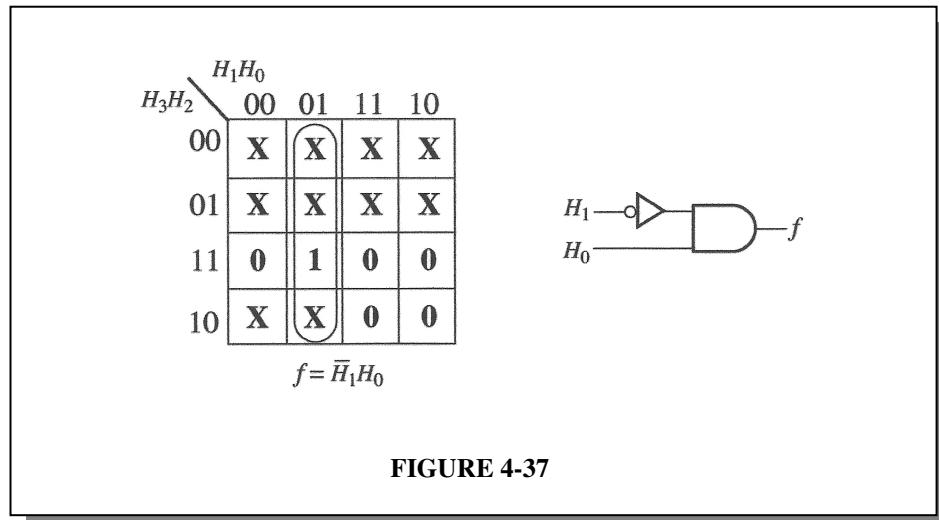
$$e = H_3 \bar{H}_2 H_2 \bar{H}_1 \bar{H}_0 + H_3 \bar{H}_2 H_1 H_0 + H_3 H_2 \bar{H}_1 \bar{H}_0 + H_3 H_2 \bar{H}_1 H_0 + H_3 H_2 H_1 \bar{H}_0 + H_3 H_2 H_1 H_0$$



Chapter 4

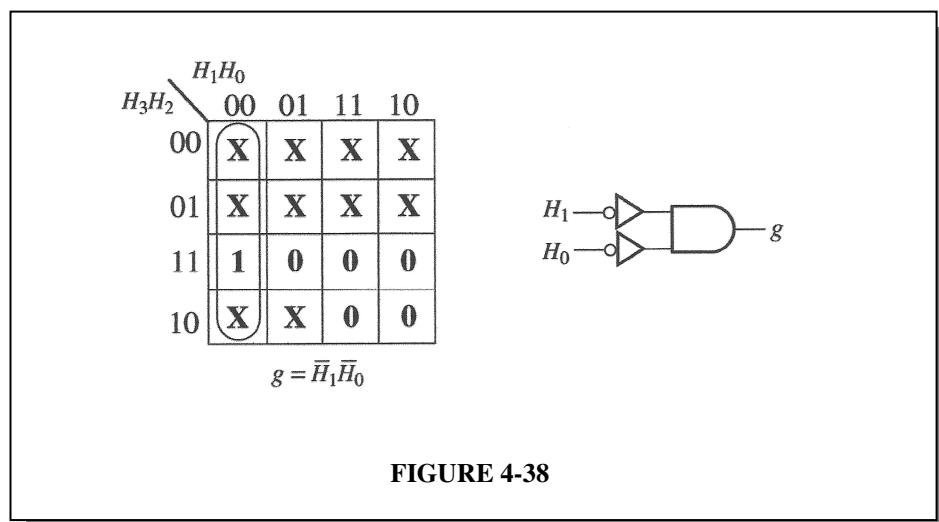
See Figure 4-37. Segment f is used for A, b, C, E , and F .

$$f = H_3 \bar{H}_2 H_1 \bar{H}_0 + H_3 \bar{H}_2 H_1 H_0 + H_3 H_2 \bar{H}_1 \bar{H}_0 + H_3 H_2 H_1 \bar{H}_0 + H_3 H_2 H_1 H_0$$

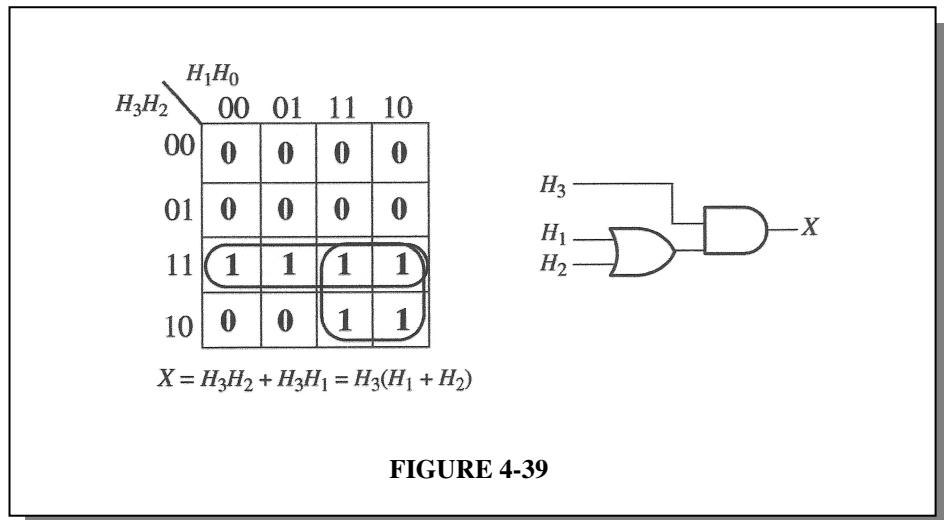


See Figure 4-38. Segment g is used for A, b, d, E , and F .

$$g = H_3 \bar{H}_2 H_1 \bar{H}_0 + H_3 \bar{H}_2 H_1 H_0 + H_3 H_2 \bar{H}_1 H_0 + H_3 H_2 H_1 \bar{H}_0 + H_3 H_2 H_1 H_0$$



- 69.** The invalid code detector must disable the display when any numerical input (0-9) occurs. A HIGH enables the display and a LOW disables it. A circuit that detects the numeric codes and produces a LOW is shown in Figure 4-39.



Multiisim Troubleshooting Practice

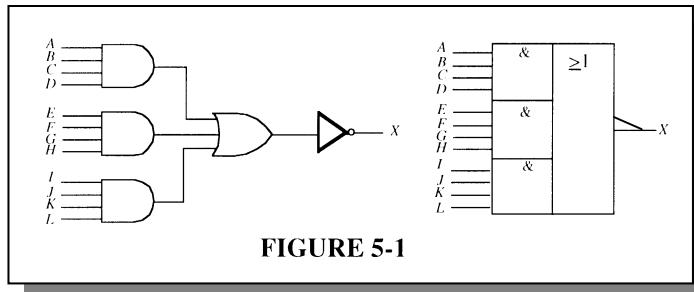
- 70.** Input C is shorted to ground.
- 71.** Bottom input of U7 is open.
- 72.** Output of U3 is shorted to ground.

CHAPTER 5

COMBINATIONAL LOGIC ANALYSIS

Section 5-1 Basic Combinational Logic Circuits

1. See Figure 5-1.



2. (a) $X = \overline{AB} + \overline{A} + AC$
 (b) $X = \overline{\overline{AB} + \overline{ACD} + DB\overline{D}}$

3. (a) $X = ABB$
 (b) $X = AB + B$
 (c) $X = \overline{A} + B$
 (d) $X = (A + B) + AB$
 (e) $X = \overline{\overline{ABC}}$
 (f) $X = (A + B)(\overline{B} + C)$

4. See Figure 5-2 for the circuit corresponding to each expression.

(a) $X = (A + B)(C + D) = AC + AD + BC + BD$
 (b) $X = \overline{\overline{ABC} + \overline{CD}} = (\overline{ABC})(CD) = (\overline{A} + \overline{B})CCD = \overline{ACD} + \overline{BCD}$
 (c) $X = (AB + C)D + E = ABD + CD + E$
 (d) $X = \overline{\overline{(A + B)}\overline{BC}} + D = \overline{\overline{(A + B)}\overline{BC}} + D = \overline{A} + B + BC + D = \overline{A} + B + D$
 (e) $X = \overline{\overline{(AB + C)}D + \overline{E}} = (AB + \overline{C})D + \overline{E} = ABD + \overline{CD} + \overline{E}$
 (f) $X = \overline{\overline{(AB + CD)}(\overline{EF} + \overline{GH})} = \overline{(AB + CD)(EF + GH)} = \overline{(AB + CD)} + \overline{(EF + GH)}$
 $\quad = \overline{(AB)}\overline{(CD)} + \overline{(EF)}\overline{(GH)}$
 $\quad = \overline{(\overline{A} + \overline{B})}\overline{(\overline{C} + \overline{D})} + (\overline{E} + \overline{F})(\overline{G} + \overline{H}) = \overline{AC} + \overline{BC} + \overline{AD} + \overline{BD} + \overline{EG} + \overline{FG} + \overline{EH} + \overline{FH}$

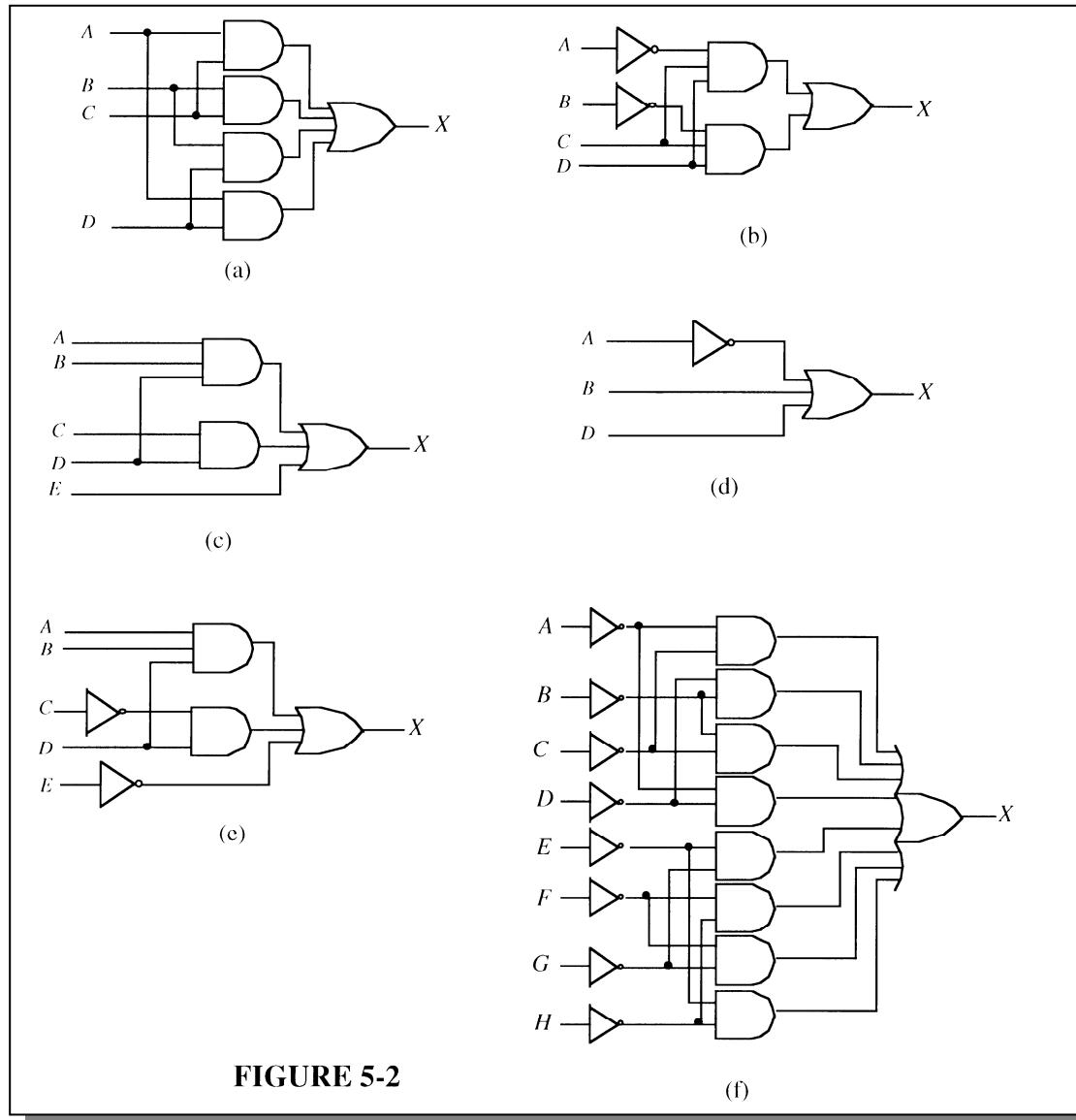


FIGURE 5-2

5. (a)

$$X = ABB$$

A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

(b)

$$X = AB + B$$

A	B	X
0	0	0
0	1	1
1	0	0
1	1	1

(c)

$$X = \bar{A} + B$$

A	B	X
0	0	1
0	1	1
1	0	0
1	1	1

(d)

$$X = (A + B) + AB$$

A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

(e)

$$X = \overline{\overline{ABC}}$$

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

(f)

$$X = (A + B)(\overline{B} + C)$$

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	1

Chapter 5

6. (a) $X = (A + B)(C + D)$	(b) $X = \overline{\overline{ABC} + \overline{CD}}$																																																																																																																																																																																																																																																																																										
<table border="1" style="border-collapse: collapse; width: 100%; border: none;"> <thead> <tr> <th>A</th> <th>B</th> <th>C</th> <th>D</th> <th>X</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> </tbody> </table>	A	B	C	D	X	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1	1	0	0	1	0	0	0	0	1	0	1	1	0	1	1	0	1	0	1	1	1	1	1	0	0	0	0	1	0	0	1	1	1	0	1	0	1	1	0	1	1	1	1	1	0	0	0	1	1	0	1	1	1	1	1	0	1	1	1	1	1	1	<table border="1" style="border-collapse: collapse; width: 100%; border: none;"> <thead> <tr> <th>A</th> <th>B</th> <th>C</th> <th>D</th> <th>X</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td></tr> </tbody> </table>	A	B	C	D	X	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	1	1	1	0	1	0	0	0	0	1	0	1	0	0	1	1	0	0	0	1	1	1	1	1	0	0	0	0	1	0	0	1	0	1	0	1	0	0	1	0	1	1	1	1	1	0	0	0	1	1	0	1	0	1	1	1	0	0	1	1	1	1	0																																																																																																																
A	B	C	D	X																																																																																																																																																																																																																																																																																							
0	0	0	0	0																																																																																																																																																																																																																																																																																							
0	0	0	1	0																																																																																																																																																																																																																																																																																							
0	0	1	0	0																																																																																																																																																																																																																																																																																							
0	0	1	1	0																																																																																																																																																																																																																																																																																							
0	1	0	0	0																																																																																																																																																																																																																																																																																							
0	1	0	1	1																																																																																																																																																																																																																																																																																							
0	1	1	0	1																																																																																																																																																																																																																																																																																							
0	1	1	1	1																																																																																																																																																																																																																																																																																							
1	0	0	0	0																																																																																																																																																																																																																																																																																							
1	0	0	1	1																																																																																																																																																																																																																																																																																							
1	0	1	0	1																																																																																																																																																																																																																																																																																							
1	0	1	1	1																																																																																																																																																																																																																																																																																							
1	1	0	0	0																																																																																																																																																																																																																																																																																							
1	1	0	1	1																																																																																																																																																																																																																																																																																							
1	1	1	0	1																																																																																																																																																																																																																																																																																							
1	1	1	1	1																																																																																																																																																																																																																																																																																							
A	B	C	D	X																																																																																																																																																																																																																																																																																							
0	0	0	0	0																																																																																																																																																																																																																																																																																							
0	0	0	1	0																																																																																																																																																																																																																																																																																							
0	0	1	0	0																																																																																																																																																																																																																																																																																							
0	0	1	1	1																																																																																																																																																																																																																																																																																							
0	1	0	0	0																																																																																																																																																																																																																																																																																							
0	1	0	1	0																																																																																																																																																																																																																																																																																							
0	1	1	0	0																																																																																																																																																																																																																																																																																							
0	1	1	1	1																																																																																																																																																																																																																																																																																							
1	0	0	0	0																																																																																																																																																																																																																																																																																							
1	0	0	1	0																																																																																																																																																																																																																																																																																							
1	0	1	0	0																																																																																																																																																																																																																																																																																							
1	0	1	1	1																																																																																																																																																																																																																																																																																							
1	1	0	0	0																																																																																																																																																																																																																																																																																							
1	1	0	1	0																																																																																																																																																																																																																																																																																							
1	1	1	0	0																																																																																																																																																																																																																																																																																							
1	1	1	1	0																																																																																																																																																																																																																																																																																							
(c) $X = (AB + C)D + E$	(d) $X = \overline{(A+B)}\overline{(BC)} + D$																																																																																																																																																																																																																																																																																										
<table border="1" style="border-collapse: collapse; width: 100%; border: none;"> <thead> <tr> <th>A</th> <th>B</th> <th>C</th> <th>D</th> <th>E</th> <th>X</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> </tbody> </table>	A	B	C	D	E	X	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0	1	1	1	0	0	1	0	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	1	0	0	1	1	0	1	0	1	0	0	0	1	0	1	1	1	0	1	1	0	0	0	0	1	1	0	1	1	0	1	1	1	0	1	0	1	1	1	1	1	1	0	0	0	0	0	1	0	0	0	1	1	1	0	0	1	0	0	1	0	0	1	1	1	1	0	1	0	0	0	1	0	1	0	1	1	1	0	1	1	0	0	1	0	1	1	1	1	1	1	0	0	0	0	1	1	0	0	1	1	1	1	0	1	0	1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	<table border="1" style="border-collapse: collapse; width: 100%; border: none;"> <thead> <tr> <th>A</th> <th>B</th> <th>C</th> <th>D</th> <th>X</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> </tbody> </table>	A	B	C	D	X	0	0	0	0	1	0	0	0	1	1	0	0	1	0	1	0	0	1	1	1	0	1	0	0	1	0	1	0	1	1	0	1	1	0	1	0	1	1	1	1	1	0	0	0	0	1	0	0	1	1	1	0	1	0	0	1	0	1	0	1	1	0	1	1	1	1	1	0	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1	1	1
A	B	C	D	E	X																																																																																																																																																																																																																																																																																						
0	0	0	0	0	0																																																																																																																																																																																																																																																																																						
0	0	0	0	1	1																																																																																																																																																																																																																																																																																						
0	0	0	1	0	0																																																																																																																																																																																																																																																																																						
0	0	0	1	1	1																																																																																																																																																																																																																																																																																						
0	0	1	0	0	0																																																																																																																																																																																																																																																																																						
0	0	1	0	1	1																																																																																																																																																																																																																																																																																						
0	0	1	1	0	0																																																																																																																																																																																																																																																																																						
0	0	1	1	1	1																																																																																																																																																																																																																																																																																						
0	1	0	0	0	0																																																																																																																																																																																																																																																																																						
0	1	0	0	1	1																																																																																																																																																																																																																																																																																						
0	1	0	1	0	0																																																																																																																																																																																																																																																																																						
0	1	0	1	1	1																																																																																																																																																																																																																																																																																						
0	1	1	0	0	0																																																																																																																																																																																																																																																																																						
0	1	1	0	1	1																																																																																																																																																																																																																																																																																						
0	1	1	1	0	1																																																																																																																																																																																																																																																																																						
0	1	1	1	1	1																																																																																																																																																																																																																																																																																						
1	0	0	0	0	0																																																																																																																																																																																																																																																																																						
1	0	0	0	1	1																																																																																																																																																																																																																																																																																						
1	0	0	1	0	0																																																																																																																																																																																																																																																																																						
1	0	0	1	1	1																																																																																																																																																																																																																																																																																						
1	0	1	0	0	0																																																																																																																																																																																																																																																																																						
1	0	1	0	1	1																																																																																																																																																																																																																																																																																						
1	0	1	1	0	0																																																																																																																																																																																																																																																																																						
1	0	1	1	1	1																																																																																																																																																																																																																																																																																						
1	1	0	0	0	0																																																																																																																																																																																																																																																																																						
1	1	0	0	1	1																																																																																																																																																																																																																																																																																						
1	1	0	1	0	1																																																																																																																																																																																																																																																																																						
1	1	0	1	1	1																																																																																																																																																																																																																																																																																						
1	1	1	0	1	1																																																																																																																																																																																																																																																																																						
1	1	1	0	1	1																																																																																																																																																																																																																																																																																						
1	1	1	1	1	1																																																																																																																																																																																																																																																																																						
A	B	C	D	X																																																																																																																																																																																																																																																																																							
0	0	0	0	1																																																																																																																																																																																																																																																																																							
0	0	0	1	1																																																																																																																																																																																																																																																																																							
0	0	1	0	1																																																																																																																																																																																																																																																																																							
0	0	1	1	1																																																																																																																																																																																																																																																																																							
0	1	0	0	1																																																																																																																																																																																																																																																																																							
0	1	0	1	1																																																																																																																																																																																																																																																																																							
0	1	1	0	1																																																																																																																																																																																																																																																																																							
0	1	1	1	1																																																																																																																																																																																																																																																																																							
1	0	0	0	0																																																																																																																																																																																																																																																																																							
1	0	0	1	1																																																																																																																																																																																																																																																																																							
1	0	1	0	0																																																																																																																																																																																																																																																																																							
1	0	1	0	1																																																																																																																																																																																																																																																																																							
1	0	1	1	1																																																																																																																																																																																																																																																																																							
1	1	0	1	1																																																																																																																																																																																																																																																																																							
1	1	0	1	1																																																																																																																																																																																																																																																																																							
1	1	1	0	1																																																																																																																																																																																																																																																																																							
1	1	1	1	1																																																																																																																																																																																																																																																																																							

(e) $X = \overline{(\overline{AB} + \overline{C})D + \overline{E}}$

A	B	C	D	E	X	A	B	C	D	E	X
0	0	0	0	0	1	1	0	0	0	0	1
0	0	0	0	1	0	1	0	0	0	1	0
0	0	0	1	0	1	1	0	0	1	0	1
0	0	0	1	1	1	1	0	0	1	1	1
0	0	1	0	0	1	1	0	1	0	0	1
0	0	1	0	1	0	1	0	1	0	1	0
0	0	1	1	0	1	1	0	1	1	0	1
0	0	1	1	1	0	1	0	1	1	1	0
0	1	0	0	0	1	1	1	0	0	0	1
0	1	0	0	1	0	1	1	0	0	1	0
0	1	0	1	0	1	1	1	0	1	0	1
0	1	0	1	1	1	1	1	0	1	1	1
0	1	1	0	0	1	1	1	1	0	0	1
0	1	1	0	1	0	1	1	1	0	1	0
0	1	1	1	0	1	1	1	1	1	0	1
0	1	1	1	1	0	1	1	1	1	1	1

(f) $X = (\overline{AB} + \overline{CD})(\overline{EF} + \overline{GH})$

A	B	C	D	E	F	G	H	I
0	X	0	X	X	X	X	X	1
X	0	0	X	X	X	X	X	1
0	X	X	0	X	X	X	X	1
X	0	X	0	0	X	X	X	1
X	X	X	X	0	X	0	X	1
X	X	X	X	X	0	0	X	1
X	X	X	X	0	X	X	0	1
X	X	X	X	X	0	X	0	1

For all other entries $X = 0$.

X = don't care

An abbreviated table is shown because there are 256 combinations.

7. $X = \overline{\overline{AB} + \overline{AB}} = (\overline{AB})(\overline{\overline{AB}}) = (\overline{A} + B)(A + \overline{B})$

Section 5-2 Implementing Combinational Logic

8. Let G = guard, S = switch, M = motor temp, and P = power. See Figure 5-3.

$$P = \overline{\overline{GS} + MS}$$

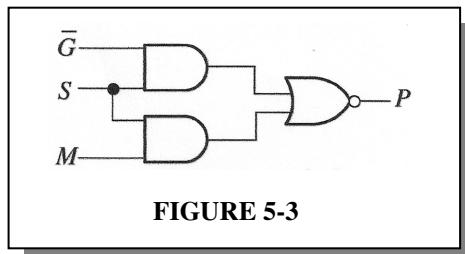


FIGURE 5-3

Chapter 5

9. $X = \overline{ABCD} + EFGH$

10. See Figure 5-4.

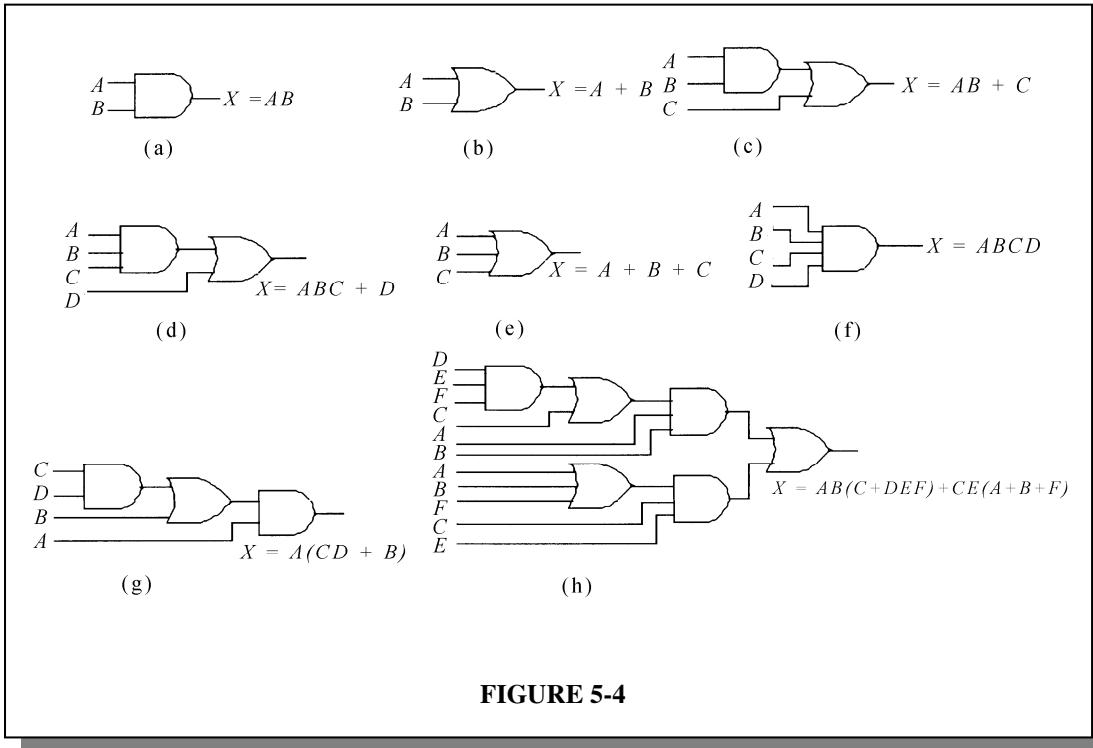
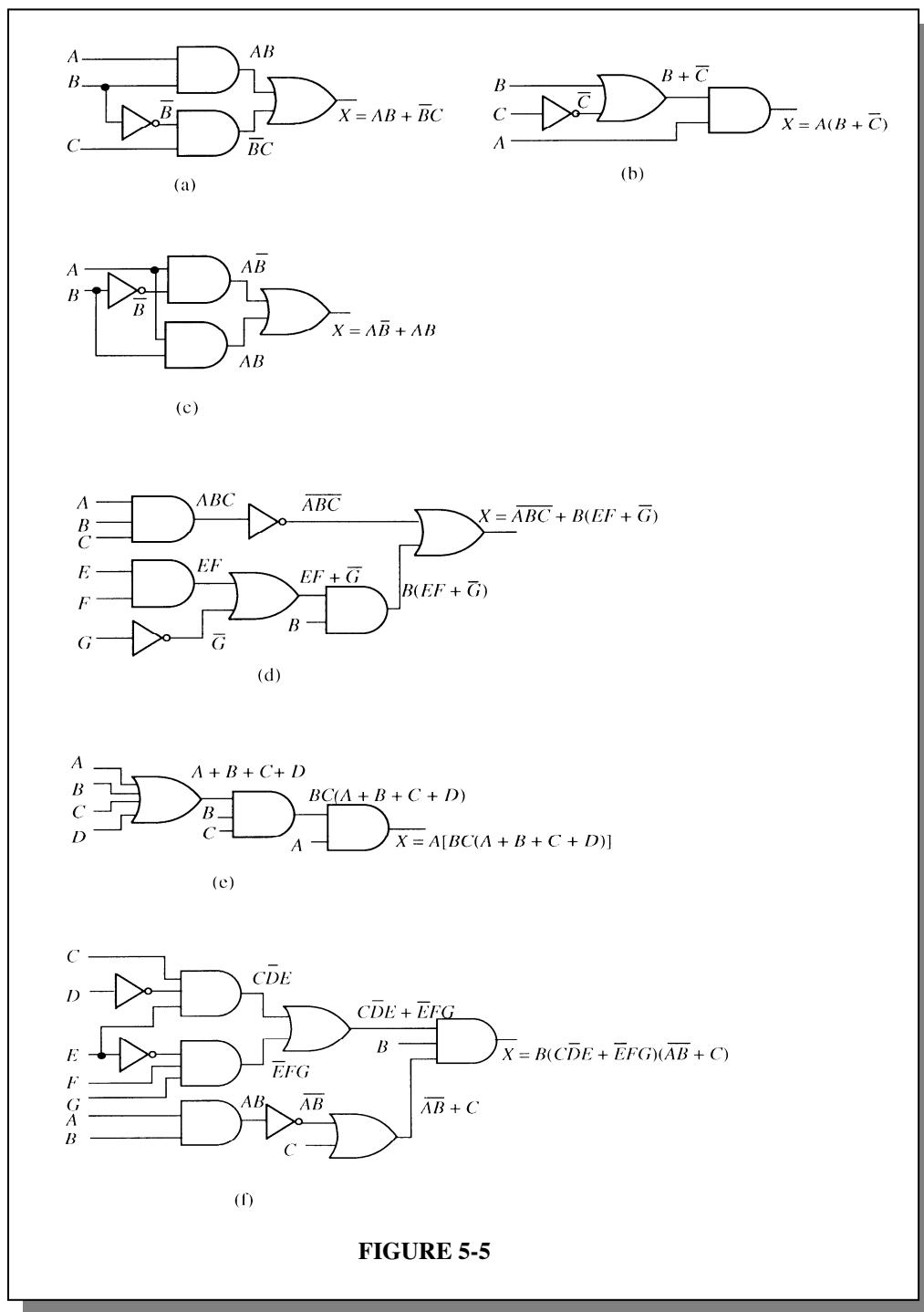


FIGURE 5-4

11. See Figure 5-5.



Chapter 5

12. See Figure 5-6.

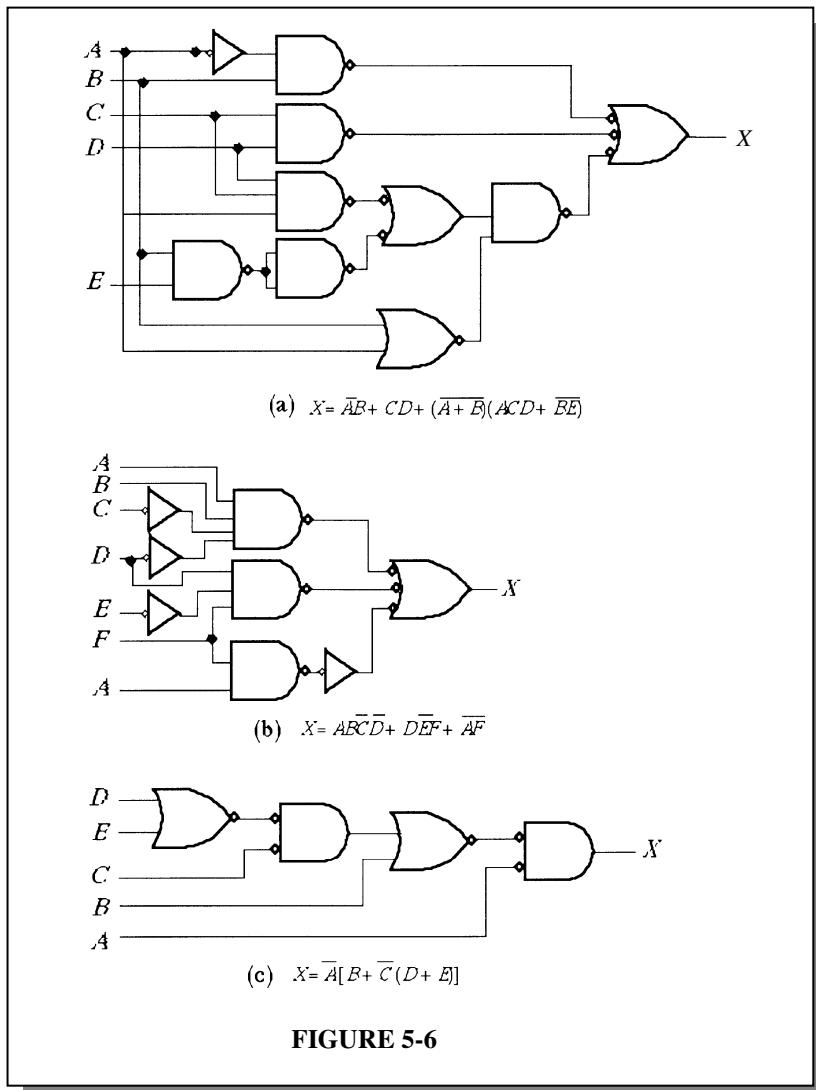


FIGURE 5-6

13. $X = \overline{ABC} + \overline{ABC} + \overline{ABC} + ABC + ABC$

See Figure 5-7.

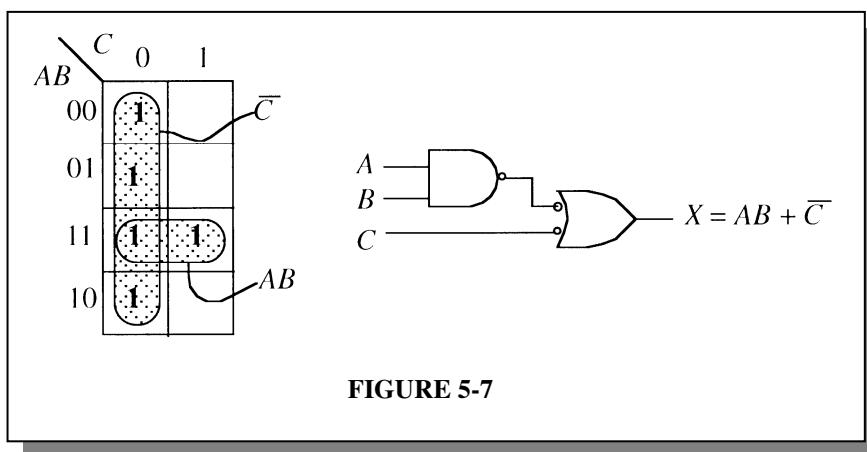
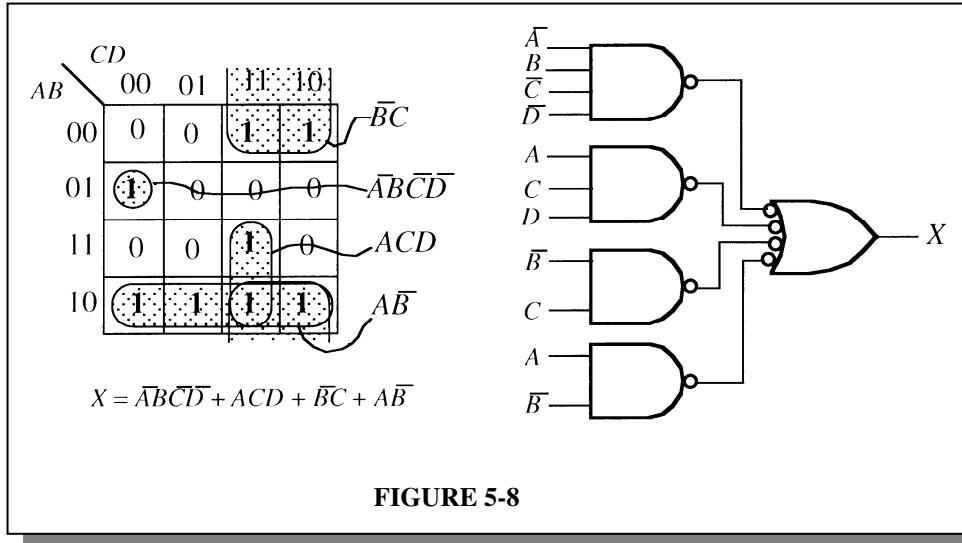


FIGURE 5-7

14. $X = \overline{ABCD} + \overline{ABC}D + \overline{ABC}\overline{D} + A\overline{B}\overline{C}\overline{D} + A\overline{B}\overline{C}D + A\overline{B}C\overline{D} + A\overline{B}CD + ABCD$
 See Figure 5-8.



15. $X = AB + ABC = AB(1 + C) = AB$

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

$X = 1$ when $AB = 1$, no matter what C is.

A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

Since C is a don't care variable, the output depends only on A and B as shown by the two-variable truth table above which is implemented with the AND gate in Figure 5-9.

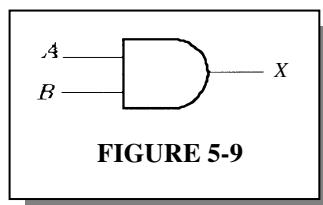


FIGURE 5-9

Chapter 5

$$\begin{aligned}
 16. \quad X &= (\overline{AB})(\overline{B+C}) + C = (\overline{AB})(\overline{B+C})\overline{C} = (\overline{AB})(\overline{B+C})\overline{C} = (\overline{A+B})(\overline{BC})\overline{C} \\
 &= (\overline{AB} + \overline{AC} + \overline{BB} + \overline{BC})\overline{C} = \overline{ABC} + \overline{AC} + \overline{BC} + \overline{B}\overline{C} \\
 &= \overline{AC}(\overline{B} + 1) + \overline{BC} = \overline{AC} + \overline{BC}
 \end{aligned}$$

See Figure 5-10.

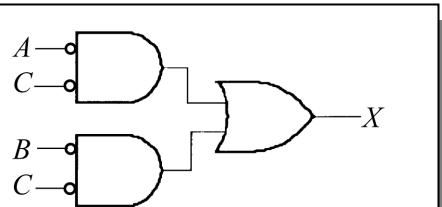


FIGURE 5-10

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

17. (a) $X = AB + \overline{BC}$

No simplification. See Figure 5-11.

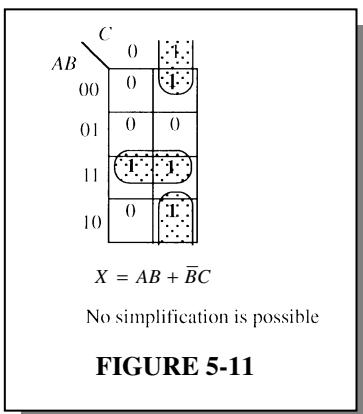


FIGURE 5-11

(b) $X = A(B + \overline{C}) = AB + A\overline{C}$

No simplification. Equation can be expressed in another form, as indicated in Figure 5-12.

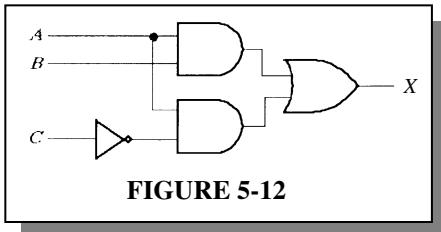


FIGURE 5-12

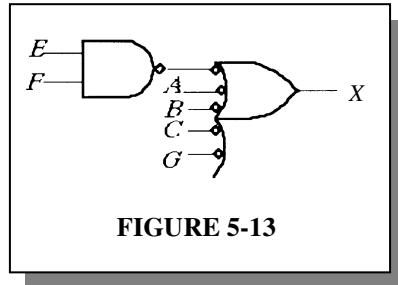
(c) $X = AB + A\overline{B} = A(B + \overline{B}) = A$

A direct connection from input to output. No gates required.

$$(d) \quad X = \overline{A}\overline{B}\overline{C} + B(EF + \overline{G}) = \overline{A} + \overline{B} + \overline{C} + BEF + B\overline{G}$$

$$= \overline{A} + \overline{C} + BEF + \overline{B} + \overline{G} = \overline{A} + \overline{C} + \overline{B} + EF + \overline{G}$$

See Figure 5-13.

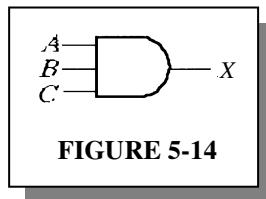


$$(e) \quad X = A(BC(A + B + C + D)) = ABCA + ABCB + ABCC + ABCD$$

$$= ABC + ABC + ABC + ABCD = ABC + ABC(1 + D)$$

$$= ABC + ABC = ABC$$

See Figure 5-14.



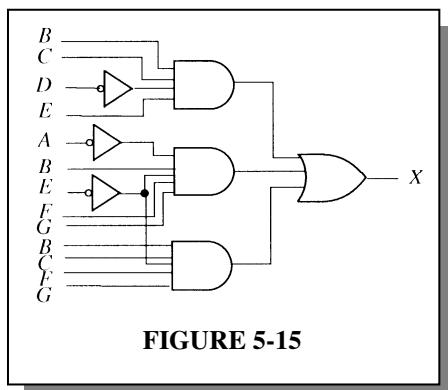
$$(f) \quad X = B(C\overline{D}E + \overline{E}FG)(\overline{A}\overline{B} + C) = (BC\overline{D}E + B\overline{E}FG)(\overline{A} + \overline{B} + C)$$

$$= \overline{ABC}\overline{D}E + \overline{AB}\overline{E}FG + BC\overline{D}E + BCE\overline{F}G$$

$$= BC\overline{D}E(\overline{A} + 1) + \overline{AB}\overline{E}FG + BCE\overline{F}G$$

$$= BC\overline{D}E + \overline{AB}\overline{E}FG + BCE\overline{F}G$$

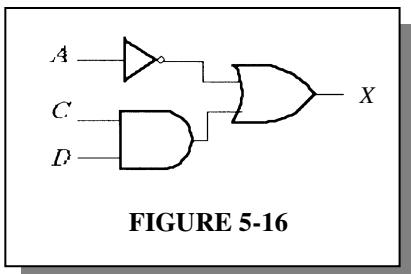
See Figure 5-15.



Chapter 5

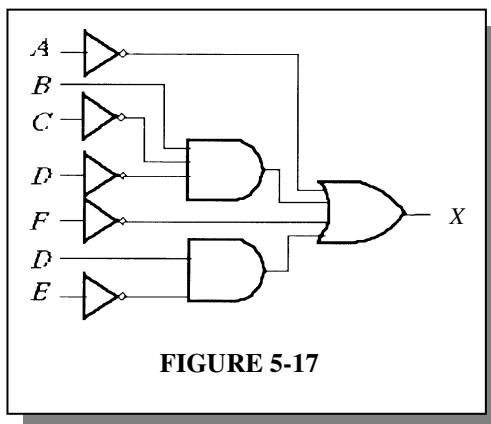
18. (a)
$$\begin{aligned} X &= \overline{AB} + CD + (\overline{A+B})(ACD + \overline{B}\overline{E}) = \overline{AB} + CD + \overline{AB}(ACD + \overline{B} + \overline{E}) \\ &= \overline{AB} + CD + \overline{AB} + \overline{AB}\overline{E} = \overline{A}(B + \overline{B}) + CD + \overline{AB}\overline{E} \\ &= \overline{A} + \overline{ABE} + CD = \overline{A}(1 + \overline{BE}) + CD = \overline{A} + CD \end{aligned}$$

See Figure 5-16.



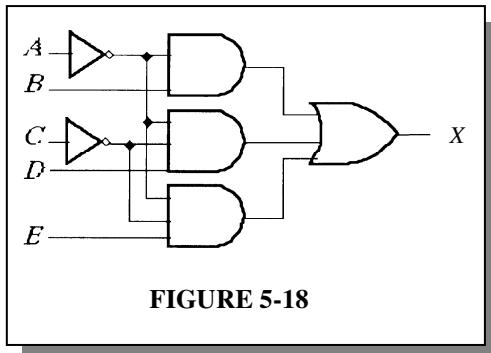
(b)
$$\begin{aligned} X &= AB\overline{C}\overline{D} + D\overline{E}F + \overline{A}\overline{F} = AB\overline{C}\overline{D} + \overline{DEF} + \overline{A} + \overline{F} \\ &= \overline{A} + B\overline{C}\overline{D} + \overline{F} + D\overline{E} \end{aligned}$$

See Figure 5-17.



(c)
$$X = \overline{A}(B + \overline{C}(D + E)) = \overline{A}(B + \overline{C}D + \overline{C}E) = \overline{AB} + \overline{AC}\overline{D} + \overline{ACE}$$

See Figure 5-18.



19. The SOP expressions are developed as follows and the resulting circuits are shown in Figure 5-19.

$$(a) \quad X = (A + B)(C + D) = AC + AD + BC + BD$$

$$(b) \quad X = \overline{\overline{ABC} + \overline{CD}} = (\overline{ABC})(\overline{CD}) = (\overline{A} + \overline{B})\overline{C}\overline{D} = \overline{ACD} + \overline{BCD}$$

$$(c) \quad X = (AB + C)D + E = ABD + CD + E$$

$$(d) \quad X = \overline{\overline{(A + B)}(\overline{BC}) + D} = \overline{\overline{(A + B)}(\overline{BC})} + D = \overline{A} + B + \overline{BC} + D \\ = \overline{A} + B(1 + C) + D = \overline{A} + B + D$$

$$(e) \quad X = \overline{\overline{(AB + \overline{C})}D + \overline{E}} = (AB + \overline{C})D + \overline{E} = ABD + \overline{CD} + \overline{E}$$

$$(f) \quad X = \overline{\overline{(AB + \overline{CD})(EF + \overline{GH})}} = (\overline{AB} + \overline{CD})(EF + \overline{GH}) = (\overline{AB} + \overline{CD}) + (\overline{EF} + \overline{GH}) \\ = (\overline{AB})(\overline{CD}) + (\overline{EF})(\overline{GH}) = (\overline{A} + \overline{B})(\overline{C} + \overline{D}) + (\overline{E} + \overline{F})(\overline{G} + \overline{H}) \\ = \overline{AC} + \overline{BC} + \overline{AD} + \overline{BD} + \overline{EG} + \overline{FG} + \overline{EH} + \overline{FH}$$

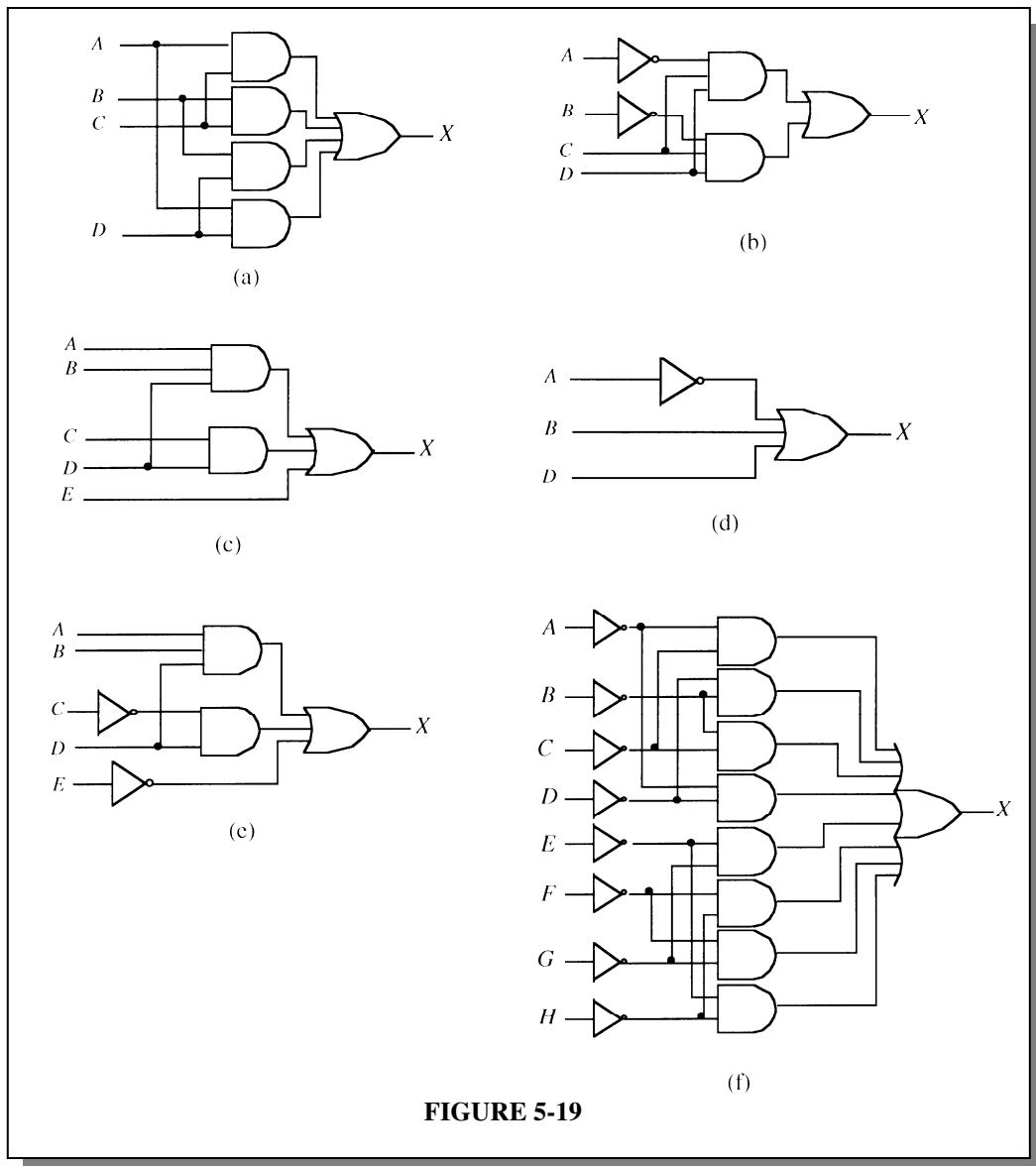
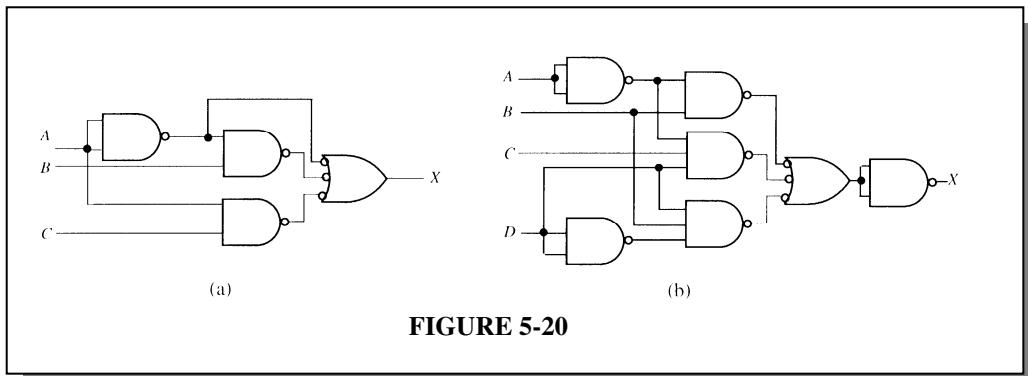


FIGURE 5-19

Chapter 5

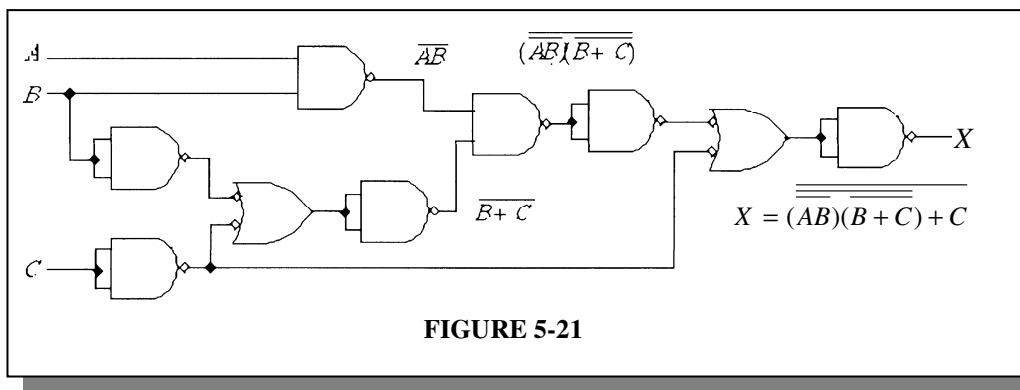
Section 5-3 The Universal Property of NAND and NOR Gates

20. See Figure 5-20.

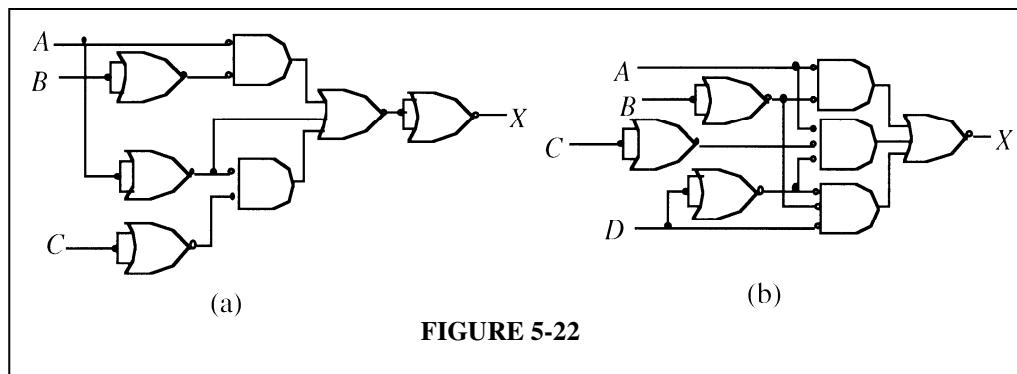


21. $X = \overline{\overline{AB}}(\overline{B+C}) + C$

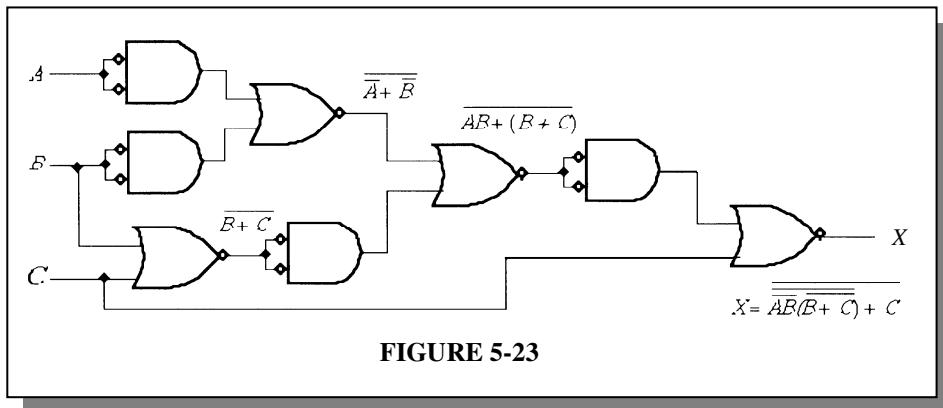
See Figure 5-21.



22. See Figure 5-22.



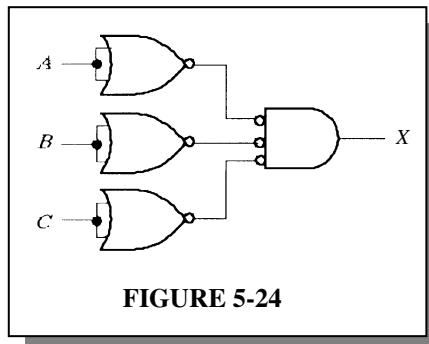
23. See Figure 5-23.



Section 5-4 Combinational Logic Using NAND and NOR Gates

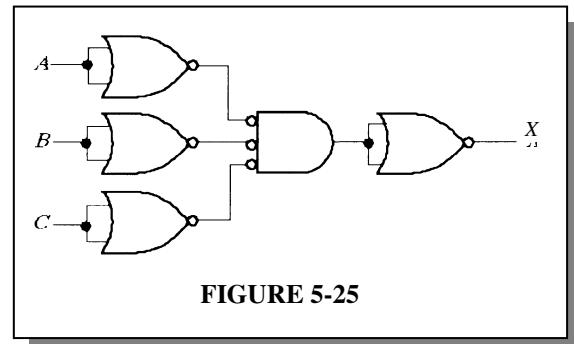
24. (a) $X = ABC$

See Figure 5-24.



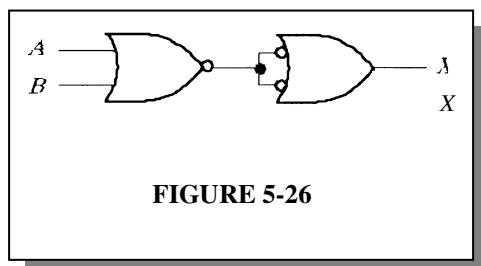
(b) $X = \overline{ABC}$

See Figure 5-25.



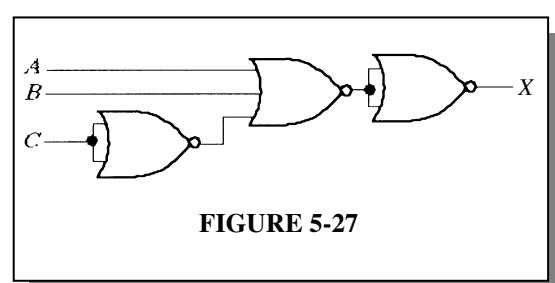
(c) $X = A + B$

See Figure 5-26.



(d) $X = A + B + \overline{C}$

See Figure 5-27.



Chapter 5

(e) $X = \overline{AB} + \overline{CD}$

See Figure 5-28.

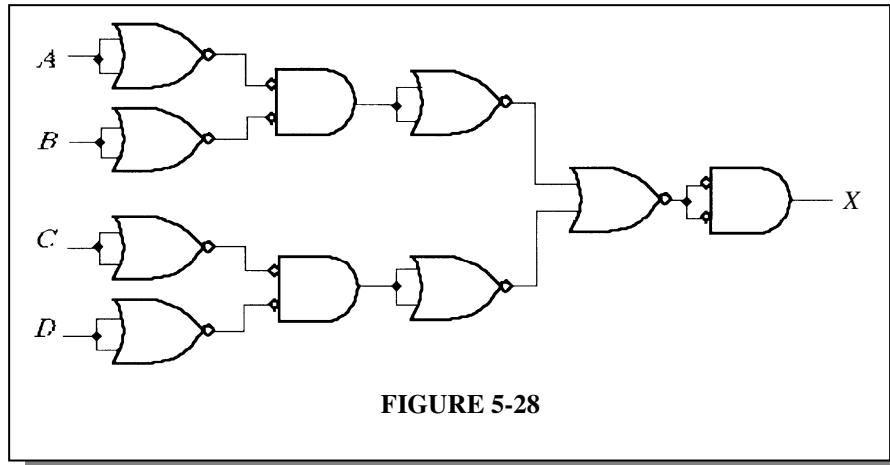


FIGURE 5-28

(f) $X = (A + B)(C + D)$

See Figure 5-29.

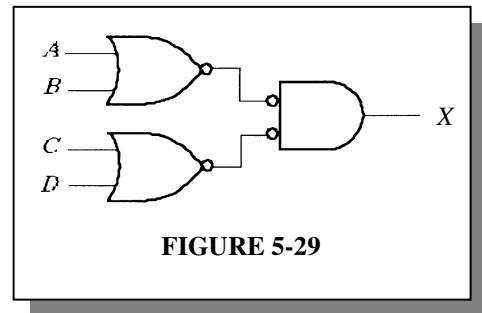


FIGURE 5-29

(g) $X = AB[C(\overline{DE} + \overline{AB}) + \overline{BCE}]$

See Figure 5-30.

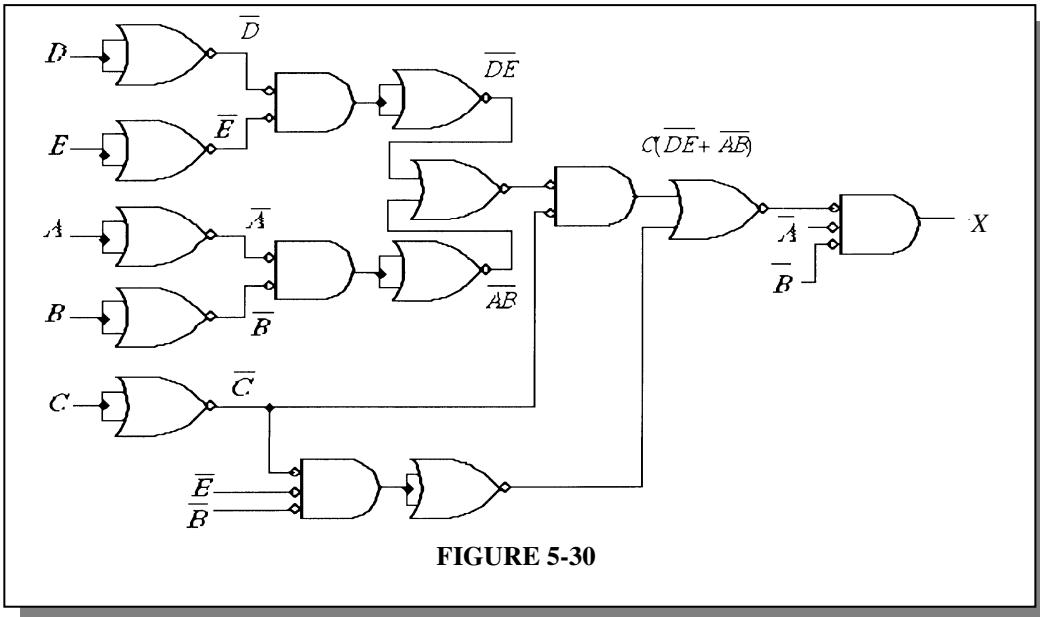
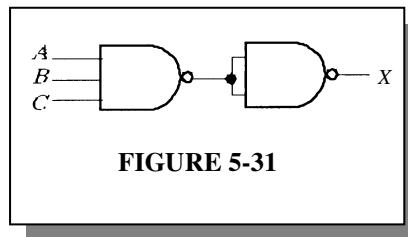


FIGURE 5-30

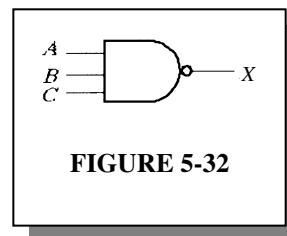
25. (a) $X = ABC$

See Figure 5-31.



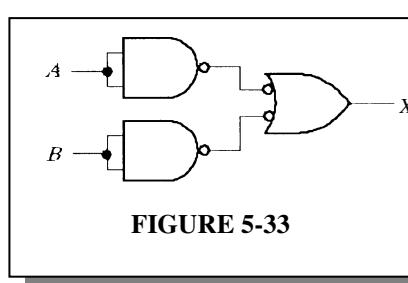
(b) $X = \overline{ABC}$

See Figure 5-32.



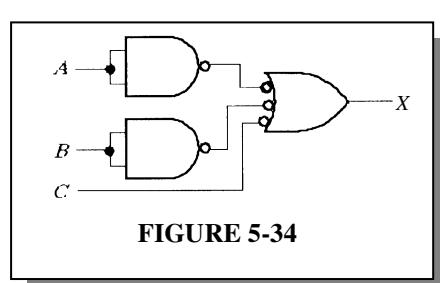
(c) $X = A + B$

See Figure 5-33.



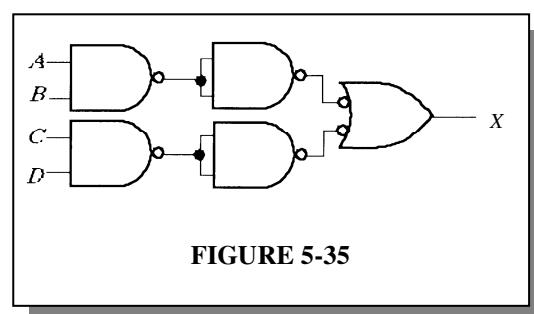
(d) $X = A + B + \overline{C}$

See Figure 5-34.



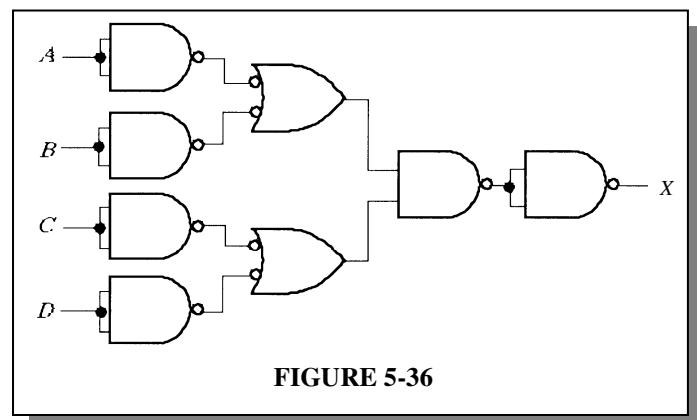
(e) $X = \overline{AB} + \overline{CD}$

See Figure 5-35.



(f) $X = (A + B)(C + D)$

See Figure 5-36.



Chapter 5

(g) $X = AB[C(\overline{DE} + \overline{AB}) + \overline{BCE}]$

See Figure 5-37.

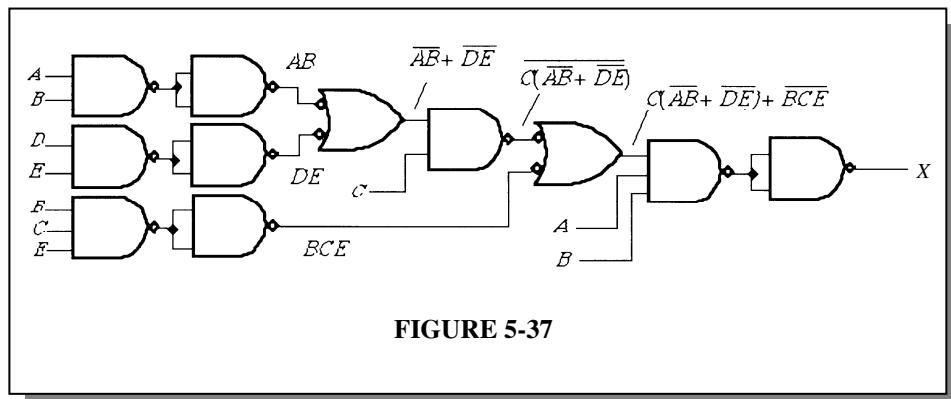


FIGURE 5-37

26. (a) $X = AB$

See Figure 5-38.

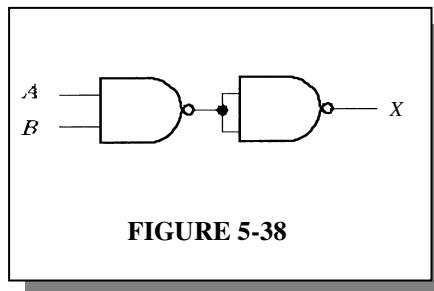


FIGURE 5-38

(b) $X = A + B$

See Figure 5-39.

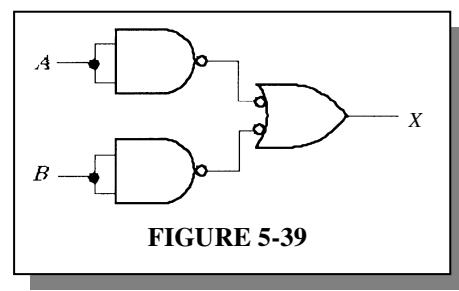


FIGURE 5-39

(c) $X = AB + C$

See Figure 5-40.

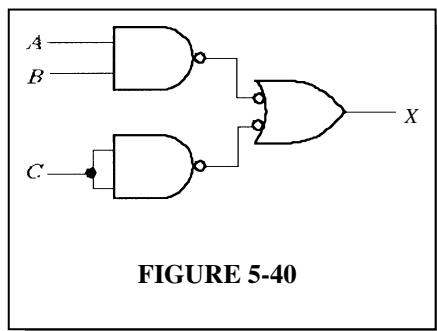


FIGURE 5-40

(d) $X = ABC + D$

See Figure 5-41.

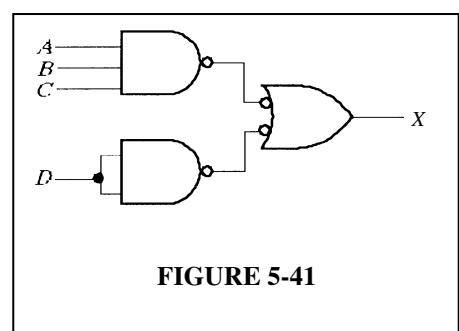
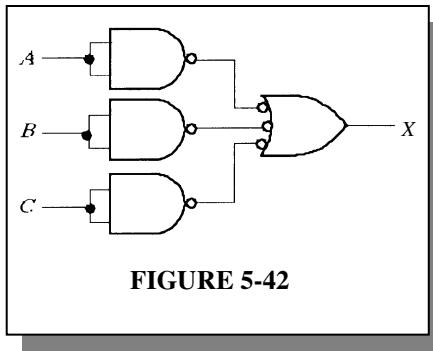
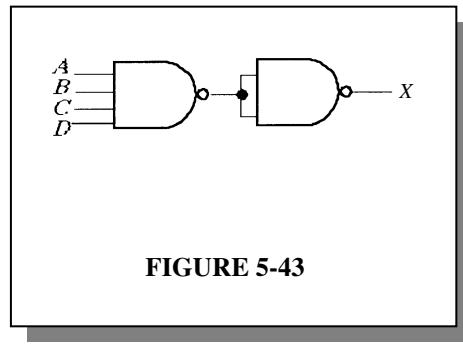


FIGURE 5-41

(e) $X = A + B + C$
See Figure 5-42.

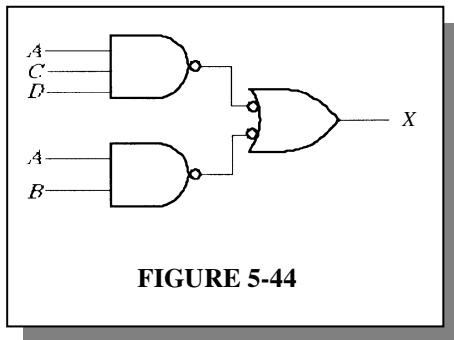


(f) $X = ABCD$
See Figure 5-43.



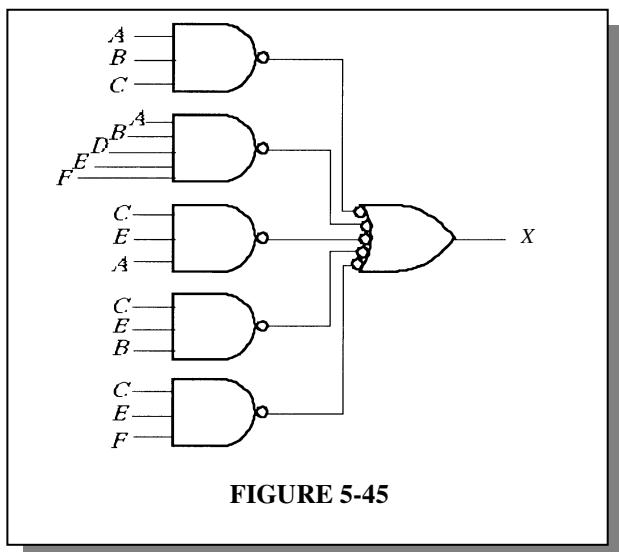
(g) $X = A(CD + B) = ACD + AB$

See Figure 5-44.



(h)
$$\begin{aligned} X &= AB(C + DEF) + CE(A + B + F) \\ &= ABC + ABDEF + CEA + CEB + CEF \end{aligned}$$

See Figure 5-45.



Chapter 5

27. (a) $X = AB + \bar{B}C$

See Figure 5-46.

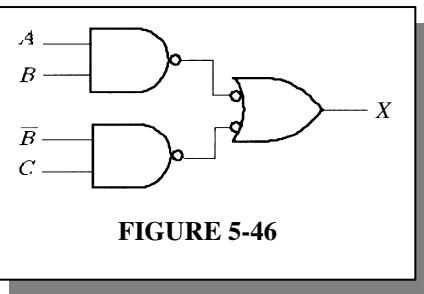


FIGURE 5-46

(b) $X = A(B + \bar{C}) = A\bar{B} + A\bar{C}$

See Figure 5-47.

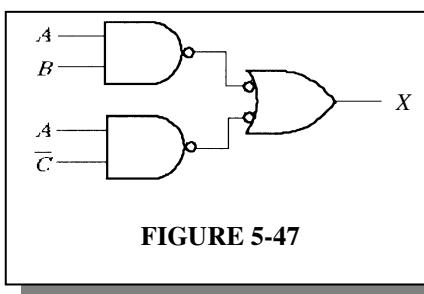


FIGURE 5-47

(c) $X = A\bar{B} + AB$

See Figure 5-48.

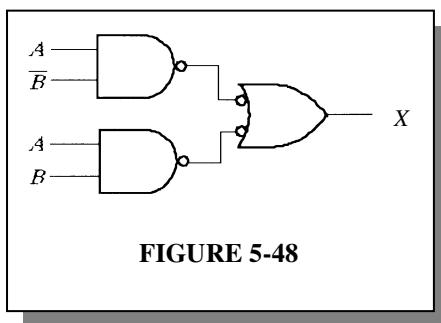


FIGURE 5-48

(d) $X = \bar{A}\bar{B}\bar{C} + B(EF + \bar{G}) = \bar{A} + \bar{B} + \bar{C} + BEF + BG$

See Figure 5-49.

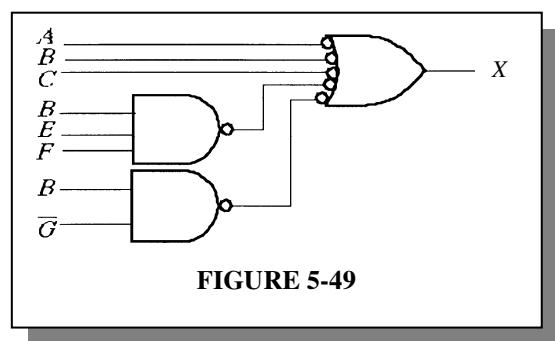
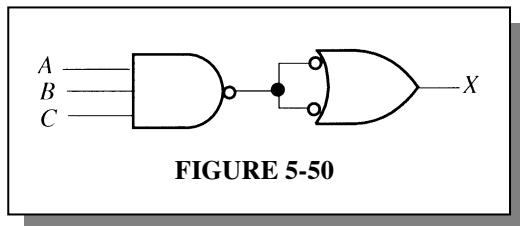


FIGURE 5-49

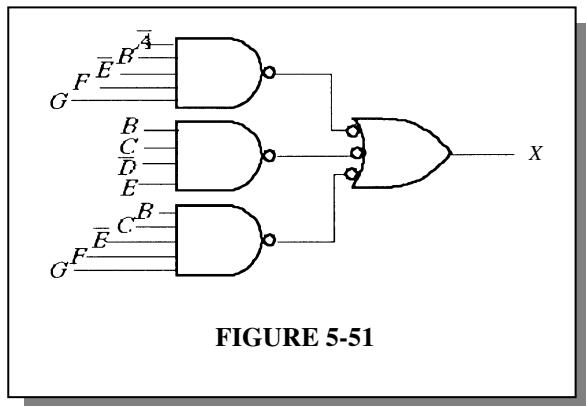
$$\begin{aligned}
 (e) \quad X &= A[BC(A + B + C + D)] = ABCA + ABCB + ABCC + ABCD \\
 &= ABC + ABC + ABC + ABCD + ABC(1 + D) = ABC
 \end{aligned}$$

See Figure 5-50.



$$\begin{aligned}
 (f) \quad X &= B(C\bar{D}E + \bar{E}FG)(\bar{A}\bar{B} + C) = B(C\bar{D}E + \bar{E}FG)(\bar{A} + \bar{B} + C) \\
 &= B(\bar{A}C\bar{D}E + \bar{A}\bar{E}FG + \bar{B}C\bar{D}E + \bar{B}\bar{E}FG + C\bar{D}E + C\bar{E}FG) \\
 &= \bar{A}B\bar{E}FG + \bar{B}B\bar{E}FG + BC\bar{D}E + BC\bar{E}FG \\
 &= \bar{A}B\bar{E}FG + BC\bar{D}E + BC\bar{E}FG
 \end{aligned}$$

See Figure 5-51.



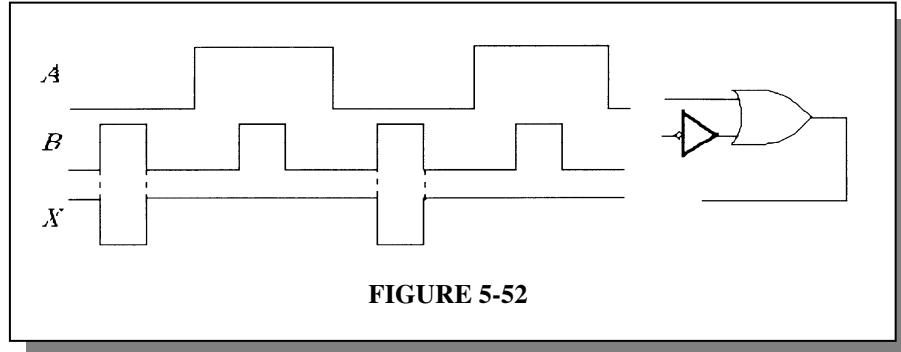
Section 5-5 Pulse Waveform Operation

28. $X = \overline{\overline{A} + \overline{B} + B} = A\overline{B} = 0$
The output X is always LOW.

29. $X = (\overline{AB})B = A + \overline{B} + \overline{B} = A + \overline{B}$

See Figure 5-52.

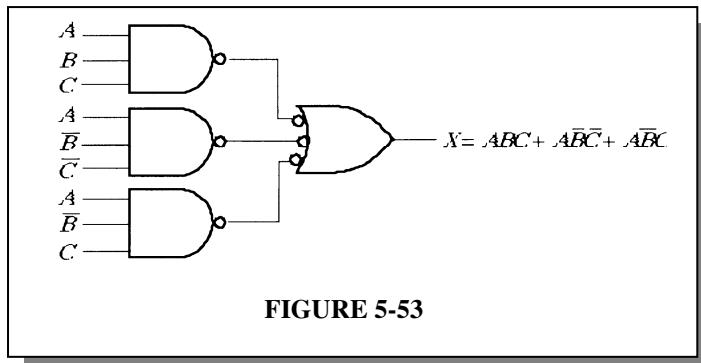
Chapter 5



30. X is HIGH when ABC are all HIGH or when A is HIGH and B is LOW and C is LOW or when A is HIGH and B is LOW and C is HIGH.

$$X = ABC + \bar{A}\bar{B}C + A\bar{B}C$$

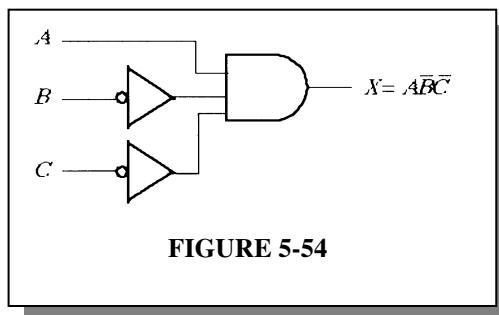
See Figure 5-53.



31. X is HIGH when A is HIGH, B is LOW, and C is LOW. We do not know if X is HIGH when all inputs are HIGH.

$$X = A\bar{B}\bar{C}$$

See Figure 5-54.



- 32.** See Figure 5-55.

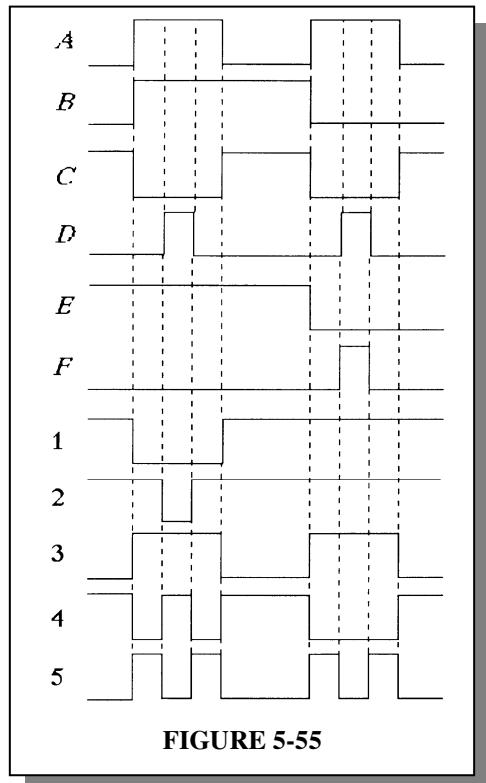


FIGURE 5-55

- 33.** The output pulse is sufficiently wide. It is greater than 25 ns. A maximum is not specified. See Figure 5-56.

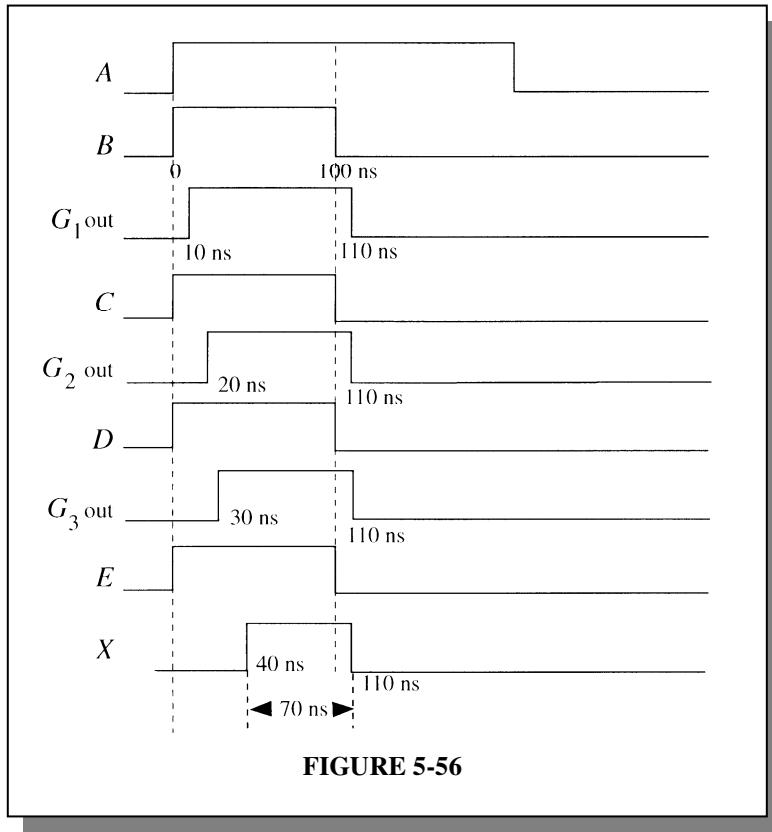


FIGURE 5-56

Chapter 5

Section 5-6 Combinational Logic with VHDL

34. entity 2 input NAND is

```
    port (A, B: in bit; X out bit);
end entity 2 input NAND;
architecture Function of 2input NAND is
begin
    X = not(A and B);
end architecture Function;
```

35. $X \leq A \text{ and } B \text{ and } C$

36. entity Circuit5_54b is

```
    port (A, B, C, D: in bit; X: out bit);
end entity Circuit5_54b;
architecture LogicFunction of Circuit5_54b is
begin
    X <= not(not A and B) or (not A and C and D) or (D and B and not D);
end architecture LogicFunction;
```

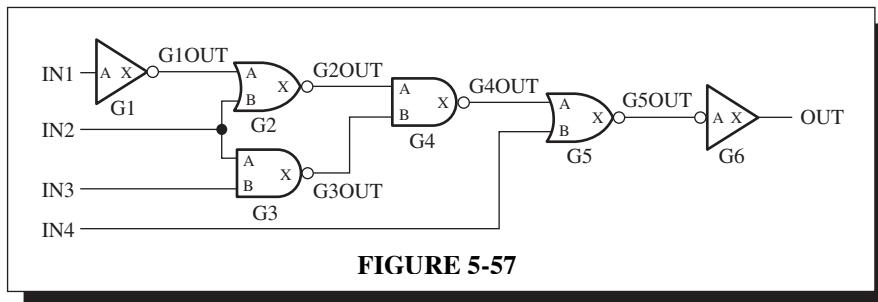
37. (e) entity Circuit5_55e is

```
    port (A, B, C: in bit; X: out bit);
end entity Circuit5_55e;
architecture LogicFunction of Circuit5_55e is
begin
    X <= (not A and B) or B or (B and not C) or (not A and not C) or (B and not C)
        or not C;
end architecture LogicFunction;
```

(f) entity Circuit5_55f is

```
    port (A, B, C: in bit; X: out bit);
end entity Circuit5_55f;
architecture LogicFunction of Circuit5_55f is
begin
    X <= (A or B) and (not B or C);
end architecture Logic Function;
```

38. See Figure 5-57 for input/output, gate, and signal labeling.



--Program for the logic circuit in Figure 5-57

```

entity (Circuit5_53d is
    port (IN1, IN2, IN3, IN4: in bit; OUT: out bit);
end entity Circuit5_53d;
architecture LogicOperation of Circuit5_53d is
--Component declaration for inverter
component Inverter is
    port (A: in bit; X: out bit);
end component Inverter;
--Component declaration for NOR gate
component NORgate is
    port (A, B: in bit; X: out bit);
end component NOR gate;
--Component declaration for NAND gate
component NANDgate is
    port (A, B: in bit; X: out bit);
end component NANDgate;
signal G1OUT, G2OUT, G3OUT, G4OUT, G5OUT: bit;
begin
    G1: Inverter port map (A => IN1, X => G1OUT);
    G2: NORgate port map (A => G1OUT, B => IN2, X => G2OUT);
    G3: NANDgate port map (A => IN2, B => IN3, X => G3OUT);
    G4: NANDgate port map (A => G2OUT, B => G3OUT, X => G4OUT);
    G5: NORgate port map (A => G4OUT, B => IN4, X => G5OUT);
    G6: Inverter port map (A => G5OUT, X => OUT);
end architecture LogicOperation;
```

39. See Figure 5-58 for input/output, gate, and signal labeling.

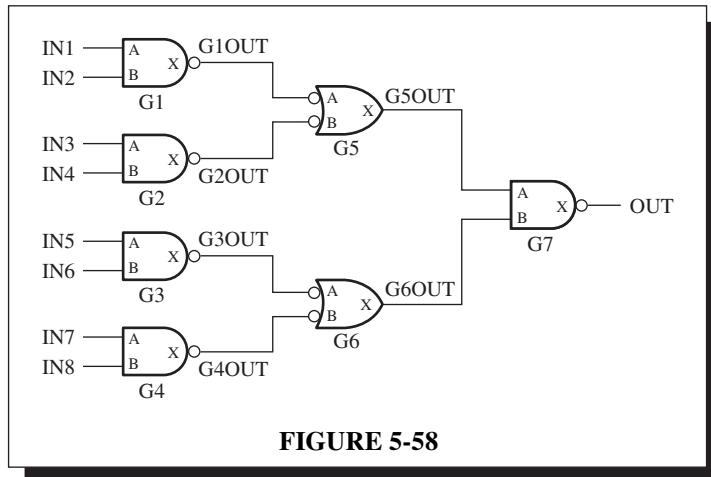


FIGURE 5-58

--Program for the logic circuit in Figure 5-58

```

entity Circuit5_53f is
    port (IN1, IN2, IN3, IN4, IN5, IN6, IN7, IN8: in bit; OUT: out bit);
end entity Circuit5_53f;
architecture LogicFunction of Circuit5_53f is
--Component declaration for NAND gate
component NANDgate is
```

Chapter 5

```

port (A, B: in bit; X: out bit);
end component NANDgate;
signal G1OUT, G2OUT, G3OUT, G4OUT, G5OUT, G6OUT: bit;
begin
    G1: NANDgate port map (A => IN1, B => IN2, X => G1OUT);
    G2: NANDgate port map (A => IN3, B => IN4, X => G2OUT);
    G3: NANDgate port map (A => IN5, B => IN6, X => G3OUT);
    G4: NANDgate port map (A => IN7, B => IN8, X => G4OUT);
    G5: NANDgate port map (A => G1OUT, B => G2OUT, X => G5OUT);
    G6: NANDgate port map (A => G3OUT, B => G4OUT, X => G6OUT);
    G7: NANDgate port map (A => G5OUT, B => G6OUT, X => OUT);
end architecture LogicFunction;

```

40. $X = \overline{ABC} + \overline{ABC} + \overline{ABC} + ABC$

This is the SOP expression for the function in Table 5-8 of the textbook. The following program applies the data flow approach for this logic function.

--Program for Table5_8 SOP logic

```

entity Table5_8 is
    port (A, B, C: in bit; X: out bit);
end entity Table5_8;
architecture LogicOperation of Table5_8 is
begin
    X <= (not A and not B and not C) or (not A and B and not C)
        or (A and not B and not C) or (A and B and not C) or (A and B and C);
end architecture LogicOperation;

```

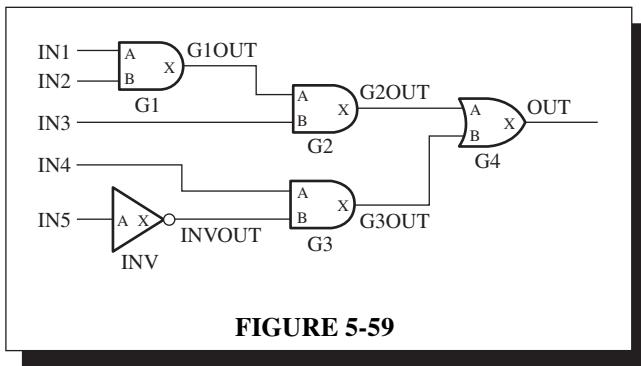
41. --Program for textbook Figure5_66 data flow approach

```

entity Fig5_69 is
    port (A, B, C, D, E: in bit; X: out bit);
end entity Fig5_69;
architecture DataFlow of Fig5_69 is
begin
    X <= (A and B and C) or (D and not E)
end architecture DataFlow;

```

See Figure 5-59 for the circuit in textbook Figure 5-66 modified for the structural approach.

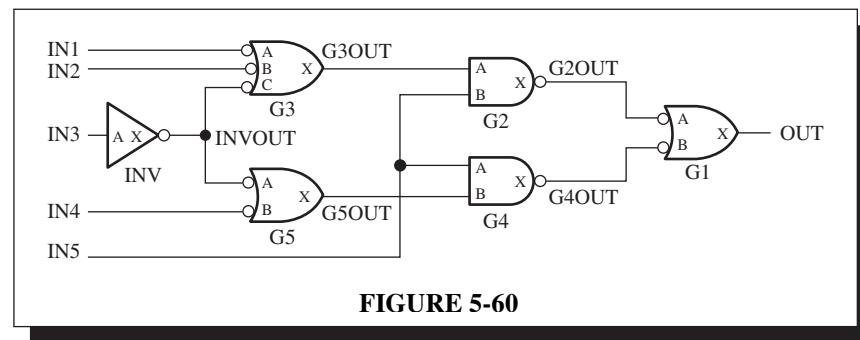


```
--Program for textbook Figure5_69 structural approach
entity Fig5_69 is
    port (IN1, IN2, IN3, IN4, IN5: in bit; OUT: out bit);
end entity Fig5_69;
architecture Structure of Fig5_69 is
--Component declaration for AND gate
component AND_gate is
    port (A, B: in bit; X: out bit);
end component AND_gate;
--Component declaration for OR gate
component OR_gate is
    port (A, B: in bit; X: out bit);
end component OR_gate;
--Component declaration for Inverter
component Inverter is
    port (A: in bit; X: out bit);
end component Inverter;
signal G1OUT, G2OUT, G3OUT, INVOUT: bit;
begin
    G1: AND_gate port map (A => IN1, B => IN2, X => G1OUT);
    G2: AND_gate port map (A => G1OUT, B => IN3, X => G2OUT);
    INV: Inverter port map (A => IN5, X => INVOUT);
    G3: AND_gate port map (A => IN4, B => INVOUT, X => G3OUT);
    G4: OR_gate port map (A => G2OUT, B => G3OUT, X => OUT);
end architecture Structure;
```

42. --Program for textbook Figure5_73 data flow approach

```
entity Fig5_73 is
    port (A, B, C, D, E: in bit; X: out bit);
end entity Fig5_73;
architecture DataFlow of Fig5_73 is
begin
    X <= (not A or not B or C) and E or (C or not D) and E;
end architecture DataFlow;
```

See Figure 5-60 for the circuit in textbook Figure 5-73 labeled for the structural approach.



Chapter 5

```
--Program for textbook Fig5_73 structural approach
entity Fig5_73 is
    port (IN1, IN2, IN3, IN4, IN5: in bit; OUT: out bit);
end entity Fig5_73;
architecture Structure of Fig5_73 is
--Component declaration for 3-input NAND gate
component NAND_gate3 is
    port (A, B, C: in bit; X: out bit);
end component NAND_gate3;
--Component declaration for 2-input NAND gate
component NAND_gate2 is
    port (A, B: in bit; X: out bit);
end component NAND_gate2;
--Component declaration for Inverter
component Inverter is
    port (A: in bit; X: out bit);
end component Inverter;
signal G2OUT, G3OUT, G4OUT, G5OUT, INVOUT: bit;
begin
    G1: NAND_gate2 port map (A => G2OUT, B => G4OUT, X => OUT);
    G2: NAND_gate2 port map (A => G3OUT, B => IN5, X => G2OUT);
    INV: Inverter port map (A => IN3, X => INVOUT);
    G3: NAND_gate3 port map (A => IN1, B => IN2, C => INVOUT, X => G3OUT);
    G4: NAND_gate2 port map (A => IN5, B => G5OUT, X => G4OUT);
    G5: NAND_gate2 port map (A => INVOUT, B => IN4, X => G5OUT);
end architecture Structure;
```

43. From the VHDL program, the logic expression is stated as a Boolean expression as follows:

$$\begin{aligned} X &= (\overline{\overline{AB}} + \overline{\overline{AC}} + \overline{\overline{AD}} + \overline{\overline{BC}} + \overline{\overline{BD}} + \overline{\overline{DC}}) \\ &= ((A+B)(A+C)(A+D)(B+C)(B+D)(D+C)) \\ &= (A+B)(A+C)(A+D)(B+C)(B+D)(D+C) \end{aligned}$$

The truth table is:

A	B	C	D	X
0	0	0	0	0
1	0	0	0	0
0	1	0	0	0
1	1	0	0	0
0	0	1	0	0
1	0	1	0	0
0	1	1	0	0
1	1	1	0	0
0	0	0	1	0
1	0	0	1	0
0	1	0	1	0
1	1	0	1	1
0	0	1	1	0
1	0	1	1	1
0	1	1	1	1
1	1	1	1	1

44. --Program for textbook Figure5_67 data flow approach
- ```

entity Fig5_67 is
 port (A1, A2, B1, B2: in bit; X: out bit);
end entity Fig5_67;
architecture LogicCircuit of Fig5_67 is
begin
 X <= (A1 and A2) or (A2 and not B1) or (not B1 and not B2) or (not B2 and A1);
end architecture LogicCircuit;
```

45. The AND gates are numbered top to bottom G1, G2, G3, G4. The OR gate is G5 and the inverters are, top to bottom. G6 and G7. Change  $A_1, A_2, B_1, B_2$  to IN1, IN2, IN3, IN4 respectively. Change X to OUT.

```

entity Circuit5_67 is
 port (IN1, IN2, IN3, (IN4: in bit; OUT: out bit);
end entity Circuit 5_67;
architecture Logic of Circuit 5_67 is
component AND_gate is
 port (A, B: in bit; X: out bit);
end component AND_gate;
component OR_gate is
 port (A, B, C, D: in bit; X: out bit);
end component OR_gate;
component Inverter is
 port (A: in bit; X: out bit);
end component Inverter;
signal G1OUT, G2OUT, G3OUT, G4OUT, G5OUT, G6OUT, G7OUT: bit;
begin
 G1: AND_gate port map (A => IN1, B => IN2, X => G1OUT);
 G2: AND_gate port map (A => IN2, B => G6OUT, X => G2OUT);
 G3: AND_gate port map (A => G6OUT, B => G7OUT, X => G3OUT);
 G4: AND_gate port map (A => G7OUT, B => IN1, X => G4OUT);
 G5: OR_gate port map (A => G1OUT, B => G2OUT, X => G3OUT,
 D => G4OUT, X => OUT);
 G6: Inverter port map (A => IN3, X => G6OUT);
 G7: Inverter port map (A => IN4, X => G7OUT);
end architecture Logic;
```

## **Section 5-7 Troubleshooting**

46.  $X = \overline{\overline{AB} + \overline{CD}} = ABCD$

X is HIGH only when  $ABCD$  are all HIGH. This does not occur in the waveforms, so X should remain LOW. **The output is incorrect.**

47.  $X = ABC + D\bar{E}$

Since X is the same as the  $G_3$  output, either  $G_1$  or  $G_2$  has failed with its output stuck LOW.

## Chapter 5

48.  $X = AB + CD + EF$

$X$  does not go HIGH when  $C$  and  $D$  are HIGH.  $G_2$  has failed with the output *open* or *stuck HIGH* or the corresponding input to  $G_4$  is *open*.

49. See Figure 5-61.

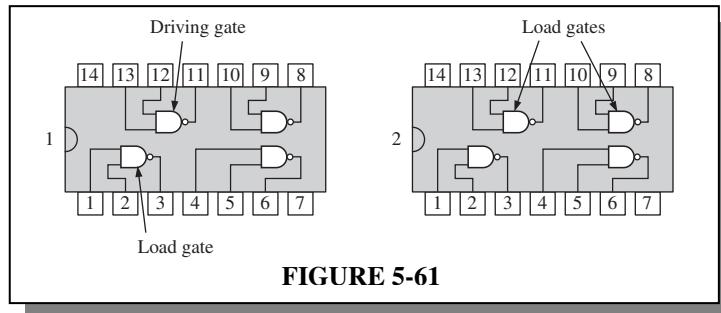


FIGURE 5-61

50.  $X = \overline{AB} + \overline{CD} + \overline{EF} = (\overline{AB})(\overline{CD})(\overline{EF}) = (A+B)(C+D)(E+F)$

Since  $X$  does not go HIGH when  $C$  or  $D$  is HIGH, the output of gate  $G_2$  must be *stuck LOW*.

51. (a) 
$$\begin{aligned} X &= (\overline{A} + \overline{B} + C)E + (C + \overline{D})E = \overline{A}E + \overline{B}E + CE + \cancel{CE} + \overline{DE} \\ &= \overline{A}E + \overline{B}E + CE + \overline{DE} \end{aligned}$$

See Figure 5-62.

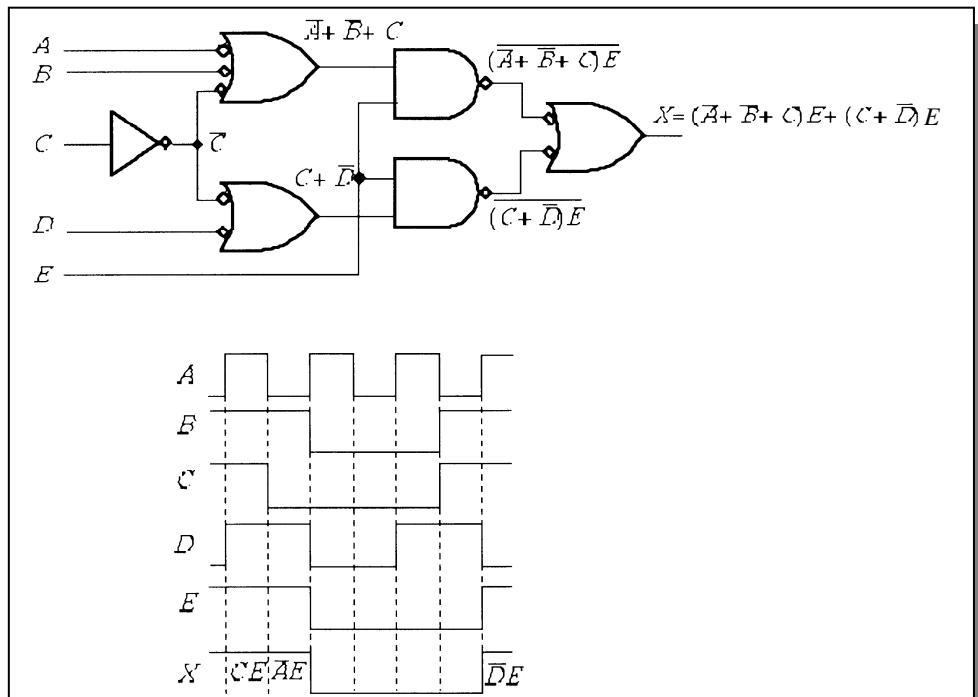


FIGURE 5-62

$$(b) \quad X = E + E(\bar{D} + C) = E(1 + \bar{D} + C) = E$$

Waveform  $X$  is the same as waveform  $E$ , in Figure 5-61. Since this is the correct waveform, the open output of gate  $G_3$  does not show up for this *particular* set of input waveforms.

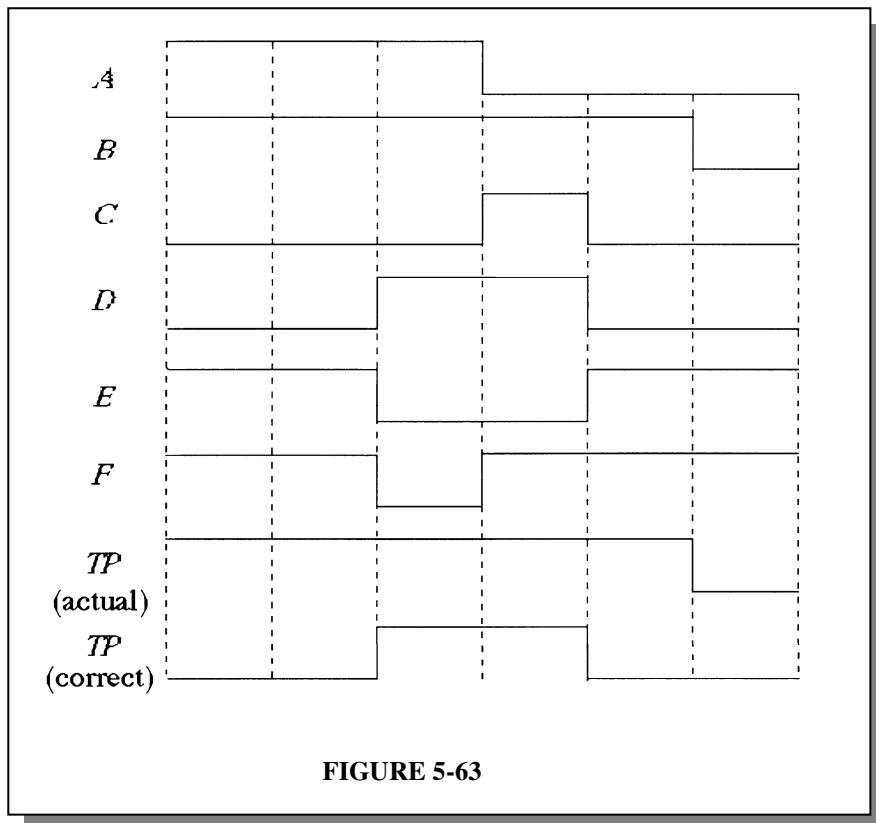
$$(c) \quad X = E + E(\bar{A} + \bar{B} + C) = E(1 + \bar{A} + \bar{B} + C) = E$$

Again waveform  $X$  is the same as waveform  $E$ . As strange as it may seem, the shorted input to  $G_5$  does not affect the output for this *particular* set of input waveforms.

Conclusion: the two faults are not indicated in the output waveform for these particular inputs.

**52.**  $TP = \overline{\overline{AB} + \overline{CD}}$

The output of the  $\overline{CD}$  gate is *stuck LOW*. See Figure 5-66.



### *Applied Logic*

- 53.** The flow sensor measures the rate of flow of the solution into the tank.  
 The temperature transducer measures temperature of the mixture.  
 The level sensors indicate when the solution is at the minimum or maximum level.

## Chapter 5

54.  $V_{\text{inlet}} = \bar{L}_{\text{min}} + \bar{L}_{\text{max}} F_{\text{inlet}}$

See Figure 5-63.

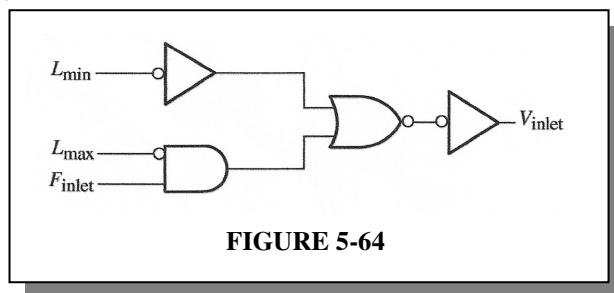


FIGURE 5-64

55.  $V_{\text{outlet}} = L_{\text{min}} \bar{F}_{\text{inlet}} T$

See Figure 5-64.

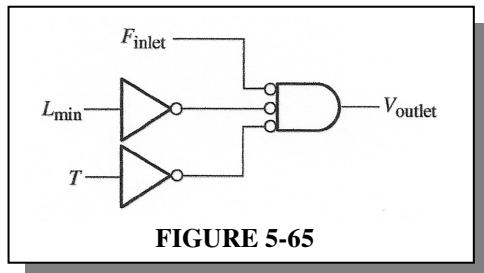


FIGURE 5-65

56. See Figure 5-65

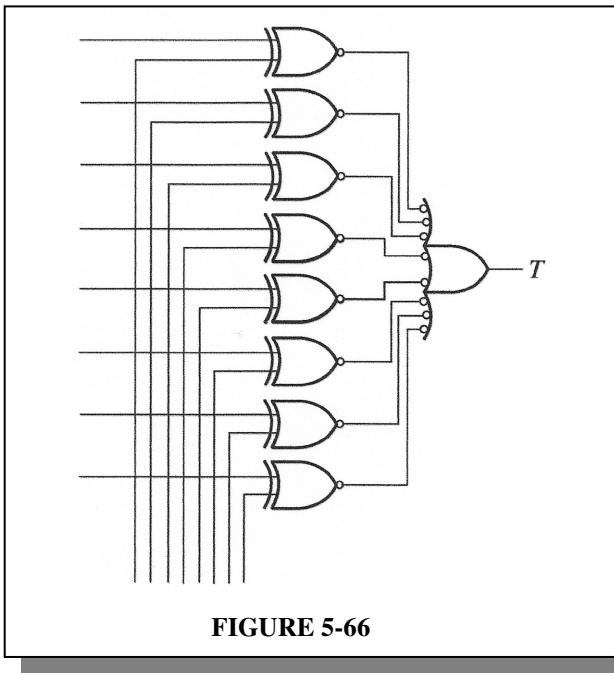


FIGURE 5-66

57.  $V_{\text{additive}} = TL_{\min}$

See Figure 5-66.

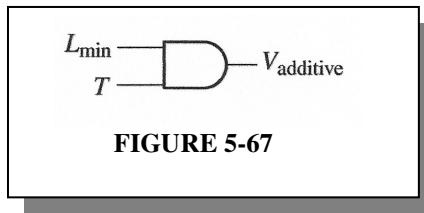


FIGURE 5-67

### Special Design Problems

58.

| $A_3$ | $A_2$ | $A_1$ | $A_0$ | $X$ |
|-------|-------|-------|-------|-----|
| 0     | 0     | 0     | 0     | 1   |
| 0     | 0     | 0     | 1     | 1   |
| 0     | 0     | 1     | 0     | 1   |
| 0     | 0     | 1     | 1     | 0   |
| 0     | 1     | 0     | 0     | 0   |
| 0     | 1     | 0     | 1     | 0   |
| 0     | 1     | 1     | 0     | 0   |
| 0     | 1     | 1     | 1     | 0   |
| 1     | 0     | 0     | 0     | 0   |
| 1     | 0     | 0     | 1     | 0   |
| 1     | 0     | 1     | 0     | 0   |
| 1     | 0     | 1     | 1     | 0   |
| 1     | 1     | 0     | 0     | 0   |
| 1     | 1     | 0     | 1     | 1   |
| 1     | 1     | 1     | 0     | 1   |
| 1     | 1     | 1     | 1     | 1   |

See Figure 5-67.

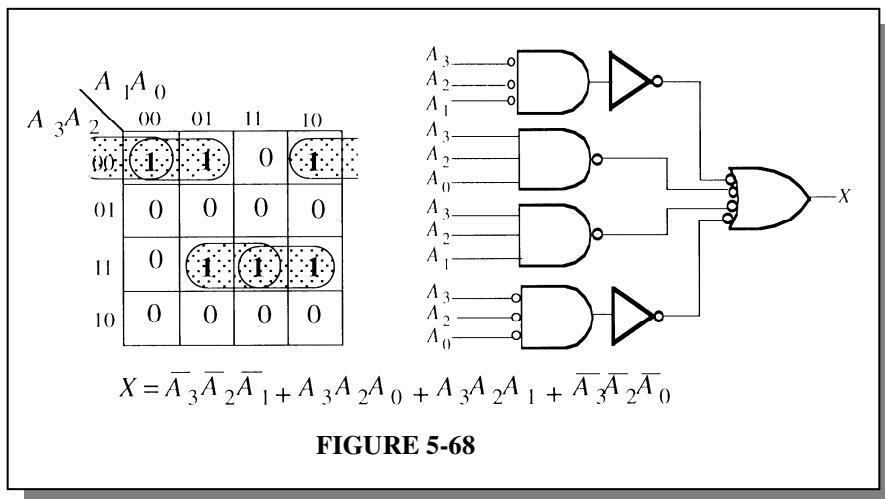


FIGURE 5-68

## Chapter 5

59. Let

$X$  = Lamp on

$A$  = Front door switch on

$\bar{A}$  = Front door switch off

$B$  = Back door switch on

$\bar{B}$  = Back door switch off

$X = A\bar{B} + \bar{A}B$ . This is an XOR operation.

See Figure 5-68.

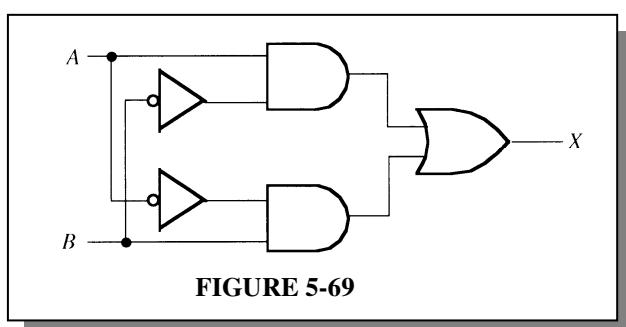


FIGURE 5-69

60. See Figure 5-69.

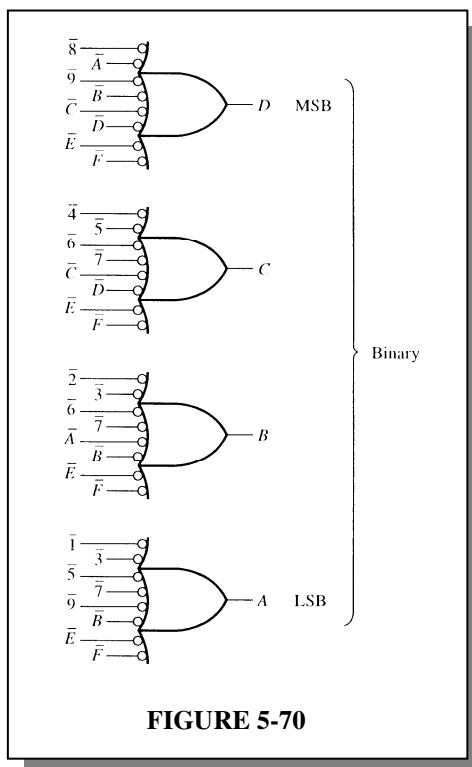


FIGURE 5-70

***Multisim Troubleshooting Practice***

- 61.** Output of U3A shorted to ground.
- 62.** Output of U3C is shorted to VCC.
- 63.** The output of U2A is always HIGH (shorted to VCC).
- 64.** Switch D is shorted to ground.

---

## CHAPTER 6

### FUNCTIONS OF COMBINATIONAL LOGIC

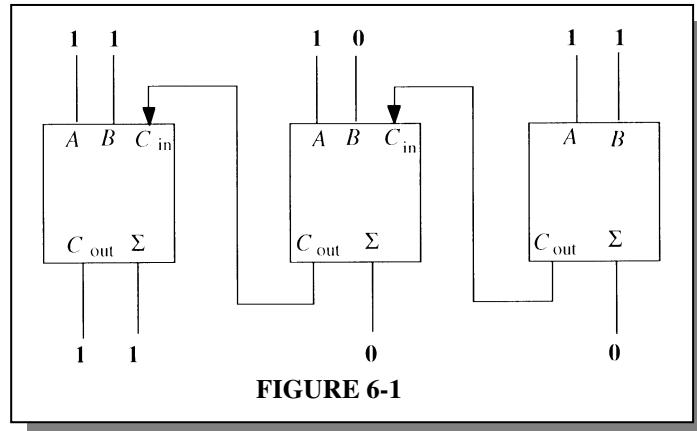
---

#### Section 6-1 Half and Full Adders

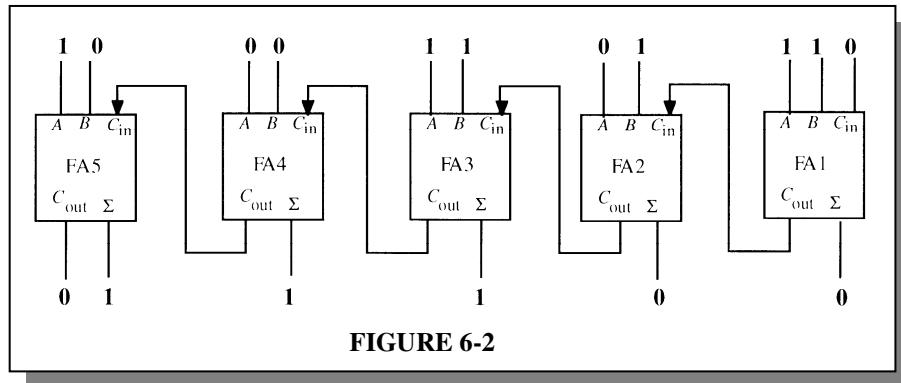
1. (a) XOR (upper) output = 0, Sum output = 1, AND (upper) output = 0, AND (lower) output = 1, Carry output = 1  
(b) XOR (upper) output = 1, Sum output = 0, AND (upper) output = 1, AND (lower) output = 0, Carry output = 1  
(c) XOR (upper) output = 1, Sum output = 1, AND (upper) output = 0, AND (lower) output = 0, Carry output = 0
2. (a)  $A = 0, B = 0, C_{in} = 0$   
(b)  $A = 1, B = 0, C_{in} = 0$  or  $A = 0, B = 1, C_{in} = 0$   
or  $A = 0, B = 0, C_{in} = 1$   
(c)  $A = 1, B = 1, C_{in} = 1$   
(d)  $A = 1, B = 1, C_{in} = 0$  or  $A = 0, B = 1, C_{in} = 1$   
or  $A = 1, B = 0, C_{in} = 1$
3. (a)  $\Sigma = 1, C_{out} = 0$                                                   (b)  $\Sigma = 1, C_{out} = 0$   
(c)  $\Sigma = 0, C_{out} = 1$                                                   (d)  $\Sigma = 1, C_{out} = 1$

#### Section 6-2 Parallel Binary Adders

4. 
$$\begin{array}{r} 111 \\ 101 \\ \hline 1100 \end{array}$$
 See Figure 6-1.



5. 
$$\begin{array}{r} 10101 \\ 00111 \\ \hline 11100 \end{array}$$
 See Figure 6-2.



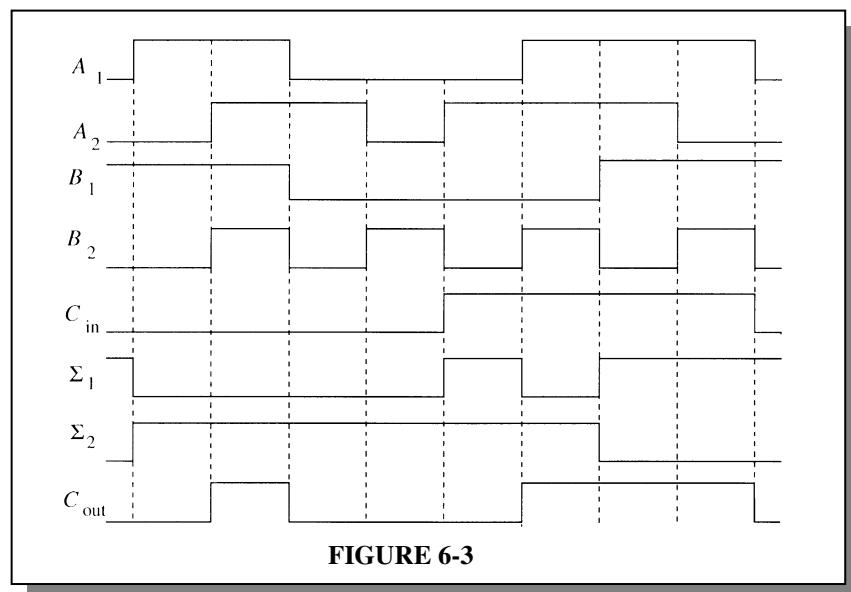
6. (a) When the Add/Subt is HIGH, the two numbers are subtracted.

(b) When the input is LOW, the numbers are added.

7.  $A = 1001 = -7, B = 1100 = -4$

$$\begin{aligned} &1001 \\ &0011 \leftarrow \text{Complement of } B \\ &\underline{1101} \leftarrow \text{LSB Carry input} \\ &1101 = -3 \text{ in 2's comp} \end{aligned}$$

8. See Figure 6-3.



## Chapter 6

9.

| $A_4$ | $A_3$ | $A_2$ | $A_1$ | $B_4$ | $B_3$ | $B_2$ | $B_1$ | $\Sigma_5$ | $\Sigma_4$ | $\Sigma_3$ | $\Sigma_2$ | $\Sigma_1$ |
|-------|-------|-------|-------|-------|-------|-------|-------|------------|------------|------------|------------|------------|
| 1     | 0     | 0     | 1     | 0     | 0     | 0     | 1     | 0          | 1          | 0          | 1          | 0          |
| 1     | 0     | 1     | 0     | 1     | 1     | 0     | 1     | 0          | 0          | 1          | 1          | 1          |
| 0     | 0     | 1     | 0     | 0     | 0     | 1     | 1     | 0          | 0          | 1          | 0          | 1          |
| 1     | 0     | 1     | 1     | 0     | 1     | 1     | 1     | 1          | 0          | 0          | 1          | 0          |

$$\Sigma_1 = 0110$$

$$\Sigma_2 = 1011$$

$$\Sigma_3 = 0110$$

$$\Sigma_4 = 0001$$

$$\Sigma_5 = 1000$$

10. 0100

$$\begin{array}{r} 1110 \\ + 10010 \\ \hline \end{array}$$

$\Sigma$  outputs should be  $C_{\text{out}}\Sigma_4\Sigma_3\Sigma_2\Sigma_1 = 10010$ .

The  $\Sigma_3$  output (pin 2) is HIGH and should be LOW.

See Figure 6-4.

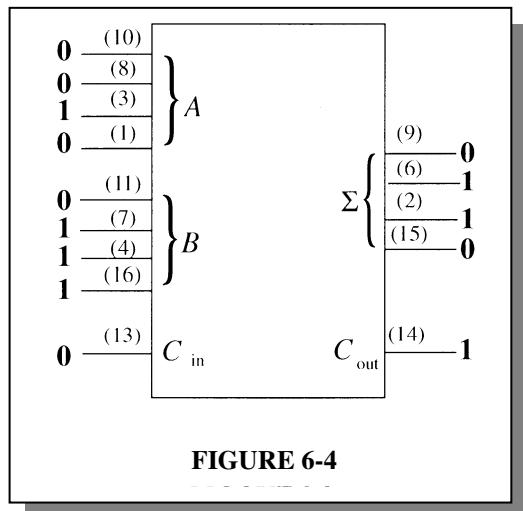


FIGURE 6-4

### Section 6-3 Ripple Carry and Look-Ahead Carry Adders

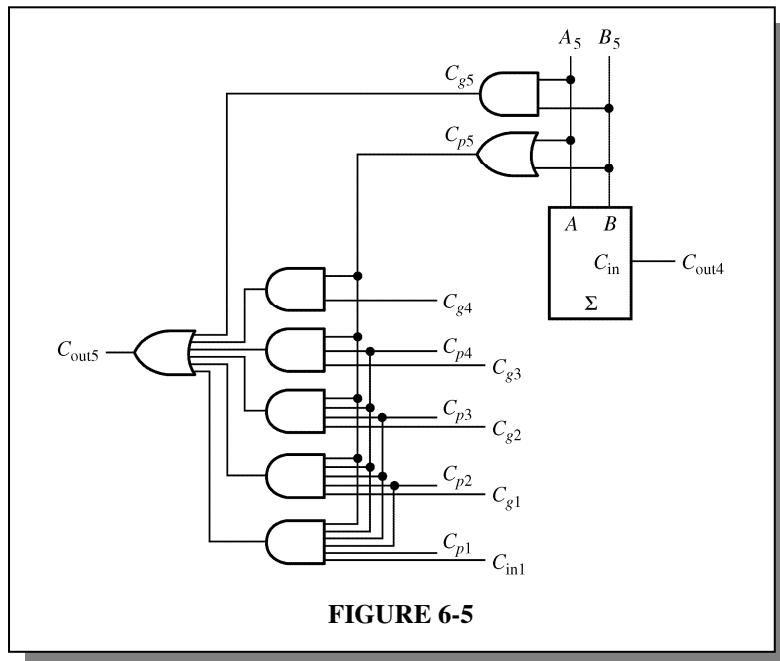
11.  $t_p(\text{tot}) = 40 \text{ ns} + 6(25 \text{ ns}) + 35 \text{ ns} = 225 \text{ ns}$

12. Full-adder 5:

$$C_{in5} = C_{out4}$$

$$C_{out5} = C_{g5} + C_{p5}C_{g4} + C_{p5}C_{p4}C_{g3} + C_{p5}C_{p4}C_{p3}C_{g2} + C_{p5}C_{p4}C_{p3}C_{g2}C_{g1} + C_{p5}C_{p4}C_{p3}C_{p2}C_{p1}C_{in1}$$

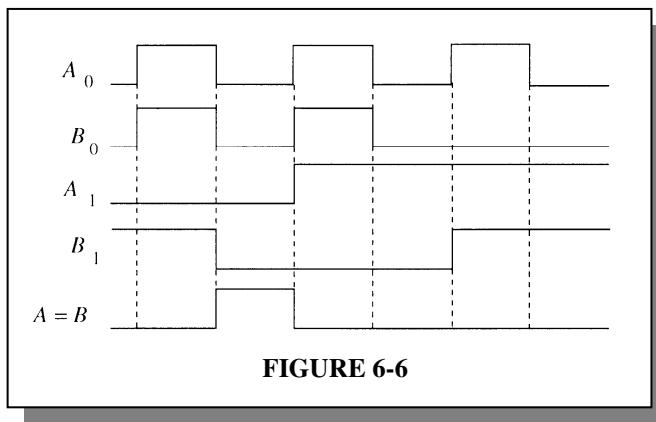
The logic to be added to text Figure 6-18 is shown in Figure 6-5.



#### **Section 6-4 Comparators**

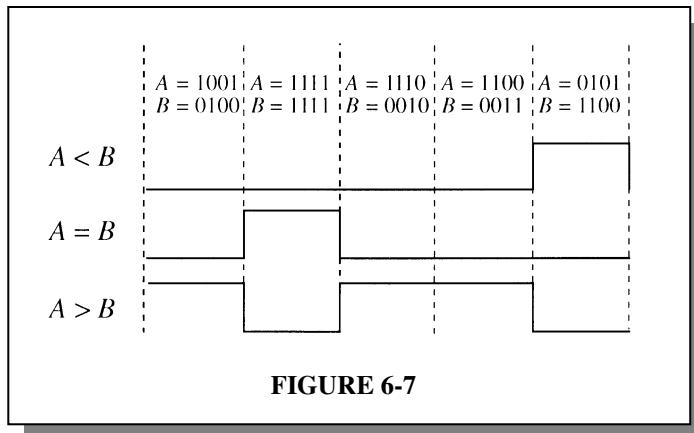
13. The  $A = B$  output is HIGH when  $A_0 = B_0$  and  $A_1 = B_1$ .

See Figure 6-6.



## *Chapter 6*

**14.** See Figure 6-7.

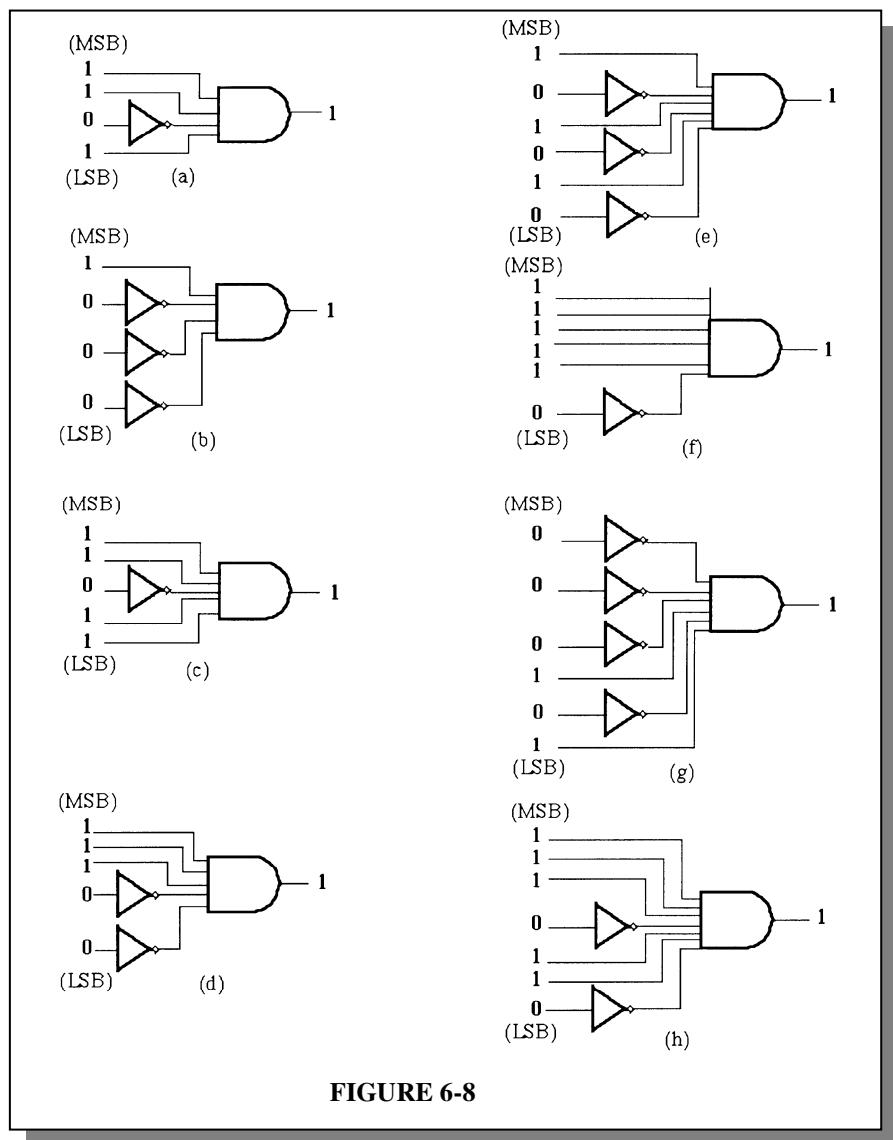


- 15.** (a)  $A > B: 1, A = B: 0, A < B: 0$   
(b)  $A > B: 0, A = B: 0, A < B: 1$   
(c)  $A > B: 0, A = B: 1, A < B: 0$

### *Section 6-5 Decoders*

- 16.** (a)  $A_3A_2A_1A_0 = \mathbf{1110}$       (b)  $A_3A_2A_1A_0 = \mathbf{1100}$   
(c)  $A_3A_2A_1A_0 = \mathbf{1111}$       (d)  $A_3A_2A_1A_0 = \mathbf{1000}$

17. See Figure 6-8.

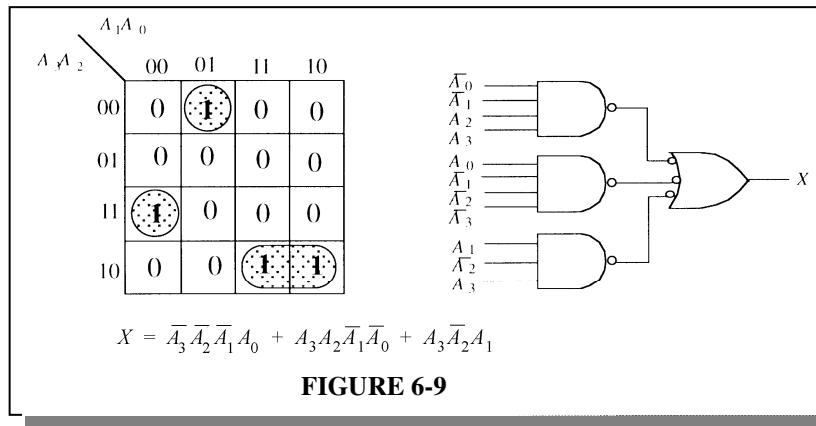


**FIGURE 6-8**

18. Change the AND gates to NAND gates in Figure 6-8.

$$19. X = \overline{A_3} \overline{A_2} \overline{A_1} A_0 + A_3 \overline{A_2} A_1 \overline{A_0} + A_3 A_2 \overline{A_1} \overline{A_0} + A_3 \overline{A_2} A_1 A_0$$

See Figure 6-9.



**FIGURE 6-9**

## Chapter 6

20.  $Y = A_2 A_1 \overline{A_0} + A_2 \overline{A_1} A_0 + \overline{A_2} A_1 \overline{A_0}$

See Figure 6-10.

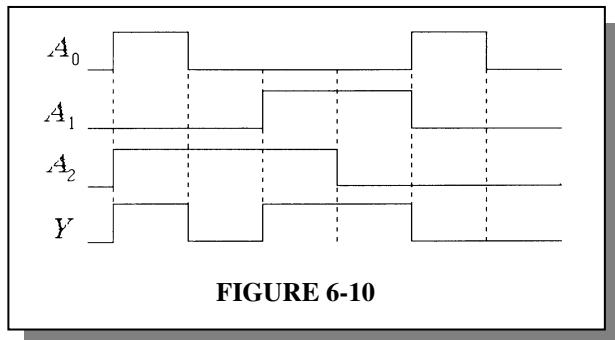


FIGURE 6-10

21. See Figure 6-11.

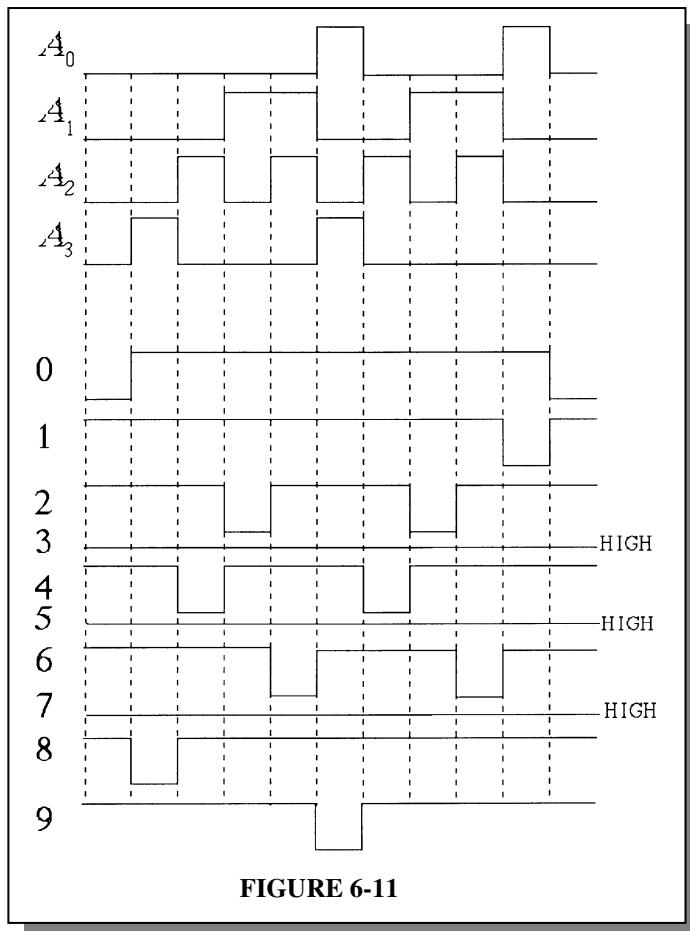


FIGURE 6-11

22. 0 1 6 9 4 4 4 8 0

### **Section 6-6 Encoders**

**23.**  $A_0, A_1$ , and  $A_3$  are HIGH.  $A_3A_2A_1A_0 = 1011$ , which is an invalid BCD code.

**24.** Pin 2 is for decimal 5, pin 5 is for decimal 8, and pin 12 is for decimal 2.  
The highest priority input is pin 5.

The completed outputs are:  $\overline{A_3}\overline{A_2}\overline{A_1}\overline{A_0} = 0111$ , which is binary 8 (1000).

### **Section 6-7 Code Converters**

**25.** (a)  $2_{10} = \mathbf{0010}_{\text{BCD}} = \mathbf{0010}_2$

(b)  $8_{10} = \mathbf{1000}_{\text{BCD}} = \mathbf{1000}_2$

(c)  $13_{10} = \mathbf{00010011}_{\text{BCD}} = \mathbf{1101}_2$

(d)  $26_{10} = \mathbf{00100110}_{\text{BCD}} = \mathbf{11010}_2$

(e)  $33_{10} = \mathbf{00110011}_{\text{BCD}} = \mathbf{100001}_2$

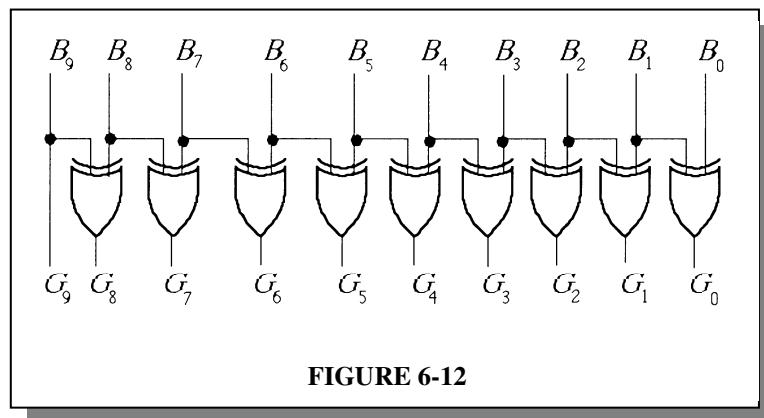
**26.** (a)  $1010101010$  binary  
 $1111111111$  gray

(b)  $11111100000$  binary  
 $1000010000$  gray

(c)  $0000001110$  binary  
 $0000001001$  gray

(d)  $1111111111$  binary  
 $1000000000$  gray

See Figure 6-12.



**27.** (a)  $1010000000$  gray  
 $1100000000$  binary

(b)  $0011001100$  gray  
 $0010001000$  binary

(c)  $1111000111$  gray  
 $1010000101$  binary

(d)  $0000000001$  gray  
 $0000000001$  binary

See Figure 6-13.

## Chapter 6

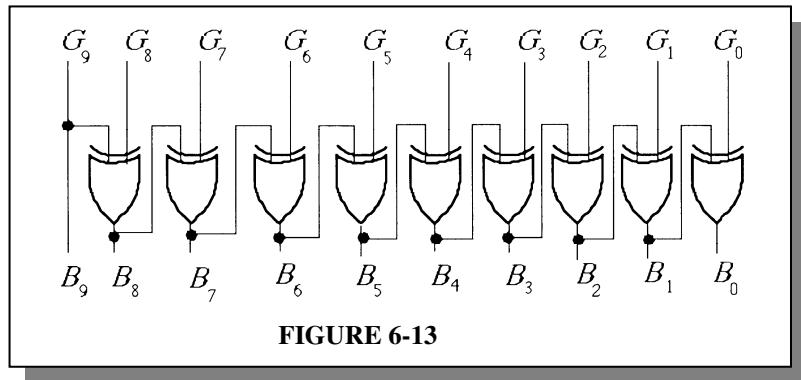


FIGURE 6-13

### Section 6-8 Multiplexers (Data Selectors)

28.  $S_1S_0 = 01$  selects  $D_1$ , therefore  $Y = 1$ .

29. See Figure 6-14.

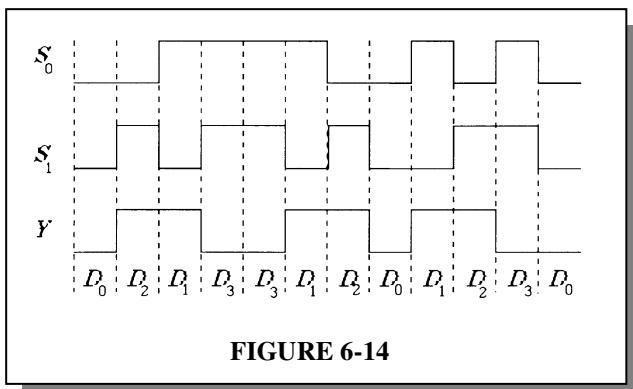


FIGURE 6-14

30. See Figure 6-15.

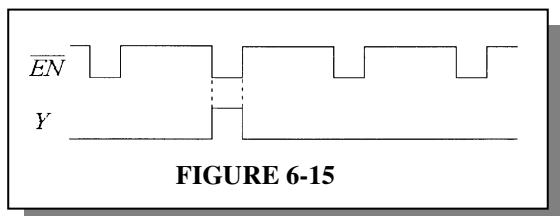
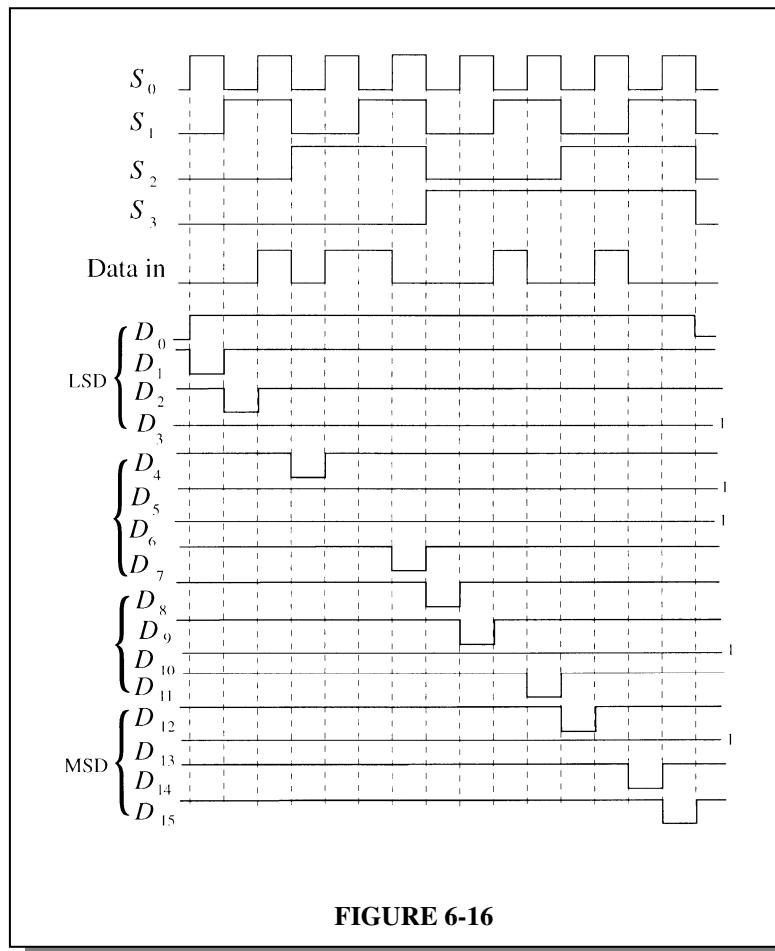


FIGURE 6-15

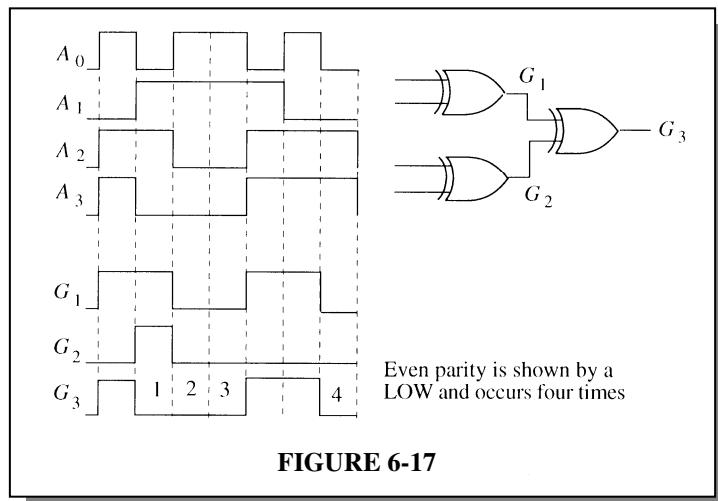
### **Section 6-9 Demultiplexers**

**31.** See Figure 6-16.



### **Section 6-10 Parity Generators/Checkers**

**32.** See Figure 6-17.



## Chapter 6

33. See Figure 6-18.

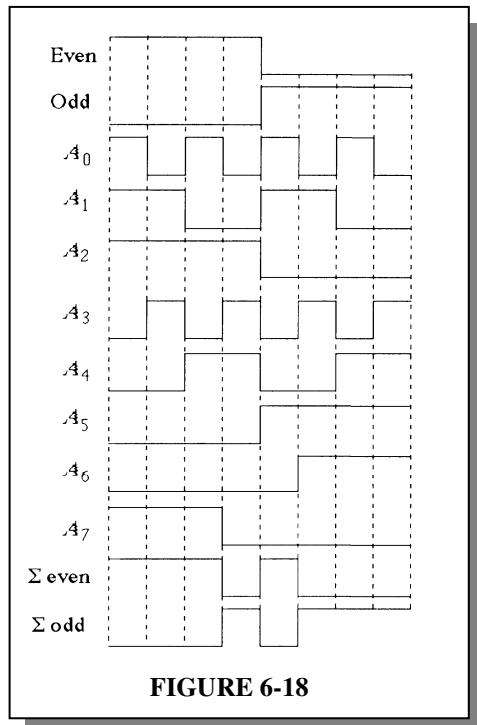


FIGURE 6-18

### Section 6-11 Troubleshooting

34. The outputs given in the problem are incorrect. By observation of these incorrect waveforms, we can conclude that the outputs of the device are not open or shorted because both waveforms are changing.

Observe that at the beginning of the timing diagram all inputs are 0 but the sum is 1. This indicates that an input is stuck HIGH. Start by assuming that  $C_{\text{in}}$  is stuck HIGH. This results in  $\Sigma$  and  $C_{\text{out}}$  output waveforms that match the waveforms given in the problem, indicating that  $C_{\text{in}}$  is indeed stuck HIGH, perhaps shorted to  $V_{\text{CC}}$ .

See Figure 6-19 for the correct output waveforms.

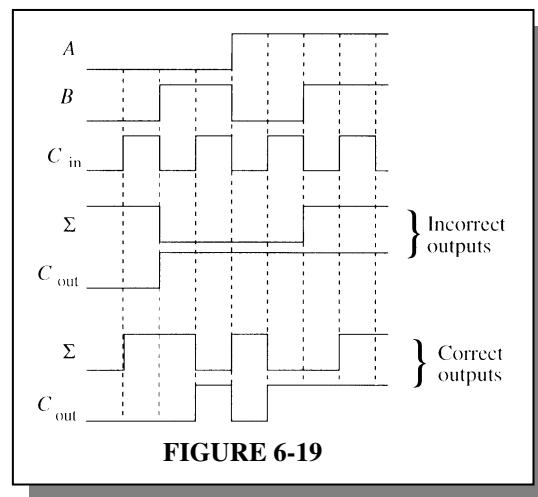


FIGURE 6-19

35. (a) OK (b) Segment *g* burned out; output G open (c) Segment *b* output stuck LOW
36. Step 1: Verify that the supply voltage is applied.  
 Step 2: Go through the key sequence and verify the output code in Table 1.

| Key  | $A_3$ | $A_2$ | $A_1$ | $A_0$ |
|------|-------|-------|-------|-------|
| None | 1     | 1     | 1     | 1     |
| 0    | 1     | 1     | 1     | 1     |
| 1    | 1     | 1     | 1     | 0     |
| 2    | 1     | 1     | 0     | 1     |
| 3    | 1     | 1     | 0     | 0     |
| 4    | 1     | 0     | 1     | 1     |
| 5    | 1     | 0     | 1     | 0     |
| 6    | 1     | 0     | 0     | 1     |
| 7    | 1     | 0     | 0     | 0     |
| 8    | 0     | 1     | 1     | 1     |
| 9    | 0     | 1     | 1     | 0     |

**TABLE 1**

Step 3: Check for proper priority operation by repeating the key sequence in Table 1 except that for each key closure, hold that key down and depress each lower-valued key as specified in Table 2.

| Hold down keys | Depress keys one at a time | $A_3$ | $A_2$ | $A_1$ | $A_0$ |
|----------------|----------------------------|-------|-------|-------|-------|
| 1              | 0                          | 1     | 1     | 1     | 0     |
| 2              | 1, 0                       | 1     | 1     | 0     | 1     |
| 3              | 2, 1, 0                    | 1     | 1     | 0     | 0     |
| 4              | 3, 2, 1, 0                 | 1     | 0     | 1     | 1     |
| 5              | 4, 3, 2, 1, 0              | 1     | 0     | 1     | 0     |
| 6              | 5, 4, 3, 2, 1, 0           | 1     | 0     | 0     | 1     |
| 7              | 6, 5, 4, 3, 2, 1, 0        | 1     | 0     | 0     | 0     |
| 8              | 7, 6, 5, 4, 3, 2, 1, 0     | 0     | 1     | 1     | 1     |
| 9              | 8, 7, 6, 5, 4, 3, 2, 1, 0  | 0     | 1     | 1     | 0     |

**TABLE 2**

37. (a) Open  $A_1$  input acts as a HIGH. All binary values corresponding to a BCD number having a 1's value of 0, 1, 4, 5, 8, or 9 will be off by 2. This will first be seen for a BCD value of 00000000.  
 (b) Open  $C_{out}$  of top adder. All values not normally involving a carry out will be off by 32. This will first be seen for a BCD value of 00000000.  
 (c) The  $\Sigma_4$  output of top adder is shorted to ground. Same binary values above 15 will be short by 16. The first BCD value to indicate this will be 00011000.  
 (d)  $\Sigma_3$  of bottom adder is shorted to ground. Every other set of 16 value starting with 16 will be short 16. The first BCD value to indicate this will be 00010110.
38. (a) The 1Y1 output of the 74LS139 is *stuck HIGH* or *open*; B cathode open.  
 (b) No power; EN input to the 74LS139 is *open*.  
 (c) The  $f$  output of the 74LS48 is *stuck HIGH*.  
 (d) The frequency of the data select input is too *low*.

## Chapter 6

- 39.**
1. Place a LOW on pin 7 (Enable).
  2. Apply a HIGH to  $D_0$  and a LOW to  $D_1$  through  $D_7$ .
  3. Go through the binary sequence on the select inputs and check  $Y$  and  $\bar{Y}$  according to Table 3.

| $S_2$ | $S_1$ | $S_0$ | $Y$ | $\bar{Y}$ |
|-------|-------|-------|-----|-----------|
| 0     | 0     | 0     | 1   | 0         |
| 0     | 0     | 1     | 0   | 1         |
| 0     | 1     | 0     | 0   | 1         |
| 0     | 1     | 1     | 0   | 1         |
| 1     | 0     | 0     | 0   | 1         |
| 1     | 0     | 1     | 0   | 1         |
| 1     | 1     | 0     | 0   | 1         |
| 1     | 1     | 1     | 0   | 1         |

**TABLE 3**

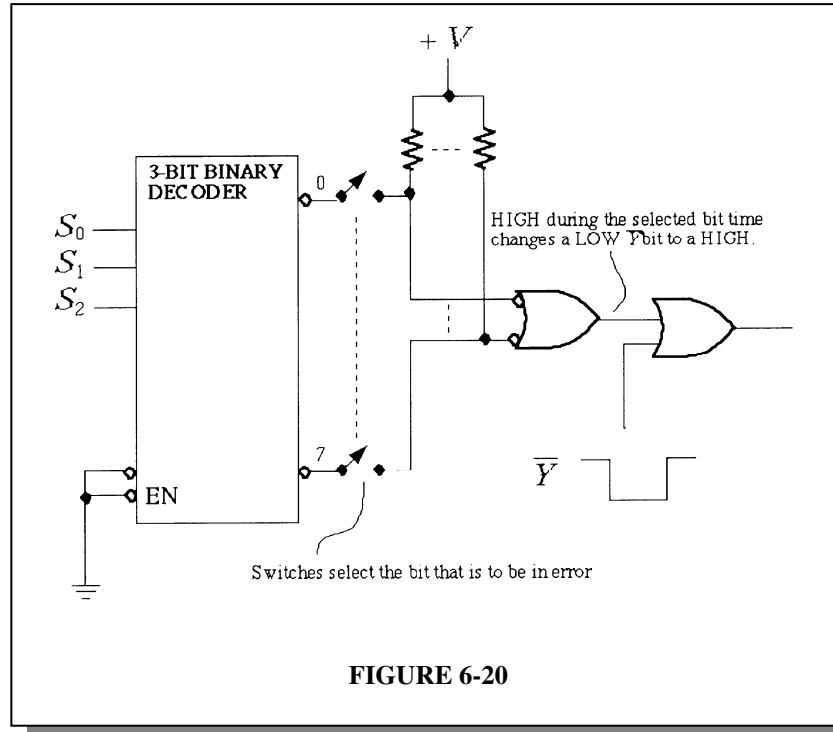
- 4.** Repeat the binary sequence of select inputs for each set of data inputs listed in Table 4. A HIGH on the  $Y$  output should occur only for the corresponding combinations of select inputs shown.

| $D_0$ | $D_1$ | $D_2$ | $D_3$ | $D_4$ | $D_5$ | $D_6$ | $D_7$ | $Y$ | $\bar{Y}$ | $S_2$ | $S_1$ | $S_0$ |
|-------|-------|-------|-------|-------|-------|-------|-------|-----|-----------|-------|-------|-------|
| L     | H     | L     | L     | L     | L     | L     | L     | 1   | 0         | 0     | 0     | 1     |
| L     | L     | H     | L     | L     | L     | L     | L     | 1   | 0         | 0     | 1     | 0     |
| L     | L     | L     | H     | L     | L     | L     | L     | 1   | 0         | 0     | 1     | 1     |
| L     | L     | L     | L     | H     | L     | L     | L     | 1   | 0         | 1     | 0     | 0     |
| L     | L     | L     | L     | L     | H     | L     | L     | 1   | 0         | 1     | 0     | 1     |
| L     | L     | L     | L     | L     | L     | H     | L     | 1   | 0         | 1     | 1     | 0     |
| L     | L     | L     | L     | L     | L     | H     | L     | 1   | 0         | 1     | 1     | 0     |
| L     | L     | L     | L     | L     | L     | L     | H     | 1   | 0         | 1     | 1     | 1     |

**TABLE 4**

- 40.** The  $\Sigma$  EVEN output of the 74LS280 should be HIGH and the output of the error gate should be HIGH because of the error condition. Possible faults are:
1.  $\Sigma$  EVEN output of the 74LS280 stuck *LOW*.
  2. Error gate faulty.
  3. The ODD input to the 74LS280 is *open* thus acting as a HIGH.
  4. The inverter going to the ODD input of the 74LS280 has an *open* output or the output is stuck *HIGH*.
- 41.** Apply a HIGH in turn to each Data input,  $D_0$  through  $D_7$  with LOWs on all the other inputs. For each HIGH applied to a data input, sequence through all eight binary combinations of select inputs ( $S_2S_1S_0$ ) and check for a HIGH on the corresponding data output and LOWs on all the other data outputs.

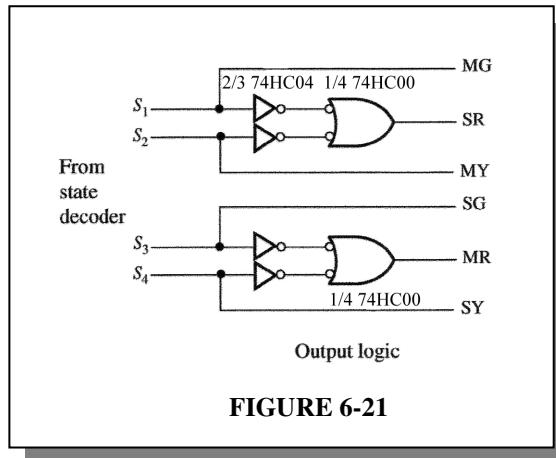
One possible approach to implementation is to decode the  $S_2S_1S_0$  inputs and generate an inhibit pulse during any given bit time as determined by the settings of seven switches. The inhibit pulse effectively changes a LOW on the  $Y$  serial data line to a HIGH during the selected bit time(s), thus producing a bit error. A basic diagram of this approach is shown in Figure 6-20.



**FIGURE 6-20**

### *Applied Logic*

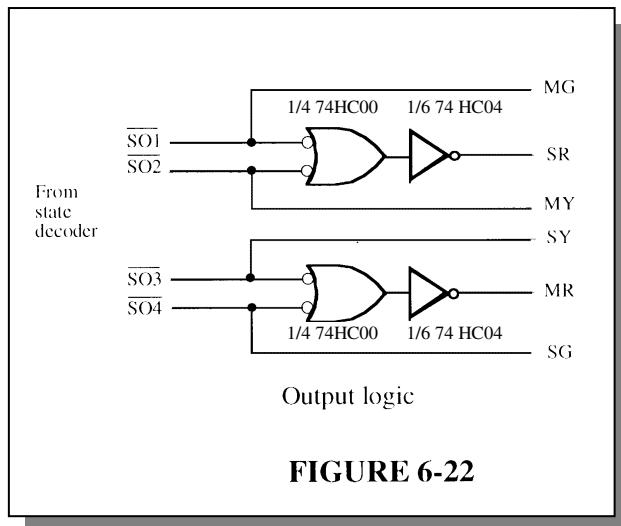
42. See Figure 6-21.



**FIGURE 6-21**

## Chapter 6

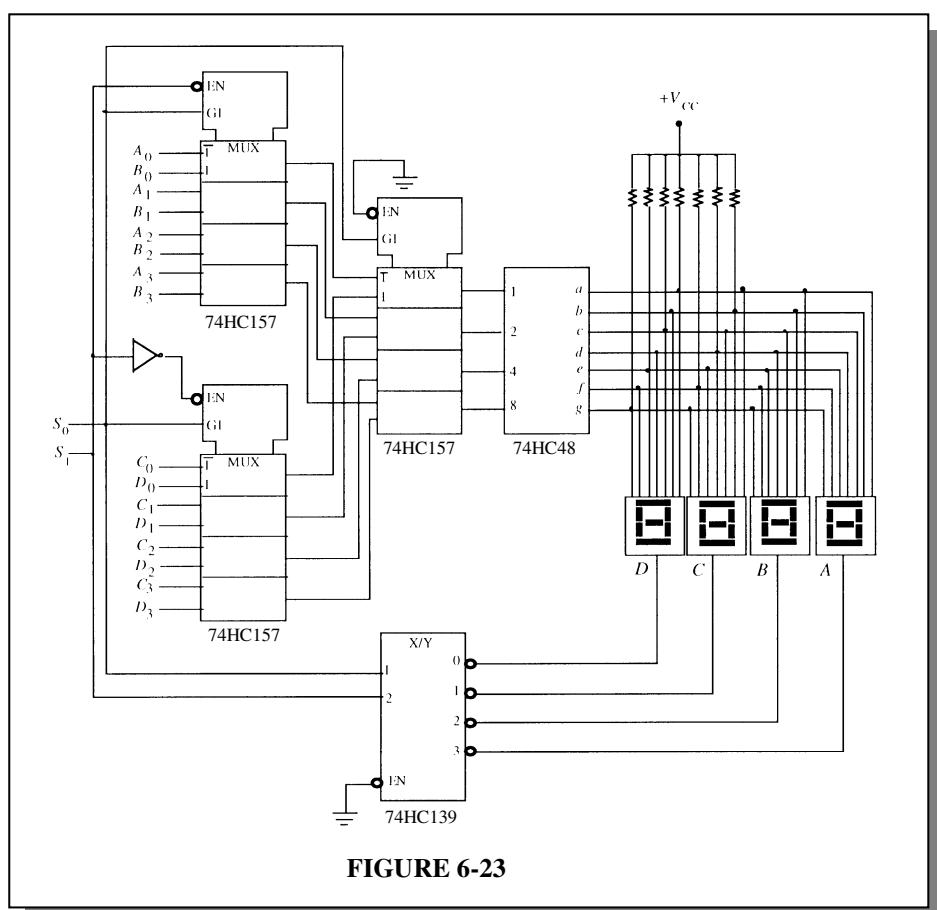
43. See Figure 6-22.



**FIGURE 6-22**

### Special Design Problems

44. See Figure 6-23.



**FIGURE 6-23**

45.  $\Sigma = \overline{A}\overline{B}C_{\text{in}} + \overline{ABC}_{\text{in}} + A\overline{B}\overline{C}_{\text{in}} + ABC_{\text{in}}$   
 $C_{\text{out}} = ABC_{\text{in}} + \overline{ABC}_{\text{in}} + A\overline{B}C_{\text{in}} + A\overline{BC}_{\text{in}}$

See Figure 6-24.

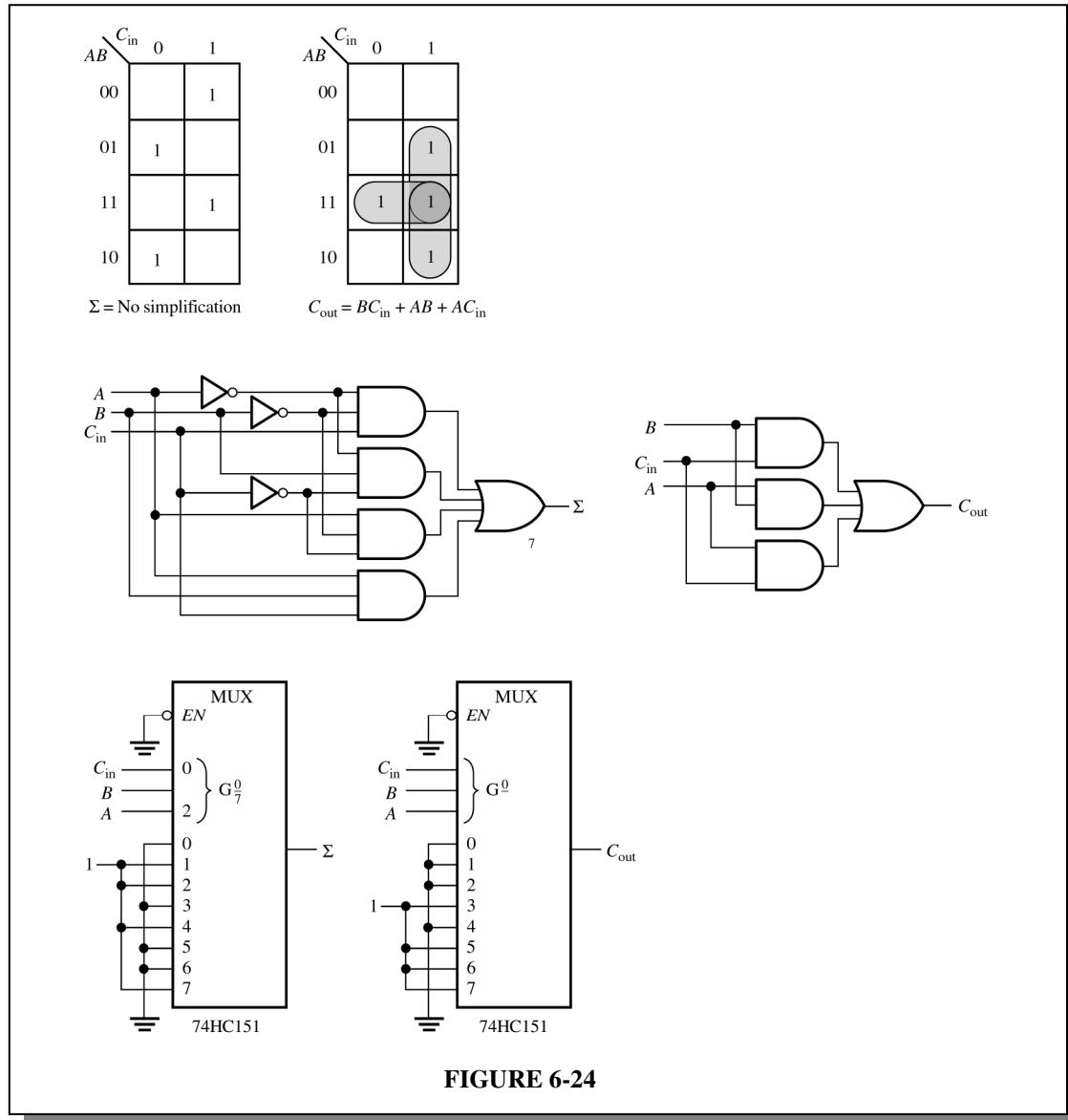


FIGURE 6-24

## Chapter 6

46. 
$$Y = \overline{A_3} \overline{A_2} A_1 \overline{A_0} + \overline{A_3} \overline{A_2} A_1 A_0 + \overline{A_3} A_2 A_1 \overline{A_0} + \overline{A_3} A_2 A_1 A_0 + A_3 \overline{A_2} \overline{A_1} \overline{A_0}$$
  

$$+ A_3 \overline{A_2} A_1 \overline{A_0} + A_3 \overline{A_2} A_1 A_0 + A_3 A_2 \overline{A_1} \overline{A_0} + A_3 A_2 A_1 A_0$$

See Figure 6-25.

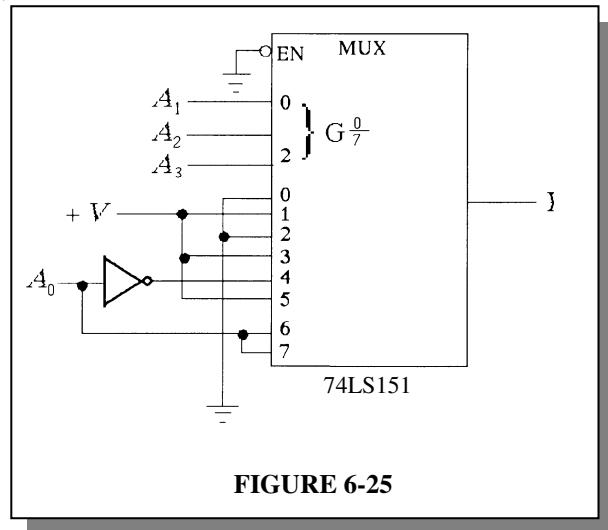


FIGURE 6-25

47. See Figure 6-26.

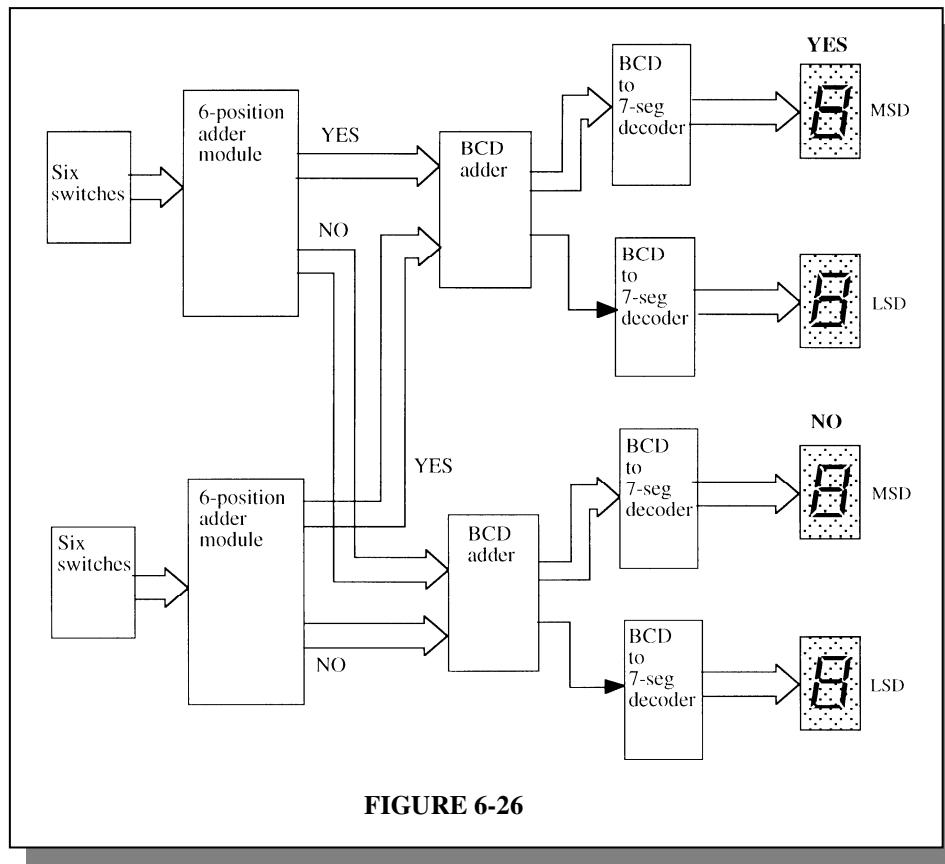
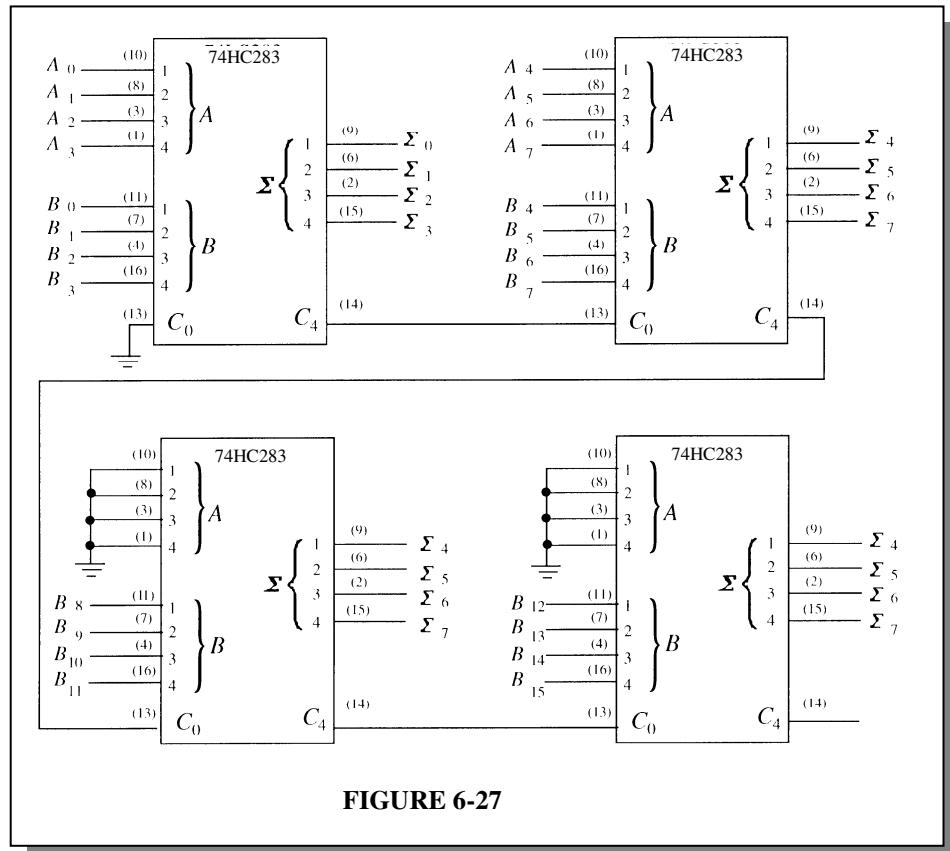


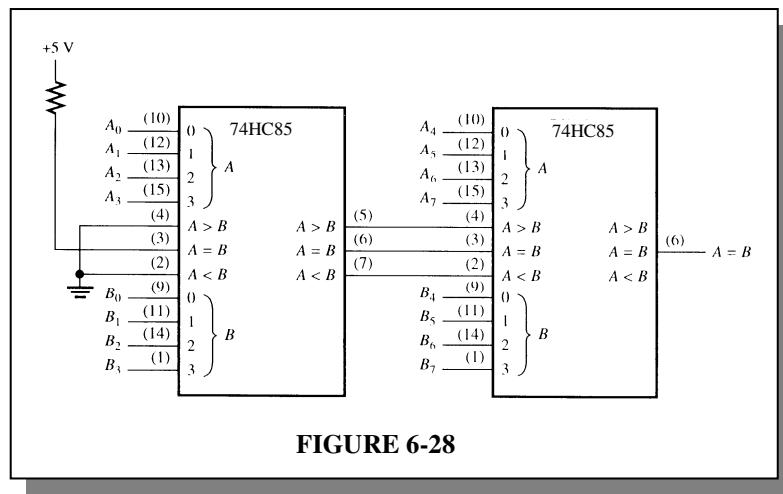
FIGURE 6-26

**48.** See Figure 6-27.



**FIGURE 6-27**

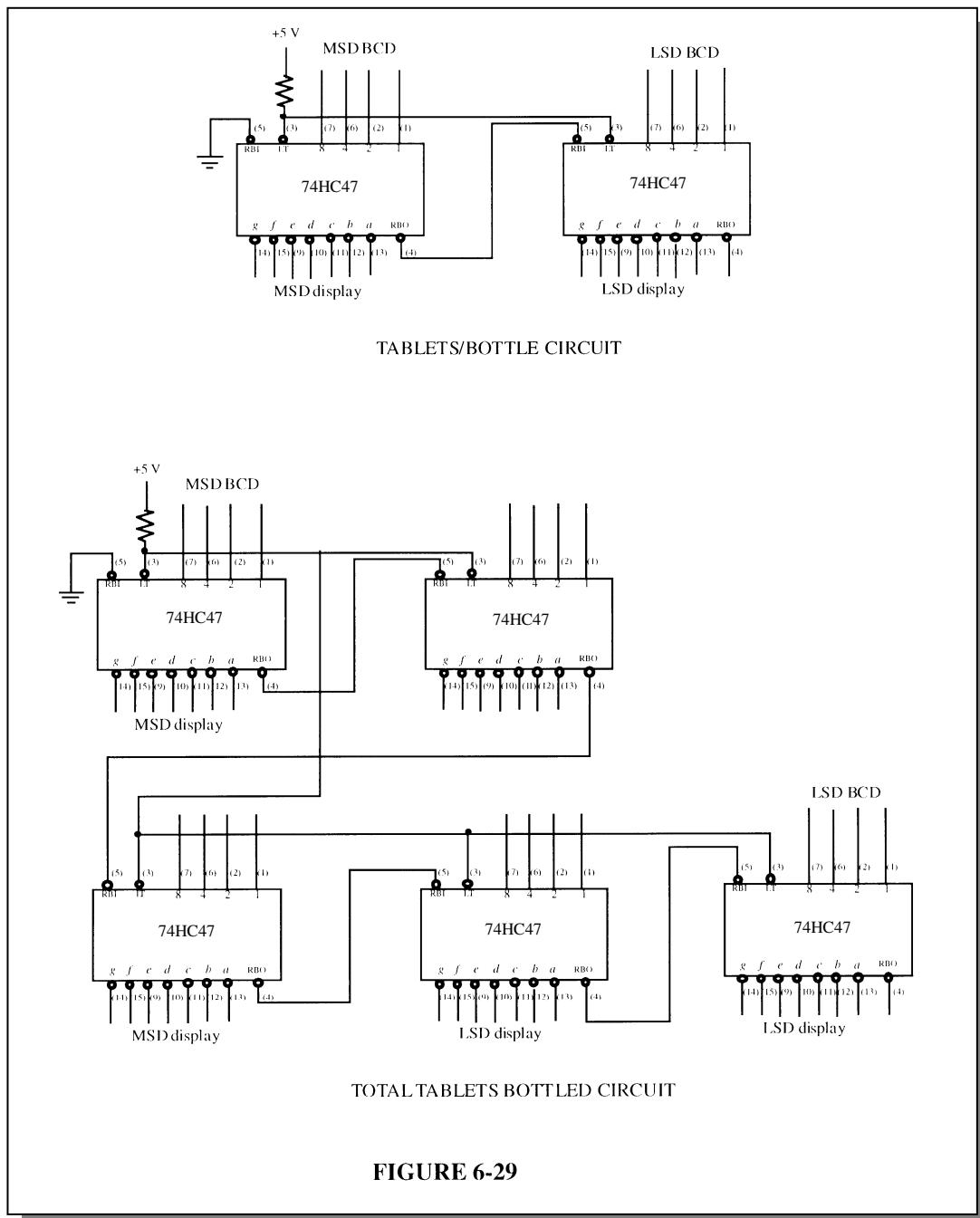
**49.** See Figure 6-28.



**FIGURE 6-28**

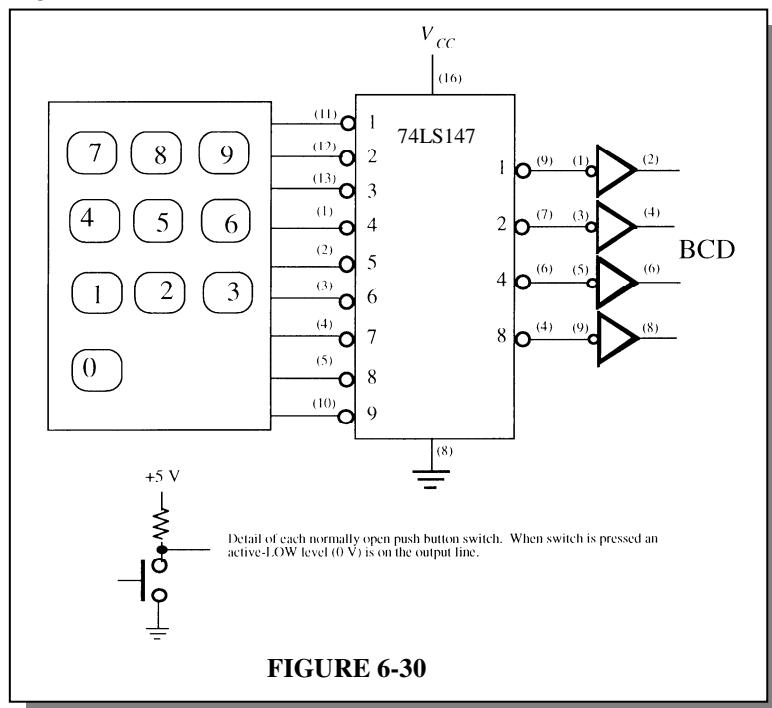
## Chapter 6

48. See Figure 6-29.



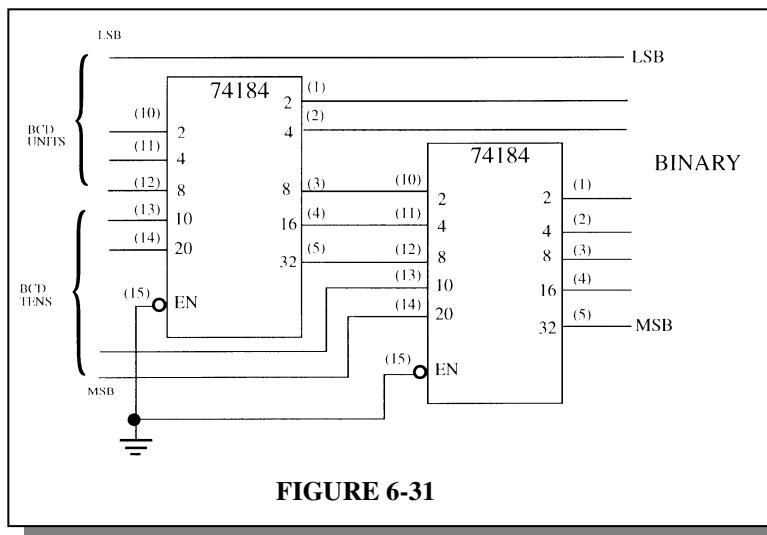
**FIGURE 6-29**

51. See Figure 6-30.



**FIGURE 6-30**

52. See Figure 6-31.



**FIGURE 6-31**

### **Multisim Troubleshooting Practice**

53.  $C_{IN}$  of UQ is shorted to VCC.
54. Output of U1A is shorted to ground.
55. Input C of 4-to16 line decoder is shorted to ground.
56. Switch contact connected to D1 input of G4 is shorted to VCC.

---

## CHAPTER 7

### LATCHES, FLIP-FLOPS, and TIMERS

---

#### *Section 7-1 Latches*

1. See Figure 7-1.

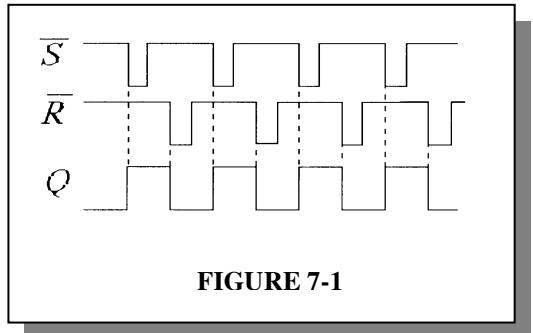


FIGURE 7-1

2. See Figure 7-2.

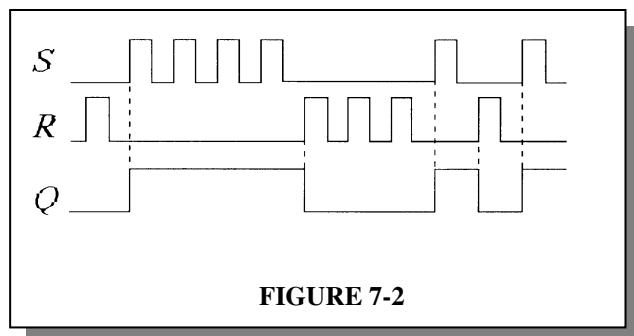


FIGURE 7-2

3. See Figure 7-3.

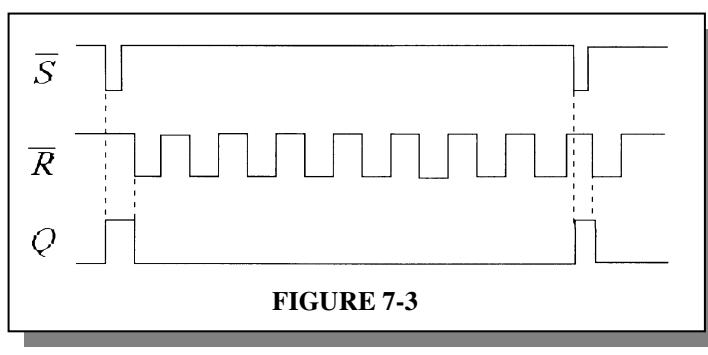
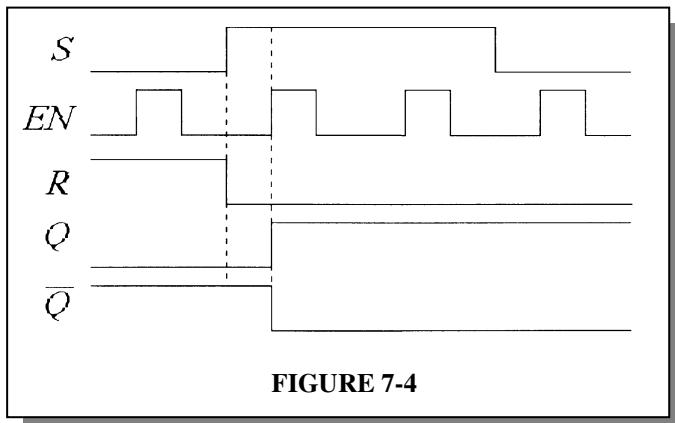


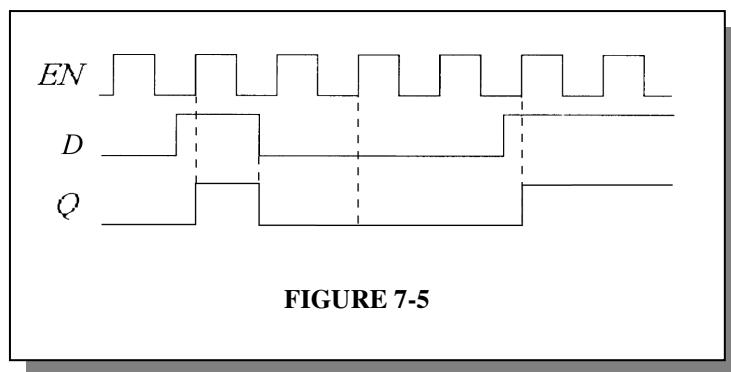
FIGURE 7-3

4. See Figure 7-4.



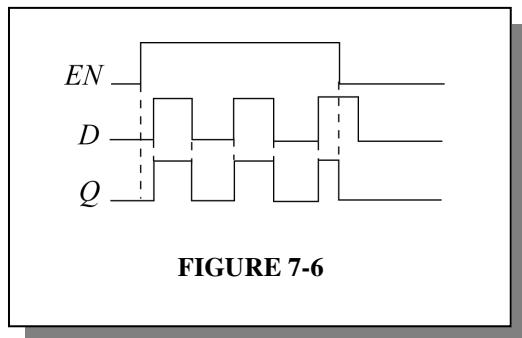
**FIGURE 7-4**

5. See Figure 7-5.



**FIGURE 7-5**

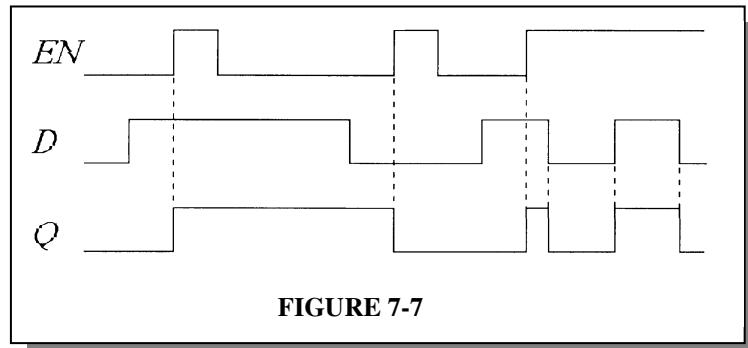
6. See Figure 7-6.



**FIGURE 7-6**

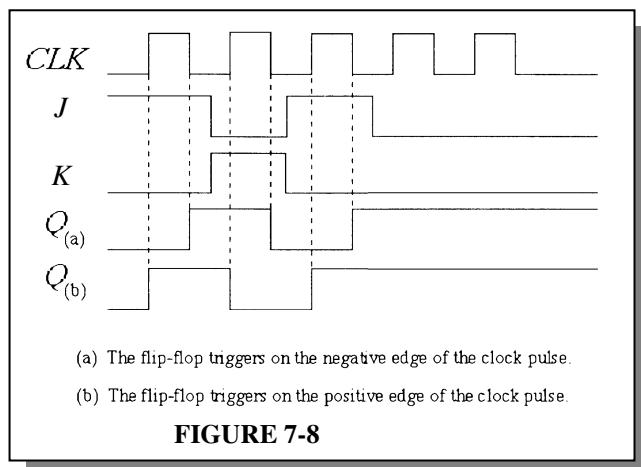
## *Chapter 7*

7. See Figure 7-7.

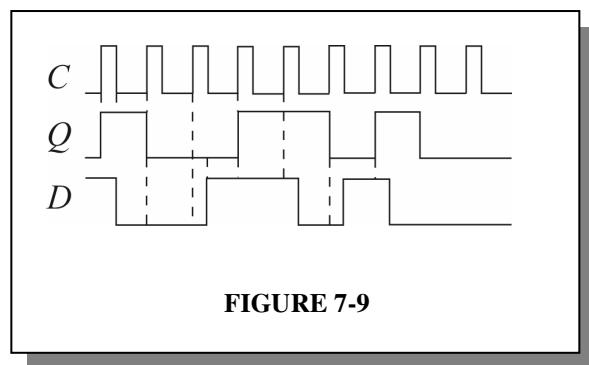


### *Section 7-2 Flip-Flops*

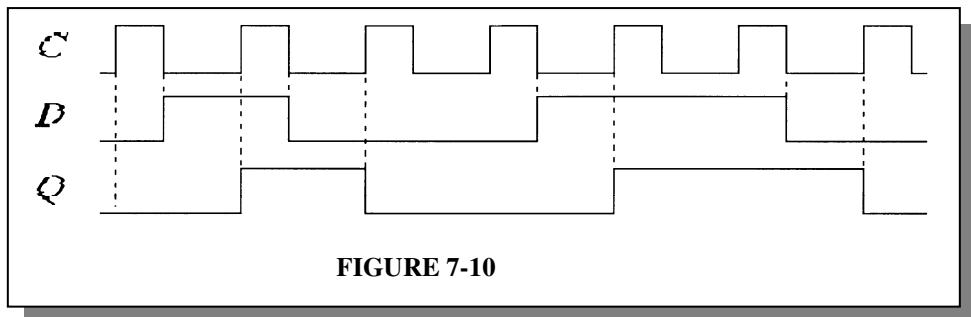
8. See Figure 7-8.



9. See Figure 7-9.

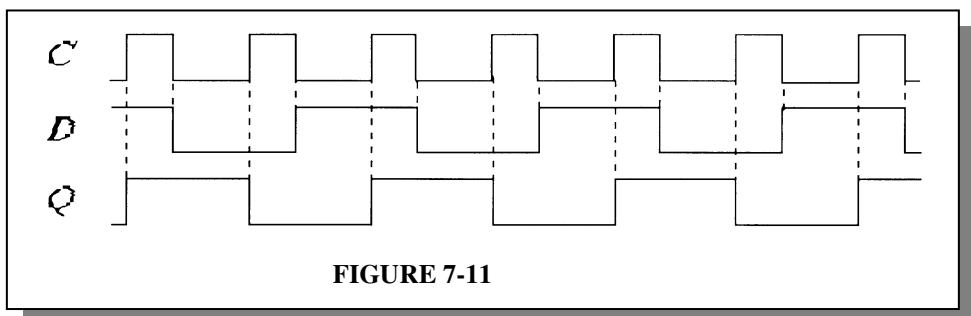


10. See Figure 7-10.



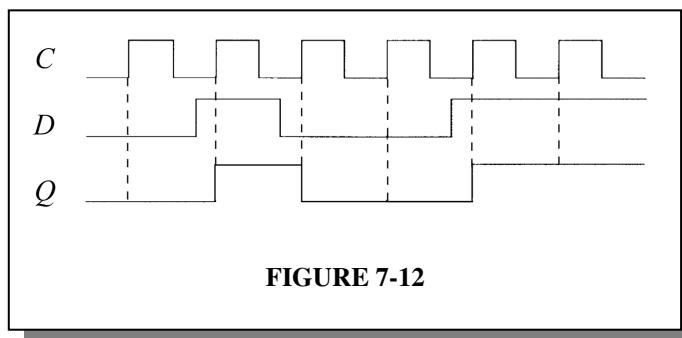
**FIGURE 7-10**

11. See Figure 7-11.



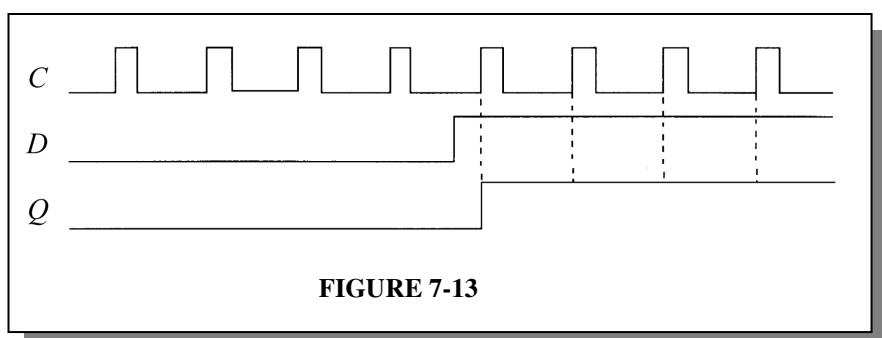
**FIGURE 7-11**

12. See Figure 7-12.



**FIGURE 7-12**

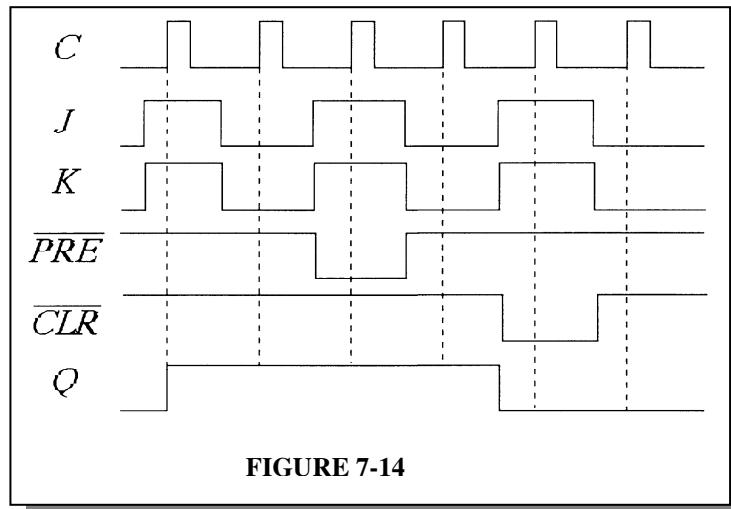
13. See Figure 7-13.



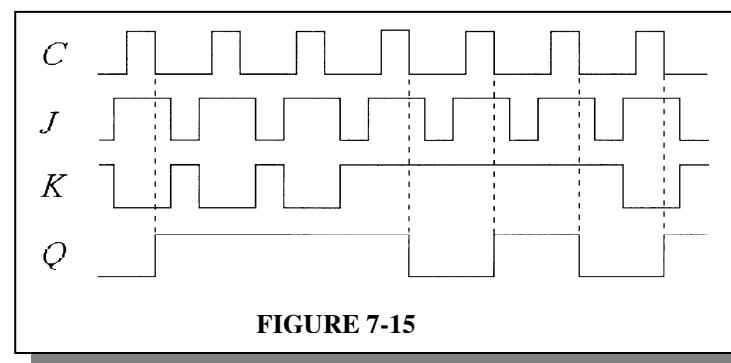
**FIGURE 7-13**

## Chapter 7

14. See Figure 7-14.



15. See Figure 7-15.

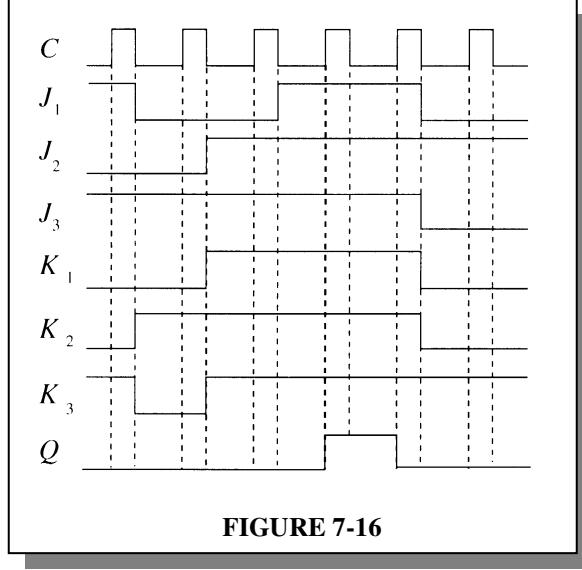


16.  $J: 0010000$

$K: 0000100$

$Q: 0011000$

17. See Figure 7-16.



18. See Figure 7-17.

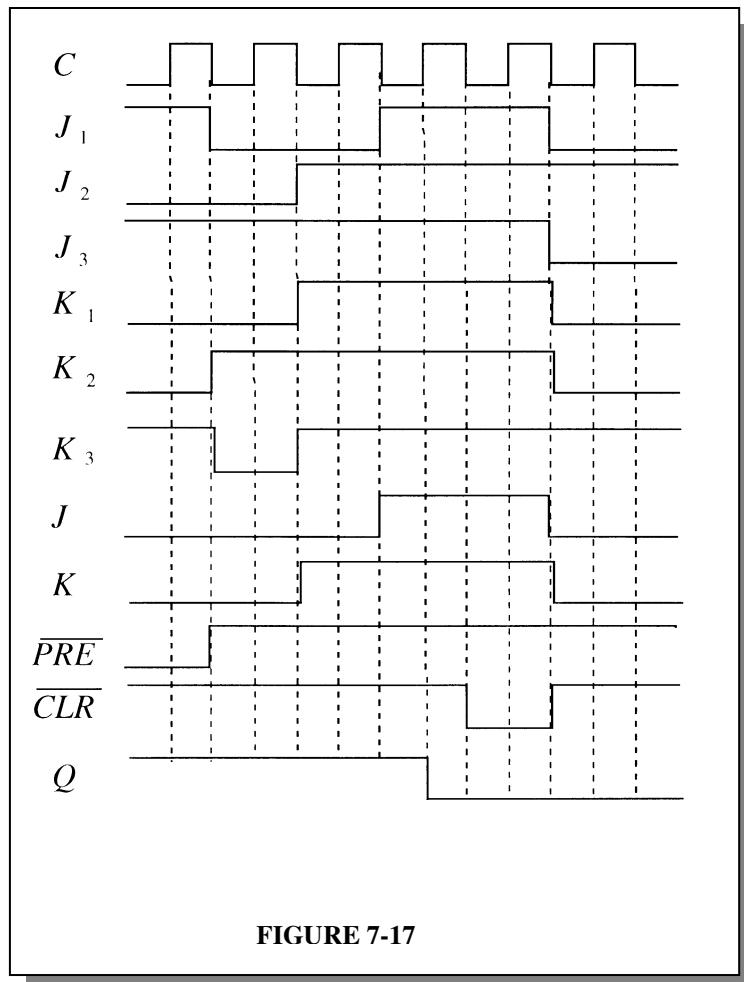


FIGURE 7-17

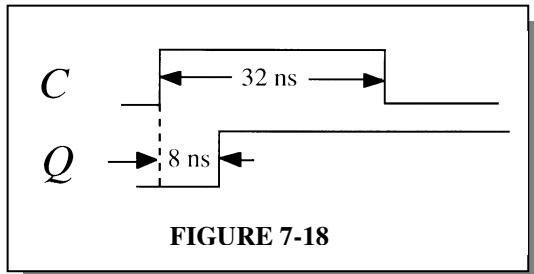
### Section 7-3 Flip-Flop Operating Characteristics

19. The direct current and dc supply voltage
20.  $t_{PLH}$  (Clock to  $Q$ ):  
Time from triggering edge of clock to the LOW-to-HIGH transition of the  $Q$  output.  
 $t_{PHL}$  (Clock to  $Q$ ):  
Time from triggering edge of clock to the HIGH-to-LOW transition of the  $Q$  output.  
 $t_{PLH}$  ( $\overline{PRE}$  to  $Q$ ):  
Time from assertion of the Preset input to the LOW-to-HIGH transition of the  $Q$  output.  
 $t_{PHL}$  ( $\overline{CLR}$  to  $Q$ ):  
Time from assertion of the clear input to the HIGH-to-LOW transition of the  $Q$  output.
21.  $T_{min} = 30 \text{ ns} + 37 \text{ ns} = 67 \text{ ns}$

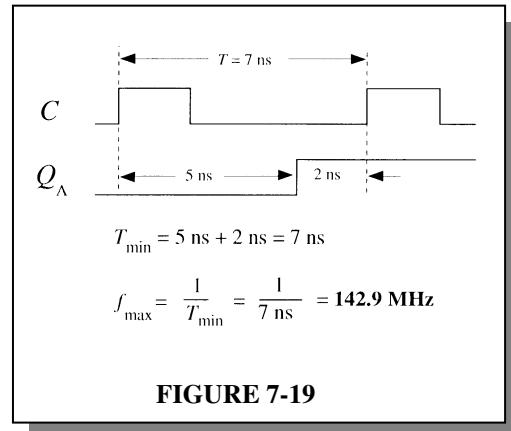
$$f_{max} = \frac{1}{T_{min}} = 14.9 \text{ MHz}$$

## Chapter 7

22. See Figure 7-18.



**FIGURE 7-18**



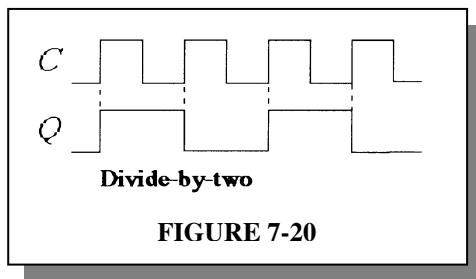
**FIGURE 7-19**

23.  $I_T = 15(10 \text{ mA}) = 150 \text{ mA}$   
 $P_T = (5 \text{ V})(150 \text{ mA}) = 750 \text{ mW}$

24. See Figure 7-19.

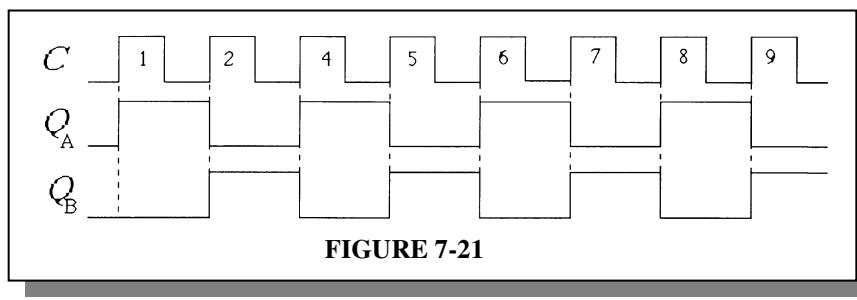
### Section 7-4 Flip-Flop Applications

25. See Figure 7-20. It divides clock by two.



**FIGURE 7-20**

26. See Figure 7-21.



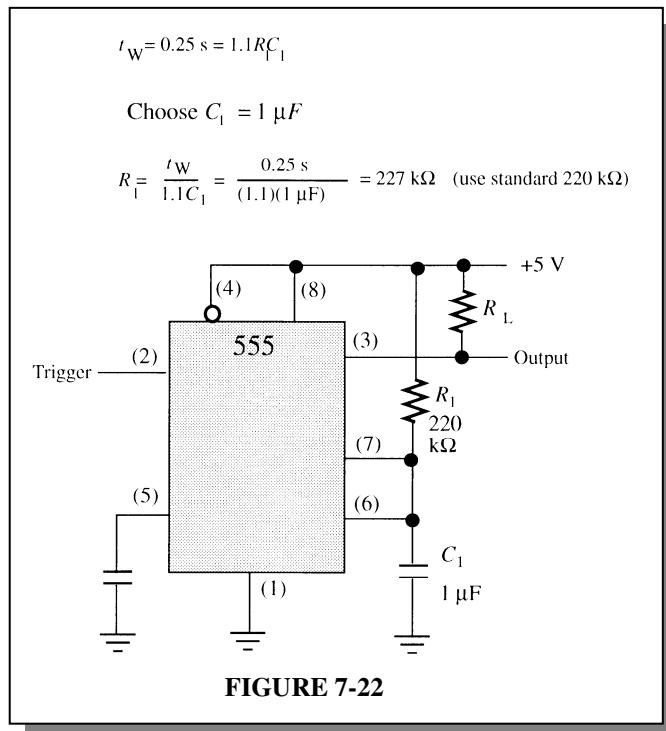
**FIGURE 7-21**

### Section 7-5 One-Shots

27.  $t_W = 0.7RC_{\text{EXT}} = 0.7(3.3 \text{ k}\Omega)(2000 \text{ pF}) = 4.62 \mu\text{s}$

28.  $R_X = \frac{t_W}{RC_{\text{EXT}}} - 0.7 = \frac{5000 \text{ ns}}{0.32 \times 10,000 \text{ pF}} - 0.7 = 1.56 \text{ k}\Omega$

29. See Figure 7-22.



### Section 7-6 Astable Multivibrator

30.  $f = \frac{1}{0.7(R_1 + 2R_2)C_2} = \frac{1}{0.7(1000 \Omega + 2200 \Omega)(0.01 \mu\text{F})} = 44.6 \text{ kHz}$

31.  $T = \frac{1}{f} = \frac{1}{20 \text{ kHz}} = 50 \mu\text{s}$

For a duty cycle of 75%:

$t_H = 37.5 \mu\text{s}$  and  $t_L = 12.5 \mu\text{s}$

$$R_1 + R_2 = \frac{t_H}{0.7C} = \frac{37.5 \mu\text{s}}{0.7(0.002 \mu\text{F})} = 26,786 \Omega$$

$$R_2 = \frac{t_L}{0.7C} = \frac{12.5 \mu\text{s}}{0.7(0.002 \mu\text{F})} = 8,929 \Omega \quad (\text{use } 9.1 \text{ k}\Omega)$$

$$R_1 = 26,786 \Omega - R_2 = 26,786 \Omega - 8,929 \Omega = 17,857 \Omega \quad (\text{use } 18 \text{ k}\Omega)$$

## Chapter 7

### Section 7-7 Troubleshooting

32. The flip-flop in Figure 7-90 of the text has an internally open  $J$  input.
33. The wire from pin 6 to pin 10 and the ground wire are reversed. Pin 7 should be at ground and pin 6 connected to pin 10.
34. See Figure 7-23.

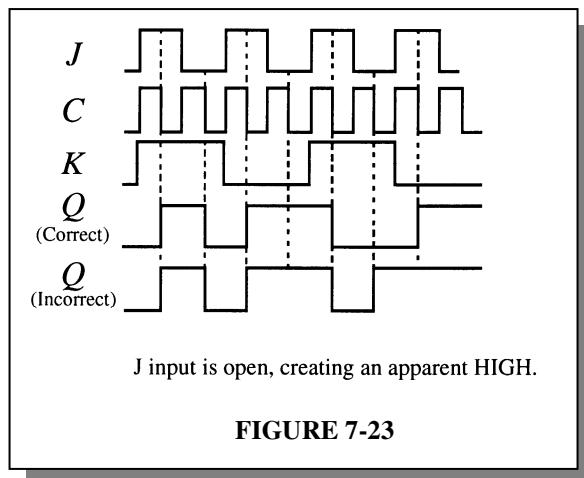


FIGURE 7-23

35. Since none of the flip-flops change, the problem must be a fault that affects all of them. The two functions common to all the flip-flops are the clock (CLK) and clear ( $\overline{CLR}$ ) inputs. One of these lines must be shorted to ground because a LOW on either one will prevent the flip-flops from changing state. Most likely, the  $\overline{CLR}$  line is shorted to ground because if the clock line were shorted chances are that all of the flip-flops would not have ended up reset when the power was turned on unless an initial LOW was applied to the  $\overline{CLR}$  at power on.
36. Small differences in the switching times of flip-flop A and flip-flop B due to propagation delay cause the glitches as shown in the expanded timing diagram in Figure 7-24. The delays are exaggerated greatly for purposes of illustration. Use synchronous clocking.

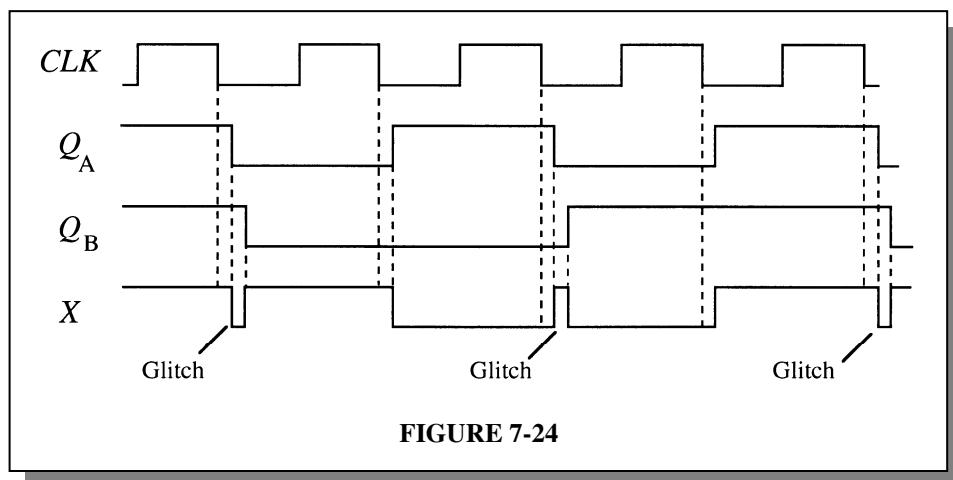
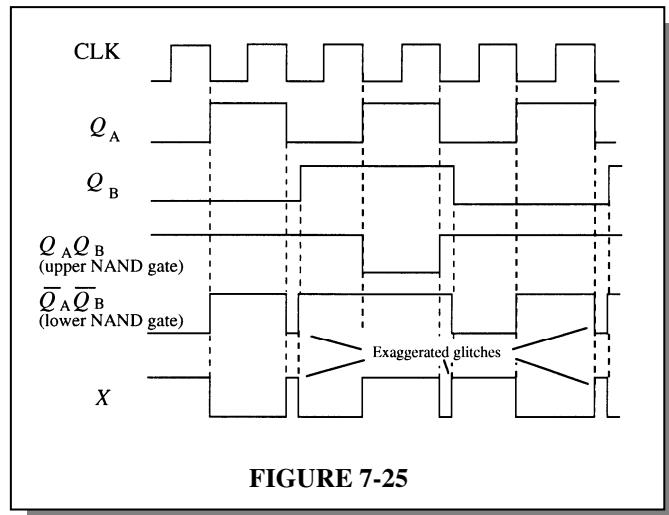


FIGURE 7-24

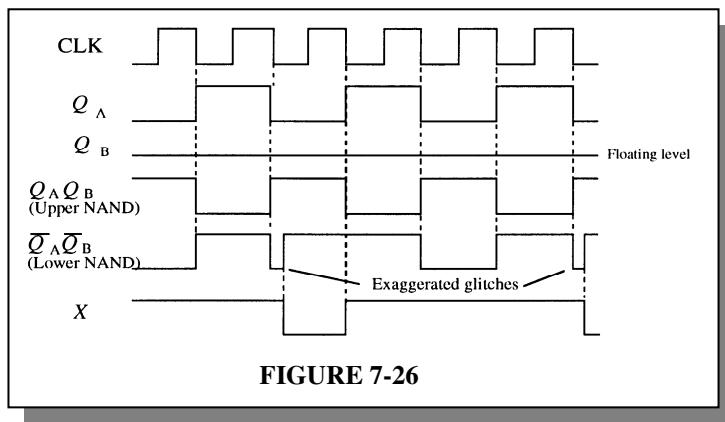
37. (a) See Figure 7-25.



**FIGURE 7-25**

- (b)  $K_B$  open acts as a HIGH and the operation is normal. The timing diagram is the same as Figure 7-25.

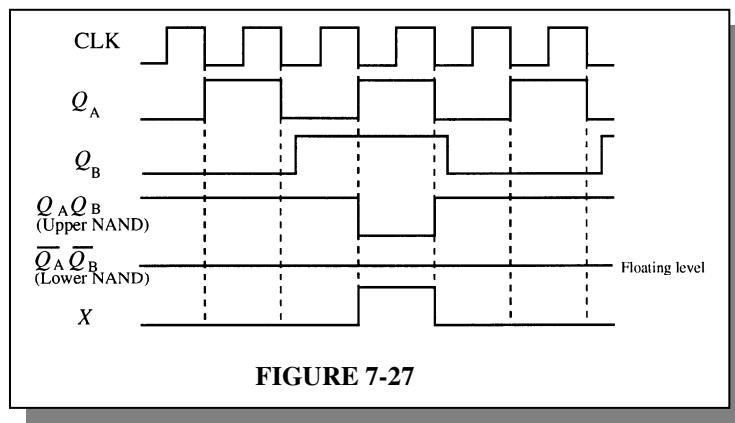
- (c) See Figure 7-26.



**FIGURE 7-26**

- (d)  $X$  remains LOW if  $Q_B = 1$  ( $\overline{Q}_B = 0$ ).  $X$  follows  $\overline{Q}_A$  if  $Q_B = 0$  ( $\overline{Q}_B = 1$ ).

- (e) See Figure 7-27.



**FIGURE 7-27**

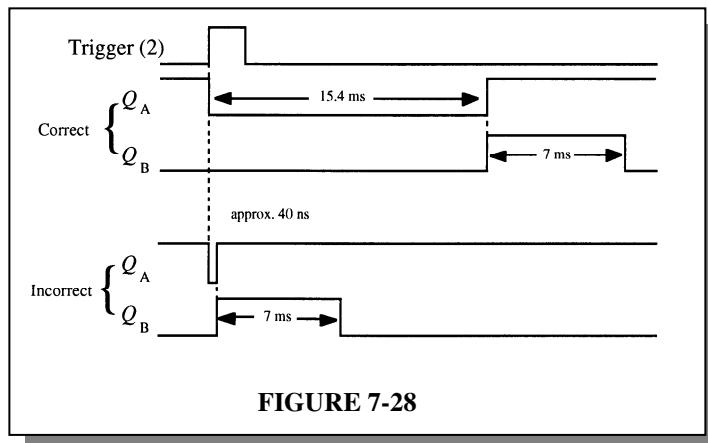
## Chapter 7

38.  $t_W = 0.7RC_{\text{EXT}}$

One-shot A:  $t_W = 0.7(0.22 \mu\text{F})(100 \text{ k}\Omega) = 15.4 \text{ ms}$

One-shot B:  $t_W = 0.7(0.1 \mu\text{F})(100 \text{ k}\Omega) = 7 \text{ ms}$

The pulse width of one shot A is apparently not controlled by the external components and the one-shot is producing its minimum pulse width of about 40 ns. An *open pin 11* would cause this problem. See Figure 7-28.



## Applied Logic

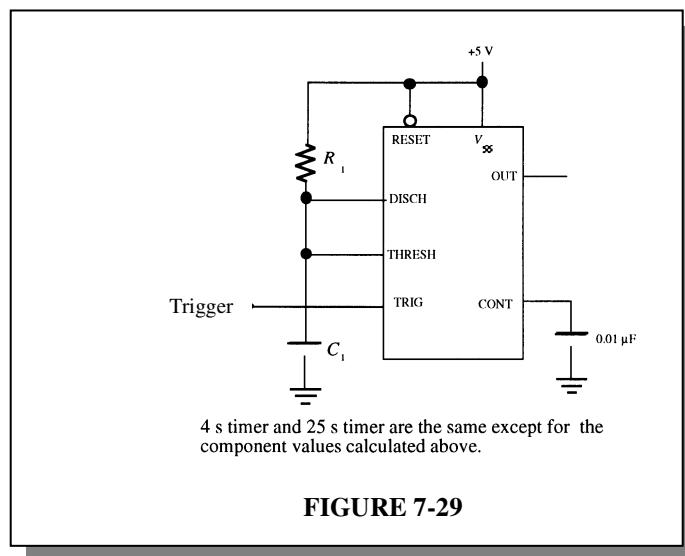
39. For the 4 s timer let  $C_1 = 1 \mu\text{F}$

$$R_1 = \frac{4 \text{ s}}{(1.1)(1 \mu\text{F})} = 3.63 \text{ M}\Omega \text{ (use } 3.9 \text{ M}\Omega)$$

For the 25 s timer let  $C_1 = 2.2 \mu\text{F}$

$$R_1 = \frac{25 \text{ s}}{(1.1)(2.2 \mu\text{F})} = 10.3 \text{ M}\Omega \text{ (use } 10 \text{ M}\Omega)$$

See Figure 7-29.



40.  $t_w = 6 \text{ s}$ . Let  $C_{\text{EXT}} = 1 \mu\text{F}$

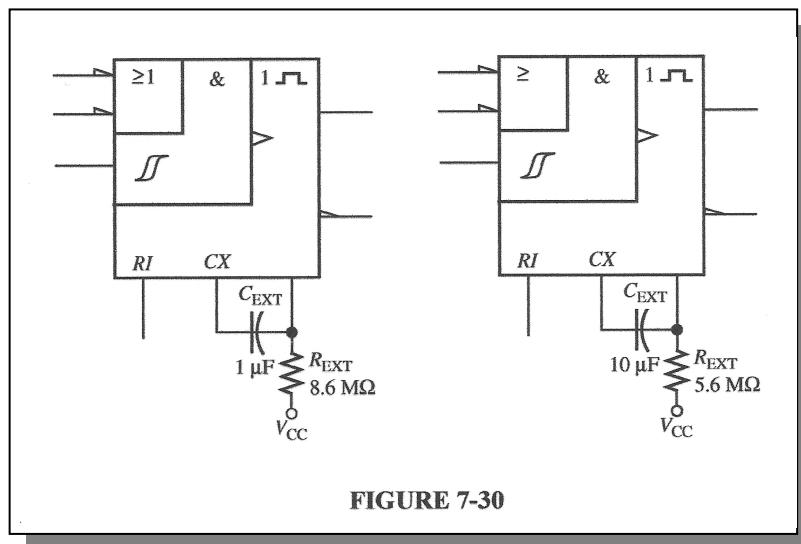
$$t_w = 0.7RC_{\text{EXT}}$$

$$R = \frac{t_w}{0.7C_{\text{EXT}}} = \frac{6 \text{ s}}{0.7(1 \mu\text{F})} = 8.6 \text{ M}\Omega$$

- $t_w = 40 \text{ s}$ . Let  $C_{\text{EXT}} = 10 \mu\text{F}$

$$R = \frac{t_w}{0.7C_{\text{EXT}}} = \frac{40 \text{ s}}{0.7(10 \mu\text{F})} = 5.7 \text{ M}\Omega$$

See Figure 7-30.



41.  $t_w = 6 \text{ s}$ . Let  $C_{\text{EXT}} = 1 \mu\text{F}$

$$t_w = 0.32R_{\text{EXT}}C_{\text{EXT}} \left(1 + \frac{0.7}{R_{\text{EXT}}}\right) = 0.32R_{\text{EXT}}C_{\text{EXT}} + (0.7)(0.32)C_{\text{EXT}}$$

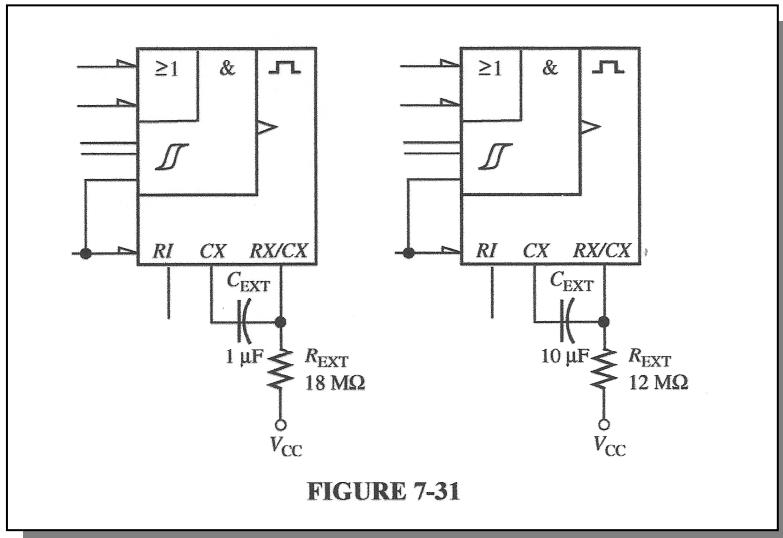
$$R_{\text{EXT}} = \frac{t_w - (0.7)(0.32)C_{\text{EXT}}}{0.32C_{\text{EXT}}} = \frac{6 \text{ s} - (0.224)(1 \mu\text{F})}{0.32(1 \mu\text{F})} = 18.8 \text{ M}\Omega$$

- $t_w = 40 \text{ s}$ . Let  $C_{\text{EXT}} = 10 \mu\text{F}$

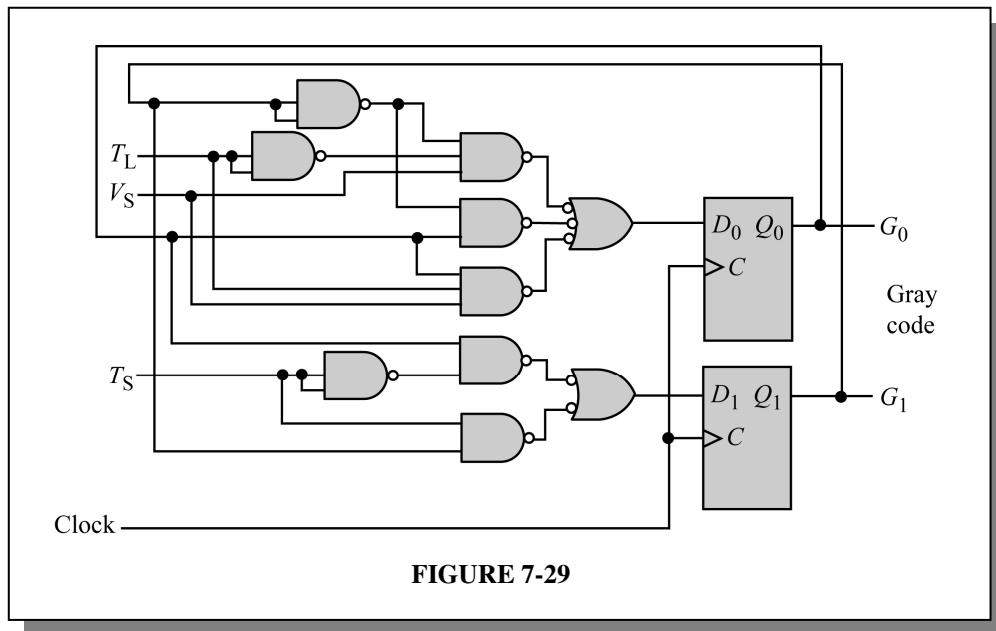
$$R_{\text{EXT}} = \frac{40 \text{ s} - (0.224)10 \mu\text{F}}{0.32(10 \mu\text{F})} = 12.5 \text{ M}\Omega$$

See Figure 7-31.

## Chapter 7



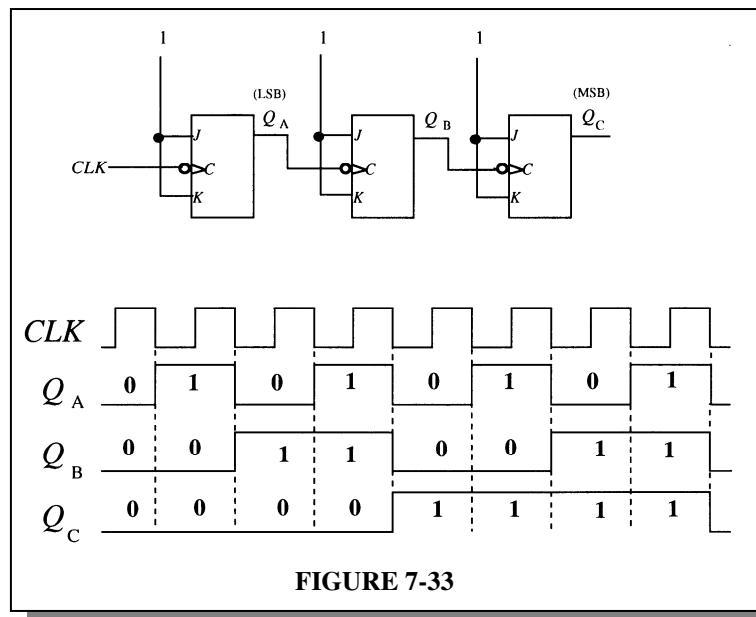
42. See Figure 7-32.



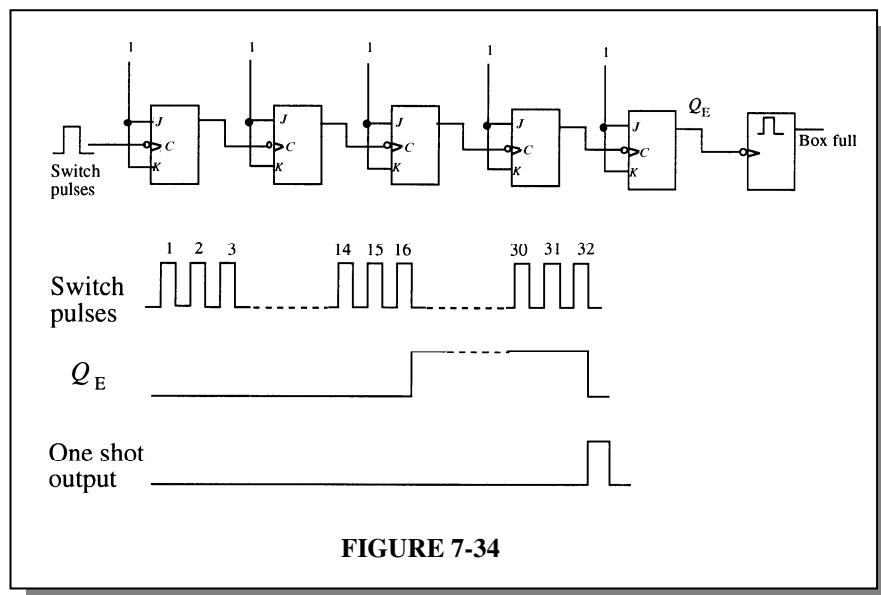
43. If a 555 timer is used, increase the  $R_{\text{EXT}}C_{\text{EXT}}$  time constant by  $60 \text{ s}/25 \text{ s} = 2.4$  times. If a 1 Hz clock is used, change the counter from a divide-by-25 to a divide-b7-60.

### **Special Design Problems**

**44.** See Figure 7-33.



**45.** See Figure 7-34 for one possibility.

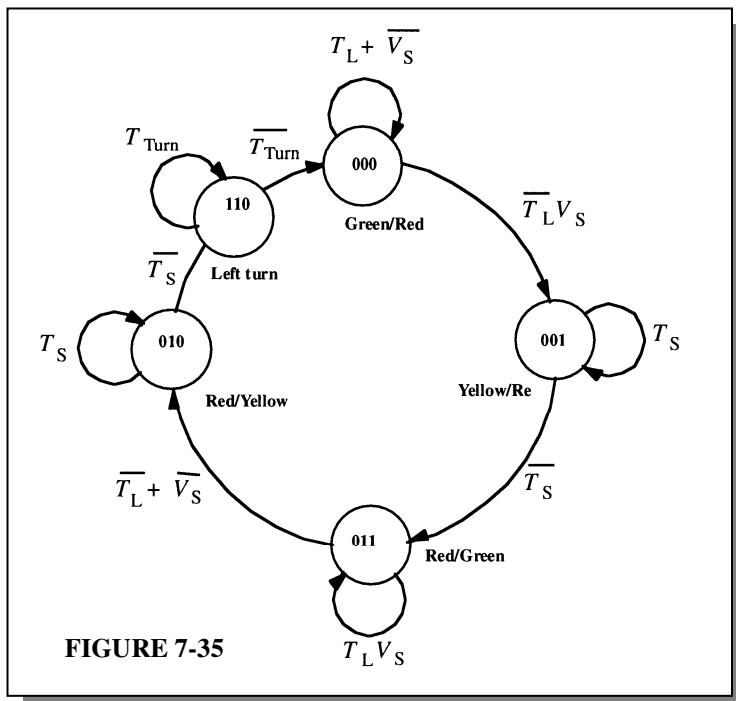


## Chapter 7

46. Changes required for the system to incorporate a 15 s left turn signal on main:

1. Change the 2-bit gray code sequence to a 3-bit sequence.
2. Add decoding logic to the State Decoder to decode the turn signal state.
3. Change the Output Logic to incorporate the turn signal output.
4. Change the Trigger Logic to incorporate a trigger output for the turn signal timer.
5. Add a 15 second timer.

See Figure 7-35.



## Multisim Troubleshooting Practice

47. R input of U1 is shorted to  $V_{CC}$ .
48. Line to K input is shorted to  $V_{CC}$ .
49. Clock input is shorted to  $V_{CC}$  (or ground).
50. 1 k $\Omega$  resistor accidentally used in place of 10 k $\Omega$  timing resistor, or a 0.1  $\mu F$  capacitor is used in place of the 1  $\mu F$  timing capacitor.

---

## CHAPTER 8

### SHIFT REGISTERS

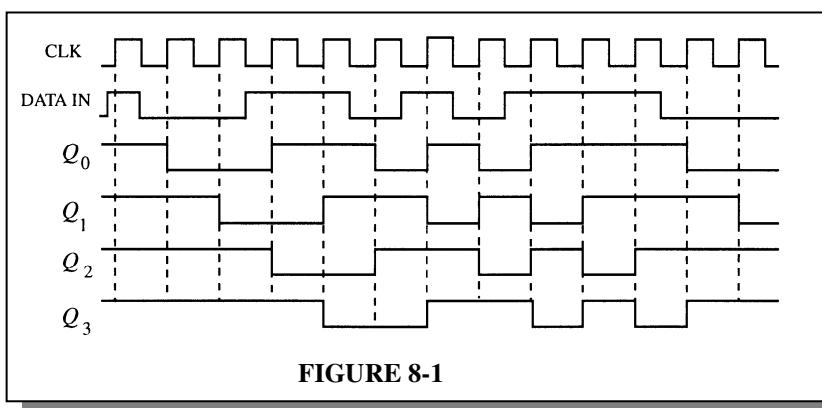
---

#### **Section 8-1 Shift Register Functions**

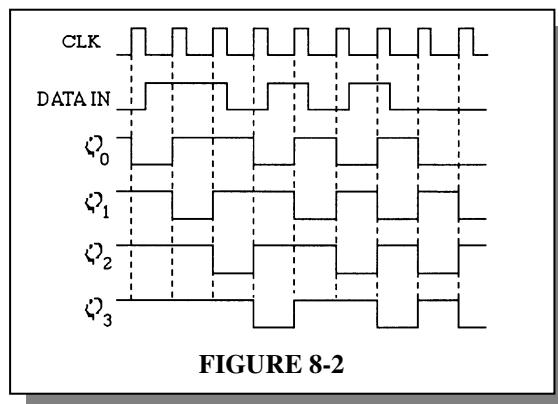
1. Shift registers store binary data in a series of flip-flops or other storage elements.
2. 1 byte = **8 bits**; 2 bytes = **16 bits**
3. Shift data and store data

#### **Section 8-2 Types of Shift Register Data I/Os**

4. Initially: 0000  
1<sup>st</sup> CLK: 1000  
2<sup>nd</sup> CLK: 1100  
3<sup>rd</sup> CLK: 0110
5. See Figure 8-1.



6. See Figure 8-2.



## Chapter 8

7.

|           |              |
|-----------|--------------|
| Initially | 101001111000 |
| CLK 1     | 010100111100 |
| CLK 2     | 001010011110 |
| CLK 3     | 000101001111 |
| CLK 4     | 000010100111 |
| CLK 5     | 100001010011 |
| CLK 6     | 110000101001 |
| CLK 7     | 111000010100 |
| CLK 8     | 011100001010 |
| CLK 9     | 001110000101 |
| CLK 10    | 000111000010 |
| CLK 11    | 100011100001 |
| CLK 12    | 110001110000 |

8. See Figure 8-3.

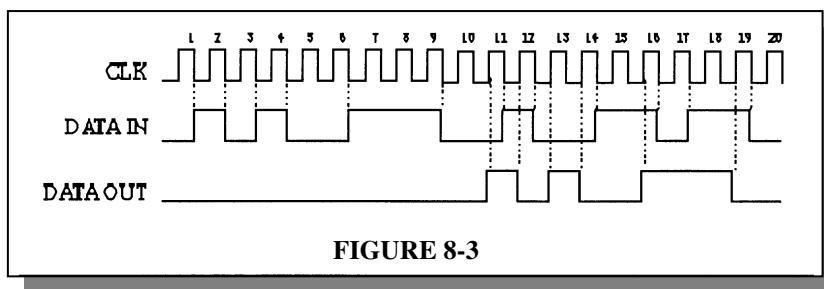


FIGURE 8-3

9. See Figure 8-4.

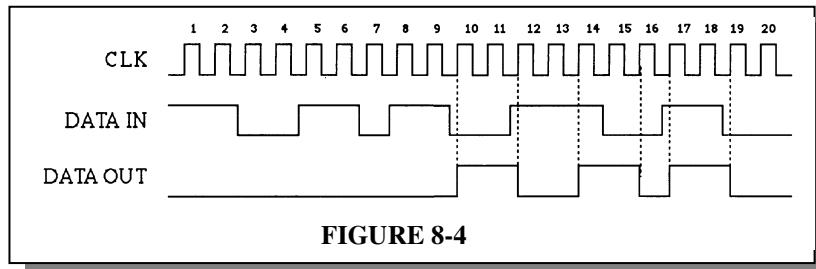


FIGURE 8-4

10. See Figure 8-5.

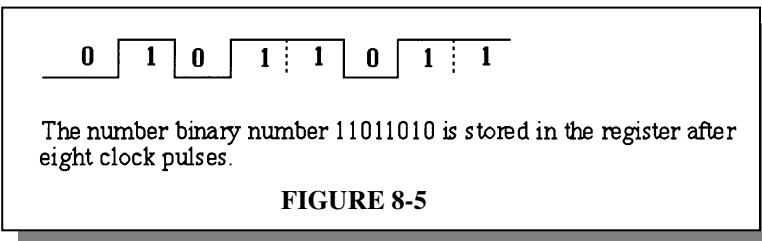
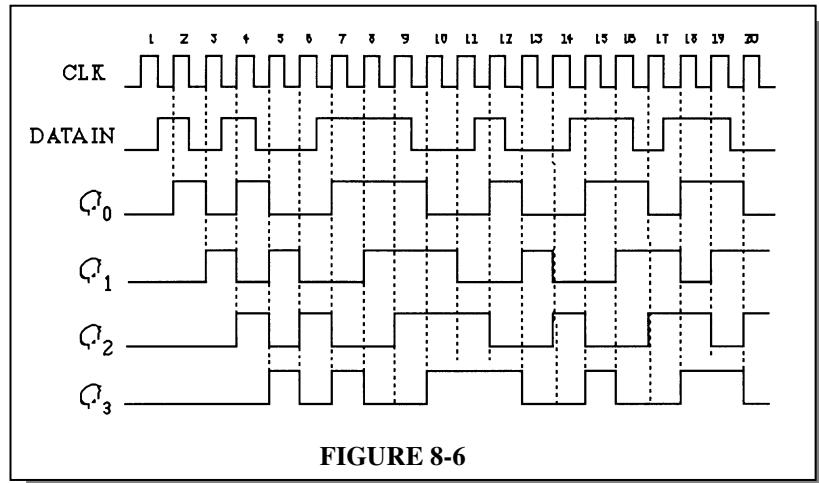


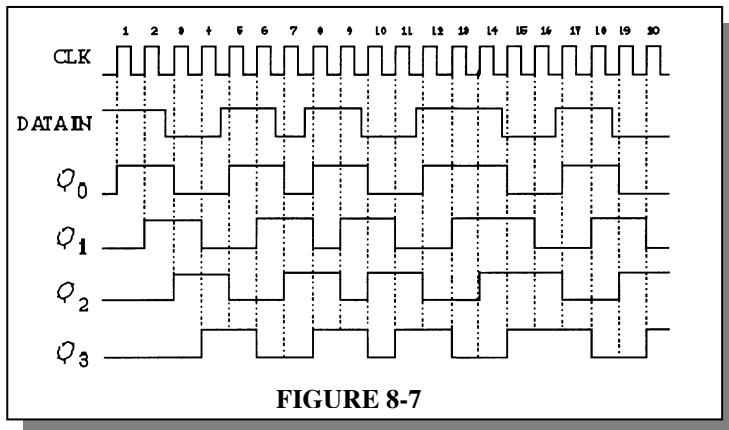
FIGURE 8-5

11. See Figure 8-6.



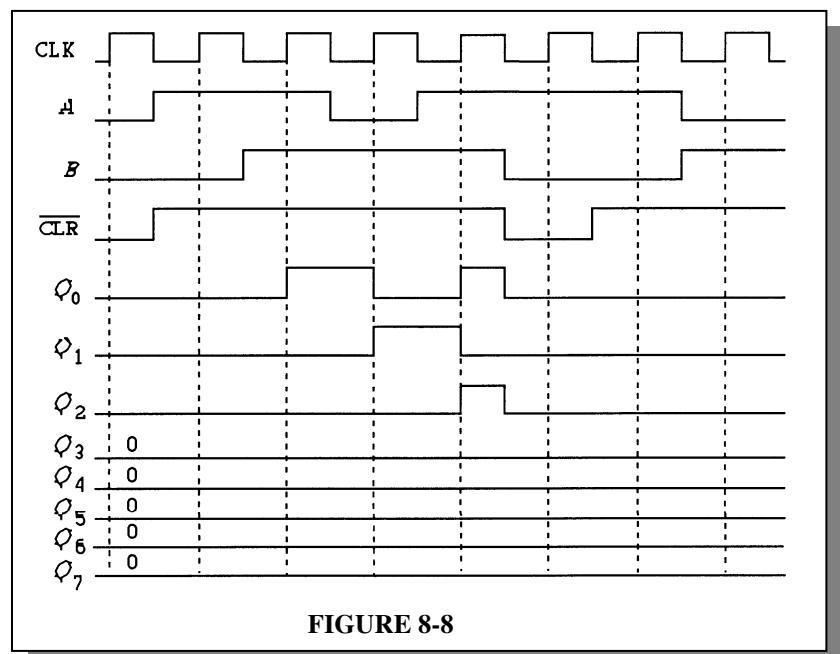
**FIGURE 8-6**

12. See Figure 8-7.



**FIGURE 8-7**

13. See Figure 8-8.



**FIGURE 8-8**

## Chapter 8

14. See Figure 8-9.

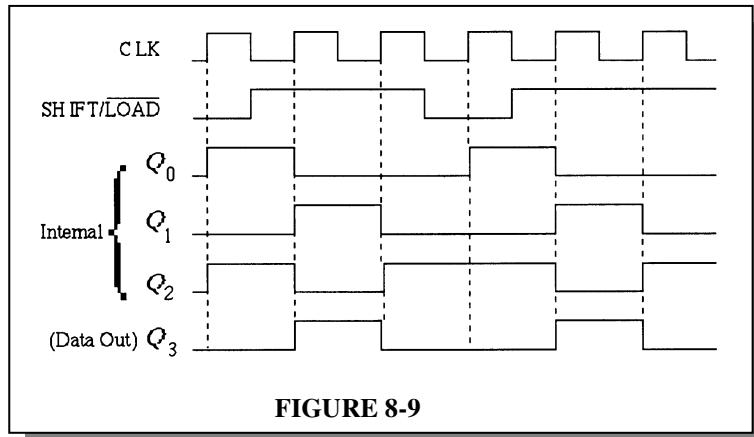


FIGURE 8-9

15. See Figure 8-10.

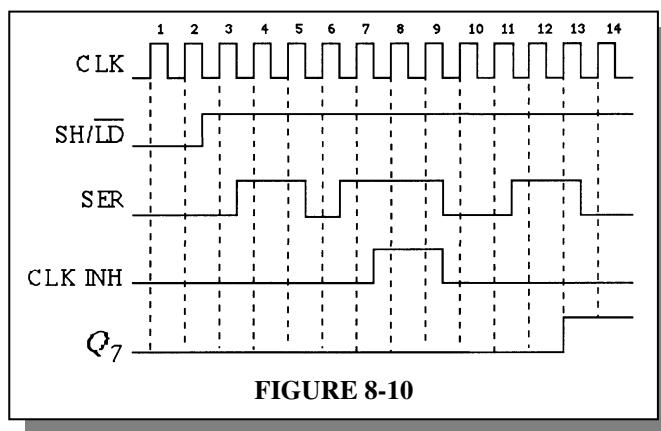


FIGURE 8-10

16. See Figure 8-11.

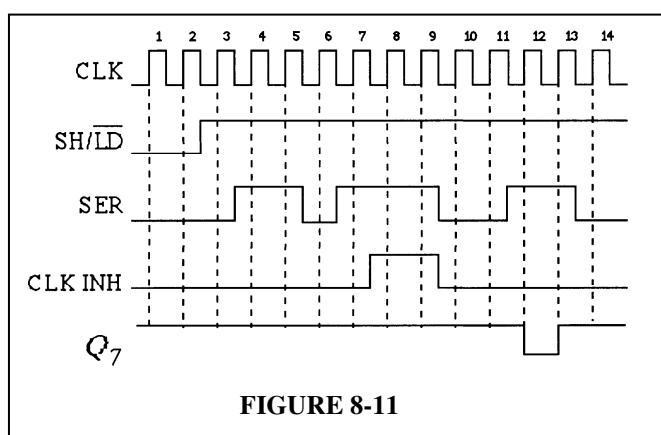


FIGURE 8-11

17. See Figure 8-12.

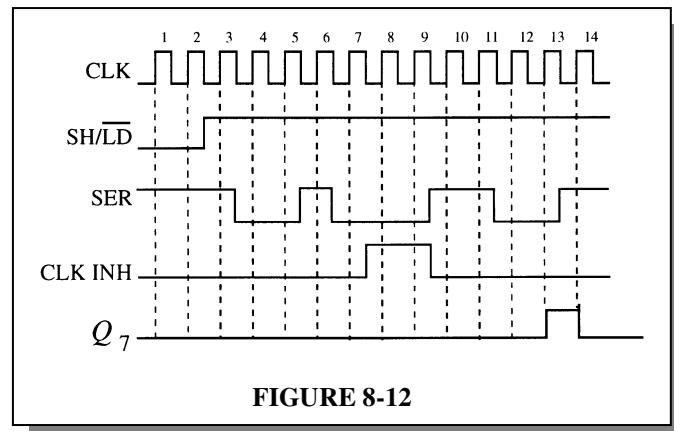


FIGURE 8-12

18. See Figure 8-13.

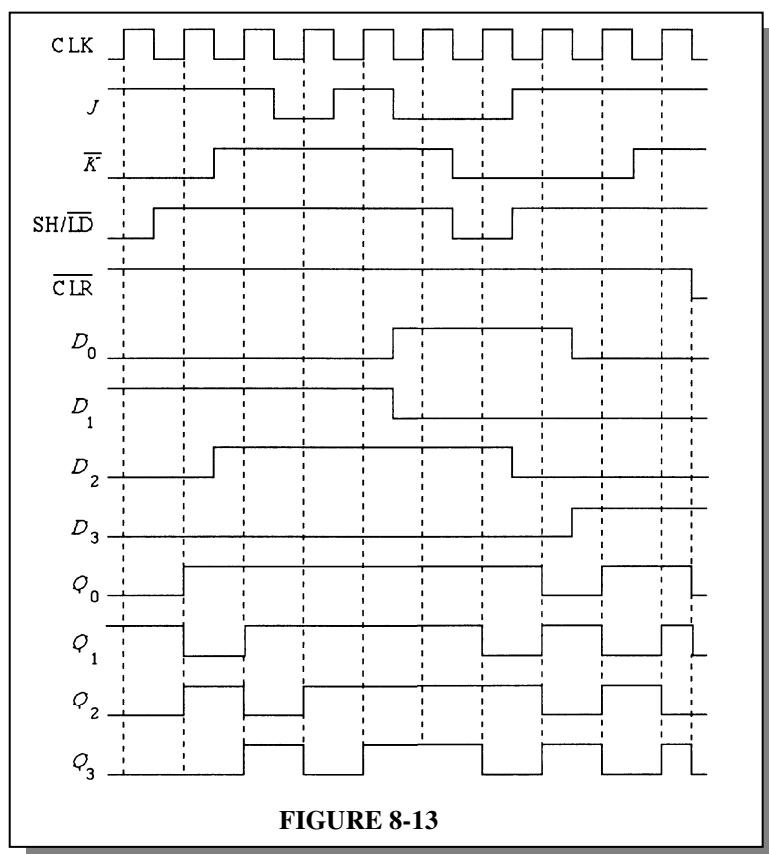


FIGURE 8-13

## Chapter 8

19. See Figure 8-14.

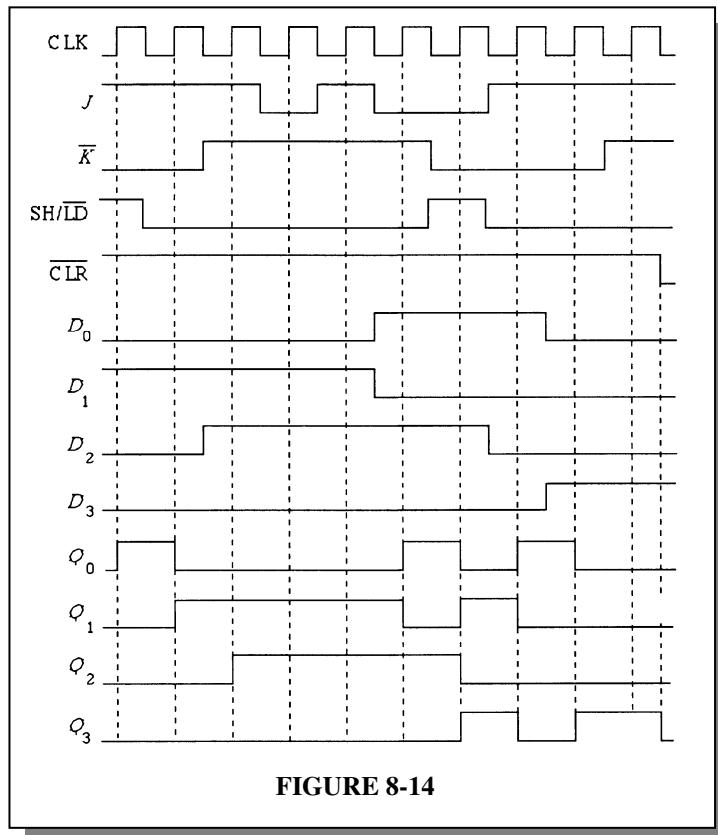


FIGURE 8-14

20. See Figure 8-15.

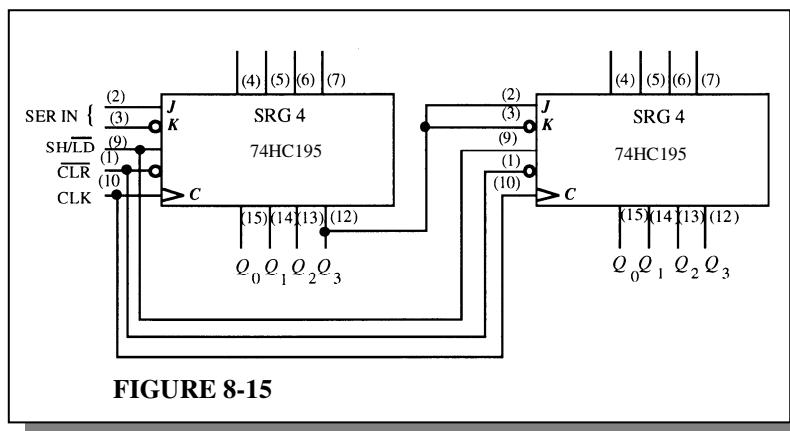


FIGURE 8-15

### **Section 8-3 Bidirectional Shift Registers**

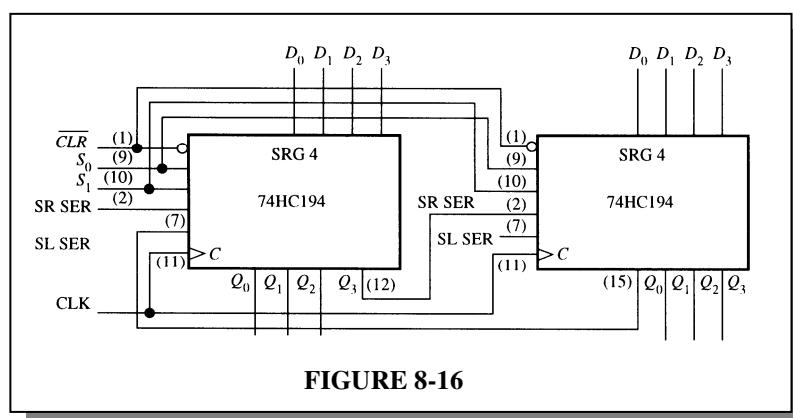
**21.**

|                |          |             |
|----------------|----------|-------------|
| Initially (76) | 01001100 |             |
| CLK 1          | 10011000 | Shift left  |
| CLK 2          | 01001100 | Shift right |
| CLK 3          | 00100110 | Shift right |
| CLK 4          | 00010011 | Shift right |
| CLK 5          | 00100110 | Shift left  |
| CLK 6          | 01001100 | Shift left  |
| CLK 7          | 00100110 | Shift right |
| CLK 8          | 01001100 | Shift left  |
| CLK 9          | 00100110 | Shift right |
| CLK 10         | 01001100 | Shift left  |
| CLK 11         | 10011000 | Shift left  |

**22.**

|                |          |             |
|----------------|----------|-------------|
| Initially (76) | 01001100 |             |
| CLK 1          | 00100110 | Shift right |
| CLK 2          | 00010011 | Shift right |
| CLK 3          | 00001001 | Shift right |
| CLK 4          | 00010010 | Shift left  |
| CLK 5          | 00100100 | Shift left  |
| CLK 6          | 01001000 | Shift left  |
| CLK 7          | 00100100 | Shift right |
| CLK 8          | 01001000 | Shift left  |
| CLK 9          | 10010000 | Shift left  |
| CLK 10         | 00100000 | Shift left  |
| CLK 11         | 00010000 | Shift right |
| CLK 12         | 00001000 | Shift right |

**23.** See Figure 8-16.



**FIGURE 8-16**

## Chapter 8

24. See Figure 8-17.

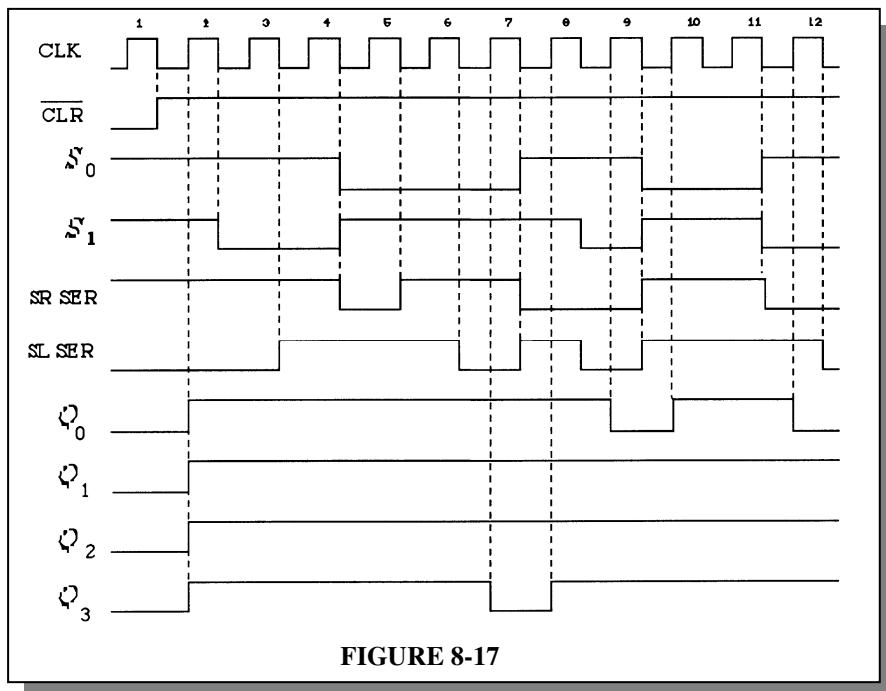


FIGURE 8-17

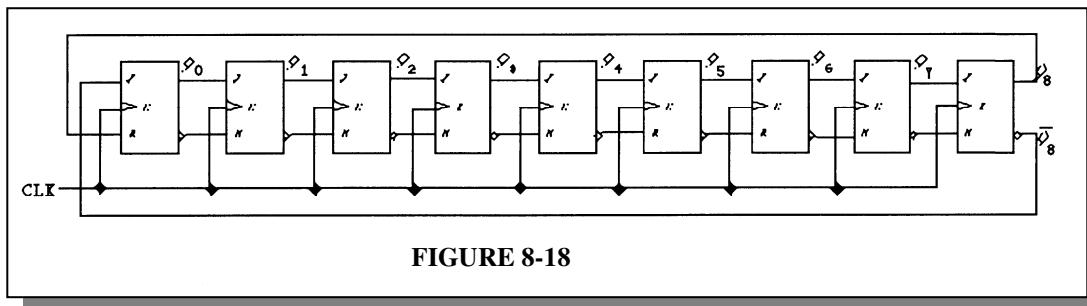
### Section 8-4 Shift Register Counters

- |                             |                          |
|-----------------------------|--------------------------|
| 25. (a) $2n = 6$<br>$n = 3$ | (b) $2n = 10$<br>$n = 5$ |
| (c) $2n = 14$<br>$n = 7$    | (d) $2n = 16$<br>$n = 8$ |

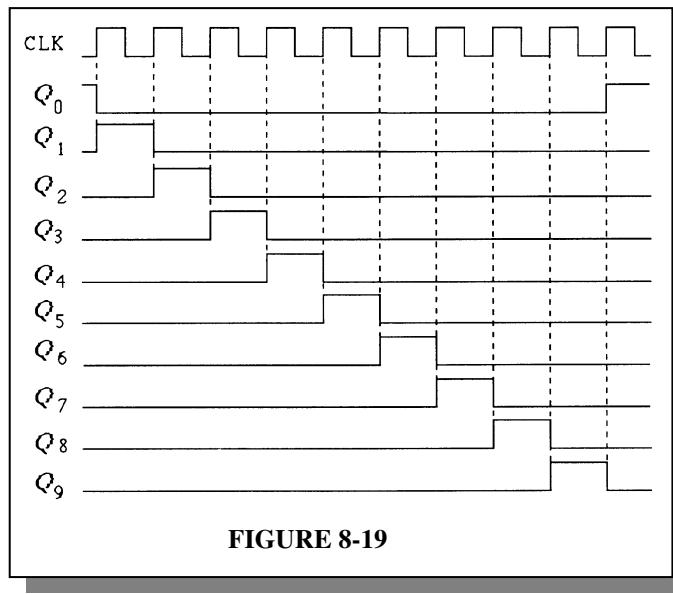
26.  $2n = 18$ ;  $n = 9$  flip-flops

| $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | $Q_5$ | $Q_6$ | $Q_7$ | $Q_8$ |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| 1     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| 1     | 1     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0     | 0     |
| 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     | 0     |
| 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0     | 0     |
| 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     | 0     |
| 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0     | 0     |
| 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 0     |
| 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     |
| 0     | 1     | 1     | 1     | 1     | 1     | 1     | 1     | 1     |
| 0     | 0     | 1     | 1     | 1     | 1     | 1     | 1     | 1     |
| 0     | 0     | 0     | 1     | 1     | 1     | 1     | 1     | 1     |
| 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     | 1     |
| 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1     | 1     |
| 0     | 0     | 0     | 0     | 0     | 0     | 1     | 1     | 1     |
| 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |

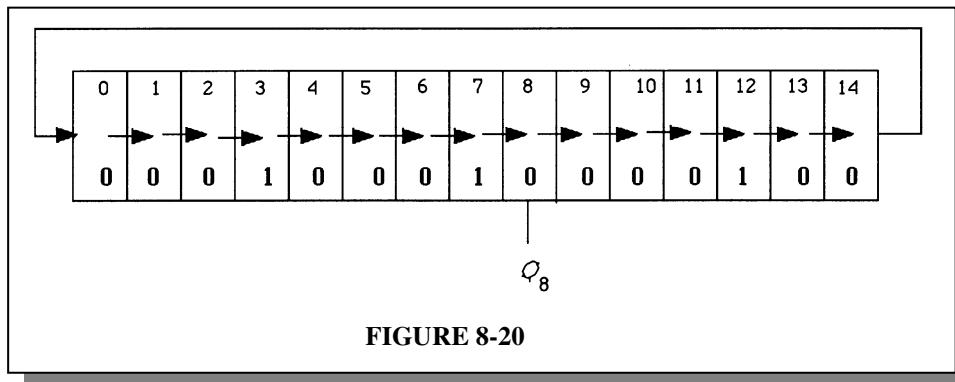
See Figure 8-18.



27. See Figure 8-19.



28. A 15-bit ring counter with stages **3**, **7**, and **12** SET and the remaining stages RESET. See Figure 8-20.



## Chapter 8

### Section 8-5 Shift Register Applications

29. See Figure 8-21.

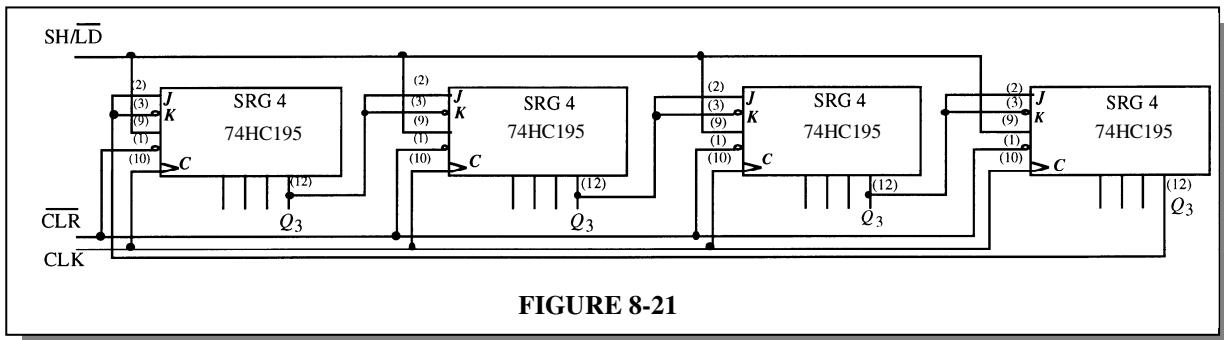


FIGURE 8-21

30. The power-on  $\overline{LOAD}$  input provides a momentary LOW to parallel load the ring counter when power is turned on.

31. An incorrect code may be produced.

### Section 8-7 Troubleshooting

32.  $Q_2$  goes HIGH on the first clock pulse indicating that the  $D$  input is open. See Figure 8-22.

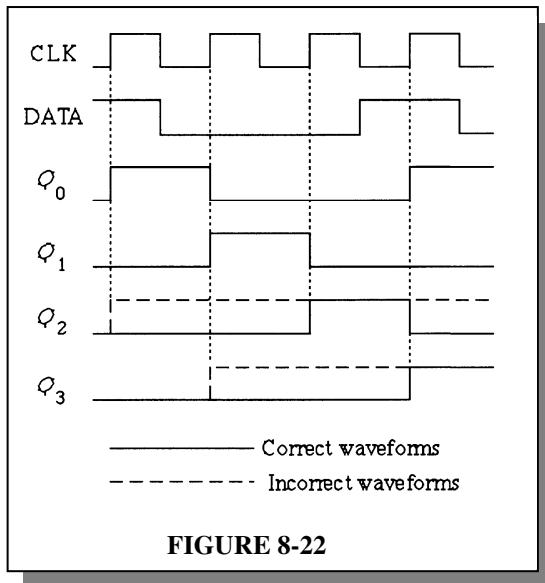
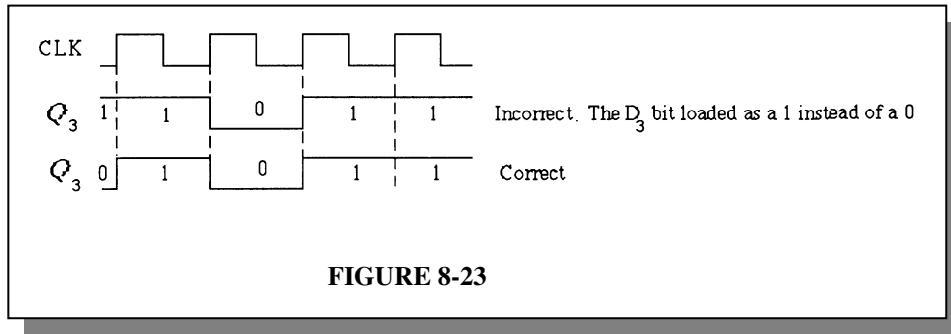


FIGURE 8-22

- 33.** Since the LSB flip-flop works during serial shift, the problem is most likely in gate G3. An open  $D_3$  input at G3 will cause the observed waveform. See Figure 8-23.



**FIGURE 8-23**

- 34.** It takes a LOW on the RIGHT/LEFT input to shift data left. An open inverter input will keep the inverter output LOW thus disabling all of the shift-left control gates G5, G6, G7, and G8.
- 35.** (a) No clock at switch closure due to faulty NAND gate or one-shot; open clock input to key code register; open SH/LD input to key code register.  
 (b) The diode in the third row is open;  $Q_2$  output of ring counter is open.  
 (c) The NAND (negative-OR) gate input connected to the first column is shorted to ground or open, preventing a switch closure transition.  
 (d) The “2” input to the column encoder is open.
- 36.** 1. Number the switches in the matrix according to the following format:

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  |
| 9  | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
| 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 |
| 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 |
| 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 |
| 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 |
| 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 |
| 57 | 58 | 59 | 60 | 61 | 62 | 63 | 64 |

## **Chapter 8**

2. Depress switches one at a time and observe the key code output according to the following Table 1.

| Switch number | Key Code Register |       |       |       |       |       |
|---------------|-------------------|-------|-------|-------|-------|-------|
|               | $Q_0$             | $Q_1$ | $Q_2$ | $Q_3$ | $Q_4$ | $Q_5$ |
| 1             | 0                 | 1     | 1     | 0     | 1     | 1     |
| 2             | 0                 | 1     | 1     | 1     | 0     | 1     |
| 3             | 0                 | 1     | 1     | 0     | 0     | 1     |
| 4             | 0                 | 1     | 1     | 1     | 1     | 0     |
| 5             | 0                 | 1     | 1     | 0     | 1     | 0     |
| 6             | 0                 | 1     | 1     | 1     | 0     | 0     |
| 7             | 0                 | 1     | 1     | 0     | 0     | 0     |
| 8             | 0                 | 1     | 1     | 1     | 1     | 1     |
| 9             | 1                 | 0     | 1     | 0     | 1     | 1     |
| 10            | 1                 | 0     | 1     | 1     | 0     | 1     |
| 11            | 1                 | 0     | 1     | 0     | 0     | 1     |
| 12            | 1                 | 0     | 1     | 1     | 1     | 0     |
| 13            | 1                 | 0     | 1     | 0     | 1     | 0     |
| 14            | 1                 | 0     | 1     | 1     | 0     | 0     |
| 15            | 1                 | 0     | 1     | 0     | 0     | 0     |
| 16            | 1                 | 0     | 1     | 1     | 1     | 1     |
| 17            | 0                 | 0     | 1     | 0     | 1     | 1     |
| 18            | 0                 | 0     | 1     | 1     | 0     | 1     |
| 19            | 0                 | 0     | 1     | 0     | 0     | 1     |
| 20            | 0                 | 0     | 1     | 1     | 1     | 0     |
| 21            | 0                 | 0     | 1     | 0     | 1     | 0     |
| 22            | 0                 | 0     | 1     | 1     | 0     | 0     |
| 23            | 0                 | 0     | 1     | 0     | 0     | 0     |
| 24            | 0                 | 0     | 1     | 1     | 1     | 1     |
| 25            | 1                 | 1     | 0     | 0     | 1     | 1     |
| 26            | 1                 | 1     | 0     | 1     | 0     | 1     |
| 27            | 1                 | 1     | 0     | 0     | 0     | 1     |
| 28            | 1                 | 1     | 0     | 1     | 1     | 0     |
| 29            | 1                 | 1     | 0     | 0     | 1     | 0     |
| 30            | 1                 | 1     | 0     | 1     | 0     | 0     |
| 31            | 1                 | 1     | 0     | 0     | 0     | 0     |
| 32            | 1                 | 1     | 0     | 1     | 1     | 1     |
| 33            | 0                 | 1     | 0     | 0     | 1     | 1     |
| 34            | 0                 | 1     | 0     | 1     | 0     | 1     |
| 35            | 0                 | 1     | 0     | 0     | 0     | 1     |
| 36            | 0                 | 1     | 0     | 1     | 1     | 0     |
| 37            | 0                 | 1     | 0     | 0     | 1     | 0     |
| 38            | 0                 | 1     | 0     | 1     | 0     | 0     |
| 39            | 0                 | 1     | 0     | 0     | 0     | 0     |
| 40            | 0                 | 1     | 0     | 1     | 1     | 1     |
| 41            | 1                 | 0     | 0     | 0     | 1     | 1     |
| 42            | 1                 | 0     | 0     | 1     | 0     | 1     |
| 43            | 1                 | 0     | 0     | 0     | 0     | 1     |
| 44            | 1                 | 0     | 0     | 1     | 1     | 0     |
| 45            | 1                 | 0     | 0     | 0     | 1     | 0     |
| 46            | 1                 | 0     | 0     | 1     | 0     | 0     |

|    |   |   |   |   |   |   |
|----|---|---|---|---|---|---|
| 47 | 1 | 0 | 0 | 0 | 0 | 0 |
| 48 | 1 | 0 | 0 | 1 | 1 | 1 |
| 49 | 0 | 0 | 0 | 0 | 1 | 1 |
| 50 | 0 | 0 | 0 | 1 | 0 | 1 |
| 51 | 0 | 0 | 0 | 0 | 0 | 1 |
| 52 | 0 | 0 | 0 | 1 | 1 | 0 |
| 53 | 0 | 0 | 0 | 0 | 1 | 0 |
| 54 | 0 | 0 | 0 | 1 | 0 | 0 |
| 55 | 0 | 0 | 0 | 0 | 0 | 0 |
| 56 | 0 | 0 | 0 | 1 | 1 | 1 |
| 57 | 1 | 1 | 1 | 0 | 1 | 1 |
| 58 | 1 | 1 | 1 | 1 | 0 | 1 |
| 59 | 1 | 1 | 1 | 0 | 0 | 1 |
| 60 | 1 | 1 | 1 | 1 | 1 | 0 |
| 61 | 1 | 1 | 1 | 0 | 1 | 0 |
| 62 | 1 | 1 | 1 | 1 | 0 | 0 |
| 63 | 1 | 1 | 1 | 0 | 0 | 0 |
| 64 | 1 | 1 | 1 | 1 | 1 | 1 |

**TABLE 1**

- 37.** (a) Contents of Data Output Register remain constant.  
 (b) Contents of both registers do not change.  
 (c) Third stage output of Data Output Register remains HIGH.  
 (d) Clock generator is disabled after each pulse by the flip-flop being continuously SET and then RESET.

### **Applied Logic**

- 38.** The purpose of the Security Code logic is to accept a 4-digit code, compare it with a stored code, and if the codes match, to disarm the system for entry.
- 39.** The states of shift registers A and C after two correct key closures are:

Shift Register A: 1001  
 Shift Register C: 00000100

- 40.** The states of shift registers A and B after each key closure when entering 7645 are:

**After key 7 is pressed:**

Shift register A contains 0111  
 Shift register B contains 11000

**After key 6 is pressed:**

Shift register A contains 0110  
 Shift register B contains 11100

**After key 4 is pressed:**

Shift register A contains 0100  
 Shift register B contains 11110

**After key 5 (an incorrect entry) is pressed:**

Shift register A contains 0000  
 Shift register B contains 10000

## Chapter 8

### Special Design Problems

41. See Figure 8-24.

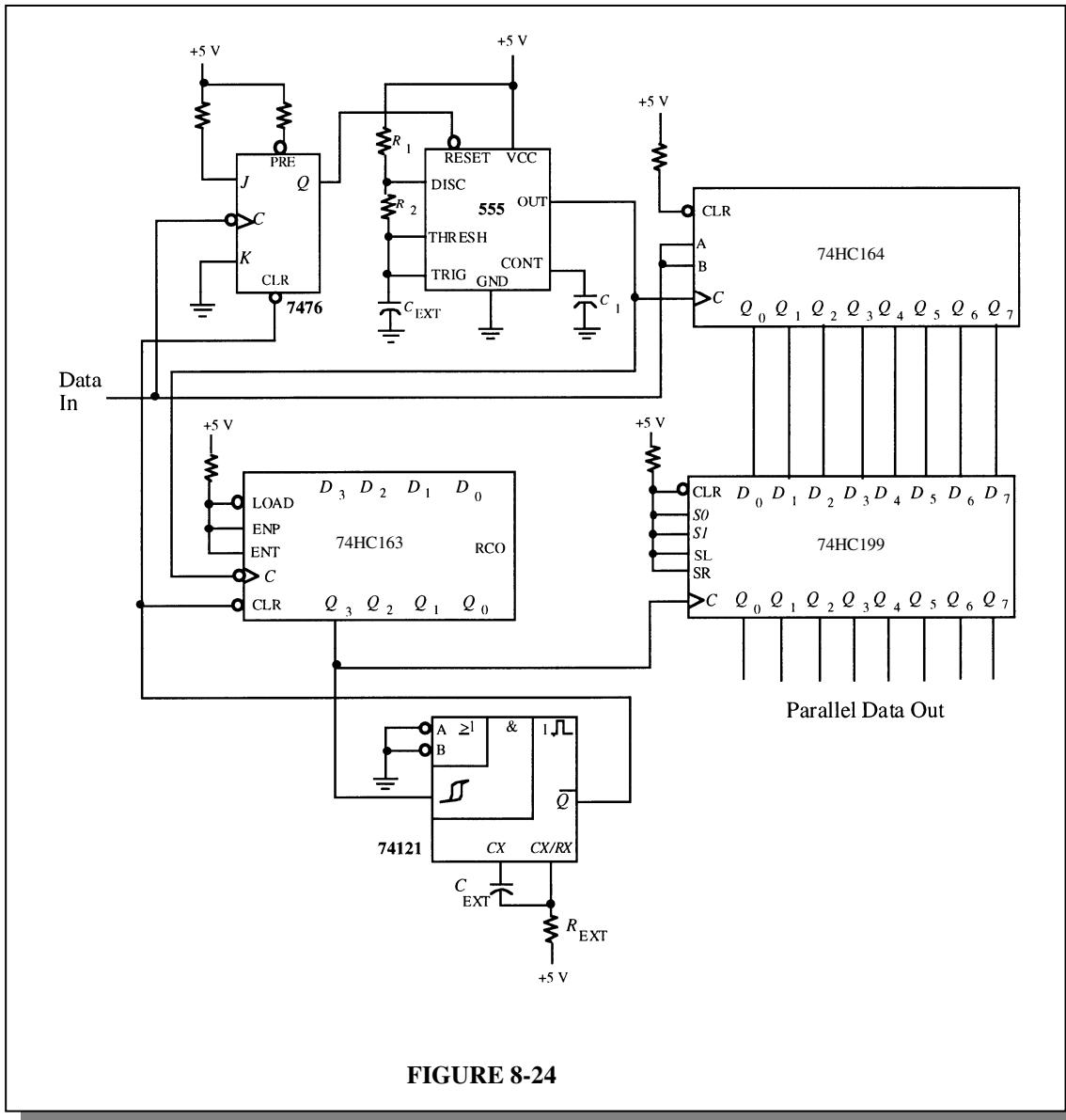
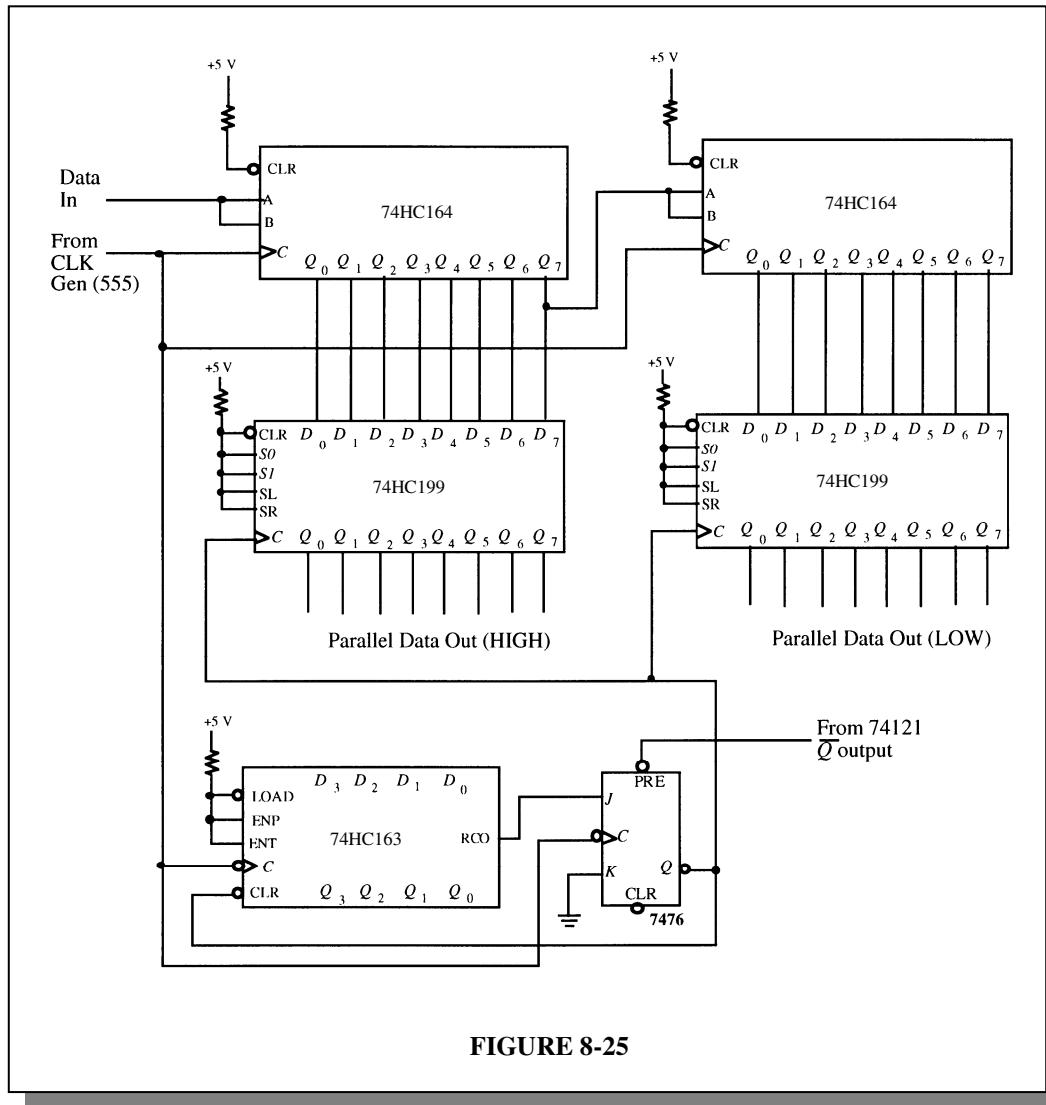


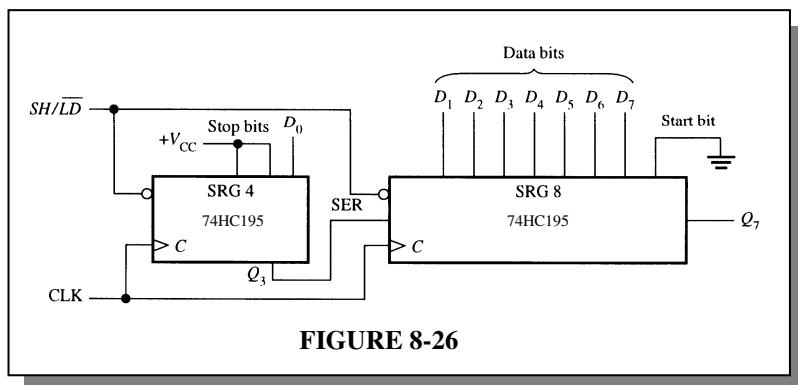
FIGURE 8-24

42. Figure 8-25 shows only the 74LS164, 74LS199, and 74LS163 portions of the circuit that require modification for 16-bit conversion.



**FIGURE 8-25**

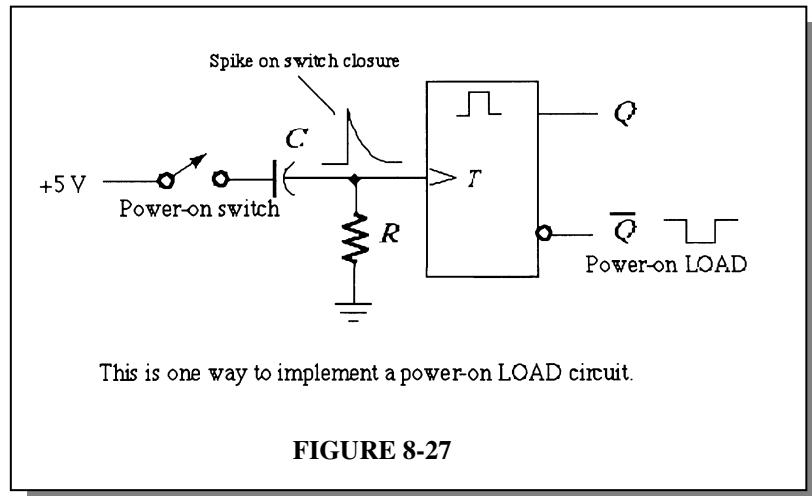
43. See Figure 8-26 for one possible implementation.



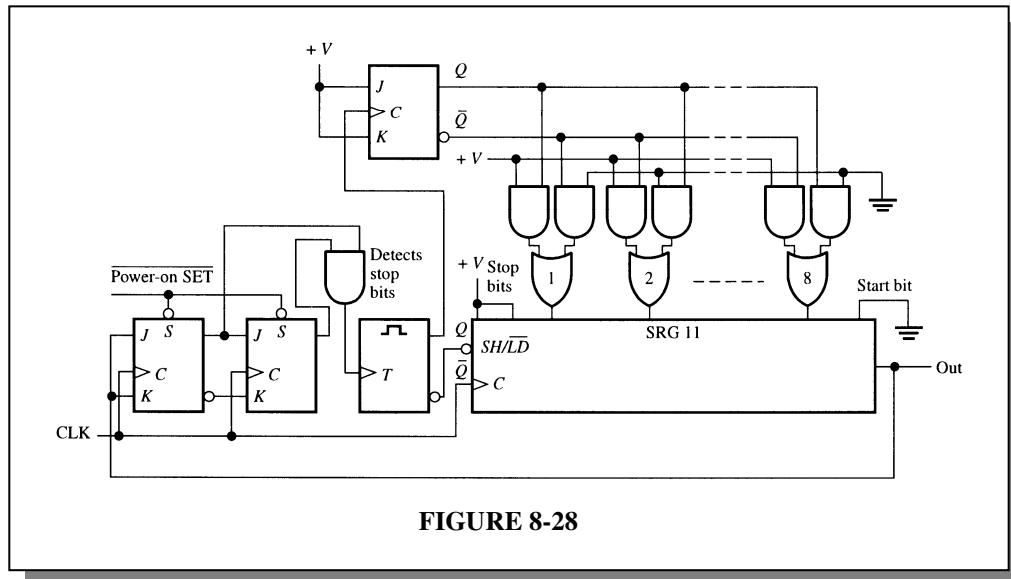
**FIGURE 8-26**

## Chapter 8

44. One possible approach is shown in Figure 8-27.



45. See Figure 8-28.



46. Register A requires 8 bits and can be implemented with one 74HC199. Register B requires 16 bits and can be implemented with two 74HC199s.

### Multisim Troubleshooting Practice

47. The D input of FF is shorted to ground  
48. The input of the inverter U1 is shorted to ground.  
49. The U3 Q' output of the Johnson counter is connected to the U2 D input

- 50.** The K input of the 74195 shift register is always HIGH (shorted to  $V_{CC}$ ), so that the input cannot toggle the serial data or leave it unchanged.
- 51.** The connection between the Q output of U3 and D input of U4 is open.

---

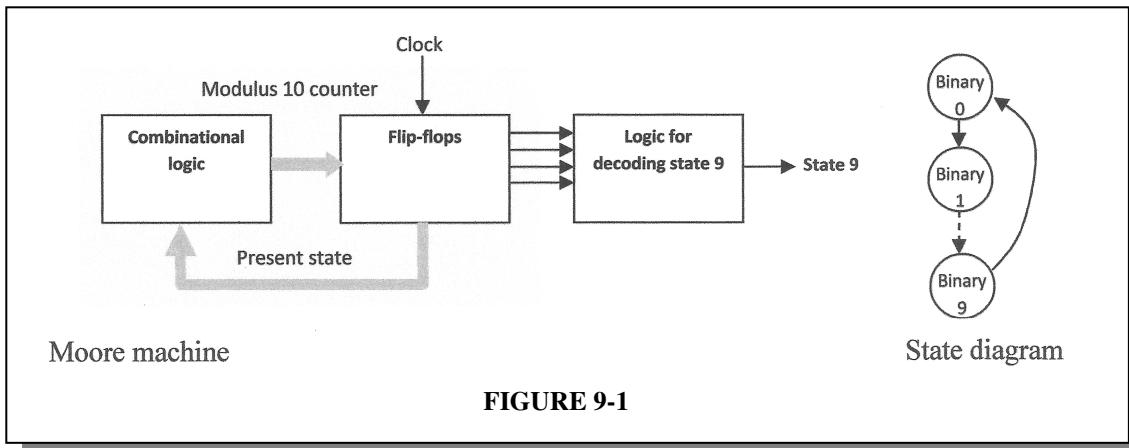
# CHAPTER 9

## COUNTERS

---

### Section 9-1 Finite State Machines

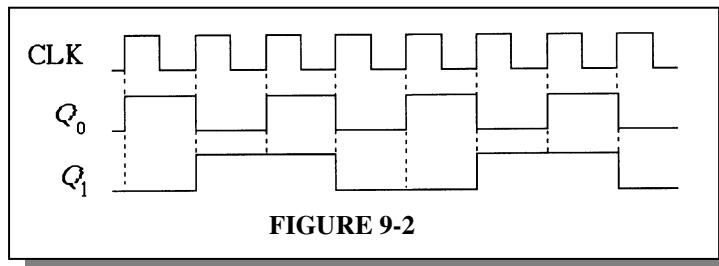
- See Figure 9-1.



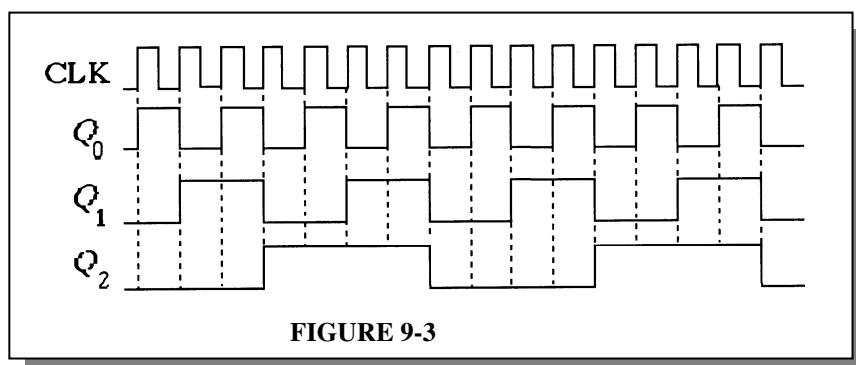
- The traffic signal controller is a Mealy machine. The next state depends not only on the present state but also on the  $T_L$ ,  $T_S$ , and  $V_s$  inputs.

### Section 9-2 Asynchronous Counter Operation

- See Figure 9-2.



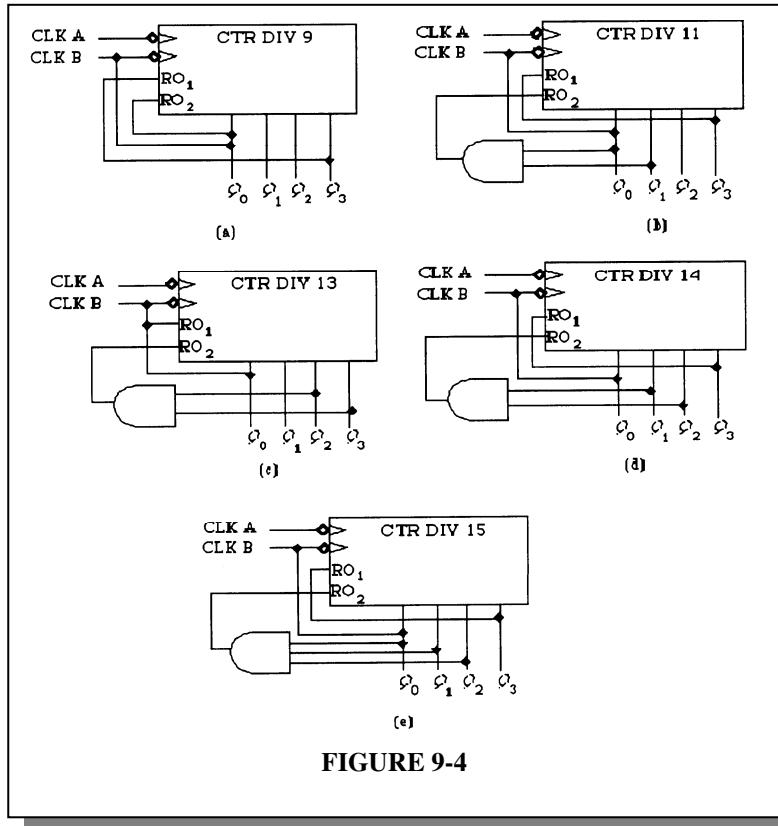
- See Figure 9-3.



5.  $t_{p(\max)} = 3(8 \text{ ns}) = 24 \text{ ns}$

Worst-case delay occurs when all flip-flops change state from 011 to 100 or from 111 to 000.

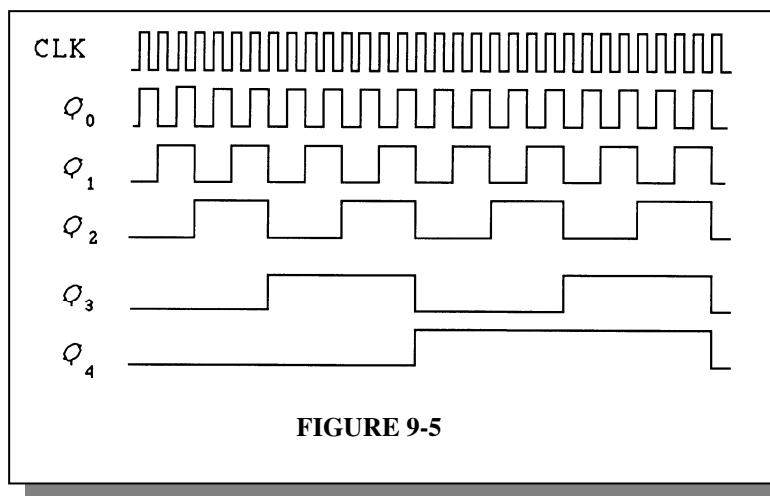
6. See Figure 9-4.



### **Section 9-3 Synchronous Counter Operation**

7. **8 ns**, the time it takes one flip-flop to change state.

8. See Figure 9-5.



## Chapter 9

9. Each flip-flop is initially reset.

| CLK | $J_0K_0$ | $J_1K_1$ | $J_2K_2$ | $J_3K_3$ | $Q_0$ | $Q_1$ | $Q_2$ | $Q_3$ |
|-----|----------|----------|----------|----------|-------|-------|-------|-------|
| 1   | 1        | 0        | 0        | 0        | 1     | 0     | 0     | 0     |
| 2   | 1        | 1        | 0        | 0        | 0     | 1     | 0     | 0     |
| 3   | 1        | 0        | 0        | 0        | 1     | 1     | 0     | 0     |
| 4   | 1        | 1        | 1        | 0        | 0     | 0     | 1     | 0     |
| 5   | 1        | 0        | 0        | 0        | 1     | 0     | 1     | 0     |
| 6   | 1        | 1        | 0        | 0        | 0     | 1     | 1     | 0     |
| 7   | 1        | 0        | 0        | 0        | 1     | 1     | 1     | 0     |
| 8   | 1        | 1        | 1        | 1        | 0     | 0     | 0     | 1     |
| 9   | 1        | 0        | 0        | 0        | 1     | 0     | 0     | 1     |
| 10  | 1        | 0        | 0        | 1        | 0     | 0     | 0     | 0     |

10. See Figure 9-6.

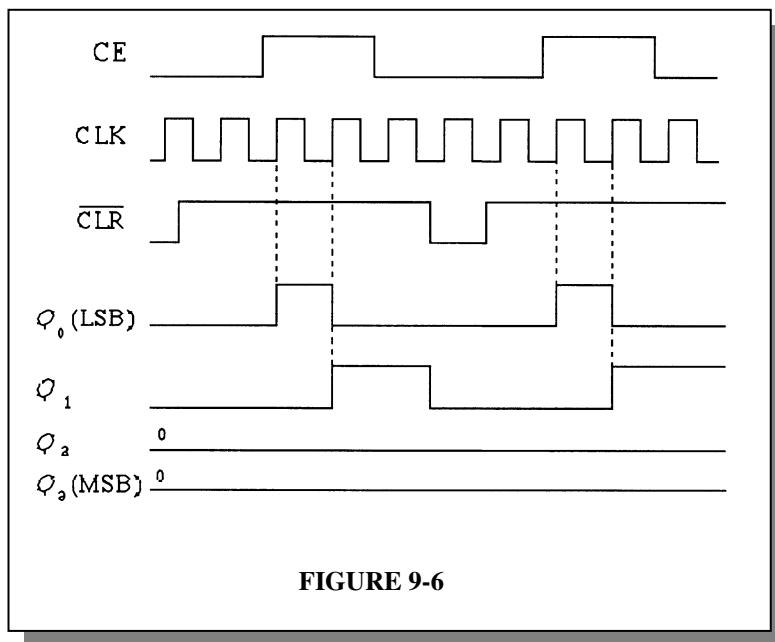


FIGURE 9-6

11. See Figure 9-7.

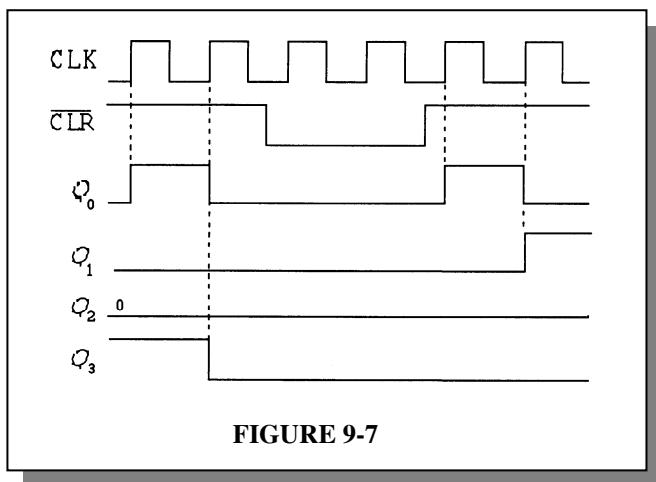
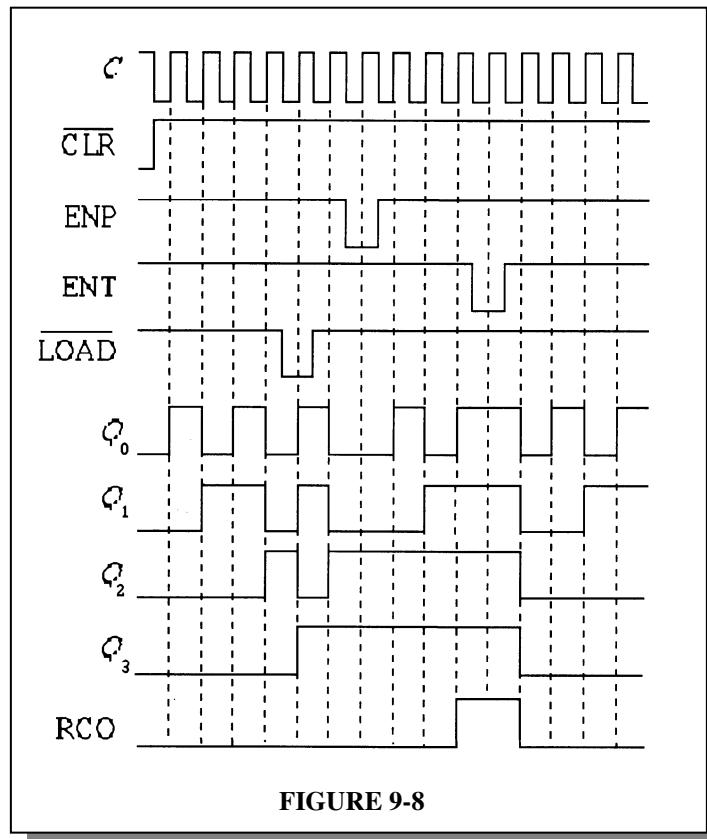


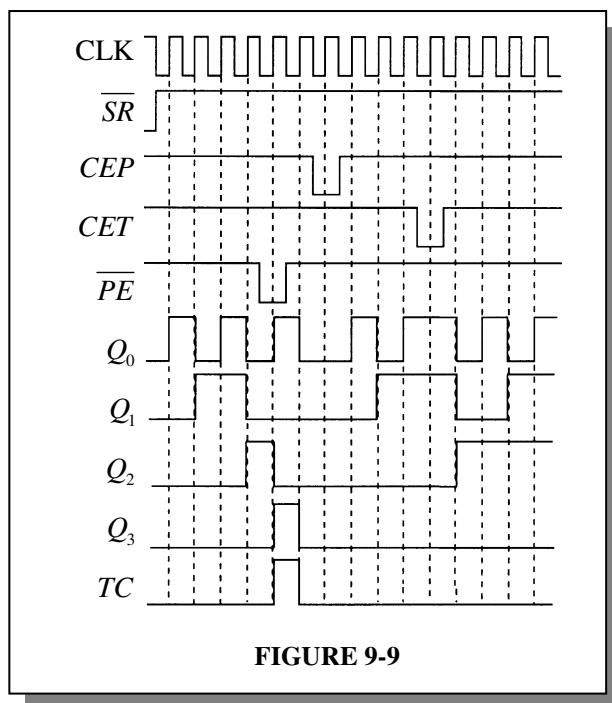
FIGURE 9-7

12. See Figure 9-8.



**FIGURE 9-8**

13. See Figure 9-9.



**FIGURE 9-9**

## Chapter 9

### Section 9-4 Up/Down Synchronous Counters

14. See Figure 9-10.

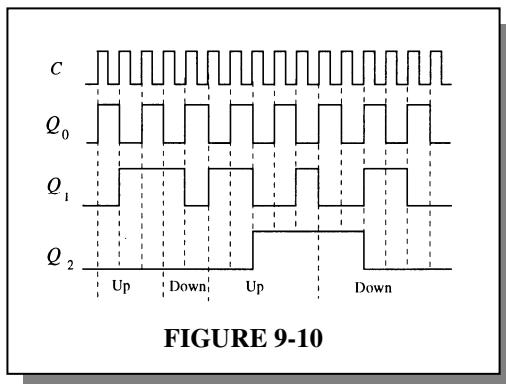


FIGURE 9-10

15. See Figure 9-11.

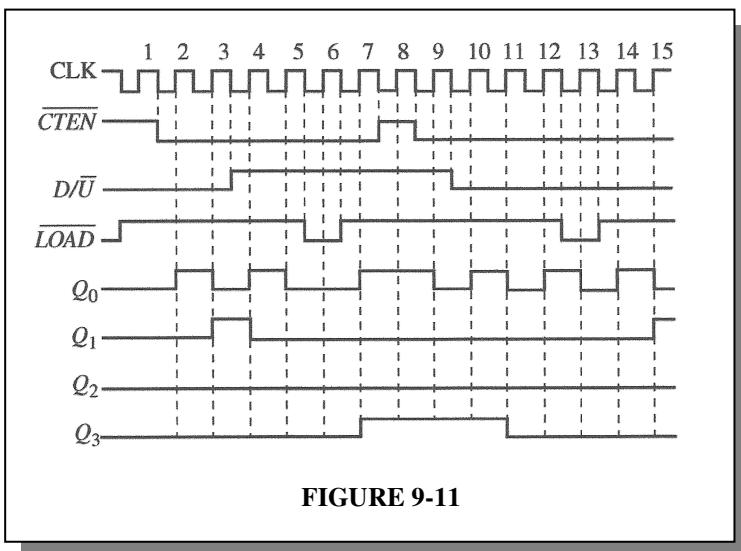


FIGURE 9-11

16. See Fig 9-12.

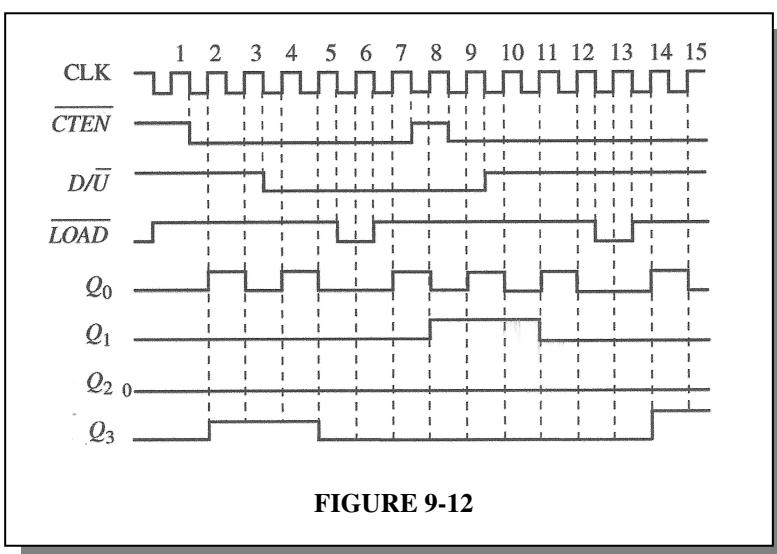
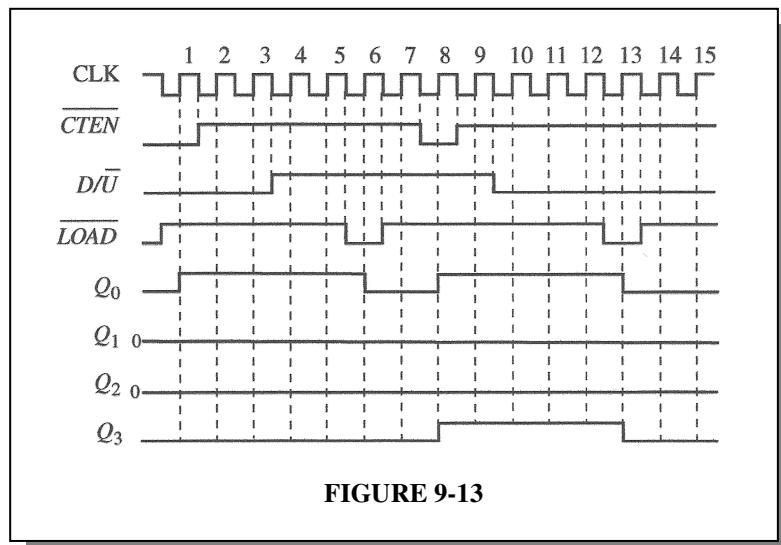


FIGURE 9-12

17. See Fig 9-13.



### **Section 9-5 Design of Synchronous Counters**

18.

|           | $Q_2$ | $Q_1$ | $Q_0$ | $D_2$ | $D_1$ | $D_0$ |
|-----------|-------|-------|-------|-------|-------|-------|
| Initially | 0     | 0     | 0     | 0     | 0     | 1     |
| At CLK 1  | 0     | 0     | 1     | 0     | 1     | 1     |
| At CLK 2  | 0     | 1     | 1     | 1     | 1     | 1     |
| At CLK 3  | 1     | 1     | 1     | 1     | 1     | 0     |
| At CLK 4  | 1     | 1     | 0     | 1     | 0     | 0     |
| At CLK 5  | 1     | 0     | 0     | 0     | 0     | 1     |
| At CLK 6  | 0     | 0     | 1     | 0     | 1     | 1     |

The sequence is 000 to 001 to 011 to 111 to 110 to 100 and back to 001, etc.

19.

|             | FF3 | FF2 | FF1 | FF0 | $Q_3$ | $Q_2$ | $Q_1$ | $Q_0$ |
|-------------|-----|-----|-----|-----|-------|-------|-------|-------|
| Initially   | Tog | Tog | Tog | Tog | 0     | 0     | 0     | 0     |
| After CLK 1 | NC  | NC  | NC  | Tog | 1     | 1     | 1     | 1     |
| After CLK 2 | NC  | NC  | Tog | Tog | 1     | 1     | 1     | 0     |
| After CLK 3 | NC  | Tog | Tog | Tog | 1     | 1     | 0     | 1     |
| After CLK 4 | Tog | Tog | Tog | Tog | 1     | 0     | 1     | 0     |
| After CLK 5 | Tog | Tog | Tog | Tog | 0     | 1     | 0     | 1     |

Tog = toggle, NC = no change

The counter locks up in the 1010 and 0101 states, alternating between them.

## Chapter 9

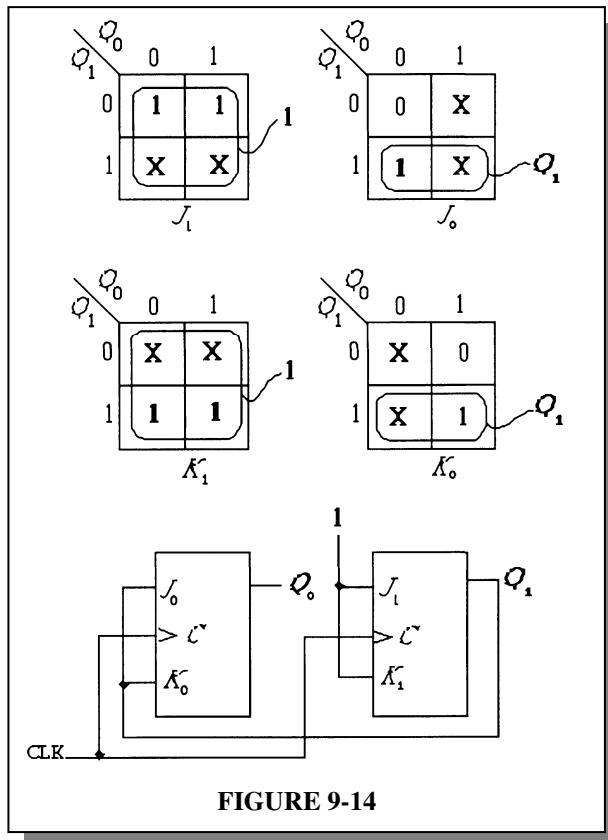
### 20. NEXT-STATE TABLE

| Present State |       | Next State |       |
|---------------|-------|------------|-------|
| $Q_1$         | $Q_0$ | $Q_1$      | $Q_0$ |
| 0             | 0     | 1          | 0     |
| 1             | 0     | 0          | 1     |
| 0             | 1     | 1          | 1     |
| 1             | 1     | 0          | 0     |

### TRANSITION TABLE

| Output State Transitions<br>(Present state to next state) |        | Flip-Flop Inputs |       |       |       |
|-----------------------------------------------------------|--------|------------------|-------|-------|-------|
| $Q_1$                                                     | $Q_0$  | $J_1$            | $K_1$ | $J_0$ | $K_0$ |
| 0 to 1                                                    | 0 to 0 | 1                | X     | 0     | X     |
| 1 to 0                                                    | 0 to 1 | X                | 1     | 1     | X     |
| 0 to 1                                                    | 1 to 1 | 1                | X     | X     | 0     |
| 1 to 0                                                    | 1 to 0 | X                | 1     | X     | 1     |

See Figure 9-14.



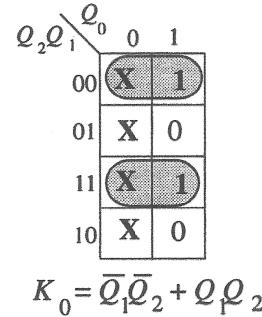
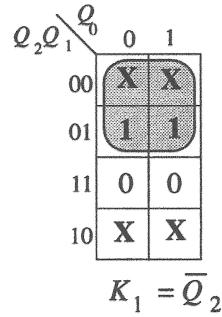
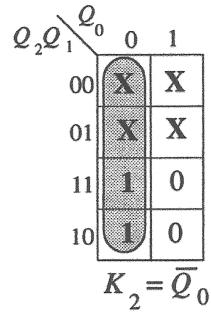
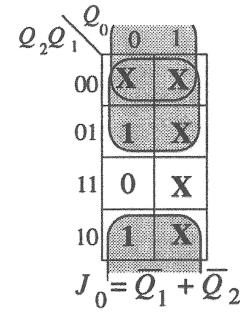
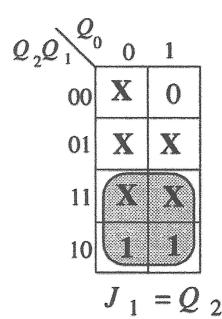
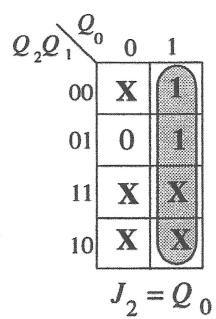
## 21. NEXT-STATE TABLE

| Present State |       |       | Next State |       |       |
|---------------|-------|-------|------------|-------|-------|
| $Q_2$         | $Q_1$ | $Q_0$ | $Q_2$      | $Q_1$ | $Q_0$ |
| 0             | 0     | 1     | 1          | 0     | 0     |
| 1             | 0     | 0     | 0          | 1     | 1     |
| 0             | 1     | 1     | 1          | 0     | 1     |
| 1             | 0     | 1     | 1          | 1     | 1     |
| 1             | 1     | 1     | 1          | 1     | 0     |
| 1             | 1     | 0     | 0          | 1     | 0     |
| 0             | 1     | 0     | 0          | 0     | 1     |

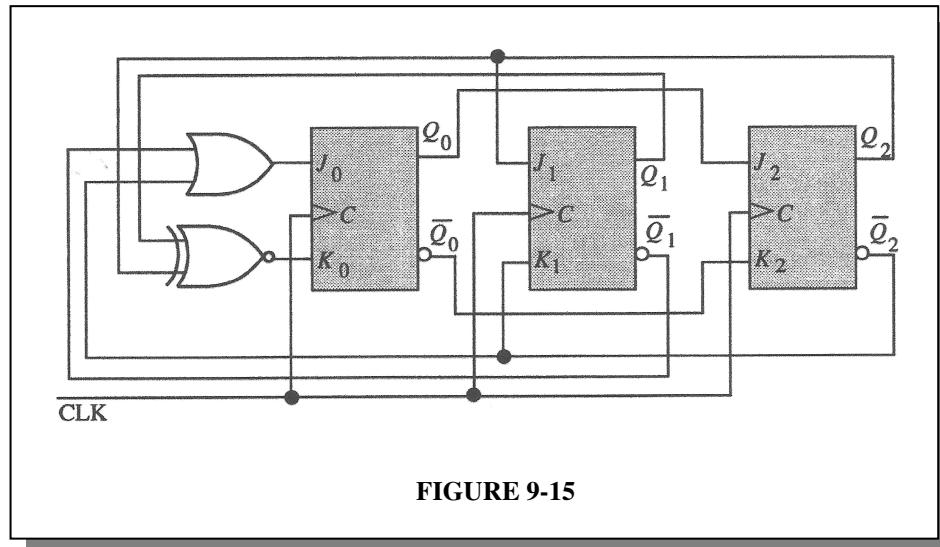
## TRANSITION TABLE

| Output State Transitions<br>(Present state to next state) |        |        | Flip-flop Inputs |       |       |       |       |       |
|-----------------------------------------------------------|--------|--------|------------------|-------|-------|-------|-------|-------|
| $Q_2$                                                     | $Q_1$  | $Q_0$  | $J_2$            | $K_2$ | $J_1$ | $K_1$ | $J_0$ | $K_0$ |
| 0 to 1                                                    | 0 to 0 | 1 to 0 | 1                | X     | 0     | X     | X     | 1     |
| 1 to 0                                                    | 0 to 1 | 0 to 1 | X                | 1     | 1     | X     | 1     | X     |
| 0 to 1                                                    | 1 to 0 | 1 to 1 | 1                | X     | X     | 1     | X     | 0     |
| 1 to 1                                                    | 0 to 1 | 1 to 1 | X                | 0     | 1     | X     | X     | 0     |
| 1 to 1                                                    | 1 to 1 | 1 to 0 | X                | 0     | X     | 0     | X     | 1     |
| 0 to 0                                                    | 1 to 0 | 0 to 1 | 0                | X     | X     | 1     | 1     | X     |
| 1 to 0                                                    | 1 to 1 | 0 to 0 | X                | 1     | X     | 0     | 0     | X     |

See Figure 9-15.



## Chapter 9



**FIGURE 9-15**

### 22. NEXT-STATE TABLE

| Present State |       |       |       | Next State |       |       |       |
|---------------|-------|-------|-------|------------|-------|-------|-------|
| $Q_3$         | $Q_2$ | $Q_1$ | $Q_0$ | $Q_3$      | $Q_2$ | $Q_1$ | $Q_0$ |
| 0             | 0     | 0     | 0     | 1          | 0     | 0     | 1     |
| 1             | 0     | 0     | 1     | 0          | 0     | 0     | 1     |
| 0             | 0     | 0     | 1     | 1          | 0     | 0     | 0     |
| 1             | 0     | 0     | 0     | 0          | 0     | 1     | 0     |
| 0             | 0     | 1     | 0     | 0          | 1     | 1     | 1     |
| 0             | 1     | 1     | 1     | 0          | 0     | 1     | 1     |
| 0             | 0     | 1     | 1     | 0          | 1     | 1     | 0     |
| 0             | 1     | 1     | 0     | 0          | 1     | 0     | 0     |
| 0             | 1     | 0     | 0     | 0          | 1     | 0     | 1     |
| 0             | 1     | 0     | 1     | 0          | 0     | 0     | 0     |

### TRANSITION TABLE

| Output State Transition<br>(Present State to next state) |        |        |        | Flip-flop Inputs |       |       |       |       |       |       |       |
|----------------------------------------------------------|--------|--------|--------|------------------|-------|-------|-------|-------|-------|-------|-------|
| $Q_3$                                                    | $Q_2$  | $Q_1$  | $Q_0$  | $J_3$            | $K_3$ | $J_2$ | $K_2$ | $J_1$ | $K_1$ | $J_0$ | $K_0$ |
| 0 to 1                                                   | 0 to 0 | 0 to 0 | 0 to 1 | 1                | X     | 0     | X     | 0     | X     | 1     | X     |
| 1 to 0                                                   | 0 to 0 | 0 to 0 | 0 to 1 | X                | 1     | 0     | X     | 0     | X     | X     | 0     |
| 0 to 1                                                   | 0 to 0 | 0 to 0 | 1 to 0 | 1                | X     | 0     | X     | 0     | X     | X     | 1     |
| 1 to 0                                                   | 0 to 0 | 0 to 1 | 0 to 0 | X                | 1     | 0     | X     | 1     | X     | 0     | X     |
| 0 to 0                                                   | 0 to 1 | 1 to 1 | 0 to 1 | 0                | X     | 1     | X     | X     | 0     | 1     | X     |
| 0 to 0                                                   | 1 to 0 | 1 to 1 | 1 to 1 | 0                | X     | X     | 1     | X     | 0     | X     | 0     |
| 0 to 0                                                   | 0 to 1 | 1 to 1 | 1 to 0 | 0                | X     | 1     | X     | X     | 0     | X     | 1     |
| 0 to 0                                                   | 1 to 1 | 1 to 0 | 0 to 0 | 0                | X     | X     | 0     | X     | 1     | 0     | X     |
| 0 to 0                                                   | 1 to 1 | 0 to 0 | 0 to 1 | 0                | X     | X     | 0     | 0     | X     | 1     | X     |
| 0 to 0                                                   | 1 to 0 | 0 to 0 | 1 to 0 | 0                | X     | X     | 1     | 0     | X     | X     | 1     |

Binary states for 10, 11, 12, 13, 14, and 15 are unallowed and can be represented by don't cares.

See Figure 9-16. Counter implementation is straightforward from input expressions.

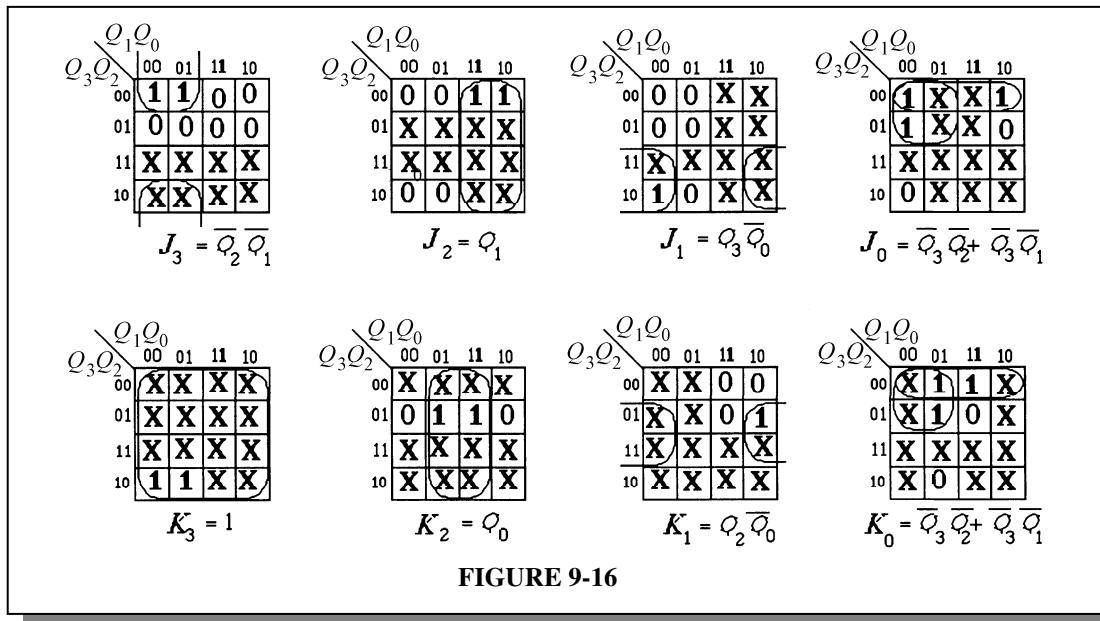


FIGURE 9-16

### 23. NEXT-STATE TABLE

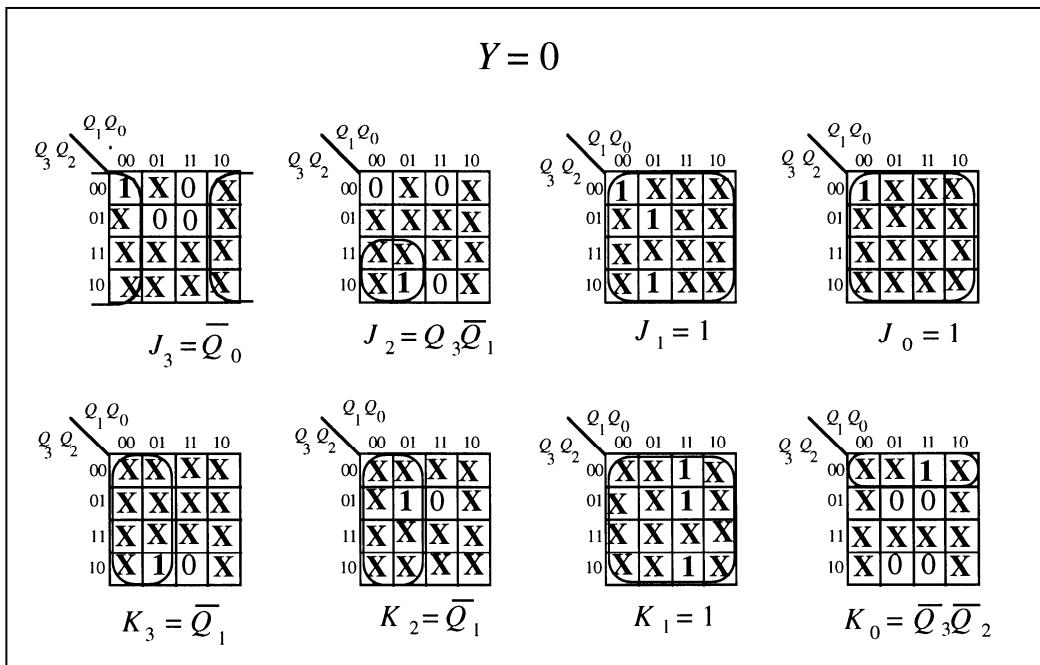
| Present State |       |       |       | Next State |       |       |       |              |       |       |       |
|---------------|-------|-------|-------|------------|-------|-------|-------|--------------|-------|-------|-------|
|               |       |       |       | Y = 1 (Up) |       |       |       | Y = 0 (Down) |       |       |       |
| $Q_3$         | $Q_2$ | $Q_1$ | $Q_0$ | $Q_3$      | $Q_2$ | $Q_1$ | $Q_0$ | $Q_3$        | $Q_2$ | $Q_1$ | $Q_0$ |
| 0             | 0     | 0     | 0     | 0          | 0     | 1     | 1     | 1            | 0     | 1     | 1     |
| 0             | 0     | 1     | 1     | 0          | 1     | 0     | 1     | 0            | 0     | 0     | 0     |
| 0             | 1     | 0     | 1     | 0          | 1     | 1     | 1     | 0            | 0     | 1     | 1     |
| 0             | 1     | 1     | 1     | 1          | 0     | 0     | 1     | 0            | 1     | 0     | 1     |
| 1             | 0     | 0     | 1     | 1          | 0     | 1     | 1     | 0            | 1     | 1     | 1     |
| 1             | 0     | 1     | 1     | 0          | 0     | 0     | 0     | 1            | 0     | 0     | 1     |

## Chapter 9

TRANSITION TABLE

| Output State Transitions<br>(Present State to next state) |        |        |        | $Y$ | Flip-flop Inputs |          |          |          |
|-----------------------------------------------------------|--------|--------|--------|-----|------------------|----------|----------|----------|
| $Q_3$                                                     | $Q_2$  | $Q_1$  | $Q_0$  |     | $J_3K_3$         | $J_2K_2$ | $J_1K_1$ | $J_0K_0$ |
| 0 to 1                                                    | 0 to 0 | 0 to 1 | 0 to 1 | 0   | 1X               | 0X       | 1X       | 1X       |
| 0 to 0                                                    | 0 to 0 | 0 to 1 | 0 to 1 | 1   | 0X               | 0X       | 1X       | 1X       |
| 0 to 0                                                    | 0 to 0 | 1 to 0 | 1 to 0 | 0   | 0X               | 0X       | X1       | X1       |
| 0 to 0                                                    | 0 to 1 | 1 to 0 | 1 to 1 | 1   | 0X               | 1X       | X1       | X0       |
| 0 to 0                                                    | 1 to 0 | 0 to 1 | 1 to 1 | 0   | 0X               | X1       | 1X       | X0       |
| 0 to 0                                                    | 1 to 1 | 0 to 1 | 1 to 1 | 1   | 0X               | X0       | 1X       | X0       |
| 0 to 0                                                    | 1 to 1 | 1 to 0 | 1 to 1 | 0   | 0X               | X0       | X1       | X0       |
| 0 to 1                                                    | 1 to 0 | 1 to 0 | 1 to 1 | 1   | 1X               | X1       | X1       | X0       |
| 1 to 0                                                    | 0 to 1 | 0 to 1 | 1 to 1 | 0   | X1               | 1X       | 1X       | X0       |
| 1 to 1                                                    | 0 to 0 | 0 to 1 | 1 to 1 | 1   | X0               | 0X       | 1X       | X0       |
| 1 to 1                                                    | 0 to 0 | 1 to 0 | 1 to 1 | 0   | X0               | 0X       | X1       | X0       |
| 1 to 0                                                    | 0 to 0 | 1 to 0 | 1 to 0 | 1   | X1               | 0X       | X1       | X1       |

See Figure 9-17.



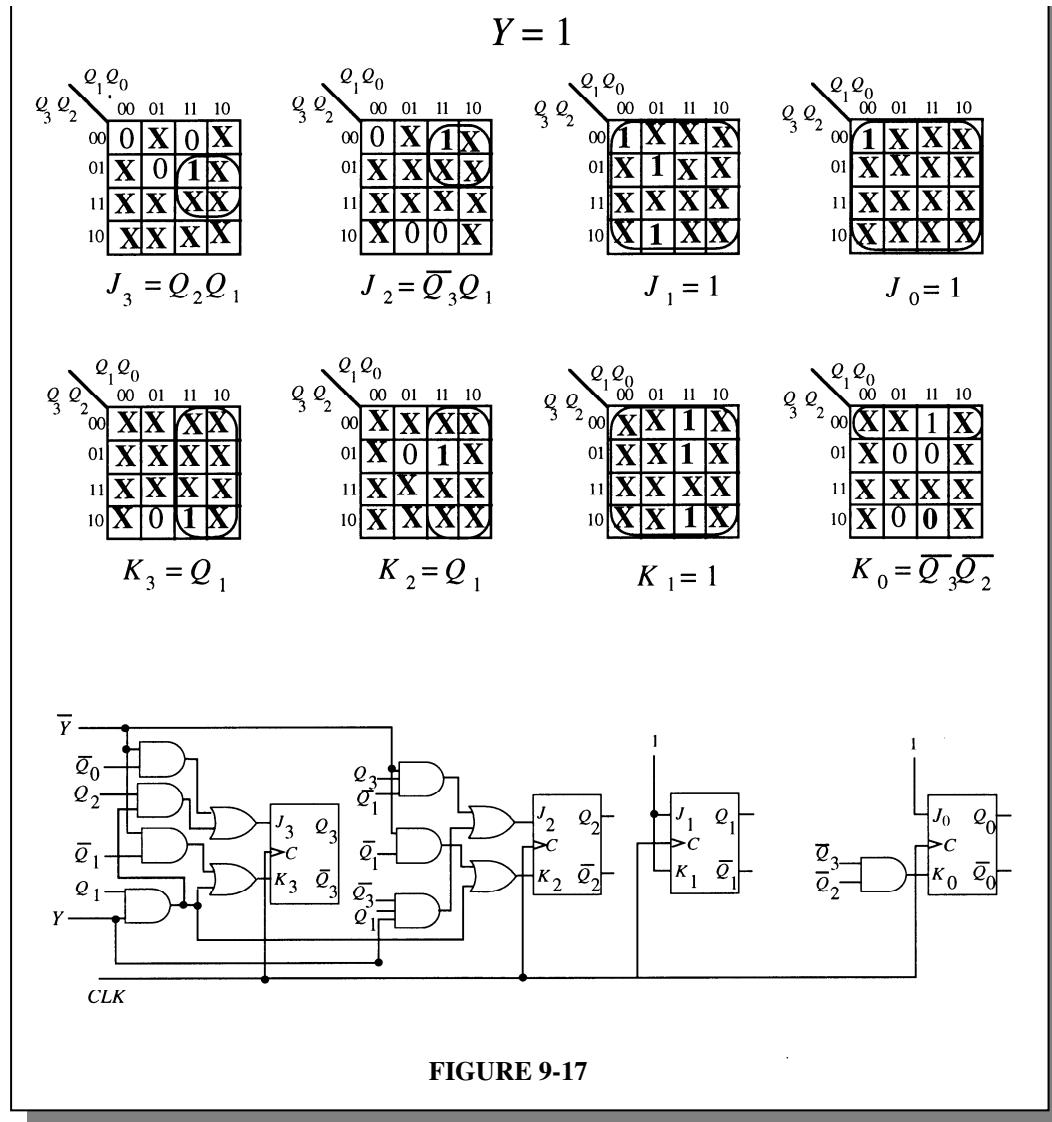


FIGURE 9-17

### Section 9-6 Cascaded Counters

24. (a) Modulus =  $4 \times 8 \times 2 = 64$

$$f_1 = \frac{1 \text{ kHz}}{4} = 250 \text{ Hz}$$

$$f_2 = \frac{250 \text{ Hz}}{8} = 31.25 \text{ Hz}$$

$$f_3 = \frac{31.25 \text{ Hz}}{2} = 15.625 \text{ Hz}$$

## Chapter 9

(b) Modulus =  $10 \times 10 \times 10 \times 2 = 2000$

$$f_1 = \frac{100 \text{ kHz}}{10} = 10 \text{ kHz}$$

$$f_2 = \frac{10 \text{ kHz}}{10} = 1 \text{ kHz}$$

$$f_3 = \frac{1 \text{ kHz}}{10} = 100 \text{ Hz}$$

$$f_4 = \frac{100 \text{ Hz}}{2} = 50 \text{ Hz}$$

(c) Modulus =  $3 \times 6 \times 8 \times 10 \times 10 = 14400$

$$f_1 = \frac{21 \text{ MHz}}{3} = 7 \text{ MHz}$$

$$f_2 = \frac{7 \text{ MHz}}{6} = 1.167 \text{ MHz}$$

$$f_3 = \frac{1.167 \text{ MHz}}{8} = 145.875 \text{ kHz}$$

$$f_4 = \frac{145.875 \text{ kHz}}{10} = 14.588 \text{ kHz}$$

$$f_5 = \frac{14.588 \text{ kHz}}{10} = 1.459 \text{ kHz}$$

(d) Modulus =  $2 \times 4 \times 6 \times 8 \times 16 = 6144$

$$f_1 = \frac{39.4 \text{ kHz}}{2} = 19.7 \text{ kHz}$$

$$f_2 = \frac{19.7 \text{ kHz}}{4} = 4.925 \text{ kHz}$$

$$f_3 = \frac{4.925 \text{ kHz}}{6} = 820.83 \text{ Hz}$$

$$f_4 = \frac{820.683}{8} = 102.6 \text{ Hz}$$

$$f_5 = \frac{102.6 \text{ Hz}}{16} = 6.41 \text{ Hz}$$

25. See Figure 9-18.

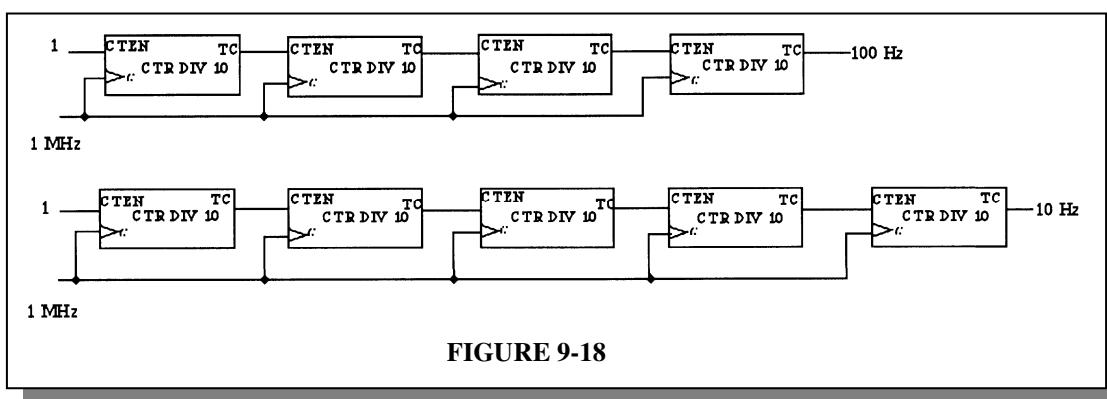
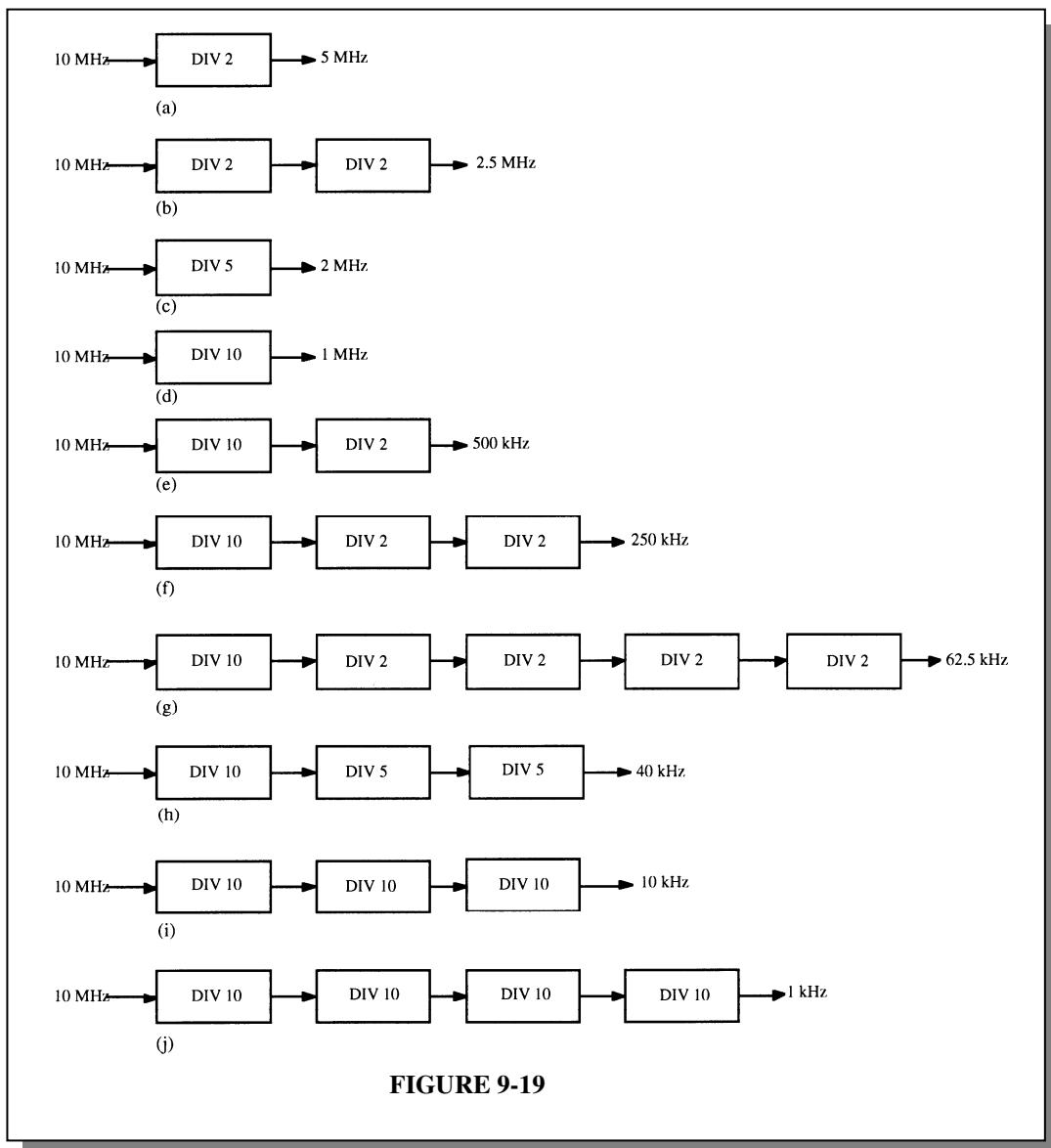


FIGURE 9-18

**26.** See Figure 9-19.

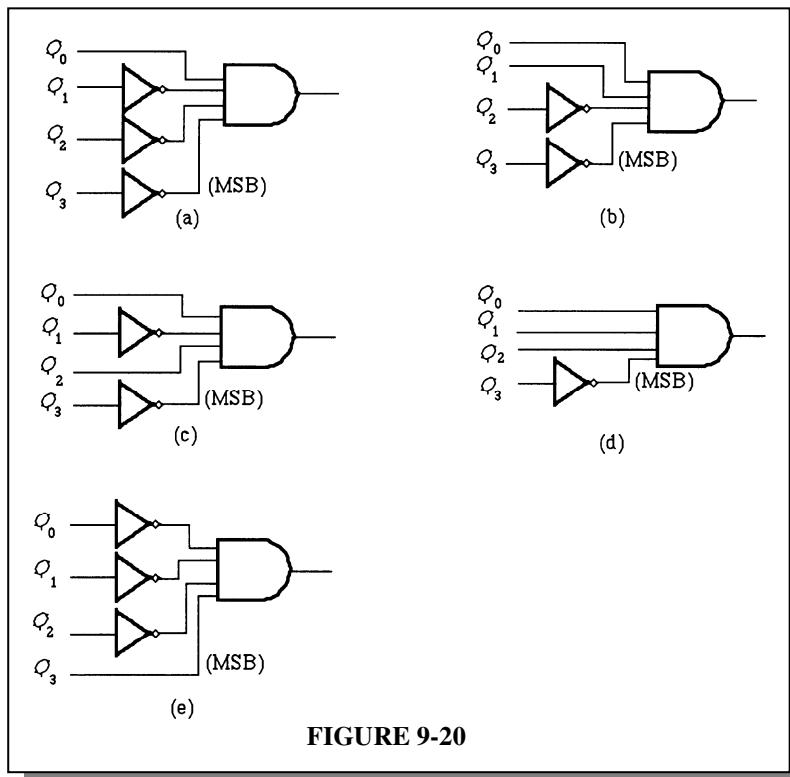


**FIGURE 9-19**

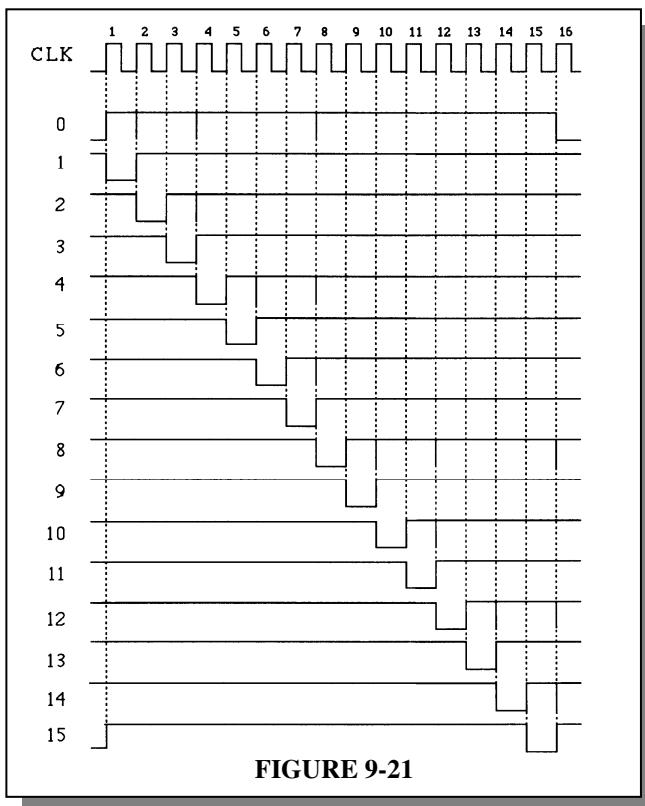
## Chapter 9

### Section 9-7 Counter Decoding

27. See Figure 9-20.



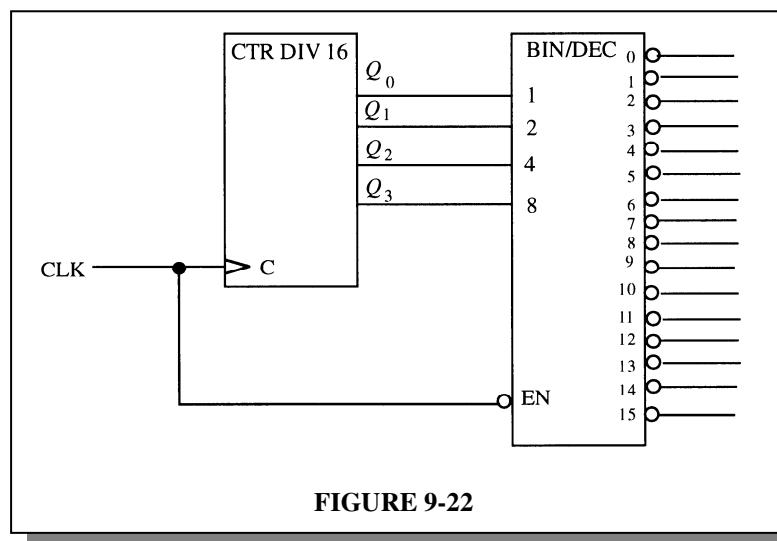
28. See Figure 9-21.



- 29.** The states with an asterisk are the transition states that produce glitches on the decoder outputs. The glitches are indicated on the waveforms in Figure 9-18 (Problem 9-24) by vertical lines.

|         |        |
|---------|--------|
| Initial | 0000   |
| CLK 1   | 0001   |
| CLK 2   | 0000 * |
|         | 0010   |
| CLK 3   | 0011   |
| CLK 4   | 0010 * |
|         | 0000 * |
|         | 0100   |
| CLK 5   | 0100   |
| CLK 6   | 0100 * |
|         | 0110   |
| CLK 7   | 0111   |
| CLK 8   | 0110 * |
|         | 0100 * |
|         | 0000 * |
|         | 1000   |
| CLK 9   | 1001   |
| CLK 10  | 1000*  |
|         | 1010   |
| CLK 11  | 1011   |
| CLK 12  | 1010 * |
|         | 1000 * |
|         | 1100   |
| CLK 13  | 1101   |
| CLK 14  | 1100 * |
|         | 1110   |
| CLK 15  | 1111   |
| CLK 16  | 1110 * |
|         | 1100 * |
|         | 1000 * |
|         | 0000   |

- 30.** See Figure 9-22.



**FIGURE 9-22**

## Chapter 9

31. See Figure 9-23.

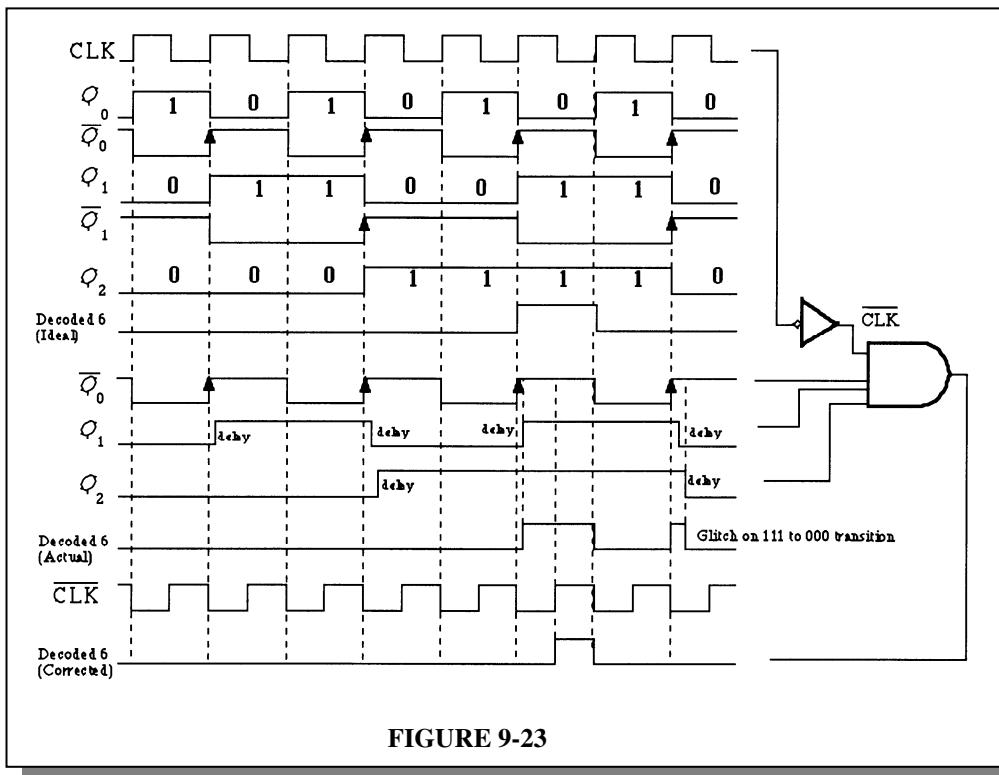


FIGURE 9-23

32. ① There is a possibility of a glitch on decode 2 at the positive-going edge of CLK 4 if the propagation delay of FF0 is less than FF1 or FF2.
- ② There is a possibility of a glitch on decode 7 at the positive-going edge of CLK 4 if the propagation delay of FF2 is less than FF0 and FF1.
- ③ There is a possibility of a glitch on decode 7 at the positive-going edge of CLK 6 if the propagation delay of FF1 is less than FF0.

See the timing diagram in Figure 9-24 which is expanded to show the delays.

Any glitches can be prevented by using CLK as an input to both decode gates.

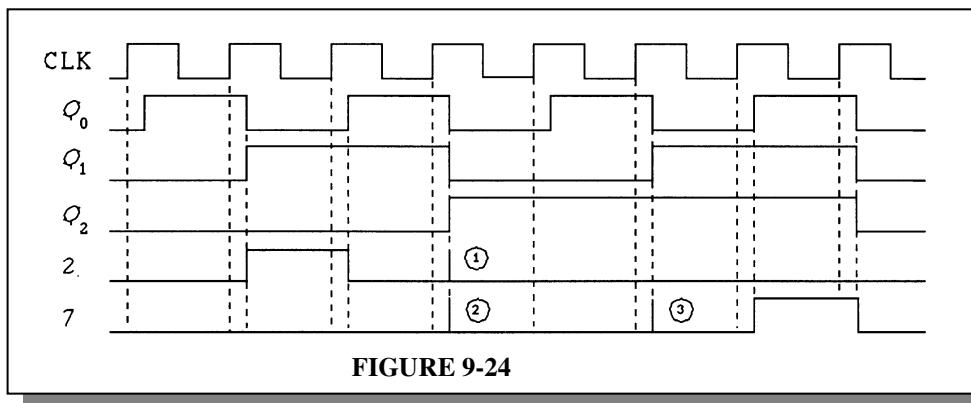


FIGURE 9-24

### Section 9-8 Counter Applications

33. For the digital clock in Figure 9-48 of the text reset to 12:00:00, the binary state of each counter after 62 60-Hz pulses are:

Hours, tens: **0001**

Hours, units: **0010**

Minutes, tens: **0000**

Minutes, units: **0001**

Seconds, tens: **0000**

Seconds, units: **0010**

34. For the digital clock, the counter output frequencies are:

**Divide-by-60 input counter:**

$$\frac{60 \text{ Hz}}{60} = 1 \text{ Hz}$$

**Seconds counter:**

$$\frac{1 \text{ Hz}}{60} = 16.7 \text{ mHz}$$

**Minutes counter:**

$$\frac{16.7 \text{ mHz}}{60} = 278 \mu\text{Hz}$$

**Hours counter:**

$$\frac{278 \mu\text{Hz}}{12} = 23.1 \mu\text{Hz}$$

35.  $53 + 37 - 26 = \mathbf{64}$

36. See Figure 9-25.

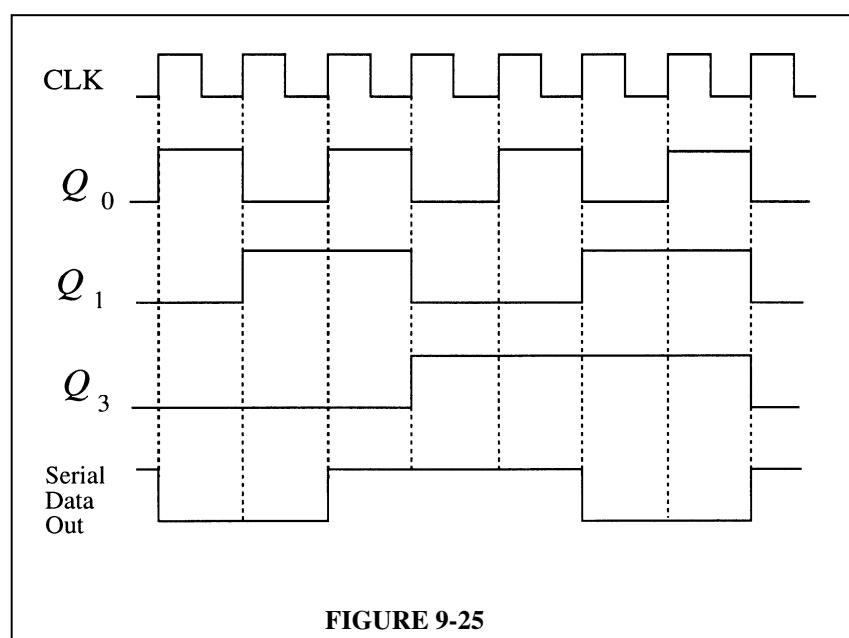
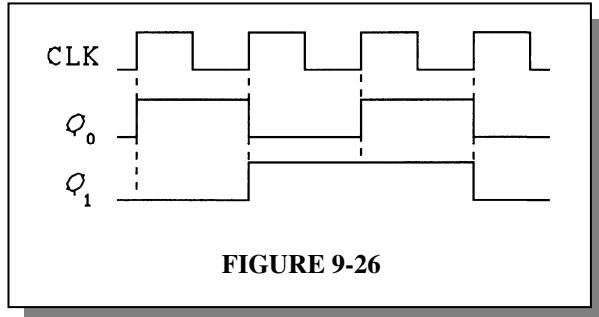


FIGURE 9-25

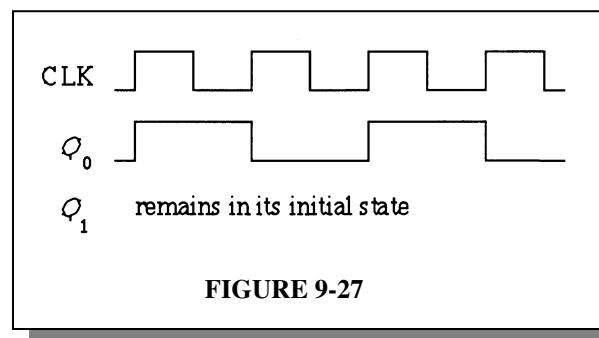
## Chapter 9

### Section 9-10 Troubleshooting

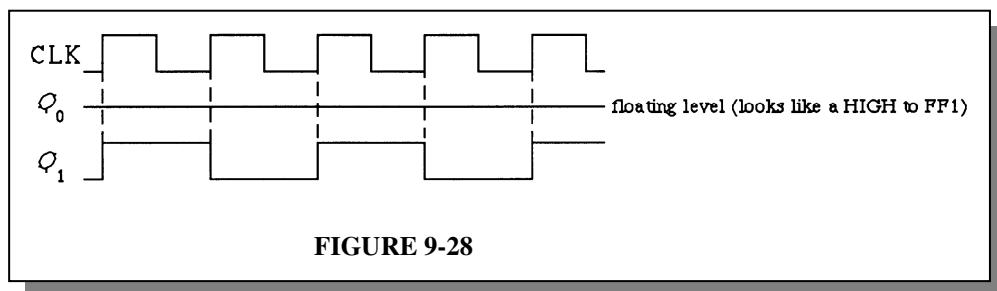
37. (a)  $Q_0$  and  $Q_1$  will not change due to the clock shorted to ground at FF0.
- (b)  $Q_0$  being open does not affect normal operation. See Figure 9-26.



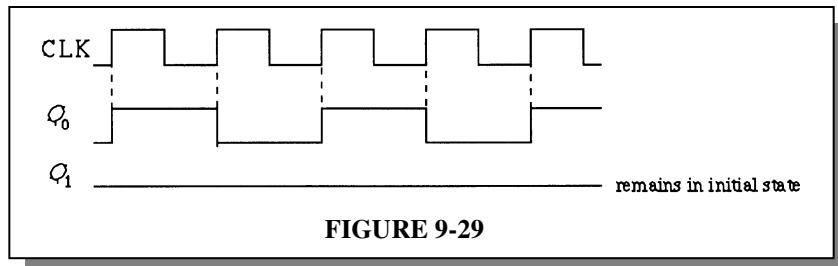
- (c) See Figure 9-27.



- (d)  $Q_0$  goes HIGH and remains HIGH.  $Q_1$  does not change.
- (e)  $Q_0$  toggles and  $Q_1$  stays LOW.
38. (a)  $Q_0$  and  $Q_1$  will not change from initial states.
- (b) See Figure 9-28.

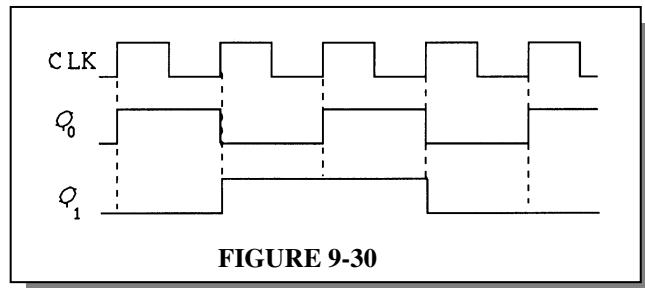


- (c) See Figure 9-29.



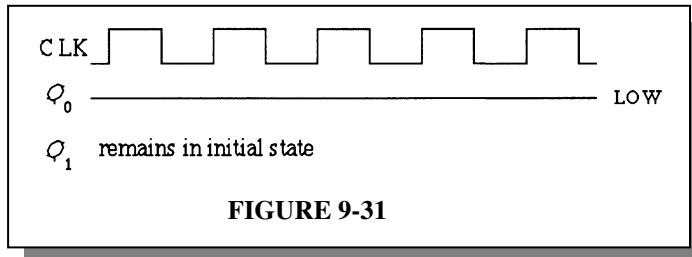
**FIGURE 9-29**

- (d) Normal operation. See Figure 9-30.



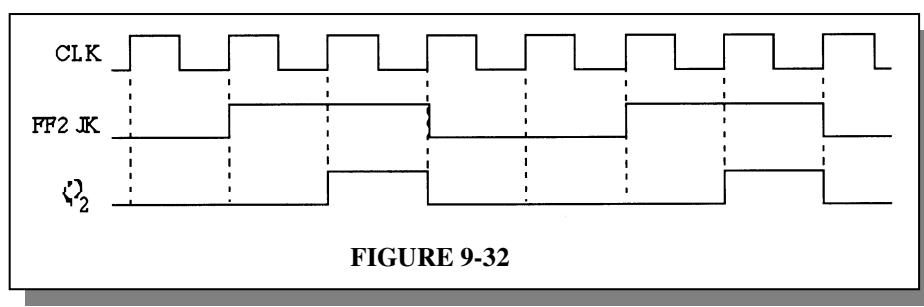
**FIGURE 9-30**

- (e) Both  $J$  and  $K$  of FF1 are pulled LOW if  $K$  is grounded, producing a no-change condition.  $Q_0$  also grounded. See Figure 9-31.



**FIGURE 9-31**

39. The  $D_1$  input is open, acting as a HIGH.
40. Since  $Q_2$  toggles on each clock pulse, its  $J$  and  $K$  inputs must be constantly HIGH. The most probable fault is that the AND gate's output is *open*.
41. If the  $Q_0$  input to the AND gate is *open*, the  $JK$  inputs to FF2 are as shown in Figure 9-32.



**FIGURE 9-32**

## **Chapter 9**

**42.** Number of states = 40,000

$$f_{out} = \frac{5 \text{ MHz}}{40,000} = 125 \text{ Hz}$$

76.2939 Hz is not correct. The faulty division factor is

$$\frac{5 \text{ MHz}}{76.2939 \text{ Hz}} = 65,536$$

Obviously, the counter is going through all of its states. This means that the 63C0<sub>16</sub> on its parallel inputs is not being loaded. Possible faults are:

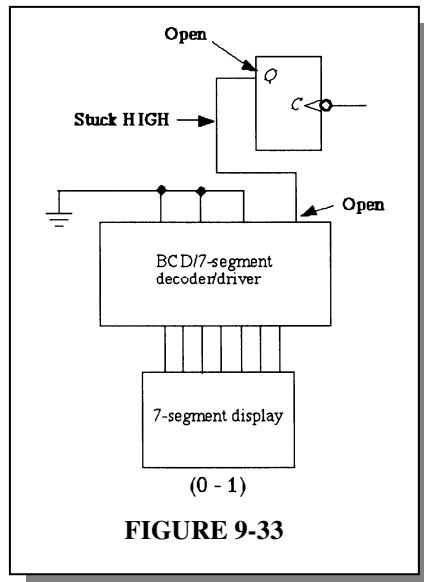
- Inverter output is stuck HIGH or open.
- RCO output of last counter is stuck LOW.

**43.**

| Stage | Open | Loaded Count | $f_{out}$  |
|-------|------|--------------|------------|
| 1     | 0    | 63C1         | 250.006 Hz |
| 1     | 1    | 63C2         | 250.012 Hz |
| 1     | 2    | 63C4         | 250.025 Hz |
| 1     | 3    | 63C8         | 250.050 Hz |
| 2     | 0    | 63D0         | 250.100 Hz |
| 2     | 1    | 63E0         | 250.200 Hz |
| 2     | 2    | 63C0         | 250 Hz     |
| 2     | 3    | 63C0         | 250 Hz     |
| 3     | 0    | 63C0         | 250 Hz     |
| 3     | 1    | 63C0         | 250 Hz     |
| 3     | 2    | 67C0         | 256.568 Hz |
| 3     | 3    | 6BC0         | 263.491 Hz |
| 4     | 0    | 73C0         | 278.520 Hz |
| 4     | 1    | 63C0         | 250 Hz     |
| 4     | 2    | 63C0         | 250 Hz     |
| 4     | 3    | E3C0         | 1.383 kHz  |

44. □ The flip-flop output is stuck HIGH or open.  
 □ The least significant BCD/7-segment input is open.

See Figure 9-33.



**FIGURE 9-33**

45. The DIV 6 is the tens of minutes counter.  $Q_1$  open causes a continuous apparent HIGH output to the decode 6 gate and to the BCD/7-segment decoder/driver.

The apparent counter sequence is shown in the table.

| Actual State of Ctr. | Apparent state |       |       |       |
|----------------------|----------------|-------|-------|-------|
|                      | $Q_3$          | $Q_2$ | $Q_1$ | $Q_0$ |
| 0                    | 0              | 0     | 1     | 0     |
| 1                    | 0              | 0     | 1     | 1     |
| 2                    | 0              | 0     | 1     | 0     |
| 3                    | 0              | 0     | 1     | 1     |
| 4                    | 0              | 1     | 1     | 0     |

The decode 6 gate interprets count 4 as a 6 (0110) and clears the counter back to 0 (actually 0010). Thus, the apparent (not actual) sequence is as shown in the table.

46. There are several possible causes of the malfunction. First check power to all units. Other possible faults are listed below.

- Sensor Latch
  - Action:* Disconnect entrance sensor and pulse sensor input.
  - Observation:* Latch should SET.
  - Conclusion:* If latch does not SET, replace it.
- NOR gate
  - Action:* Pulse sensor input.
  - Observation:* Pulse on gate output.
  - Conclusion:* If there is no pulse, replace gate.

## Chapter 9

- Counter
  - Action: Pulse sensor input.
  - Observation: Counter should advance.
  - Conclusion: If counter does not advance, replace it.
- Output Interface
  - Action: Pulse sensor input until terminal count is reached.
  - Observation: FULL indication and gate lowered
  - Conclusion: No FULL indication or if gate does not lower, replace interface.
- Sensor/Cable
  - Action: Try to activate sensor.
  - Observation: If all previous checks are OK, sensor or cable is faulty.
  - Conclusion: Replace sensor or cable.

### Applied Logic

47. The CALL logic is located on each floor. See Figure 9-34. The floor code is hardwired and is unique to each floor. The fifth floor logic is shown to illustrate.

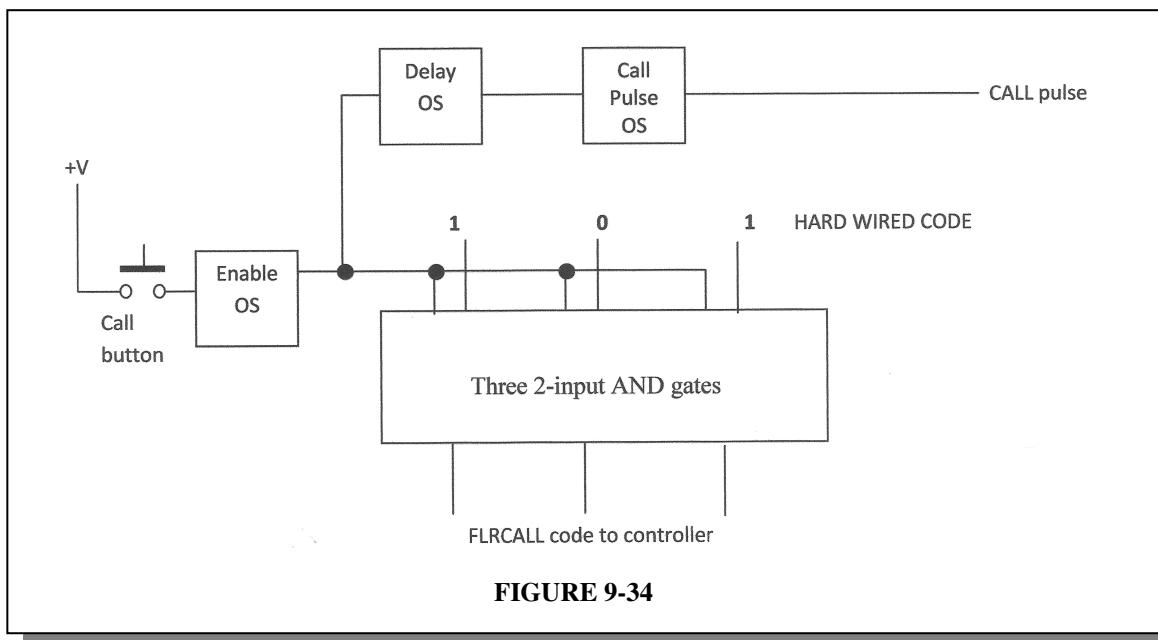
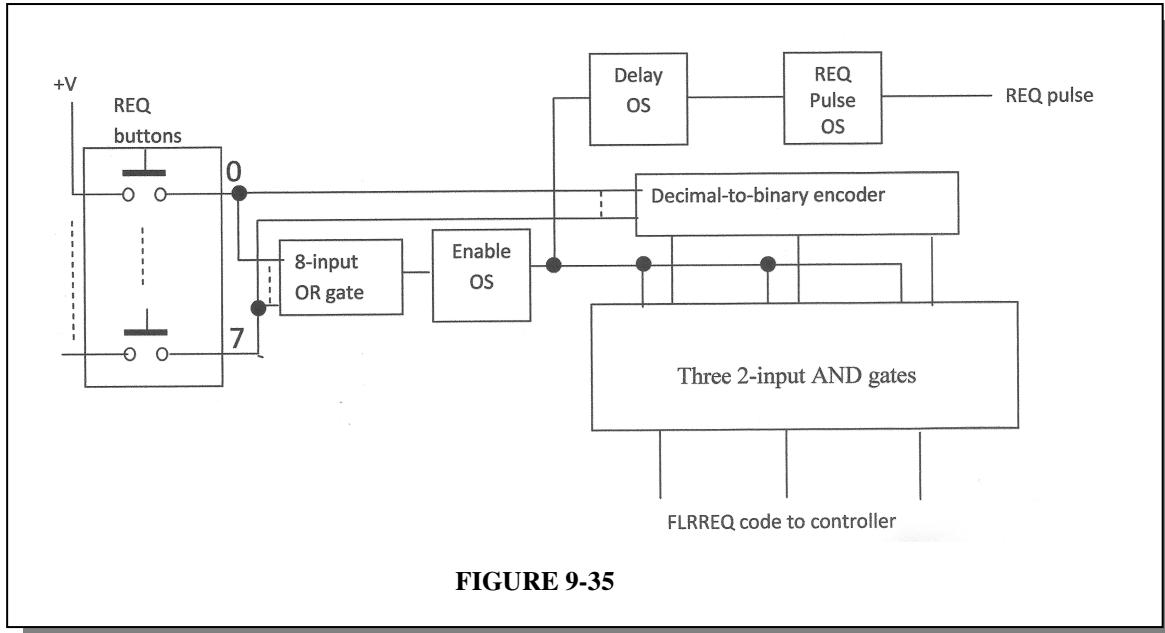


FIGURE 9-34

48. REQ logic located in the elevator. See Figure 9-35.

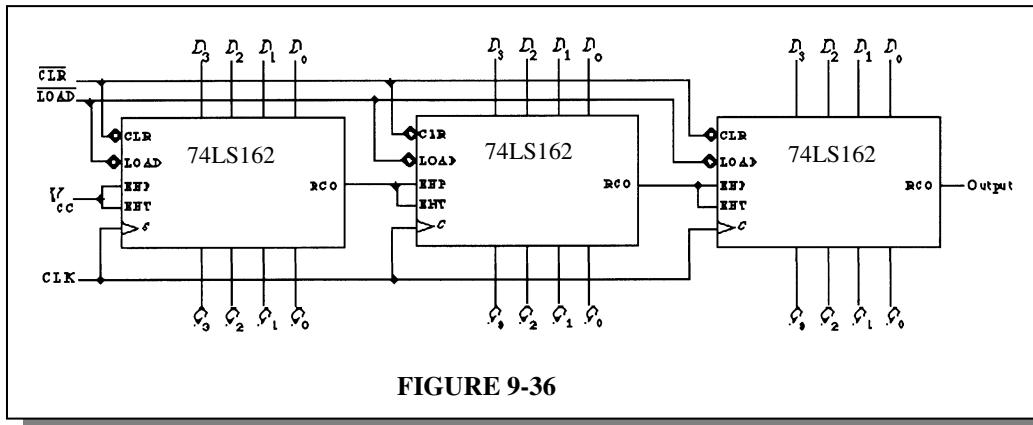


**FIGURE 9-35**

49. (a) Change floor counter to two bits. (b) Change the Call/Req Code Register and associated logic to two bits. (c) Modify the 7-segment decoder for a 2-bit code.

### **Special Design Problems**

50. See Figure 9-36.



**FIGURE 9-36**

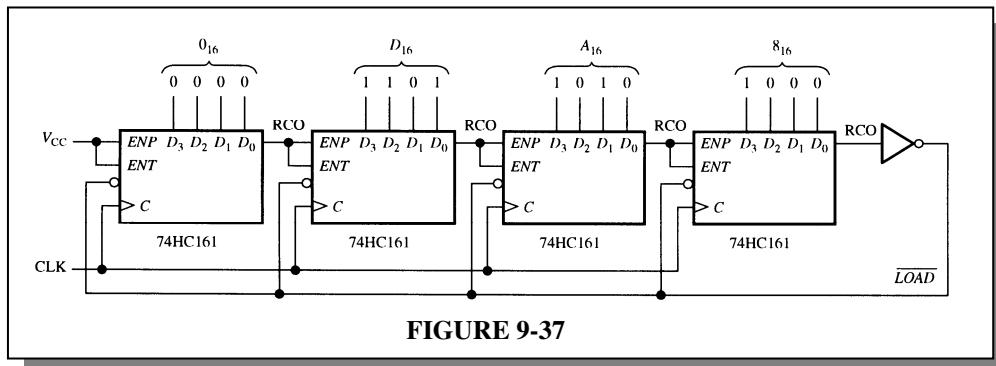
## Chapter 9

51.  $65,536 - 30,000 = 35,536$

Preset the counter to 35,536 so that it counts from 35,536 up to 65,536 on each full cycle, thus producing a sequence of 30,000 states (modulus 30,000).

$$35,536 = 1000101011010000_2 = \mathbf{8AD0}_{16}$$

See Figure 9-37.



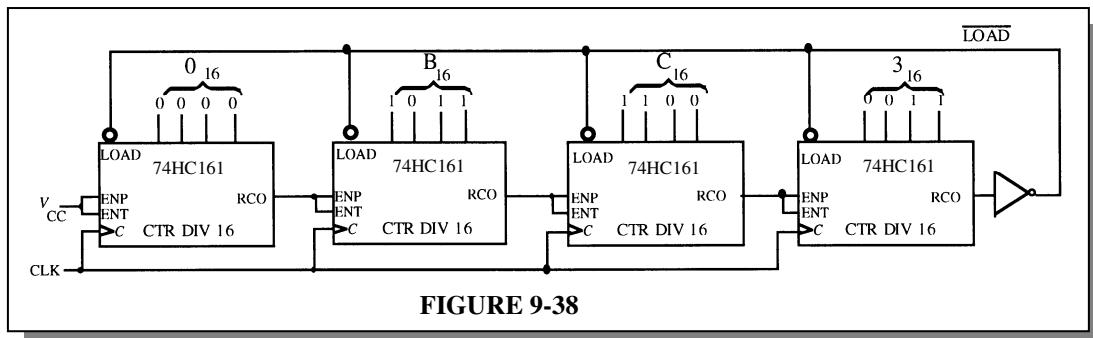
**FIGURE 9-37**

52.  $65,536 - 50,000 = 15,536$

Preset the counter to 15,536 so that it counts from 15,536 up to 65,536 on each full cycle, thus producing a sequence of 50,000 states (modulus 50,000).

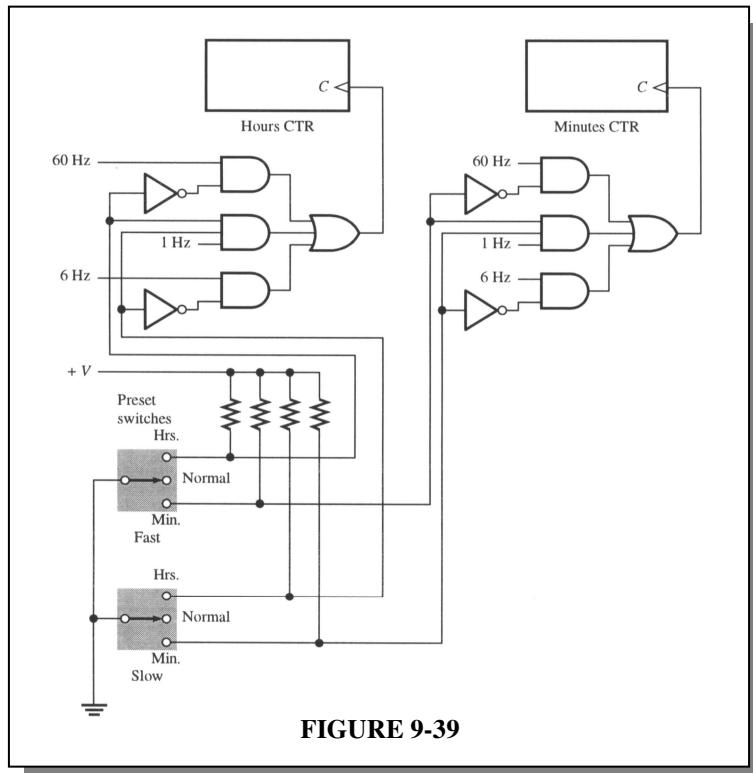
$$15,536 = 11110010110000_2 = \mathbf{3CB0}_{16}$$

See Figure 9-38.



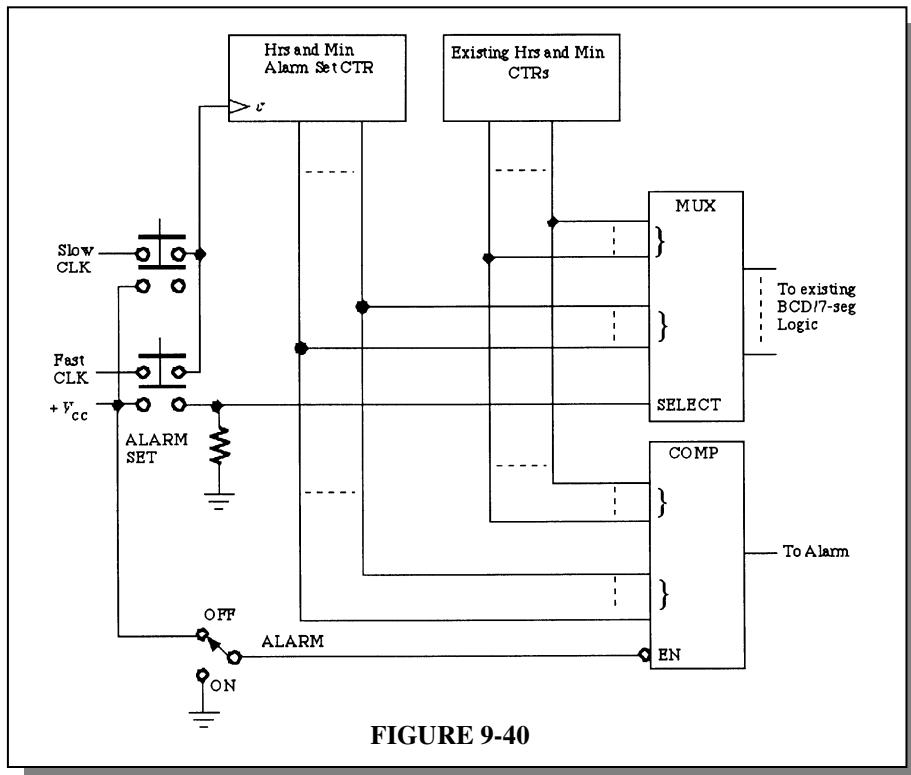
**FIGURE 9-38**

53. The approach is to preset the hours and minutes counters independently, each with a fast or slow preset mode. The seconds counter is not preset. One possible implementation is shown in Figure 9-39.



**FIGURE 9-39**

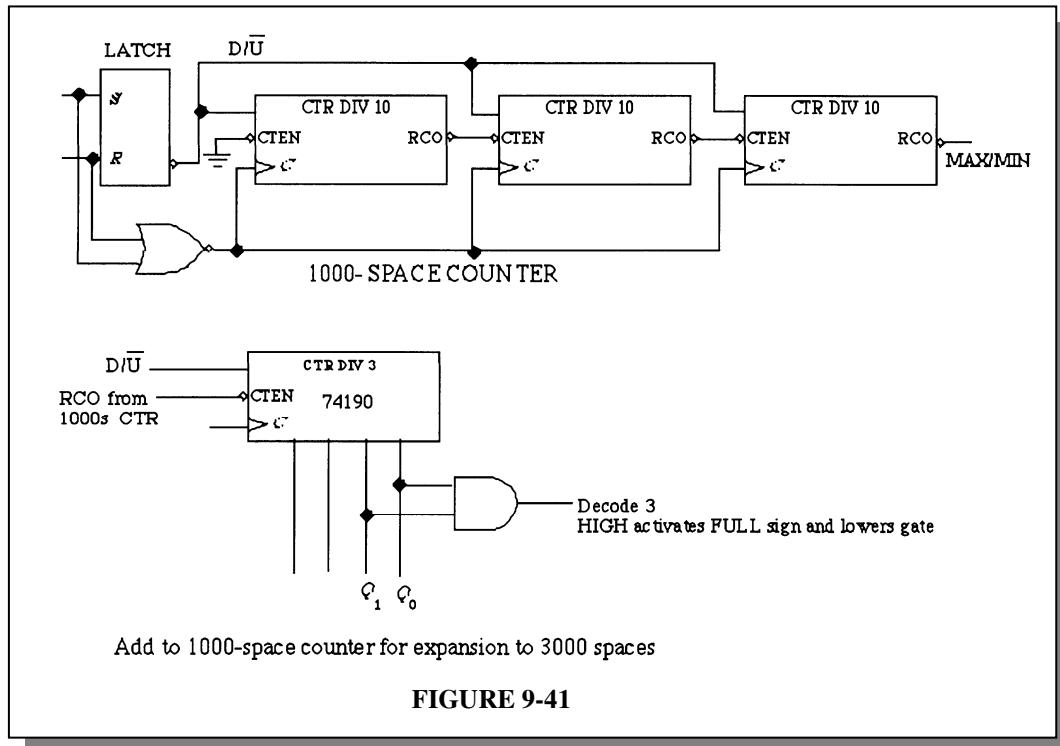
54. See Figure 9-40.



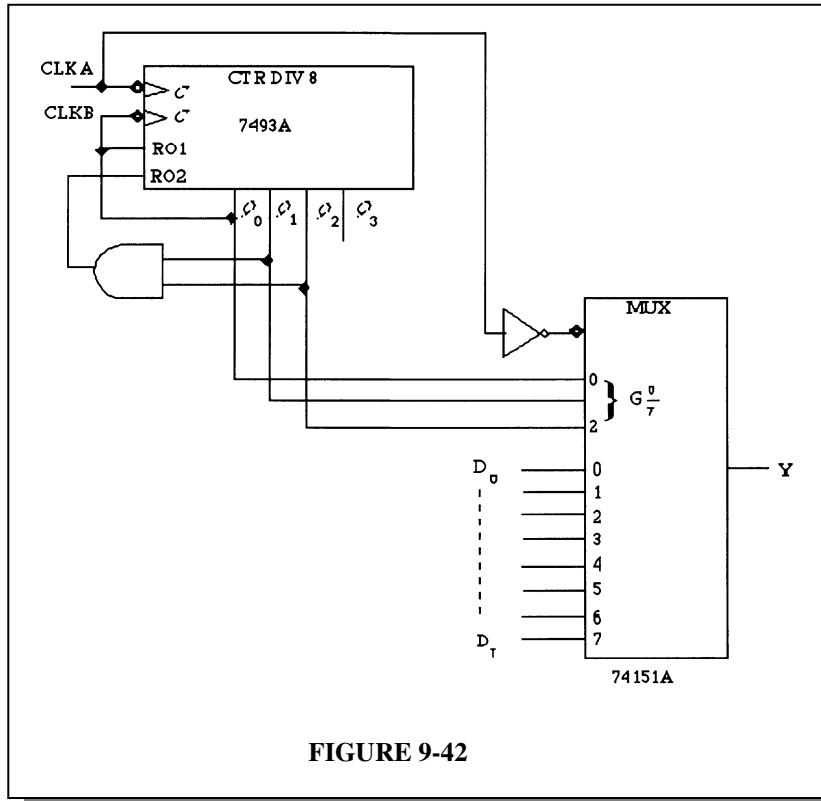
**FIGURE 9-40**

## Chapter 9

55. See Figure 9-41.



56. See Figure 9-42.



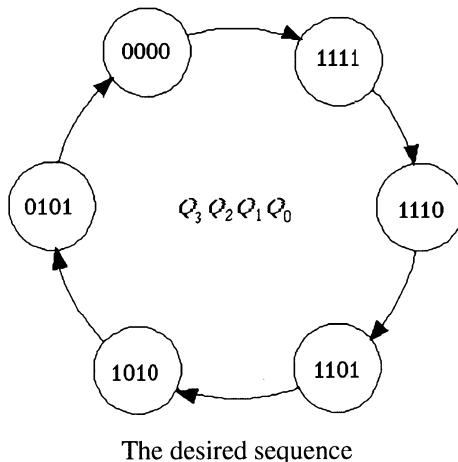
## 57. NEXT-STATE TABLE

| Present State |       |       |       | Next State |       |       |       |
|---------------|-------|-------|-------|------------|-------|-------|-------|
| $Q_3$         | $Q_2$ | $Q_1$ | $Q_0$ | $Q_3$      | $Q_2$ | $Q_1$ | $Q_0$ |
| 0             | 0     | 0     | 0     | 1          | 1     | 1     | 1     |
| 1             | 1     | 1     | 1     | 1          | 1     | 1     | 0     |
| 1             | 1     | 1     | 0     | 1          | 1     | 0     | 1     |
| 1             | 1     | 0     | 1     | 1          | 0     | 1     | 0     |
| 1             | 0     | 1     | 0     | 0          | 1     | 0     | 1     |
| 0             | 1     | 0     | 1     | 0          | 0     | 0     | 0     |

## TRANSITION TABLE

| Output State Transitions |        |        |        | Flip-flop Inputs |          |          |          |
|--------------------------|--------|--------|--------|------------------|----------|----------|----------|
| $Q_3$                    | $Q_2$  | $Q_1$  | $Q_0$  | $J_3K_3$         | $J_2K_2$ | $J_1K_1$ | $J_0K_0$ |
| 0 to 1                   | 0 to 1 | 0 to 1 | 0 to 1 | 1X               | 1X       | 1X       | 1X       |
| 1 to 1                   | 1 to 1 | 1 to 1 | 1 to 0 | X0               | X0       | X0       | X1       |
| 1 to 1                   | 1 to 1 | 1 to 0 | 0 to 1 | X0               | X0       | X1       | 1X       |
| 1 to 1                   | 1 to 0 | 0 to 1 | 1 to 0 | X0               | X1       | 1X       | X1       |
| 1 to 0                   | 0 to 1 | 1 to 0 | 0 to 1 | X1               | 1X       | X1       | 1X       |
| 0 to 0                   | 1 to 0 | 0 to 0 | 1 to 0 | 0X               | X1       | 0X       | X1       |

See Figure 9-43.



## Chapter 9

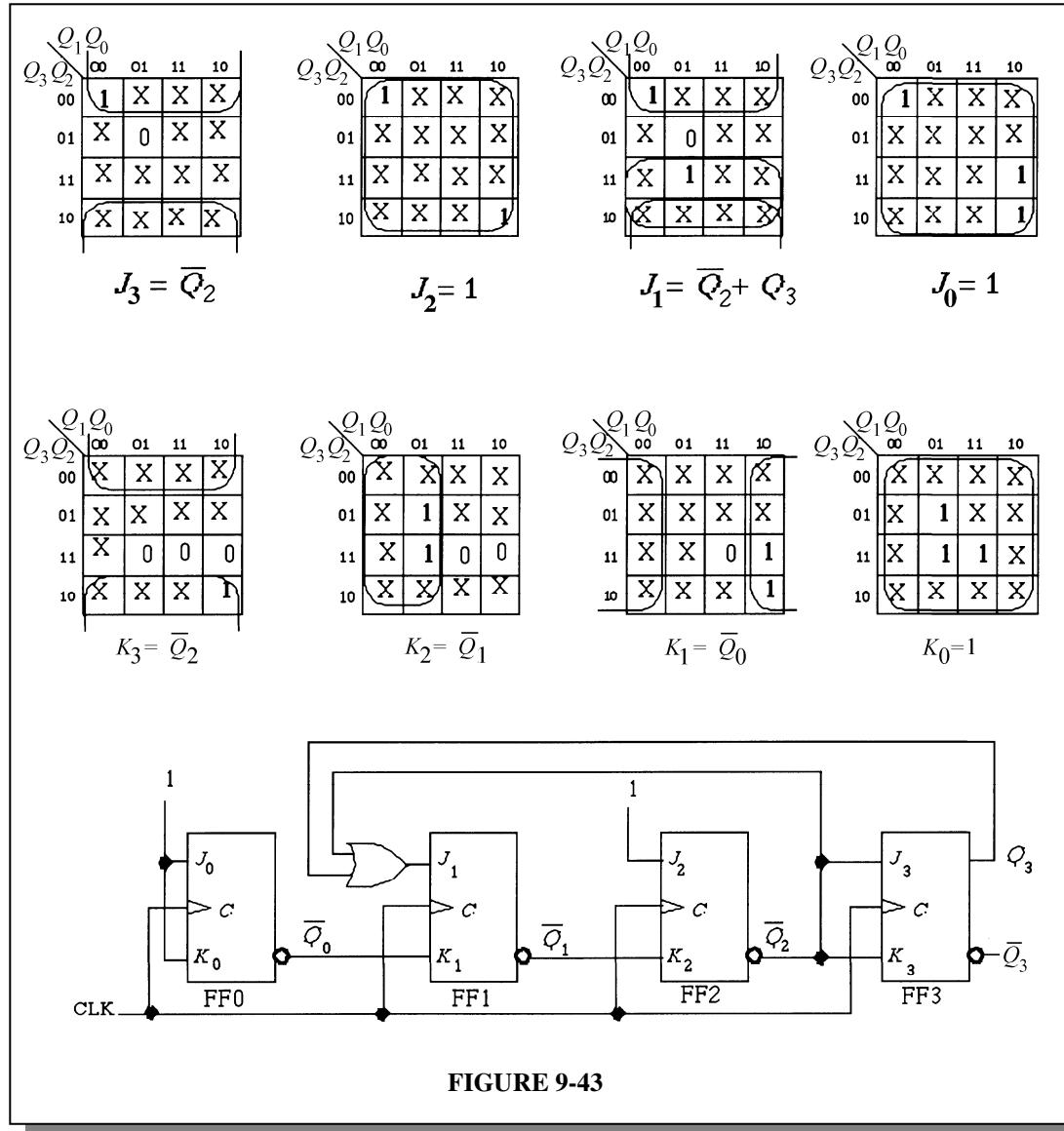


FIGURE 9-43

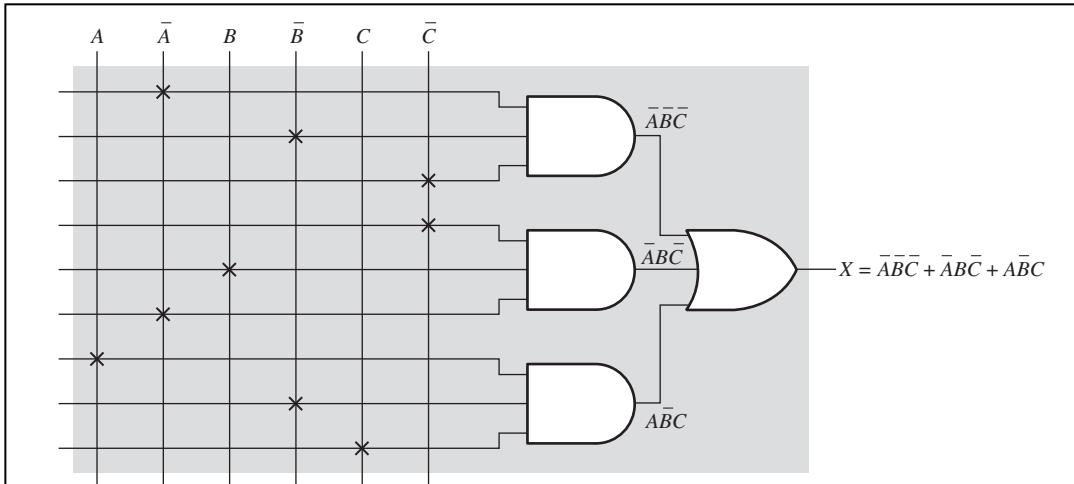
58. The line to the CLK input of U3 is open.
59. The input of the U5 AND gate that connects to the Q output of U2 shorted to VCC.
60. Q output of U3 is shorted to ground.
61. Line to LOAD' input always LOW.
62. Line to U'/D input of counter always HIGH.

## CHAPTER 10

### PROGRAMMABLE LOGIC

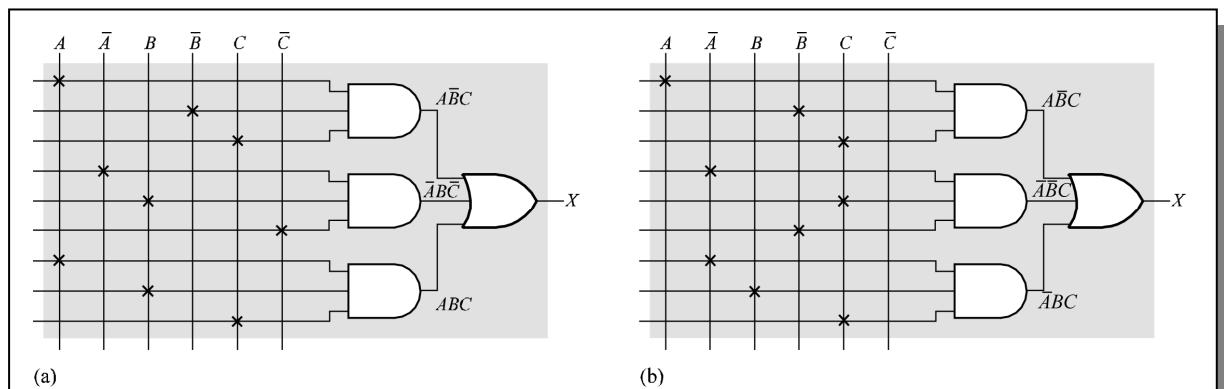
#### Section 10-1 Simple Programmable Logic Devices (SPLDs)

1.  $X = \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}\bar{C} + A\overline{B}\bar{C}$ . See Figure 10-1.



**FIGURE 10-1**

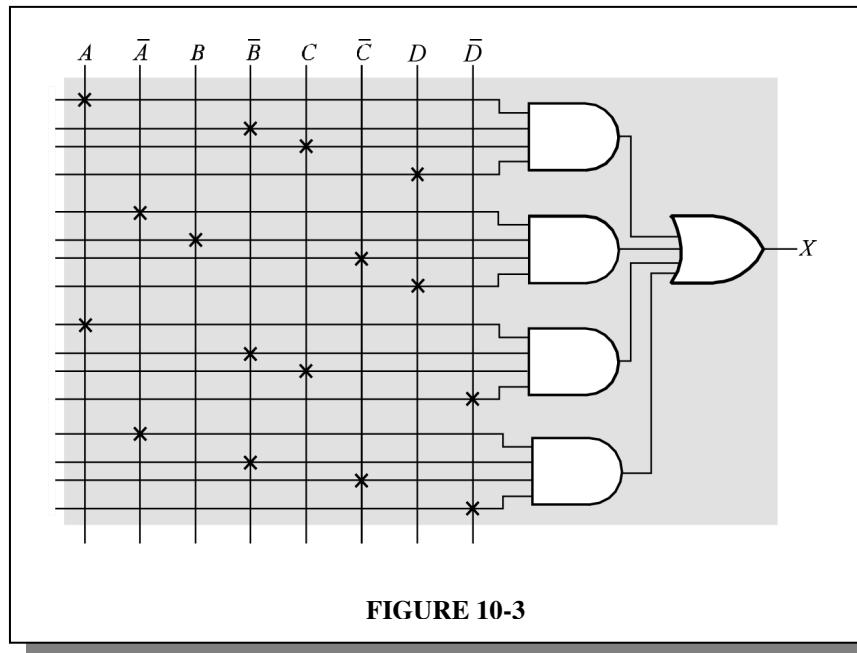
2. See Figure 10-2.



**FIGURE 10-2**

## Chapter 10

3. See Figure 10-3.

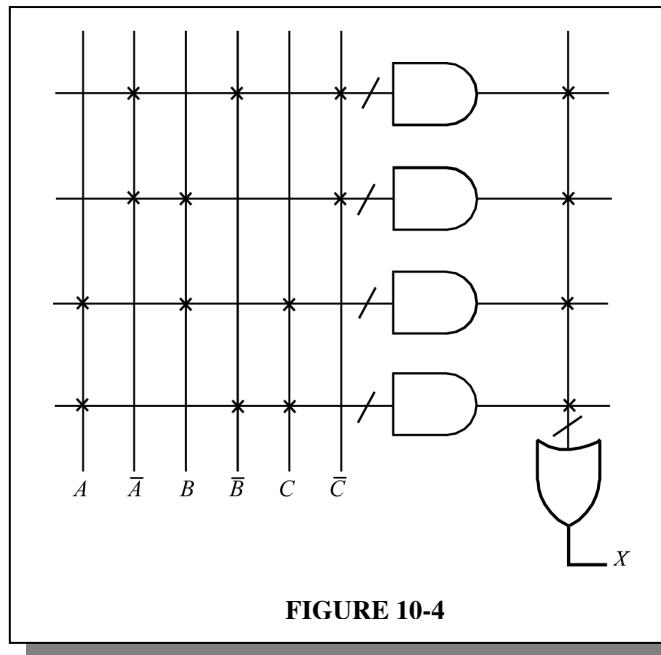


4. Typically, an exclusive-OR gate is used to determine the polarity of the output. When a 1 is applied to one input of the XOR gate, the output of the XOR is the complement of the signal on the other input. When a 0 is applied to one input of the XOR, the signal on the output of the XOR is the same as the signal on the other input.

### Section 10-2 Complex Programmable Logic Devices (CPLDs)

5. A CPLD basically consists of multiple SPLDs that can be connected with a programmable interconnect array.
6. (a) Inputs from PIA to LAB: **36**      (b) Outputs from LAB to PIA: **16**  
(c) Inputs from I/O to PIA: **8 to 16**      (d) Outputs from LAB to I/O: **8 to 16**
7. (a)  $\overline{ABC}\overline{D}$       (b)  $ABC(\overline{D}\overline{E}) = ABC(\overline{D} + \overline{E}) = ABC\overline{D} + ABC\overline{E}$
8.  $A\overline{B}\overline{C}\overline{D} + EFGH + AB\overline{C}D + \overline{A}B\overline{C}D$
9.  $A\overline{B} + \overline{A}B$

10. See Figure 10-4.



**FIGURE 10-4**

$$11. \quad X_1 = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}BCD + ABC\bar{D}; \quad X_2 = ABCD + AB\bar{C}D + \bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}CD$$

### Section 10-3 Macrocell Modes

12. (a) A 0 on the select line selects  $D_0$ . The output is **1**.  
 (b) A 1 on the select line selects  $D_1$ . The output is **0**.
13. (a) Since the  $D_0$  (upper) input of MUX 5 is selected, the macrocell is configured for **combinational** logic. The output of the XOR goes through MUX 5 to the “To I/O” output making it a **1**.  
 (b) Since the  $D_1$  (lower) input of MUX 5 is selected, the macrocell is configured for **registered** logic. The output of the flip-flop goes through MUX 5 to the “To I/O” output making it a **0**.
14. (a) The macrocell is configured for **registered** logic because the  $D_1$  input of MUX 8 is selected, allowing the flip-flop output to pass through.  
 (b) The **GCK1** clock is applied to the flip-flop because the  $D_1$  input of MUX 3 and the  $D_1$  input of MUX 5 are selected.  
 (c) The OR gate output is applied to the XOR which is set for noninversion by MUX 1. The output of the XOR is selected by MUX2 and a **1** is applied to the D/T input of the flip-flop.  
 (d) The output of MUX 8 is a **1** because MUX 8 selects the Q output of the flip-flop (assuming that the S and R inputs are 0).

## Chapter 10

15. (a) The macrocell is configured for **registered** logic because the  $D_1$  input of MUX 8 is selected, allowing the flip-flop output to pass through.
- (b) The **GCK1** clock is applied to the flip-flop because the  $D_1$  input of MUX 3 and the  $D_1$  input of MUX 5 are selected.
- (c) The OR gate output is applied to the XOR which is set for inversion by MUX 1. The output of the XOR is selected by MUX 2 and a **0** is applied to the D/T input of the flip-flop.
- (d) The output of MUX 8 is a **0** because MUX 8 selects the Q output of the flip-flop (assuming that the S and R inputs are 0).

### Section 10-4 Field-Programmable Gate Arrays (FPGAs)

16. An FPGA typically consists of configurable logic blocks (CLBs). Each CLB is made up of a number of logic modules with a local interconnect. Each logic module typically consists of a look-up table (LUT) and associated logic. Global column and row interconnects are used to connect the CLBs to I/Os as well as each other.
17. SOP output =  $\overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}C + \overline{A}BC + A\overline{B}C + ABC$
18. See Figure 10-5.

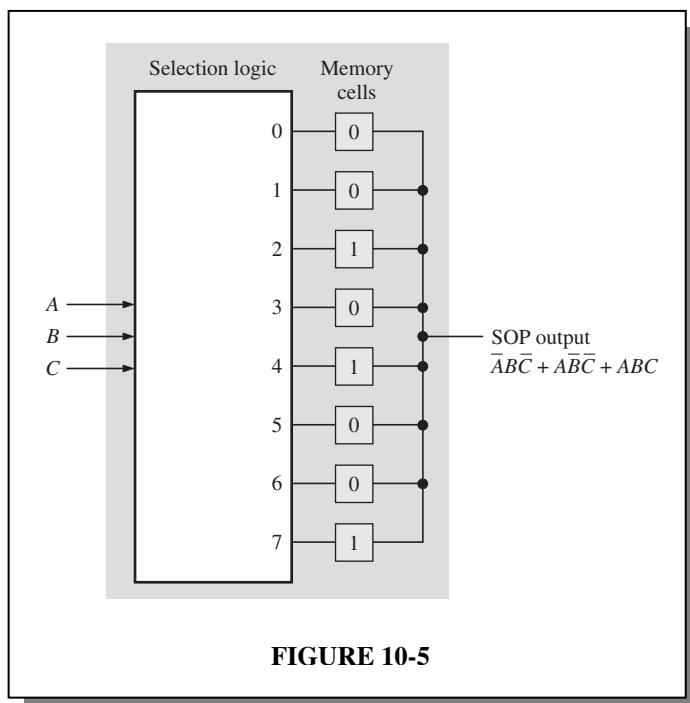
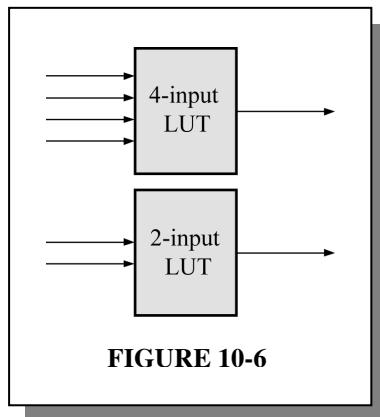


FIGURE 10-5

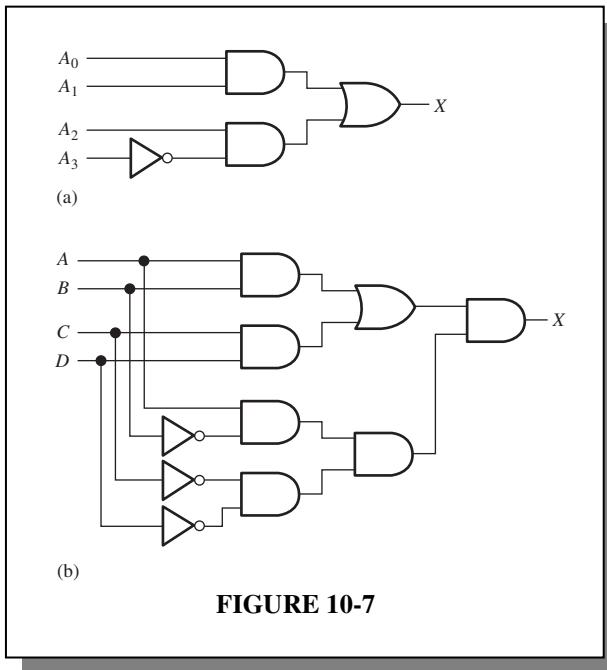
- 19.** See Figure 10-6.



$$\begin{aligned} \mathbf{20.} \quad & (A_4 A_3 \bar{A}_2 A_1 + \bar{A}_4 \bar{A}_3 \bar{A}_2 A_1) A_0 + (\bar{A}_5 A_3 A_2 A_1 + A_5 \bar{A}_3 A_2 \bar{A}_1 + A_5 A_3 A_2 \bar{A}_1) A_0 \\ & = A_4 A_3 \bar{A}_2 A_1 A_0 + \bar{A}_4 \bar{A}_3 \bar{A}_2 A_1 A_0 + \bar{A}_5 A_3 A_2 A_1 \bar{A}_0 + A_5 \bar{A}_3 A_2 \bar{A}_1 \bar{A}_0 + A_5 A_3 A_2 \bar{A}_1 \bar{A}_0 \end{aligned}$$

### **Section 10-5 Programmable Logic Software**

- 21.** See Figure 10-7.



## Chapter 10

22. 
$$\begin{aligned} X &= \overline{ABCD} + A\overline{BCD} + A\overline{B}\overline{C}D + ABC\overline{D} + ABCD + \overline{A}\overline{B}\overline{C}\overline{D} \\ &= ABD + ACD + ABC + BCD + \overline{ABC}\overline{D} \end{aligned}$$

See Figure 10-8.

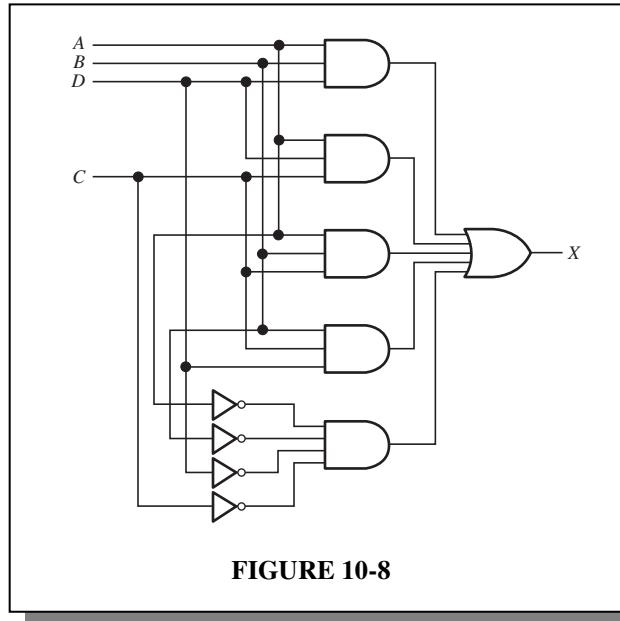


FIGURE 10-8

23. See Figure 10-9.

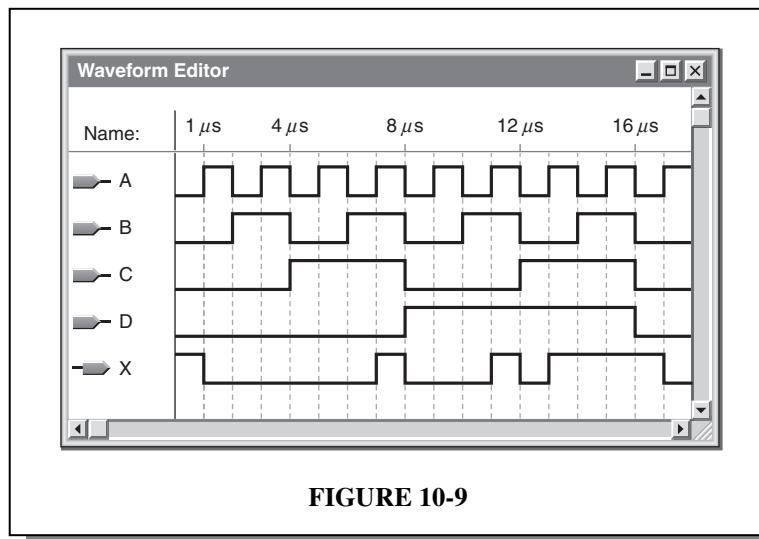
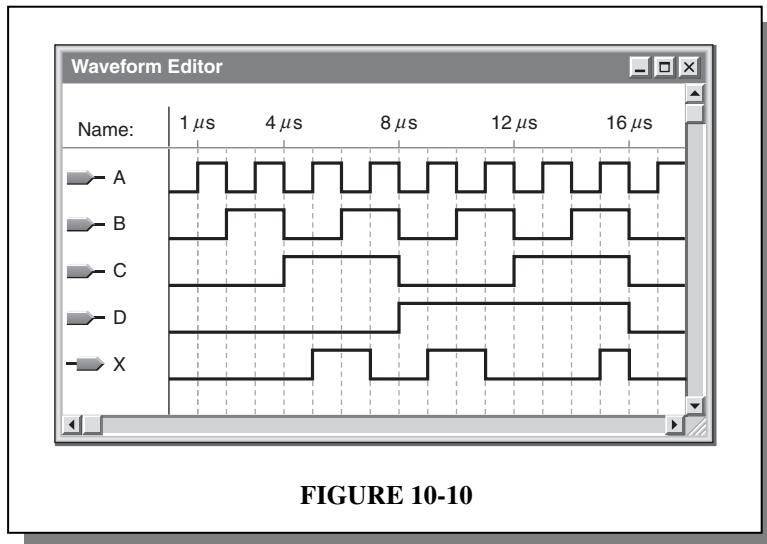


FIGURE 10-9

24.  $X = \overline{ABCD} + AB\overline{CD} + ABCD + A\overline{BCD} + \overline{ABC}D$ . See Figure 10-10.



### **Section 10-6 Boundary Scan Logic**

25. The Shift input = 1, data are applied to SDI, go through the MUX, and are clocked into Capture register A on the leading edge of the clock pulse. From the output of Capture register A, the data go through the upper MUX and are clocked into Capture register B on the trailing edge of the clock pulse.
26. PDI/O = 0 and OE = 1. The data from the internal programmable logic pass through the selected MUX and through the output buffer to the pin.
27. PDI/O = 0 and OE = 0. The data are applied to the input pin and go through the selected MUX to the internal programmable logic.
28. SHIFT = 1, PDI/O = 1, and OE = 0. Data are applied to SDI, go through the MUX, and are clocked into Capture register A on the leading edge of the clock pulse. From the output of Capture register A, the data go through the upper MUX and are clocked into Capture register B on the trailing edge of the clock pulse. A pulse on the UPDATE input clocks the data into Update register B. The data on the output of Capture Register B go through the MUX to the internal programmable logic. The data also appear on the SDO.

## **Chapter 10**

### **Section 10-7 Troubleshooting**

- 29.** 000011001010001111011 shifted from TDI to TDO, left-most bit first. The bold-faced code will appear on the logic inputs in the sequence shown.

|    |                                          |
|----|------------------------------------------|
| 0  | <b>0000</b> 11001010001111011            |
| 1  | <b>0000</b> 11001010001111011            |
| 3  | <b>0000</b> 11001010001111011            |
| 6  | <b>0000</b> 11001010001111011            |
| 12 | <b>0000</b> 1100 <b>10</b> 10001111011   |
| 9  | <b>0000</b> 1100 <b>10</b> 10001111011   |
| 2  | <b>0000</b> 1100 <b>10</b> 10001111011   |
| 5  | <b>0000</b> 1100 <b>10</b> 10001111011   |
| 10 | <b>0000</b> 1100 <b>10</b> 10001111011   |
| 4  | <b>0000</b> 1100 <b>10</b> 10001111011   |
| 8  | <b>0000</b> 110010 <b>1000</b> 1111011   |
| 1  | <b>0000</b> 1100101 <b>0001</b> 1111011  |
| 3  | <b>0000</b> 11001010 <b>0001</b> 1111011 |
| 7  | <b>0000</b> 1100101000 <b>1111</b> 011   |
| 15 | <b>0000</b> 1100101000 <b>1111</b> 011   |
| 14 | <b>0000</b> 1100101000 <b>1111</b> 011   |
| 13 | <b>0000</b> 1100101000 <b>1111</b> 011   |
| 11 | <b>0000</b> 1100101000 <b>1111</b> 011   |

- 30.**
1. Change the code register from three bits to Four bits
  2. Change the floor counter to count from 0 through 15 instead of 0 through 7.
  3. Change the comparator to accept four bit numbers.
  4. Change the decoder to four bits.
  5. Add a second decoder for the t.
  6. Add a second 7-segment display for the tens digit.
  7. Add another 7-segment decoder for the tens digit of the floor count.
  8. Add a four-bit binary to BCD converter to provide the two-digit BCD input to the 7-segment decoders.
- 31.** The AND-OR logic switches either the Call code from the floor panel or the Request code from the elevator panel and the associated clock into the register based on the state of the flip-flop.

32. Seven segment. VHDL for floors 0–15.

```
library ieee;
use ieee.std_logic_1164.all;

entity SevenSegment is
 port(q, b, c, de, e, f, g: out std_logic;
 H0,H1,H2,H3: inout std_logic);
endentity SevenSegment;

architecture SevenSegmentBehavior of SevenSegment is
begin
 a <= H1 or H3 or (H2 and H0) or (not H2 and not);
 b <= not H2 or (not H0 and not H1) or (H0 and H1);
 c <= H0 or not H1 or H2;
 d <= H3 or (not H0 and not H2) or (not H2 and H1) or
 (H1) and not H0) or (H2 and not H1 and H0);
 e <= (not H0 and not H2) or (H1 and not H0);
 f <= (not H1 and H2) or (not H1 and not H0) or (H2 and not H0) or H3;
 g <= (not H2 and H1) or (H1 and not H0) or (H2 and not H1) or H3;
end architecture
```

---

# CHAPTER 11

## DATA STORAGE

---

### Section 11-1 Semiconductor Memory Basics

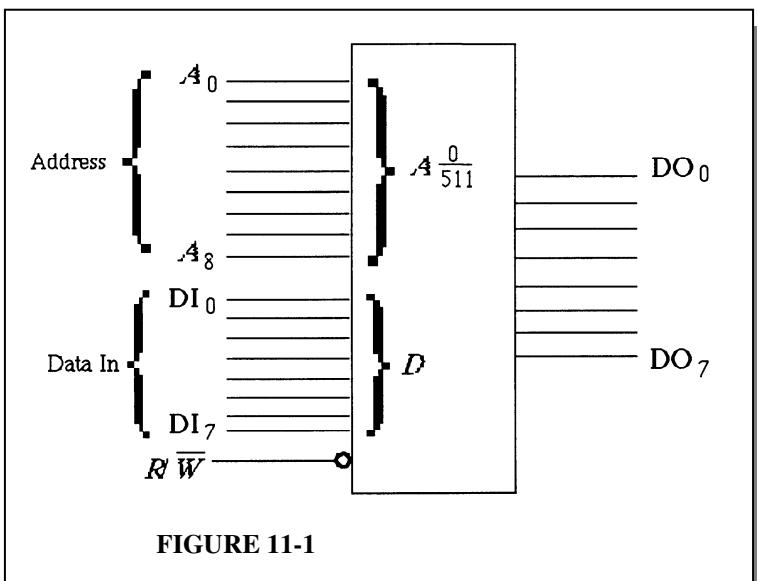
1. (a) ROM: no read/write control  
(b) RAM
2. They are random access memories because any address can be accessed at any time. You do not have to go through all the preceding addresses to get to a specific address.
3. **Address bus** provides for transfer of address code to memory for accessing any memory location in any order for a read or a write operation.  
**Data bus** provides for transfer of data between the microprocessor and memory or input/output devices.
4. (a)  $0A_{16} = 00001010_2 = 10_{10}$   
(b)  $3F_{16} = 00111111_2 = 63_{10}$   
(c)  $CD_{16} = 11001101_2 = 205_{10}$

### Section 11-2 Random-Access Memories (RAMs)

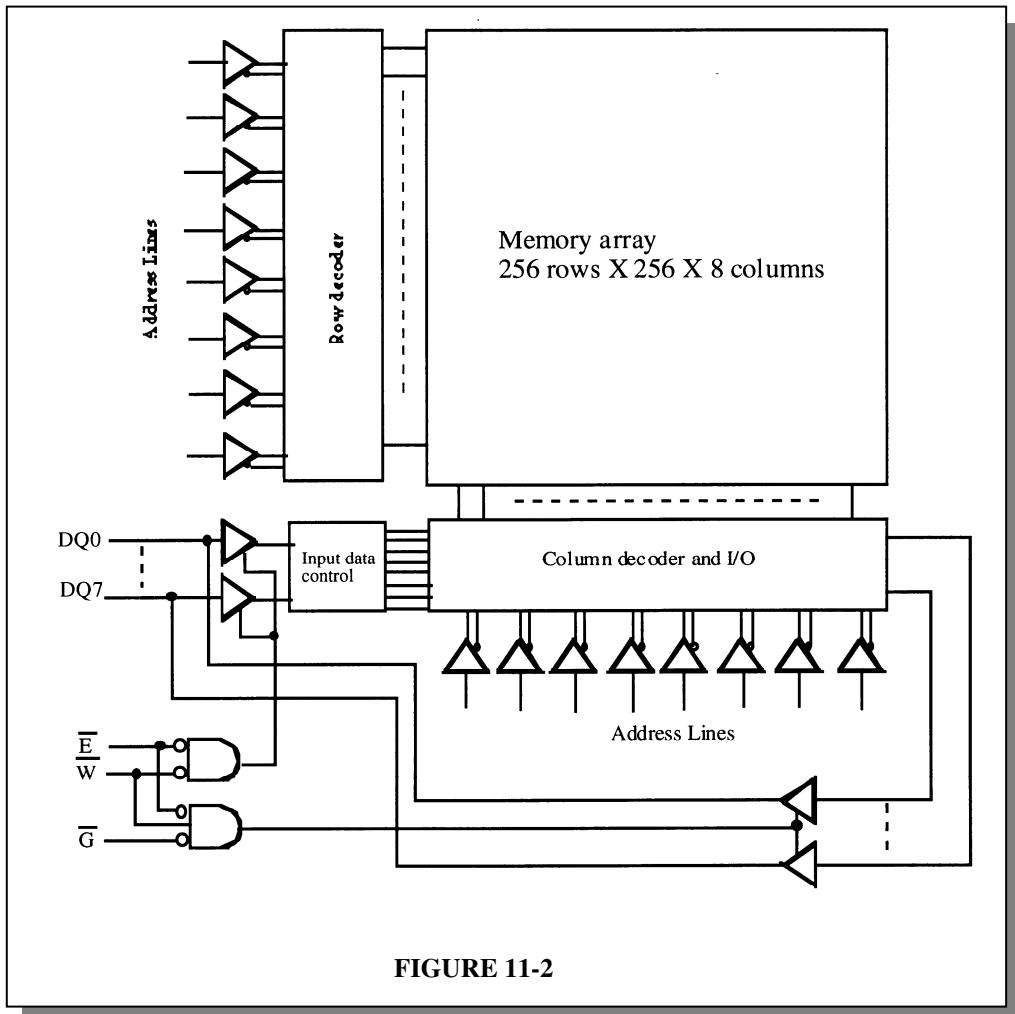
5.

|       | BIT 0 | BIT 1 | BIT 2 | BIT 3 |
|-------|-------|-------|-------|-------|
| ROW 0 | 1     | 0     | 0     | 0     |
| ROW 1 | 0     | 0     | 0     | 0     |
| ROW 2 | 0     | 0     | 1     | 0     |
| ROW 3 | 0     | 0     | 0     | 0     |

6. See Figure 11-1.



7.  $64k \times 8 = 512 \times 128 \times 8 = \mathbf{512 \text{ rows} \times 128 \text{ 8-bit columns}}$
8. See Figure 11-2.



**FIGURE 11-2**

## Chapter 11

9. The difference between SRAM and DRAM is that data in a SRAM are stored in latches or flip-flops indefinitely as long as power is applied while data in a DRAM are stored in capacitors which require periodic refreshing to retain the stored data.
10. The bit capacity of a DRAM with 12 address lines is

$$2^{2 \times 12} = 2^{24} = 16,777,216 \text{ bits} = 16 \text{ Mbits}$$

### Section 11-3 Read-Only Memories (ROMs)

11.

| Inputs |       | Outputs |       |       |       |
|--------|-------|---------|-------|-------|-------|
| $A_1$  | $A_0$ | $O_3$   | $O_2$ | $O_1$ | $O_0$ |
| 0      | 0     | 0       | 1     | 0     | 1     |
| 0      | 1     | 1       | 0     | 0     | 1     |
| 1      | 0     | 1       | 1     | 1     | 0     |
| 1      | 1     | 0       | 0     | 1     | 0     |

12.

| Inputs |       |       | Outputs |       |       |       |
|--------|-------|-------|---------|-------|-------|-------|
| $A_2$  | $A_1$ | $A_0$ | $O_3$   | $O_2$ | $O_1$ | $O_0$ |
| 0      | 0     | 0     | 0       | 1     | 0     | 0     |
| 0      | 0     | 1     | 1       | 1     | 1     | 1     |
| 0      | 1     | 0     | 1       | 0     | 1     | 1     |
| 0      | 1     | 1     | 1       | 0     | 0     | 1     |
| 1      | 0     | 0     | 1       | 1     | 1     | 0     |
| 1      | 0     | 1     | 1       | 0     | 0     | 0     |
| 1      | 1     | 0     | 0       | 0     | 1     | 1     |
| 1      | 1     | 1     | 0       | 1     | 0     | 1     |

13.

| BCD   |       |       |       | Excess-3 |       |       |       |
|-------|-------|-------|-------|----------|-------|-------|-------|
| $D_3$ | $D_2$ | $D_1$ | $D_0$ | $E_3$    | $E_2$ | $E_1$ | $E_0$ |
| 0     | 0     | 0     | 0     | 0        | 0     | 1     | 1     |
| 0     | 0     | 0     | 1     | 0        | 1     | 0     | 0     |
| 0     | 0     | 1     | 0     | 0        | 1     | 0     | 1     |
| 0     | 0     | 1     | 1     | 0        | 1     | 1     | 0     |
| 0     | 1     | 0     | 0     | 0        | 1     | 1     | 1     |
| 0     | 1     | 0     | 1     | 1        | 0     | 0     | 0     |
| 0     | 1     | 1     | 0     | 1        | 0     | 0     | 1     |
| 0     | 1     | 1     | 1     | 1        | 0     | 1     | 0     |
| 1     | 0     | 0     | 0     | 1        | 0     | 1     | 1     |
| 1     | 0     | 0     | 1     | 1        | 1     | 0     | 0     |

See Figure 11-3.

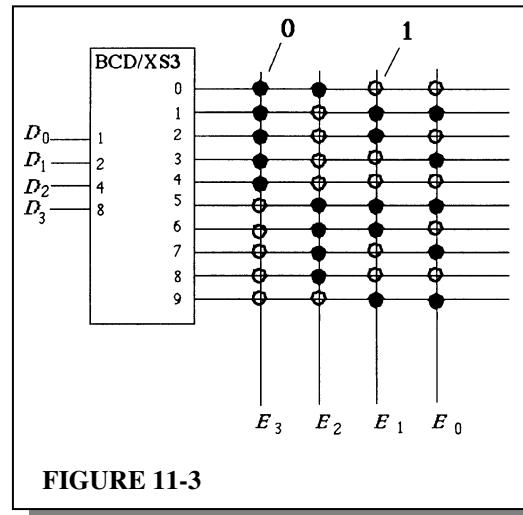


FIGURE 11-3

14.  $2^{14} = 16,384$  addresses  
 $16,384 \times 8 \text{ bits} = 131,072 \text{ bits}$

### **Section 11-4 Programmable ROMs (PROMs and EPROMs)**

**15.** Blown links: 1 – 17, 19 – 23, 25 – 31, 34, 37, 38, 40 – 47, 53, 55, 58, 61, 62, 63, 65, 67, 69.

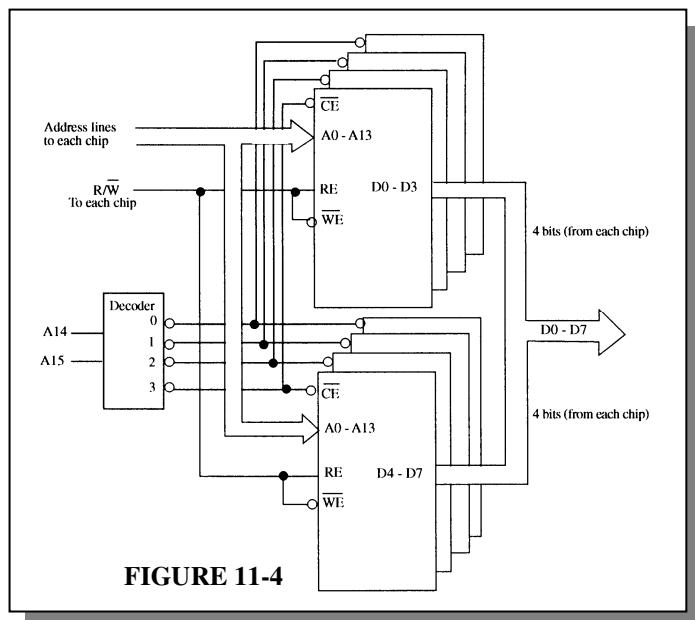
| <b>X Input</b> |       |       | $X^3$ | <b>X Output</b> |       |       |       |       |       |       |       |       |
|----------------|-------|-------|-------|-----------------|-------|-------|-------|-------|-------|-------|-------|-------|
| $X_2$          | $X_1$ | $X_0$ |       | $2^8$           | $2^7$ | $2^6$ | $2^5$ | $2^4$ | $2^3$ | $2^2$ | $2^1$ | $2^0$ |
| 0              | 0     | 0     | 0     | 0               | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| 1              | 0     | 0     | 1     | 0               | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 1     |
| 2              | 0     | 1     | 0     | 8               | 0     | 0     | 0     | 0     | 0     | 1     | 0     | 0     |
| 3              | 0     | 1     | 1     | 27              | 0     | 0     | 0     | 0     | 1     | 1     | 0     | 1     |
| 4              | 1     | 0     | 0     | 64              | 0     | 0     | 1     | 0     | 0     | 0     | 0     | 0     |
| 5              | 1     | 0     | 1     | 125             | 0     | 0     | 1     | 1     | 1     | 1     | 0     | 1     |
| 6              | 1     | 1     | 0     | 216             | 0     | 1     | 1     | 0     | 1     | 1     | 0     | 0     |
| 7              | 1     | 1     | 1     | 343             | 1     | 0     | 1     | 0     | 1     | 0     | 1     | 1     |

**16.**

| <b>Address</b>   | <b>Contents</b> |
|------------------|-----------------|
| $A_{13}-----A_0$ | $Q_7-----Q_0$   |
| 01001100010011   | 10101100        |
| 11011101011010   | 00100101        |
| 01011010011001   | 10110011        |
| 11010010001110   | 00101000        |
| 01010010100101   | 10001011        |
| 01010000110100   | 11010101        |
| 01001001100001   | 11001001        |
| 11011011100100   | 01001001        |
| 01101110001111   | 01010010        |
| 10111110011010   | 01001000        |
| 10101110011010   | 11001000        |

### **Section 11-6 Memory Expansion**

**17.** 16k × 4 DRAMS can be connected to make a 64k × 8 DRAM as shown in Figure 11-4.



**FIGURE 11-4**

## Chapter 11

18. See Figure 11-5.

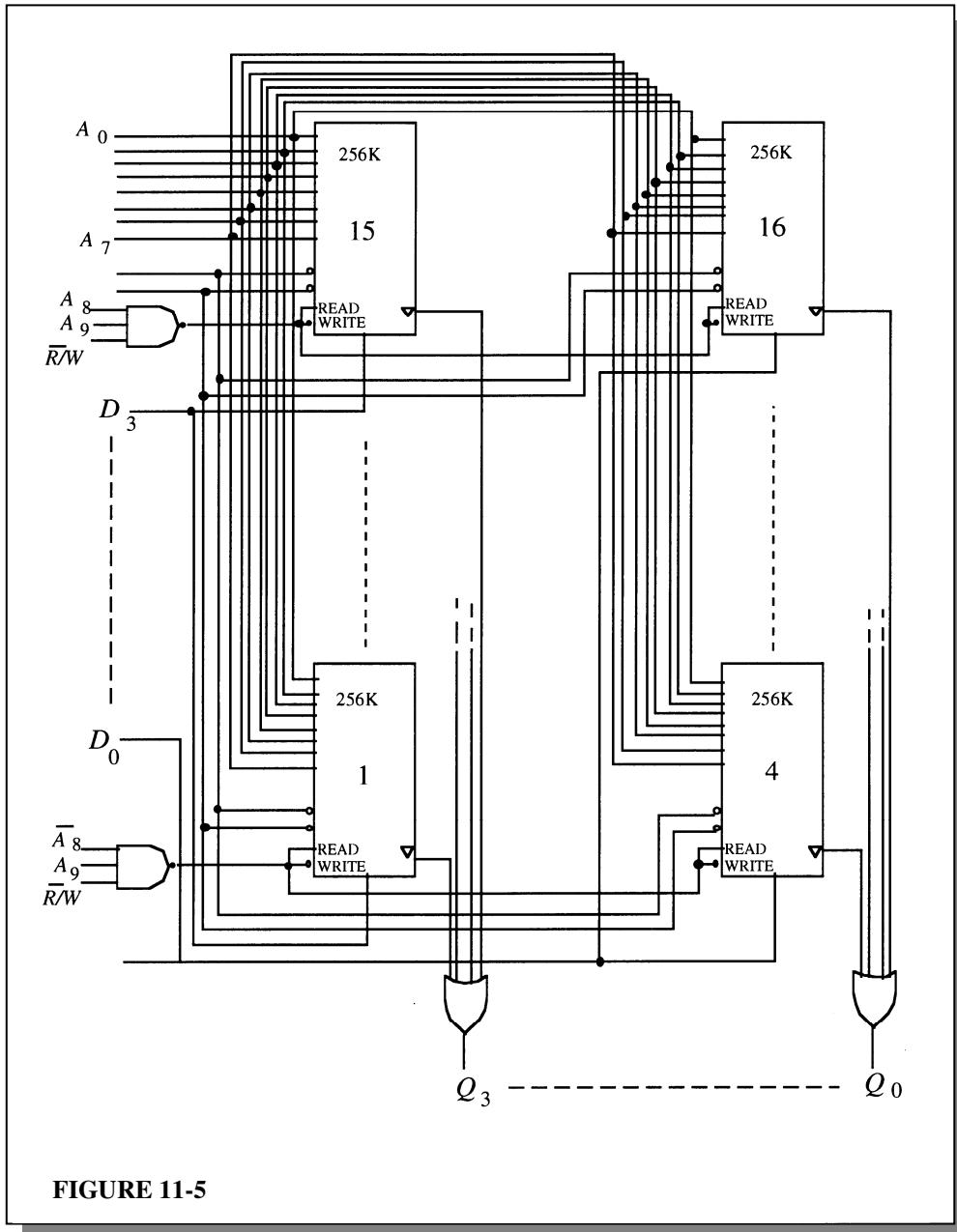
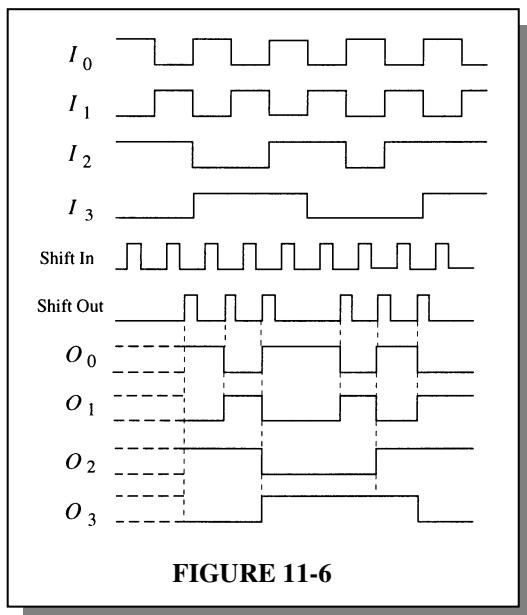


FIGURE 11-5

19. Word length = 8 bits, word capacity = **64k words**  
Word length = 4 bits, word capacity = **256k words**

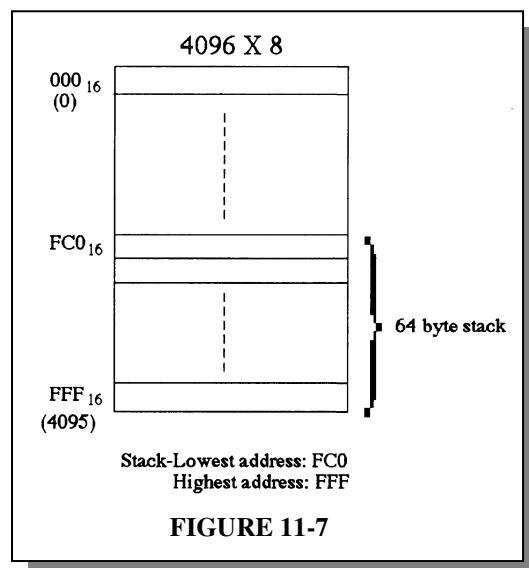
### **Section 11-7 Special Types of Memories**

**20.** See Figure 11-6.



**FIGURE 11-6**

**21.** See Figure 11-7.



**FIGURE 11-7**

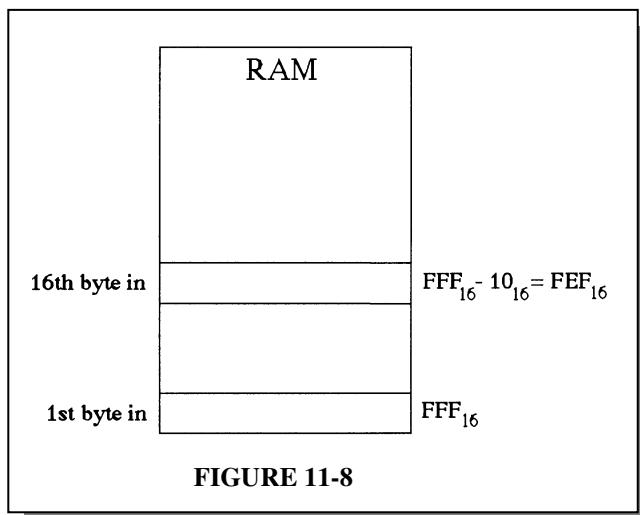
## **Chapter 11**

- 22.** The first byte goes into  $\text{FFF}_{16}$ .

The last byte (16th) goes into a lower address:  $16_{10} = 10_{16}$

$$\text{FFF}_{16} - 10_{16} = \text{FEF}_{16}$$

See Figure 11-8.



### **Section 11-8 Magnetic and Optical Storage**

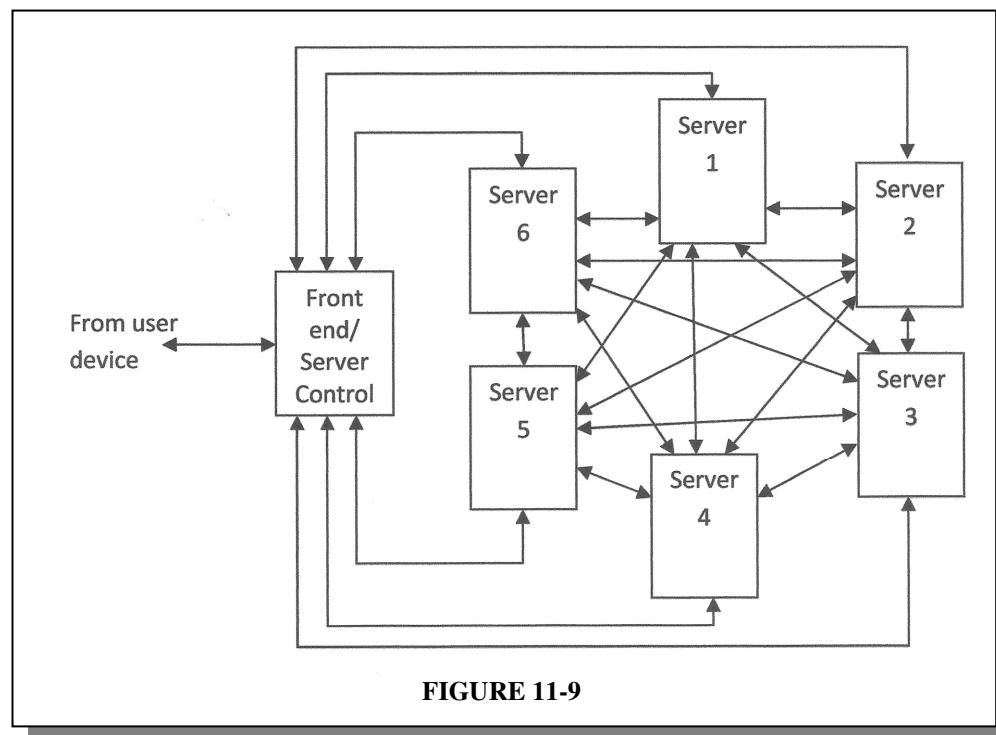
- 23.** A hard disk is formatted into tracks and sectors. Each track is divided into a number of sectors with each sector of a track having a physical address. Hard disks typically have from a few hundred to a few thousand tracks.
- 24.** Seek time is the average time required to position the drive head over the track containing the desired data. The latency period is the average time required for the data to move under the drive head.
- 25.** Magnetic tape has a longer access time than disk because data must be accessed sequentially rather than randomly.
- 26.** A magneto-optic disk is a read/write medium using lasers and magnetic fields.  
A CD-ROM (compact-disk ROM) is a read-only optical (laser) medium.  
A WORM (write-once-read-many) is an optical medium in which data can be written once and read many times.
- 27.** Blu-ray uses a blue laser and DVD uses a red laser.
- 28.** A Blu-ray disc has a higher definition and storage density than a DVD.

### **Section 11-9 Memory Hierarchy**

29. Beginning with the closest memory to the processor in terms of access time: registers, caches, main memory, hard disk, and auxiliary storage.
30. The hit rate is the percentage of memory accesses that successfully find the requested data in the given level of memory.
31. The miss rate is the percentage of memory accesses that fail to find the requested data in the given level of memory. Hit rate is equal to  $1 - \text{miss rate}$ .
32. Miss rate =  $1 - \text{hit rate} = 1 - 0.7 = 0.3$

### **Section 11-10 Cloud Storage**

33. See Figure 11-9.



34. A server provides data storage and/or processing.
35. The architecture is the way in which a cloud storage system is structured and organized. Generically, a cloud storage system consists of a front end that uses access protocols, a controller that uses data handling protocols, and a back end that provides storage.

## **Chapter 11**

- 36.** **Latency** The time between a request for data and the delivery of the data to the user is the latency of a system. Delay is due to the time for each component of the cloud storage system to respond to a request and to the time for data to be transferred to the user.

**Bandwidth** This is a measure of the range of frequencies that can be simultaneously transferred to the cloud and is defined as a range of frequencies that can be handled by the system. Generally the wider the **bandwidth**, the shorter the latency and vice versa.

**Multitenancy** The property of a cloud storage system that allows multiple users to share the same software applications and hardware and the same data storage mechanism but do not see each other's data.

**Scalability** The scalability indicates the ability of a cloud storage system to handle increasing amounts of data in a smooth and easy manner or its ability to improve movement of data through the system (throughput) when additional resources (typically hardware) are added.

**Elasticity** The ability to deal with *variations* in the amount of data (load) being transferred in and out of the storage system without service interrupts. There is a subtle difference between scalability and elasticity when describing a system's behavior. Essentially, scalability is a static parameter that indicates how much the system can be expanded and elasticity is a dynamic parameter that refers to the implementation of scalability.

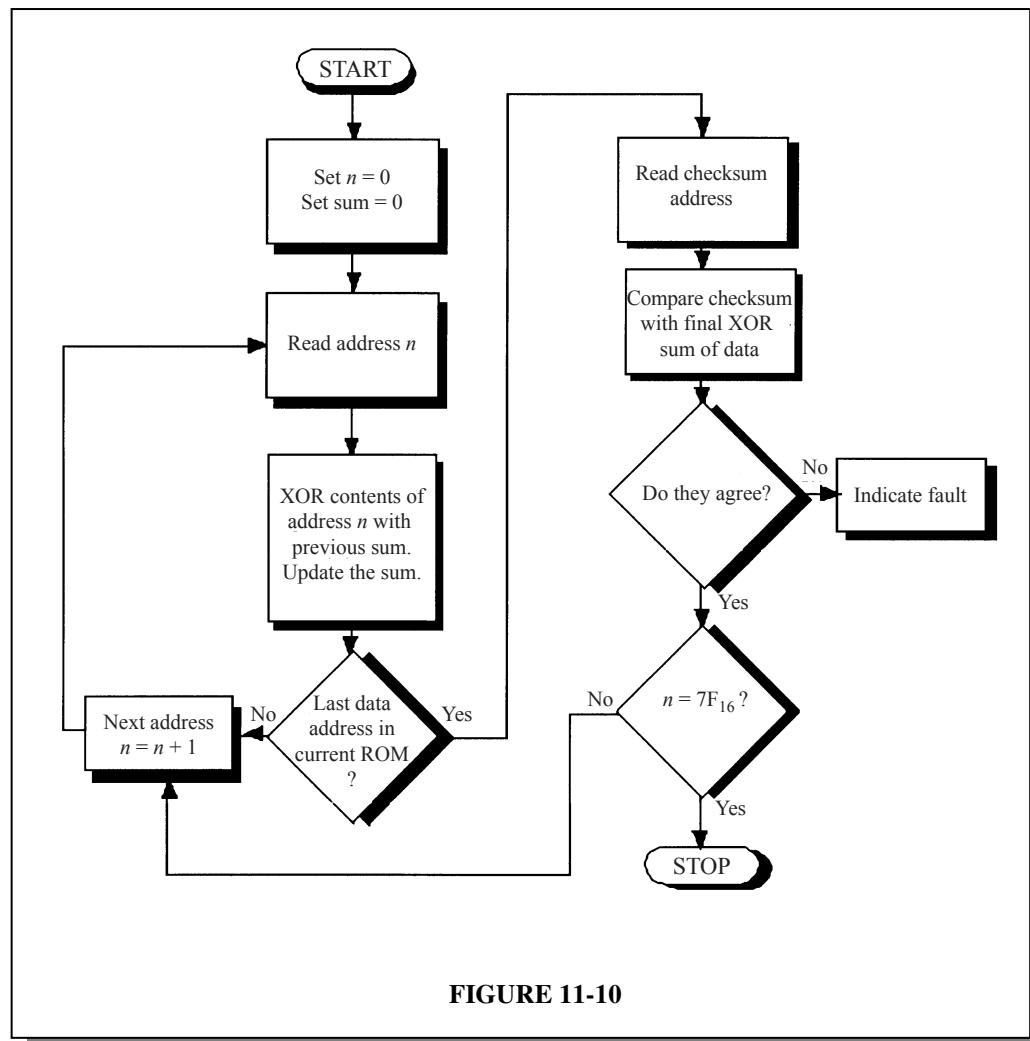
### **Section 11-11 Troubleshooting**

- 37.** The correct checksum is **00100**.

The actual checksum is 01100. The second bit from the left is in error.

- 38.** (a)
- |       |                         |                          |
|-------|-------------------------|--------------------------|
| ROM0: | Low address - $00_{16}$ | High address - $1F_{16}$ |
| ROM1: | Low address - $20_{16}$ | High address - $3F_{16}$ |
| ROM2: | Low address - $40_{16}$ | High address - $5F_{16}$ |
| ROM3: | Low address - $60_{16}$ | High address - $7F_{16}$ |
- (b) Same as flow chart in Figure 11-75 in text except that the last data address is specified as **7E<sub>16</sub>** ( $7F_{16} - 1$ ).

- (c) See Figure 11-10.



- (d) A single checksum will not isolate the faulty chip. It will only indicate that there is an error in one of the chips.
- 39.**
- (a)  $40_{16} - 5F_{16}$  is 64 – 95 decimal; ROM 2
  - (b)  $20_{16} - 3F_{16}$  is 32 – 63 decimal; ROM 1
  - (c)  $00_{16} - 7F_{16}$  is 0 – 127 decimal; All ROMs

---

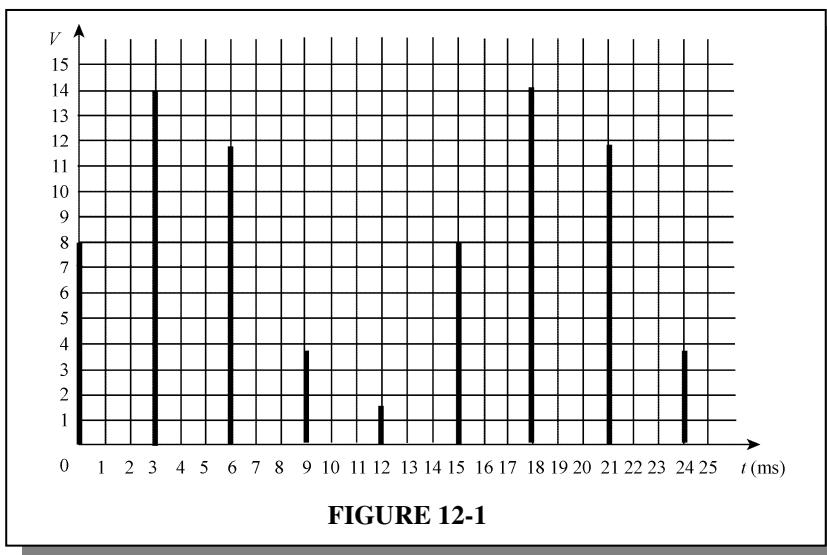
## CHAPTER 12

### SIGNAL CONVERSION AND PROCESSING

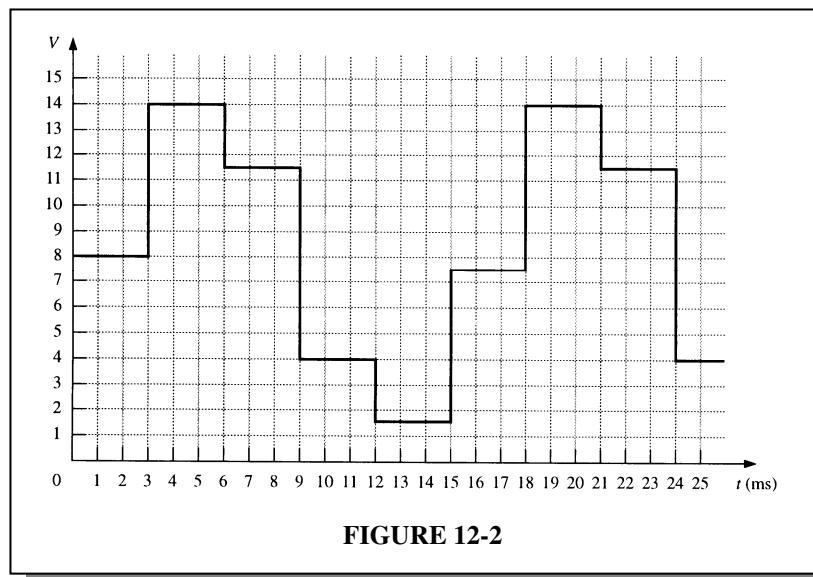
---

#### *Section 12-2 Analog-to-Digital Conversion*

1. See Figure 12-1.

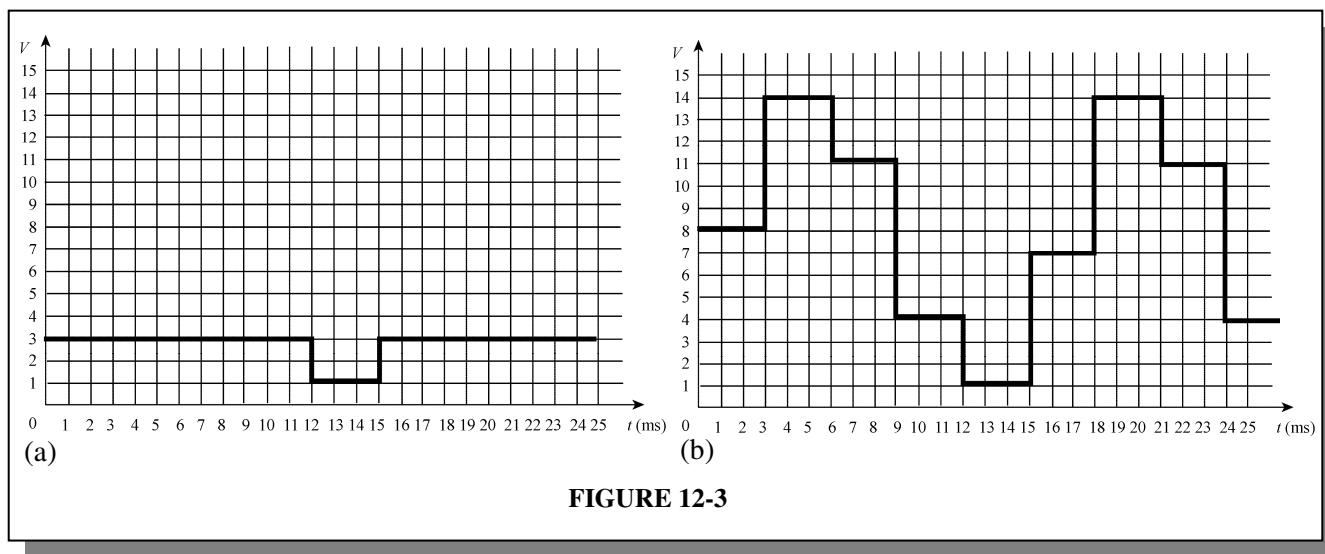


2. See Figure 12-2.



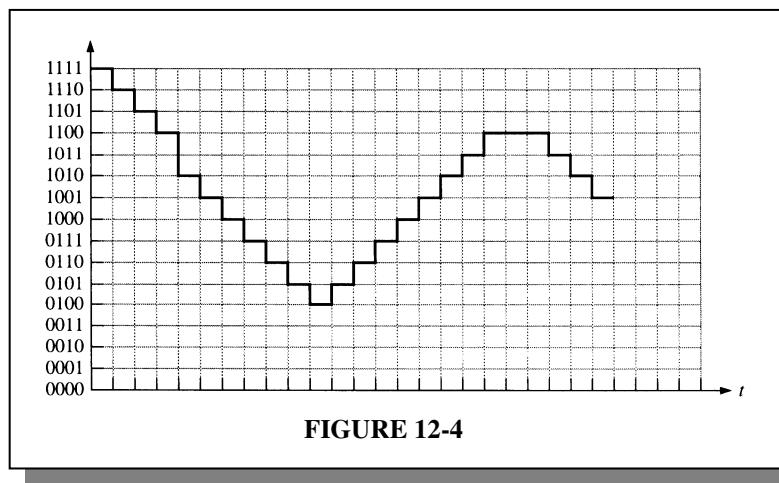
3. 11, 11, 11, 11, 01, 11, 11, 11, 11  
4. 1000, 1110, 1011, 0100, 0001, 0111, 1110, 1011, 0100

5. See Figure 12-3.



**FIGURE 12-3**

6. See Figure 12-4.



**FIGURE 12-4**

## **Section 12-2 Methods of Analog-to-Digital Conversion**

$$7. \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{2 \text{ V}}{10 \text{ mV}} = 200$$

$$8. \frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{R_F}{R_{\text{IN}}}$$

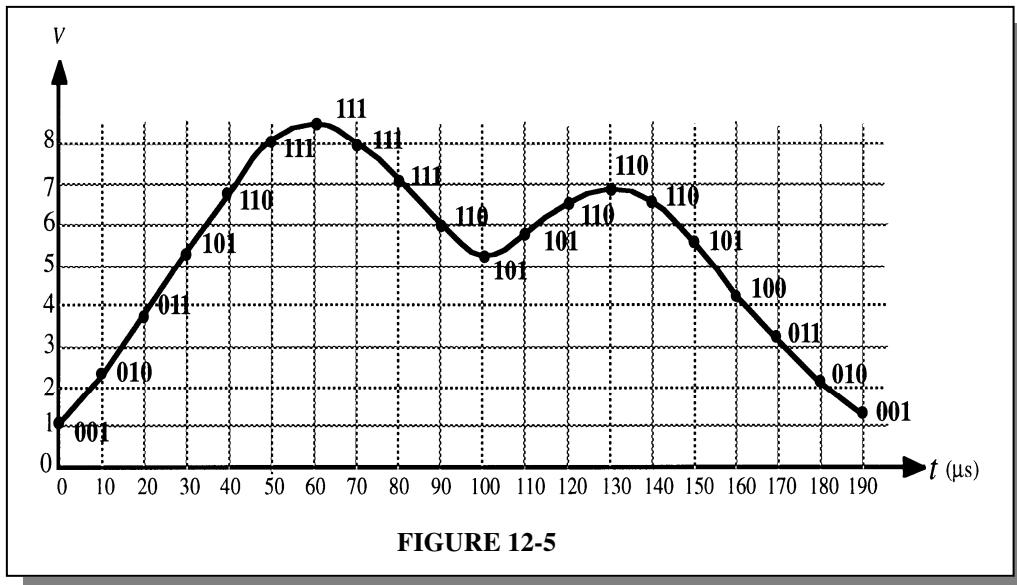
$$R_F = R_{\text{in}} \left( \frac{V_{\text{OUT}}}{V_{\text{IN}}} \right) = 1 \text{ k}\Omega (330) = 330 \text{ k}\Omega$$

$$9. A_v = \frac{R_f}{R_i} = \frac{47 \text{ k}\Omega}{2.2 \text{ k}\Omega} = -21.4$$

## Chapter 12

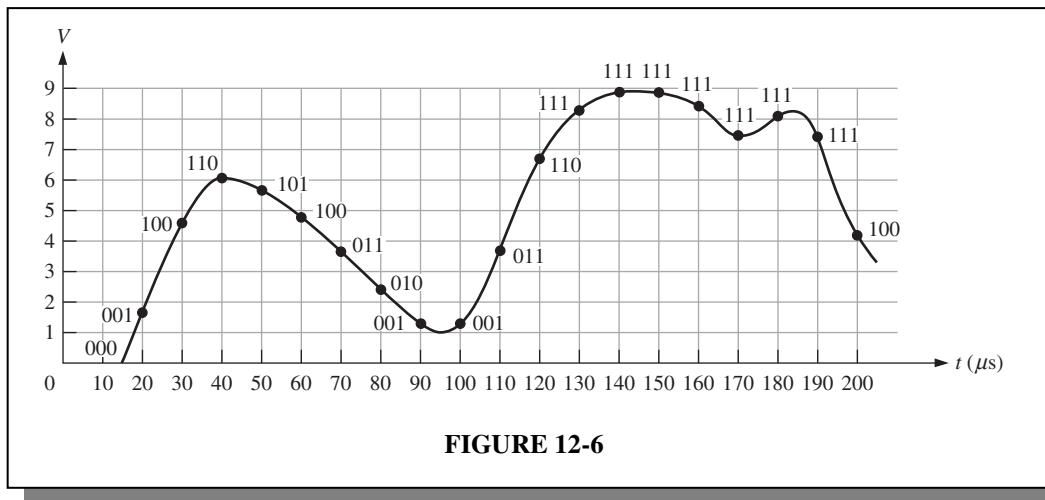
10. Number of comparators =  $2^n - 1 = 2^8 - 1 = 255$
11. 001, 010, 011, 101, 110, 111, 111, 111, 110, 101, 101, 110, 110, 101, 100, 011, 010, 001.

See Figure 12-5.



12. Output of 3-bit converter: 000, 001, 100, 110, 101, 100, 011, 010, 001, 001, 011, 110, 111, 111, 111, 111, 111, 111, 100.

See Figure 12-6.



**13.**

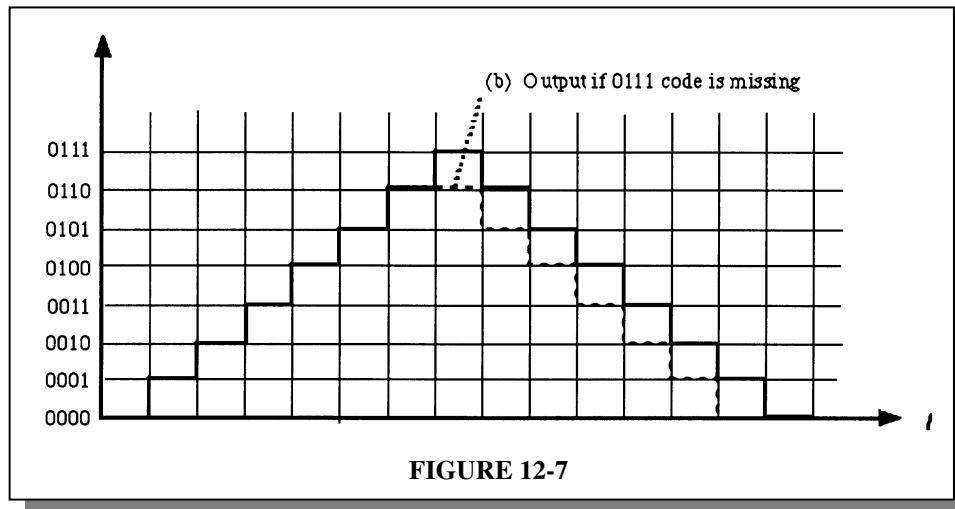
| SAR | Comment                          |
|-----|----------------------------------|
| 11  | Less than $V_{in}$ . Keep the 1. |
| 11  | Less than $V_{in}$ . Keep the 1. |
| 11  | Less than $V_{in}$ . Keep the 1. |

Conversion never terminates since 2 bits cannot represent the input.

**14.**

| SAR  | Comment                                      |
|------|----------------------------------------------|
| 1000 | Greater than $V_{in}$ . Reset MSB.           |
| 0100 | Less than $V_{in}$ . Keep the 1.             |
| 0110 | Equal to $V_{in}$ . Keep the 1 (final state) |

**15.** See Figure 12-7.



### Section 12-3 Methods of Digital-to-Analog Conversion

**216.**  $R_0 = 10 \text{ k}\Omega$

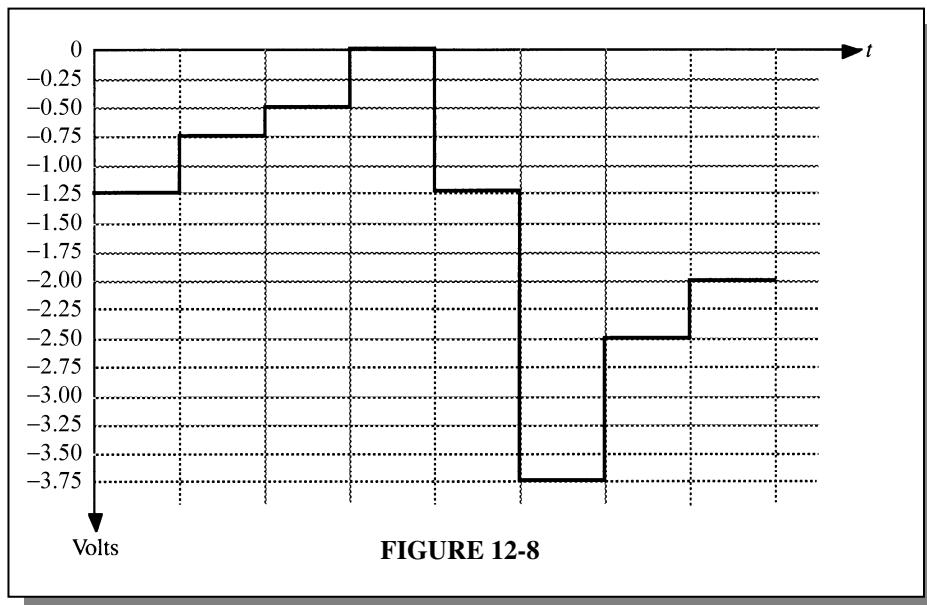
$$R_1 = \frac{R_0}{2} = \frac{10 \text{ k}\Omega}{2} = 5 \text{ k}\Omega$$

$$R_2 = \frac{R_0}{4} = \frac{10 \text{ k}\Omega}{4} = 2.5 \text{ k}\Omega$$

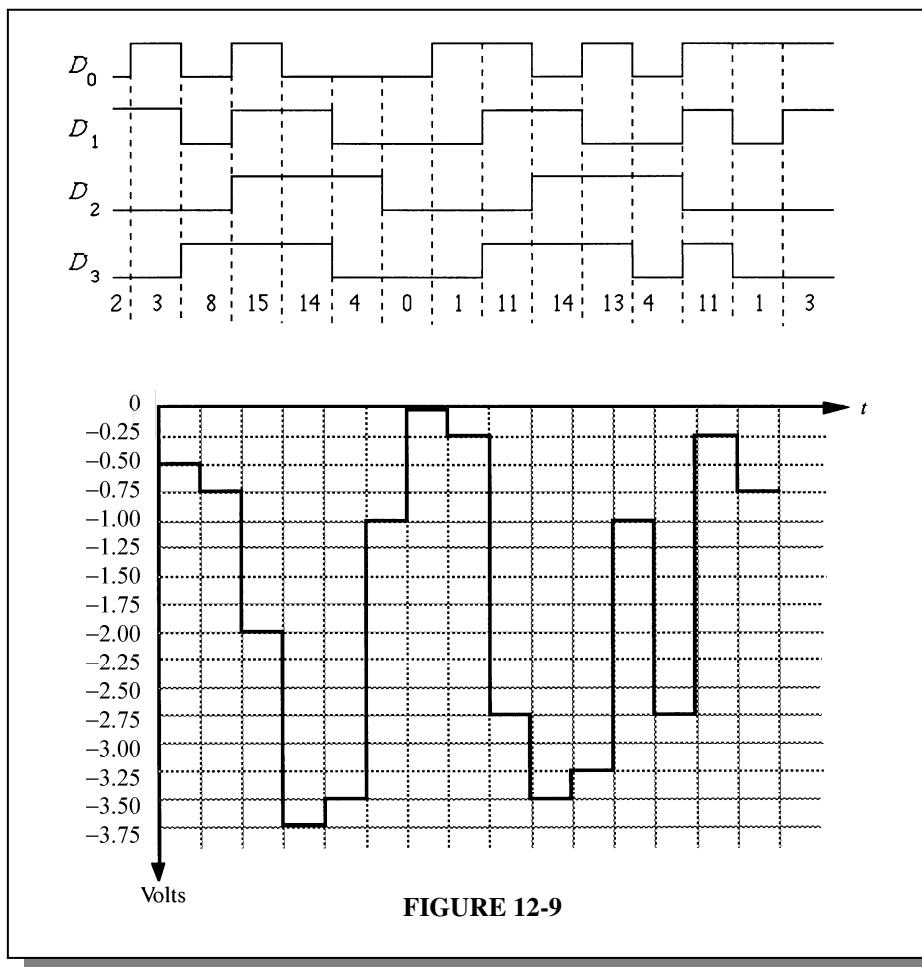
$$R_3 = \frac{R_0}{8} = \frac{10 \text{ k}\Omega}{8} = 1.25 \text{ k}\Omega$$

## Chapter 12

17. See Figure 12-8.

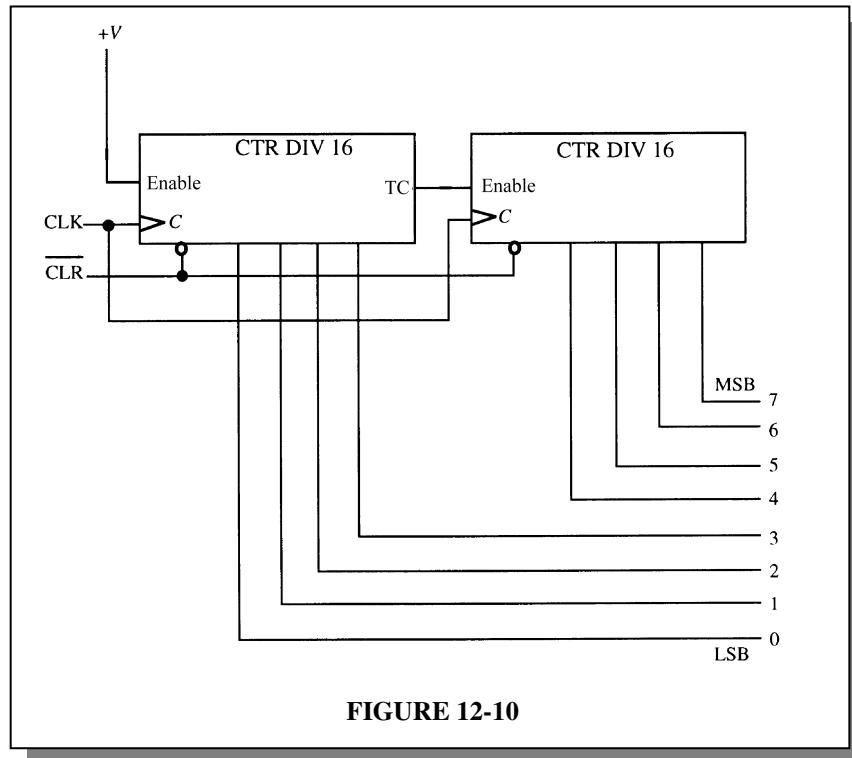


18. See Figure 12-9.



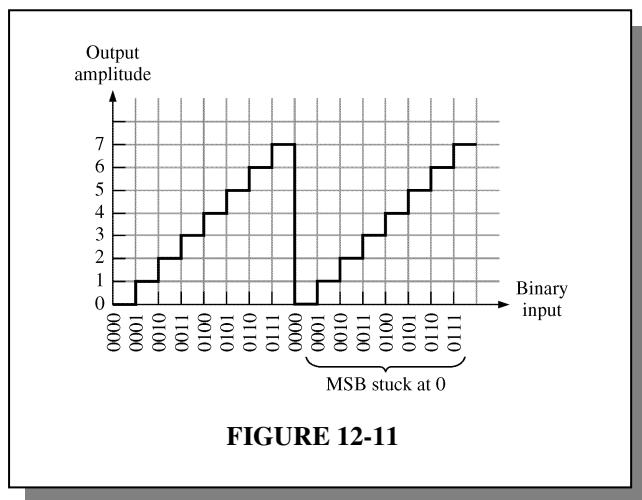
19. (a)  $\left(\frac{1}{(2^3-1)}\right)100 = 14.3\%$
- (b)  $\left(\frac{1}{2^{10}-1}\right)100 = 0.098\%$
- (c)  $\left(\frac{1}{2^{18}-1}\right)100 = 0.00038\%$

20. See Figure 12-10.



**FIGURE 12-10**

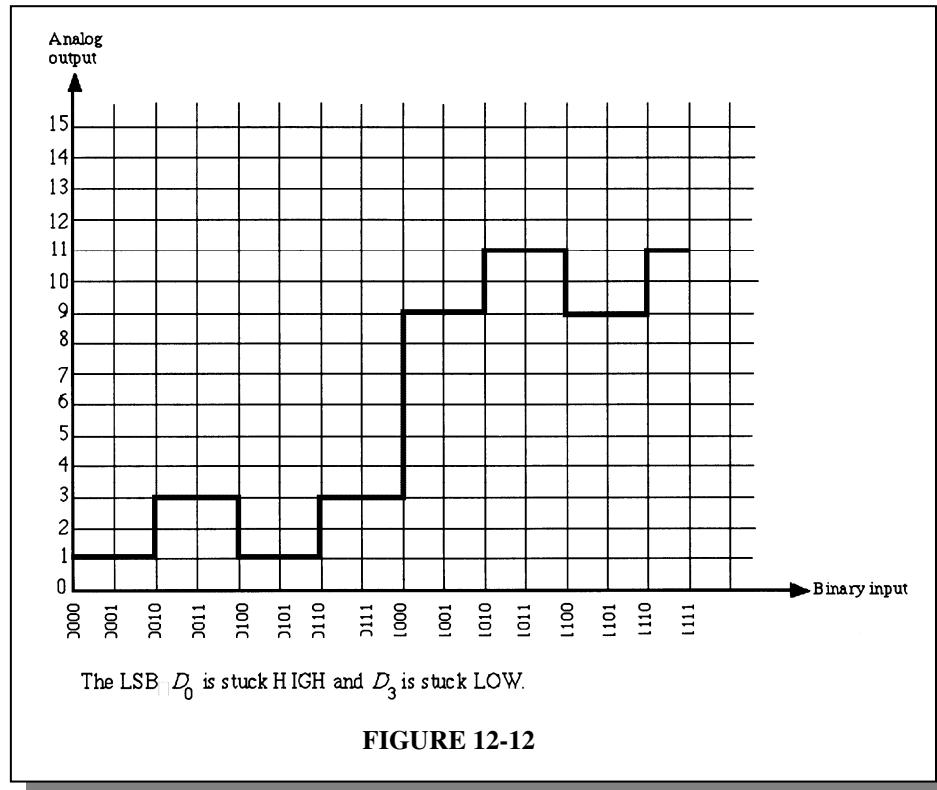
21. See Figure 12-11.



**FIGURE 12-11**

## **Chapter 12**

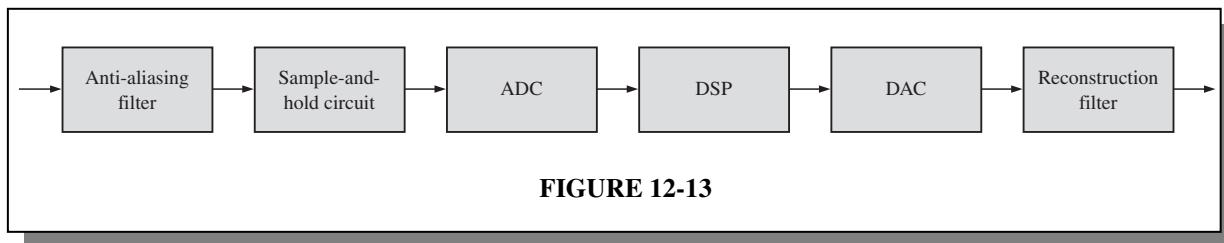
- 22.** See Figure 12-12.



**FIGURE 12-12**

### **Section 12-4 Digital Signal Processing**

- 23.** The purpose of analog-to-digital conversion is to change an analog signal into a sequence of digital codes that represent the amplitude of the analog signal with respect to time.
- 24.** See Figure 12-13.



**FIGURE 12-13**

- 25.** The purpose of digital-to-analog conversion is to change a sequence of digital codes into an analog signal represented by the digital codes.

**Section 12-5 The Digital Signal Processor (DSP)**

**26.**  $2000 \text{ MIPS} \times \frac{32 \text{ bit/instruction}}{8 \text{ bits/byte}}$

=  $2000 \text{ MIPS} \times 4 \text{ bytes/instruction}$

=  $8000 \text{ Mbytes/s}$

**27.**  $\frac{400 \text{ Mbits/s}}{32 \text{ bits/instruction}} = 12.5 \text{ million instructions/s}$

**28.**  $1000 \text{ MFLOPS} = 1,000,000,000 \text{ floating-point operations/s}$

- 29.**
1. Program address generate (PG). The program address is generated by the CPU.
  2. Program address send (PS). The program address is sent to the memory.
  3. Program access ready wait (PW). A memory read operation occurs.
  4. Program fetch packet receive (PR). The CPU receives the packet of instructions.

- 30.**
1. Instruction dispatch (DP): Instruction packets are split into execute packets and assigned to functional units;
  2. Instruction decode (DC): Instructions are decoded.

---

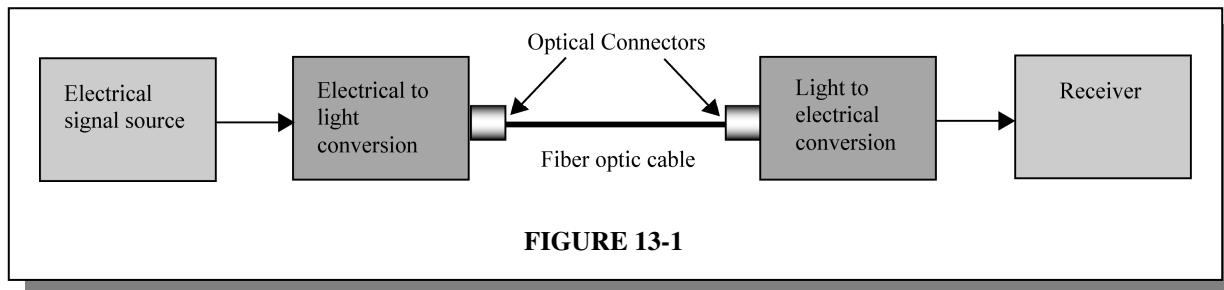
## CHAPTER 13

# DATA TRANSMISSION

---

### Section 13-1 Data Transmission Media

1. A coaxial cable consists of an outer jacket, metallic shield, dielectric, and center conductor.
2. Types of twisted pair cable: UTP: unshielded tested pair; STP: shielded twisted pair
3. Advantages of fiber optics over electrical transmission media are faster data rates, higher signal capacity (more signals at a time), transmission over longer distances, and not susceptible to EMI.
4. Three parts of an optical fiber are the core through which the light travels, the highly reflective cladding surrounding the core, and the protective jacket around the cladding.
5. In multimode, the light entering the optical fiber will tend to propagate through the core in multiple rays (modes), basically due to varying angles as each light ray moves along.
6. The 50/125 and 62.5/125 are multimode fibers. The 8.3/125 is a single-mode fiber.
7. See Figure 13-1.



8. A frequency of 100 MHz is a radio wave.
9. Visible light is in the frequency range  $4 \times 10^{14}$  Hz to  $7.5 \times 10^{14}$  Hz. Figure 13-10 in the textbook shows the range in units of wavelength (nm).

### Section 13-2 Methods and Modes of Data Transmission

10. Number of bits =  $(1 \times 10^6 \text{ bits/s})(1 \times 10^{-3} \text{ s}) = 1000 \text{ bits}$
11.  $\frac{8 \text{ bits}}{1 \mu\text{s}} = 8 \text{ Mbps}$

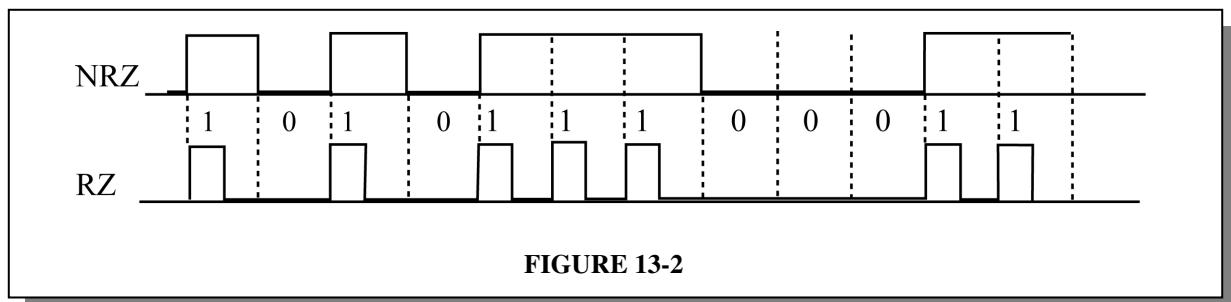
12. Bit rate =  $\frac{(3 \text{ bits/symbol})(12 \text{ symbols})}{0.5 \mu\text{s}} = \frac{36 \text{ bits}}{0.5 \mu\text{s}} = 72 \text{ Mbps}$

$$\text{Baud} = \frac{72 \text{ Mbps}}{(3 \text{ bits/symbol})} = 24 \text{ Mbaud}$$

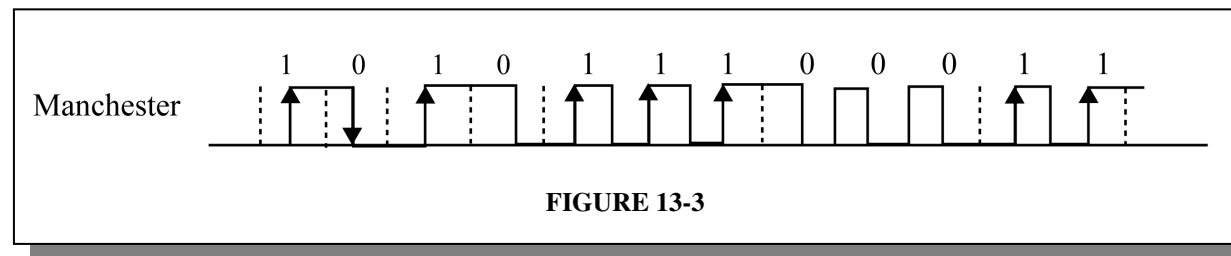
13. Baud =  $\frac{25 \text{ Mbps}}{(5 \text{ bits/symbol})} = 5 \text{ Mbaud}$

14. Efficiency =  $\frac{\text{Data bits}}{\text{data bits}} = \frac{16}{20} = 0.8$

15. See Figure 13-2.



16. See Figure 13-3.



17. The bit sequence represented by the Manchester code is **001110011**.

- *Preamble:* A group of bits at the beginning of a frame that is used to alert the receiver that a new frame has arrived and to synchronize the receiver's clock with the transmitted clock.
- *Address Fields:* A group of bits containing the address(s) of the sender and the receiver. One or both addresses may be present in a given protocol.
- *Control Field:* This group of bits identifies the type of data being sent, such as handshaking (establishes a connection), file transfers, and the size of the data.
- *Data Field:* This sequence is the actual information being sent and can be of a fixed length or a variable length. If it is a fixed-length field, a group of bits called a *pad* is used to fill in if the actual data field is less than the fixed field.

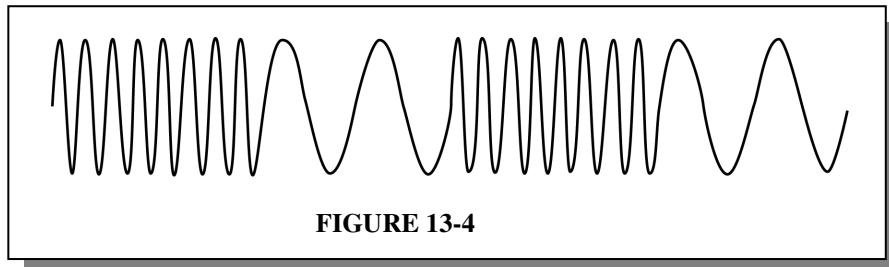
## Chapter 13

- *Frame Check:* This field contains an error check such as parity, CRC (cyclic redundancy check), or checksum, which is a value computed by a simple algorithm of the data bits in the frame.
- *End Frame:* A group of bits that tells the receiver when the end of the frame occurs.

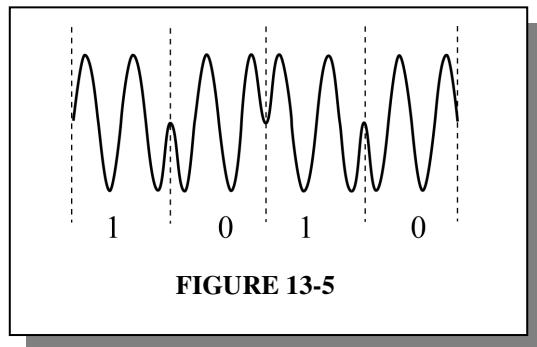
### Section 13-3 Modulation of Analog Signals with Digital Data

19. The binary code represented by the ASK signal is **11010111110001000001**.

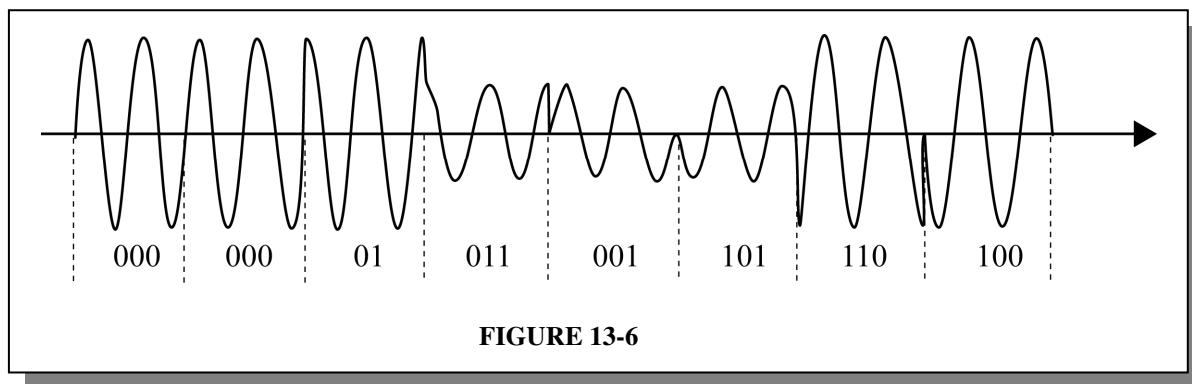
20. See Figure 13-4. FSK represents 1010.



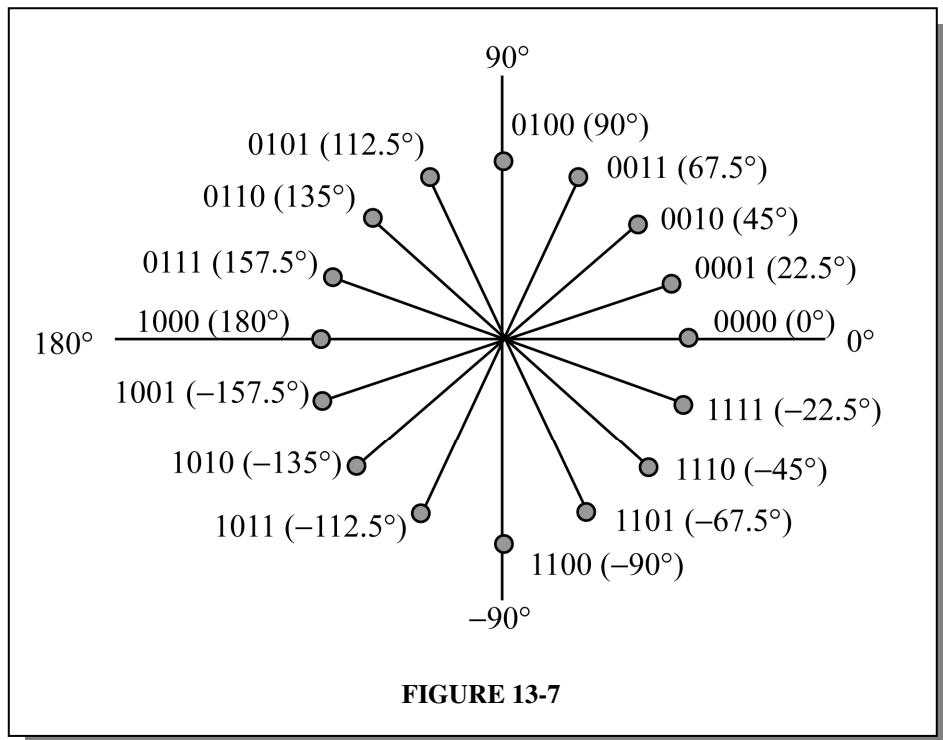
21. See Figure 13-5.



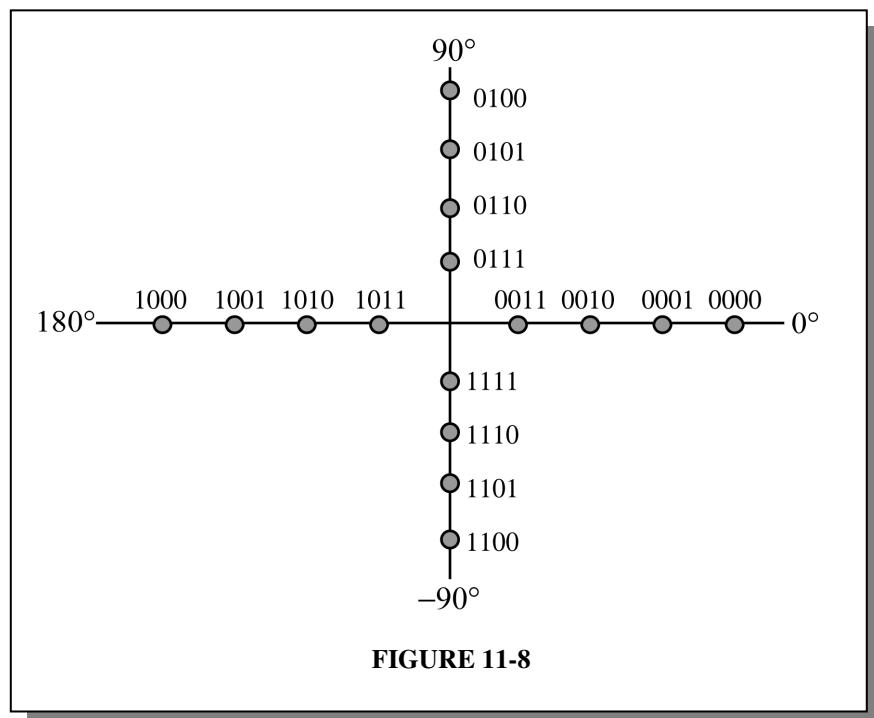
22. See Figure 13-6.



- 23.** See Figure 13-7.



- 24.** Four phases and four amplitudes can be used as shown in Figure 13-8.

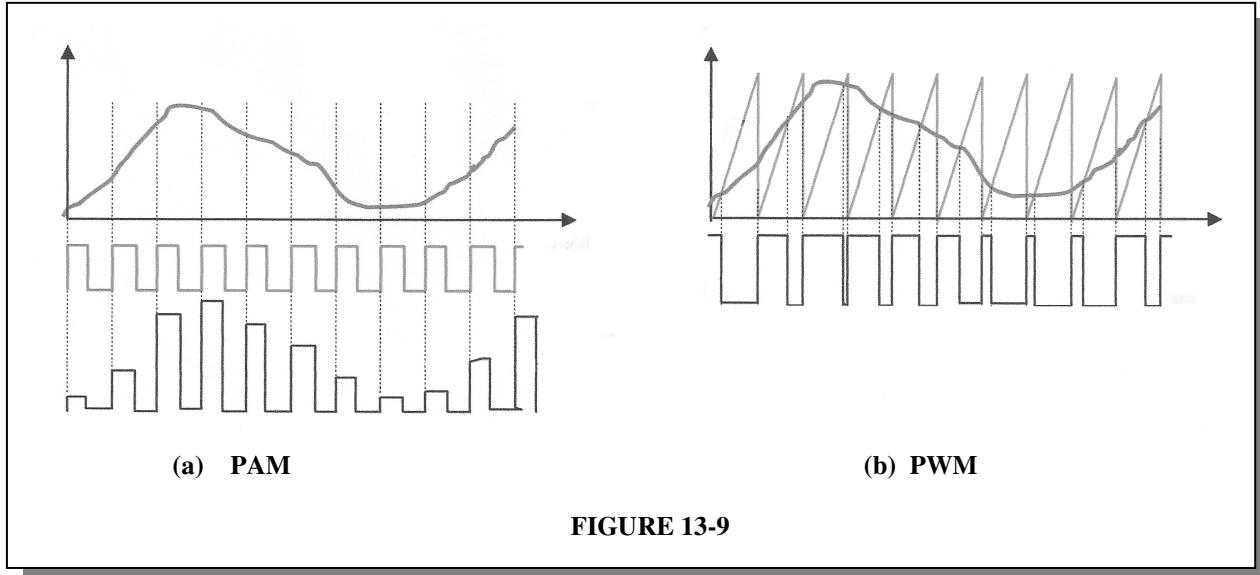


## Chapter 13

### Section 13-4 Modulation of Digital Signals with Analog Data

25. In the PWM intersective method, the sawtooth intersects the sinusoidal modulating signal twice during each cycle. The sawtooth is either increasing above the sine wave or decreasing below the sine wave. When the sawtooth is increasing above the sine wave, a low level is generated, and when it is decreasing below the sine wave, a high level is generated. The resulting output is a series of pulses with widths proportional to the amplitude of the sine wave.

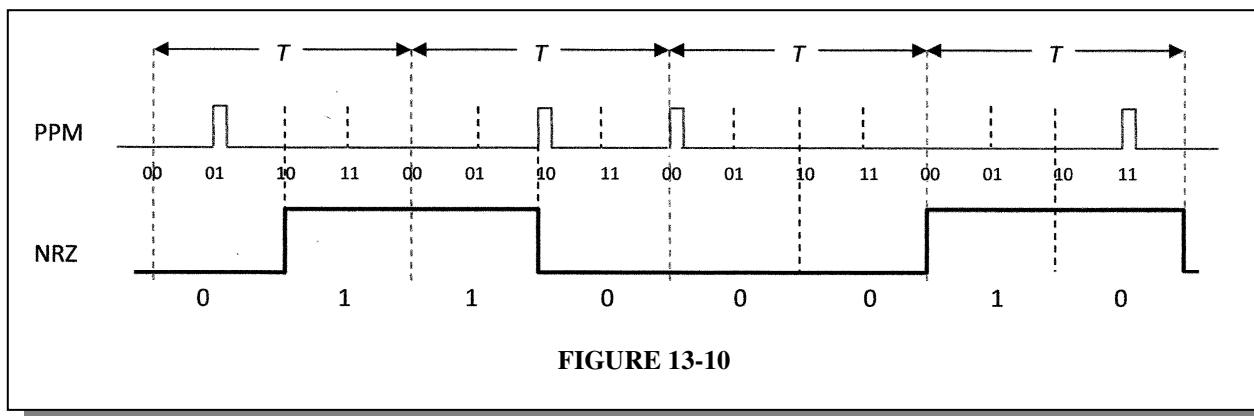
26. See Figure 13-9.



27. It takes three bits to describe each of the eight positions.

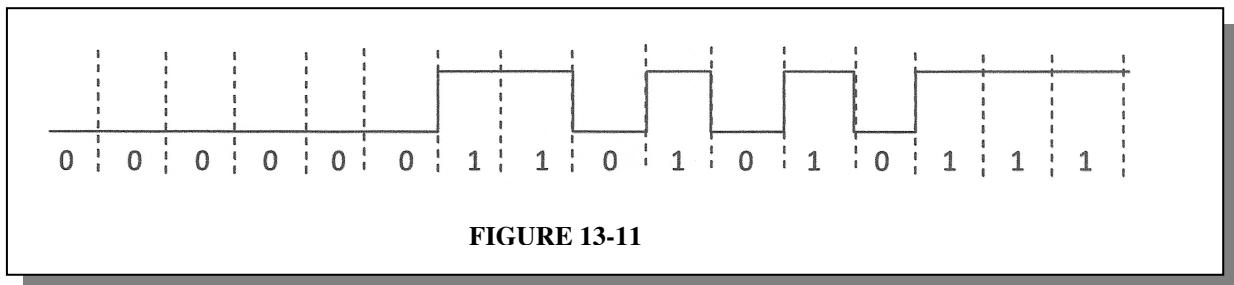
$$\text{Data rate } \frac{3 \text{ bits}}{10 \text{ ms}} = 300 \text{ bps}$$

28. The bit sequence of the PPM signal is 01100011. See Figure 13-10.



29.  $16 = 2^4$ . Four bits are required to represent 16 voltage levels.

- 30.** The sequence of bits is 0000001101010111. The NRZ code is shown in Figure 13-11.



### **Section 13-5 Multiplexing and Demultiplexing**

- 31.** Bit interleaved: A single data bit from a source is transmitted on the channel, followed by a data bit from another source, and so on.  
Byte interleaved: A byte of data from a source is transmitted on the channel, followed by a byte from another source, and so on.
- 32.** In synchronous TDM, the time slots allotted to each source are fixed, and each time slot is transmitted whether or not the source has data to send. In statistical TDM, the time slot assignments are variable so that only data from active sources are transmitted and no blank time slots are transmitted.
- 33.** In FDM, band-pass filters are used on the receiving end to separate the transmitted signals.
- 34.** The frequency separation between each source in FDM is called the **guard band**.

### **Section 13-6 Bus Basics**

- 35.** Physical characteristics of a bus: Number of conductors, length, configuration, (serial or parallel), type of connector, number of connector pins, pin configuration.  
Electrical/performance characteristics of a bus: Signal format, signal voltage, clock frequency, transfer speed, bandwidth, data frame format, handshaking protocol, error detection, impedances.
- 36.** Bus width is the number of bits that a bus can transmit at one time. Bus bandwidth, expressed in MBps is the number of bytes per clock cycle times the number of clock cycles per second.

$$37. \text{ Bandwidth} = \frac{(\text{width})(\text{frequency})}{8 \text{ bits/byte}} = \frac{(16 \text{ bits})(100 \text{ MHz})}{8 \text{ bits/byte}} = 200 \text{ MBps}$$

$$\text{Bandwidth} = \frac{\frac{(\text{width})(\text{frequency})}{8 \text{ bits/byte}}}{2^{20}} \cdot 10^6 = 191 \text{ MBps}$$

## **Chapter 13**

- 38.** Simple handshake protocol: A requesting device sends a request for data to a responding device. The responding device acknowledges the request and sends that data.
- 39.** A differential bus provides much higher data rates and longer transmission distances than does a single-ended bus.

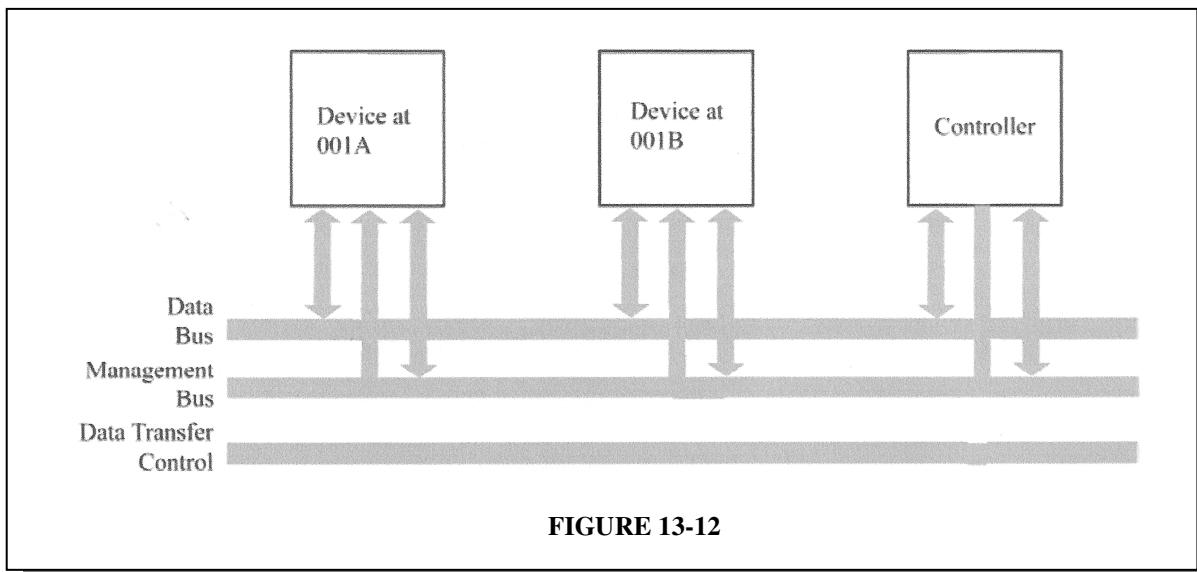
### **Section 13-7 Parallel Buses**

- 40.** The PCI bus is an internal synchronous bus for interconnecting chips, expansion boards, and processor/memory subsystems. The original PCI bus has a width of 32 bits and a frequency of 33 MHz. Another version has a width of 64 bits and a frequency of 66 MHz. Still later versions enable 64-bit data transfers using up to a 133 MHz clock to enable bandwidths of up to 1066 MBps.

The PCI-X bus is a high-performance enhancement of the PCI and is backward compatible with PCI, although it is a faster bus and has some additional features. It is a 64-bit bus. PCI-X runs at a frequency of 133 MHz, and the PCI-X 2.0 revision supports frequencies of 266 MHz and 533 MHz. Some of the additional features increase system reliability by minimizing errors at a high transfer rates.

- 41.** The PCI-Express bus does not use a shared bus as PCI and PCI-X do.
- 42.** x2 indicates a two-lane bus.
- 43.** The terms *talker* and *listener* area associated with the IEE-488 bus (GPIB).
- 44.**

|                   |                            |
|-------------------|----------------------------|
| BSY: Busy         | MSG: Message               |
| SEL: Select       | REQ: Request               |
| RST: Reset        | ACK: Acknowledge a request |
| C/D: Control Data | ATN: Attention             |
- 45.** Three data bytes are transferred because the NDAC line goes HIGH three times, each time indicating that a data byte is accepted.
- 46.** A controller is sending data to two listeners. The first two bytes of data (3F and 41) go to the listener with address 001A. The second two bytes go to the listener with address 001B. The handshake signals (DAV, NRFD, and NDAC) indicate that the data transfer is successful. See Figure 13-12.



### **Section 13-8 The Universal Serial Bus (USB)**

- 40. (a) SCSI            (b) USB            (c) Super speed USB (V 3.0)
- 48. Four types of USB packets: Token, data, handshake, and start-of-frame.
- 49. *Sync Field:* All packets start with a sync (synchronization) field. The sync field consists of 8 bits for low and full speed or 32 bits for high speed and is used to synchronize the receiver clock with that of the transmitter.

*PID Field:* The packet identification field is used to identify the type of packet that is being transmitted. There are 4 bits in the PID; however, to ensure it is received correctly, the 4 bits are complemented and repeated, making an 8-bit PID code.

*Data Field:* Contains up to 1024 bytes of data.

*CRC Field:* Cyclic Redundancy Checks are performed on the data within the packet using from 5 bits to 16 bits, depending on the type of packet.

*EOP Field:* This field signals the end of packet.

- 50. USE 3.0 uses NRZ encoding.
- 51. Maximum USB data bytes =  $\frac{8192 \text{ bits}}{8 \text{ bits per byte}} = 1024 \text{ bytes}$
- 52. From Table 13-8 in the textbook, the maximum cable length connecting to USB 2.0 devices is 16.4 ft.

## Chapter 13

### Section 13-9 Other Serial Buses

53. RS-232 uses single-ended transmission. RS-422 uses differential transmission.
54. (1) MOSI (master out slave in) is initiated by the master and received by the slave.  
(2) MISO (master in slave out) is initiated by the slave and received by the master.  
(3) SCLK (serial clock) is generated by the master for synchronizing data transfers.  
(4) SS (slave select) is generated by the master to select an individual slave.
55.  $I^2C$  is an internal serial bus primarily for connecting ICs on a PC board.
- 56.
- | SOF                                            | Arbitration field                | Control field | Data field | CRC field | ACK      | EOF |
|------------------------------------------------|----------------------------------|---------------|------------|-----------|----------|-----|
| (1 bit)<br>Identifier (11 bits)<br>RTR (1 bit) | Reserve (2 bits)<br>DLC (4 bits) | (0 – 8 bytes) | (16 bits)  | (2 bits)  | (7 bits) |     |
57. Other possible units on an automotive CAN system include wiper control unit, parking control unit, entertainment system unit, tire pressure monitor, seat position unit, heads-up display unit.
58. IEEE-1394 S100 data rate = **98.304 MBps**: IEEE-1392 S1600 data rate = 1.6 Gbps.

### Section 13-10 Bus Interfacing

59. See Figure 13-13.

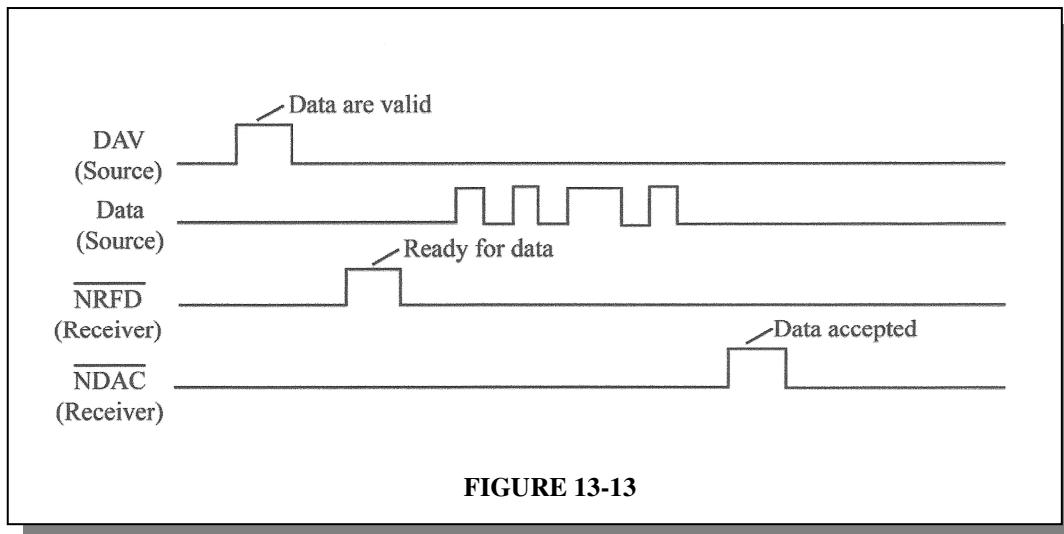
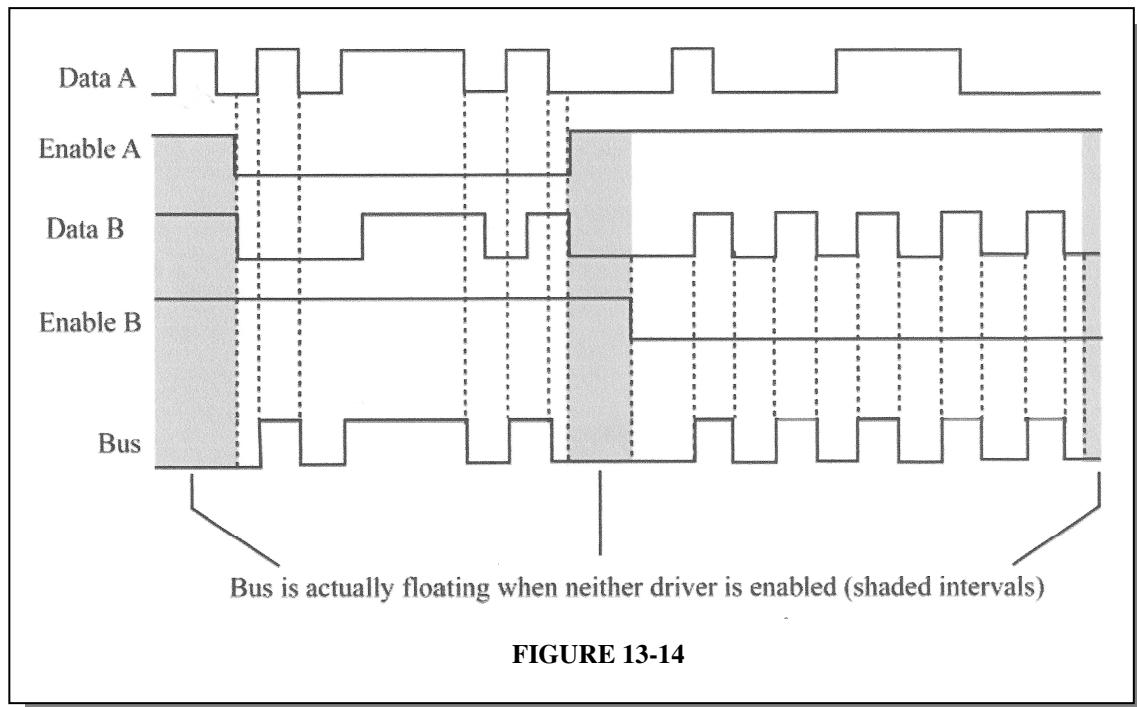
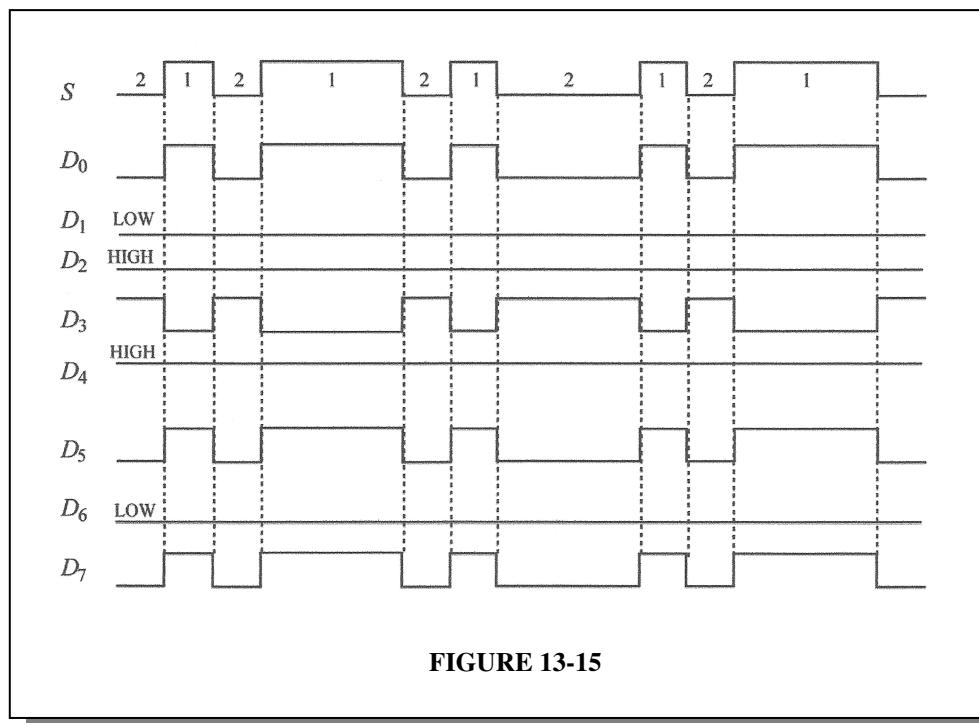


FIGURE 13-13

60. See Figure 13-14.



61. See Figure 13-15.



---

## **CHAPTER 14**

### **DATA PROCESSING AND CONTROL**

---

#### ***Section 14-1 The Basic Computer System***

1. The basic elements of a computer are the CPU, memory/storage, input/output, and buses.
2. The functional units of a CPU are the arithmetic logic unit (ALU), the instruction decoder, the register set, and timing/control unit.
3. A bus is a conductor or set of conductors for transferring data that meets certain specifications.
4. The control bus signal lines vary in characteristics, nature, and function whereas the address and data bus signals are functionally identical within each bus.

#### ***Section 14-2 Practical Computer System Considerations***

5. Tristate and open-collector outputs are used to connect devices to a bus.
6. Signal loading is caused by the input current requirement or the input capacitance of a device or devices that the signal is driving. If the number of devices exceeds the fan-out specification of the driving device, signal loading occurs. Buffers are used to prevent signal loading.
7. (a) Nine loads      (b) Two loads
8. A decoder is used to select and enable a device based on the address of the device. The chip select input of a given device is enabled.
9. The wait state holds the state of the bus signals for one processor clock to allow the processor to complete an access operation.

#### ***Section 14-3 The Processor: Basic Operation***

10. The basic elements of a microprocessor or CPU are the ALU (arithmetic logic unit), the instruction decoder, the timing/control unit, and register set.
11. The microprocessor controls system hardware, provides hardware support for the operating system, and executes application programs.
12. The three microprocessor buses are the address bus, the data bus, and the control bus.
13. During fetch, an instruction is read from memory and decoded. During execute, the processor carries out the sequence of operations called for by the instruction.
14. Pipelining is a process used by a microprocessor to begin executing the next instruction in a program before the previous instruction has been completed. Several instructions can be in the pipeline simultaneously, each at different processing stages called segments. When a segment

completes an operation, it passes the result of the operation to the next segment and fetches the next operation from the preceding segment.

#### **Section 14-4 The Processor: Addressing Modes**

**15.** Sequence of events in the inherent addressing mode:

- (1) Address of op-code placed on address bus
- (2) Op-code (instruction) placed on data bus and stored in data register
- (3) Instruction decoded
- (4) Instruction carried out

**16.** Sequence of events in the direct addressing mode:

*First fetch/execute cycle:*

- (1) Address of op-code, placed on address bus
- (2) Op-code (instruction) placed on data bus and stored in data register
- (3) Instruction decoded
- (4) Instruction carried out

*Second fetch/execute cycle:*

- (5) Address of operand placed on address bus
- (6) Operand address placed on data bus and stored in data register
- (7) Operand address loaded into address register.

*Third fetch/execute cycle:*

- (8) Address of operand placed on address bus
- (9) Operand address placed on data bus and stored in data register
- (10) Operand loaded into accumulator

**17.** Sequence of events in the indexed addressing mode:

*First fetch/execute cycle:*

- (1) Address of indexed op-code placed on address bus
- (2) Indexed op-code placed on data bus and stored in data register
- (3) Indexed instruction decoded
- (4) Address of operand fetched

*Second fetch/execute cycle:*

- (5) Offset address selected
- (6) Offset address placed on data bus and stored in data register
- (7) Offset address added to contents of index register to produce address of operand.

*Third fetch/execute cycle:*

- (8) Address of operand transferred to address register
- (9) Address of operand placed on address bus
- (10) Operand address placed on data bus and stored in data register
- (11) Operand loaded into accumulator

## **Chapter 14**

- 18.** The processor will branch to the address which is the sum of the program count and the relative address in the data register: Address =  $125_{10} + 55_{10} = 180_{10}$  ( $10110100_2$ ).

### **Section 14-5 The Processor: Special Operations**

- 19.** The interrupt vector table is used in auto-vectorized interrupts to obtain the starting address for an interrupt service routine (ISR).
- 20.** The interrupt service routine (ISR) is similar to a standard (normal) subroutine with the following exceptions:
1. The processor automatically saves status information about the program that is executing at the time of the interrupt.
  2. The processor obtains the address of the ISR.
  3. The ISR uses an RTI instruction rather than a standard RET to return to the main program.
- 21.** The sequence of events during a bus request operation is as follows:
- (1) The bus master requesting control of the system buses submits a request by asserting the processor's bus request (BR) line.
  - (2) The processor tristates the system buses and signals that it has released control of the buses by asserting the bus grant (BG) line.
  - (3) The requesting bus master uses the system address, data, and control lines to transfer data between system devices.
  - (4) After completing the data transfers, the requesting bus master tristates the system buses and signals the end of the bus request operation by asserting the bus grant acknowledge (BGACK) line.
- 22.** DMA is direct memory access. The purpose of DMA is to transfer large amounts of data between system devices in a fraction of the time required by the system processor.

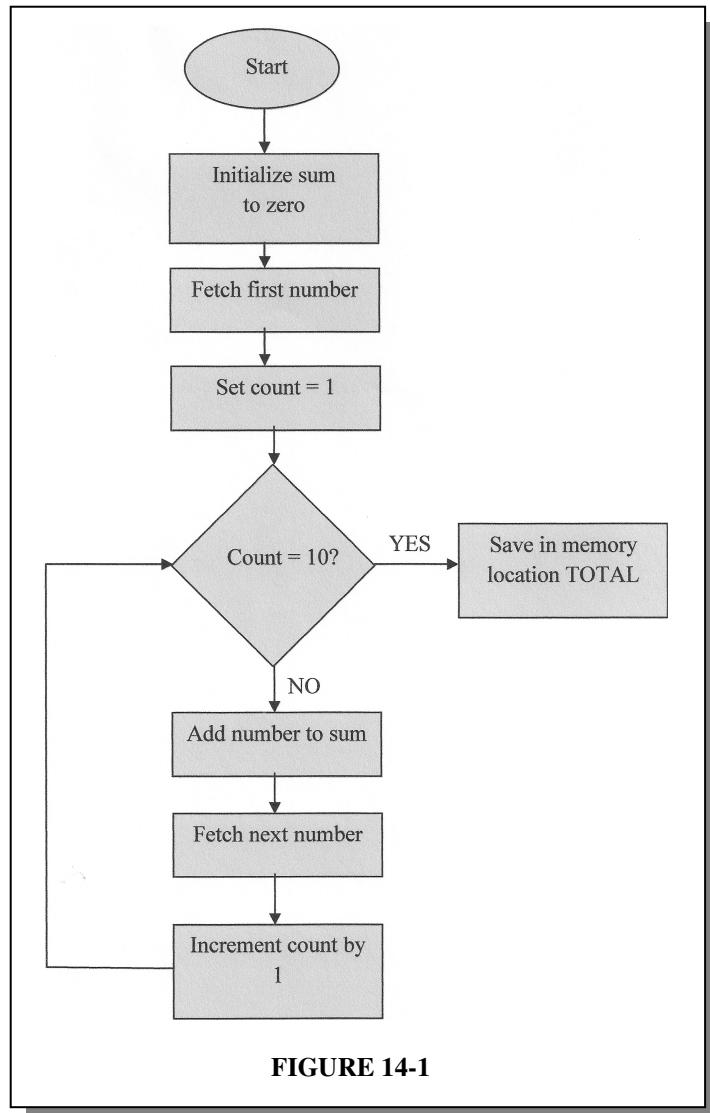
### **Section 14-6 Operating Systems and Hardware**

- 23.** The first group consists of application software, which includes word processors, spreadsheets, computer games, and other programs, written to accomplish some specific task. The second group consists of system software, a major portion of which is the operating system. The operating system manages the system hardware, supervises the running of applications software, provides a standard operating environment for programs in which they can run and interacts with the computer hardware.
- 24.** The three basic duties of a multitasking operating system are to allocate system resources, protect processes and system resources, and provide system services.
- 25.** Two ways in which computers execute more than one process are multitasking and multiprocessing.
- 26.** Running multiple processes can result in corruption of shared memory, corruption of one process's data by another, one process blocking another process's access to resources, and one process monopolizing system resources.

27. MMUs handle memory accessing including memory protection, wait state generation, address translation for virtual memory, and cache control.

### **Section 14-7 Programming**

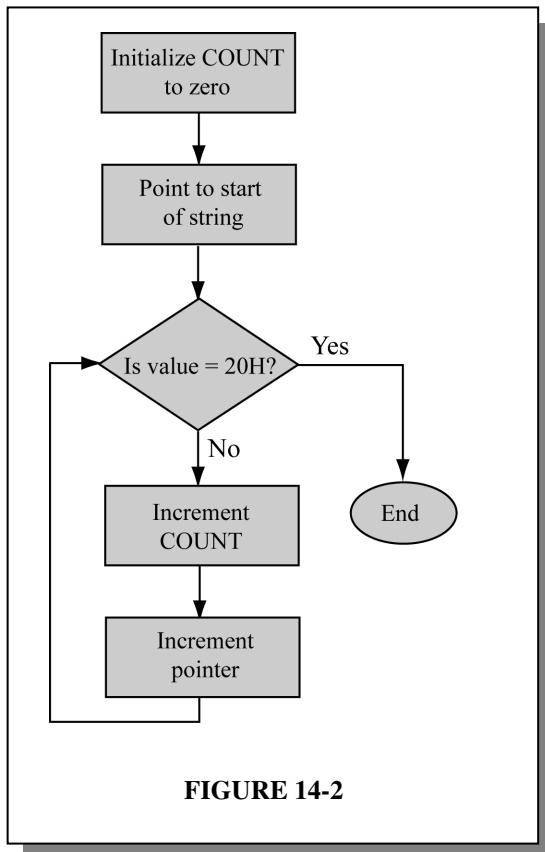
28. An assembler is a program that converts an assembly language program into machine language that can be recognized by the microprocessor.
29. One possible flow chart is shown in Figure 14-1.



**FIGURE 14-1**

## **Chapter 14**

- 30.** The flowchart in Figure 14-2 shows how you can count the number of bytes in a string and place the count in a memory location called COUNT. The string starts at a location named START and 20H (space) to indicate the end.



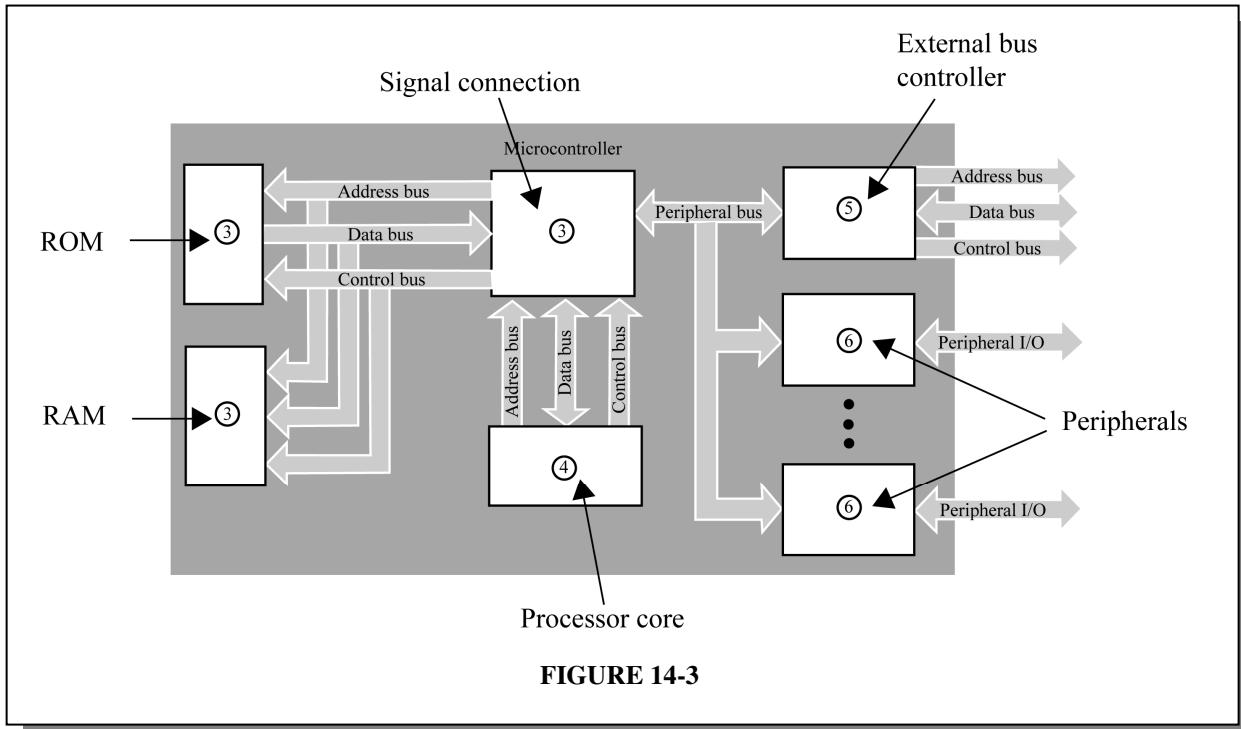
**FIGURE 14-2**

- 31.** Move contents of bx register into ax register.
- 32.** A compiler is a program that compiles or translates a program written in a high-level language and converts it into machine code.

### **Section 14-8 Microcontrollers and Embedded Systems**

- 33.** A microcontroller is a device that combines a microprocessor with common peripheral units.

- 34.** See Figure 14-3.



- 35.** Microcontrollers are widely used in embedded applications because they provide the interface and processing resources required by embedded systems.
- 36.** The microcontroller includes certain peripherals that are external to a microprocessor.
- 37.** An SoC is a system on a chip and has all the components and functions to implement a complete system such as a computer. A microcontroller is similar to a SoC but generally more limited in available functions.
- 38.** The SoC is generally based on ARM architecture.

---

---

## CHAPTER 15 (ON-LINE) INTEGRATED CIRCUIT TECHNOLOGIES

---

### Section 15-1 Basic Operational Characteristics and Parameters

1. No, because the  $V_{OH(min)}$  is less than the  $V_{IH(min)}$ . The gate may interpret 2.2 V as a LOW.
2. Yes, they are compatible because the  $V_{OL(max)}$  is less than the  $V_{IL(max)}$ .
3.  $V_{NH} = V_{OH(min)} - V_{IH(min)} = 2.4 \text{ V} - 2.25 \text{ V} = 0.15 \text{ V}$   
 $V_{NL} = V_{IL(max)} - V_{OL(max)} = 0.65 \text{ V} - 0.4 \text{ V} = 0.25 \text{ V}$
4. The maximum amplitudes equal the noise margins of 0.15 V and 0.25 V.
5. Gate A:  $V_{NH} = 2.4 \text{ V} - 2 \text{ V} = 0.4 \text{ V}$   
 $V_{NL} = 0.8 \text{ V} - 0.4 \text{ V} = 0.4 \text{ V}$   
Gate B:  $V_{NH} = 3.5 \text{ V} - 2.5 \text{ V} = 1 \text{ V}$   
 $V_{NL} = 0.6 \text{ V} - 0.2 \text{ V} = 0.4 \text{ V}$   
Gate C:  $V_{NH} = 4.2 \text{ V} - 3.2 \text{ V} = 1 \text{ V}$   
 $V_{NL} = 0.8 \text{ V} - 0.2 \text{ V} = 0.6 \text{ V}$

**Gate C** has the highest noise margins.

6.  $P_{D(LOW)} = (5 \text{ V})(2 \text{ mA}) = 10 \text{ mW}$   
 $P_{D(HIGH)} = (5 \text{ V})(3.5 \text{ mA}) = 17.5 \text{ mW}$   
 $P_{D(avg)} = \frac{P_{D(LOW)} + P_{D(HIGH)}}{2} = \frac{27.5 \text{ mW}}{2} = 13.75 \text{ mW}$
7. The pulse goes through three gates in the shortest path.  
 $3 \times 4 \text{ ns} = 12 \text{ ns}$
8.  $t_{p(avg)} = \frac{t_{PLH} + t_{PHL}}{2} = \frac{2 \text{ ns} + 3 \text{ ns}}{2} = 2.5 \text{ ns}$
9. Gate A average propagation delay:

$$\frac{t_{PLH} + t_{PHL}}{2} = \frac{1 \text{ ns} + 1.2 \text{ ns}}{2} = 1.1 \text{ ns}$$

Speed/Power product =  $(1.1 \text{ ns})(15 \text{ mW}) = 16.5 \text{ pJ}$

Gate B average propagation delay:

$$\frac{5 \text{ ns} + 4 \text{ ns}}{2} = 4.5 \text{ ns}$$

Speed/Power product =  $(4.5 \text{ ns})(8 \text{ mW}) = 36 \text{ pJ}$

$$\text{Gate C average propagation delay: } \frac{10 \text{ ns} + 10 \text{ ns}}{2} = 10 \text{ ns}$$

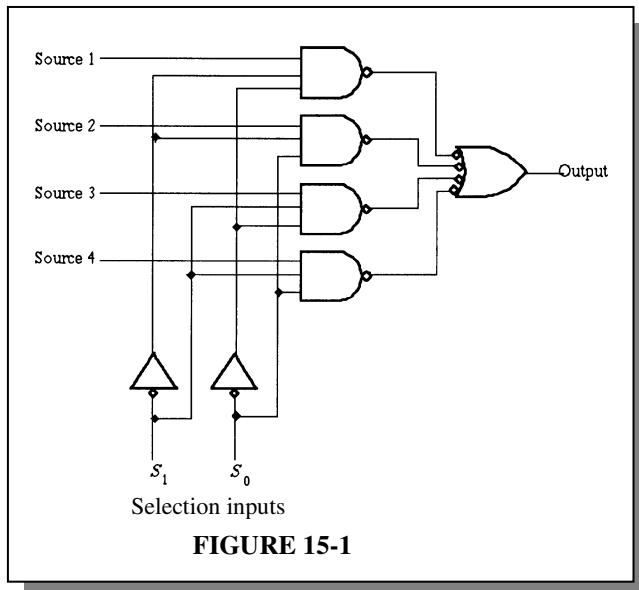
$$\text{Speed/Power product} = (10 \text{ ns})(0.5 \text{ mW}) = 5 \text{ pJ}$$

**Gate C** has the best speed/power product.

10. Gate A can be operated at the highest frequency because it has the shortest propagation delay.
11. G2 is overloaded because it has 12 unit loads.
12. The network in (a) can operate at the highest frequency because the driving gate has fewer loads.

### **Section 15-2 CMOS Circuits**

13. (a) ON                (b) OFF  
 (c) OFF                (d) ON
14. Unused inputs should be connected as follows:  
 Negative-OR gate (NAND) to  $V_{CC}$   
 NAND gate to  $+V_{CC}$   
 NOR gate to ground
15. See Figure 15-1 for another possible approach in addition to circuit given in text answers.



**FIGURE 15-1**

### **Section 15-3 TTL Circuits**

16. (a) ON: high voltage on base forward-biases the base-emitter junction.  
 (b) OFF: insufficient voltage on base to forward-bias the base-emitter junction.  
 (c) OFF: emitter is more positive than the base which reverse-biases the base-emitter junction.  
 (d) OFF: base and emitter at same voltage. No forward bias.

## Chapter 15

17. See Figure 15-2.

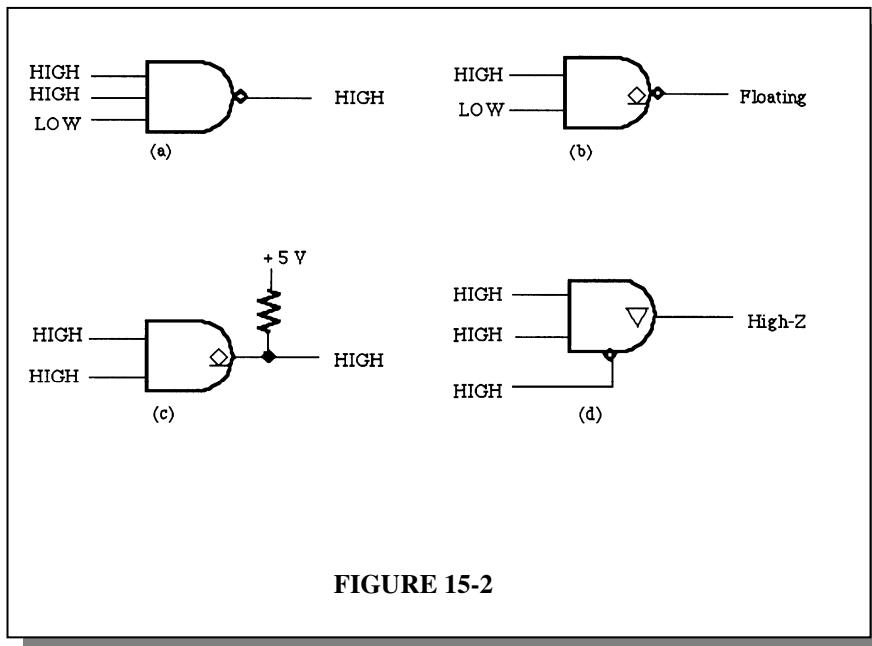


FIGURE 15-2

18. Connect a  $1\text{ k}\Omega$  pull-up resistor to the unused inputs of the two NAND gates. Connect the unused input of the NOR gate to ground. Connect a pull-up resistor to the open collector of the NOR gate (value depends on load).

### Section 15-4 Practical Considerations in the Use of TTL

19. See Figure 15-3.

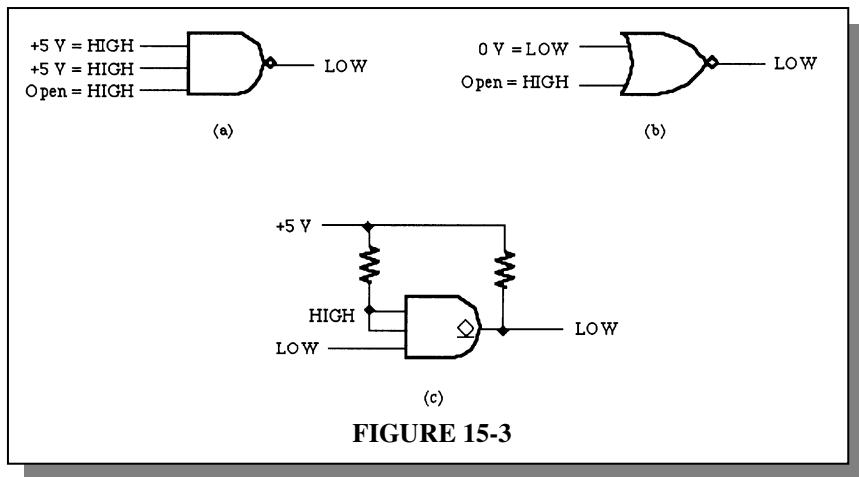


FIGURE 15-3

- 20.** (a) The driving gate output is HIGH, it is sourcing 3 unit loads.  
 $I_T = 3(40 \mu\text{A}) = 120 \mu\text{A}$

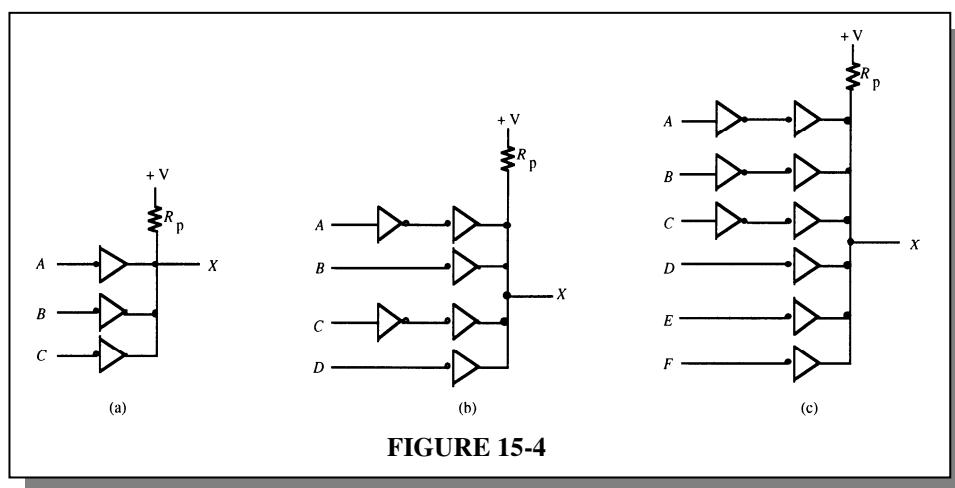
- (b) The driving gate output is LOW, it is sinking current from 2 unit loads.  
 $I_T = 2(-1.6 \text{ mA}) = -3.2 \text{ mA}$

- (c) G1 output is HIGH, it is sourcing 6 unit loads.  
 $I_T = 6(40 \mu\text{A}) = 240 \mu\text{A}$

G2 output is LOW, it is sinking current from 2 unit loads.  
 $I_T = 2(-1.6 \text{ mA}) = -3.2 \text{ mA}$

G3 output is HIGH, it is sourcing 2 unit loads.  
 $I_T = 2(40 \mu\text{A}) = 80 \mu\text{A}$

- 21.** See Figure 15-4. Pull-up resistors of second-level inverters are not shown.



**FIGURE 15-4**

**22.** (a)  $X = ABCD$

(b)  $X = (\overline{ABC})(\overline{DE})(\overline{FG})$

(c)  $X = (\overline{A+B})(\overline{C+D})(\overline{E+F})(\overline{G+H}) = \overline{ABCDEFGH}$

- 23.** Worst case for determining minimum  $R_p$  is when only one gate is sinking all of the current (40 mA maximum).

For 10 UL:  $I_L = 10(1.6 \text{ mA}) = 16 \text{ mA}$

For each gate:  $I_{Rp(max)} = I_{OL(max)} - 16 \text{ mA} = 40 \text{ mA} - 16 \text{ mA} = 24 \text{ mA}$

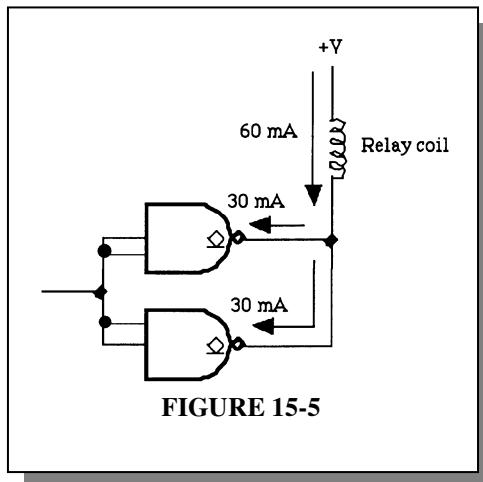
$$V_{Rp} = 5 \text{ V} - 0.25 \text{ V} = 4.75 \text{ V}$$

$$R_{p(min)} = \frac{V_{Rp}}{I_{Rp(max)}} = \frac{4.75 \text{ V}}{24 \text{ mA}} = 198 \Omega$$

$R_{p(min)}$  for (a), (b), and (c) is the same value.

## Chapter 15

24. See Figure 15-5.



### Section 15-5 Comparison of CMOS and TTL Performance

25. **F series:**  $SPP = 3.3 \text{ ns} \times 6 \text{ mW} = 19.8 \text{ pJ}$   
**LS series:**  $SPP = 10 \text{ ns} \times 2.2 \text{ mW} = 22 \text{ pJ}$   
**ALS series:**  $SPP = 7 \text{ ns} \times 1.4 \text{ mW} = 9.8 \text{ pJ}$   
**ABT series:**  $SPP = 3.2 \text{ ns} \times 17 \mu\text{W} = 0.0544 \text{ pJ}$   
**HC series:**  $SPP = 7 \text{ ns} \times 2.75 \mu\text{W} = 0.01925 \text{ pJ}$   
**AC series:**  $SPP = 5 \text{ ns} \times 0.55 \mu\text{W} = 0.00275 \text{ pJ}$   
**AHC series:**  $SPP = 3.7 \text{ ns} \times 2.75 \mu\text{W} = 0.010175 \text{ pJ}$   
**LV series:**  $SPP = 9 \text{ ns} \times 1.6 \mu\text{W} = 0.0144 \text{ pJ}$   
**LVC series:**  $SPP = 4.3 \text{ ns} \times 0.8 \mu\text{W} = 0.00344 \text{ pJ}$   
**ALVC series:**  $SPP = 3 \text{ ns} \times 0.8 \mu\text{W} = 0.0024 \text{ pJ}$

**ALVC** has the best (lowest value) speed-power product. It is, however, misleading to compare CMOS and TTL in terms of SPP because the power of CMOS goes up with frequency.

26. (a) ALVC  
(b) AHC  
(c) AC  
(d) ALVC
27. (a) A and B to X:  $3(3.3 \text{ ns}) = 9.9 \text{ ns}$   
C and D to X:  $2(3.3 \text{ ns}) = 6.6 \text{ ns}$
- (b) A to X1, X2, X3:  $2(7 \text{ ns}) = 14 \text{ ns}$   
B to X1: 7 ns  
C to X2: 7 ns  
D to X3: 7 ns
- (c) A, B to X:  $3(3.7 \text{ ns}) = 11.1 \text{ ns}$   
C, D, to X:  $2(3.7 \text{ ns}) = 7.4 \text{ ns}$

- 28.** (a) HC has an  $f_{\max} = 50 \text{ MHz}$

$$f_{\text{clock}} = \frac{1}{50 \text{ ns}} = 20 \text{ MHz}$$

- (b) LS has an  $f_{\max} = 33 \text{ MHz}$

$$f_{\text{clock}} = \frac{1}{60 \text{ ns}} = 16.7 \text{ MHz}$$

- (c) AHC has an  $f_{\max} = 170 \text{ MHz}$

$$f_{\text{clock}} = \frac{1}{4 \text{ ns}} = 250 \text{ MHz}$$

Since  $f_{\text{clock}} > f_{\max}$  for the AHC flip-flop, the output will be erratic.

### **Section 15-6 Emitter-Coupled Logic (ECL) Circuits**

- 29.** ECL operates with nonsaturated BJTs whereas TTL transistors saturate when turned on.

- 30.** (a) Lowest propagation delay - ECL

- (b) Lowest power - HCMOS

- (c) Lowest speed/power product - HCMOS

*Chapter 15*

## PART 2

*Applied Logic  
Solutions*

---

## CHAPTER 4

### APPLIED LOGIC

---

1. The digit 2 is formed by segments  $a, b, d, e, g$ .
2. The digit 5 is formed by segments  $a, c, d, f, g$ .
3. The letter A is formed by segments  $a, b, c, e, f, g$ .
4. The letter E is formed by segments  $a, d, e, f, g$ .
5. There is no segment common to all digits.
6. There is no segment common to all the letters shown in text Figure 4-46.
7. Segment  $d$  is used in letters b, C, d, and E. The hexadecimal code for each letter is as follows:  
b—1011; c—1100; d—1101; E—1100.

$$d = H_3 \overline{H}_2 H_1 H_0 + H_3 H_2 \overline{H}_1 H_0 + H_3 H_2 \overline{H}_1 H_0 + H_3 H_2 H_1 \overline{H}_0$$

|           |     | $H_1 H_0$ |    |     |     |    |
|-----------|-----|-----------|----|-----|-----|----|
|           |     | $H_3 H_2$ | 00 | 01  | 11  | 10 |
| $H_1 H_0$ | 00  | X         | X  | X   | (X) |    |
|           | 01  | X         | X  | (X) | X   |    |
| 11        | 0   | 0         | 1  | 0   |     |    |
| 10        | (X) | X         | 0  | 1   |     |    |

The minimized expression for segment  $d$  is

$$d = \overline{H}_2 \overline{H}_0 + H_2 H_1 H_0$$

8. Segment  $e$  is used in letters A, b, C, d, and E. The hexadecimal code for each letter is as follows: A—1010; b—1011; c—1100; d—1101; E—1110.

The expression for segment  $e$  is

$$e = H_3 \bar{H}_2 H_1 H_0 + H_3 \bar{H}_2 H_1 H_0 + H_3 H_2 \bar{H}_1 \bar{H}_0 + H_3 H_2 H_1 \bar{H}_0$$

|           |         | $H_1 H_0$ |    |    |
|-----------|---------|-----------|----|----|
|           |         | 00        | 01 | 11 |
| $H_3 H_2$ | 00      | X X X X   |    |    |
|           | 01      | X X X X   |    |    |
| 11        | 0 0 1 0 |           |    |    |
| 10        | X X 0 0 |           |    |    |

The minimized expression for segment  $e$  is

$$e = H_2 H_1 H_0$$

9. Segment  $f$  is used in letters A, b, C, and E. The hexadecimal code for each letter is as follows: A—1010; b—1011; C—1100; E—1110.

The expression for segment  $f$  is

$$f = H_3 \bar{H}_2 H_1 \bar{H}_0 + H_3 \bar{H}_2 H_1 H_0 + H_3 H_2 \bar{H}_1 \bar{H}_0 + H_3 H_2 H_1 \bar{H}_0$$

|           |         | $H_1 H_0$ |    |    |
|-----------|---------|-----------|----|----|
|           |         | 00        | 01 | 11 |
| $H_3 H_2$ | 00      | X X X X   |    |    |
|           | 01      | X X X X   |    |    |
| 11        | 0 1 1 0 |           |    |    |
| 10        | X X 0 0 |           |    |    |

$$f = H_2 H_0$$

The minimized expression for segment  $f$  is

$$f = H_2 H_0$$

10. Segment  $g$  is used in letters A, b, d, and E. The hexadecimal code for each letter is as follows:  
 A—1010; b—1011; d—1101; E—1110.

The expression for segment  $g$  is

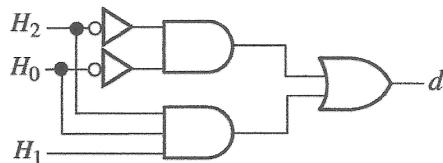
$$g = H_3 \overline{H}_2 H_1 \overline{H}_0 + H_3 \overline{H}_2 H_1 H_0 + H_3 H_2 \overline{H}_1 H_0 + H_3 H_2 H_1 \overline{H}_0$$

|  |  | $H_1 H_0$ | 00 | 01 | 11 | 10 |   |
|--|--|-----------|----|----|----|----|---|
|  |  | $H_3 H_2$ | 00 | X  | X  | X  | X |
|  |  | 01        | X  | X  | X  | X  | X |
|  |  | 11        | 1  | 0  | 1  | 0  | 0 |
|  |  | 10        | X  | X  | 0  | 0  | 0 |

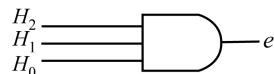
The minimized expression for segment  $g$  is

$$g = H_2 H_1 H_0 + \overline{H}_1 \overline{H}_0$$

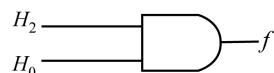
11. The location for segment  $d$  is



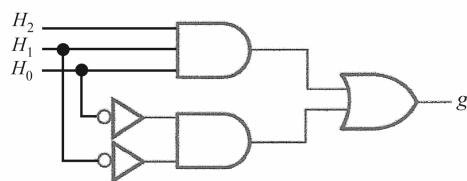
12. The logic for segment  $e$  is



13. The logic for segment  $f$  is



14. The logic for segment  $g$  is



```

15. entity SEGLOGIC is
 port (H0, H1, H2: in bit; SEGd: out bit);
end entity SEGLOGIC;
architecture Logic Function of SEGLOGIC is;
begin
 SEGd <= (not H2 and not H0) or (H0 and H1 and H2);
end architecture Logic Function;

entity SEGLOGIC is
 port (H0, H1, H2: in bit; SEGe: out bit);
end entity SEGLOGIC;
architecture Logic Function of SEGLOGIC is;
begin
 SEGe <= H0 and H1 and H2;
end architecture Logic Function;

entity SEGLOGIC is
 port (H0, H2: in bit; SEGf: out bit);
end entity SEGLOGIC;
architecture Logic Function of SEGLOGIC is;
begin
 SEGf <= H0 and H2;
end architecture Logic Function;

entity SEGLOGIC is
 port (H0, H1, H2: in bit; SEGg: out bit);
end entity SEGLOGIC;
architecture Logic Function of SEGLOGIC is;
begin
 SEGg <= (not H1 and not H0) or (H0 and H1 and H2);
end architecture Logic Function;

```

---

## CHAPTER 5

### APPLIED LOGIC

---

1. The two invalid conditions in text Table 5-6 are not possible because if the maximum level,  $L_{MAX}$ , has been reached as indicated by a 1, the minimum level  $L_{MIN}$  also must have been reached, but the 0 indicates that it has not.
2. The inlet valve is open under *three* conditions as indicated by  $V_{INLET} = 1$ .
3. The inlet valve turns off when the maximum level is reached.
4. The standard SOP expression for  $V_{inlet}$  is

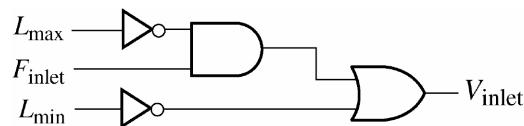
$$V_{inlet} = \bar{L}_{max} \bar{L}_{min} \bar{F}_{inlet} + \bar{L}_{max} \bar{L}_{min} F_{inlet} + \bar{L}_{max} L_{min} F_{inlet}$$

|                   | $F_{inlet}$ | 0 | 1 |
|-------------------|-------------|---|---|
| $L_{max} L_{min}$ | 00          | 1 | 1 |
|                   | 01          |   | 1 |
|                   | 11          |   |   |
| 10                | X           | X |   |

The simplified  $V_{inlet}$  expression is correct.

$$V_{inlet} = \bar{L}_{min} + \bar{L}_{max} \bar{F}_{inlet}$$

5. The simplified logic for the inlet valve control:



6. The additional input to the outlet valve control is  $T$  for temperature. The corn syrup must be at a specified temperature for proper viscosity before the syrup can be released into the mixing vat.
7. The outlet valve is open under two conditions as specified by the 1s in text Table 5-7.
8. Once the tank starts draining, the outlet valve remains open (on) until the minimum level is reached.

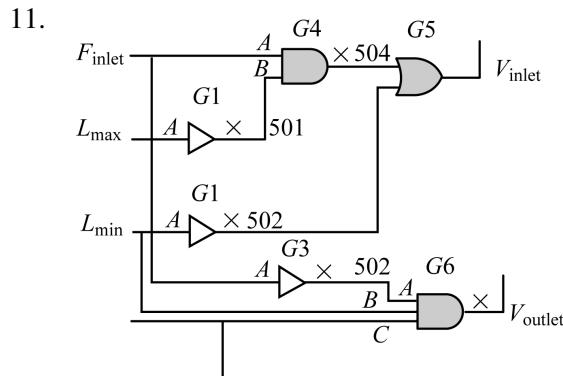
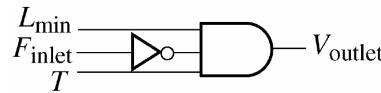
9. The standard SOP expression for  $V_{\text{outlet}}$  is

$$V_{\text{outlet}} = \bar{L}_{\max} L_{\min} \bar{F}_{\text{inlet}} T + L_{\max} L_{\min} \bar{F}_{\text{inlet}} T$$

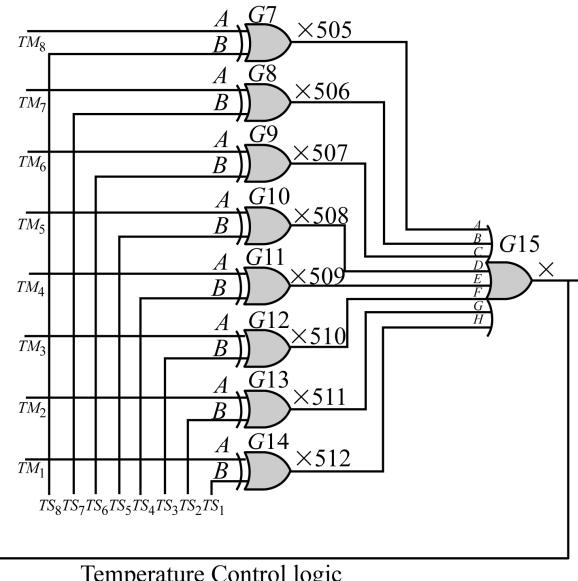
| $L_{\max} L_{\min}$ | $F_{\text{inlet}} T$ | 00 | 01 | 11 | 10 |
|---------------------|----------------------|----|----|----|----|
| 00                  |                      |    |    |    |    |
| 01                  |                      | 1  |    |    |    |
| 11                  |                      | 1  |    |    |    |
| 10                  | X                    | X  | X  | X  | X  |

The simplified  $V_{\text{outlet}}$  expression is correct.

10. The simplified logic for the outlet valve control:



Tank control logic



Temperature Control logic

```

entity TankControl is
 port (Finlet, Lmax, Lmin, TS1, TS2, TS3, TS4, TS5, TS6, TS7, TS8, TM1, TM2, TM3, TM4,
 TM5, TM6, TM7, TM8: in bit; Vinlet, Voutlet, T: out bit);
end entity TankControl;
architecture ValveTempLogic of TankControl is

```

```

--Component declaration for inverter
component NOT is
 port (A: in bit; Y out bit);
end component NOT;
--Component declaration for 2-input AND gate
component AND2 is
 port (A, B: in bit; Y out bit);
end component AND2;
--Component declaration for 3-input AND gate
component AND3 is
 port (A, B, C: in bit; Y out bit);
end component AND3;
--Component declaration for 2-input OR gate
component OR2 is
 port (A, B: in bit; Y out bit);
end component OR2;
--Component declaration for 8-input OR gate
component OR8 is
 port (A, B, C, D, E, F, G, H: in bit; Y out bit);
end component OR8;
--Component declaration for XOR gate
component XOR is
 signal (S01, S02, S03, S04, S05, S06, S07, S08, S09, S10, S11, S12, S13, S14, S15: bit;
bgin
--Vinlet
G1: NOT port map (A=>Lmax, X=>S01);
G2: NOT port map (A=>Lmax, X=>S02);
G4: AND2 port map (A=>Finlet, B=>S01, X=>S04);
G5: OR2 port map (A=>S04, B=>S02, X=>Vinlet);
--Voutlet
G3: NOT port map (A=>Finlet, X=>S03);
G6: AND3 port map (A=>S03, B=>Lmin, C=>T, X=>Voutet);
--Temperature control
G7: XOR port map (A=>TM8, B=>TS8, X=>S05);
G8: XOR port map (A=>7, B=>TS7, X=>S06);
G9: XOR port map (A=>TM6, B=>TS6, X=>S07);
G10: XOR port map (A=>TM5, B=>TS5, X=>S08);
G11: XOR port map (A=>TM4, B=>TS4, X=>S09);
G12: XOR port map (A=>TM3, B=>TS3, X=>S10);
G13: XOR port map (A=>TM2, B=>TS2, X=>S11);
G14: XOR port map (A=>TM1, B=>TS1, X=>S12);
G15: OR8 port map (A=>S05, B=>S06, C=>S07, D=>S08, E=>S09, F=>S10, G=>S11, H=>S12
X=>T);
end architecture ValveTempLogic;

```

### **Putting your Knowledge to Work**

This assumes that the syrup is acceptable as long as its temperature is not more than 9° below the specified temperature. The temperature control circuit could be modified by eliminating the LSD in the BCD code for the measured temperature.

---

## CHAPTER 6

### APPLIED LOGIC

---

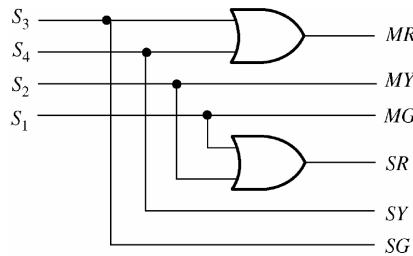
1. The system remains in the first state (00) for 25 s if there is a vehicle on the side street or as long as there is not vehicle on the side street.
2. The system remains in the fourth state (10) for 4 s.
3. The expression for the condition producing a transition from the first state to the second state is

$$\bar{T}_L V_s$$

4. The expression for the condition that keeps the system in the second state is

$$T_S$$

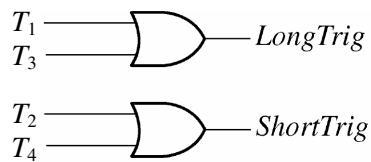
5. The diagram for the light output logic:



6. The truth tabel for the light output logic:

| Inputs |       |       |       | Outputs |      |      |      |      |      |
|--------|-------|-------|-------|---------|------|------|------|------|------|
| $L_4$  | $L_3$ | $L_2$ | $L_1$ | $MR$    | $MY$ | $MG$ | $SR$ | $SY$ | $SG$ |
| 0      | 0     | 0     | 1     | 0       | 0    | 1    | 1    | 0    | 0    |
| 0      | 0     | 1     | 0     | 0       | 1    | 0    | 1    | 0    | 0    |
| 0      | 1     | 0     | 0     | 1       | 0    | 0    | 0    | 0    | 1    |
| 1      | 0     | 0     | 0     | 1       | 0    | 0    | 0    | 1    | 0    |

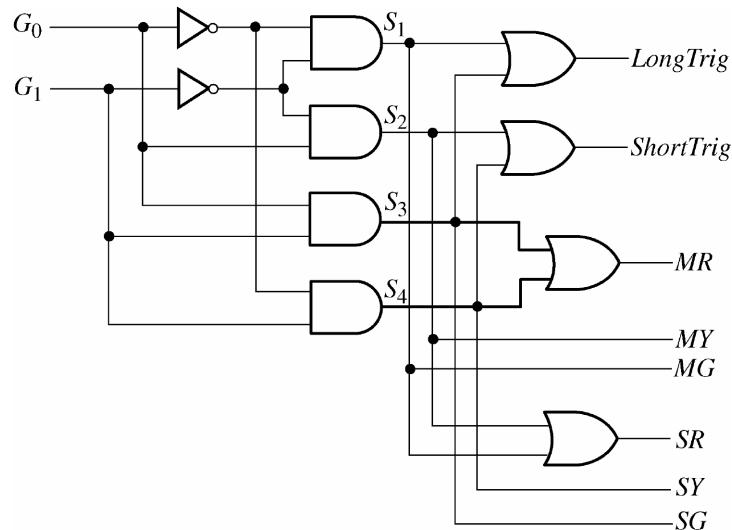
7. The diagram for the trigger logic:



8. The truth table for the trigger logic:

| Inputs |       |       |       | Outputs    |             |
|--------|-------|-------|-------|------------|-------------|
| $T_4$  | $T_3$ | $T_2$ | $T_1$ | $LongTrig$ | $ShortTrig$ |
| 0      | 0     | 0     | 1     | 1          | 0           |
| 0      | 0     | 1     | 0     | 0          | 1           |
| 0      | 1     | 0     | 0     | 1          | 0           |
| 1      | 0     | 0     | 0     | 0          | 1           |

9. The diagram of the complete combinational logic:



Inverters: 74HC04; input pins: 1, 3; output pins: 2, 4

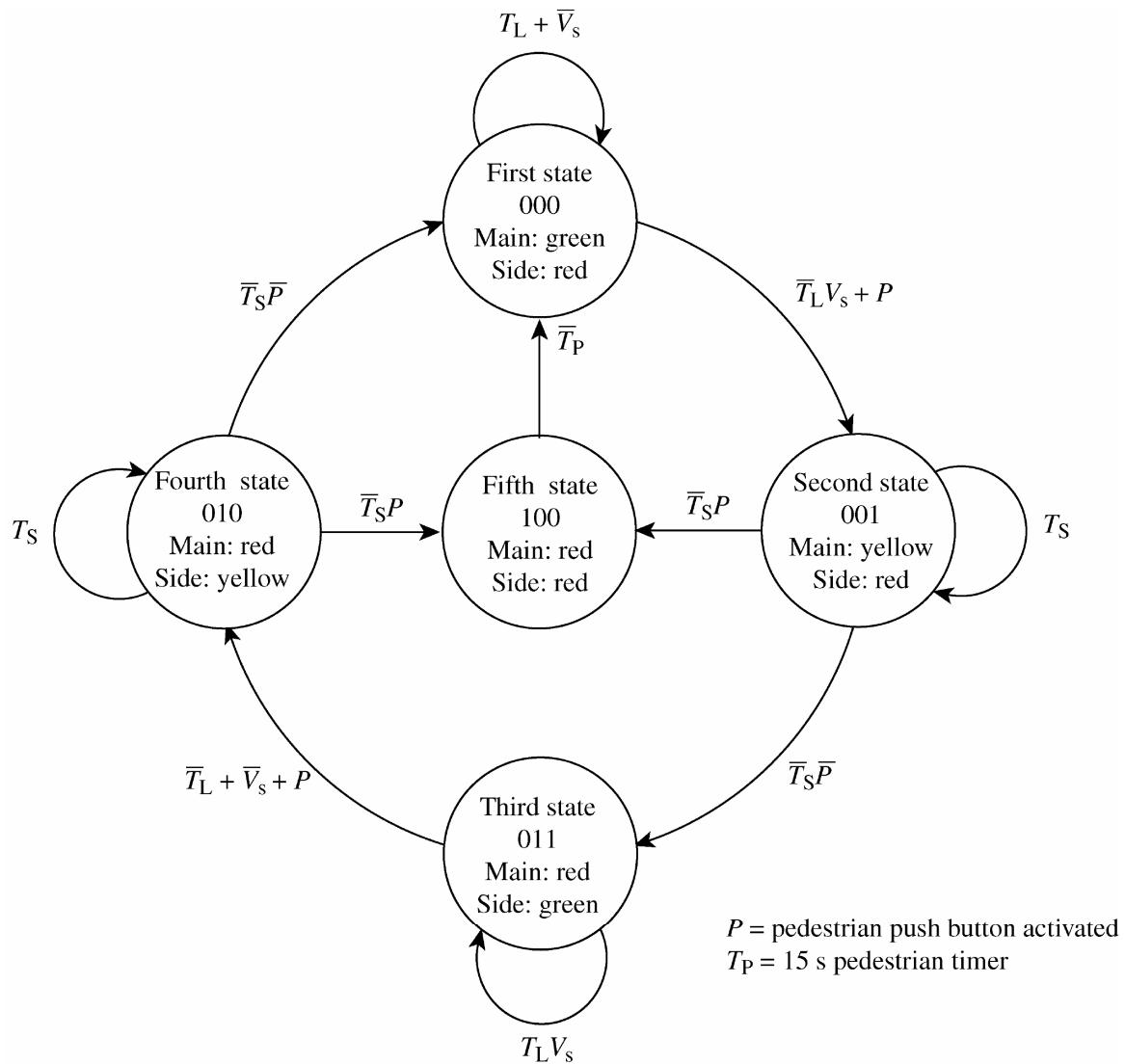
AND gates: 74HC08; input pins: 1, 2, 4, 5, 9, 10, 12, 13  
output pins: 3, 6, 8, 11;

OR gates: 74HC32; input pins: 1, 2, 4, 5, 9, 10, 12, 13  
output pins: 3, 6, 8, 11

$V_{CC}$  = pin 14, GND = 7 (all)

## Putting Your Knowledge to Work

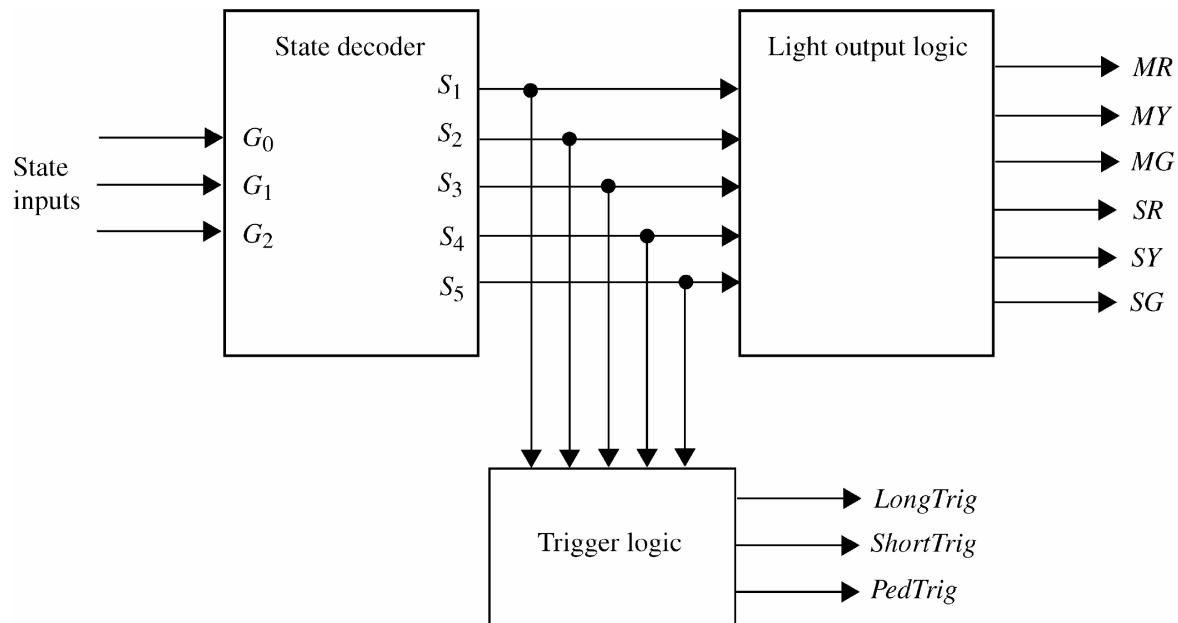
- (a) One approach is shown by the modified state diagram.



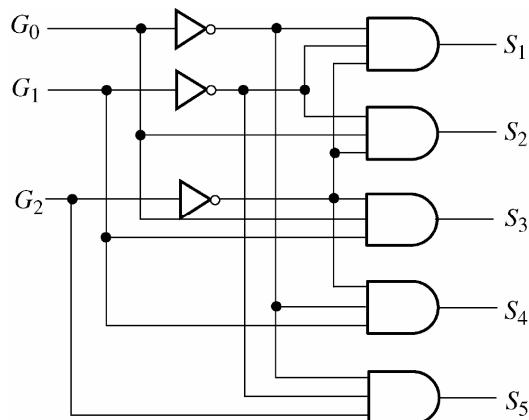
When a pedestrian pushes the button, one of the following sequences occurs:

- If a system is in first state (000), it goes immediately to second state (001) for 4 s and then to fifth state (100) for 15 s and then back to first state (000).
- If a system is in third state (011), it goes immediately to fourth state (010) for 4 s and then to fifth state (100) for 15 s and then back to first state (000).
- If a system is in either second or fourth states, the short timer is retriggered and the system remains in that state for another 4 s before going to the fifth state.

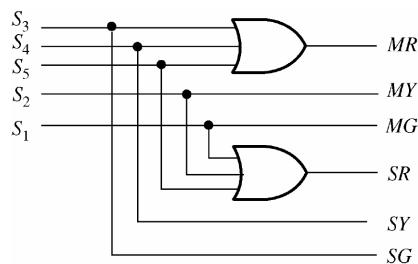
(b) The modified combinational logic block diagram:



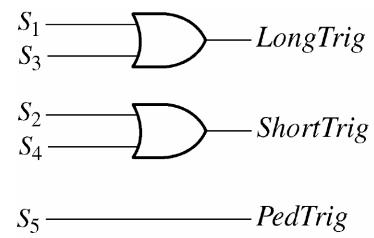
The modified state decoder logic:



The modified light output logic:



The modified trigger logic:



---

## CHAPTER 7

### DIGITAL SYSTEM APPLICATION

---

1. The resistor and capacitor values for the 25 s timer are determined as follows.

Let  $C_1 = 150 \mu\text{F}$

$$t_w = 1.1R_1C_1$$

$$R_1 = \frac{t_w}{1.1C_1} = \frac{25 \text{ s}}{1.1(100 \mu\text{F})} = 227 \text{ k}\Omega$$

Other combinations are possible.

2. The resistor and capacitor values for the 4 s timer are determined as follows.

Let  $C_1 = 100 \mu\text{F}$

$$t_w = 1.1R_1C_1$$

$$R_1 = \frac{4 \text{ s}}{1.1(100 \mu\text{F})} = 36.4 \text{ k}\Omega$$

Other combinations are possible.

3. The purpose of the frequency divider is to produce a 1 HZ clock for the timer circuits.

4. The Boolean rule used is  $A + \bar{A} = 1$ .

In this case, the terms  $G_1G_0$  were factored out leaving  $T_S + \bar{T}_S$ :

$$\bar{G}_1G_0 + (T_S + \bar{T}_S) = \bar{G}_1G_0(1) = \bar{G}_1G_0$$

5.  $D_0$  is reduced by first expanding to standard SOP form:

$$\begin{aligned} D_0 &= \bar{G}_1\bar{G}_0\bar{T}_L V_s + \bar{G}_1G_0 + G_1G_0T_L V_s \\ &= \bar{G}_1\bar{G}_0\bar{T}_L V_s + \bar{G}_1G_0\bar{T}_L \bar{V}_s + \bar{G}_1G_0\bar{T}_L V_s + \bar{G}_1G_0T_L \bar{V}_s + \bar{G}_1G_0T_L V_s + G_1G_0T_L V_s \end{aligned}$$

| $G_1G_0$ | $T_L V_s$ | 00  | 01  | 11  | 10 |
|----------|-----------|-----|-----|-----|----|
| 00       |           |     | (1) |     |    |
| 01       | (1)       | (1) | (1) | (1) |    |
| 11       |           |     |     | (1) |    |
| 10       |           |     |     |     |    |

The reduced expression is

$$D_0 = \bar{G}_1G_0 + \bar{G}_1\bar{T}_L V_s + G_0T_L V_s$$

6.  $D_1$  has five variables and is reduced by applying Boolean rules:

$$\begin{aligned} D_1 &= \bar{G}_1 G_0 \bar{T}_S + G_1 G_0 T_L V_S + G_1 G_0 \bar{T}_L + G_1 G_0 \bar{V}_S + G_1 \bar{G}_0 T_S \\ &= \bar{G}_1 G_0 \bar{T}_S + G_1 G_0 (T_L V_S + \bar{T}_L) + G_1 G_0 \bar{V}_S + G_1 \bar{G}_0 T_S \end{aligned}$$

Applying the rule 11:  $A + AB = A + B$

$$\begin{aligned} D_1 &= \bar{G}_1 G_0 \bar{T}_S + G_1 G_0 (V_S + \bar{T}_L) + G_1 G_0 \bar{V}_S + G_1 \bar{G}_0 T_S \\ D_1 &= \bar{G}_1 G_0 \bar{T}_S + G_1 G_0 V_S + G_1 G_0 \bar{T}_L + G_1 G_0 \bar{V}_S + G_1 \bar{G}_0 T_S \\ &= \bar{G}_1 G_0 \bar{T}_S + G_1 G_0 (V_S + \bar{T}_L + \bar{V}_S) + G_1 \bar{G}_0 T_S \end{aligned}$$

Applying the rules 2 and 6:  $A + 1 = 1$  and  $A = A = 1$

$$D_1 = \bar{G}_1 G_0 \bar{T}_S + G_1 G_0 (1) + G_1 \bar{G}_0 T_S = \bar{G}_1 G_0 \bar{T}_S + G_1 G_0 T_S + G_1 G_0 \bar{T}_S + G_1 \bar{G}_0 T_S$$

|           |       |   |   |
|-----------|-------|---|---|
| $G_1 G_0$ | $T_S$ | 0 | 1 |
| 00        |       |   |   |
| 01        |       | 1 |   |
| 11        |       | 1 | 1 |
| 10        |       |   | 1 |

The reduced expression is

$$D_1 = G_0 \bar{T}_S + G_1 T_S$$

7. The expression agrees with text Figure 8-64.

### Putting your Knowledge to Work

The combinational logic portion of the system was modified in Chapter 6 to accommodate a pedestrian input to turn both lights red for 15 s. To accomplish this exercise, the student must recognize that the timing circuits and the sequential logic must also be modified.

**Timing circuit modification:** An additional 555 timer configured as a one-shot with a 15 s output pulse is added:

Let  $C_1 = 100 \mu\text{F}$

$$t_W = 1.1 R_1 C_1$$

$$R_1 = \frac{15 \text{ s}}{1.1(100 \mu\text{F})} = 136 \text{ k}\Omega$$

**Sequential logic modificaiton:** A third flip-flop is added. First, the next-state table is modified to accommodate the pedestrian input (P).

| PRESENT STATE |       |       | NEXT STATE |       |       | INPUT CONDITIONS            | FF INPUTS |       |       |
|---------------|-------|-------|------------|-------|-------|-----------------------------|-----------|-------|-------|
| $Q_2$         | $Q_1$ | $Q_0$ | $Q_2$      | $Q_1$ | $Q_0$ |                             | $D_2$     | $D_1$ | $D_0$ |
| 0             | 0     | 0     | 0          | 0     | 0     | $T_L + \bar{V}_s$           | 0         | 0     | 0     |
| 0             | 0     | 0     | 0          | 0     | 1     | $\bar{T}_L V_s + P$         | 0         | 0     | 1     |
| 0             | 0     | 1     | 0          | 0     | 1     | $T_s$                       | 0         | 0     | 1     |
| 0             | 0     | 1     | 0          | 1     | 1     | $\bar{T}_s \bar{P}$         | 0         | 1     | 1     |
| 0             | 0     | 1     | 1          | 0     | 0     | $\bar{T}_s P$               | 1         | 0     | 0     |
| 0             | 1     | 1     | 0          | 1     | 1     | $T_L V_s$                   | 0         | 1     | 1     |
| 0             | 1     | 1     | 0          | 1     | 0     | $\bar{T}_L + \bar{V}_s + P$ | 0         | 1     | 0     |
| 0             | 1     | 0     | 0          | 1     | 0     | $T_s$                       | 0         | 1     | 0     |
| 0             | 1     | 0     | 0          | 0     | 0     | $\bar{T}_s \bar{P}$         | 0         | 0     | 0     |
| 0             | 1     | 0     | 1          | 0     | 0     | $\bar{T}_s P$               | 1         | 0     | 0     |
| 1             | 0     | 0     | 0          | 0     | 0     | $\bar{T}_p$                 | 0         | 0     | 0     |

$$\begin{aligned} D_0 &= \bar{G}_2 \bar{G}_1 \bar{G}_0 + (\bar{T}_L V_s + P) + \bar{G}_2 \bar{G}_1 G_0 T_S + \bar{G}_2 \bar{G}_1 G_0 \bar{T}_S \bar{P} + \bar{G}_2 G_1 G_0 T_L V_s \\ &= \bar{G}_2 \bar{G}_1 \bar{G}_0 \bar{T}_L V_s + \bar{G}_2 \bar{G}_1 \bar{G}_0 P + \bar{G}_2 \bar{G}_1 G_0 T_S + \bar{G}_2 \bar{G}_1 G_0 \bar{T}_S \bar{P} + \bar{G}_2 G_1 G_0 T_L V_s \end{aligned}$$

$$\begin{aligned} D_1 &= \bar{G}_2 \bar{G}_1 G_0 \bar{T}_S \bar{P} + \bar{G}_2 G_1 G_0 T_L V_s + \bar{G}_2 G_1 G_0 (\bar{T}_L + \bar{V}_s + P) + \bar{G}_2 G_1 \bar{G}_0 \bar{T}_S \\ &= \bar{G}_2 \bar{G}_1 G_0 \bar{T}_S \bar{P} + \bar{G}_2 G_1 G_0 T_L V_s + \bar{G}_2 G_1 G_0 \bar{T}_L + \bar{G}_2 G_1 G_0 \bar{V}_s + \bar{G}_2 G_1 G_0 P + \bar{G}_2 G_1 \bar{G}_0 \bar{T}_S \end{aligned}$$

$$D_2 = \bar{G}_2 \bar{G}_1 \bar{G}_0 \bar{T}_S P + \bar{G}_2 G_1 \bar{G}_0 \bar{T}_S P$$

Notice that the expressions contain up to seven variables. Karnaugh map simplification would not be feasible. If you wish to minimize the expression, the Quine-McCluskey method can be used but will be left as an exercise that can be assigned to students.

$D_0$  will take three 5-input AND (or NAND) gates, two 4-input AND (or NAND) gates, and one 5-input OR (or NAND) gate.

$D_1$  will take two 5-input AND (or NAND) gates, two 4-input AND (or NAND) gates, and one 6-input OR (or NAND).

$D_2$  will take two 5-input AND (or NAND) gates and one 2-input OR (or NAND) gate.

---

## **CHAPTER 8**

### **APPLIED LOGIC**

---

1. The BCD code sequence for 4739 is 0100, 0111, 0011, 1001.
2. The state of shift register C after two correct code digits are entered is 00000100.
3. The purpose of the OR gate is to produce a trigger when a key is pressed in order to generate the clock pulses for the system.
4. When the digit 4 is entered, 0100, appears on the outputs of register A.

#### **Putting Your Knowledge to Work**

The security code logic can be modified for a 5-digit code by moving the HIGH parallel input of shift register C back one position. It would then take five clock pulses to shift the 1 to the output.

---

## **CHAPTER 9**

### **APPLIED LOGIC**

---

1. The floor counter contains the number of the current floor where the elevator is located. The counter increments or decrements each time the elevator goes to another floor.
2. The system is in the WAIT state when it is not transporting passengers. When a floor call signal is received the elevator leaves the WAIT state and goes to the calling floor. Once the passengers have left, the door is closed and the elevator waits for another call.
3. When the floor number in the floor counter equals the number of the calling or requested floor, the comparator issues an equal signal causing the elevator to stop.
4. This is a simplified system that allows only one call or request at a time. It cannot respond to multiple calls or requests.

#### **Putting Your Knowledge to Work**

To modify the elevator for ten floors, the floor counter and call request register must be four bits. The comparator must be able to handle four bit numbers. The display decoder must accept four bits.

---

# CHAPTER 10

## APPLIED LOGIC

---

### Putting Your Knowledge to Work

The modified portions of the elevator and component codes for 10 floors:

#### ELEVATOR.vhd

```
line 4: entity - port(CallCode, PanelCode: in std_logic_vector(3 downto 0);
line 18: FLRCALLCOMPARATOR port(CallCode, PanelCode: in std_logic_vector(3 downto 0);
lines 24,25: CODEREGISTER FlrCodeIn: in std_logic_vector(0 to 3);
 FlrCodeOut; out std_logic_vector(0 to 3));
line 39: signal FRCNT, FRCLOUT, FRIN: std_logic_vector(0 to 3):="0000";

entity CODEREGISTER is
port(clk: in std_logic;
 FlrCodeIn: in std_logic_vector(0 to 3);
 FlrCodeOut: out std_logic_vector(0 to 3));
end entity CODEREGISTER;

entity FLRCALLCOMPARATOR is
port(FlrCodeCall, FlrCodeCnt: in std_logic_vector(3 downto 0);
 Up, Down, Stop: inout std_logic);
end entity FLRCALLCOMPARATOR;

entity FLOORCOUNTER is
port(UP, DOWN, Sensor: in std_logic;
 FLRCODE: out std_logic_vector(3 downto 0));
end entity FLOORCOUNTER;

entity SevenSegment is
port(a,b,c,d,e,f,g: out std_logic;
 H0,H1,H2,H3: inout std_logic);
end entity SevenSegment;

architecture SevenSegmentBehavior of SevenSegment is
begin
 a <= H1 or H3 or (H2 and H0) or (not H2 and not H0);
 b <= not H2 or (not H0 and not H1) or (H0 and H1);
 c <= H0 or not H1 or H2;
 d <= H3 or (not H0 and not H2) or (not H2 and H1) or
 (H1 and not H0) or (H2 and not H1 and H0);
 e <= (not H0 and not H2) or (H1 and not H0);
 f <= (not H1 and H2) or (not H1 and not H0) or (H2 and not H0) or H3;
 g <= (not H2 and H1) or (H1 and not H0) or (H2 and not H1) or H3;
end architecture SevenSegmentBehavior;
```



# PART 3

Laboratory Solutions for  
*Experiments in*  
*Digital Fundamentals*

**Eleventh Edition**

**David Buchla**

**Doug Joksch**

## Table of Contents

|                                                                     |                                     |
|---------------------------------------------------------------------|-------------------------------------|
| Multisim Simulation Results .....                                   | 253                                 |
| Experiment 1: Basic Laboratory Instruments .....                    | 254                                 |
| Experiment 2: Constructing a Logic Probe.....                       | 256                                 |
| Experiment 3: Number Systems: .....                                 | <b>Error! Bookmark not defined.</b> |
| Experiment 4: Logic Gates: .....                                    | 259                                 |
| Experiment 5: More Logic Gates: (TTL) .....                         | 261                                 |
| Experiment 6: Interpreting Manufacturer's Data Sheets:.....         | 264                                 |
| Experiment 7: Boolean Laws and DeMorgan's Theorem.....              | 267                                 |
| Experiment 8: Logic Circuit Simplification .....                    | 270                                 |
| Experiment 9: The Perfect Pencil Machine .....                      | <b>Error! Bookmark not defined.</b> |
| Experiment 10: The Molasses Tank .....                              | 276                                 |
| Experiment 11 Adder and Magnitude Comparator.....                   | 278                                 |
| Experiment 12: Combinational Logic Using Multiplexers.....          | 279                                 |
| Experiment 13: Combinational Logic Using Demultiplexers .....       | 281                                 |
| Experiment 14: The D Latch and D Flip-Flop.....                     | 282                                 |
| Experiment 15: The Fallen Carton Detector.....                      | 283                                 |
| Experiment 16: The J-K Flip-Flop .....                              | 284                                 |
| Experiment 17: One Shots and Astable Multivibrators .....           | 285                                 |
| Experiment 18: Shift Register Counters .....                        | 286                                 |
| Experiment 19: Application of Shift Register Circuits.....          | 288                                 |
| Experiment 20: The Baseball Scoreboard .....                        | 291                                 |
| Experiment 21: Asynchronous Counters .....                          | 292                                 |
| Experiment 22: Analysis of Synchronous Counters with Decoding ..... | 295                                 |
| Experiment 23: Design of Synchronous Counters.....                  | 297                                 |
| Experiment 24: The Traffic Light Controller .....                   | 299                                 |
| Experiment 25: Semiconductor Memories .....                         | 300                                 |
| Experiment 26: D/A and A/D Conversion.....                          | 301                                 |
| Experiment 27: Applications of Bus Systems .....                    | 302                                 |

## Multisim Simulation Results

There are recent Multisim files selected experiments on the companion website. The Multisim suffix is different for the different versions. The naming convention for all files is EXP-xxnf for files with no fault (“xx” refers to the experiment number). The “nf” in the file name is replaced with f1 and f2 for files with hidden faults. The circuit restrictions password that will allow faults to be revealed is **pldlm** for all Multisim versions.

# Experiment 1: Basic Laboratory Instruments

## Data and Observations

Data and the number of significant figures will vary according to signal generator and measurement equipment. Sample (measured) data is shown.

**TABLE 1-1**

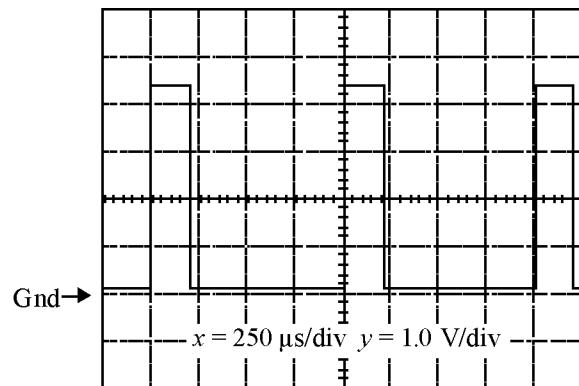
|                         |                 |
|-------------------------|-----------------|
| Voltage Setting = 5.0 V | Voltage Reading |
| Power Supply meter      | 5.0 V           |
| DMM                     | 5.02 V          |
| Oscilloscope            | 5.04 V          |

**TABLE 1-2**

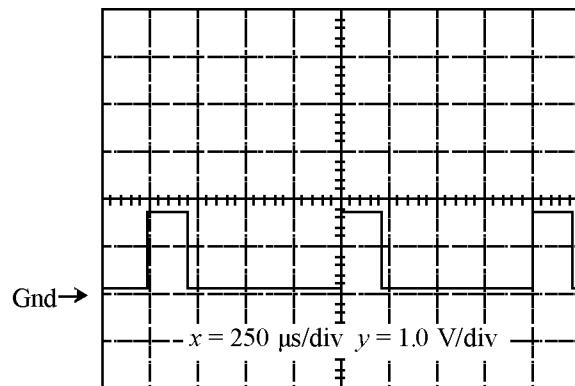
| Function Generator Parameters (at 1.0 kHz) | Measured Values |
|--------------------------------------------|-----------------|
| Pulse Width                                | 197 $\mu$ s     |
| Period                                     | 1.00 ms         |
| Amplitude                                  | 4.3 V           |

**TABLE 1-3**

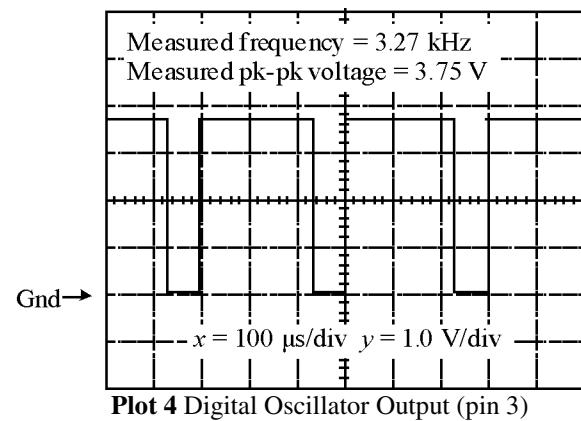
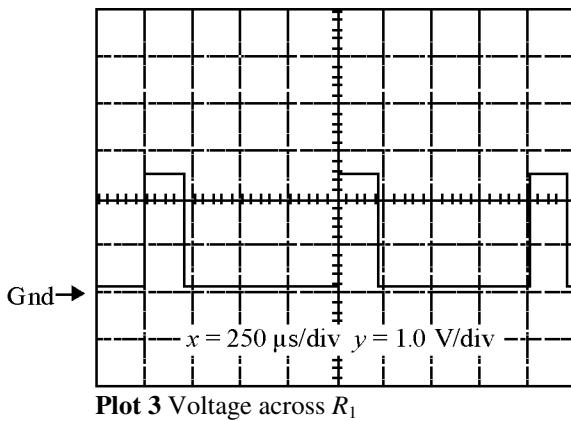
| Step | Digital Oscillator Parameters | Measured Values |
|------|-------------------------------|-----------------|
| 12   | Period                        | 306 $\mu$ s     |
|      | Duty cycle                    | 78%             |
|      | Amplitude                     | 3.75 V          |
|      | Frequency                     | 3.27 kHz        |
| 13   | Period                        | 352 ms          |
|      | Frequency                     | 2.84 Hz         |



**Plot 1** Generator waveform



**Plot 2** Voltage across LED



### Further Investigation Results:

With the partial failure consisting of a  $100\ \Omega$  resistor in parallel with the LED, most of the current goes through the resistor (Figure 1-7b). This current can be traced through  $R_1$  and  $R_2$  and back to the supply using a logic pulser and current tracer as shown in Figure 1-8. With the short circuit (Figure 1-9), the current can be traced along the protoboard's bus, through the short and back to the supply with no current in the resistors or the LED.

### Evaluation and Review Questions

1. The circuit can be damaged if the wrong voltage is connected to it.
2. Vertical section: sets the amplitude of the input signal and develops voltages for display section; it sends signals to the trigger section.  
Trigger section: causes the start of the acquisition of the waveform. A stable display requires the trigger to occur at the same point on the waveform for each acquisition.  
Horizontal section: controls the time base.  
Display section: changes the intensity or other display parameters.
3. A probe from each channel is connected across the ungrounded component. All grounds are connected to the circuit ground. The scope is configured to measure the difference between the two channels. (This will vary between scope types; it sometimes requires the channels to be added with one channel inverted).
4. (a) The oscillator works but the LED is off. The voltage at pin 3 and the LED are identical.  
(b) The oscillator works but the frequency is too low (depending on the capacitor).  
(c) Reversing the power and ground leads will result in destructively high current.  
(d) The oscillator works but the LED is off. No voltage appears at the LED (but pin 3 is okay).
5. A digital oscilloscope is typically as accurate as a DMM and allows detection of noise or ripple with a power supply. A DMM is typically more portable. An analog scope is not as accurate as a DMM but does not show potential problems such as noise or ripple. A digital scope may be as accurate as a DMM because of automated measurement capability and gives more information than a DMM about potential problems such as the presence of noise.
6. Pulses from the logic pulser are applied to the circuit board trace that normally carries power but with power removed. The current tracer can be moved along this line, following the path of current until the short is found. (Note that this technique can be used for any board, analog or digital).

## Experiment 2: Constructing a Logic Probe

### Data and Observations

Step 3: Logic thresholds HIGH 1.98 V LOW 0.76 V

**TABLE 2-1**

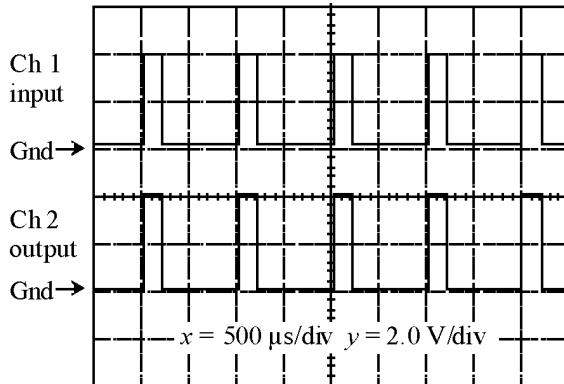
| Step |                      | Output Logic Level |               |               |
|------|----------------------|--------------------|---------------|---------------|
|      |                      | input is LOW       | input is OPEN | input is HIGH |
| 4    | one inverter         | HIGH               | LOW           | LOW           |
| 5    | two series inverters | LOW                | HIGH          | HIGH          |

**TABLE 2-2**

| Step |                                 | Input Logic Level (pin 3) | Output Logic Level (pin 3) | Logic Level (pin 5) | Logic Level (pin 6) |
|------|---------------------------------|---------------------------|----------------------------|---------------------|---------------------|
| 7    | $V_{in}$ momentarily on ground. |                           | HIGH                       |                     |                     |
| 8    | $V_{in}$ momentarily on +5.0 V. |                           | LOW                        |                     |                     |
| 9    | Fault condition: open at pin 5  | LOW                       | HIGH                       | INVALID             | LOW                 |
| 10   | Voltages with fault: DMM        | 0.06 V                    | 4.14 V                     | 1.64 V              | 0.06 V              |
| 11   | Voltages with fault: (scope)    | 0.06 V                    | 4.18 V                     | 1.65 V              | 0.06 V              |

### Further Investigation Results:

The signals are nearly identical as shown. In the experimental circuit, a slight difference in amplitude was noted and the output is delayed by 14 ns on the leading edge and 16 ns on the trailing edge. The time difference is due to transition time through the gates.



### Evaluation and Review Questions:

1. Increase the value of the  $330\ \Omega$  resistor in the input voltage divider.
2. Two inverters in series form a buffer that can allow additional drive current from the same logic output.
3. (a) The circuits are identical.  
 (b) If the input to the first inverter is open, an invalid level of approximately 1.6 V will be observed.  
 (c) If the input to the first inverter is open, then the output will be LOW.
4. A logic probe can quickly determine if a valid logic HIGH or LOW is present at some point in a circuit whereas a DMM can assign a numeric quantity to the level.
5. (a)  $V_{out}$  will alternate between a HIGH and LOW at a rapid rate.  
 (b) Approximately 50 ns.  
 (c) Since the period will be approximately 100 ns, the oscillation frequency is 10 MHz.
6. A steady state invalid level is an indication of an open input.

## Experiment 3: Number Systems:

### Data and Observations

| Inputs        |             | Output                |
|---------------|-------------|-----------------------|
| Binary Number | BCD Number  | Seven-Segment Display |
| 0 0 0 0       | <b>0000</b> | 0                     |
| 0 0 0 1       | <b>0001</b> | 1                     |
| 0 0 1 0       | <b>0010</b> | 2                     |
| 0 0 1 1       | <b>0011</b> | 3                     |
| 0 1 0 0       | <b>0100</b> | 4                     |
| 0 1 0 1       | <b>0101</b> | 5                     |
| 0 1 1 0       | <b>0110</b> | 6                     |
| 0 1 1 1       | <b>0111</b> | 7                     |
| 1 0 0 0       | <b>1000</b> | 8                     |
| 1 0 0 1       | <b>1001</b> | 9                     |
| 1 0 1 0       | INVALID     | 0                     |
| 1 0 1 1       | INVALID     | 1                     |
| 1 1 0 0       | INVALID     | 2                     |
| 1 1 0 1       | INVALID     | 3                     |
| 1 1 1 0       | INVALID     | 4                     |
| 1 1 1 1       | INVALID     | 5                     |

TABLE 3-1

Step 6. Method to cause leading zero suppression: The 7447A's ripple-blanking input for the most significant digit is connected to a LOW. If inputs A, B, C, D are also LOW, the display will be off and the ripple blanking output is LOW. Successive digits are blanked by connecting the ripple blanking output from the most significant digit to the next decoder's ripple-blanking input.

TABLE 3-2

| Trouble Number | Trouble                                           | Observations                                                                                              |
|----------------|---------------------------------------------------|-----------------------------------------------------------------------------------------------------------|
| 1              | LED for the C input is open                       | <i>The "C" switch has no effect on the output. The "C" input on the 7447A is always LOW.</i>              |
| 2              | A input to 7447A is open                          | <i>Only odd numbers can be observed on the display because the open A input is interpreted as a HIGH.</i> |
| 3              | <b>LAMP TEST</b> is shorted to ground             | <i>All segments are on; switches have no effect.</i>                                                      |
| 4              | Resistor connected to pin 15 of the 7447A is open | <i>Upper left (f) segment is always off. Numbers 0, 4, 5, 6, 8, 9 are shown incorrectly.</i>              |

**Further Investigation Results:**

The circuit needed is the same as Figure 3-2 except the MSB is disconnected and grounded at the BCD input to the 7447A. The LED used to indicate the D input can be connected to an LED that represents the octal MSB or it could be shown on the A input of a second 7447A decoder. The idea of this investigation is to reinforce converting a binary number to an octal number by grouping the binary bits by groups of three.

**Evaluation and Review Questions:**

1. Segment *g* open on seven segment display, open wire or resistor to *g* segment, bad 7447A.
2. Leave switches with binary 1000 and test logic at segment *g*. If the *g* segment is LOW, the segment is bad; if it is HIGH, move to pin 14 of 7447A and test the logic. If it is LOW, the resistive path is open; if it is HIGH, test inputs to 7447A.
3. All segments will be off.
4. Binary is a base two weighted number system. Column values increase by powers of two. BCD is a code that represents each decimal digit with 4 binary bits.

5.

| Binary          | Octal      | Hexadecimal | Decimal    | BCD                   |
|-----------------|------------|-------------|------------|-----------------------|
| <b>01001100</b> | <u>114</u> | <u>4C</u>   | <u>76</u>  | <u>0111 0110</u>      |
| <u>11000100</u> | <b>304</b> | <u>C4</u>   | <u>196</u> | <u>0001 1001 0110</u> |
| <u>11100110</u> | <b>346</b> | <b>E6</b>   | <u>230</u> | <u>0010 0011 0000</u> |
| <u>111001</u>   | <u>71</u>  | <u>39</u>   | <b>57</b>  | <u>0101 0111</u>      |
| <u>110001</u>   | <b>61</b>  | <u>31</u>   | <u>49</u>  | <b>0100 1001</b>      |

6. a. The base can be found algebraically by solving  $1x^2 + 2x^1 + 5 = 85$  (*x* represents the base). The positive root (base) is 8.  
b. 16

## Experiment 4: Logic Gates: Data and Observations

**TABLE 4-2** NAND Gate.



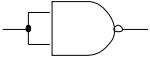
| Inputs |   | Output   | Measured Output Voltage |
|--------|---|----------|-------------------------|
| A      | B | X        |                         |
| 0      | 0 | <b>1</b> | <b>3.95 V</b>           |
| 0      | 1 | <b>1</b> | <b>3.95 V</b>           |
| 1      | 0 | <b>1</b> | <b>3.95 V</b>           |
| 1      | 1 | <b>0</b> | <b>0.06 V</b>           |

**TABLE 4-3** NOR Gate.



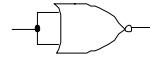
| Inputs |   | Output   | Measured Output Voltage |
|--------|---|----------|-------------------------|
| A      | B | X        |                         |
| 0      | 0 | <b>1</b> | <b>4.01 V</b>           |
| 0      | 1 | <b>0</b> | <b>0.06 V</b>           |
| 1      | 0 | <b>0</b> | <b>0.06 V</b>           |
| 1      | 1 | <b>0</b> | <b>0.06 V</b>           |

**TABLE 4-4**  
Truth table for Figure 4-4.



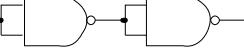
| Input | Output   | Measured Output Voltage |
|-------|----------|-------------------------|
| A     | X        |                         |
| 0     | <b>1</b> | <b>3.95 V</b>           |
| 1     | <b>0</b> | <b>0.06 V</b>           |

**TABLE 4-5**  
Truth table for Figure 4-5.



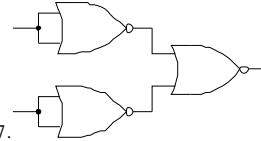
| Input | Output   | Measured Output Voltage |
|-------|----------|-------------------------|
| A     | X        |                         |
| 0     | <b>1</b> | <b>4.01 V</b>           |
| 1     | <b>0</b> | <b>0.06 V</b>           |

**TABLE 4-6**  
Truth table for Figure 4-6.



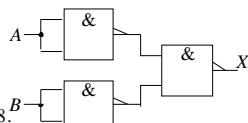
| Input | Output   | Measured Output Voltage |
|-------|----------|-------------------------|
| A     | X        |                         |
| 0     | <b>0</b> | <b>0.05 V</b>           |
| 1     | <b>1</b> | <b>3.97 V</b>           |

**TABLE 4-7**  
Truth table for Figure 4-7.



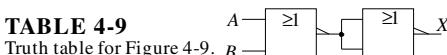
| Inputs |   | Output   | Measured Output Voltage |
|--------|---|----------|-------------------------|
| A      | B | X        |                         |
| 0      | 0 | <b>0</b> | <b>0.06 V</b>           |
| 0      | 1 | <b>0</b> | <b>0.06 V</b>           |
| 1      | 0 | <b>0</b> | <b>0.06 V</b>           |
| 1      | 1 | <b>0</b> | <b>3.96 V</b>           |

**TABLE 4-8**  
Truth table for Figure 4-8.



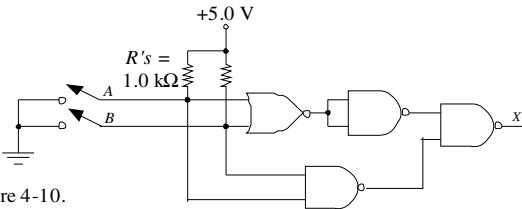
| Inputs |   | Output   | Measured Output Voltage |
|--------|---|----------|-------------------------|
| A      | B | X        |                         |
| 0      | 0 | <b>0</b> | <b>0.05 V</b>           |
| 0      | 1 | <b>1</b> | <b>3.98 V</b>           |
| 1      | 0 | <b>1</b> | <b>3.98 V</b>           |
| 1      | 1 | <b>1</b> | <b>3.98 V</b>           |

**TABLE 4-9**  
Truth table for Figure 4-9.



| Inputs |   | Output   | Measured Output Voltage |
|--------|---|----------|-------------------------|
| A      | B | X        |                         |
| 0      | 0 | <b>0</b> | <b>0.06 V</b>           |
| 0      | 1 | <b>1</b> | <b>3.96 V</b>           |
| 1      | 0 | <b>1</b> | <b>3.96 V</b>           |
| 1      | 1 | <b>1</b> | <b>3.95 V</b>           |

### Further Investigation Results:



**TABLE 4-10**  
Truth table for Figure 4-10.

| Inputs |   | Output   | Measured Output Voltage |
|--------|---|----------|-------------------------|
| A      | B | X        |                         |
| 0      | 0 | <b>1</b> | <b>3.97 V</b>           |
| 0      | 1 | <b>0</b> | <b>0.06 V</b>           |
| 1      | 0 | <b>0</b> | <b>0.06 V</b>           |
| 1      | 1 | <b>1</b> | <b>3.97 V</b>           |

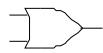
### Evaluation and Review Questions:

1. a. Fig. 4-4 and 4-5.  
b. Fig. 4-7.  
c. Fig 4-8 and 4-9
2. Betty. A LOW on any input produces a LOW on the output. This describes an AND gate.
3. A HIGH on any input causes a HIGH output. This describes an OR gate.
- 4.
5. When the signal is HIGH, data is transmitted; when it is LOW, data is received.
6. The fact that an output is at a constant level does not in itself indicate a bad gate. If the circuit is not working properly, check the inputs first. If all inputs are HIGH, and the output is HIGH, the gate may be bad, but connections to the output should be checked to see if another component is holding the output HIGH.

## Experiment 5: More Logic Gates: (TTL)

### Data and Observations:

**TABLE 5-2**  
OR Gate

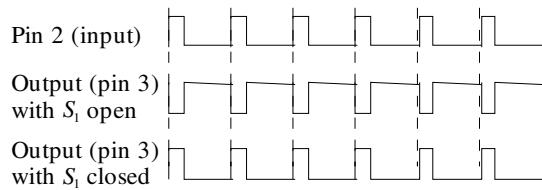


| Inputs |   | Output   | Measured Output Voltage |
|--------|---|----------|-------------------------|
| A      | B | X        |                         |
| 0      | 0 | <b>0</b> | <b>0.07V</b>            |
| 0      | 1 | <b>1</b> | <b>3.93 V</b>           |
| 1      | 0 | <b>1</b> | <b>3.93 V</b>           |
| 1      | 1 | <b>1</b> | <b>3.93 V</b>           |

**TABLE 5-3**  
XOR Gate



| Inputs |   | Output   | Measured Output Voltage |
|--------|---|----------|-------------------------|
| A      | B | X        |                         |
| 0      | 0 | <b>0</b> | <b>0.06 V</b>           |
| 0      | 1 | <b>1</b> | <b>3.94 V</b>           |
| 1      | 0 | <b>1</b> | <b>3.94 V</b>           |
| 1      | 1 | <b>0</b> | <b>0.06 V</b>           |



**PLOT 1**

**TABLE 5-3**

| $D_3$ | $D_2$ | $D_1$ | $D_0$ | $Q_3$    | $Q_2$    | $Q_1$    | $Q_0$    |
|-------|-------|-------|-------|----------|----------|----------|----------|
| 0     | 0     | 0     | 0     | <b>0</b> | <b>0</b> | <b>0</b> | <b>0</b> |
| 0     | 0     | 0     | 1     | <b>1</b> | <b>1</b> | <b>1</b> | <b>1</b> |
| 0     | 0     | 1     | 0     | <b>1</b> | <b>1</b> | <b>1</b> | <b>0</b> |
| 0     | 0     | 1     | 1     | <b>1</b> | <b>1</b> | <b>0</b> | <b>1</b> |
| 0     | 1     | 0     | 0     | <b>1</b> | <b>1</b> | <b>0</b> | <b>0</b> |
| 0     | 1     | 0     | 1     | <b>1</b> | <b>0</b> | <b>1</b> | <b>1</b> |
| 0     | 1     | 1     | 0     | <b>1</b> | <b>0</b> | <b>1</b> | <b>0</b> |
| 0     | 1     | 1     | 1     | <b>1</b> | <b>0</b> | <b>0</b> | <b>1</b> |
| 1     | 0     | 0     | 0     | <b>1</b> | <b>0</b> | <b>0</b> | <b>0</b> |
| 1     | 0     | 0     | 1     | <b>0</b> | <b>1</b> | <b>1</b> | <b>1</b> |
| 1     | 0     | 1     | 0     | <b>0</b> | <b>1</b> | <b>1</b> | <b>0</b> |
| 1     | 0     | 1     | 1     | <b>0</b> | <b>1</b> | <b>0</b> | <b>1</b> |
| 1     | 1     | 0     | 0     | <b>0</b> | <b>1</b> | <b>0</b> | <b>0</b> |
| 1     | 1     | 0     | 1     | <b>0</b> | <b>0</b> | <b>1</b> | <b>1</b> |
| 1     | 1     | 1     | 0     | <b>0</b> | <b>0</b> | <b>1</b> | <b>0</b> |
| 1     | 1     | 1     | 1     | <b>0</b> | <b>0</b> | <b>0</b> | <b>1</b> |

**TABLE 5-5**

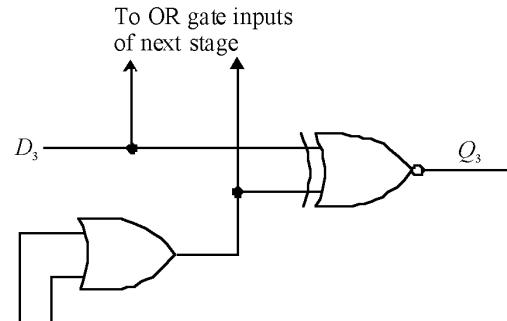
| Symptom Number | Symptom                                                               | Possible Cause                                                                      |
|----------------|-----------------------------------------------------------------------|-------------------------------------------------------------------------------------|
| 1              | None of the LEDs operate; the switches have no effect.                | <i>Power supply not on or open lead from the power or ground line to the board.</i> |
| 2              | LEDs on the output side do not work; those on the input side do work. | <i>Power or ground connection to the 7486 open.</i>                                 |
| 3              | The LED representing $Q_3$ is sometimes on when it should be off.     | <i>An input to the top XOR gate is likely to be open.</i>                           |
| 4              | The Complement switch has no effect on the outputs.                   | <i>Open or shorted connection from switch or a bad switch.</i>                      |

### Evaluation and Review Questions

- One input is a control input and the other is the data. The data is unchanged if the control input is LOW but is inverted if the control input is HIGH. This is easily seen on a truth table to the right.

| Control | Data | Output |
|---------|------|--------|
| 0       | 0    | 0      |
| 0       | 1    | 1      |
| 1       | 0    | 1      |
| 1       | 1    | 0      |

- The circuit can be expanded by “chaining” additional OR gates to D3 and the output of the upper OR gate as shown in the partial schematic to the right. The output of the OR gate is connected to the input of the next XOR gate. The other XOR input is connected to the data line as before.



### Further Investigation Results:

Each time a switch is thrown, no matter which one, the LED will change states (either on or off).

### Data and Observations (VHDL)

*Note:* The complete student programs in Figures 5-6 and 5-9 are given in the experiment and on the CD. No student inputs are required for the programs in this experiment, so student and instructor's programs are identical.

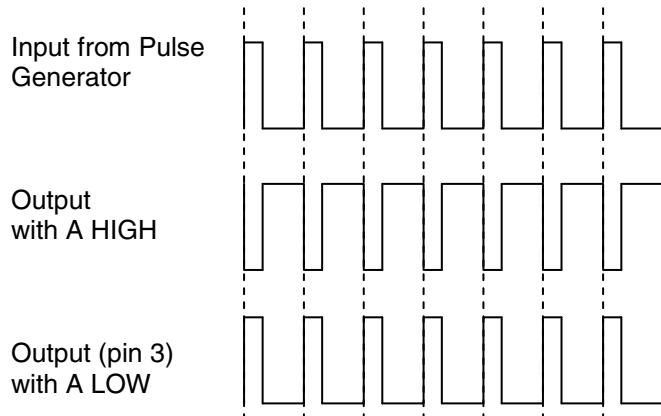
High level voltages shown are for a PLDT-2 board to an LED output with the LED on.

TABLE 5-7   
OR Gate.

| Inputs |   | Output | (Optional)<br>Measured<br>Voltage |
|--------|---|--------|-----------------------------------|
| A      | B | X      |                                   |
| 0      | 0 | 0      | 0.001 V                           |
| 0      | 1 | 1      | 3.15 V                            |
| 1      | 0 | 1      | 3.15 V                            |
| 1      | 1 | 1      | 3.15 V                            |

TABLE 5-8   
XOR Gate.

| Inputs |   | Output | (Optional)<br>Measured<br>Voltage |
|--------|---|--------|-----------------------------------|
| A      | B | X      |                                   |
| 0      | 0 | 0      | 0.001 V                           |
| 0      | 1 | 1      | 3.15 V                            |
| 1      | 0 | 1      | 3.15 V                            |
| 1      | 1 | 0      | 3.15 V                            |



**PLOT 2**

**Table 5-9** is identical to **Table 5-4** in the TTL section.

### Review Questions (VHDL)

1. LED4 through LED7 will light for all input conditions except A, B, C, and D set to LOW.
2. One way is to use the equation **LED1 <= (A or B) xor C**. Although it is not part of the question, a VHDL program is shown below. It will have a square wave output that starts one clock pulse after the counter is reset.

## Experiment 6: Interpreting Manufacturer's Data Sheets:

### Data and Observations:

**TABLE 6-1**

TTL 7404

| Recommended Operating Conditions                                                                    |                                |                                                               |     |      |        |      |       |                  |                     |  |
|-----------------------------------------------------------------------------------------------------|--------------------------------|---------------------------------------------------------------|-----|------|--------|------|-------|------------------|---------------------|--|
| Symbol                                                                                              | Parameter                      | DM5405                                                        |     |      | DM7404 |      |       | Units            | Measured Value      |  |
|                                                                                                     |                                | Min                                                           | Nom | Max  | Min    | Nom  | Max   |                  |                     |  |
| $V_{CC}$                                                                                            | Supply Voltage                 | 4.5                                                           | 5   | 5.5  | 4.75   | 5    | 5.25  | V                |                     |  |
| $V_{IH}$                                                                                            | High-Level Input Voltage       | 2                                                             |     |      | 2      |      |       | V                | a. <b>4.98 V</b>    |  |
| $V_{IL}$                                                                                            | Low-Level Input Voltage        |                                                               |     | 0.8  |        |      | 0.8   | V                | b. <b>0.289 V</b>   |  |
| $I_{OH}$                                                                                            | High-Level Output Current      |                                                               |     | -0.4 |        |      | -0.4  | mA               | c. <b>-0.245 mA</b> |  |
| $I_{OL}$                                                                                            | Low-Level Output Current       |                                                               |     | 16   |        |      | 16    | mA               | d. <b>14.5 mA</b>   |  |
| $T_A$                                                                                               | Free Air Operating Temperature | -55                                                           |     | 125  | 0      |      | 70    | °C               |                     |  |
| Electrical Characteristics Over Recommended Operating Free Air Temperature (unless otherwise noted) |                                |                                                               |     |      |        |      |       |                  |                     |  |
| Symbol                                                                                              | Parameter                      | Conditions                                                    |     | Min  | Typ    | Max  | Units |                  |                     |  |
| $V_I$                                                                                               | Input clamp voltage            | $V_{CC}=\text{Min}, I_I=-12\text{mA}$                         |     |      |        | -1.5 | V     |                  |                     |  |
| $V_{OH}$                                                                                            | High-level output voltage      | $V_{CC}=\text{Min}, V_{OH}=\text{Max}$<br>$V_{IL}=\text{Min}$ |     | 2.4  | 3.4    |      | V     | e. <b>3.68 V</b> |                     |  |

| Electrical Characteristics Over Recommended Operating Free Air Temperature (unless otherwise noted) |                                   |                                                               |      |     |      |      |       |                    |
|-----------------------------------------------------------------------------------------------------|-----------------------------------|---------------------------------------------------------------|------|-----|------|------|-------|--------------------|
| Symbol                                                                                              | Parameter                         | Conditions                                                    |      | Min | Type | Max  | Units | Measured Value     |
| $V_{OL}$                                                                                            | Low Level Output Voltage          | $V_{CC}=\text{Min}, I_{OL}=\text{Max}$<br>$V_{IH}=\text{Min}$ |      |     | 0.2  | 0.4  | V     | f. <b>0.222 V</b>  |
| $I_I$                                                                                               | Input Current @ Max Input Voltage | $V_{CC}=\text{Max}, V_I=5.5\text{ V}$                         |      |     |      | 1    | mA    |                    |
| $I_{IH}$                                                                                            | High-Level Input Current          | $V_{CC}=\text{Max}, V_I=2.4\text{ V}$                         |      |     |      | 40   | μA    | g. <b>7.4 μA</b>   |
| $I_{IL}$                                                                                            | Low-Level Input Current           | $V_{CC}=\text{Min}, V_I=0.4\text{ V}$                         |      | 2.4 | 3.4  | -1.6 | μA    | h. <b>-0.88 mA</b> |
| $I_{OS}$                                                                                            | Short Circuit Output Current      | $V_{CC}=\text{Max}$                                           | DM54 | -20 |      | -55  | mA    |                    |
|                                                                                                     |                                   |                                                               | DM74 | -18 |      | -55  |       |                    |
| $I_{CCH}$                                                                                           | Supply Current With Outputs High  | $V_{CC}=\text{Max}$                                           |      |     | 6    | 12   | mA    |                    |
| $I_{CCL}$                                                                                           | Supply Current With Outputs Low   | $V_{CC}=\text{Max}$                                           |      |     | 18   | 33   | mA    |                    |

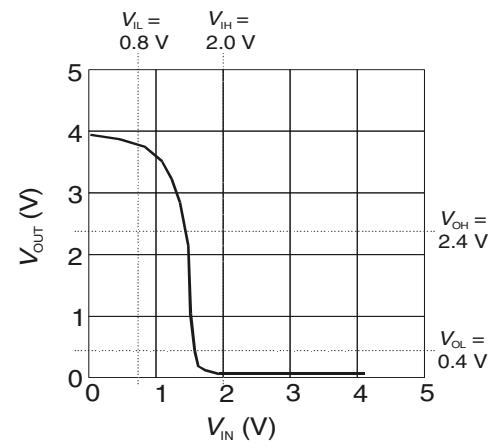
**TABLE 6-2 CMOS 4081**

|     | Quantity                                  | Manufacturer's Specified Value        | Measured Value                   |
|-----|-------------------------------------------|---------------------------------------|----------------------------------|
| (a) | $V_{OL(max)}$ , low-level output voltage  | <b>0.55 V</b>                         | <b>0.1 mV</b>                    |
| (b) | $V_{OH(min)}$ , high-level output voltage | <b>4.95 V</b>                         | <b>4.99 V</b>                    |
| (c) | $V_{IL(max)}$ , low-level input voltage   | <b>1.5 V</b>                          | <b>1.5 V</b>                     |
| (d) | $V_{IH(min)}$ , high-level output voltage | <b>3.5 V</b>                          | <b>3.5 V</b>                     |
| (e) | $I_{OL(min)}$ , high-level output current | <b>0.51 mA</b>                        | <b>1.10 mA</b>                   |
| (f) | $I_{OH(min)}$ , high-level output current | <b>-0.51 mA</b>                       | <b>-1.05 mA</b>                  |
| (g) | $I_{IN(typ)}$ , input current             | <b><math>\pm 10^{-5} \mu A</math></b> | <b>0.04 <math>\mu A^*</math></b> |

\* limited by instruments

#### Further Investigation Results:

| $V_{in}$ (V) | $V_{out}$ (V) |
|--------------|---------------|
| 0.4          | <b>3.98</b>   |
| 0.8          | <b>3.64</b>   |
| 1.2          | <b>2.88</b>   |
| 1.3          | <b>2.52</b>   |
| 1.4          | <b>1.39</b>   |
| 1.5          | <b>0.03</b>   |
| 1.6          | <b>0.03</b>   |
| 2.0          | <b>0.03</b>   |
| 2.4          | <b>0.03</b>   |
| 2.8          | <b>0.03</b>   |
| 3.2          | <b>0.03</b>   |
| 3.6          | <b>0.03</b>   |
| 4.0          | <b>0.03</b>   |



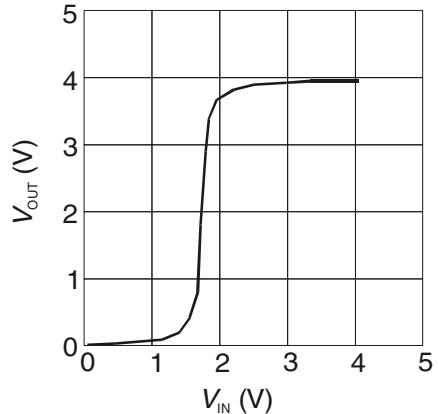
**PLOT 1**

**Review Questions:**

1. A load causes the output LOW to be higher. (The measured LOW with no load was 30 mV; with the minimum load, the measured LOW was 222 mV).
2.  $R = 2.4 \text{ V} / 0.4 \text{ mA} = 6 \text{ k}\Omega$ .
3.  $V_{NL(LOW)} = 0.3 \text{ V}$   
 $V_{NL(HIGH)} = 0.5 \text{ V}$
4. a. Circuit (a) is better.  
b. The  $I_{OH}$  specification is exceeded in circuit (b). In (a), the LED is turned on with  $I_{OL}$  and is within the specified limit.
5. Logic levels are specified with reference to ground and can produce incorrect logic if the ground level is wrong. The scope should be dc coupled to assure the troubleshooter knows the ground level of the signal. (Note that in some

digital scopes, the ground level is shown with a small arrow to the side of the display.)

6. The transfer curve for an AND gate (with inputs tied together) is shown below. The threshold is expected to occur at +1.6 V.



Plot for Question 6

## Experiment 7: Boolean Laws and DeMorgan's Theorem

Data and Observations:

TABLE 7-2

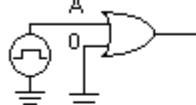
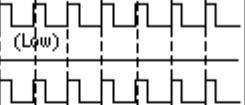
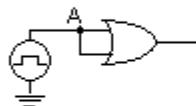
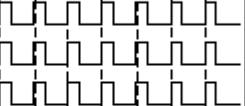
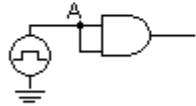
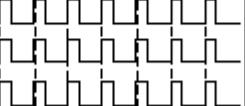
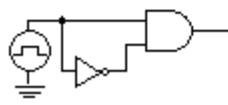
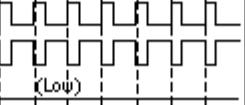
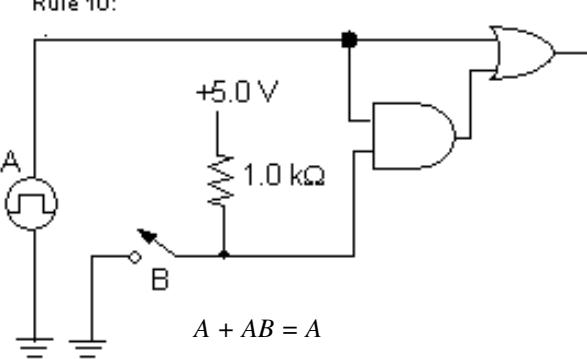
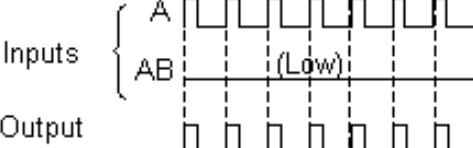
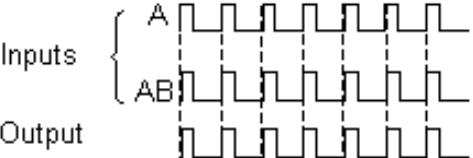
| Schematic                                                                         | Timing Diagram                                                                                                    | Boolean Rule      |
|-----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------|-------------------|
|  | Inputs: A, 0<br>Output:          | $A + 0 = A$       |
|  | Inputs: A, A<br>Output:          | $A + A = A$       |
|  | Inputs: A, A<br>Output:          | $A * A = A$       |
|  | Inputs: A, $\bar{A}$<br>Output:  | $A * \bar{A} = 0$ |

TABLE 7-3

| Schematic                                                                                                        | Timing Diagram                                                                                                                                                                                                                                                                                                                          |
|------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>Rule 10:</p>  $A + AB = A$ | <p>Timing diagram for <math>B = 0</math>:</p> <p>Inputs: A, AB<br/>Output: </p> <p>Timing diagram for <math>B = 1</math>:</p> <p>Inputs: A, AB<br/>Output: </p> |

**TABLE 7.4**

| Schematic                              | Timing Diagram                                                                                                        |
|----------------------------------------|-----------------------------------------------------------------------------------------------------------------------|
| <p>Rule 11:</p> $A + \bar{A}B = A + B$ | <p>Inputs { A<br/>AB<br/>Output</p> <p>Timing diagram for <math>B = 1</math>:</p> <p>Inputs { A<br/>AB<br/>Output</p> |

**Further Investigation Results****TABLE 7-5**

Truth table for Figure 7-5

| Inputs | Output |   |   |
|--------|--------|---|---|
| A      | B      | C | X |
| 0      | 0      | 0 | 1 |
| 0      | 0      | 1 | 0 |
| 0      | 1      | 0 | 0 |
| 0      | 1      | 1 | 0 |
| 1      | 0      | 0 | 1 |
| 1      | 0      | 1 | 0 |
| 1      | 1      | 0 | 1 |
| 1      | 1      | 1 | 0 |

$$X = (A + \bar{B})\bar{C}$$

**TABLE 7-6**

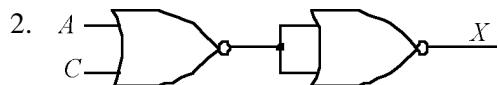
Truth table for Figure 7-6

| Inputs | Output |   |   |
|--------|--------|---|---|
| A      | B      | C | X |
| 0      | 0      | 0 | 1 |
| 0      | 0      | 1 | 0 |
| 0      | 1      | 0 | 0 |
| 0      | 1      | 1 | 0 |
| 1      | 0      | 0 | 1 |
| 1      | 0      | 1 | 0 |
| 1      | 1      | 0 | 1 |
| 1      | 1      | 1 | 0 |

$$X = \bar{A}B + \bar{C}$$

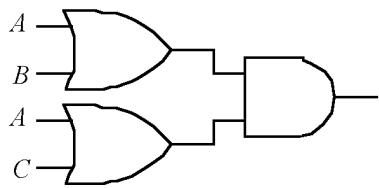
**Evaluation and Review Questions:**

1.  $A(A + B) + C = AA + AB + C$  (distribution)  
 $= A + AB + C$  (rule 7)  
 $= A + C$  (rule 10)

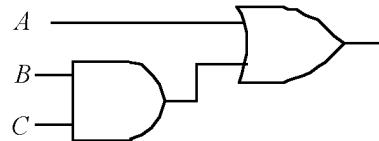


3.

Rule 12:  
 $(A + B)(A + C)$



$$= A + BC$$



4. Because the two circuits have identical truth tables, they perform the same logic.

$$\overline{(AB + C)} = \overline{AB}\overline{C} = (A + \overline{B})\overline{C}$$

5.  $(\overline{A} \cdot 1) = A + 0 = A$

6. Answers vary but should follow a logical sequence. An example is:

1. Verify that each IC has power and ground connected and that it is the correct voltage.
2. Select an input that should turn on the LED (such as all switches closed to ground.) With this input, verify that the A, B, and C inputs to their respective gates are all LOW.
3. With all inputs LOW, verify that the output of the 4069 gates are both HIGH and that the output of the 4071 is HIGH. Verify that the output of the 4081 is HIGH.
4. Check that the LED is inserted in the correct direction and that there is a path from the output of the 4081 through a 1.0 kΩ resistor through the LED to ground.

## Experiment 8: Logic Circuit Simplification

### Data and Observations

Note: Truth tables 8-2, 8-3, 8-6 and 8-7 are identical. Only Table 8-2 is shown.

**TABLE 8-2 same as TABLE 8-6(VHDL)**

Truth table for BCD invalid code detector

| Inputs  | Output |
|---------|--------|
| D C B A | X      |
| 0 0 0 0 | 0      |
| 0 0 0 1 | 0      |
| 0 0 1 0 | 0      |
| 0 0 1 1 | 0      |
| 0 1 0 0 | 0      |
| 0 1 0 1 | 0      |
| 0 1 1 0 | 0      |
| 0 1 1 1 | 0      |
| 1 0 0 0 | 0      |
| 1 0 0 1 | 0      |
| 1 0 1 0 | 1      |
| 1 0 1 1 | 1      |
| 1 1 0 0 | 1      |
| 1 1 0 1 | 1      |
| 1 1 1 0 | 1      |
| 1 1 1 1 | 1      |

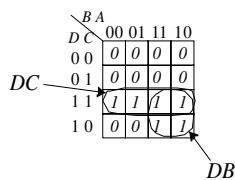


FIGURE 8-3 and FIGURE 8-6(VHDL)  
Karnaugh Map of truth table for invalid BCD code detect

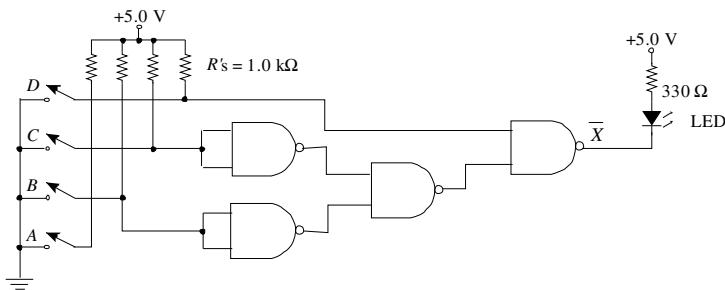
Minimum sum-of-products read from map:

$$X = \underline{DB + DC}$$

Factoring D from both product terms gives:

$$X = \underline{D(B + C)}$$

Step 5: Circuit for BCD invalid code detector (replacing OR gate with equivalent NAND gates):



Note that the A switch is not used in the invalid code detector.

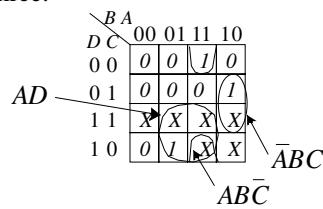
**TABLE 8-4**

| Problem Number | Problem                                                                                | Effect                                                                                                                                  |
|----------------|----------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 1              | The pull-up resistor for the $D$ switch is open.                                       | <i>The D input will be an invalid HIGH when the D switch is open. The circuit will perform normally except is susceptible to noise.</i> |
| 2              | The ground to the NAND gate is open.                                                   | <i>The LED will not turn on under any conditions since there is no return path for LED current.</i>                                     |
| 3              | A 3.3 k $\Omega$ resistor was accidentally used in place of the 330 $\Omega$ resistor. | <i>Circuit operates normally but LED is slightly dimmer (may depend on the LED).</i>                                                    |
| 4              | The LED was inserted backward.                                                         | <i>The LED will not turn on under any conditions.</i>                                                                                   |
| 5              | Switch A is shorted to ground.                                                         | <i>The A input is not used so it will have no effect.</i>                                                                               |

**Further Investigation Results:****TABLE 8-5. same as TABLE 8-8 (VHDL)**

Truth table for BCD numbers divisible by three:

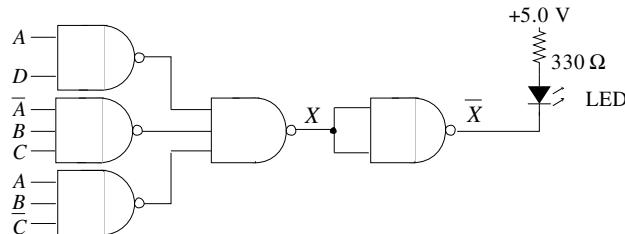
| Inputs          | Output |
|-----------------|--------|
| $D \ C \ B \ A$ | $X$    |
| 0 0 0 0         | 0      |
| 0 0 0 1         | 0      |
| 0 0 1 0         | 0      |
| 0 0 1 1         | 1      |
| 0 1 0 0         | 0      |
| 0 1 0 1         | 0      |
| 0 1 1 0         | 1      |
| 0 1 1 1         | 0      |
| 1 0 0 0         | 0      |
| 1 0 0 1         | 1      |
| 1 0 1 0         | X      |
| 1 0 1 1         | X      |
| 1 1 0 0         | X      |
| 1 1 0 1         | X      |
| 1 1 1 0         | X      |
| 1 1 1 1         | X      |

FIGURE 8-5 and FIGURE 8-9(VHDL)  
Karnaugh Map of truth table for BCD numbers divisible by three.

Minimum sum-of-products read from map:

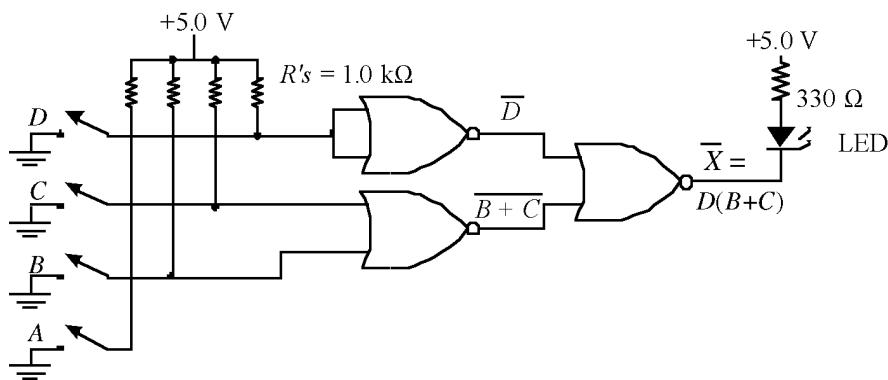
$$X = AD + ABC\bar{C} + \bar{A}BC$$

Circuit:



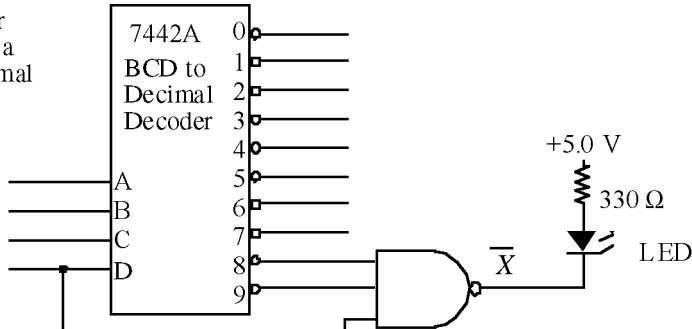
**Evaluation and Review Questions:**

1. The path from the OR gate to the NAND gate may be open or the inputs to the NAND gate may both be shorted to  $D$ . To troubleshoot the problem, put the circuit in state 1000 or 1001 and test the logic at the OR gate output and at the input of the NAND gate.
2. Equivalent circuit for Figure 8-4 using only NOR gates:

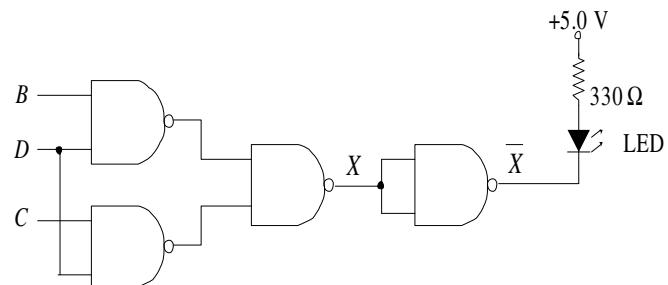


3. Outputs 8 and 9 from the 7442 decoder are connected, along with the  $D$  input, to a three input NAND gate and to an active LOW LED. See drawing below.

Invalid code detector  
for a circuit that has a  
7442A BCD to decimal  
decoder.



4.  $\bar{X} = \bar{D}(\bar{B}\bar{C})$   
 $X = \overline{\bar{D}(\bar{B}\bar{C})}$   
 $X = D + BC$
5. Sum of products (SOP) form  $X = BD + CD$ .  
Product of sums (POS form)  $X = D(B+C)$ . This can be done by factoring or by reading the 0's directly from the map (see Section 4-10 of text).
6. Implementation from the expression in step 2 ( $X = BD + CD$ ) is shown in the schematic below:



### Data and Observations (VHDL)

Except for the VHDL code, data and observations are identical to the TTL section and are not shown. The completed program in Figure 8-10 is as follows (student answer in **bold**):

```
entity lab8 is
 port (B, C, D: in bit; X: out bit);
end entity lab8;

architecture Invalid of lab8 is
begin
 X <= (B or C) and D;
end architecture Invalid;
```

Figure 8-8

### Further Investigation Results (VHDL)

The truth table shown as Table 8-8 is identical with Table 8-5 in the TTL section. The completed program in Figure 8-12 is as follows (student answer in **bold**):

```
entity lab8FI is
 port (A, C, D: in bit; X: out bit);
end entity lab8FI;

architecture Div3 of lab8FI is
begin
 X <= (A and D) or (A and B and not C) or
 (not A and B and C);
end architecture Div3;
```

Figure 8-10

### Review Questions (VHDL)

1. A was not in the output terms for the Karnaugh maps in Figure 8-8. Because this is a small section of a larger digital application, we do not eliminate A from the system.
2. entity lab8 is  
 port (B, C, D: in bit; X: out bit);  
end entity lab8;  
  
architecture Invalid of lab8 is  
begin  
 X <= (**B nor C**) nor (**D nor D**); - using only nor gates  
end architecture Invalid;

## Experiment 9: The Perfect Pencil Machine

The perfect pencil machine is a combinational logic circuit that delivers a pencil or change for certain combinations of inputs representing coin switches. Coin switches are provided for one nickel, ( $N_1$ ), two dimes ( $D_1$  and  $D_2$ ), and a quarter ( $Q$ ). (Only one nickel switch is used to simplify the problem). The two dime switches are stacked on top of each other such that  $D_1$  is always activated before  $D_2$ . The truth table has a number of don't care ( $X$ ) entries, considered to be impossible inputs as described in the experiment. For example,  $D_2$  cannot be inserted in the machine until  $D_1$  has activated its switch and more than two coins cannot be entered in the machine. These "don't cares" allow the logic to be simplified considerably.

TABLE 9-2  
Truth table for model-2 perfect pencil machine

| Inputs |       |       |     | Outputs |    |        |        |
|--------|-------|-------|-----|---------|----|--------|--------|
| $N_1$  | $D_1$ | $D_2$ | $Q$ | P       | NC | $DC_1$ | $DC_2$ |
| 0      | 0     | 0     | 0   | 0       | 0  | 0      | 0      |
| 0      | 0     | 0     | 1   | 1       | 0  | 1      | 0      |
| 0      | 0     | 1     | 0   | X       | X  | X      | X      |
| 0      | 0     | 1     | 1   | X       | X  | X      | X      |
| 0      | 1     | 0     | 0   | 0       | 0  | 0      | 0      |
| 0      | 1     | 0     | 1   | 1       | 0  | 1      | 1      |
| 0      | 1     | 1     | 0   | 1       | 1  | 0      | 0      |
| 0      | 1     | 1     | 1   | X       | X  | X      | X      |
| 1      | 0     | 0     | 0   | 0       | 0  | 0      | 0      |
| 1      | 0     | 0     | 1   | 1       | 1  | 1      | 0      |
| 1      | 0     | 1     | 0   | X       | X  | X      | X      |
| 1      | 0     | 1     | 1   | X       | X  | X      | X      |
| 1      | 1     | 0     | 0   | 1       | 0  | 0      | 0      |
| 1      | 1     | 0     | 1   | X       | X  | X      | X      |
| 1      | 1     | 1     | 0   | X       | X  | X      | X      |
| 1      | 1     | 1     | 1   | X       | X  | X      | X      |

$P = \text{Pencil}$

| $D_2 Q$ | 00 | 01 | 11 | 10 |
|---------|----|----|----|----|
| $ND_1$  | 0  | 1  | X  | X  |
| 00      | 0  | 1  | X  | 1  |
| 01      | 1  | X  | X  | X  |
| 11      | 0  | X  | X  | X  |
| 10      | 0  | 1  | X  | X  |

$P = ND_1 + D_2 + Q$

$NC = \text{Nickel Change}$

| $D_2 Q$ | 00 | 01 | 11 | 10 |
|---------|----|----|----|----|
| $ND_1$  | 0  | 0  | X  | X  |
| 00      | 0  | 0  | X  | 1  |
| 01      | 0  | 1  | X  | 0  |
| 11      | 0  | X  | X  | X  |
| 10      | 0  | 1  | X  | X  |

$NC = NQ + D_2$

$DC_1 = \text{First dime change}$

| $D_2 Q$ | 00 | 01 | 11 | 10 |
|---------|----|----|----|----|
| $ND_1$  | 0  | 1  | X  | X  |
| 00      | 0  | 1  | X  | 0  |
| 01      | 0  | X  | X  | X  |
| 11      | 0  | 1  | X  | X  |
| 10      | 0  | 1  | X  | X  |

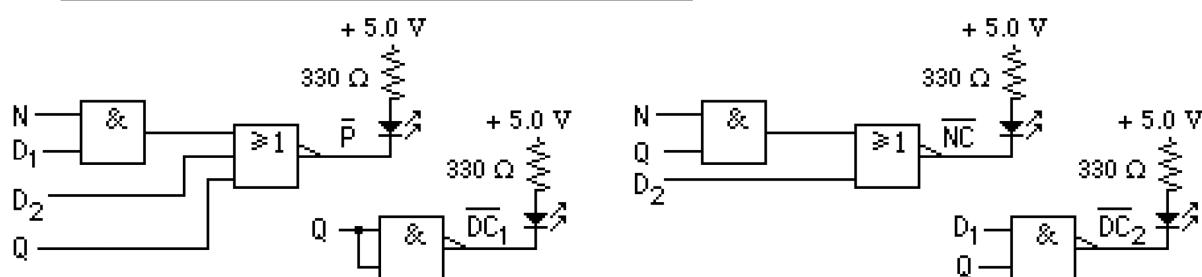
$DC_1 = Q$

$DC_2 = \text{Second dime change}$

| $D_2 Q$ | 00 | 01 | 11 | 10 |
|---------|----|----|----|----|
| $ND_1$  | 0  | 0  | X  | X  |
| 00      | 0  | 0  | X  | X  |
| 01      | 0  | 1  | X  | 0  |
| 11      | 0  | X  | X  | X  |
| 10      | 0  | 0  | X  | X  |

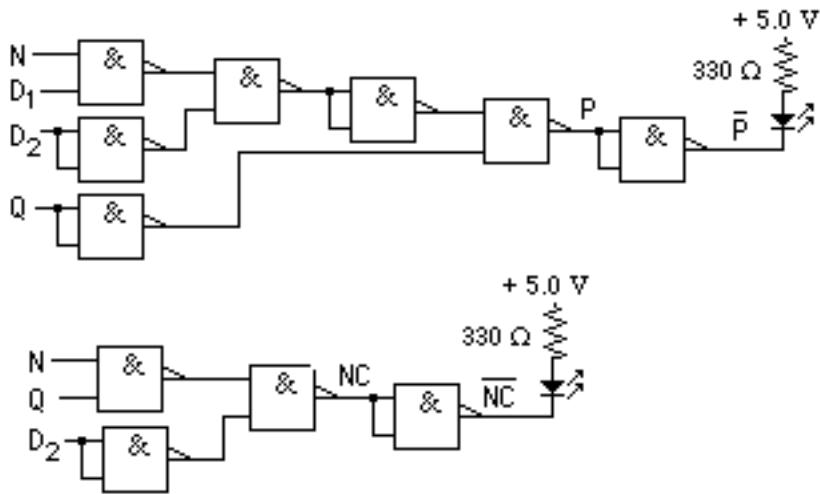
$DC_2 = D_1 Q$

A simplified implementation is shown (switches not shown). The output logic from the maps has been inverted to light LEDs with a LOW rather than a HIGH in keeping with TTL specified  $I_O$  values.



**Further Investigation Results:**

This investigation requires the student to modify his or her experiment to use only 2-input NAND gates. The two circuits for dime change logic already meet that requirement. Modifications for the pencil and nickel change logic are shown below:



## Experiment 10: The Molasses Tank

The Molasses Tank is a combinational logic problem designed to reinforce Karnaugh mapping, circuit implementation, troubleshooting, and report writing. Although standard combinational logic is implemented, one of the inputs to the truth table is the output valve logic,  $V_{OUT}$ , to produce latching action. The truth table for the output valve is given in the experiment and the truth table for the alarm,  $A$ , and the input valve,  $V_{IN}$ , are given here. (The input valve is implemented in the Further Investigation with an extra Karnaugh map provided in the manual for this). Maps for these three outputs are also shown. (The heater output was not required in the experiment, but could be implemented as  $H = T_C \cdot L_L$ .) A circuit implementation using inverters and NAND gates is shown (note that  $A$  is implemented after applying DeMorgan's theorem). Active LOW outputs are used for the LEDs as given in the truth tables. Other implementations are possible.

| $L_H$ | $L_L$ | $T_C$ | $V_{OUT}$ |
|-------|-------|-------|-----------|
| 0 0   | 0 0   | 0 0   | 1 1       |
| 0 0   | 0 1   | 0 1   | 0 1       |
| 0 0   | 1 0   | 1 0   | 1 1       |
| 0 0   | 1 1   | 1 1   | 1 0       |
| 0 1   | 0 0   | 0 0   | 1 1       |
| 0 1   | 0 1   | 0 1   | 1 0       |
| 0 1   | 1 0   | 1 0   | 1 1       |
| 0 1   | 1 1   | 1 1   | 1 0       |
| 1 0   | 0 0   | 0 0   | 0 0       |
| 1 0   | 0 1   | 0 1   | 0 1       |
| 1 0   | 1 0   | 0 1   | 0 1       |
| 1 0   | 1 1   | 0 1   | 0 1       |
| 1 1   | 0 0   | 1 0   | 1 1       |
| 1 1   | 0 1   | 1 0   | 1 1       |
| 1 1   | 1 0   | 1 0   | 1 1       |
| 1 1   | 1 1   | 1 1   | 1 1       |

$$V_{OUT} = \overline{L_H} \overline{L_L} + \overline{L_H} V_{OUT} + L_L T_C$$

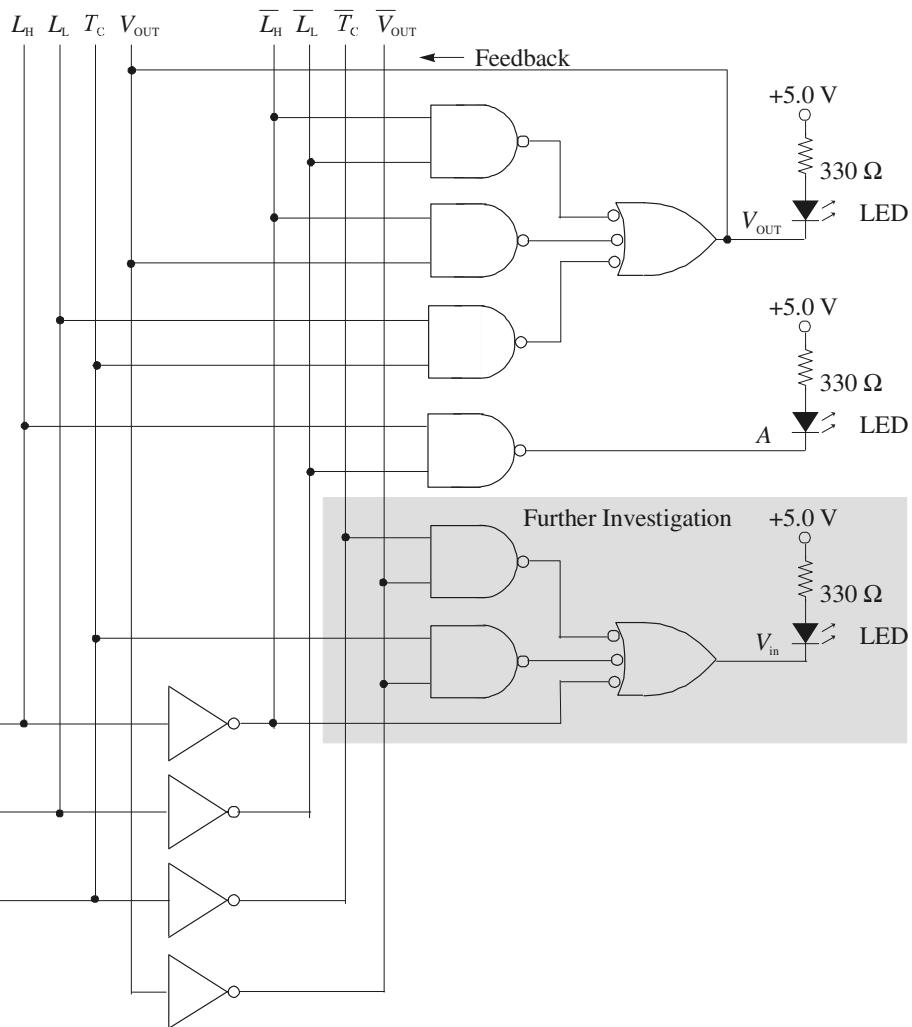
| $L_H$ | $L_L$ | $T_C$ | $V_{OUT}$ |
|-------|-------|-------|-----------|
| 0 0   | 0 0   | 0 0   | 1 1       |
| 0 0   | 0 1   | 0 1   | 0 1       |
| 0 0   | 1 0   | 1 0   | 1 1       |
| 0 0   | 1 1   | 1 1   | 1 0       |
| 0 1   | 0 0   | 0 0   | 1 1       |
| 0 1   | 0 1   | 0 1   | 1 0       |
| 0 1   | 1 0   | 1 0   | 1 1       |
| 0 1   | 1 1   | 1 1   | 1 0       |
| 1 0   | 0 0   | 0 0   | 0 0       |
| 1 0   | 0 1   | 0 1   | 0 1       |
| 1 0   | 1 0   | 0 1   | 0 1       |
| 1 0   | 1 1   | 0 1   | 0 1       |
| 1 1   | 0 0   | 1 0   | 1 1       |
| 1 1   | 0 1   | 1 0   | 1 1       |
| 1 1   | 1 0   | 1 0   | 1 1       |
| 1 1   | 1 1   | 1 1   | 1 1       |

$$A = \overline{L_H} + L_L = \overline{L_H} \cdot \overline{L_L}$$

| $L_H$ | $L_L$ | $T_C$ | $V_{OUT}$ |
|-------|-------|-------|-----------|
| 0 0   | 0 0   | 0 0   | 1 0       |
| 0 0   | 0 1   | 1 0   | 0 1       |
| 0 0   | 1 0   | 0 0   | 1 0       |
| 0 0   | 1 1   | 1 1   | 1 1       |
| 0 1   | 0 0   | 0 0   | 1 1       |
| 0 1   | 0 1   | 1 0   | 0 1       |
| 0 1   | 1 0   | 0 0   | 1 1       |
| 0 1   | 1 1   | 1 1   | 1 1       |
| 1 0   | 0 0   | 0 0   | 0 0       |
| 1 0   | 0 1   | 0 1   | 0 1       |
| 1 0   | 1 0   | 0 1   | 0 1       |
| 1 0   | 1 1   | 0 1   | 0 1       |
| 1 1   | 0 0   | 1 0   | 1 1       |
| 1 1   | 0 1   | 1 0   | 1 1       |
| 1 1   | 1 0   | 1 1   | 1 1       |
| 1 1   | 1 1   | 1 1   | 1 1       |

$$V_{IN} = \overline{T_C} \overline{V_{OUT}} + T_C \overline{V_{OUT}} + L_H$$

| $L_H$ | $L_L$ | $T_C$ | $V_{OUT}$ | $A$ | $V_{IN}$ |
|-------|-------|-------|-----------|-----|----------|
| 0 0   | 0 0   | 0 0   | 1 1       | 1   | 1        |
| 0 0   | 0 1   | 0 1   | 1 0       | 1   | 0        |
| 0 0   | 1 0   | 1 0   | 1 1       | 1   | 1        |
| 0 0   | 1 1   | 1 1   | 1 0       | 1   | 0        |
| 0 1   | 0 0   | 0 0   | 1 1       | 1   | 1        |
| 0 1   | 0 1   | 0 1   | 1 0       | 1   | 0        |
| 0 1   | 1 0   | 1 0   | 1 1       | 1   | 1        |
| 0 1   | 1 1   | 1 1   | 1 0       | 1   | 0        |
| 1 0   | 0 0   | 0 0   | 0 0       | 0   | 1        |
| 1 0   | 0 1   | 0 1   | 0 1       | 0   | 1        |
| 1 0   | 1 0   | 0 1   | 0 1       | 0   | 1        |
| 1 0   | 1 1   | 0 1   | 0 1       | 0   | 1        |
| 1 1   | 0 0   | 1 0   | 1 1       | 1   | 1        |
| 1 1   | 0 1   | 1 0   | 1 1       | 1   | 1        |
| 1 1   | 1 0   | 1 1   | 1 1       | 1   | 1        |
| 1 1   | 1 1   | 1 1   | 1 1       | 1   | 1        |



### Data and Observations (VHDL)

The truth table and maps are the same as the TTL section. The completed program is shown below with student inputs in **bold**.

```
library ieee;
use ieee.std_logic_1164.all;
entity Molassas2 is
 port(Lh, Li, Tc: in std_logic;
 Vout, Vin, A: inout std_logic);
end entity Molassas2;

architecture Behavior of Molassas2 is
begin
 Vout <= not((not Lh and not Li) or (not Lh and not Vout) or (Li and Tc));
 Vin <= not((not Tc and Vout) or (Tc and Vout) or Lh);
 A <= not(not Lh or Li);
end architecture Behavior;
```

**Figure 10-5**

### Further Investigation Results (VHDL)

The heater logic is shown in bold, added to the original program that was in Figure 10-5. The entity name was changed.

```
library ieee;
use ieee.std_logic_1164.all;
entity MolassasFI is
 port(Lh, Li, Tc: in std_logic;
 Vout, Vin, A, Heater: inout std_logic);
end entity MolassasFI;

architecture Behavior of MolassasFI is
begin
 Vout <= not((not Lh and not Li) or (not Lh and not Vout) or (Li and Tc));
 Vin <= not((not Tc and not Vout) or (Tc and not Vout) or Lh);
 A <= not(not Lh or Li);
 Heater <= Tc and Li;
end architecture Behavior;
```

### Review Questions (VHDL)

1. No. inout is bidirectional allowing data to be written and read from the same port.
2. Bidirectional mode such as inout and buffer allows for feedback in the case of the molassas tank where valve status is required.
3. In the case of the Vout signal, the open or close state drives the logic for the next state and is not directly accessible.

# Experiment 11 Adder and Magnitude Comparator

## Data and Observations

The connections to the adder needed to complete the circuit in Figure 11-2 for a binary to excess-three conversion circuit are:

| input:         | connect to:      |
|----------------|------------------|
| B <sub>4</sub> | A>B              |
| B <sub>3</sub> | Ground           |
| B <sub>2</sub> | $\overline{A>B}$ |
| B <sub>1</sub> | +5.0 V           |
| C <sub>0</sub> | Ground           |

Results for the binary to excess-3 conversion are given in Table 11-4. The inverters are considered part of the display, therefore, logic shown on Table 11-4 is before the 7404 inverters (a logic 1 turns ON an LED).

## Further Investigation Results:

TABLE 11-4

Truth table for Figure 11-2

| Inputs<br>(Binary) |   |   |   | Outputs<br>(Excess-3) |   |   |   |   |
|--------------------|---|---|---|-----------------------|---|---|---|---|
| D                  | C | B | A | A'                    | D | C | B | A |
| 0                  | 0 | 0 | 0 | 0                     | 0 | 0 | 1 | 1 |
| 0                  | 0 | 0 | 1 | 0                     | 0 | 1 | 0 | 0 |
| 0                  | 0 | 1 | 0 | 0                     | 0 | 1 | 0 | 1 |
| 0                  | 0 | 1 | 1 | 0                     | 0 | 1 | 1 | 0 |
| 0                  | 1 | 0 | 0 | 0                     | 0 | 1 | 1 | 1 |
| 0                  | 1 | 0 | 1 | 0                     | 1 | 0 | 0 | 0 |
| 0                  | 1 | 1 | 0 | 0                     | 1 | 0 | 0 | 1 |
| 0                  | 1 | 1 | 1 | 0                     | 1 | 0 | 1 | 0 |
| 1                  | 0 | 0 | 0 | 0                     | 1 | 0 | 1 | 1 |
| 1                  | 0 | 0 | 1 | 0                     | 1 | 1 | 0 | 0 |
| 1                  | 0 | 1 | 0 | 1                     | 0 | 0 | 1 | 1 |
| 1                  | 0 | 1 | 1 | 1                     | 0 | 1 | 0 | 0 |
| 1                  | 1 | 0 | 0 | 1                     | 0 | 1 | 0 | 1 |
| 1                  | 1 | 0 | 1 | 1                     | 1 | 0 | 1 | 0 |
| 1                  | 1 | 1 | 0 | 1                     | 0 | 1 | 1 | 1 |
| 1                  | 1 | 1 | 1 | 1                     | 1 | 1 | 0 | 0 |

TABLE 11-5

Truth table for overflow error.

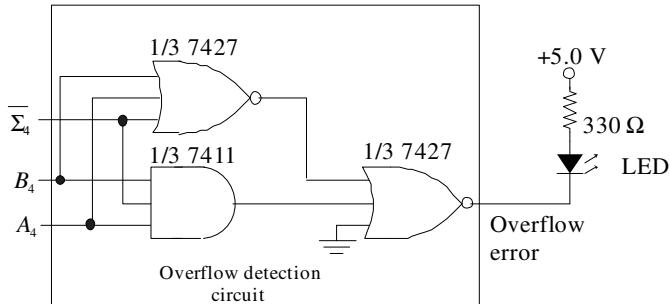
| Inputs                                   | Output |
|------------------------------------------|--------|
| A <sub>4</sub> B <sub>4</sub> $\Sigma_4$ | X      |
| 0 0 0                                    | 0      |
| 0 0 1                                    | 1      |
| 0 1 0                                    | 0      |
| 0 1 1                                    | 0      |
| 1 0 0                                    | 0      |
| 1 0 1                                    | 0      |
| 1 1 0                                    | 1      |
| 1 1 1                                    | 0      |

$$\Sigma_4 = A_4 B_4 \Sigma_4$$

$$X = A_4 B_4 \overline{\Sigma_4} + \overline{A_4} B_4 \Sigma_4$$

$$X = A_4 B_4 \overline{\Sigma_4} + A_4 B_4 \overline{\Sigma_4}$$

FIGURE 11-5  
Karnaugh map for overflow error.



## Evaluation and Review Questions:

- a. The input to the 7404 will see an illegal logic HIGH, causing the A' LED to be on.  
b. Approx 1.6 V.
- The carry-out ( $C_4$ ) of the lower order adder is connected to the carry-in ( $C_0$ ) of the higher order adder. The schematic (using 74LS83A ICs) is shown in text as Figure 8-13.
- It is the carry-in.
- Connect the  $B$  inputs of the upper 7485 to 1000 and the lower comparator  $B$  inputs to 1100. Connect cascading inputs on both so that  $A=B$  inputs are HIGH; all other cascading inputs are LOW.
- To form the two's complement, invert the bits of the subtrahend and add one by connecting the carry-in to a HIGH.
- An additional voting switch can be connected to the carry-in logic of the parallel adders.

## Experiment 12: Combinational Logic Using Multiplexers

### Data and Observations

**TABLE 12-1**

Truth table for 2-bit comparator  $A \geq B$ .

| Inputs |       |       | Output | Connect Data to: |
|--------|-------|-------|--------|------------------|
| $A_2$  | $A_1$ | $B_2$ | $B_1$  |                  |
| 0      | 0     | 0     | 0      | 1                |
| 0      | 0     | 0     | 1      | 0                |
| 0      | 0     | 1     | 0      | 0                |
| 0      | 0     | 1     | 1      | 0                |
| 0      | 1     | 0     | 0      | 1                |
| 0      | 1     | 0     | 1      | 1                |
| 0      | 1     | 1     | 0      | 0                |
| 0      | 1     | 1     | 1      | 0                |
| 1      | 0     | 0     | 0      | 1                |
| 1      | 0     | 0     | 1      | 1                |
| 1      | 0     | 1     | 0      | 1                |
| 1      | 0     | 1     | 1      | 0                |
| 1      | 1     | 0     | 0      | 1                |
| 1      | 1     | 0     | 1      | 1                |
| 1      | 1     | 1     | 0      | 1                |
| 1      | 1     | 1     | 1      | 1                |

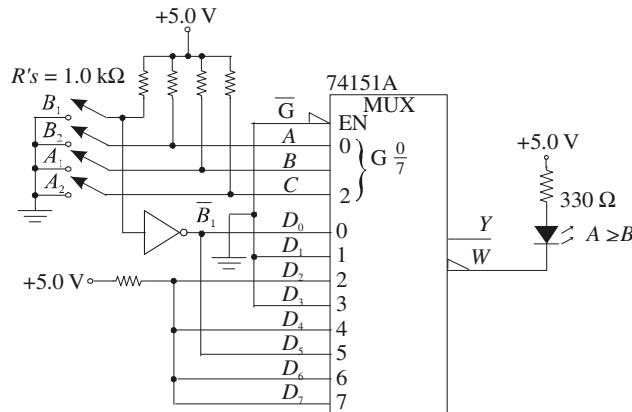
### Further Investigation Results

**TABLE 12-2**

Truth table for even parity generator.

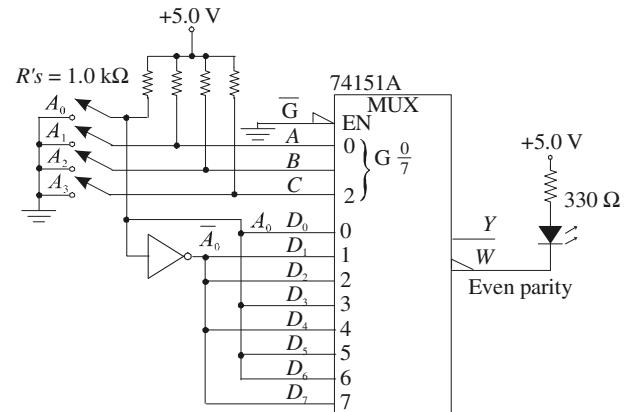
| Inputs |       |       | Output | Connect Data to: |
|--------|-------|-------|--------|------------------|
| $A_3$  | $A_2$ | $A_1$ | $A_0$  |                  |
| 0      | 0     | 0     | 0      | 0                |
| 0      | 0     | 0     | 1      | 1                |
| 0      | 0     | 1     | 0      | 1                |
| 0      | 0     | 1     | 1      | 0                |
| 0      | 1     | 0     | 0      | 1                |
| 0      | 1     | 0     | 1      | 0                |
| 0      | 1     | 1     | 0      | 0                |
| 0      | 1     | 1     | 1      | 1                |
| 1      | 0     | 0     | 0      | 1                |
| 1      | 0     | 0     | 1      | 1                |
| 1      | 0     | 1     | 0      | 0                |
| 1      | 0     | 1     | 1      | 1                |
| 1      | 1     | 0     | 0      | 0                |
| 1      | 1     | 0     | 1      | 1                |
| 1      | 1     | 1     | 0      | 1                |
| 1      | 1     | 1     | 1      | 0                |

Circuit:



**Figure 12-4**

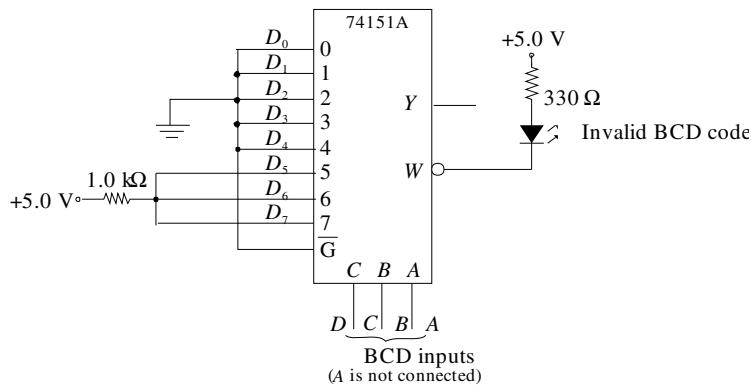
Circuit:



**Figure 12-5**

### Evaluation and Review Questions:

1. The BCD invalid code detector can be designed as shown:



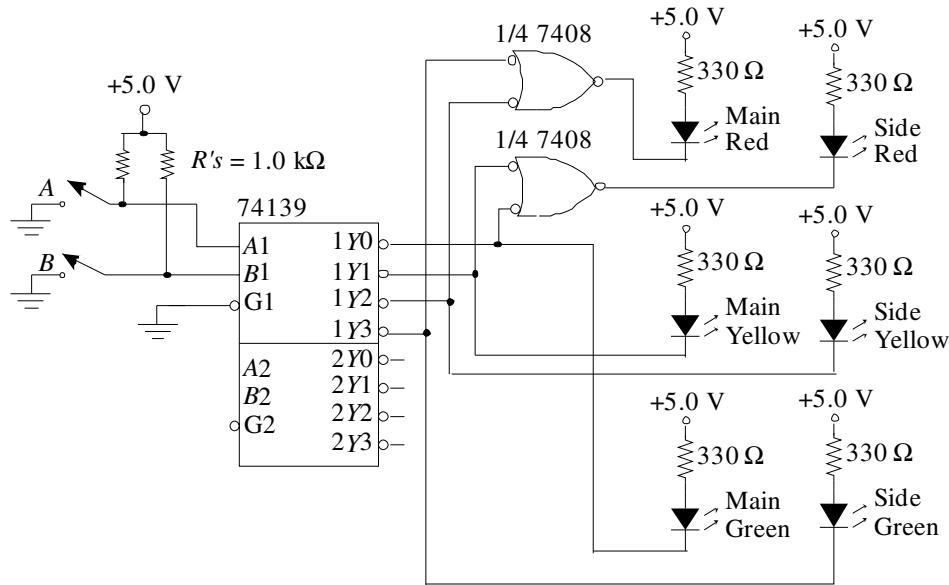
$$2. \quad A_2 \bar{A}_1 \bar{A}_0 + \bar{A}_2 \bar{A}_1 A_0 + A_2 \bar{A}_1 A_0 + A_2 A_1 \bar{A}_0$$

3. The input which affects the second half of the truth table is the  $A_2$  input. Place the circuit in a fault condition and check the inputs to the multiplexer beginning with the  $A_2$  input.
4. The inverter output is used with minterms 0, 1, 10, and 11. However it will be incorrect only when  $B_1$  should be HIGH - which is a fault condition for minterm 0 and 10. Place the circuit in one of these fault conditions and check the appropriate inputs to the multiplexer. Since the multiplexer input is incorrect, the troubleshooter is led to test the inverter and discover the fault.
5. The lines on the truth table that would be incorrect are  $A_2 A_1 B_2 B_1 = 0 0 0 1$  and  $A_2 A_1 B_2 B_1 = 1 0 1 1$ . All other lines will read correctly.
6. Odd parity can be obtained from the  $Y$  output of the 74151A.

## Experiment 13: Combinational Logic Using Demultiplexers

### Traffic Light Output logic (Figure 13-6):

Connect 1Y<sub>1</sub> to Main Yellow and to Side Red through the 7408 AND gate. Connect 1Y<sub>3</sub> to Main Red through a 7408 AND gate and to Side Green. Connect 1Y<sub>2</sub> to Main Red through a 7408 AND gate and to Side Yellow. The enable (G<sub>1</sub>) is wired LOW with switches to the A<sub>1</sub> and B<sub>1</sub> select inputs. The circuit is shown below:



### Further Investigation Results (TTL)

The NAND gate serves as a decoder for a particular output state from the counter. The decoded output then enables the decoder and lights a corresponding LED. As long as the CLK input to the counter is above approximately 100 Hz, the LED appears to be on steady. Different LEDs can be selected by changing the decoder's inputs.

### Evaluation and Review Questions:

1. Use one-half of the 74LS139A for the least significant four bits and the other half for the most significant four bits. Use the enable input on each decoder for the third select input, inverting it for the most significant four bits.
2. To emphasize the active-LOW inputs and outputs.
3. Gray code is useful to prevent glitches in the decoded outputs.
4. a. The input is an illegal HIGH, preventing the 1Y<sub>0</sub> and the 1Y<sub>1</sub> outputs from being selected.  
b. The input is LOW, preventing the 1Y<sub>2</sub> and the 1Y<sub>3</sub> outputs from being selected.  
c. The chip is not selected; therefore all outputs will be HIGH.
5. The sequence of the lights would be incorrect. This can be corrected by reversing the output logic for states 2 and 3. The disadvantage is possible glitches in the decoded outputs.
6. Connect the C input to the enable (G<sub>1</sub>) input. This enables the decoder only if C is LOW. Then connect the yellow lights through XOR gates. This logic is easy to show using a truth table. The second line of the truth table cannot occur so it is shown as a "don't care". The truth table is seen to be equivalent to an XOR gate if a 1 is substituted for the "don't care".

## Experiment 14: The D Latch and D Flip-Flop

Step 3 Observations: The output of the latch changes only when the switch makes initial contact with the A or B terminals. The latch does not change when the switch is "bounced".

Step 5 Observations: As long as the enable is HIGH, the output ( $Q$ ) follows the pulse generator input. When enable is LOW, changes on the D input are not seen on the output, however; the outputs can be latched by grounding either one momentarily, even when enable is not asserted.

Step 6 Observations: The burglar alarm basically illustrates the functions of the D latch. When enable is asserted HIGH, the opening of a door or window switch causes the alarm LED to latch on. Closing the door or window switch has no effect on the output. The alarm LED is turned off by closing all switches (or placing it in standby) and pressing the reset pushbutton.

Step 7 and 8 Observations: The setup time specification for a 7474 is 20 ns. The four inverters provide sufficient setup time to read the pulse as a HIGH, causing the output to remain a constant HIGH. When the delay is removed, the output is a constant LOW.

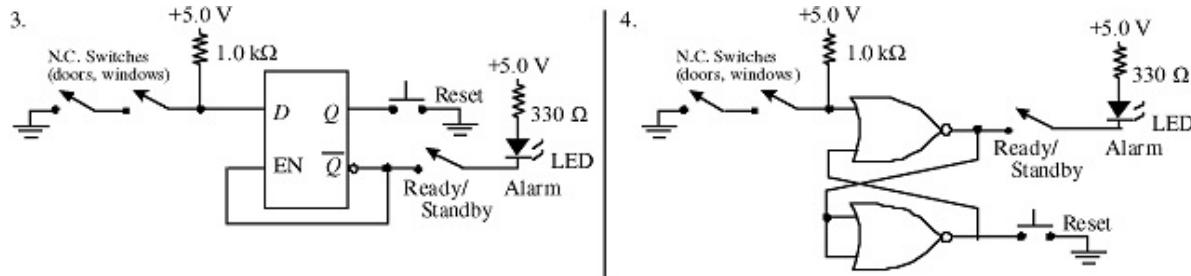
Step 10 Observations: The D flip-flop needs setup time as shown with the clock delay circuit. When sufficient setup time is given, the output will go HIGH; otherwise, it is LOW. The preset and clear inputs are asserted with a LOW input and are observed to be asynchronous inputs. With the clock delay in place and connecting the  $Q$  to D, the scope signal can be made to appear as if timing is changing when in fact it is not. (Trigger from the clock to show the timing problem).

### Further Investigation Results:

The serial parity test circuit changes the parity every time a logic 1 is received but does not change parity when a logic 0 is received. The circuit has an advantage over the parallel parity test circuit in Floyd's text only when the data is already in serial form and needs to be tested. In this case, the serial tester circuit is simpler and just as fast.

### Evaluation and Review Questions:

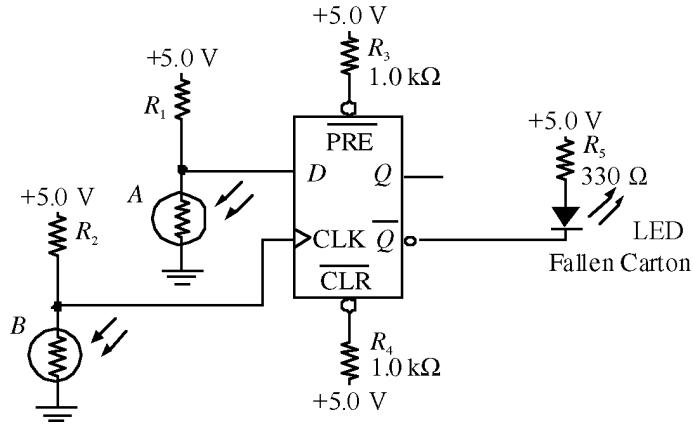
1. The switch debounce circuit requires two contacts (throws) because the output will not change if a single contact were used.
2. No. With NOR gates, the output would change as the switch pole is first moved from the contact but the other NOR gate output would be unaffected – causing bouncing to be seen on the output. A similar problem would occur on the other contact.



5. There are several possibilities. Among them are:
  1. Reset or enable switch stuck LOW.
  2. Open path to the alarm LED including open resistor or open diode.
  3. Faulty NAND gate (open output on lower right NAND gate, shorted output on top right gate, etc.)  
The most likely fault is an open connection rather than a faulty component.
6. A latch would oscillate very rapidly whenever the data was high.

## Experiment 15: The Fallen Carton Detector

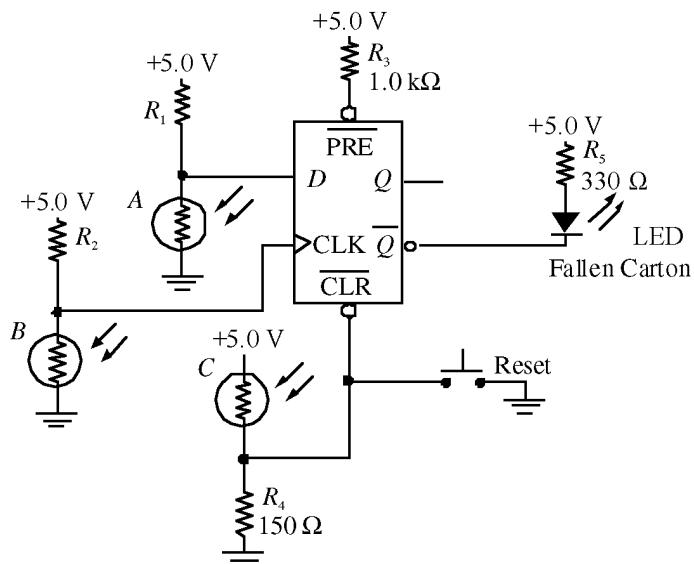
The fallen carton detector is a sequential logic circuit which is designed to detect if a carton, moving on a conveyor belt, is upright or has fallen over. If the carton has fallen, the circuit is to trip a solenoid (indicated by an LED). The circuit can be implemented with a D flip-flop as shown. Student circuits may vary.



Students will need to experiment to determine optimum series resistors ( $R_1$  and  $R_2$ ) to use with the photocells and with the particular room lighting. With a CdS photocell, a value of about 10 kΩ worked in normal room light when connected to a 7474 D flip-flop. The voltage will be LOW when uncovered (<0.2 V) and will be HIGH (>3.0 V) when covered.

### Further Investigation Results:

As the carton is sent into the reject hopper, a photocell can sense its presence. The photocell output can be connected to the CLR input of the D flip-flop to produce a LOW input when it is covered by reversing the photocell and the series resistor. Because TTL logic requires more current to pull it down, the value of  $R_4$  must be much smaller than in the first circuit. A value of 150 Ω works well with the photocell and the particular room light tested. A reset button is also connected to the CLR input of the D flip-flop. The modified circuit is shown below.



## Experiment 16: The J-K Flip-Flop

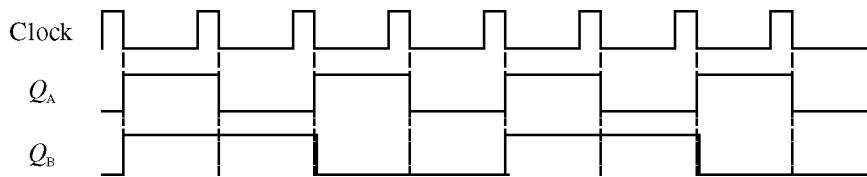
### Data and Observations

Step 1 Observations: The preset and clear inputs are asserted with a LOW input and are asynchronous. When both are LOW at the same time, both  $Q$  and  $\bar{Q}$  are HIGH.

Step 2 Observations: The truth table is verified –  $Q$  follows  $J$  when the  $J$  and  $K$  inputs are different. The output does not change when both inputs are LOW and the output toggles when the inputs are both HIGH. The output is observed to change on the trailing edge of the clock. The output duty cycle is seen to be 50%.

Step 3 Observations: The circuit toggles for each clock pulse.

Step 4 Observations: The ripple counter divides the input frequency in two as shown in the timing diagram:



**Plot 1**

### Further Investigation Results:

Measured  $t_{PLH} = 20$  ns. Manufacturer's specified  $t_{PLH} = 16$  ns (typ), 25 ns (max).

Measured  $t_{PHL} = 25$  ns. Manufacturer's specified  $t_{PHL} = 25$  ns (typ), 40 ns (max).

### Evaluation and Review Questions:

1. An asynchronous input is independent of the clock and can affect the output without the presence of a clock signal. A synchronous input can only affect the output when a clock signal is present.
2. a. Assert the preset input ( $\overline{PRE}$ ) which is asynchronous.  
b. Clock the flip-flop when  $J$  is HIGH and  $K$  is LOW.
3. The output is latched.
4. If  $Q$  is connected to  $J$  and  $\overline{Q}$  is connected to  $K$ , the clock will not change the output logic.
5. The CLK input is open; the Q output is shorted LOW; the  $\overline{CLR}$  input is shorted LOW.
6. Green LED could be open,  $330 \Omega$  resistor open, +5.0 V supply not connected to  $330 \Omega$  resistor, bad 74LS76.

## Experiment 17: One Shots and Astable Multivibrators

**TABLE 17-1**

Data for 74121 monostable multivibrator

| Quantity                      | Computed Value | Measured Value |
|-------------------------------|----------------|----------------|
| Timing Resistor, $R_T$        | <b>7.14 kΩ</b> | <b>6.89 kΩ</b> |
| External Capacitor, $C_{EXT}$ | <b>0.01 μF</b> | <b>0.01 μF</b> |
| Pulse width, $t_W$            | <b>48.2 μs</b> | <b>46.0 μs</b> |

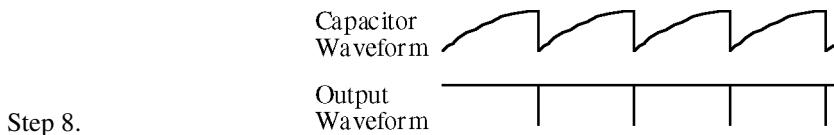
**TABLE 17-2**

Data for 555 timer as an astable multivibrator

| Quantity         | Computed Value  | Measured Value  |
|------------------|-----------------|-----------------|
| Resistor, $R_1$  | <b>7.5 kΩ</b>   | <b>7.46 kΩ</b>  |
| Resistor, $R_2$  | <b>10 kΩ</b>    | <b>10.1 kΩ</b>  |
| Capacitor, $C_1$ | <b>0.01 μF</b>  | <b>0.01 μF</b>  |
| Frequency        | <b>5.24 kHz</b> | <b>5.50 kHz</b> |
| Duty Cycle       | <b>0.64</b>     | <b>0.66</b>     |

Step 3. Input logic levels and generator connection: To trigger the 74121 with a leading edge clock, either  $A_1$  or  $A_2$  must be held LOW and the signal generator is connected to the  $B$  input.

Step 5. Observations as the frequency is raised to 50 kHz: The pulse width remains the same; it does not stay HIGH when the frequency is increased.



**Plot 1**

Step 9. Observations with a short across  $R_2$ : The output stays HIGH except for a short "spike" that appears each time a new cycle is initiated.

Step 10. Various solutions are possible. One solution is to modify the circuit shown in Figure 17-2 by changing  $R_2$  to 3.3 kΩ. (The calculated value is 3.45 kΩ.)

### Further Investigation Results

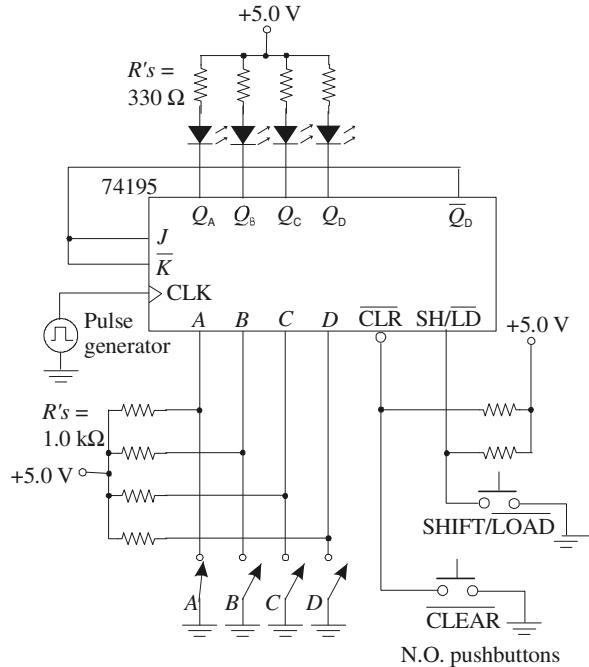
Both timers need trailing edge triggers that can be obtained on the 74121 by connecting  $A_1$  and  $A_2$  together and connecting  $B$  HIGH (see Figure 17-1). The manufacturer specifies that the external resistor cannot be larger than 40 kΩ. An approximate 4-s pulse can be obtained by selecting a 150 μF capacitor and a 39 kΩ resistor as shown in Figure 17-1 (computed = 4.1 s). A 25 s pulse can be obtained by selecting a 1000 μF capacitor and a 36 kΩ resistor (computed = 25.2 s).

### Evaluation and Review Questions:

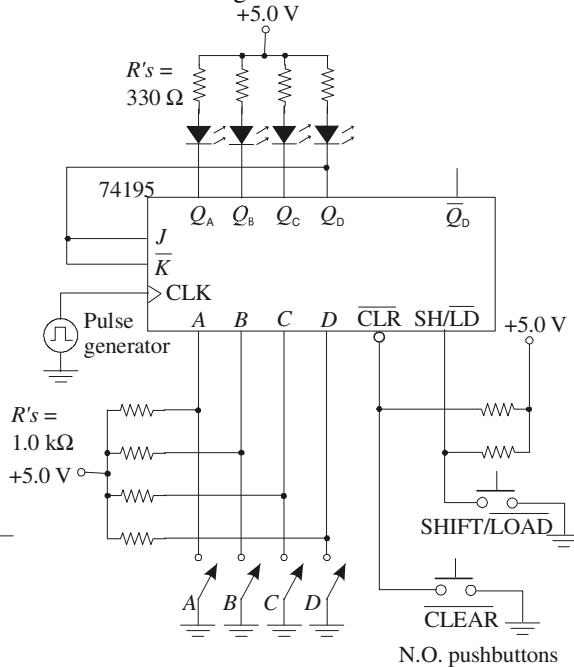
1. A non-retriggerable monostable ignores any triggers that occur during the timing cycle.
2. a. 0.036 μF.  
b. Select an external variable resistor. For the computed capacitance, the external resistance needs to vary from 2 kΩ to 10 kΩ.
3. Largest recommended resistor is 40 kΩ. The largest capacitor is 1000 μF. With this combination the pulse width is 28 seconds.
4. Duty cycle = 50.1%; frequency = 400 Hz.
5. The required frequency is 0.083 Hz. The sum of  $R_1 + 2R_2 = 1.72 \text{ M}Ω$ . From the duty cycle equation, the resistors are found to be:  $R_1 = 0.36 \text{ M}Ω$  and  $R_2 = 0.68 \text{ M}Ω$ .
6. The voltage ranges from +5.0 to +10.0 V.

## Experiment 18: Shift Register Counters

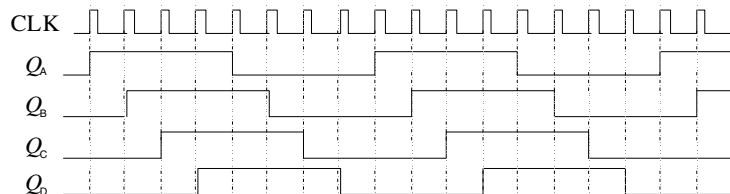
Schematic for Johnson Counter:



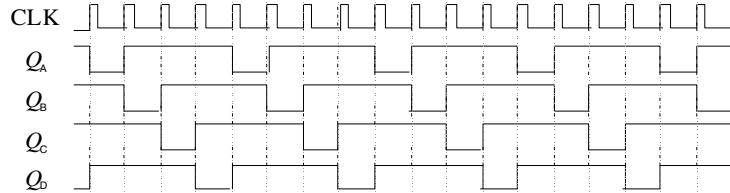
Schematic for Ring Counter:



Timing diagram for Johnson counter:

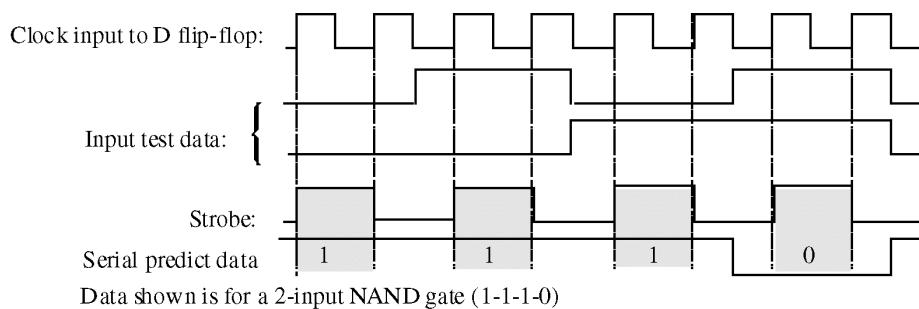


Timing diagram for ring counter loaded with 1110:



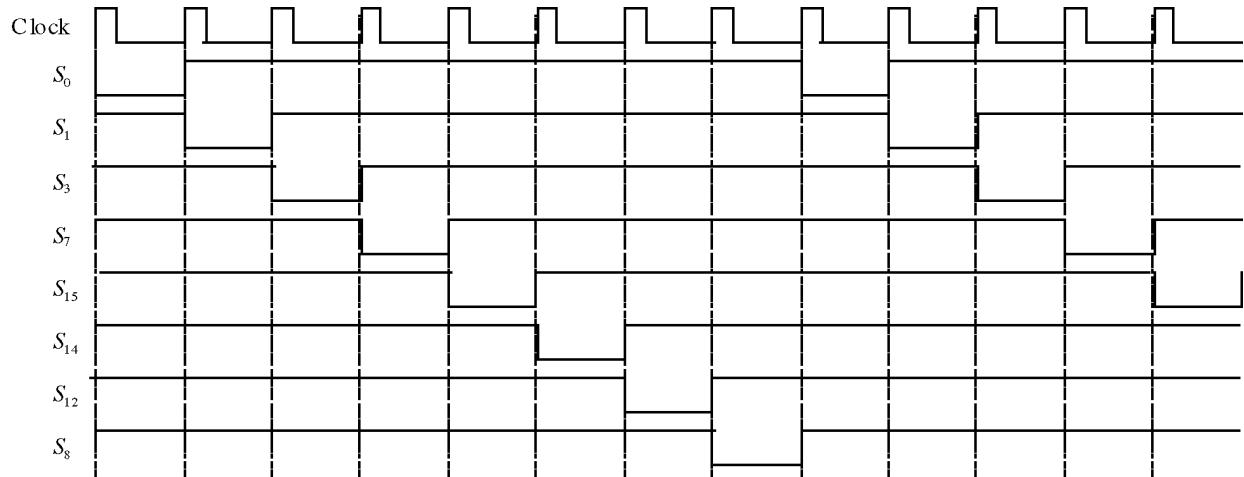
### Further Investigation Results

The **Serial predict data** is compared with the data from the device when the **Strobe** line goes HIGH as shown in the following timing diagram:



**Evaluation and Review Questions:**

1. The  $Q_D$  output of the first 74195 is connected to the  $J-K$  inputs of the second. The  $\bar{Q}_D$  output from the second 74195 is connected to the  $J-K$  inputs of the first.
2. To prevent the data from shifting more than one position for each clock pulse.
3. a. 101-110-011. b. 101-010-101. (An interesting but generally not useful result!).
4. After the stored data has been clocked out, the same input data will appear at all outputs.
5. The 8 active states are shown in the diagram. (Repeats after 8 states).



6. Politely tell the boss that a normal ring counter is self-decoding and that a decoder is not necessary.

## Experiment 19: Application of Shift Register Circuits

### Data and Observations:

Observations from step 2: After loading the data, the start bit flip-flop is observed to have a LOW (LED on). Data from the shift register can be seen to move to the right at each clock pulse. The data at the  $Q_A$  output moves to the *Serial data out* position after 5 clock pulses. The register is then filled with HIGHs (LEDs all off) until reloaded.

Sample calculation of the resistors for the 555 configured as an astable multivibrator are given. (See Figure 17-2 for the circuit for the astable configuration.)

$$f = \frac{1}{0.7(R_1 + 2R_2)C} = \frac{1}{1 \text{ ms}} \quad t_H = 0.8 \text{ ms} \quad t_L = 0.2 \text{ ms}$$

Let  $C = 0.1 \mu\text{F}$ .

Then:

$$R_1 + R_2 = \frac{t_H}{0.7 C} = \frac{0.8 \text{ ms}}{0.7(0.1 \mu\text{F})} = 11.4 \text{ k}\Omega$$

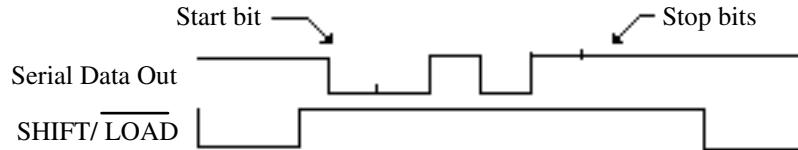
and

$$R_2 = \frac{t_L}{0.7 C} = \frac{0.2 \text{ ms}}{0.7(0.1 \mu\text{F})} = 2.86 \text{ k}\Omega \text{ (choose } 2.7 \text{ k}\Omega)$$

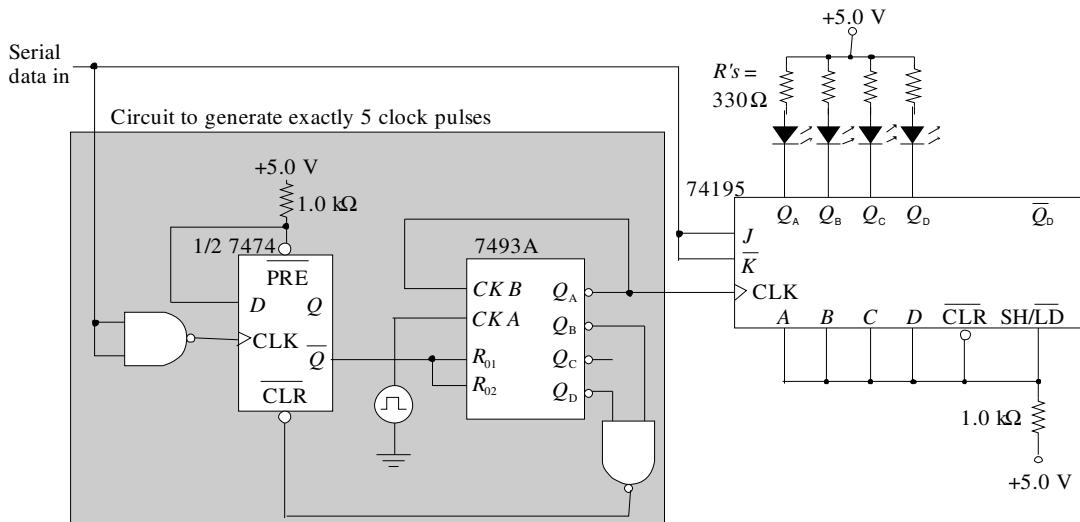
$$R_1 = 11.4 \text{ k}\Omega - 2.7 \text{ k}\Omega = 8.7 \text{ k}\Omega \text{ (choose } 9.1 \text{ k}\Omega)$$

With the values selected above, the duty cycle is 81% and the frequency is 985 Hz.

Step 4: Because of the asynchronous relation between the data clock and the SHIFT/LOAD pulse, the time between the serial data out and the SHIFT/LOAD and the start bit is not fixed.



Step 5: The circuit to send exactly five clock pulses is shown in the shaded box of the receiver. Only when the start bit is detected, is the data shifted in the 74195. The frequency of the pulse generator is set to twice that of the transmitter in order to generate one complete pulse with every two clocks. (The 7493A counts to ten during this process.)



**FIGURE 19–5**

#### Further Investigation Results:

The receiver pulse generator is set twice as fast as the transmitter's pulse generator because the circuit that generates 5 clock pulses divides the receiver frequency by two. The generator frequencies should be close to the 2-1 ratio, but it is not necessary to be exact. Five data pulses are used to send the start bit right through the receiver (into the "bit bucket"), moving only the data that was set at the transmitter into the receiver. The stop bits are represented by HIGHs, and since the line is held HIGH (no transition), the receiver will not be clocked until a new start bit is received.

#### Evaluation and Review Questions:(TTL)

1. The J-K inputs are connected HIGH. This HIGH is shifted into the 74195A at each clock pulse.
2. The first bit is a start bit which is not part of the data. The extra clock pulse causes it to be clocked through the receiver's shift register.
3. The start bit transition is a falling edge (HIGH to LOW). The NAND gate, which acts as an inverter, changes the active edge so that it can trigger the 7474 with a leading edge.
4.
  - a. The numbers to be added are entered into the input shift registers. The full adder produces the sum and the carry bit sequentially as each bit is shifted through the input registers. As the sum is produced, it is moved sequentially through the output shift register. The carry-out flip-flop stores the carry bit to be added to the next most significant bit.
  - b. The output shift register will contain 0011; the carry-out flip-flop will contain 1.
5. A 74195A shift register can be configured as a ring counter. The register is loaded with the pattern 1000 which is recirculated. The outputs are taken from either Q<sub>A</sub> and Q<sub>C</sub> or from Q<sub>B</sub> and Q<sub>D</sub>.
6. If the start bit flip-flop is loaded with a HIGH instead of a LOW, the start bit will not occur. This could occur if the clear input to the start bit flip-flop were open.

### Data and Observations:(VHDL)

The J-K flip flop program is given as a component in Figure 23-6 and is complete as shown. The completed program for the Johnson counter in Figure 23-7 is shown with student inputs in **bold**.

```

library IEEE;
use IEEE.std_logic_1164.all;

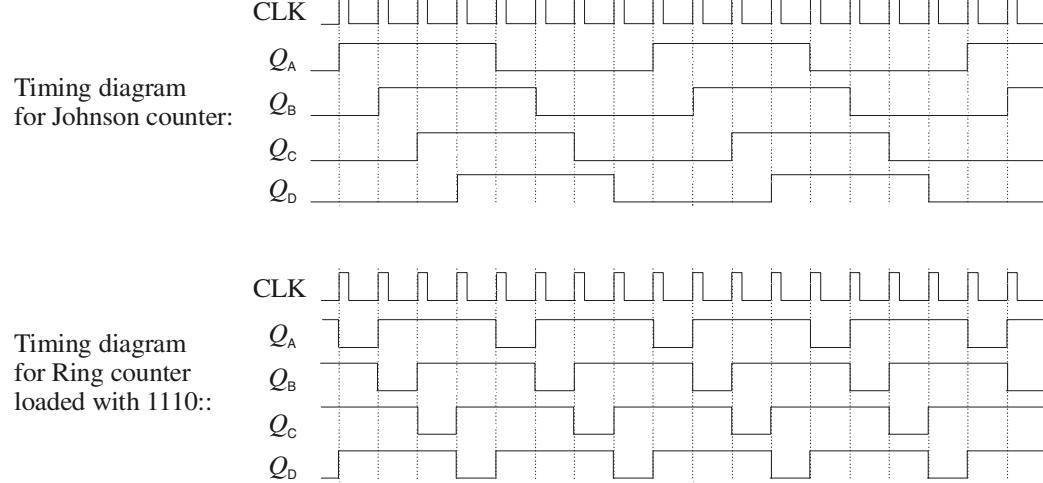
entity Counter is
 port (clock,ShiftLoad,A, B, C, D: in std_logic;
 A, QB, QC, QD: inout std_logic);
end entity Counter;

architecture CounterBehavior of Counter is
signal QANot, QBNot, QCNot, QDNot: std_logic;
signal Pre0, Pre1, Pre2, Pre3, Clr0, Clr1, Clr2, Clr3 : std_logic;

component JKFlipFlop is
 port (J, K, Clr, Pre, Clock: in std_logic;
 Q, QNot: inout std_logic);
end component JKFlipFlop;
begin
begin
 Pre0 <= A nand not ShiftLoad; Clr0 <= not A nand not ShiftLoad;
 Pre1 <= B nand not ShiftLoad; Clr1 <= not B nand not ShiftLoad;
 Pre2 <= C nand not ShiftLoad; Clr2 <= not C nand not ShiftLoad;
 Pre3 <= D nand not ShiftLoad; Clr3 <= not D nand not ShiftLoad;
 -- J and K are reversed for FF0
 FF0:JKFlipFlop port map (J=>QDNot,K=>QD,Clr=>Clr0,Pre=>Pre0,Clock=>clock,Q=>QA, QNot=>QANot);
 FF1:JKFlipFlop port map (J=>QA,K=>QANot,Clr=>Clr1,Pre=>Pre1,Clock=>clock,Q=>QB, QNot=>QBNot);
 FF2:JKFlipFlop port map (J=>QB,K=>QBNot,Clr=>Clr2,Pre=>Pre2,Clock=>clock,Q=>QC, QNot=>QCNot);
 FF3:JKFlipFlop port map (J=>QC,K=>QCNot,Clr=>Clr3,Pre=>Pre3,Clock=>clock,Q=>QD, QNot=>QDNot);
end architecture CounterBehavior;

```

**Figure 19-10**



### Further Investigation Results (VHDL)

Student inputs are shown in **bold**:

```

library ieee;
use ieee.std_logic_1164.all;
entity JKCounter is
 port (Clock, Shift_Load, Data0, Data1, Data2: in std_logic;
 QA, QB, QC: buffer std_logic);
end entity JKCounter;

```

```

architecture CounterBehavior of JKCounter is
signal QANot, QBNot, QCNot: std_logic;
signal Pre0, Pre1, Pre2, Clr0, Clr1, Clr2: std_logic;

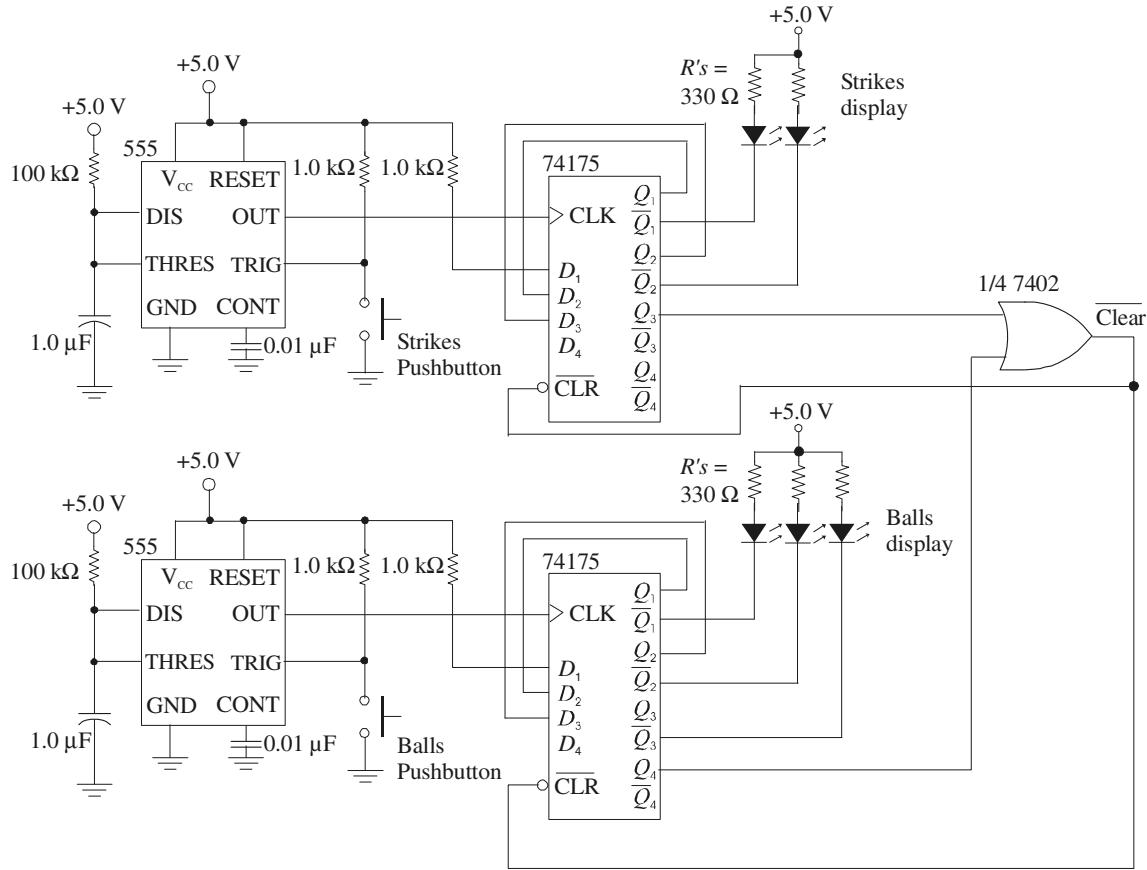
component JKFlipFlop is
port (J, K, Clr, Pre, Clock: in std_logic;
 Q, QNot: inout std_logic);
end component JKFlipFlop;
begin
 Pre0 <= Data0 nand Shift_Load; Clr0 <= not Data0 nand Shift_Load;
 Pre1 <= Data1 nand Shift_Load; Clr1 <= not Data1 nand Shift_Load;
 Pre2 <= Data2 nand Shift_Load; Clr2 <= not Data2 nand Shift_Load;
 FF0:JKFlipFlop port map (J=>QCNot,K=>QC,Clr=>Clr0,Pre=>Pre0,Clock=>Clock,Q=>QA,QNot=>QANot);
 FF1:JKFlipFlop port map (J=>QA,K=>QANot,Clr=>Clr1,Pre=>Pre1,Clock=>Clock,Q=>QB,QNot=>QBNot);
 FF2:JKFlipFlop port map (J=>QB,K=>QBNot,Clr=>Clr2,Pre=>Pre2,Clock=>Clock,Q=>QC,QNot=>QCNot);
end architecture CounterBehavior;

```

**Figure 19-13**

## Experiment 20: The Baseball Scoreboard

The baseball scoreboard is a sequential logic circuit that can be implemented with shift registers or with a counter. One possible solution, using 74175 quad D flip-flops connected as shift registers is shown. Switch debounce is provided by the 555 timers.



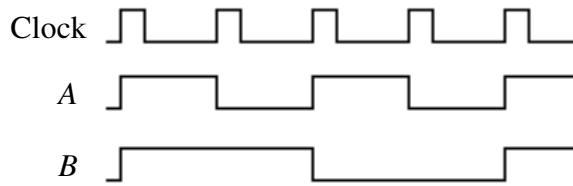
### Further Investigation Results (TTL)

Student answers will vary. The inning display can be set up as a 16-position shift register with a single LED on at any given time. Another approach is to use a 16-bit DMUX driven with a manually clocked 4-bit counter controlling the select inputs of the DMUX. Outs can be connected as a 2-bit shift register made from D flip-flops controlled by a debounced pushbutton, similar to the circuits shown above.

## Experiment 21: Asynchronous Counters

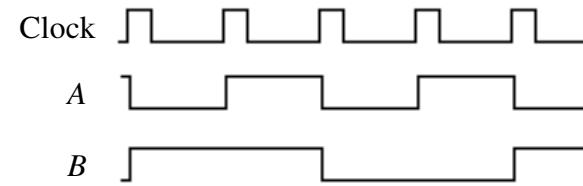
### Data and Observations

Waveforms from step 1:



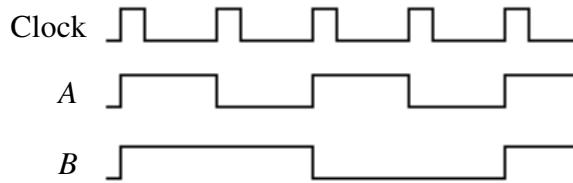
Counter is a down counter.

Waveforms from step 2:



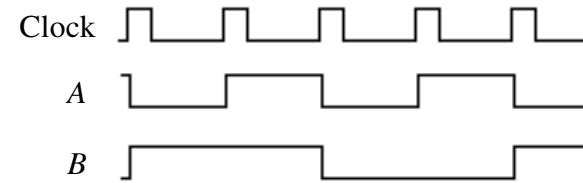
Counter is an up counter.

Waveforms from step 3: (same as step 1)



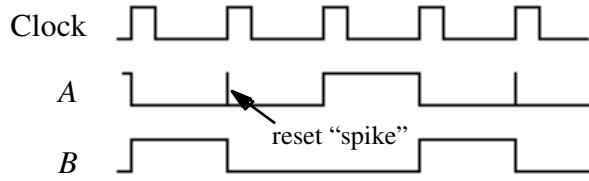
Counter is a down counter.

Waveforms from step 4: (same as step 2)



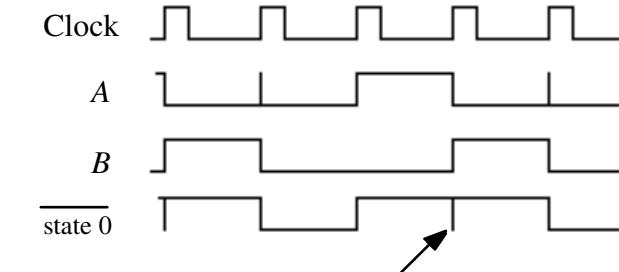
Counter is an up counter.

Waveforms from step 5:



Counter sequence is 0 - 1 - 2 - reset. The short "spike" is caused by the reset in state 3.

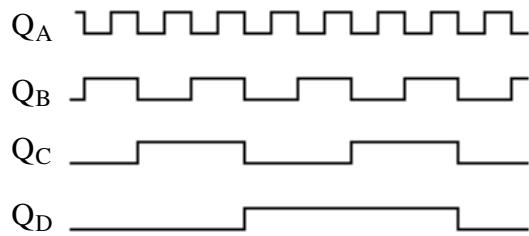
Waveforms from step 6:



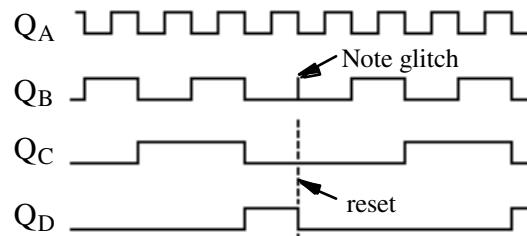
The decoded output shows a "glitch" when both A and B change together.

Notice that the "glitch" in step 5 is a consequence of detecting state 3 and using it to reset the counter. The "glitch" in the state zero decoded output is different. It is caused by the fact that the counter is momentarily in state zero due to propagation delay between the two flip-flops.

Waveforms from step 7:

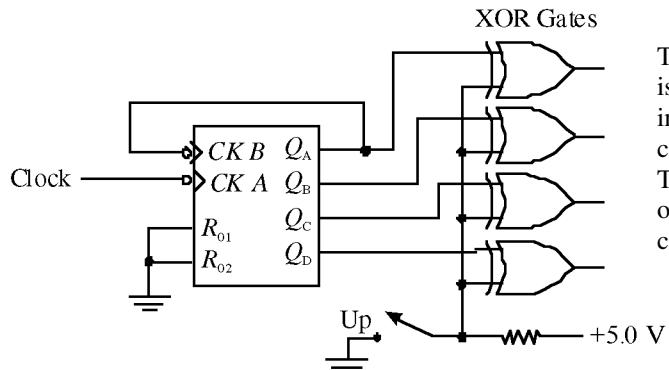


Waveforms from step 8:



The sequence is 0-1-2-3-4-5-6-7-8-9 - reset  
(momentarily in state 10)

### Further Investigation Results:



The XOR gates act as inverters when the Up switch is closed and act as buffers when it is open. By inverting or not inverting the waveforms, the counter can appear as an up or a down counter. The disadvantage of the method is that the reversal of the bits when the switch is open or closed will cause the count to change at the switching time.

### Evaluation and Review Questions:

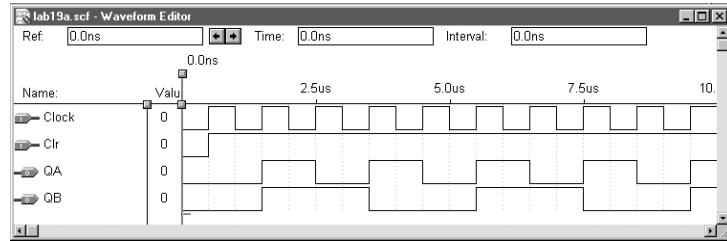
1. a. The A signal is 4X faster than the clock. Since the measurement shows that it is 4.00 kHz, the clock frequency is 1.00 kHz.  
b. If you want to check the time relationship of any other signal with respect to the displayed signals, it is easier to make the comparison with the slower waveform. Since it is a digital scope, the two channels are digitized together and so this reason is for convenience only. If this were an analog scope, a timing error can be made by triggering on a faster signal to observe (and compare) a slower signal.
2. a. The count sequence is truncated by decoding one number more than the ending number and using the decoded output to reset the counter.  
b. The procedure produces a glitch because the counter is in the decoded state for a very short interval.
3. The clear input may be shorted LOW, producing a HIGH output on both flip-flops; the line from  $Q$  to D on the A flip flop may be open causing an (invalid) HIGH to be clocked into the A flip-flop at each clock pulse.
4. The time relationship determined from a two channel oscilloscope could be interpreted incorrectly because the scope can be triggered by *any* arbitrary clock pulse. Relative timing is unambiguous when the various waveforms are compared to the slowest waveform.
5. a. Circuit:
- b. Waveforms:

6. The sequence is 0-1-2-3-4-5-8-9-reset (momentarily in state 10)

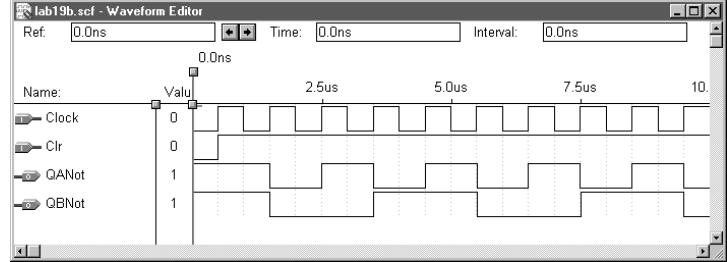
### Data and Observations (VHDL)

Note: Programs given in this experiment are complete as shown; the student and instructor programs are identical.

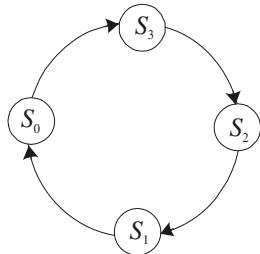
Step 8. Counter is a down counter. See Plot 9.



Step 11. Counter is an up counter. See Plot 10.



Step 14. State diagram:



### Further Investigation Results (VHDL)

Counter is an up counter. The program is different but the result in Plot 11 is identical to Plot 10.

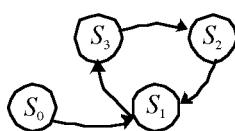
## Experiment 22: Analysis of Synchronous Counters with Decoding

**TABLE 22-2**

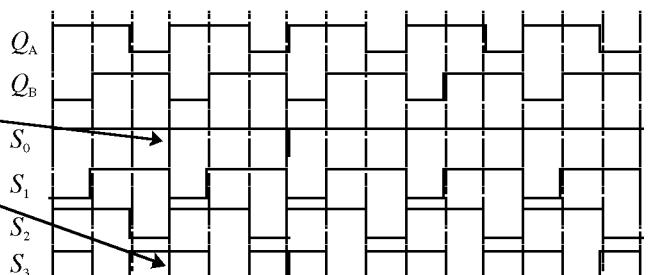
Analysis of synchronous counter  
shown in Figure 19-3

| Outputs | Inputs              |                   |           |             |
|---------|---------------------|-------------------|-----------|-------------|
|         | $J_B = Q_A$         | $K_B = \bar{Q}_A$ | $J_A = 1$ | $K_A = Q_B$ |
| 0 0     | 0                   | 1                 | 1         | 0           |
| 0 1     | 1                   | 0                 | 1         | 0           |
| 1 1     | 1                   | 0                 | 1         | 1           |
| 1 0     | 0                   | 1                 | 1         | 1           |
| 0 1     | <b>(Repeats...)</b> |                   |           |             |

State diagram:



Note the glitches in the decoders for state 0 and state 3



**Plot 1**

Step 4: State diagram:

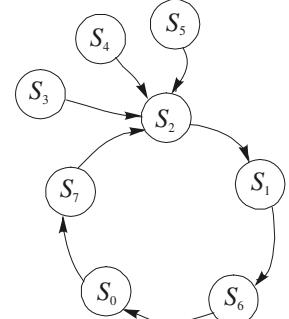


**TABLE 22-3**

Analysis of counter shown in Figure 22-4

Step 6: State diagram:

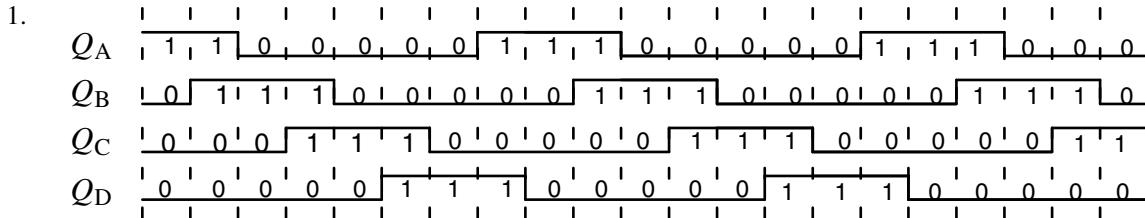
| Outputs | Inputs                                      |           |           |                   |                   |           |
|---------|---------------------------------------------|-----------|-----------|-------------------|-------------------|-----------|
|         | $J_C = \bar{Q}_A$                           | $K_C = 1$ | $J_B = 1$ | $K_B = \bar{Q}_A$ | $J_A = \bar{Q}_C$ | $K_A = 1$ |
| 0 0 0   | 1                                           | 1         | 1         | 1                 | 1                 | 1         |
| 1 1 1   | 0                                           | 1         | 1         | 0                 | 0                 | 1         |
| 0 1 0   | 0                                           | 1         | 1         | 1                 | 1                 | 1         |
| 0 0 1   | 1                                           | 1         | 1         | 0                 | 1                 | 1         |
| 1 1 0   | 0                                           | 1         | 1         | 1                 | 0                 | 1         |
| 0 0 0   | <b>Repeats..test unused states:</b>         |           |           |                   |                   |           |
| 0 1 1   | 0                                           | 1         | 1         | 0                 | 1                 | 1         |
| 0 1 0   | <b>Returns to a tested state (main seq)</b> |           |           |                   |                   |           |
| 1 0 0   | 1                                           | 1         | 1         | 1                 | 0                 | 1         |
| 0 1 0   | <b>Returns to a tested state (main seq)</b> |           |           |                   |                   |           |
| 1 0 1   | 1                                           | 1         | 1         | 0                 | 0                 | 1         |
| 0 1 0   | <b>Returns to a tested state (main seq)</b> |           |           |                   |                   |           |



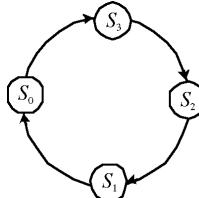
### Further Investigation Results:

The circuit shows the letters for the word C-L-U-E in the seven segment display.

### Evaluation and Review Questions:



2. The sequence is that of a down counter:



3. Full decoding means all possible states must be decoded. Because there are three outputs, full decoding can be accomplished with a 3 to 8 decoder such as the 74LS138.
4. Connect the pushbutton so that it clears the *A* and *C* counters and presets the *B* counter using the asynchronous clear and preset inputs.
5. The counter can be locked in state 3 if there are no clock pulses or if the common preset line is shorted LOW.
6. State 9 (*DCBA* = 1001) should go to state 1 (*DCBA* = 0001) but isn't changing. By observation, three of the F/F's do not change states for this transition (FFA, FFB, and FFC). FFD should change and isn't changing, so it is the likely culprit.

### Data and Observations (VHDL)

Data is the same as the TTL section, except the state outputs are active HIGH (for all active HIGH boards). Table 22-4 is the same as Table 22-2 in the TTL section. The state diagram is the same as in the TTL section but the timing diagram will show the active HIGH states as shown in Plot 2.

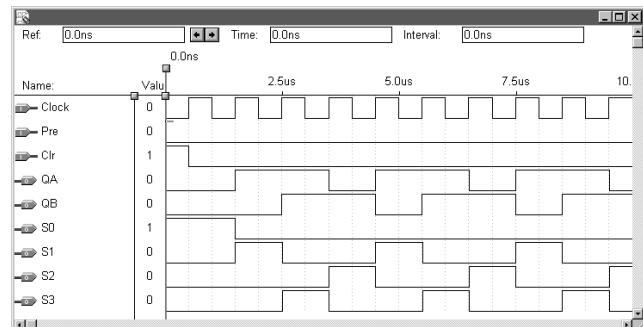
The equations for the flip-flops for the program in step 6 are shown in the following program segment. Student inputs are shown in **bold**:

```

Begin
 High <= '1';
 FF0: JKFlipFlop port map (J=>High,K=>QB,Clr=>Clr,Pre=>Pre,Clock=>Clock,Q=>QA, QNot=>QANot);
 FF1: JKFlipFlop port map (J=>QA,K=>QANot,,Clr=>Clr,Pre=>Pre,Clock=>Clock,Q=>QB, QNot=>QBNot);
 S0 <= QANot and QBNot;
 S1 <= QA and QBNot;
 S2 <= QANot and QB;
 S3 <= QA and QB;
end architecture Counter;

```

**Figure 22-8**(partial program shown)



**Plot 3**

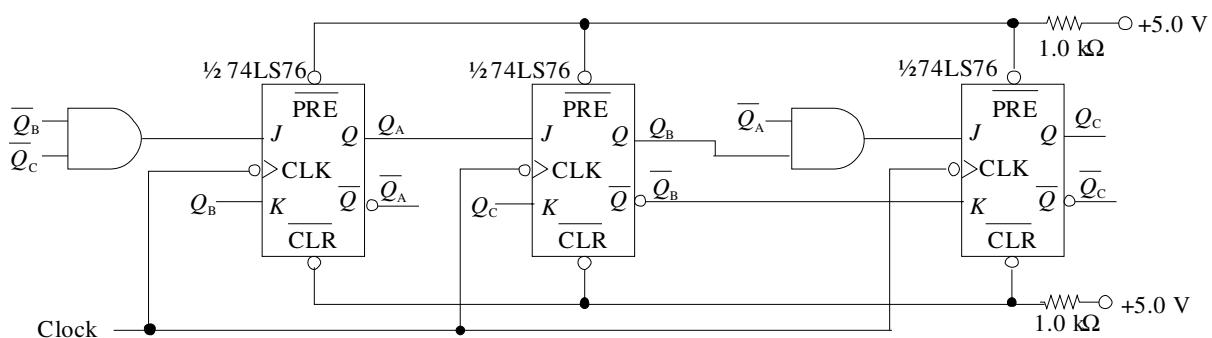
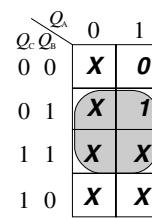
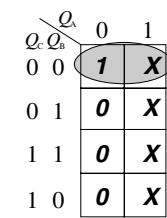
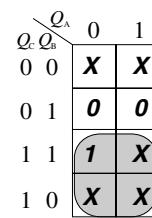
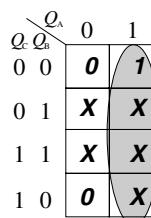
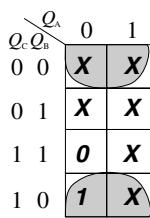
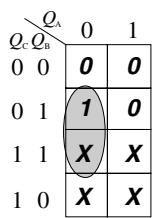
**Table 22-5 is the same as Table 22-3 in the TTL section, so both have identical state diagrams also.**

### Review Questions (VHDL)

- No hardware changes are needed.
- Implement the logic as a component that can be called three times to control each of the stepper motors.

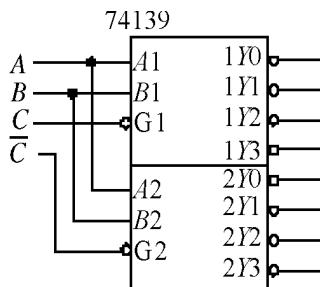
## Experiment 23: Design of Synchronous Counters

| Present State |       |       | Next State |       |       |
|---------------|-------|-------|------------|-------|-------|
| $Q_C$         | $Q_B$ | $Q_A$ | $Q_C$      | $Q_B$ | $Q_A$ |
| 0             | 0     | 0     | 0          | 0     | 1     |
| 0             | 0     | 1     | 0          | 1     | 1     |
| 0             | 1     | 1     | 0          | 1     | 0     |
| 0             | 1     | 0     | 1          | 1     | 0     |
| 1             | 1     | 0     | 1          | 0     | 0     |
| 1             | 0     | 0     | 0          | 0     | 0     |



### Further Investigation Results:

The 74139 can be connected to form a 3-to-8 decoder as shown below:



### Evaluation and Review Questions:

Note: A variation for drawing Karnaugh maps was presented in the lab book in Figure 20-3 and repeated here for reference. The  $Q_B$  and  $Q_A$  variables are not written side-by-side; rather they are written nearly vertically. Some students find it easier to read the map to relate the number to the variable when they are drawn like this.

1.

| $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
|-------|-------|-------|-------|
| 0     | 0     | 0     | 0     |
| 1     | X     | X     | X     |
| 0     | 1     | X     | X     |
| 1     | 0     | X     | X     |
| 1     | 1     | X     | X     |
| 0     | 0     | X     | X     |

$$J_B = Q_A \bar{Q}_D$$

| $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
|-------|-------|-------|-------|
| 0     | 0     | 0     | 0     |
| 1     | X     | X     | X     |
| 0     | 1     | X     | X     |
| 1     | 0     | X     | X     |
| 1     | 1     | X     | X     |
| 0     | 0     | X     | X     |

$$K_B = Q_C$$

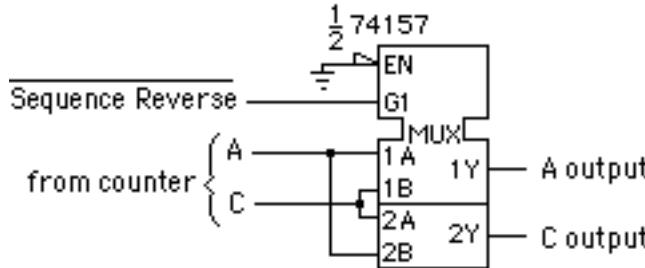
| $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
|-------|-------|-------|-------|
| 0     | 0     | 0     | 0     |
| 1     | X     | X     | X     |
| 0     | 1     | X     | X     |
| 1     | 0     | X     | X     |
| 1     | 1     | X     | X     |
| 0     | 0     | X     | X     |

$$J_A = \bar{Q}_B \bar{Q}_C$$

| $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
|-------|-------|-------|-------|
| 0     | 0     | 0     | 0     |
| 1     | X     | X     | X     |
| 0     | 1     | X     | X     |
| 1     | 0     | X     | X     |
| 1     | 1     | X     | X     |
| 0     | 0     | X     | X     |

$$K_A = Q_B$$

2. Since the largest binary number in the circuit for the experiment is less than ten, a BCD to seven-segment decoder (such as the 7447A) can be used to convert the binary number into a value that can be shown in a seven-segment display.
3. The reset button is connected between ground and the preset input of FFC and FFB; it is also connected between ground and the clear input of FFA.
4. The count sequence can be reversed by reversing the  $A$  and  $C$  bits from the counter. This can be accomplished by a 2-input MUX, such as the 74157, as shown below:



5. When the counter goes from state 3 to state 2, the  $A$  output is seen to do a 1 to 0 transition. Likewise, when the counter goes from state 6 to state 4, the  $B$  output does a 1 to 0 transition. These transitions are unique, therefore trigger by connecting the  $A$  and  $B$  outputs to the  $A_1$  and  $A_2$  trigger inputs of the 74121 ( $B$  trigger is HIGH). (See the function table for the 74121, given in Figure 17-1).
6. a. The  $D$  transition table is shown. The  $Q_{n+1}$  output follows  $D$  at the clock edge.

| $Q_n$ | $Q_{n+1}$ | $D$ |
|-------|-----------|-----|
| 0 → 0 | 0         | 0   |
| 0 → 1 | 1         |     |
| 1 → 0 | 0         |     |
| 1 → 1 | 1         |     |

- b. The  $J-K$  flip-flop is more versatile because it has the latch and toggle states. For this reason, there are  $X$ 's on the transition table which aid in designing a simpler circuit for irregular count sequences.

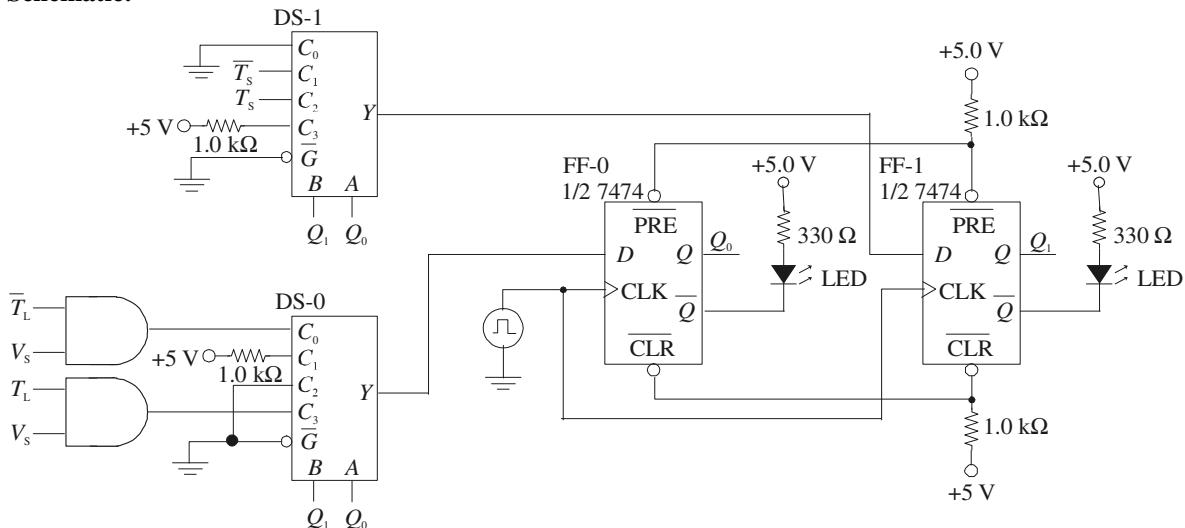
## Experiment 24: The Traffic Light Controller

Note - Table 24-1 lists present states in the gray-code sequence selected for the controller (0-1-3-2) rather than binary sequence.

**Table 24-1**

| Present State |       | Next State |       | Input Conditions                                          | Input Product Term for Data Selector-1 | Input Product Term for Data Selector-0 |
|---------------|-------|------------|-------|-----------------------------------------------------------|----------------------------------------|----------------------------------------|
| $Q_1$         | $Q_0$ | $Q_1$      | $Q_0$ |                                                           |                                        |                                        |
| 0             | 0     | 0          | 0     | $\overline{T_L} + \overline{V_S}$<br>$\overline{T_L} V_S$ | 0                                      | $\overline{T_L} V_S$                   |
| 0             | 0     | 0          | 1     |                                                           |                                        |                                        |
| 0             | 1     | 0          | 1     | $T_S$<br>$\overline{T_S}$                                 | $\overline{T_S}$                       | 1                                      |
| 0             | 1     | 1          | 1     |                                                           |                                        |                                        |
| 1             | 1     | 1          | 1     | $T_L V_S$<br>$\overline{T_L} + \overline{V_S}$            | 1                                      | $T_L V_S$                              |
| 1             | 1     | 1          | 0     |                                                           |                                        |                                        |
| 1             | 0     | 1          | 0     | $T_S$<br>$\overline{T_S}$                                 | $T_S$                                  | 0                                      |
| 1             | 0     | 0          | 0     |                                                           |                                        |                                        |

**Schematic:**



**Figure 24-4**

### Further Investigation Results (TTL)

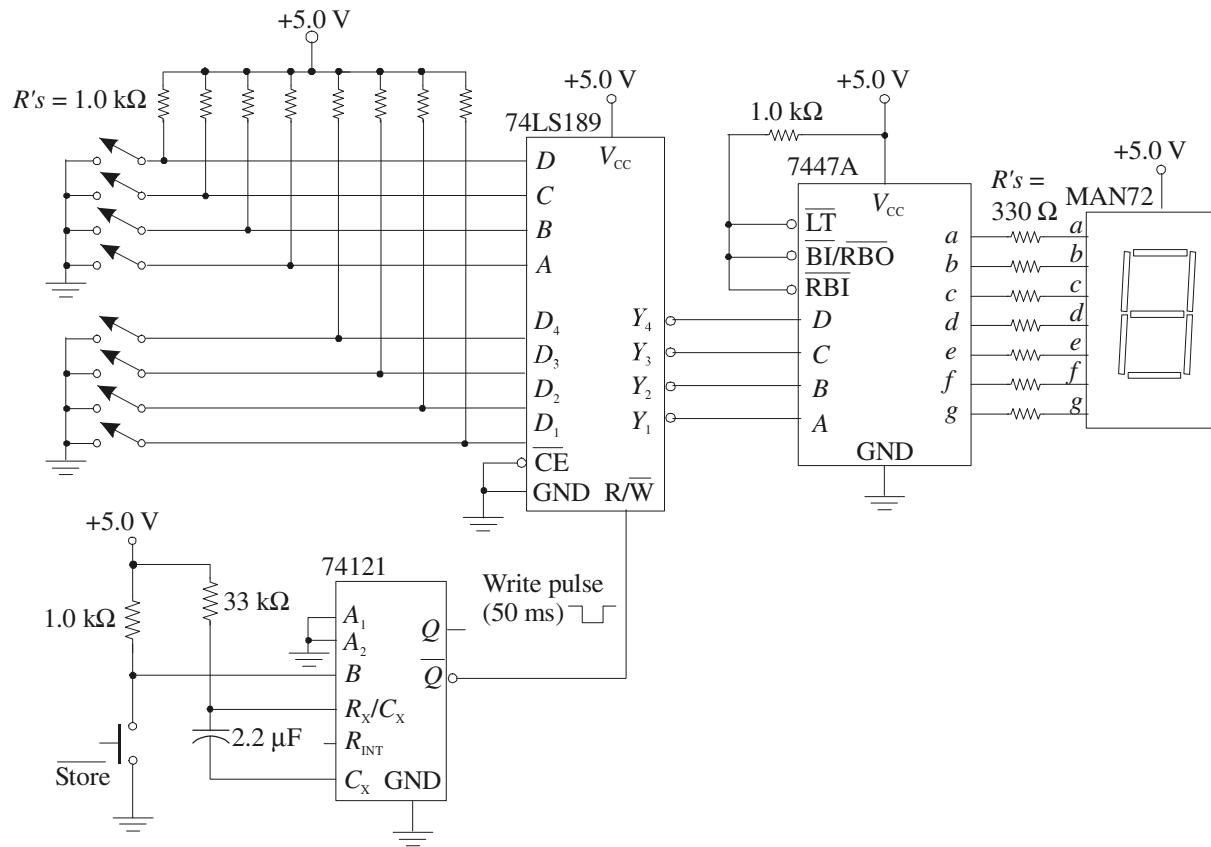
The first idea is sound; the short timer can be eliminated if states change in no less than 4 s. The equations would need to be changed to implement this. The second idea will not allow the state machine to function as designed.

### Evaluation and Review Questions:

- Gray code is selected to avoid false states due to decoding glitches.
- The long timer ( $T_L$ ) and the vehicle sensor ( $V_S$ ) must both be HIGH.
- A third flip-flop is needed for the counter and the MUXs would be changed to 3-to-8 lines.
- Connect the  $Y$  output from the MUXs to  $J$ ; this line is inverted and connected to  $K$ .
- Refer to the 7th line down on Table 19-1. In order to have both  $A$  inputs trigger on a trailing edge,  $B$  must be HIGH.
- The next state will sequence only if the long timer ( $T_L$ ) is LOW and the vehicle sensor ( $V_S$ ) is HIGH. Because the long timer is okay, test  $V_S$ . If it is okay, check the counter for clock pulses and correct inputs on  $D$ . If okay, check asynchronous inputs, power, and grounds.

## Experiment 25: Semiconductor Memories

The schematic for the addition to the security entry system is shown. The combination is entered as the *complements* of the BCD numbers (95614) stored in locations 0000 through 0100. Location 0101 should have 0000 stored to blank the 7-segment display after the last number.



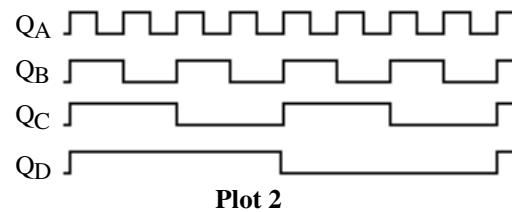
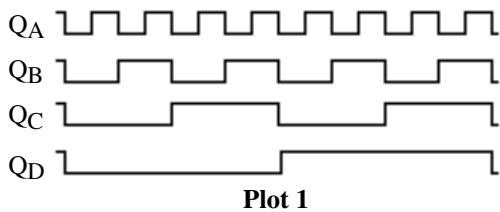
### Further Investigation Results:

The 7493A is set up to count from 0 through 5 by connecting the  $Q_B$  and  $Q_C$  outputs to the reset inputs and  $Q_A$  output to the CLK  $B$  input.

### Evaluation and Review Questions:

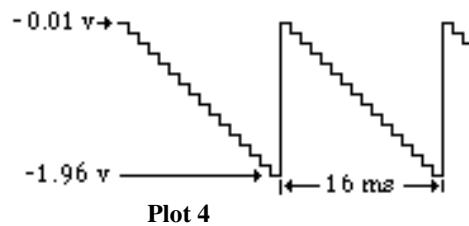
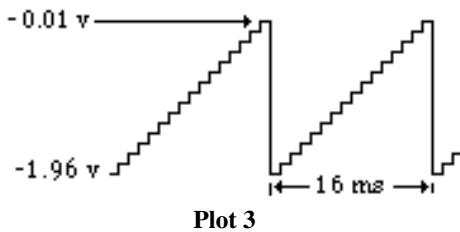
- For this experiment, address and data switches are set manually, and do not change. Therefore, it is not necessary to debounce the start push-button. It is included in the system because this is a simulation of a portion of a larger system.
- The number to be stored is 0000. The output is the complement of the stored number.
- a. Locations are addressed by binary numbers. On chip decoding means that the binary addresses are converted internally to the specific row information needed.  
b. Setup time is 25 ns, hold time is 0 ns. The data must be available 25 ns before the write pulse goes HIGH.
- 256 locations
- a. The word length needs to be expanded to 7 bits by adding a memory as in Figure 27-2b.  
b. Locations would store the encoded combination for the seven segment display.
- When  $R/\bar{W}$  is LOW, the outputs are in the high impedance state (see spec sheet).

## Experiment 26: D/A and A/D Conversion

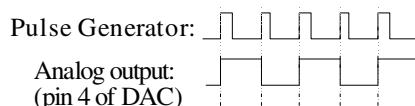


**Table 26-1**

| Quantity                      | Measured Value |
|-------------------------------|----------------|
| DAC full-scale output voltage | -1.96 V        |
| Volts/step                    | 0.13 V/step    |



Steps 7 and 8: The digital light meter has an oscillating behavior because of the tracking A/D converter. The D/A output waveform is shown below. The D/A output waveform increases its dc level from a minimum of approx -2 volts to approximately -0.2 volts as the light level increases.



### Further Investigation Results

Measured data for the circuit in Figure 26-1 is shown. The voltages listed are at the thresholds. Data are linear.

| Voltage | Display | Voltage | Display | Voltage | Display |
|---------|---------|---------|---------|---------|---------|
| Voltage | Display | Voltage | Display | Voltage | Display |
| 0.009 V | 0       | 1.35 V  | 4       | 2.59 V  | 8       |
| 0.437 V | 1       | 1.63 V  | 5       | 2.91 V  | 9       |
| 0.675 V | 2       | 1.93 V  | 6       | 3.23 V  | █       |
| 1.009 V | 3       | 2.26 V  | 7       | 3.53 V  | █       |
|         |         |         |         | 3.83 V  | █       |
|         |         |         |         | 4.17 V  | █       |
|         |         |         |         | 4.49 V  | █       |
|         |         |         |         | 4.85 V  | blank   |

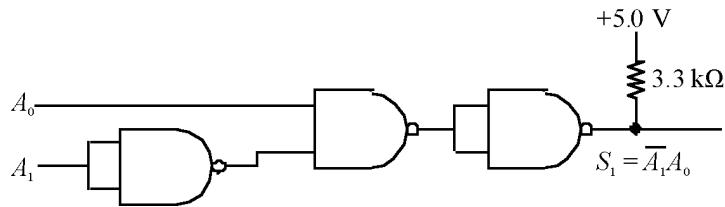
### Evaluation and Review Questions:

1. a. Binary 1010 is represented by -1.30 V. b. The output frequency is 62.5 Hz.
2.  $(-1.95 \text{ V})/255 \text{ steps} = -7.65 \text{ mV/step}$
3. a. The output voltage is larger because the reference current is larger.  
b. The resolution measured in volts/step increases. (Note that if measured simply by number of bits, the resolution is unchanged.)
4. The oscillation is caused by the quantizing error between the analog voltage from the photocell and the digitized representation from the converter. If the least significant bit is not used, the oscillation can be eliminated.
5. a. Decrease the reference current by increasing the  $5.1 \text{ k}\Omega$  resistor or decrease the  $2.0 \text{ k}\Omega$  load resistor.  
b. No. The change only effects the digital display, not the basic sensitivity of the photocell.
6. A higher clock frequency causes the meter to respond faster to changes but has the disadvantage of causing the display to change rapidly, making it more difficult to read.

## Experiment 27: Applications of Bus Systems

Observations from step 3: With all switches on the 14532B open, the chip outputs are all LOW, including the GS output as shown on the second line of the 14532B truth table. The transistors act as inverters, causing the corresponding inputs on the 14051B to be HIGH. If the inhibit line is tied LOW on the 14051B, the internal FET switch is closed that connects X7 to the common out/in line. This completes the path from the 555 timer to the LED representing the least significant bit, causing it to blink.

Decoder schematic: The decoder schematic depends on the particular address assigned to each student. As an example, a 7400 NAND gate, shown decoding address 01, is drawn below:



### Further Investigation Results:

Answers may vary. A 4-bit counter such as the 7493A may be selected or the student may design a two-bit counter with *J-K* or *D* flip-flops (such as the ripple counter drawn in Figure 18-2). The counter output is connected to a 7447A BCD to seven segment decoder similar to Figure 3-2.

### Evaluation and Review Questions:

1. a. The transistors are used to provide an open-collector connection to the data bus.  
b. The display is an input device. The bus can have multiple input devices connected to it without bus contention problems.
2. Each priority encoder is located at a unique address as determined by the individual decoders.
3. The 14051B can be connected as a MUX by connecting inputs to the X lines and taking the output from the common *out/in* line. The select inputs behave the same for both configurations.
4.  $R_{16}$  is a current limiting resistor for the LEDs. If it opens, no LED will be on.
5. a. The constant HIGH is connected to the selected output, causing the selected LED to stay on.  
b. All LEDs will be off.
6. a. The line will be LOW.  
b. A data line can be pulled LOW by any transistor connected to the line that is conducting because it provides a direct path to ground.  
c. Check the address bus to determine which indicator is being addressed.

## PART 3

# *Multisim Problem Solutions*

Name \_\_\_\_\_  
Date \_\_\_\_\_

Course \_\_\_\_\_  
Instructor \_\_\_\_\_

### **PROBLEM CIRCUITS FOR CHAPTER 3**

*Digital Fundamentals* by Tom Floyd, 11th Edition

| Circuit File | Circuit Fault                                        | Predicted Effect of Fault                 | Observed Effect of Introduced Fault | Fault Verified |
|--------------|------------------------------------------------------|-------------------------------------------|-------------------------------------|----------------|
| P03-52       | Input B of AND gate U <sub>1</sub> shorted to ground | Output X is always LOW.                   | Output X is always LOW.             | ✓              |
| P03-53       | Input B of NAND gate shorted to V <sub>CC</sub>      | Output X is LOW whenever input A is HIGH. | Output X is LOW whenever A is HIGH. | ✓              |

| Circuit File | Observed Operation                           | Suspected Fault                                  | Effect of Introduced Fault             | Fault Verified |
|--------------|----------------------------------------------|--------------------------------------------------|----------------------------------------|----------------|
| P03-54       | Output is X is LOW whenever input B is HIGH. | Input A of NOR gate shorted to ground.           | Output is X is LOW whenever B is HIGH. | ✓              |
| P03-55       | Output X is the inverse of input A.          | Input B of XOR gate shorted to V <sub>CC</sub> . | Output X is the inverse of input A.    | ✓              |

Name \_\_\_\_\_  
Date \_\_\_\_\_

Course \_\_\_\_\_  
Instructor \_\_\_\_\_

## **PROBLEM CIRCUITS FOR CHAPTER 4**

*Digital Fundamentals*, 11th Edition by Tom Floyd

| Circuit File | Circuit Fault                           | Predicted Effect of Fault                                                                                                                                                                                                         | Observed Effect of Introduced Fault                                                                                                                                                                                           | Fault Verified |
|--------------|-----------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| P04-70       | Input C is shorted to ground.           | X <sub>1</sub> and X <sub>2</sub> are always off. X <sub>3</sub> is on only when both B and C are HIGH. X <sub>4</sub> is on when either B or C is LOW.                                                                           | X <sub>1</sub> and X <sub>2</sub> are always off. X <sub>3</sub> is on only when B and C are both HIGH (switches B and C are both open).                                                                                      | ✓              |
| P04-71       | Bottom input of U <sub>7</sub> is open. | X <sub>1</sub> and X <sub>4</sub> are on when A is LOW and B and C both are HIGH. X <sub>2</sub> and X <sub>4</sub> are on when B is LOW and A and C both are HIGH. X <sub>3</sub> is on when C is LOW and both A and B are HIGH. | X <sub>1</sub> and X <sub>4</sub> on when A is LOW and B and C both are HIGH. X <sub>2</sub> and X <sub>4</sub> are on when B is LOW and A and C both are HIGH. X <sub>3</sub> is on when C is LOW and both A and B are HIGH. | ✓              |

| Circuit File | Observed Operation                                                                                                                                                                                                                         | Suspected Fault                                | Effect of Introduced Fault                                                                                                                                                                                                                 | Fault Verified |
|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| P04-72       | X <sub>1</sub> is on when either A or B is LOW. X <sub>2</sub> is always off. X <sub>3</sub> is on when both A and B are HIGH or when C is LOW. X <sub>4</sub> is always ON. X <sub>5</sub> is on when C is HIGH and either A or B is LOW. | Output of U <sub>3</sub> is shorted to ground. | X <sub>1</sub> is on when either A or B is LOW. X <sub>2</sub> is always off. X <sub>3</sub> is on when both A and B are HIGH or when C is LOW. X <sub>4</sub> is always ON. X <sub>5</sub> is on when C is HIGH and either A or B is LOW. | ✓              |

Name \_\_\_\_\_  
Date \_\_\_\_\_

Course \_\_\_\_\_  
Instructor \_\_\_\_\_

## **PROBLEM CIRCUITS FOR CHAPTER 5**

*Digital Fundamentals, 11th Edition by Tom Floyd*

| Circuit File | Circuit Fault                    | Predicted Effect of Fault                                            | Observed Effect of Introduced Fault                                  | Fault Verified |
|--------------|----------------------------------|----------------------------------------------------------------------|----------------------------------------------------------------------|----------------|
| P05-61       | Output of U3A shorted to ground. | The Finlet and Lmin switches have no effect on the Vinlet indicator. | The Finlet and Lmin switches have no effect on the Vinlet indicator. | ✓              |
| P05-62       | Output of U3C is shorted to VCC. | The Finlet switch has no effect on the Vinlet indicator.             | The Finlet switch has no effect on the Vinlet indicator.             | ✓              |

| Circuit File | Observed Operation                           | Suspected Fault                                    | Effect of Introduced Fault                   | Fault Verified |
|--------------|----------------------------------------------|----------------------------------------------------|----------------------------------------------|----------------|
| P05-63       | The Vinlet indicator is always ON.           | The output of U2A is always HIGH (shorted to VCC). | The Vinlet indicator is always ON.           | ✓              |
| P05-64       | The Voutlet and T indicators are always OFF. | Switch D is shorted to ground.                     | The Voutlet and T indicators are always OFF. | ✓              |

Name \_\_\_\_\_  
Date \_\_\_\_\_

Course \_\_\_\_\_  
Instructor \_\_\_\_\_

## **PROBLEM CIRCUITS FOR CHAPTER 6**

*Digital Fundamentals, 11<sup>th</sup> Edition by Tom Floyd*

| Circuit File | Circuit Fault                       | Predicted Effect of Fault                                                                         | Observed Effect of Introduced Fault                                                               | Fault Verified |
|--------------|-------------------------------------|---------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------|----------------|
| P06-53       | $C_{IN}$ of U1 is shorted to VCC.   | Output is always 1 greater than it should be.                                                     | Output is always 1 greater than it should be.                                                     | ✓              |
| P06-54       | Output of U1A is shorted to ground. | Output is unaffected by states of A0 and B0 so that comparator output is TRUE anytime $A1 = B1$ . | Output is unaffected by states of A0 and B0 so that comparator output is TRUE anytime $A1 = B1$ . | ✓              |

Name \_\_\_\_\_  
 Date \_\_\_\_\_

Course \_\_\_\_\_  
 Instructor \_\_\_\_\_

| Circuit File | Observed Operation                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Suspected Fault                                                      | Effect of Introduced Fault                                | Fault Verified |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------|-----------------------------------------------------------|----------------|----|---------|----|---------|----|---------|----|---------|----|---------|----|---------|----|---------|----|---------|----|---------|----|---------|-----|---------|-----|---------|----|---------|----|---------|-----|---------|-----|--------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|--------|---------|----|---------|----|---------|----|---------|----|---------|----|---------|----|---------|----|---------|----|---------|----|---------|----|---------|-----|---------|-----|---------|----|---------|----|---------|-----|---------|-----|---|
| P06-55       | <p>Inputs are encoded as follows:</p> <table> <thead> <tr> <th>S1 S2 S3 S4</th> <th>Output</th> </tr> </thead> <tbody> <tr><td>0 0 0 0</td><td>D0</td></tr> <tr><td>1 0 0 0</td><td>D1</td></tr> <tr><td>0 1 0 0</td><td>D2</td></tr> <tr><td>1 1 0 0</td><td>D3</td></tr> <tr><td>0 0 1 0</td><td>D0</td></tr> <tr><td>1 0 1 0</td><td>D1</td></tr> <tr><td>0 1 1 0</td><td>D2</td></tr> <tr><td>1 1 1 0</td><td>D3</td></tr> <tr><td>0 0 0 1</td><td>D8</td></tr> <tr><td>1 0 0 1</td><td>D9</td></tr> <tr><td>0 1 0 1</td><td>D10</td></tr> <tr><td>1 1 0 1</td><td>D11</td></tr> <tr><td>0 0 1 1</td><td>D8</td></tr> <tr><td>1 0 1 1</td><td>D9</td></tr> <tr><td>0 1 1 1</td><td>D10</td></tr> <tr><td>1 1 1 1</td><td>D11</td></tr> </tbody> </table> | S1 S2 S3 S4                                                          | Output                                                    | 0 0 0 0        | D0 | 1 0 0 0 | D1 | 0 1 0 0 | D2 | 1 1 0 0 | D3 | 0 0 1 0 | D0 | 1 0 1 0 | D1 | 0 1 1 0 | D2 | 1 1 1 0 | D3 | 0 0 0 1 | D8 | 1 0 0 1 | D9 | 0 1 0 1 | D10 | 1 1 0 1 | D11 | 0 0 1 1 | D8 | 1 0 1 1 | D9 | 0 1 1 1 | D10 | 1 1 1 1 | D11 | <p>Input C of 4-to-16 line decoder is shorted to ground.</p> | <p>Inputs are encoded as follows:</p> <table> <thead> <tr> <th>S1 S2 S3 S4</th> <th>Output</th> </tr> </thead> <tbody> <tr><td>0 0 0 0</td><td>D0</td></tr> <tr><td>1 0 0 0</td><td>D1</td></tr> <tr><td>0 1 0 0</td><td>D2</td></tr> <tr><td>1 1 0 0</td><td>D3</td></tr> <tr><td>0 0 1 0</td><td>D0</td></tr> <tr><td>1 0 1 0</td><td>D1</td></tr> <tr><td>0 1 1 0</td><td>D2</td></tr> <tr><td>1 1 1 0</td><td>D3</td></tr> <tr><td>0 0 0 1</td><td>D8</td></tr> <tr><td>1 0 0 1</td><td>D9</td></tr> <tr><td>0 1 0 1</td><td>D10</td></tr> <tr><td>1 1 0 1</td><td>D11</td></tr> <tr><td>0 0 1 1</td><td>D8</td></tr> <tr><td>1 0 1 1</td><td>D9</td></tr> <tr><td>0 1 1 1</td><td>D10</td></tr> <tr><td>1 1 1 1</td><td>D11</td></tr> </tbody> </table> | S1 S2 S3 S4 | Output | 0 0 0 0 | D0 | 1 0 0 0 | D1 | 0 1 0 0 | D2 | 1 1 0 0 | D3 | 0 0 1 0 | D0 | 1 0 1 0 | D1 | 0 1 1 0 | D2 | 1 1 1 0 | D3 | 0 0 0 1 | D8 | 1 0 0 1 | D9 | 0 1 0 1 | D10 | 1 1 0 1 | D11 | 0 0 1 1 | D8 | 1 0 1 1 | D9 | 0 1 1 1 | D10 | 1 1 1 1 | D11 | ✓ |
| S1 S2 S3 S4  | Output                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 0 0 0 0      | D0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 1 0 0 0      | D1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 0 1 0 0      | D2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 1 1 0 0      | D3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 0 0 1 0      | D0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 1 0 1 0      | D1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 0 1 1 0      | D2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 1 1 1 0      | D3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 0 0 0 1      | D8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 1 0 0 1      | D9                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 0 1 0 1      | D10                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 1 1 0 1      | D11                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 0 0 1 1      | D8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 1 0 1 1      | D9                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 0 1 1 1      | D10                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 1 1 1 1      | D11                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| S1 S2 S3 S4  | Output                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 0 0 0 0      | D0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 1 0 0 0      | D1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 0 1 0 0      | D2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 1 1 0 0      | D3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 0 0 1 0      | D0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 1 0 1 0      | D1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 0 1 1 0      | D2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 1 1 1 0      | D3                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 0 0 0 1      | D8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 1 0 0 1      | D9                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 0 1 0 1      | D10                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 1 1 0 1      | D11                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 0 0 1 1      | D8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 1 0 1 1      | D9                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 0 1 1 1      | D10                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| 1 1 1 1      | D11                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |                                                                      |                                                           |                |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |
| P06-56       | <p>Output Y is always HIGH when input D1 is selected.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | <p>Switch contact connected to D1 input of G4 is shorted to VCC.</p> | <p>Output Y is always HIGH when input D1 is selected.</p> | ✓              |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |             |        |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |    |         |     |         |     |         |    |         |    |         |     |         |     |   |

Name \_\_\_\_\_  
Date \_\_\_\_\_

Course \_\_\_\_\_  
Instructor \_\_\_\_\_

## **PROBLEM CIRCUITS FOR CHAPTER 7**

*Digital Fundamentals*, 11th Edition by Tom Floyd

| Circuit File | Circuit Fault                                             | Predicted Effect of Fault                                                                                                                           | Observed Effect of Introduced Fault                                                                                                                 | Fault Verified |
|--------------|-----------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| P07-47       | R input of U <sub>1</sub> is shorted to V <sub>CC</sub> . | The flip-flop will be reset and unable to set.                                                                                                      | The flip-flop will be reset and unable to set.                                                                                                      | ✓              |
| P07-48       | Line to K input is shorted to V <sub>CC</sub> .           | If line to J input is LOW, Q output will go and remain LOW and Q' output will go and remain HIGH. If line to J input is HIGH, Q and Q' will toggle. | If line to J input is LOW, Q output will go and remain LOW and Q' output will go and remain HIGH. If line to J input is HIGH, Q and Q' will toggle. | ✓              |

| Circuit File | Observed Operation                                                                                          | Suspected Fault                                                                                                                         | Effect of Introduced Fault                                                                                    | Fault Verified |
|--------------|-------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------|----------------|
| P07-49       | The SET' and RESET' inputs affect the Q and Q' outputs, but the D input DO not affect the Q and Q' outputs. | Clock input is shorted to V <sub>CC</sub> (or ground).                                                                                  | The SET' and RESET' inputs affect the Q and Q' outputs, but the D input will not affect the Q and Q' outputs. | ✓              |
| P07-50       | Pulse width of one shot is 690 µs rather than 6.9 ms.                                                       | 1 kΩ resistor accidentally used in place of 10 kΩ timing resistor, or a 0.1 µF capacitor is used in place of the 1 µF timing capacitor. | Pulse width of one shot is 690 µs rather than 6.9 ms.                                                         | ✓              |

Name \_\_\_\_\_  
Date \_\_\_\_\_

Course \_\_\_\_\_  
Instructor \_\_\_\_\_

| Circuit File | Observed Operation                                                                                 | Suspected Fault                                 | Effect of Introduced Fault                                                                         | Fault Verified |
|--------------|----------------------------------------------------------------------------------------------------|-------------------------------------------------|----------------------------------------------------------------------------------------------------|----------------|
| P07-51       | The Q output of U <sub>1</sub> toggles as expected but the Q output of U <sub>2</sub> remains LOW. | D input of U <sub>2</sub> is shorted to ground. | The Q output of U <sub>1</sub> toggles as expected but the Q output of U <sub>2</sub> remains LOW. | ✓              |

Name \_\_\_\_\_  
Date \_\_\_\_\_

Course \_\_\_\_\_  
Instructor \_\_\_\_\_

## **PROBLEM CIRCUITS FOR CHAPTER 8**

*Digital Fundamentals*, 11th Edition by Tom Floyd

| Circuit File | Circuit Fault                                                           | Predicted Effect of Fault                                                                                                                                              | Observed Effect of Introduced Fault                                                                                                                                | Fault Verified |
|--------------|-------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| P08-47       | The D input of FF1 is shorted to ground.                                | The last two bits shifted out of SDO will always be 0.                                                                                                                 | The last two bits shifted out of SDO are always 0.                                                                                                                 | ✓              |
| P08-48       | The input of the inverter U1 is shorted to ground.                      | The shift register will shift data from left to right ( $Q_3$ to $Q_0$ ) but not right to left ( $Q_0$ to $Q_3$ ).                                                     | The shift register shifts data from left to right ( $Q_3$ to $Q_0$ ) but not right to left ( $Q_0$ to $Q_3$ ).                                                     | ✓              |
| P08-49       | The U3 Q' output of the Johnson counter is connected to the U2 D input. | Initializing the counter with S2 will set output $Q_0$ HIGH, but clocking the counter will cause only outputs $Q_1$ through $Q_3$ to function as in a Johnson counter. | Initializing the counter with S2 sets output $Q_0$ HIGH, but clocking the counter will cause only outputs $Q_1$ through $Q_3$ to function as in a Johnson counter. | ✓              |

| Circuit File | Observed Operation                                                                                                                                  | Suspected Fault                                                                                                                                              | Effect of Introduced Fault                                                                                                                          | Fault Verified |
|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| P08-50       | The 74195 shift register only can shift in 1s (for $J=1$ and $\sim K=0$ or 1) or remain unchanged (for $J=1$ and $\sim K = 0$ or 1) in serial mode. | The $\sim K$ input of the 74195 shift register is always HIGH (shorted to $V_{CC}$ ), so that the input cannot toggle the serial data or leave it unchanged. | The 74195 shift register only can shift in 1s (for $J=1$ and $\sim K=0$ or 1) or remain unchanged (for $J=1$ and $\sim K = 0$ or 1) in serial mode. | ✓              |

Name \_\_\_\_\_  
Date \_\_\_\_\_

Course \_\_\_\_\_  
Instructor \_\_\_\_\_

| Circuit File | Observed Operation                                                                             | Suspected Fault                                                      | Effect of Introduced Fault                                               | Fault Verified |
|--------------|------------------------------------------------------------------------------------------------|----------------------------------------------------------------------|--------------------------------------------------------------------------|----------------|
| P08-51       | Data from U1 shifts through to U3, but the output of U4 does not change (or is unpredictable). | The connection between the Q output of U3 and D input of U4 is open. | Data from U1 shifts through to U3, but the output of U4 does not change. | ✓              |

Name \_\_\_\_\_  
Date \_\_\_\_\_

Course \_\_\_\_\_  
Instructor \_\_\_\_\_

## **PROBLEM CIRCUITS FOR CHAPTER 9**

*Digital Fundamentals, 11th Edition by Tom Floyd*

| Circuit File | Circuit Fault                                                                                                         | Predicted Effect of Fault                                                                                                                        | Observed Effect of Introduced Fault                                                                                                              | Fault Verified |
|--------------|-----------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|----------------|
| P09-58       | The line to the CLK input of U <sub>3</sub> is open.                                                                  | Q <sub>0</sub> and Q <sub>1</sub> will sequence normally. Q <sub>2</sub> and Q <sub>3</sub> will remain LOW.                                     | Q <sub>0</sub> and Q <sub>1</sub> will sequence normally. Q <sub>2</sub> and Q <sub>3</sub> will remain LOW.                                     | ✓              |
| P09-59       | The input of the U <sub>5</sub> AND gate that connects to the Q output of U <sub>2</sub> shorted to V <sub>CC</sub> . | The Q <sub>2</sub> Q <sub>1</sub> Q <sub>0</sub> count sequence is to 000, 001, 110, 111, 000... rather than a 3-bit binary up count.            | The Q <sub>2</sub> Q <sub>1</sub> Q <sub>0</sub> count sequence is to 000, 001, 110, 111, 000... rather than a 3-bit binary up count.            | ✓              |
| P09-60       | Q output of U <sub>3</sub> is shorted to ground.                                                                      | The Q <sub>3</sub> Q <sub>2</sub> Q <sub>1</sub> Q <sub>0</sub> count sequence is 0000, 0001, 0010, 0011, 0000... rather than a decade up count. | The Q <sub>3</sub> Q <sub>2</sub> Q <sub>1</sub> Q <sub>0</sub> count sequence is 0000, 0001, 0010, 0011, 0000... rather than a decade up count. | ✓              |

| Circuit File | Observed Operation                                                                                        | Suspected Fault                 | Effect of Introduced Fault                                                                                | Fault Verified |
|--------------|-----------------------------------------------------------------------------------------------------------|---------------------------------|-----------------------------------------------------------------------------------------------------------|----------------|
| P09-61       | Outputs of 74HC163 counter always matches the values on its parallel inputs during synchronous operation. | Line to LOAD' input always LOW. | Outputs of 74LS163 counter always matches the values on its parallel inputs during synchronous operation. | ✓              |

Name \_\_\_\_\_  
Date \_\_\_\_\_

Course \_\_\_\_\_  
Instructor \_\_\_\_\_

| Circuit File | Observed Operation                                         | Suspected Fault                            | Effect of Introduced Fault                                 | Fault Verified |
|--------------|------------------------------------------------------------|--------------------------------------------|------------------------------------------------------------|----------------|
| P09-62       | 74HC190 decade counter always functions as a down counter. | Line to U'/D input of counter always HIGH. | 74LS190 decade counter always functions as a down counter. | ✓              |