Computer Logic and Digital Circuit Design (PHYS306/COSC330): Unit 3

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Summary

Reading: chapter 7

We now know how to generate and process digital data. We can do algebra, compare numbers, encode, decode, and multiplex. *How does memory work? How is information held in digital systems?*

1. S-R latches
   - Basic latch, de-bounce
   - Gated latch
   - D-latch
2. Flip-flops
   - JK flip-flops
   - Synchronous vs. level-sensitive
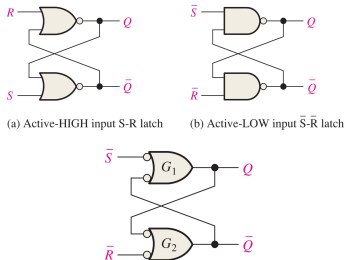
S-R Latches

S-R Latches

(a) Active-HIGH input S-R latch   (b) Active-LOW input $\bar{S}$-$\bar{R}$ latch

Truth table for an active-LOW input $\bar{S}$-$\bar{R}$ latch.

Inputs		Outputs		
$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$	Comments
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1	1	Invalid condition

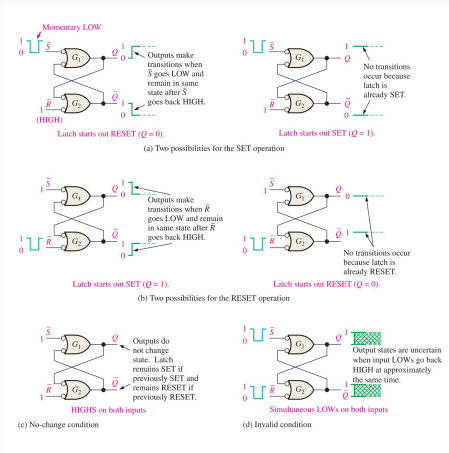**Figure 1:** An S-R latch is a *multivibrator* that holds its state when SET, or RESET.

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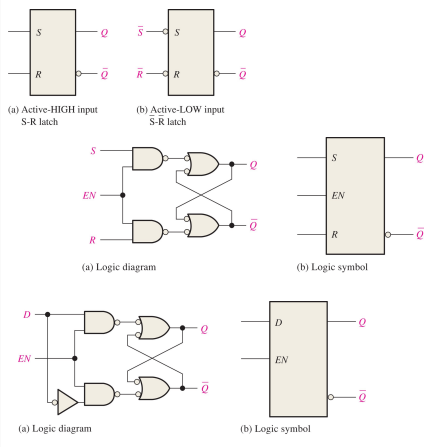**Figure 2:** Summary of potential states of a basic S-R latch.

S-R Latches

(a) Active-HIGH input S-R latch

(b) Active-LOW input S-R latch

(a) Logic diagram

(b) Logic symbol

(a) Logic diagram

(b) Logic symbol

Figure 3: The basic, gate-enabled, and D-latch systems. For the latter two, both the gate and symbol are shown.
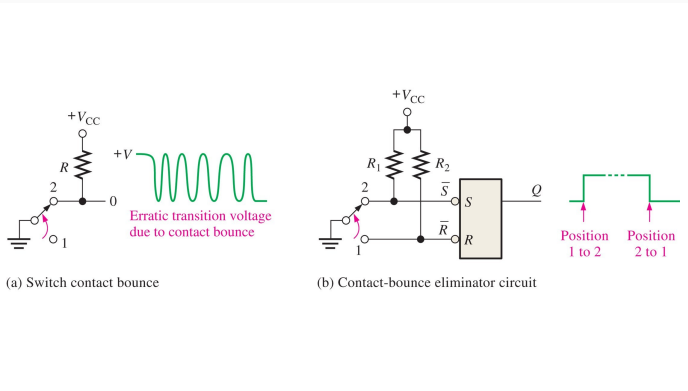
S-R Latches

(a) Switch contact bounce

(b) Contact-bounce eliminator circuit

Figure 4: De-bouncing is important any time a mechanical switch is meant to interact with digital logic.

Flip Flops

Flip-Flops

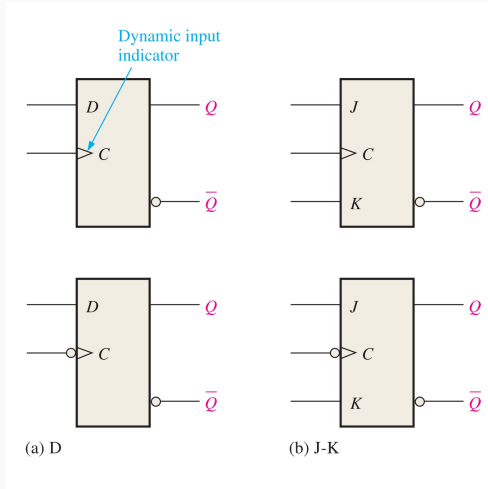**Figure 5:** Four types of **synchronous** latches called flip-flops.
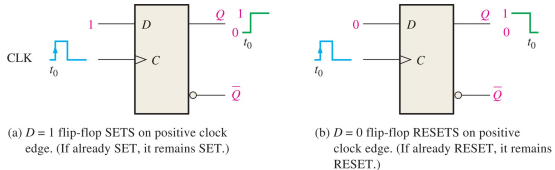
(a) $D = 1$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)

(b) $D = 0$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)

TABLE 7–2

Truth table for a positive edge-triggered D flip-flop.

Inputs		Outputs		
D	CLK	Q	$\bar{Q}$	Comments
0	↑	0	1	RESET
1	↑	1	0	SET

↑ = clock transition LOW to HIGH

Figure 6: The symbol and TT for the D-flip flop. The behavior is simular to a D-latch without enable, but only on positive edge of clock (posedge).
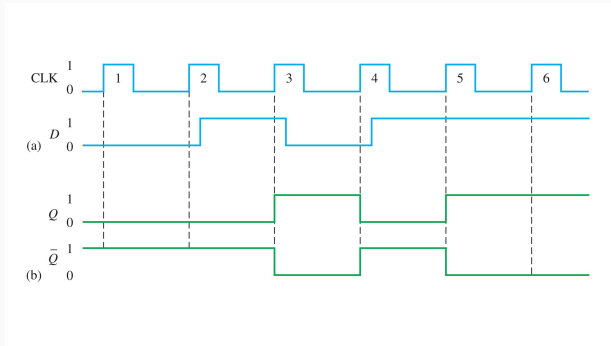
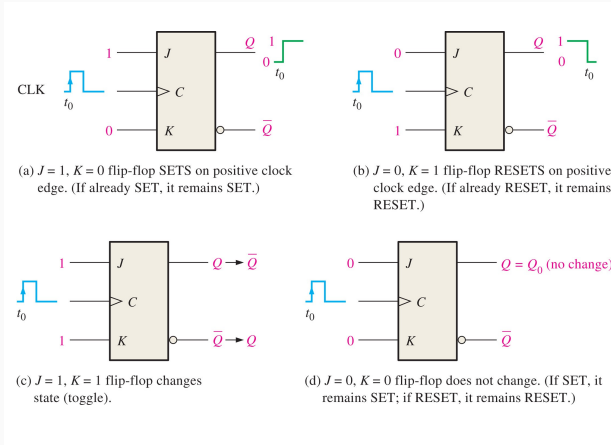# Flip-Flops

Figure 7: Example of D flip-flop behavior.

(a) $J = 1$, $K = 0$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)

(b) $J = 0$, $K = 1$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)

(c) $J = 1$, $K = 1$ flip-flop changes state (toggle).

(d) $J = 0$, $K = 0$ flip-flop does not change. (If SET, it remains SET; if RESET, it remains RESET.)

Figure 8: The JK flip flop, triggered on posedge. There are still the SET and RESET states, but the other two states differ from the SR latch.
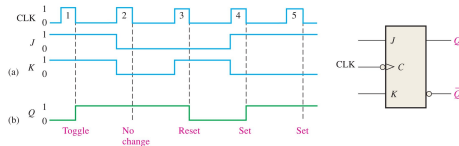
Figure 9: The TT for the JK flip flop, which is also **synchronous**. An example timing diagram is given for the JK as well.
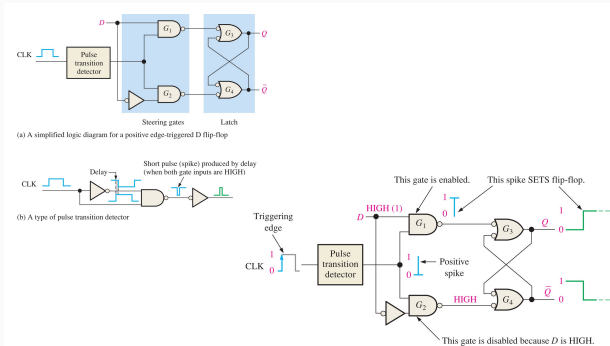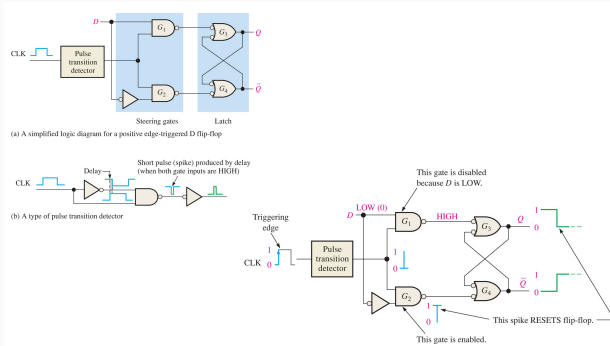
Figure 10: How does the posedge triggering work? Physically, it is based on *propagation delay*. The D flip-flop is pictured as an example, with spikes. *What counts as a spike?*

(a) A simplified logic diagram for a positive edge-triggered D flip-flop

(b) A type of pulse transition detector

Figure 11: How does the posedge triggering work? Physically, it is based on *propagation delay*. The D flip-flop is pictured as an example, with spikes. *What counts as a spike?*
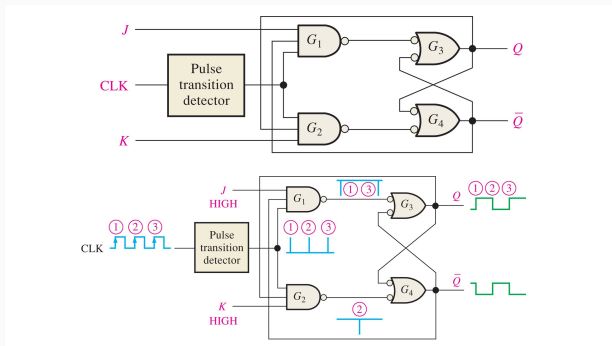
Figure 12: Circuit diagram with symbols for the JK flip flop, with posedge trigger. The JK flip-flop is in toggle mode.
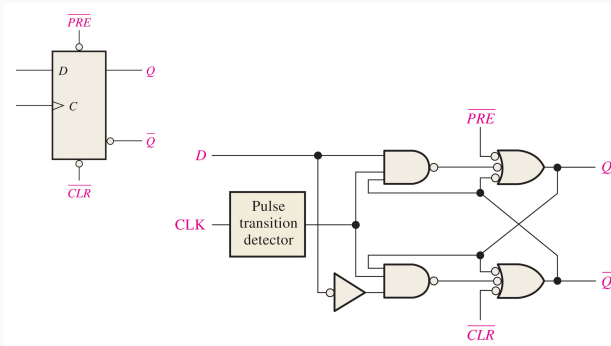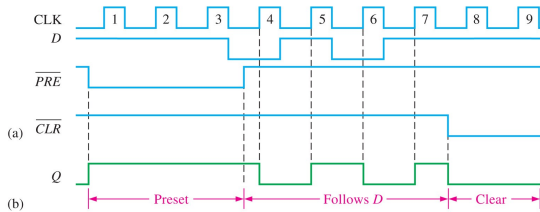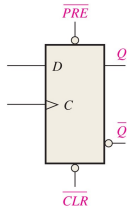
Flip-Flops

Figure 13: Addig two asynchronous features, preset and clear. These override the synchronous features due to the way they are used.

Flip-Flops

Conclusion

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