Physics 306 Midterm #2

1).

1 1 1   1 0 1   1 0 1   1 0

A B Cin   A B Cin   A B Cin   A B Cin

Cout Σ   Cout Σ   Cout Σ   Cout Σ

1   1   2   1

8ns   8ns   8ns   8ns

32ns is the worst case

$f = 1/T$ $f = 1/32 = .031 = 6Hz$

$f = 1/32ns$

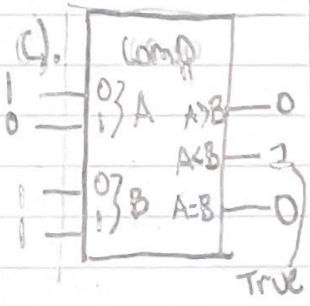$= .03125 GHz$

a).

b). $1/64ns = \boxed{.015625 GHz}$

c). ✳ Each clock pulse in wavedrom is 4ns. When each sum is taking place, the timing diagram shows "HIGH". The first carry in takes place after FA1 which can be seen in the wavedrom. I divided the clock period to be 4ns; disregard the first pulse.

2). K-map   AND $\begin{smallmatrix}A\\B\end{smallmatrix}\!\!\Rightarrow$ OR $\begin{smallmatrix}A\\B\end{smallmatrix}\!\!\Rightarrow$ XNOR $\begin{smallmatrix}A\\B\end{smallmatrix}\!\!\Rightarrow\!\!\circ$

A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

B
A \ 0 1

| 0 | 0 | 0 |
| 1 | 1 | 0 |

A̅B

B
A \ 0 1

| 0 | 0 | 1 |
| 1 | 0 | 0 |

A̅B

B
A \ 0 1

| 0 | 1 | 0 |
| 1 | 0 | 1 |

$\overline{A+B}$

A).
MSB
LSB

Comp   True

A>B ———— ⌐ 1
A<B ———— 0
A=B ———— 0

2 > 1 true ✓

B).

Comp

A>B — 0
A<B — 0
A=B — 1
↑
True

2=2 ✓
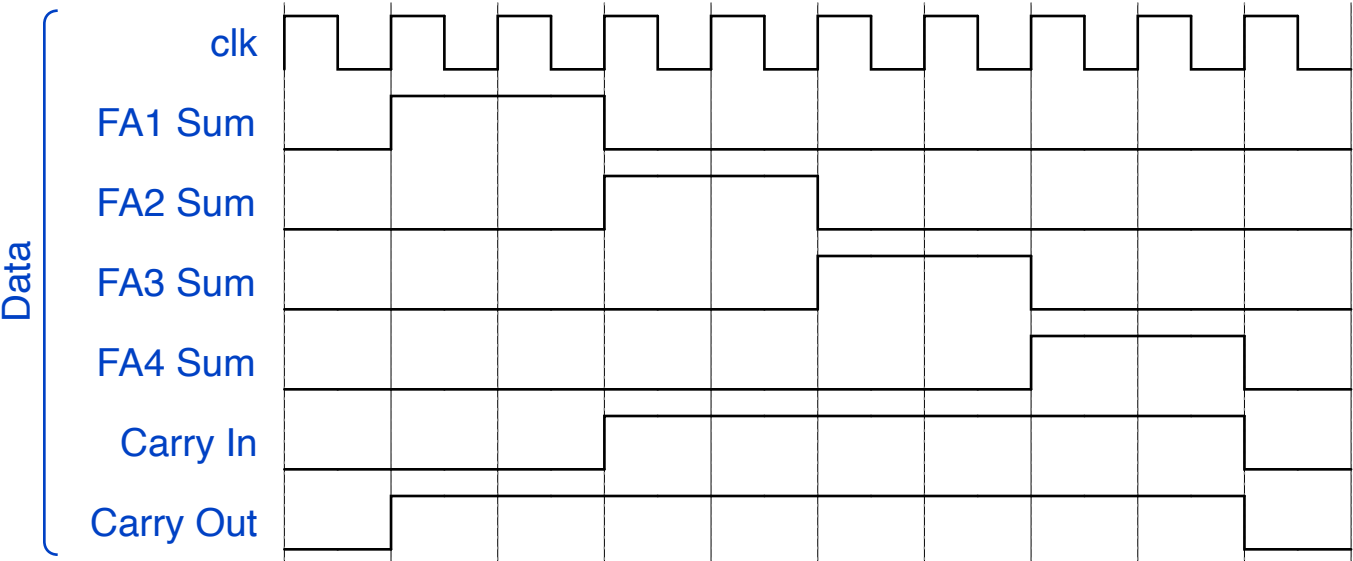
C).

Comp

A>B — 0
A<B — 1
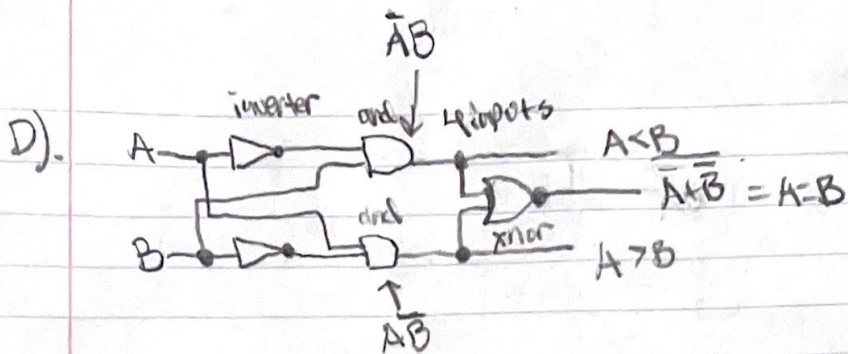A=B — 0
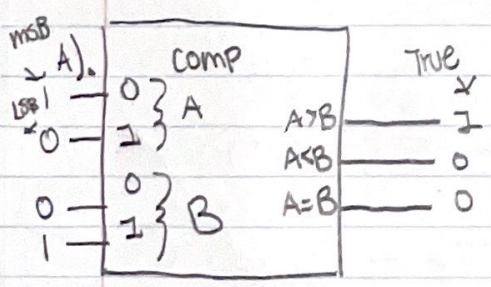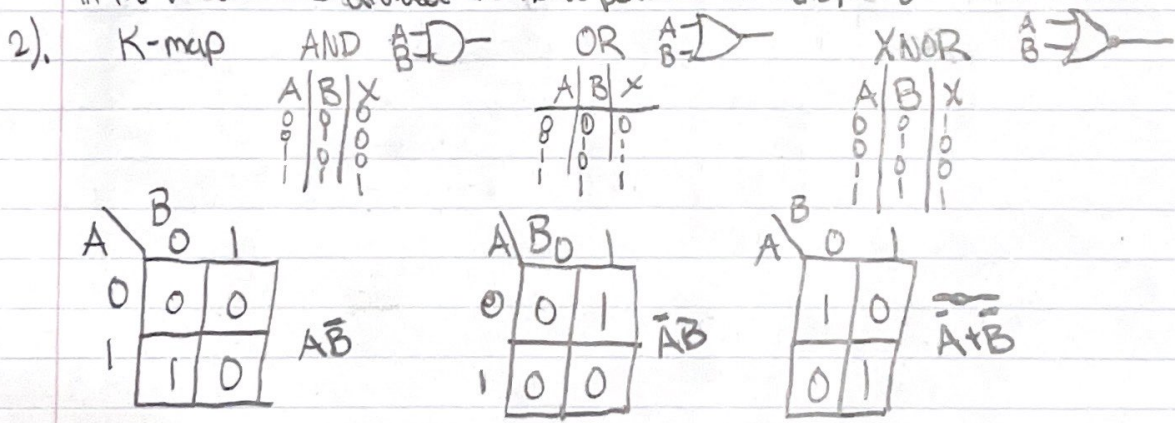
True
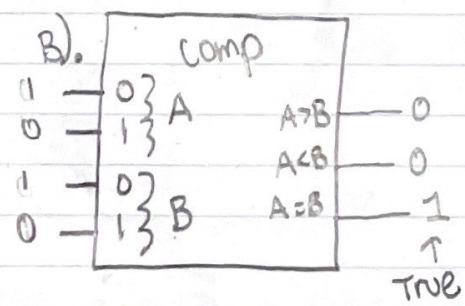
2<3 ✓

```
1  { "signal" : [
2    ["Data",
3      { name: "clk",      wave: "p........." },
4
5      { "name": "FA1 Sum", "wave": "lh.l......" },
6      { "name": "FA2 Sum", "wave": "l..h.l...." },
7      { "name": "FA3 Sum", "wave": "l....h.l.." },
8
9      { "name": "FA4 Sum", "wave": "l......h.l" },
10
11     { "name": "Carry In", "wave": "l..h.....l" },
12     { "name": "Carry Out", "wave": "lh.......l" },
13
14
15
16
17    ],
18    ,
19  ],
20    "config" : { "hscale" : 1 }
21  }
```
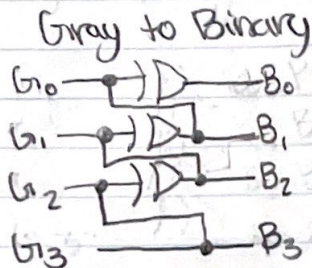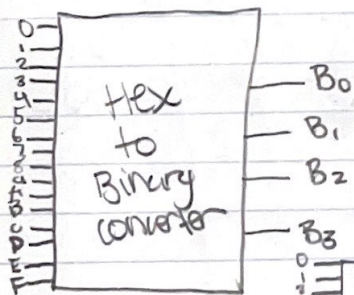
D).

$$\overline{AB}$$

A —— inverter —— and ↓ 4 inputs

A > B̄
$$\overline{A+\overline{B}} = A=B$$
A > B

xnor

↑
$$A\overline{B}$$

3).

Gray to Binary

G_0 —————— B_0
G_1 —————— B_1
G_2 —————— B_2
G_3 —————— B_3

*See waveform for timing diagram

4). A)

0 1 2 3 4 5 6 7 8 9 A B C D E F

A_0 (LSB)
A_1
A_2
A_3 (MSB)

Not the best drawing :(

b).

0
1
2
3
4
5
6
7
8
9
A
B
C
D
E
F

Hex to Binary converter

—— B_0
—— B_1
—— B_2
—— B_3

c). Didn't really understand this part. Hopefully I was on the right track!

Hex to Binary converter

Hex to Binary converter

32 data select lines

2 digit hex

2 digit hex

2:1 MUX

Binary output
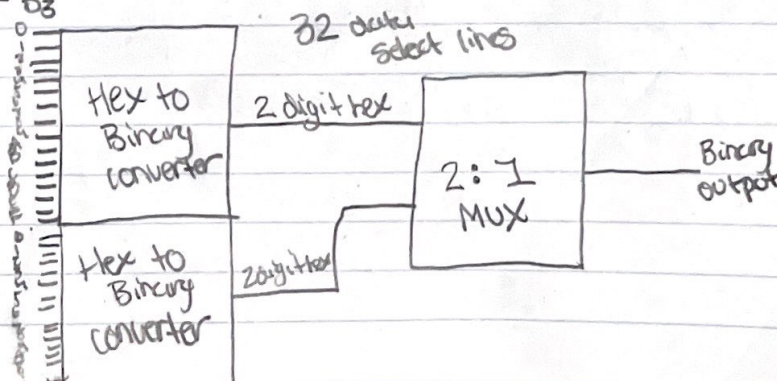
```
1  { "signal" : [
2    ["Data",
3      { name: "clk",      wave: "p..................." },
4
5      { "name": "G0", "wave": "lh.l.h.l.h.l.h.l" },
6      { "name": "G1", "wave": "l.h...l...h...l." },
7      { "name": "G2", "wave": "l...h.......l..." },
8      { "name": "G3", "wave": "l.......h......." },
9         { "name": "B0", "wave": "lhlhlhlhlhlhlhlh" },
10        { "name": "B1", "wave": "l.h.l.h.l.h.l.h." },
11        { "name": "B2", "wave": "l...h...l...h..." },
12        { "name": "B3", "wave": "l.......h......." },
13
14
15    ],
16    ,
17  ],
18    "config" : { "hscale" : 1 }
19  }
```
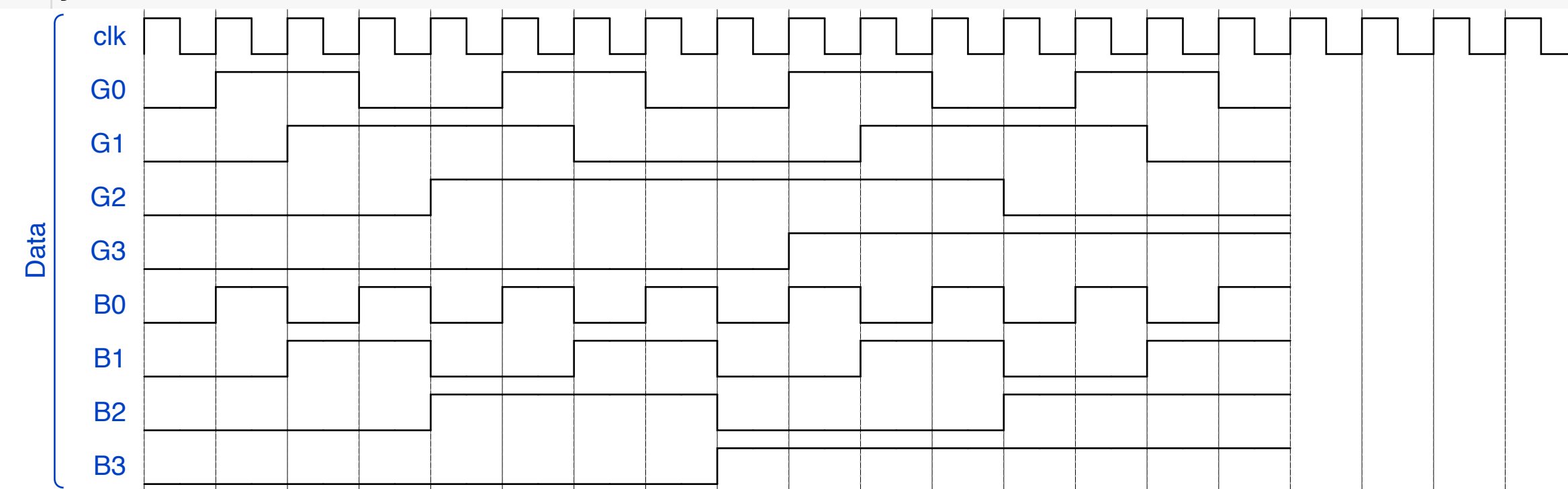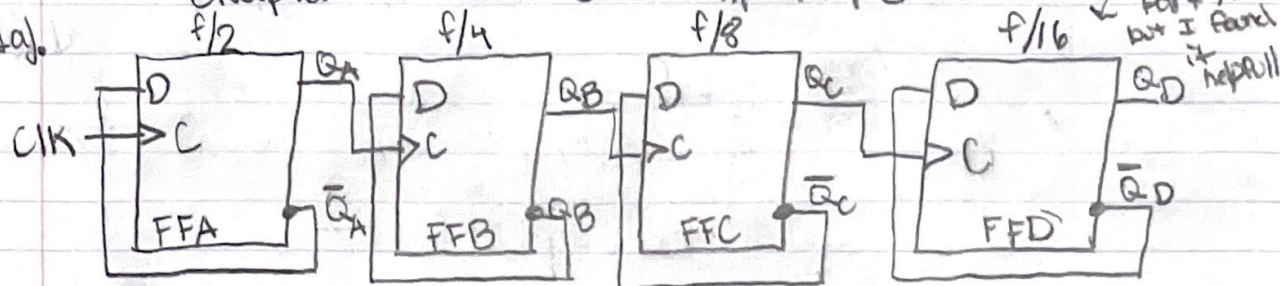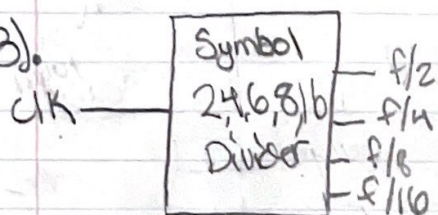
Chapter 7 Latches & Flip Flops

*not part of
Part A
but I found
it helpful

A). f/2   f/4   f/8   f/16

D   QA   D   QB   D   Qc   D   QD
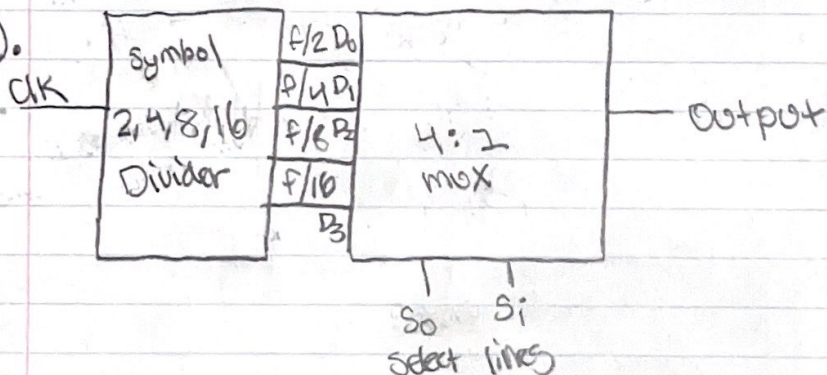
CLK → C   C   C   C

FFA Q̄A   FFB Q̄B   FFC Q̄c   FFD Q̄D

* each flip flop cuts the clock
frequency by two so we achieve
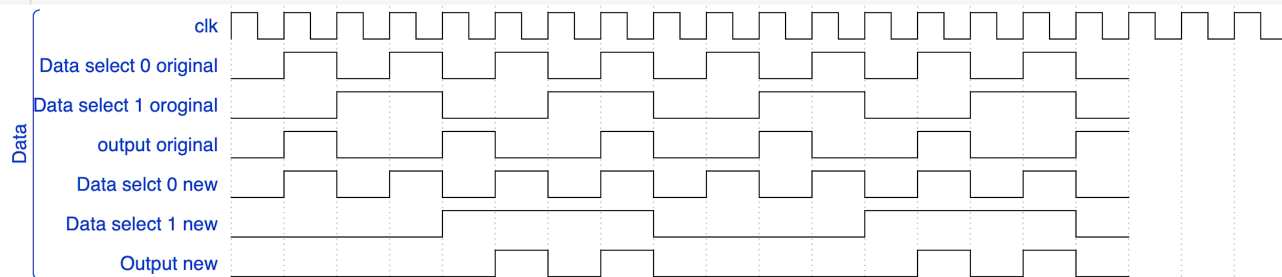the other two divisors simply by
adding flip flops

B).
clk —

| Symbol
2,4,6,8,16
Divider |
— f/2
— f/4
— f/8
— f/16

C).
clk —

| Symbol
2,4,8,16
Divider |

| f/2 D₀
f/4 D₁
f/6 D₂
f/16
D₃ |

4:1
mux

— Output

S₀   S₁
select lines

D). * See wavedrom

S₀	S₁	D
0	0	D₀ → output
0	1	D₁ → output
1	0	D₂ → output
1	1	D₃ both → output

the "output new" on wavedrom
shows a different delta select
lines compared to the original
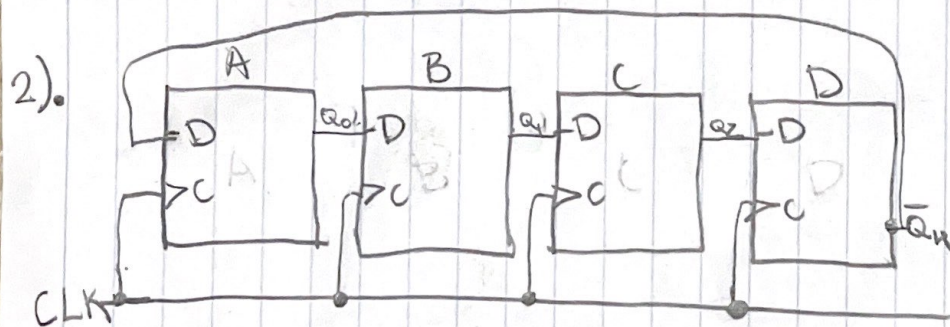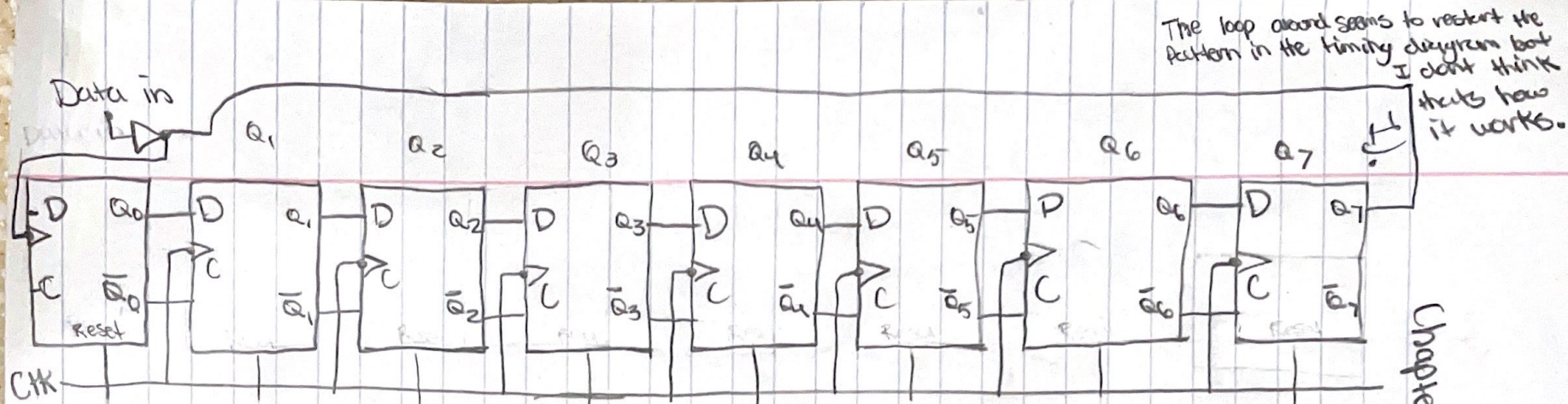S₀ & S₁ & output above the
new ones. Hopefully I did the right

```
{ "signal" : [
  ["Data",
   { name: "clk",      wave: "p.................." },

   { "name": "Data select 0 original", "wave": "lhlhlhlhlhlhlhlhl" },
   { "name": "Data select 1 oroginal ", "wave": "l.h.l.h.l.h.l.h.l" },
   { "name": "output original", "wave": "lhl.hl.hl.hl.hl.h" },

   { "name": "Data selct 0 new", "wave": "lhlhlhlhlhlhlhlhl" },

   { "name": "Data select 1 new", "wave": "l...h...l...h...l" },
   { "name": "Output new", "wave": "l....hlhl....hlhl" },



  ],
  ,
],
  "config" : { "hscale" : 1 }
}
```

Data in

1).

Q₁   Q₂   Q₃   Q₄   Q₅   Q₆   Q₇

CLK

2).

A   B   C   D

CLK

* See waveform

If we set each clock pulse to every 100ns, then at least two of the four channels will be high, causing the output to be true all the time.

* See waveform

Chapter 8 & 9 Shift Registers

```json
{ "signal" : [
  ["Data",
   { name: "clk",      wave: "p................" },

   { "name": "Q0", "wave": "lh...l..........." },
   { "name": "Q1", "wave": "l.h...l.........." },
   { "name": "Q2", "wave": "l..h...l........." },

   { "name": "Q3", "wave": "l...h...l........" },

   { "name": "Johnson Output", "wave": "lh.......l......." },



  ],
  ,
],
  "config" : { "hscale" : 1 }
}
```