1 Introductory Concepts

1a) On question 3 it says that D_i represents parallel data with a clock frequency of 4 MHz.

so, since $f = \frac{1}{T} \Rightarrow 4\,MHz = \frac{1}{.25\,\mu s}$

so the period of the clock signal is $T = .25\,\mu s$.

$D_1 = \frac{T_w}{T} = \frac{.25}{.50} =$ **50% duty cycle**

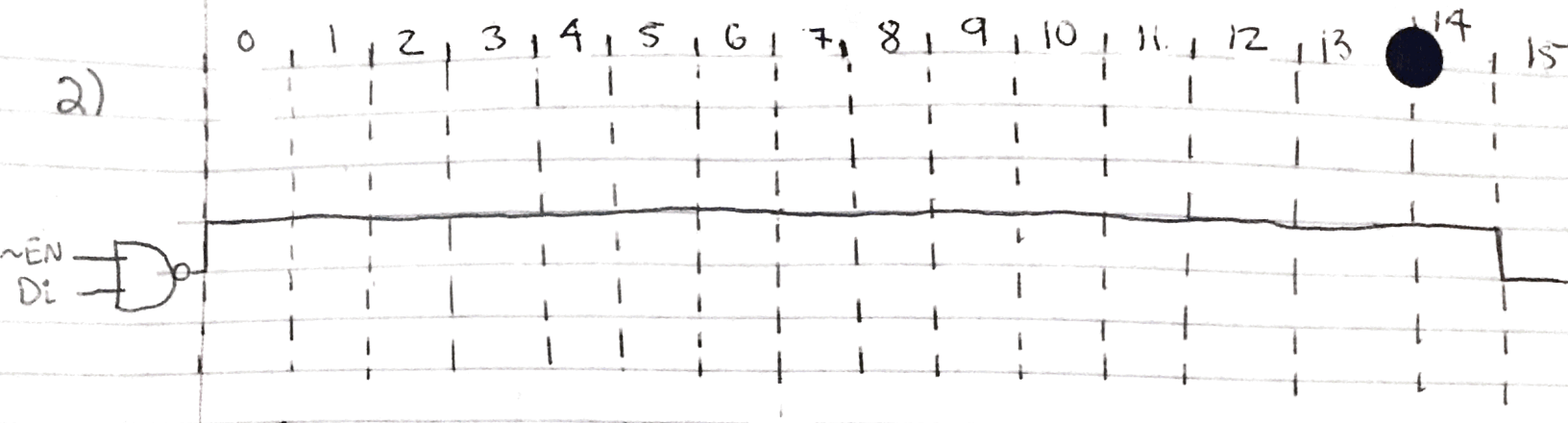
$D_2 = \frac{T_w}{T} = \frac{.50}{1.00} =$ **50% duty cycle**

$D_3 = \frac{T_w}{T} = \frac{1}{2} =$ **50% duty cycle**

$D_4 = \frac{T_w}{T} = \frac{2}{4} =$ **50% duty cycle**

b)
D_0: 0101 0101 0101 0101
D_1: 0011 0011 0011 0011
D_2: 0000 1111 0000 1111
D_3: 0000 0000 1111 1111

2)



3) a) $f = 4$ MHz so, $T = .25$ MS

the rate is $\frac{1 \text{ bit}}{.25 \text{ MS}} \times \frac{4 \times 10^6}{4 \times 10^6} = \boxed{\frac{4 \times 10^6 \text{ bits}}{1 \text{ second}}}$

b) It would definetely be **slower**.

I want to say it'd be 4 times slower since there are 4 inputs so: $\boxed{\frac{1 \times 10^6 \text{ bits}}{1 \text{ second}}}$

2 Number Systems, Operations & Codes

1. a) 1024

1024/2 = 512 r 0
512/2 = 256 r 0
256/2 = 128 r 0
128/2 = 64 r 0
64/2 = 32 r 0
32/2 = 16 r 0
16/2 = 8 r 0
8/2 = 4 r 0
4/2 = 2 r 0
2/2 = 1 r 0
1/2 = 0 r 1

Binary:
10000000000

b) 0xBBBB

0xB = 1011 so:

Binary:
1011101110111011

c) -2048

2048/2 = 1024 r0
1024/2 = 512 r0
512/2 = 256 r0
256/2 = 128 r0
128/2 = 64 r0
64/2 = 32 r0
32/2 = 16 r0
16/2 = 8 r0
8/2 = 4 r0
4/2 = 2 r0
2/2 = 1 r0
1/2 = 0 r 1

Binary:
1100000000000
↑ negative indicator

Since its negative the first digit will tell us it is negative.

2a) 65535

65535/16 = 4095 r F
4095/16 = 255 r F
255/16 = 15 r F
15/16 = 0 r F

hex: 0xFFFF

b) 1000 1000 1000 1000

1000 = 8

hex: 0x8888

3) 1024

1024/8 = 128 r0
128/8 = 16 r0
16/8 = 2 r0
2/8 = 0 r2

Octal: 2000

4) a) 2 bit changes occur

b) 1100

c) The shaft can encode 15 distinct angles and the angular precision is:
angular precision = $\frac{360^\circ}{15} = 24^\circ$

d) 8 bit encoder angular precision $\frac{360^\circ}{255} = 1.41^\circ$

3 Logic Gates

1.

$$\overline{\overline{(A(\bar{A}B))}\ \overline{(B(\bar{A}B))}}$$

$(A(\bar{A}B)) + (B(\bar{A}B))$ de Morgans

$(A(\bar{A}+B)) + (B(\bar{A}+\bar{B}))$ deMorgans

$A\bar{A} + A\bar{B} + B\bar{A} + B\bar{B}$ Distribute

$A\bar{B} + \bar{A}B$ $A\bar{A}=0$ XOR

$$\overline{(A\bar{B}+\bar{A}B)(A\bar{B}+\bar{A}B)}$$

$$\overline{A\bar{B}+\bar{A}B} + \overline{A\bar{B}+\bar{A}B}$$ De Morgan's

$(\overline{A\bar{B}})(\overline{\bar{A}B}) + \overline{A\bar{B}}(\overline{\bar{A}B})$

$(\bar{A}+B)(A+\bar{B}) + (\bar{A}+B)(A+\bar{B})$

$\bar{A}A + \bar{A}\bar{B} + B\bar{B} + AB + \bar{A}A + \bar{A}\bar{B} + B\bar{B} + AB$

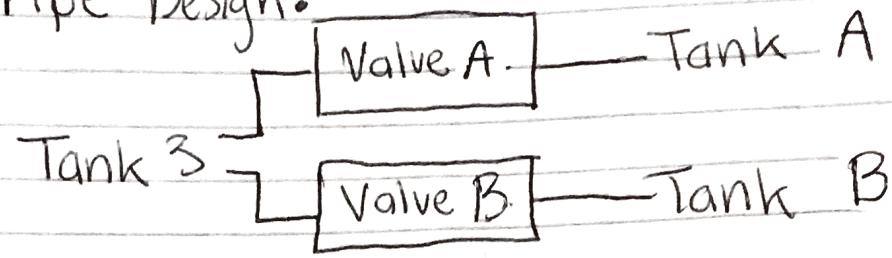
$\bar{A}\bar{B} + \bar{A}\bar{B} + AB + AB$

$\bar{A}\bar{B} + AB$ XNOR Gate

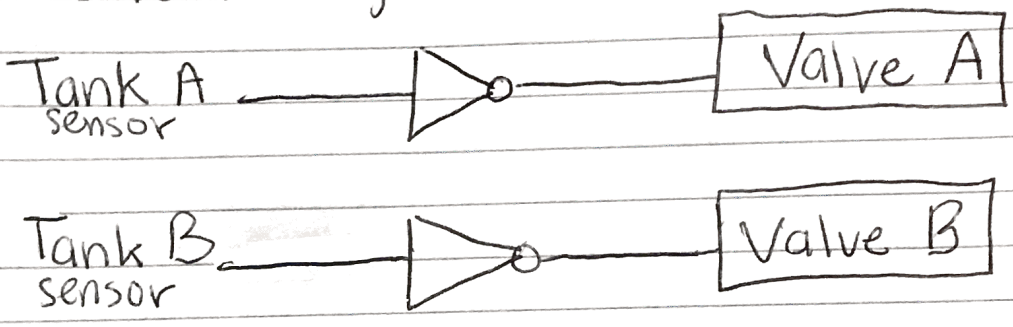
Truth Table:

B	A	X
0	0	1
0	1	0
1	0	0
1	1	1

3c) Pipe Design:



Circuit Logic



The valve will open on a High Signal. When the sensor reads LOW we will invert that to send a HIGH to the valve and when the sensor reads HIGH we will invert that to send a LOW to the valve and shut it off.

4 Boolean Algebra & Logic Simp.

1a) $X = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + ABCD + ABC\bar{D}$

b)

AB \ CD	00	01	11	10
00	1	1		
01				
11			1	1
10				

$\bar{A}\bar{B}C + ABC$

c) Stock D seems to be irrelevant to the state of the portfolio.

2a)

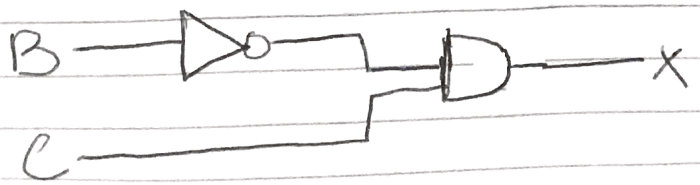
A \ BC	00	01	11	10
0	0	1	0	0
1	0	1	0	0

$X = \bar{B}C$

$X = (A + \bar{A})\bar{B}C$

$X = A\bar{B}C + \bar{A}\bar{B}C$

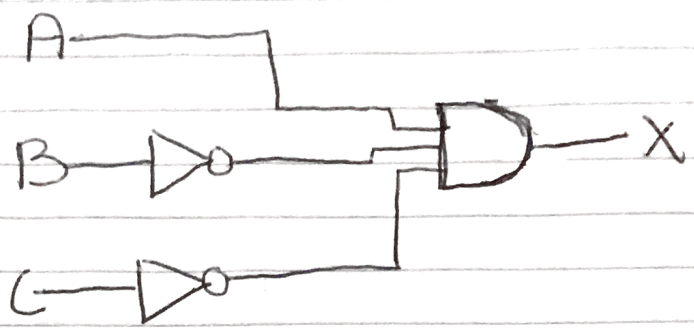
b)



5 Combinatorial Logic Analysis

1.

A	B	C	X
0	0	0	0
1	0	0	1
1	1	1	0
0	0	1	0
...	...	...	0



Bonus 2)

A, B, C, D, E = 100ns

Each gate has 10ns propogation delay so,

AB = -10
BC = -10
CD = -10
DE = -10
All Delay = -40

100ns
- 40ns
60ns

The pulse width of a 10 second propagation delay through each gate will still give you the desired 25ns minimum pulse width output.