Syllabus for Computer Logic and Circuit Design: PHYS306/COSC330

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Abstract

The core concepts of digital logic and digital circuit design are presented via integrated lectures and laboratory activities. The course begins with binary mathematics and floating point representation. The concepts of Boolean logic and logic gates, truth tables, combinatorial logic and Karnaugh maps follow. These core concepts prove useful in engineering, business, and science. Hands-on experience with programmable logic (firmware) and electronics lab equipment are emphasized in lab activities. Following the core modules, more complex digital functions are introduced. Examples include adders, comparators, multiplexers and demultiplexers, latches and flip-flops (memory elements), registers and shift registers, counters, and finite-state-machines (FSMs). We conclude with analog-to-digital conversion (ADCs), and digital-to-analog conversion (DACs). The ADC/DAC module builds to digital signal processing (DSP), as time permits. Students will create and present final projects that integrate course concepts using programmable logic and Python code.

***Pre-requisites**: PHYS180, COSC120. Pre-requisites may be waived at instructor discretion.*
***Course credits, Liberal Arts Categorization**: 3 Credits, None*
***Regular course hours**: Tuesdays and Thursdays from 15:00 - 16:20 in SLC 102 (lecture) and 104 (electronics lab).*
***Instructor contact information**: Discord: 918particle, Email: jhanson2@whittier.edu, Office: SLC 212, YouTube Channel: `www.youtube.com/918particle`, Book online appointments: `https://fgucmvjkylvmgqfsco.10to8.com`.*
***Office hours**: Use booking service link above to schedule meetings, and indicate in-person or online.*
***Attendance/Absence**: Students needing to reschedule midterms must notify the professor a few days in advance.*
***Late work policy**: Late work is generally not accepted, but is left to the discretion of the instructor.*
***Text**: Digital Fundamentals, Eleventh Edition., by Thomas L. Floyd (Pearson). This is a widely adopted text with a variety of online features, bonus chapters, code examples, and excellent homework sets. As a general rule, Prof. Hanson does not require students to purchase expensive texts. Please make arrangements with Prof. Hanson if you need assistance acquiring the book.*
***Grading**: The course grade will be a weighted average of assignment scores, and the weights are listed in Tab. 1.*

Assignment	Weight	Date
Homework sets	20%	Weekly on Fridays
Midterm 1	20%	February 22nd (take-home)
Midterm 2	20%	March 28th (take-home)
Final Exam	20%	May 1st (take-home)
Final Project	20%	April 23rd and 25th (in-class)

Table 1: A list of major assignments and grade weights.

***Grade Settings**: $< 60\% = F$, $> 60\%, \leq 70\% = D$, $> 70\%, \leq 80\% = C$, $> 80\%, \leq 90\% = B$, $< 90\%, \leq 100\% = A$. Pluses and minuses: 0-3% minus, 3%-6% straight, 6%-10% plus (e.g. 79% = C+, 91% = A-)*
***Homework Sets**: Due weekly on Fridays, including textbook problems, subitted code, and digital designs.*
***ADA Statement on Disability Services**: Whittier College is committed to make learning experiences as accessible as possible. If you experience physical or academic barriers due to a disability, you are encouraged to contact Student Disability Services (SDS) to discuss options. To learn more about academic accommodations, email disabilityservices@whittier.edu, call (562) 907-4825, or go to SDS which is located on the ground floor of Wardman Library.*
***Academic Honesty Policy**: `http://www.whittier.edu/academics/academichonesty`*
***Course Objectives**:*

- Fluency with number systems and binary codes, logic gates and Boolean algebra, and complex logic functions
- Application of digital logic in science, engineering, and business administration
- Practice translating a diagram to a prototype, and troubleshooting
- Create and control programmable logic using Python
- Create and verify final project designs that accomplish design tasks
- Present final project results to peers

Course Outline:

1. Week 0 - **Reading: Chapter 1 of Digital Fundamentals.**
   (a) First meeting - Tuesday, January 16th, 2024.
      i. Course introduction, syllabus distribution
      ii. *Laboratory tour and introductory laboratory exercises*
         A. Introduction to system on a chip (SoC): PYNQ-Z1
         B. Basic linux terminal commands
   (b) Second meeting - Thursday, January 18th, 2024.
      i. Digital concepts lecture content, block diagram of designs
      ii. Digital concepts and introduction of integrate circuit
         A. The PYNQ-Z1 SoC and Jupyter Notebooks
         B. Oscilloscopes and signal generation
2. Week 1 - **Reading: Chapters 1-2 of Digital Fundamentals.**
   (a) First meeting - Tuesday, January 23rd, 2024. *Reading: Chapter 1.*
      i. Logic functions: basic, combinatorial, and serial and parallel
      ii. Programmable logic and fixed IC logic
      iii. Test and measurement instruments
      iv. *Laboratory exercise, part I*
         A. Digital signals from PYNQ-Z1
         B. PL layer and `logictools` library
   (b) Second meeting - Thursday, January 25th, 2024. *Reading: Chapters 2-1 through 2-7*
      i. Decimal and binary numbers, conversions and arithmetic, signed numbers
      ii. *Laboratory exercise, part II*
         A. Representing a binary number with LEDs and `logictools`
         B. Capturing digital signals with the oscilloscope
3. Week 2 - **Reading: Chapter 2 of Digital Fundamentals.**
   (a) First meeting - Tuesday, January 30th, 2024. *Reading: Chapter 2-1 through 2-7.*
      i. Binary arithmetic, signed numbers
      ii. *Laboratory exercise, part I*
         A. Representing a binary number with LEDs, part II
         B. The `logictools` boolean generator: multiple logic functions, associative property
   (b) Second meeting - Thursday, February 1st, 2024. *Reading: Chapters 2-8, 2-10 through 2-12*
      i. Hexadecimal numbers
      ii. BCD, gray codes, and the parity and CRC error codes
      iii. *Laboratory exercise, part II*
         A. Breadboard prototyping
         B. Digital voltmeters, DC power supplies
4. Week 3 - **Reading: Chapters 3 of Digital Fundamentals.**
   (a) First meeting - Tuesday, February 6th, 2024. *Reading: Chapters 3-1 through 3-3*
      i. Hexadecimal numbers
      ii. BCD, gray codes, and the parity and CRC error codes
      iii. *Laboratory exercise, part I*
         A. Decimal, binary, and hexadecimal conversion (Python codelab)
         B. Random number generation, and matplotlib (`common` Jupyter notebooks)
         C. PYNQ-Z1 and `logictools`: finite state machines (FSMs) and logic simplification, part I
   (b) Second meeting - Thursday, February 8th, 2024. *Reading: Chapters 3-4 through 3-6*
      i. Logic gates: NOT, AND, OR, NAND, NOR, XOR, XNOR
      ii. *Laboratory exercise, part II*
         A. PYNQ-Z1 and `logictools`: finite state machines (FSMs) and logic simplification, part II

5. Week 4 - **Reading: Chapters 3-4 of Digital Fundamentals.**
   (a) First meeting - Tuesday, February 13th, 2024. *Reading: Chapters 3-8 and 3-9, 4-1 and 4-2*
      i. Programmable logic with gates
      ii. Boolean algebra, with applications and examples in business and engineering
      iii. *Laboratory exercise, part 1*
         A. PYNQ-Z1 and `logictools`: finite state machines (FSMs) and logic simplification, part III
   (b) Second meeting - Thursday, February 15th, 2024. *Reading: Chapters 4-3 through 4-10*
      i. DeMorgan's Theorems; further abstract examples in business and engineering
      ii. Boolean analysis of logic circuits, simplification
      iii. Truth tables, Karnaugh maps and SOP/POS minimization
      iv. *Laboratory exercise, part II*
         A. PYNQ-Z1 `logictools`: trace analyzer and pattern generator
         B. Use pattern generator to create multi-pin digital patterns, view with trace analyzer
6. Week 5 - **Reading: Chapter 5 of Digital Fundamentals**
   (a) First meeting - Tuesday, February 20th, 2024. *Reading: Chapters 5-1 through 5-3*
      i. Combinatorial systems of logic gates
      ii. Universal NAND and NOR gates
      iii. *Laboratory exercise, part I*
         A. Plot the trace of combinatorial logic, part I
   (b) Second meeting - Thursday, February 22nd, 2024. *Reading: Chapters 5-4 through 5-7*
      i. *Laboratory exercise, part II*
         A. Cumulative exercise with boolean generator, pattern generator, trace analyzer, and stepper
7. Week 6 - **Reading: Review chapters 1-5 of Digital Fundamentals**
   (a) First meeting - Tuesday, February 27th, 2024.
      i. Review material, collection of example problems
      ii. Catch-up on laboratory exercises and troubleshooting
   (b) Second meeting - Thursday, February 29th, 2024.
      i. **First midterm exam**
         A. Covers material from chapters 1-5
         B. Emphasis on binary operations, boolean algebra, and simple collections of gates
8. Week 7 - **Reading: Chapter 6 of Digital Fundamentals**
   (a) First meeting - Tuesday, March 5th, 2024. *Reading: Chapters 6-1 through 6-6*
      i. Adders, comparators, and encoders
      ii. *Laboratory exercise, part I*
         A. Probing fixed IC gates with scope and LEDs
   (b) Second meeting - Thursday, March 7th, 2024. *Reading: Chapters 6-7 through 6-11*
      i. Multiplexers and Demultiplexers
      ii. *Laboratory exercise, part II*
         A. Comparing fixed IC gates to programmable logic
         B. *Introduction to WeVideo, with Sonia Chaidez from Wardman Library*
9. **Spring Break:** March 11th - 15th, 2024.
10. Week 9 - **Reading: Chapters 7 and 8**
   (a) First meeting - Tuesday, March 19th, 2024. *Reading: Chapters 7-1 through 7-4, 7-5*
      i. S-R latches
      ii. Flip-flops, D and J/K
      iii. *Laboratory exercise, part I*
         A. Probing fixed IC counters with scope and LEDs, part I
         B. Formation of final project teams
   (b) Second meeting - Thursday, March 21st, 2024. *Reading: Chapters 7-5, and 8-1 through 8-4*

i. One-shots (timers) and pulse generation
ii. Shift registers
iii. *Laboratory exercise, part II*
    A. Probing fixed IC counters with scope and LEDs, part II
    B. Formation of final project teams

11. Week 10 - **Reading: Chapters 8 and 9**
    (a) First meeting - Tuesday, March 26th, 2024. *Reading: Chapters 8-5, 9-1 through 9-5*
        i. Shift register applications
        ii. Finite state machines (FSMs)
        iii. Asynchronous and synchronous counters
        iv. *Laboratory exercise, part I*
            A. Catch-up on laboratory exercises and troubleshooting
            B. *Work on final project proposals*
            C. Optional: FSM and counter example with `logictools`
    (b) Second meeting - Thursday, March 28th, 2024. *Reading: 9-6 through 9-8*
        i. Cascaded counters and applications of counters
        ii. *Laboratory exercise, part II*
            A. Study period for second midterm
            B. *Final project proposals due*
12. Week 11 - **Reading: Review chapters 6-9**
    (a) First meeting - Tuesday, April 2nd, 2024.
        i. Review material, collection of example problems
    (b) Second meeting - Thursday, April 4th, 2024.
        i. **Second midterm exam**
            A. Covers material from chapters 6-9
            B. Emphasis on adders, timers and pulse generation, shift registers, FSMs and counters
13. Week 12 - **Reading: Chapter 12**
    (a) First meeting - Tuesday, April 9th, 2024. **Reading: Chapters 12-1 through 12-3**
        i. Analog-to-Digital Conversion (ADC)
        ii. Digital-to-Analog Conversion (DAC)
        iii. *Laboratory exercise, part I*
            A. ADC/DAC with PMODs, part I
            B. Produce analog voltage from programmable logic, read analog voltage to programmable logic
    (b) Second meeting - Thursday, April 11th, 2024. **Reading: Chapters 12-4 through 12-5**
        i. Digital Signal Processing (DSP) - an introduction to sampling and digitization
        ii. *Laboratory exercise, part II*
            A. ADC/DAC with PMODs, part II
            B. ADC/DAC and Fourier series
14. Week 13 - **Reading: Chapters 2-3 of Digital Signal Processing**
    (a) First meeting - Tuesday, April 16th, 2024. *Reading: Chapter 2 of DSP*
        i. Selected topics in statistics and probability
        ii. Mathematics of sampling and digitization
        iii. *Laboratory exercise, part I*
            A. Hardware acceleration of an FIR data filter, part I
            B. Creation of custom PYNQ firmware with open-source IP
    (b) Second meeting - Thursday, April 18th, 2024. *Reading: Chapter 3 of DSP*
        i. The sampling theorem
        ii. Aliasing and anti-aliasing
        iii. *Laboratory exercise, part II*
            A. Hardware acceleration of an FIR data filter, part II

B. Measurement of the speed-up factor during data filtering

15. Week 14 [*Optional extra topics*] - **Reading: Chapters 30-31 of Digital Signal Processing**

    (a) First meeting - Tuesday, April 23rd, 2024. *Reading: Chapter 30 of DSP Guide*

        i. Complex numbers and the usage of complex numbers in DSP

        ii. *Laboratory exercise, part I*

            A. Exploring the Fourier transform, part I

            B. Power spectra and spectrograms

    (b) Second meeting - Thursday, April 25th, 2024. *Reading: Chapter 31 of DSP Guide*

        i. Complex numbers and the FFT, filters

        ii. *Laboratory exercise, part II*

            A. Exploring the Fourier transform, part II

            B. Filters

            C. Hardware-accelerated FIR filter and power spectrum

16. Week 14 - **Group presentations and Final Exam**

    (a) Meetings - Tuesday, April 23rd, 2024, and Thursday, April 25th, 2024.

        i. *Group presentations: 15 minutes each, 1-2 students per group*

        ii. *Final presentations can be via **option A**, live in person, or **option B** through WeVideo. A WeVideo tutorial will be given as part of the course.*

    (b) The final exam will be issued on May 1st, 2024 in take-home style. It will be due 48 hours after issued, and submitted in PDF form to Moodle.