Computer Logic and Digital Circuit Design (PHYS306/COSC330): Unit 3

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Summary

Unit 3 Summary

Functions of Combinatorial Logic

Reading: 6-1 - 6-6 (Tuesday)

Reading: 6-7 - 6-11 (Thursday)

1. Half-Adders and Full-Adders
    - Example from study guide
    - Propagation delays
2. Comparators
3. Decodors/Encoders

Half-Adders and Full-Adders, Ripple-Carry

Half-Adders and Full-Adders, Ripple-Carry

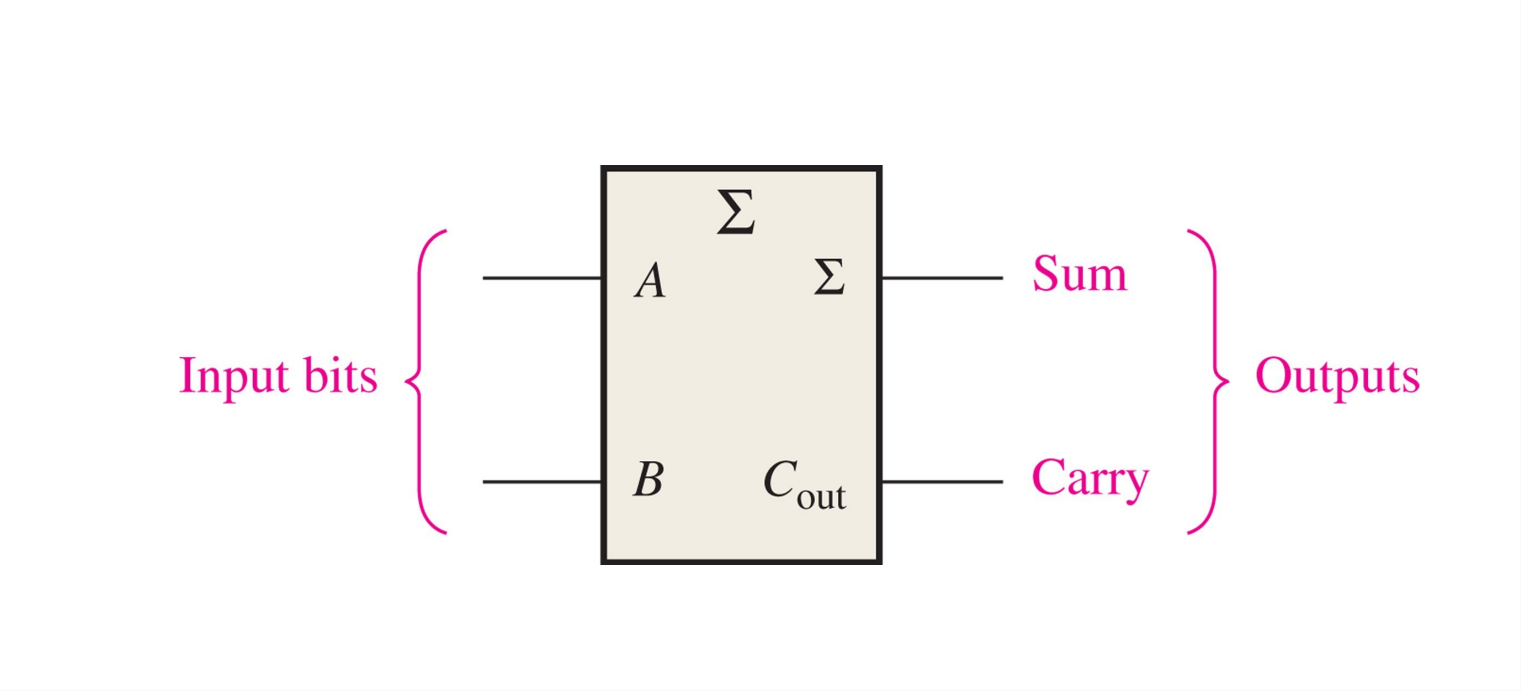


Figure 1: The desired inputs and outputs of the half-adder. There is no carry-input.

Half-Adders and Full-Adders, Ripple-Carry

TABLE 6–1

Half-adder truth table.

A	B	C_{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Σ = sum
C_{out} = output carry
A and B = input variables (operands)

Figure 2: The truth table of the half-adder for 2-bits. What gate action does this match?

Half-Adders and Full-Adders, Ripple-Carry

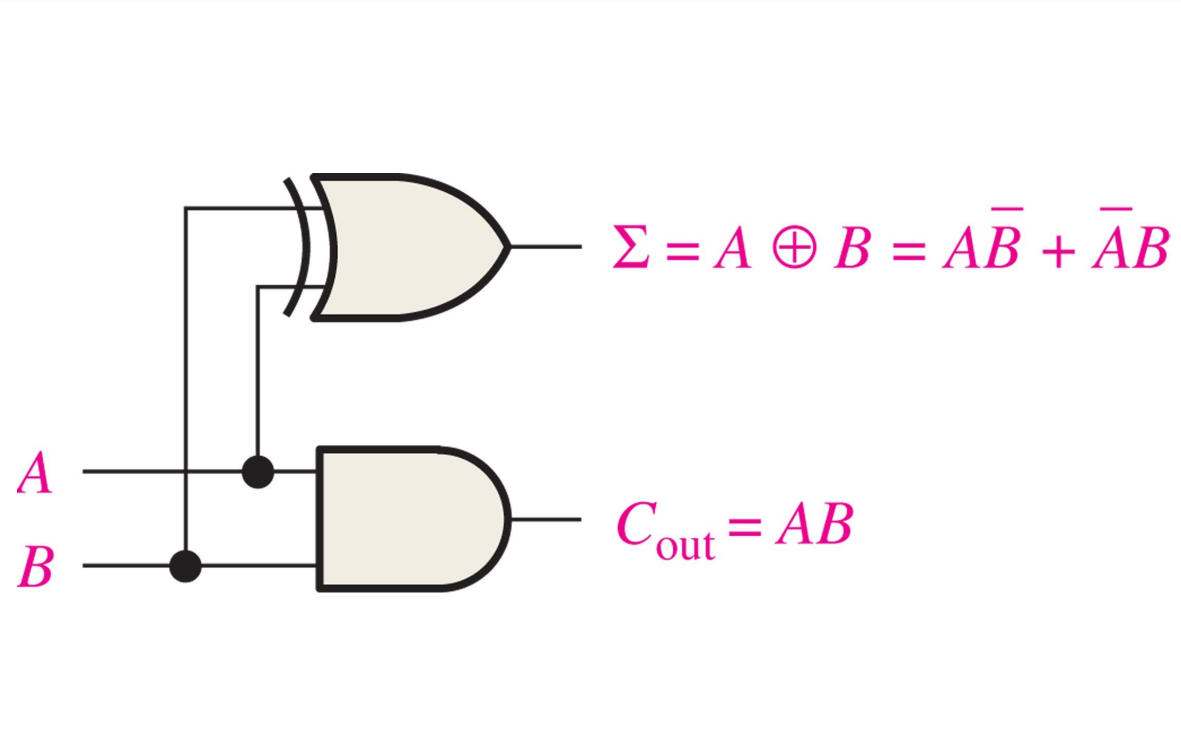


Figure 3: The logic function circuit diagram for the half-adder.

Half-Adders and Full-Adders, Ripple-Carry

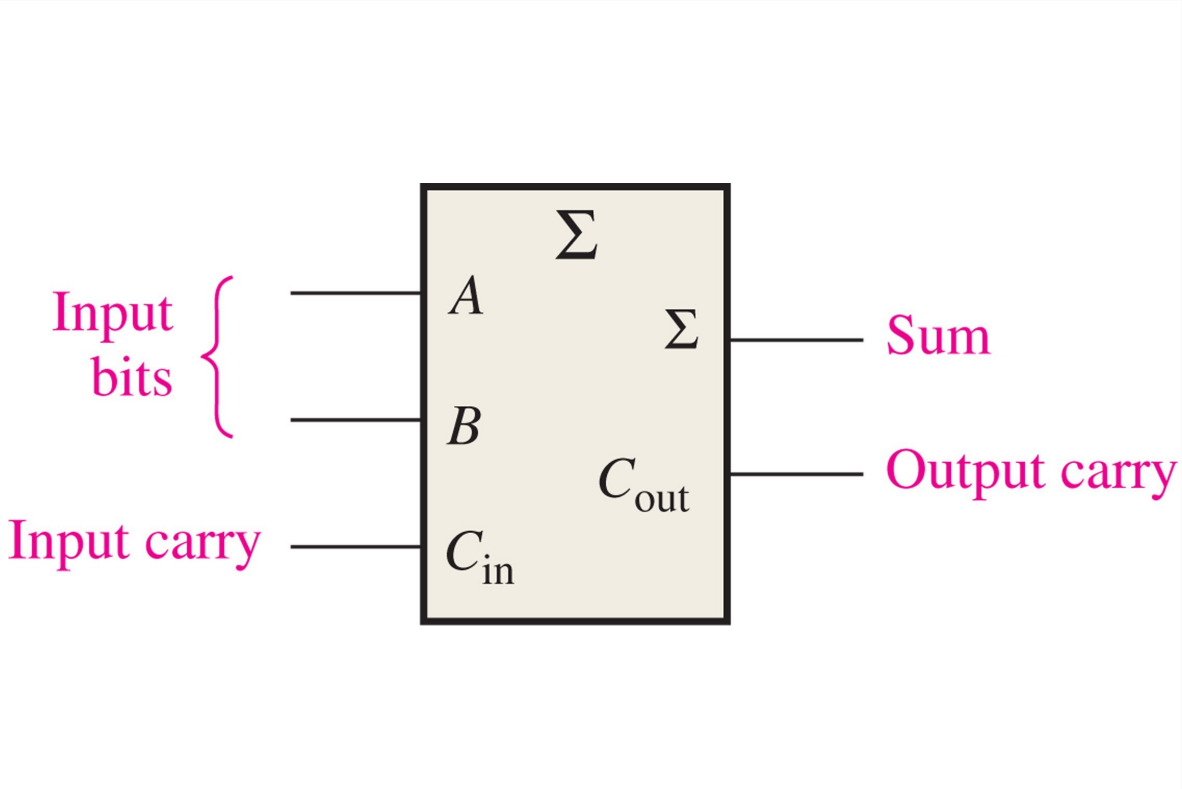


Figure 4: The desired inputs and outputs for the full-adder, with carry-input and carry-output.

Half-Adders and Full-Adders, Ripple-Carry

TABLE 6–2

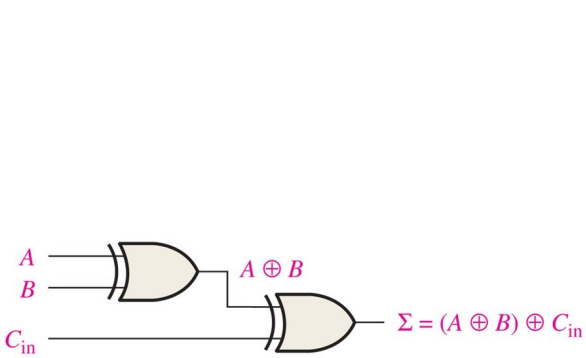
Full-adder truth table.

A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

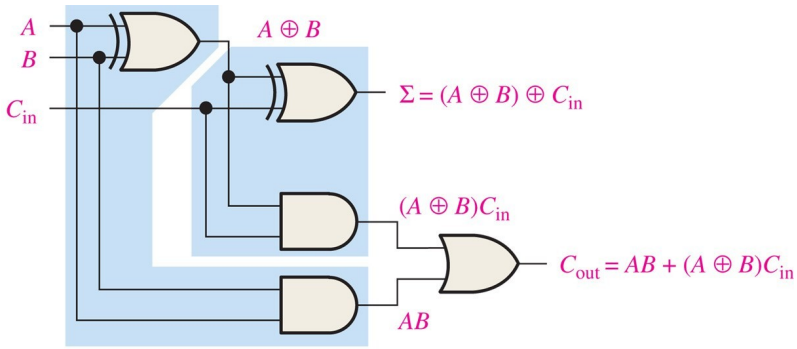
C_{in} = input carry, sometimes designated as CI
C_{out} = output carry, sometimes designated as CO
Σ = sum
A and B = input variables (operands)

Figure 5: The truth table for the full-adder is more complex due to the increased number of inputs.

Half-Adders and Full-Adders, Ripple-Carry



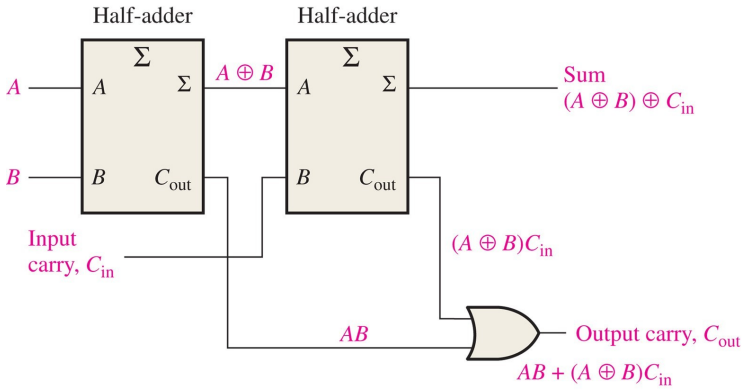
(a) Logic required to form the sum of three bits



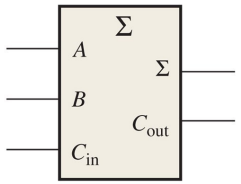
(b) Complete logic circuit for a full-adder (each half-adder is enclosed by a shaded area)

Figure 6: Circuit diagrams for the half-adder (left) and full-adder (right).

Half-Adders and Full-Adders, Ripple-Carry



(a) Arrangement of two half-adders to form a full-adder



(b) Full-adder logic symbol

Figure 7: Two half-adders to form a full-adder.

Half-Adders and Full-Adders, Ripple-Carry

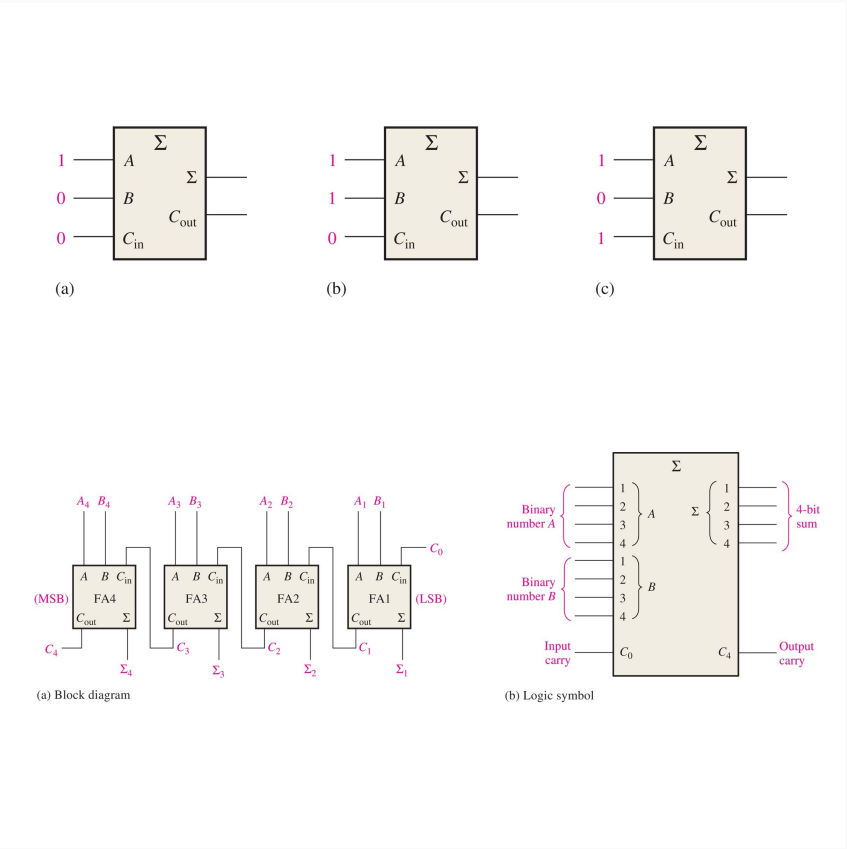


Figure 8: Four FA (full-adders) to add bits to the numbers being added.

Half-Adders and Full-Adders, Ripple-Carry

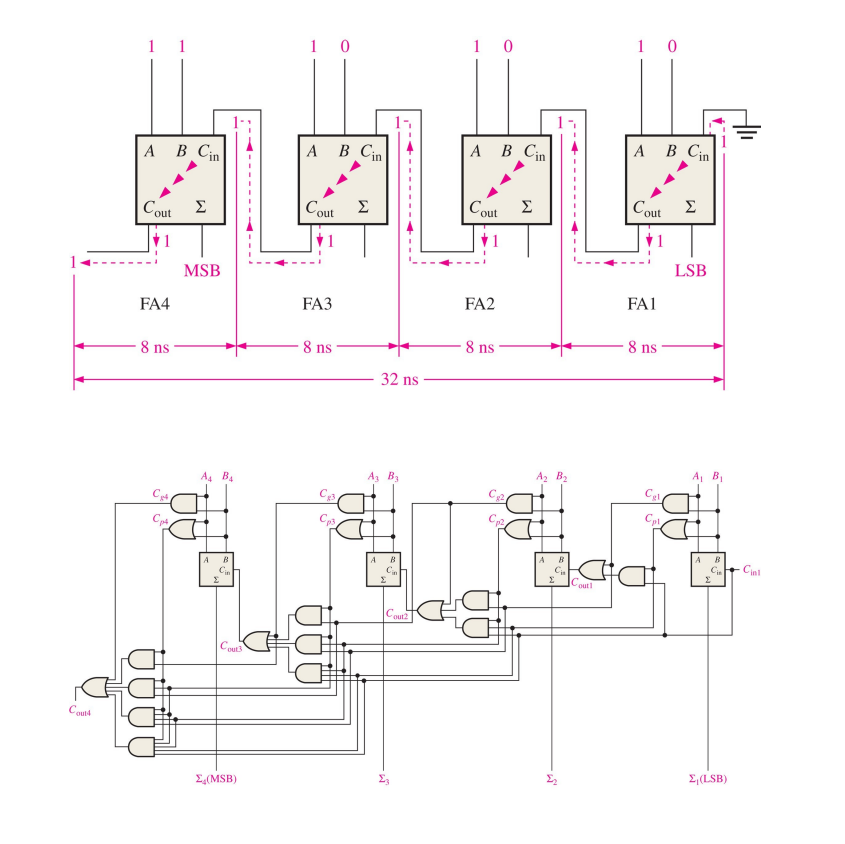


Figure 9: Propagation delays add serially in a full-adder with ripple carry topology.

Conclusion

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