Study Guide for Midterm 2

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November 17, 2021

1 Chapter 6 - Functions of Combinational Logic

1. a) Design a circuit below that adds two numbers in binary corresponding to outputs from two separate encoders. (b) Demonstrate how your design would add 1 and 9 with a timing diagram. (c) Add a separate input line with XNOR gates that switches the system to subtraction in 2's complement form.

2. Using basic logic gates like XNOR, AND, and inverters, (a) create a comparator that yields HIGH if the *magnitude* of two 2-bit binary numbers is equal. Assume that one or both of the numbers is a negative one, and that if a number is negative it is in *1's complement form.*

3. Generate the logic gates that convert 4-bit binary to 4-bit gray code, and show that it works with a timing diagram.

4. Consider Fig. 1. (a) Produce the output timing diagram. (b) Now develop a symbol for the 4 parallel bit parity checker, and connect four of them to a 4-to-1 multiplexer, with two data select lines. (c) Devise a *simple* timing diagram that align the data select lines with parity check outputs.

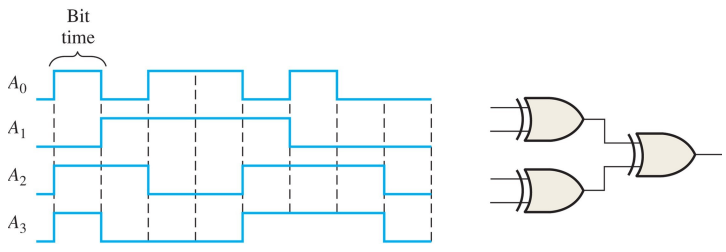
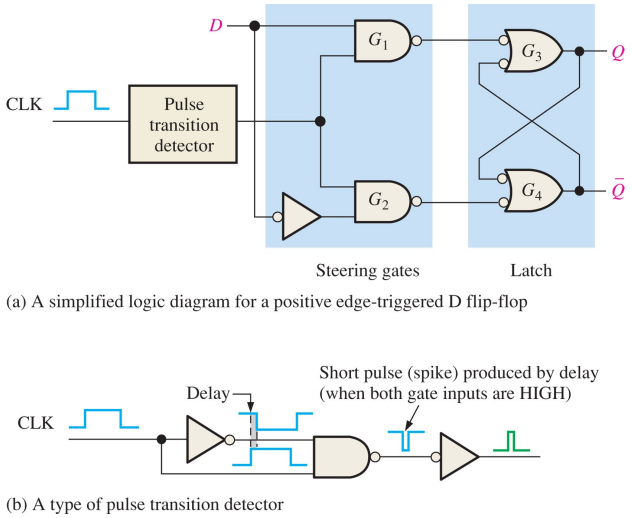


Figure 1: A parity checker for 4 parallel bits.

2 Chapter 7 - Latches, Flip-flops, and Timers

1. Consider Fig. 2. (a) If the CLK signal frequency is 20 MHz, what is the period? (b) If the delay through the inverter is 5 ns, what is the pulse width of the output from the pulse transition detector? (c) What is the duty cycle relative to the CLK signal? (d) Produce the timing diagram of the D-FF with the following bitstream as the input: 10001000, where each new bit is associated with a CLK pulse.



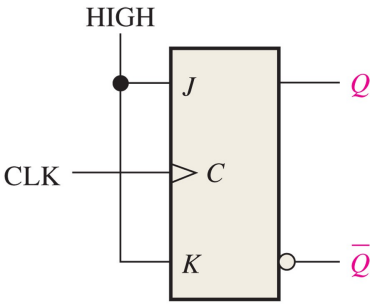
(a) A simplified logic diagram for a positive edge-triggered D flip-flop

(b) A type of pulse transition detector

A D Flip-flop with positive edge triggering.
- The pulse transition detector is responsible for the positive edge trigger
- CLK pulse passes through inverter with intrinsic delay, and another wire
- Both fed into effective AND gate, producing narrow pulse centered on CLK rising edge

Figure 2: The inner workings of a D FF with positive edge trigger.

2. Consider Fig. 3. (a) If the CLK frequency is 40 MHz, with what frequency does the Q output oscillate? (b) Using the same principle, construct a circuit with JK flip-flops that changes the CLK frequency from 40 MHz to 10 MHz.



JK Flip-Flop in permanent toggle mode.
- HIGH is connected to J and K inputs
- Positive edge of CLK signal triggers

Figure 3: A simple circuit built from a JK flip-flop (FF).

3 Chapters 8 and 9 - Shift Registers and Counters

1. Consider Fig. 4. (a) Design a timing diagram and serial input (serial data in) that causes a single bit to enter the register and then bounce from right to left repeatedly. (b) What is the frequency and duty cycle of Q_3?

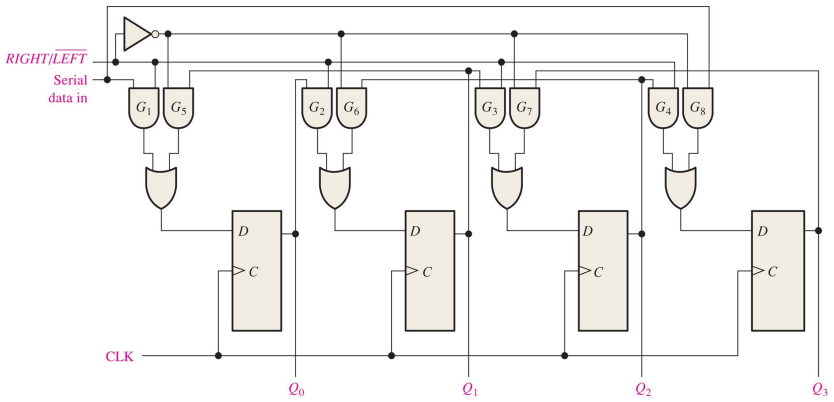


Figure 4: A 4-bit bidirectional shift register.

2. Consider Fig. 5. The waveforms are applied to the count enable, clear, and clock inputs as indicated. Show the counter output waveforms in proper relation to these inputs. The clear input is asynchronous.

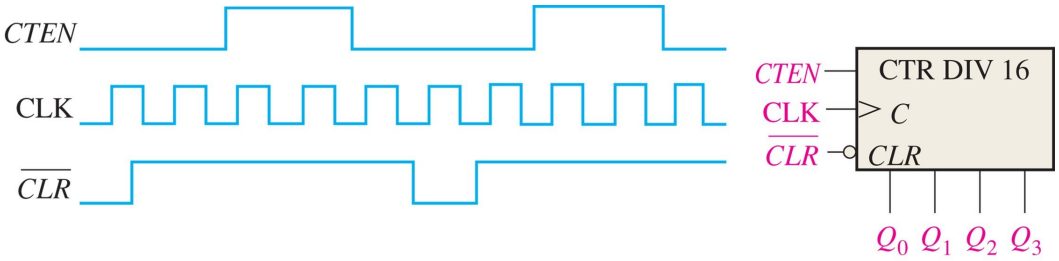


Figure 5: A 16-state counter with enable and clear functions.