Study Guide for Midterm 1

Dr. Jordan Hanson - Whittier College Dept. of Physics and Astronomy March 24, 2020

Chapter 1 - Introductory Concepts 1

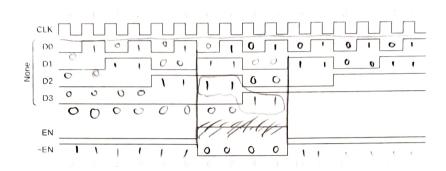
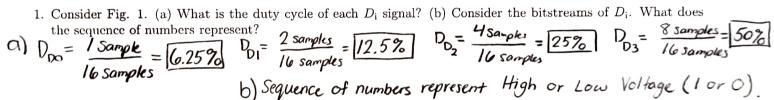


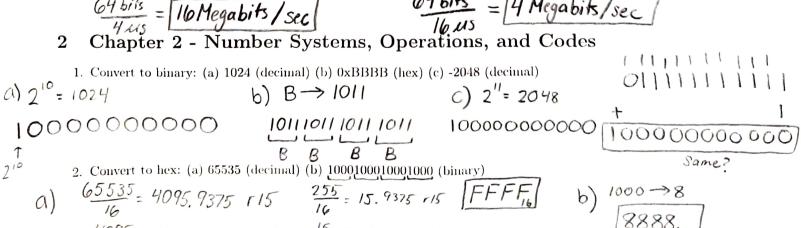
Figure 1: A timing diagram including a clock signal (CLK), a 4-bit parallel data stream (D0-D3), and enable/disable signals (EN/ \sim EN).



2. (a) Imagine that D_i signals enter a NAND gate, along with the \sim EN signal. Draw the resulting timing diagram.

3. Suppose
$$D_i$$
 represents parallel data with a clock frequency of 4 MHz. (a) What is the total bitrate (bits per second)? (b) What would be the bit rate if the system was serial instead of parallel?

a) 64 bits $\frac{1}{4} \mu s \cdot 16 = 4 \mu s$ b) 64 bits $\frac{1}{4} \mu s \cdot 4 = 16 \mu s$ $\frac{64 \text{ bits}}{4 \mu s} = \frac{16 \text{ Megabits / sec}}{16 \mu s} = \frac{4 \text{ Megabits / sec}}{16 \mu s}$ 2 Chapter 2 - Number Systems, Operations, and Codes



 $\frac{4095}{3} = 255.9375$ r/5 $\frac{15}{8}$ 0.9375 r/5 3. Cofeert to octal, in which the base is 8: 1024 (decimal).

3.
$$\frac{1024}{8} = 128 \text{ ro}$$

$$\frac{128}{8} = 16 \text{ ro}$$

$$\frac{16}{8} = 2 \text{ ro}$$

$$\frac{2}{8} = 0 \text{ ro.25} \times 8 = 2$$

4. Consider the gray code angular encoder in Fig. 2. (a) If the shaft rotates 180 degrees, how many bit changes occur? (b) If it rotates 180 degrees, and the initial gray code is 0000, what is the final gray code? (c) With 4-bit gray code, how many distinct angles can the shaft encode? What is 360 degrees divided by this number (i.e. the angular precision)? (d) What would be the angular precision of an 8 bit encoder?

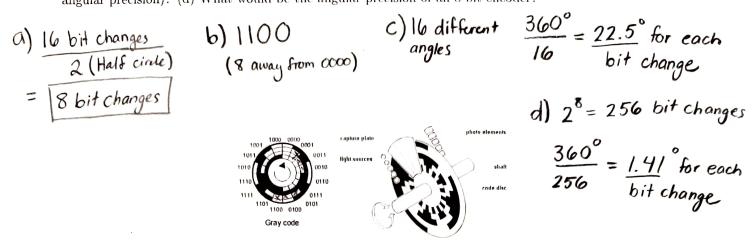


Figure 2: A gray code shaft encoder, or angular encoder, reports the angular position of an object digitally, using the gray code.

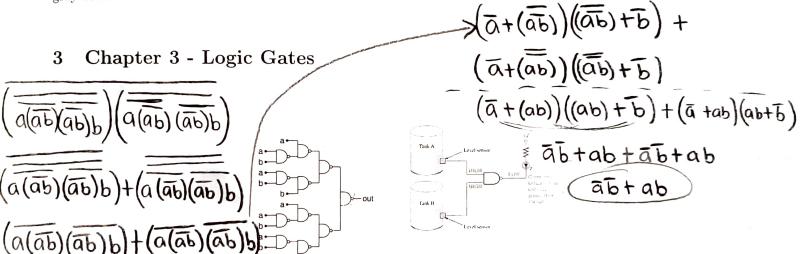
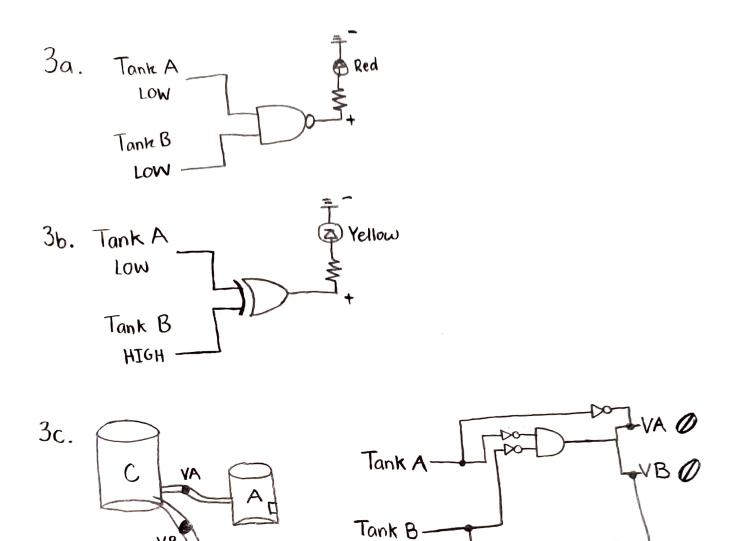


Figure 3: (Left) A logic gate combination. (Right) A liquid tank-level system built from a NAND gate.

1. Generate the simplified logic expression and truth table for Fig. 3, left. What do you call this type of gate?

2. Suppose signals D_0 and D_1 in Fig. 1 are connected to a and b in Fig. 3, left. Generate the timing diagram for out.

3. Creative design: A liquid tank system is depicted in Fig. 3. The sensors are HIGH when the liquid is above the level (green ON). (a) Create a red LED system that activates when both tanks are below the level, and draw it below. (b) Create a yellow LED system that activates when one tank is below and one tank is above the level. (c) Add a third tank with more liquid, and two pipes guiding liquid to tank A and B. Each pipe should have a valve. Add logic that opens the correct valve so as to fill only the low tank until it is no longer below the level.



Now Personally, I am into cars and learning about all these logic gates and circuits is allowing me to think about how my car's ECU functions with these gates. And now I understand how to read error codes in my car (i.e. MAF sensor circuit LOW or knock sensor circuit HIGH).

Chapter 4 - Boolean Algebra and Logic Simplification 4

- 1. Suppose an investment firm holds stock shares in four different stocks within a portfolio, labled A through D. The companies corresponding to stocks A through D are labeled inactive or active by the firm, based on information about their productivity. The firm notices that the portfolio output is on (rising) under the following conditions:
 - ✓ All four companies are inactive, or ...

Companies A through C are inactive, while company D is active, or ...

inactive >0

✓ All companies are active, or ...

Companies A through C are active, while company D is inactive.

(a) Develop a S-SOP expression for X, the portfolio's state (on or off) based on the data above. (b) Use a domain-4 Karnaugh map to simplify the S-SOP expression. (c) Which stock appears to be irrelevant to the state of the portfolio?

a) X = ABCD+ABCD+ABCD

b) x = ABC + ABC

C) Stock D is irrelevant.

2. A circuit contains three main branches leading to one output. The output is observed to fail under the following conditions below. (a) Use the domain-3 Karnaugh map to determine the conditions under which it does succeed. and write an S-SOP expression for the circuit. (b) Draw the circuit using gates.

when . A: false, B: false, C: false (0)

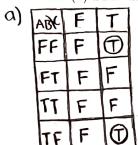
► A: false, B: true, C: false

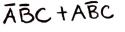
◆A: true, B: true, C: false

✓ A: true, B: false, C: false

✓ A: false, B: true, C: true

✓ A: true, B: true, C: true

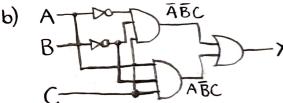




00

01

1 1 10



Chapter 5 - Combinatorial Logic Analysis 5

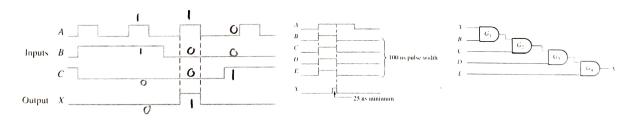
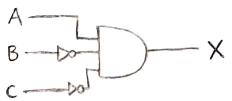


Figure 4: Diagrams for Sec. 5. (Left) Inputs are ABC, and the output is X. (Right) The inputs are ABCDE, and the output is X.

1. For the input waveforms shown in Fig. 4 (left), what logic circuit will generate the output waveform?



	ABC	0	
Ì	00	0	6
	01	C	0
	11	0	0
	10	T(1)	0

2. Bonus: Assumming a propagation delay of 10 ns through each gate in Fig. 4, determine if the desired output waveform X will be generated. The desired output is a pulse with a minimum width of 25 ns.