Tuesday Reading Assessment: Chapter 1

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1 Properties of Digital Pulses

1. A canonical digital pulse is depicted in Fig. 1 (left). Digital components like logic gates have finite capacitance and input impedance that depends on frequency.
   - Suppose the amplitude is CMOS HIGH (between 3.5V and 5V), and has a measured value of 3.55 V. What are the 10% and 90% amplitudes?
   - Suppose we treat the rise as linear, and we label the time of the 10% amplitude as $t = 0$ μs. If the rise occurs at 33 V/μs, when does the 90% amplitude occur? This is the rise time.
   - What is the pulse width, if the pulse width is 5 times the rise time?
   - If the next pulse always occurs two pulse widths from the initial rise, what are the period and frequency of the signal?

2 Logic Operations

1. Three basic logic gates are depicted in Fig. 1 (right).
   - What is the output bit stream from left gate if the input is: 1000 1000?
   - What is the output bit stream from the middle gate if the two input bit streams are: 1000 1000 and 1001 1001?
   - What is the output bit stream from the right gate if the two input bit streams are: 1000 1000 and 1001 1001?

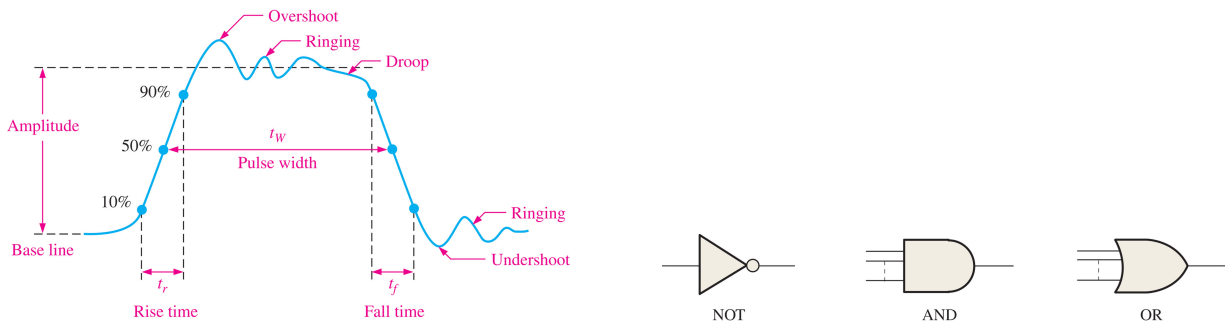

Figure 1: (Left) Properties of a digital pulse. (Right) Three basic logic gates.