Loren
Grey

Computer Logic Midterm

1. a)

D0: T = 2 ms $t_w = 1$ $(\frac{1}{2})100\% = 50\%$

D1: T = 4 ms $t_w = 2$ $(\frac{2}{4})100\% = 50\%$

D2: T = 8 ms $t_w = 4$ $(\frac{4}{8})100\% = 50\%$

D3: T = 16 $t_w = 8$ $= 50\%$

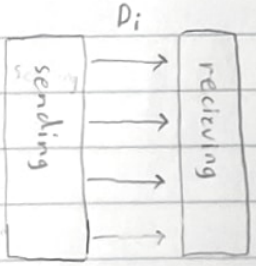
b) The sequence of numbers count the time t_w and represent columns for different outputs given the inputs D_0, D_1, D_2, and D_3.

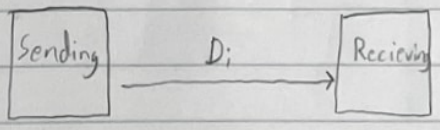
For example:

D0	=	1
D1	=	0
D2	=	0
D3	=	0

2. See wavedrom diagrams at attached doc.

3.





a) parallel → one time interval

$T = \frac{1}{4\,MHz} = .25\,\mu s$

b) frequency = 4 MHz

$T = \frac{1}{f} = \frac{1}{4\,MHz} = .25\,\mu s$

1 bit per .25 μs so 15(.25) = 3.75 μs to transfer each D_i

So total will be $D_i \times .25\,\mu s$ to complete transfer.

Chapter 2

1.

a) 1024/2

=512/2	0
256/2	0
128/2	0
64/2	0
32/2	0
16/2	0
8/2	0
4/2	0
2/2	0
1/2	1

1000000000

b) $B \times 16^3 + B \times 16^2 + B \times 16^1 + B \times 16^0$

$= 11 \times 16^3 + 11 \times 16^2 + 11 \times 16 + 11 \times 1$

= 48059 - decimal

48059/2	1	197/2	1
24029/2	1	98/2	1
12014/2	0	46/2	0
6007/2	1	23/2	1
3003/2	1	11/2	1
1501/2	1	5/2	1
750/2	0	2/2	0
375/2	1	1/2	1

1011101110111011

c)

-2048/2	0	64/2	0	2/2	0
1024/2	0	32/2	0	1/2	1
512/2	0	16/2	0		
256/2	0	8/2	0		
128/2	0	4/2	0		

-10000000000000

2.

a)

65535/16	15 = F
4095/16	15 = F
255/16	15 = F
15/16	15 = F
0	

FFFF

b) 1000100010001000

1000 1000 1000 1000

8 8 8 8

= 8888

3.

a) 

000 → 100 (3 changes) → 101 (1 change) → 110 (2 changes) → 111 (1 change) → 011 (1 change)

000 (3 changes)

1 + 2 + 1 + 3 + 1 + 2 + 1 + 3

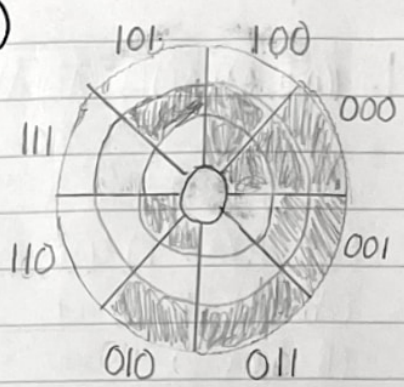
= **14 bit changes**

b) 000 → 001 → 011 → 010 → 110 (1 change) → 111 (1 change) → 101 (1 change) → 100 (1 change) → 000 (1 change)

1 + 1 + 1 + 1 + 1 + 1 + 1 + 1

= **8 bit changes**

c) from out → in



d) 3-bit / 45° → 8-bit / 8×15 = **8-bit / 120°**

Chapter 3

1. $\overline{(\overline{(\overline{AB})A})}\ \overline{(\overline{(\overline{AB})B})}\ \overline{(\overline{(\overline{AB})A})}\ \overline{(\overline{(AB)}B)}$

=

$\overline{ABA}\ \overline{\overline{AB}B} + \overline{\overline{AB}A}\ \ \overline{\overline{AB}B}$

$= (AB + \bar{A})(AB + \bar{B}) + (AB + \bar{A})(AB + \bar{B})$

$= (AB + \bar{A})(AB + \bar{B})$

$= (B + \bar{A})(A + \bar{B})$

$= BA + (A + \bar{B})\bar{A}$

$= BA + \bar{A}A + \bar{A}\bar{B}$

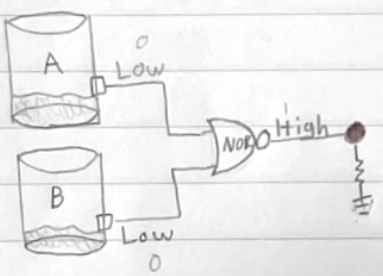
$= \boxed{BA + \bar{A}\bar{B}}$

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	1

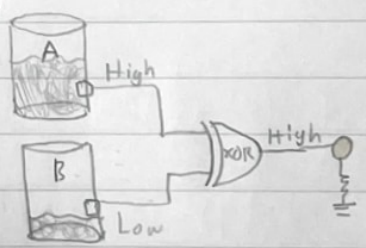
X-NOR gate

2. See wavedrom Doc

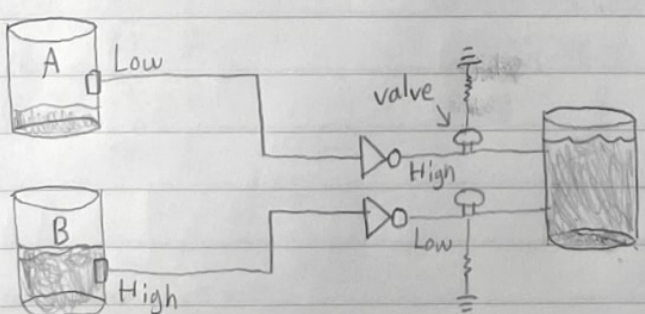
3. a)



b)



c)



Chapter 4

1.

a) $\boxed{ABCD + \bar{A}BCD + \bar{A}B\bar{C}D + \bar{B}ACD = X_{(ON)}}$

A	B	C	D	X
0	0	0	0	OFF
0	0	0	1	OFF
0	0	1	0	OFF
0	0	1	1	ON
0	1	0	0	OFF
0	1	0	1	OFF
0	1	1	0	OFF
0	1	1	1	ON
1	0	0	0	OFF
1	0	0	1	OFF
1	0	1	0	OFF
1	0	1	1	ON
1	1	0	0	OFF
1	1	0	1	OFF
1	1	1	0	OFF
1	1	1	1	ON

b)

AB \ CD	00	01	11	10
00	$\bar{A}\bar{B}\bar{C}\bar{D}$	$\bar{A}\bar{B}\bar{C}D$	$\bar{A}\bar{B}CD$	$\bar{A}\bar{B}C\bar{D}$
01	$\bar{A}B\bar{C}\bar{D}$	$AB\bar{C}D$	$\bar{A}BCD$	$\bar{A}BC\bar{D}$
11	$AB\bar{C}\bar{D}$	$AB\bar{C}D$	$ABCD$	$ABC\bar{D}$
10	$A\bar{B}\bar{C}\bar{D}$	$A\bar{B}\bar{C}D$	$A\bar{B}CD$	$A\bar{B}C\bar{D}$

Simplified S-Sop : CD

c) Stocks A and B should be eliminated from the portfolio because the profit only depends on C and D.

2.

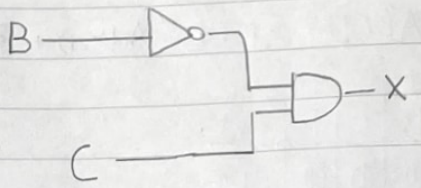
a)

A \ BC	00	01	11	10
0	$\bar{A}\bar{B}\bar{C}$	$\bar{A}\bar{B}C$	$\bar{A}BC$	$\bar{A}B\bar{C}$
1	$A\bar{B}\bar{C}$	$A\bar{B}C$	ABC	$AB\bar{C}$

A can be true or false : $\bar{A}\bar{B}C + A\bar{B}C$

S-SOP = $\boxed{\bar{B}C}$

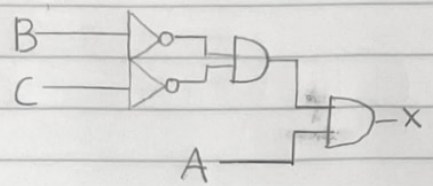
b)



Chapter 5

1.

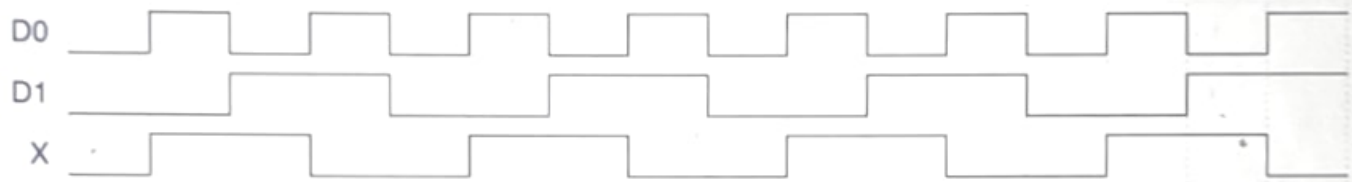
A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0



Chapter 1

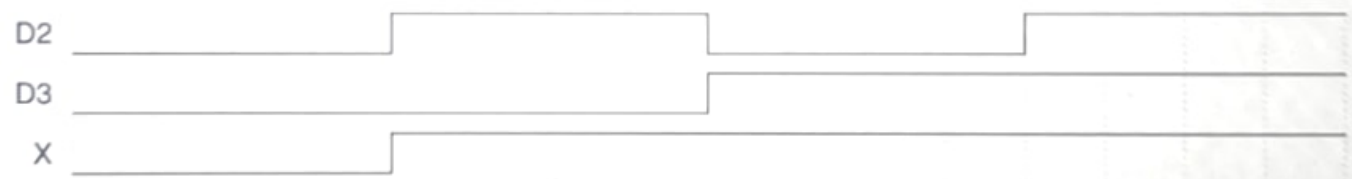
2a) Output of a XOR gate with D0 and D1 ad inputs:

```
{ signal: [
{ name: "D0", wave: 'lhlhlhlhlhlhlhlh' },
{ name: "D1", wave: 'l.h.l.h.l.h.l.h.' },
{ name: "X", wave: 'lh.l.h.l.h.l.h.l' }
]}
```



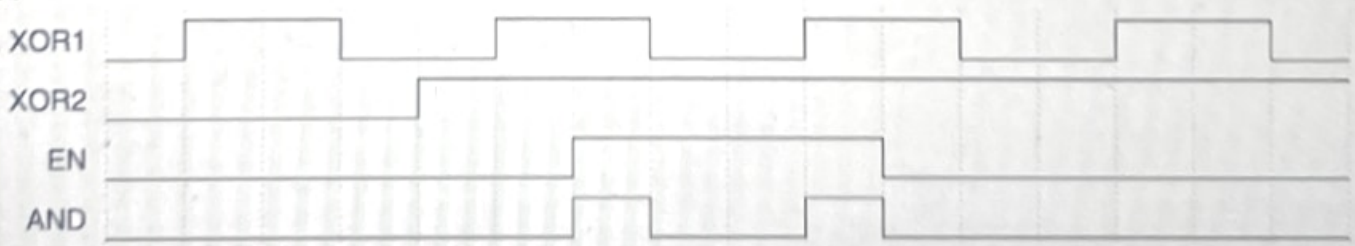
2b) Output of a XOR gate with D2 and D3 ad inputs:

```
{ signal: [
{ name: "D2", wave: 'l...h...l...h...' },
{ name: "D3", wave: 'l.......h.......' },
{ name: "X", wave: 'l...h..........' }
]}
```



2c) Output of a XOR gate with D0 and D1 ad inputs

```
{ signal: [
{ name: "XOR1", wave: 'lh.l.h.l.h.l.h.l' },
{ name: "XOR2", wave: 'l...h..........' },
{ name: "EN", wave: 'l.....h...l.....' },
{ name: "AND", wave: 'l.....hl.hl.....' }
]}
```



Chapter 3

2. Output of a XOR gate with D0 and D1 ad inputs

```
{ signal: [
{ name: "D0", wave: 'lhlhlhlhlhlhlhlh' },
{ name: "D1", wave: 'l.h.l.h.l.h.l.h.' },
{ name: "XNOR", wave: 'hl.h.l.h.l.h.l.h' }
]}
```