Syllabus for Computer Logic and Circuit Design: PHYS306/COSC330

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Abstract

In this inaugural course on computer logic and digital circuit design will be divided into two parts: first, a **theoretical** mathematical basis for digital circuits will be introduced, followed by a tactile introduction to **experimentation** with digital circuits, concluding with *analog to digital conversion*. The theoretical portion of the course will cover binary numerical representation, boolean algebra, truth tables, and combinatorial logic, culminating with the concept of tasks and functions represented by arrays of logic gates. In the experimental portion of the course, the theory will be applied understanding digital circuit elements such as logic gate arrays, flip-flops, counters, memory elements (RAM), and analog to digital conversion. The course will conclude (time permitting) with an introduction to microcontrollers.

Pre-requisites: *PHYS180 and COSC120. (This is the inaugural semester of a course which is expected to evolve over time. The pre-requisites may be waved at the discretion of the instructor to admit a broad initial group of students).*
Course credits, Liberal Arts Categorization: *3 Credits, None*
Regular course hours: *Tuesday and Thursday from 13:30 - 14:50 in SLC 104*
Instructor contact information: *jhanson2@whittier.edu, tel. 562.907.5130*
Office hours: *Monday 8:00-10:00 in SLC 212*
Attendance/Absence: *Students needing to reschedule midterms and exams should notify the professor a reasonable time beforehand. Further attendance issues are left to the discretion of the instructor.*
Late work policy: *Late work will not be accepted.*
Text: *Learning the Art of Electronics by Thomas C. Hayes. This is a laboratory book derived from text The Art of Electronics, 3rd Edition by Horowitz and Hill. The text is a beautiful and vastly comprehensive desk reference for electronics design. The laboratory book is recommended for purchase, but the text is not required. Please inform the instructor if you cannot purchase the laboratory book, and arrangements will be made.*
Grading: *There is no final exam for this course. There will be two midterms, each worth 15% of the final grade. There will be two group presentations, each worth 15% of the grade (see below). Finally, the remaining 40% of the grade will be homework comprised of reading quizzes, exercises, and selected simple circuit projects.*
Grade Settings: *$< 60\%$ = F, $> 60\%, \leq 70\%$ = D, $> 70\%, \leq 80\%$ = C, $> 80\%, \leq 90\%$ = B, $< 90\%, \leq 100\%$ = A. Pluses and minuses: 0-3% minus, 3%-6% straight, 6%-10% plus (e.g. 79% = C+, 91% = A-)*
Homework Sets: *Due weekly on Tuesdays. Initial problem sets will focus on theoretical exercises from laboratory book and lecture notes. As the semester progresses, the homework will shift to circuit projects, and submission of code or algorithms. Reading quizzes will be in a JITT format (Just in Time Teaching), due each class period.*
Bonus Essay: *Students may submit an essay on the history of scientific developments covered in the course, due at the end of the semester. The essay must address scientific arguments and results, must include library references, and must have at least 10 pages. The grade of this paper will replace the lowest midterm score if submitted.*
ADA Statement on Disability Services: *The Americans with Disabilities Act (ADA) is a federal anti-discrimination statute that provides comprehensive civil rights protection for persons with disabilities. Among other things, this legislation requires that all students with disabilities be guaranteed a learning environment that provides for reasonable accommodation of their disabilities. If you believe you have a disability requiring an accommodation, please contact Disability Services: disabilityservices@whittier.edu, tel. 562.907.4825.*
Academic Honesty Policy: $http://www.whittier.edu/academics/academichonesty$
Course Objectives:

- To master binary logic and the application of binary logic to circuits

- To train in the art of transforming a diagram into a working prototype

- To develop confidence in electronics design and experimentation

Course Outline:

1. **Part 0: Introduction to circuits and general review - Week 1**

   (a) Unit 1: Go! Build a heterodyne AM radio from a pile of parts and instructions
      i. Soldering, resistors, capacitors, and DC power (batteries)
      ii. Kirchhoff's rules, Ohm's law

2. **Part 1: Theoretical digital logic concepts - Weeks 2-6**

   (a) Unit 1: Digital Mathematics and Logic
      i. Introduction to digital concepts
      ii. Decimal, binary and hexidecimal number systems
      iii. Numerical operations and codes

   (b) Unit 2: Theoretical logic gates and gate operations
      i. Logic gates of various types, truth tables
      ii. Programmable logic
      iii. Boolean algebra and logic simplification
      iv. Karnaugh maps

   (c) Unit 3: Combinatorial logic, and functions of combinatorial logic
      i. Basic combinatorial circuits
      ii. Universal gates
      iii. Time-dependent waveform analysis
      iv. Adders, comparators, decoder/encoder, multiplexers

3. **First midterm, and first set of group presentations, end of Week 6**

   (a) Midterm 1
      i. Conceptual understanding of AM radio functionality
      ii. Numerical problems regarding binary numbers
      iii. Logic problems regarding gates and their truth tables and Karnaugh maps

   (b) Group presentation 1 - Design and test a circuit involving a binary adder
      i. Stage 1: propose a simple circuit or digital project, submit by *Week 2*
      ii. Stage 2: submit design, either copied from book, internet, or a custom design by *Week 4*
      iii. Stage 3: build and test project in groups *as determined by group*
      iv. Stage 4: present results, followed by group discussion and questions *during Week 6*

4. **Part 2: Experimentation with digital circuits - Weeks 7-13**

   (a) Logic Gates laboratory - Learning AoE Unit 14L
   (b) Flip-flops laboratory - Learning AoE Unit 15L
   (c) Counters laboratory - Learning AoE Unit 16L
   (d) Random Access Memory (RAM) laboratory - Learning AoE Unit 17L
   (e) Analog to digital conversion laboratory - Learning AoE Unit 18L

5. **Second midterm, and second set of group presentations, end of Week 13**

   (a) Midterm 2
      i. Design of NAND gates (exam format)
      ii. Design of flip-flops (exam format)
      iii. Concept of analog to digital converion
      iv. Debug a counter (lab format)

   (b) Group presentation 2 - Design and test a digital circuit of group's choice
      i. Stage 1: propose a simple circuit or digital project, submit by *Week 7*
      ii. Stage 2: submit design, either copied from book, internet, or a custom design by *Week 9*
      iii. Stage 3: build and test project in groups *as determined by group*
      iv. Stage 4: present results, followed by group discussion and questions *during Week 13*