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See attached pages for work shown

Computer Logic and Digital Circuit Design: Midterm 1

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means
I had trouble
or was
unsure
of answer

1 Chapter 1 - Introductory Concepts

$$T_{D0} = 2 \text{ s}$$
$$t_{wD0} = 1$$

$$T_{D1} = 4 \text{ s}$$
$$t_{wD1} = 2$$

$$T_{D2} = 8 \text{ s}$$
$$t_{wD2} = 4$$

$$T_{D3} = 16 \text{ s}$$
$$t_{wD3} = 8$$

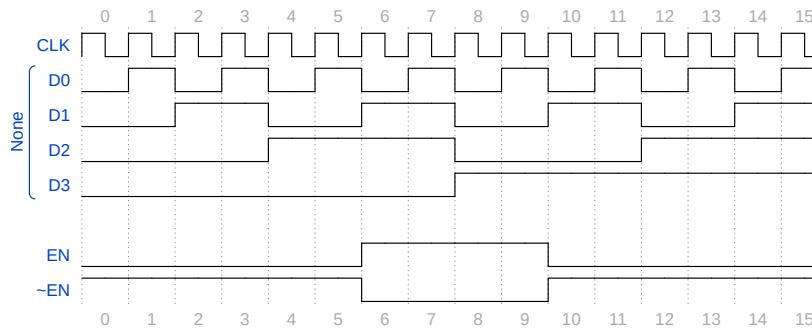


Figure 1: A timing diagram including a clock signal (CLK), a 4-bit parallel data stream (D0-D3), and enable/disable signals (EN/~EN).

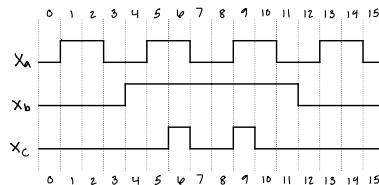
confused about what
is being asked here

1. Consider Fig. 1. (a) What is the duty cycle of each D_i signal? (b) Consider the bitstreams of D_i . What does the sequence of numbers represent?

(a) each D_i signal has a 50% duty cycle

(b) binary data stream that determines whether the system is enabled
or disabled? parallel data

2. (a) Create the timing diagram representing the output of an XOR gate with D_0 and D_1 as inputs. (b) Do the same for D_2 and D_3 . (c) Finally, create the timing diagram representing the output of a 3-input AND gate with the XOR gates from parts (a) and (b), and the EN signal as inputs.



3. Suppose D_i represents parallel data with a clock frequency of 4 MHz. (a) What is the total bitrate (bits per second)? (b) What would be the bit rate if the system was serial instead of parallel?

a) 16 Megabits per second

b) 4 Megabits per second

2 Chapter 2 - Number Systems, Operations, and Codes

1. Convert to binary: (a) 1024 (b) 0xBBB (c) -2048

a) 100000000000 b) 1011101110111011 c) 1000 0000 0000

2. Convert to hex: (a) 65535 (b) 1000100010001000

a) FFFF

b) 8888



3. Design problem. Consider the angular shaft encoder in Fig. 2. The IR emitter/detector detects IR light reflected from white sectors, while the dark sectors absorb the light. The sectors are encoded in binary. For example, starting from inner sectors and reading outward, dark-dark-light is translated to state 001 by the detector. If the shaft rotates 45 degrees, the detector records a state change. (a) If the initial state is 000 and the shaft rotates 360 degrees, how many bit changes occur? (b) How many bit changes would occur if the shaft position was encoded in gray code? (c) Draw the correct face of the shaft encoder, encoded in 3-bit gray code instead of binary¹ (d) If 45 degrees is the angular precision with 3-bit gray code, what is the angular precision with 8 bit gray code?

a) 14

see attached
pages for work

d) 1.4° ??

b) 8

c) grey code

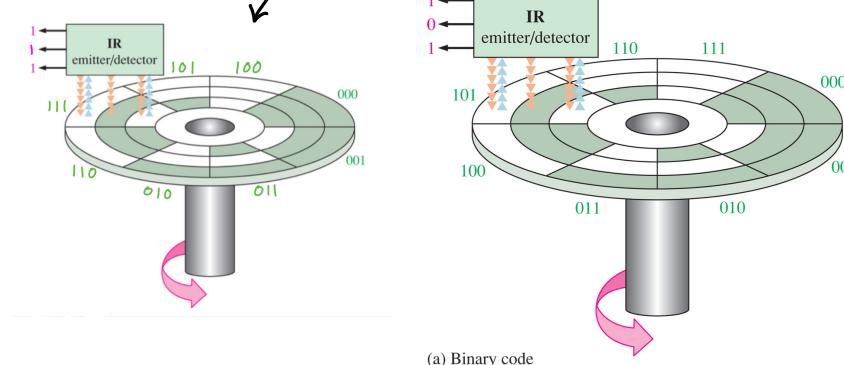


Figure 2: A gray code shaft encoder, or angular encoder, reports the angular position of an object digitally, using the gray code.

3 Chapter 3 - Logic Gates

		out
a	b	
0	0	1
1	0	0
0	1	0
1	1	1

Nand

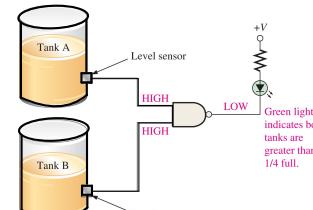
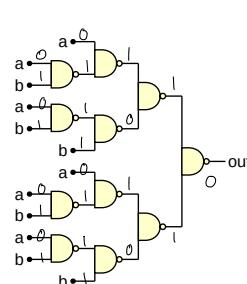
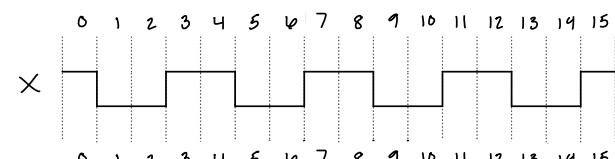


Figure 3: (Left) A logic gate combination. (Right) A liquid tank-level system built from a NAND gate.

1. Generate the simplified logic expression and truth table for Fig. 3, left. What do you call this type of gate?



2. Suppose signals D_0 and D_1 in Fig. 1 are connected to a and b in Fig. 3, left. Generate the timing diagram.

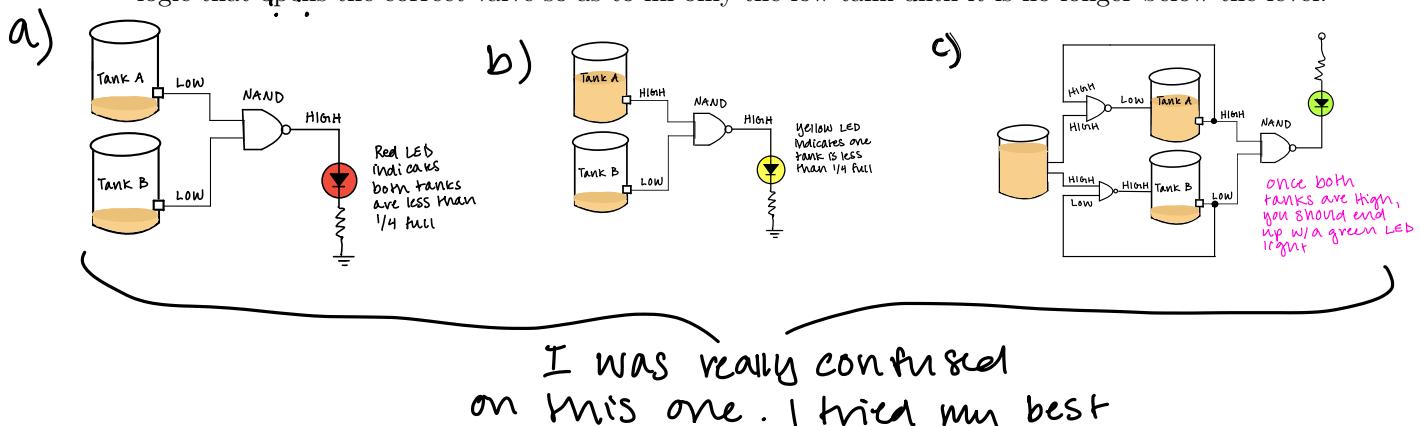


¹Caution: I believe the figure in the textbook contains errors.



?? attached pages have bigger version
of systems

- 3. Design problem.** A liquid tank system is depicted in Fig. 3 (right). The sensors are HIGH when the liquid is above the level. (a) Create and display a red LED system that activates when both tanks are *below* the level. (b) Create and display a yellow LED system that activates when one tank is below and one tank is above the level. (c) Add a third tank with two pipes guiding liquid to tanks A and B. Each pipe should have a valve. Add logic that opens the correct valve so as to fill only the low tank until it is no longer below the level.



4 Chapter 4 - Boolean Algebra and Logic Simplification

1. Suppose an investment firm manages a portfolio with shares in four stocks, labeled A through D. The companies corresponding to stocks A through D are labeled *inactive* or *active* by the firm, based on productivity information. The firm notices that returns (profits) for the portfolio increase under the following conditions:

- All four companies are active, or ...
- Companies A and B are inactive, while companies C and D are active, or ...
- Company A is inactive, while companies B, C, and D are active, or ...
- Company B is inactive, while companies A, C, and D are active.

- (a) Develop a S-SOP expression for X , the portfolio's state. If profit is increasing, label the output ON, and label it OFF if profit is decreasing. (b) Use a domain-4 Karnaugh map to simplify the S-SOP expression. (c) Based on your analysis, which stock or stocks should be eliminated from the portfolio?

a) $ON = ABCD + \bar{A}\bar{B}CD + \bar{A}\bar{B}CD + A\bar{B}CD$

b)

$\bar{C}D$	00	01	11	10
$\bar{A}B$	00	OFF	OFF	ON OFF
01	OFF	OFF	ON	OFF
11	OFF	OFF	ON	OFF
10	OFF	OFF	ON	OFF

c) companies A and B stocks should be eliminated from the portfolio (I think)



2. A circuit contains three main branches leading to one output. The output is observed to fail under the following conditions below. (a) Use the domain-3 Karnaugh map to determine the conditions under which it does succeed, and write an S-SOP expression for the circuit. (b) Draw the circuit using gates.

- A: false, B: false, C: false
- A: false, B: true, C: false
- A: true, B: true, C: false
- A: true, B: false, C: false
- A: false, B: true, C: true
- A: true, B: true, C: true

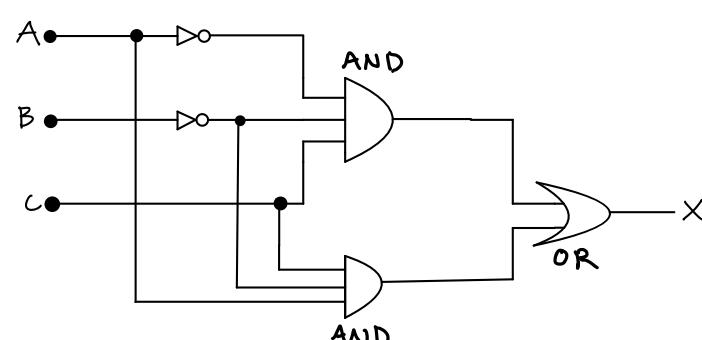
a)

C		
$A\bar{B}$	\bar{B}	1
00	0	1
01	0	0
11	0	0
10	0	1

$$X = \bar{A}\bar{B}C + A\bar{B}C$$

S-SOP expression

b)



5 Chapter 5 - Combinatorial Logic Analysis

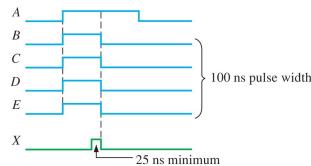
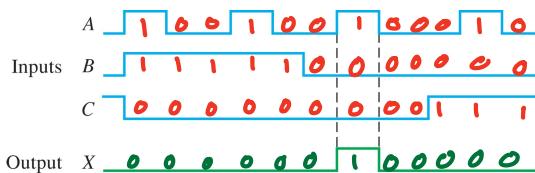
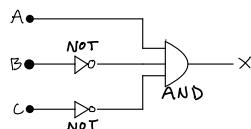


Figure 4: Diagrams for Sec. 5. (Left) Inputs are ABC, and the output is X. (Right) The inputs are ABCDE, and the output is X.

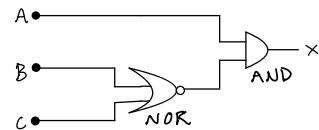
- For the input waveforms shown in Fig. 4 (left), what logic circuit will generate the output waveform?

$$X = A \bar{B} \bar{C}$$



$$X = A(\bar{B} + \bar{C})$$

or



- Bonus:** Assuming a propagation delay of 10 ns through each gate in Fig. 4, determine if the *desired* output waveform X will be generated. The desired output is a pulse with a minimum width of 25 ns.

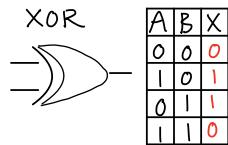
X will not be generated since the output pulse width would be greater than the desired output minimum pulse width ??

I got that the pulse width would be 90ns which is greater than the 25ns minimum.

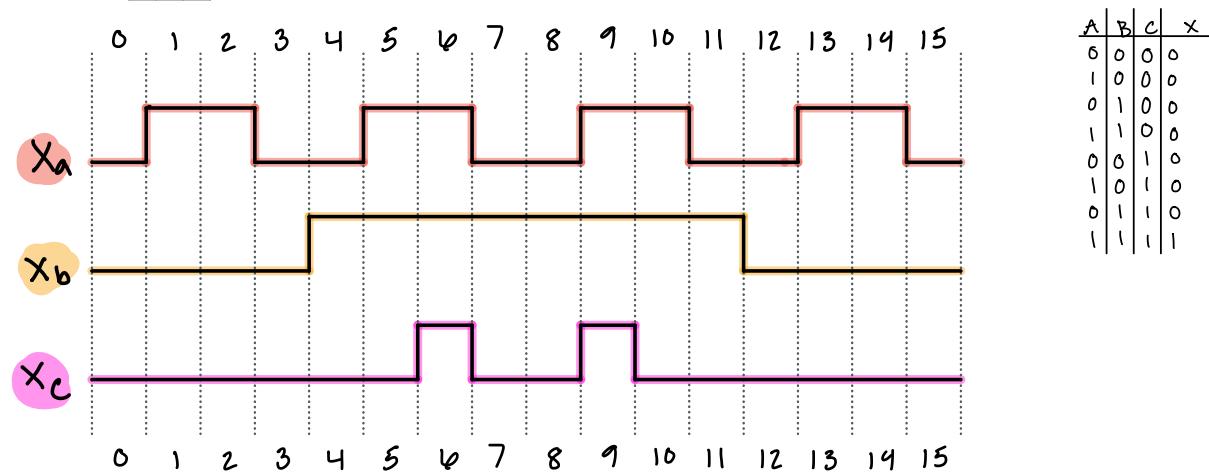
(See work on attached pages)

2)

a) Create timing diagram representing output of an XOR gate w/ D_0 and D_1 as inputs



b) do the same for D_2 and D_3



c) 3-input AND gate w/ x_a , x_b and EN signal as outputs

3) D_i reps parallel data w/ clock frequency

4 MHz

a) what is total bits per second?

$$f = 4 \times 10^6 \text{ Hz}$$

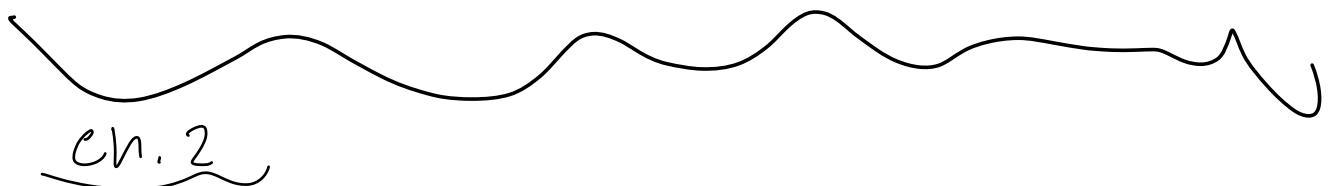
length of time:
 $0.25 \mu\text{s}(16) = 4 \mu\text{s}$

$$T = \frac{1}{4 \times 10^6 \text{ Hz}} = 0.25 \mu\text{s}$$

64 bits in $4 \mu\text{s} \Rightarrow$ 16 Megabits per second

b) if system was serial:

would take 4x as long
64 bits in 16μs \Rightarrow 4 Megabits per second



1) convert to binary

a) 1024

$$10000000000$$

$$\frac{1024}{2} = 512$$

$$\frac{512}{2} = 256$$

$$\frac{256}{2} = 128$$

$$\frac{128}{2} = 64$$

$$\frac{64}{2} = 32$$

$$\frac{32}{2} = 16$$

$$\frac{16}{2} = 8$$

$$\frac{8}{2} = 4$$

$$\frac{4}{2} = 2$$

$$\frac{2}{2} = 1$$

$$\frac{1}{2} = 0$$

b) 0xB BBBB

$$1011101110111011$$

$$B = 1011$$

$$BBBB = 1011101110111011$$

c) -2048

$$100000000000$$

$$\frac{2048}{2} = 1024$$

⋮

2) convert to hex

a) 65535

binary:

hex: FFFF

b)

$$1000 = 8$$

$$\Rightarrow 0x8888$$

many book
enjoy many figures

3. Design problem. Consider the angular shaft encoder in Fig. 2. The IR emitter/detector detects IR light reflected from white sectors, while the dark sectors absorb the light. The sectors are encoded in binary. For example, starting from inner sectors and reading outward, dark-dark-light is translated to state 001 by the detector. If the shaft rotates 45 degrees, the detector records a state change. (a) If the initial state is 000 and the shaft rotates 360 degrees, how many bit changes occur? (b) How many bit changes would occur if the shaft position was encoded in gray code? (c) Draw the correct face of the shaft encoder, encoded in 3-bit gray code instead of binary¹ (d) If 45 degrees is the angular precision with 3-bit gray code, what is the angular precision with 8 bit gray code?

- 1 indicated when there is a reflected beam
- 0 indicated when there is no reflected beam

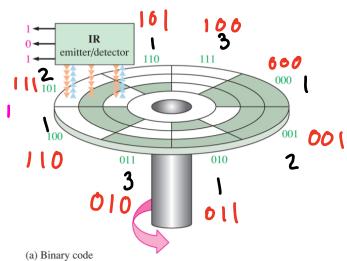


Figure 2: A gray code shaft encoder, or angular encoder, reports the angular position of an object digitally, using the gray code.

a) either 13 or
14 - but I think
14

b) 8

d) If 45° is the angular precision w/ 3-bit grey code, what is the angular precision w/ 8-bit grey code?

$$\frac{360^\circ}{8} = 45^\circ$$

$2^8 = 256$ sectors for 8-bit gray code

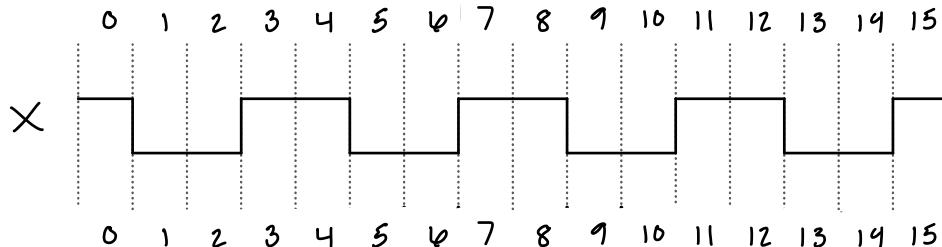
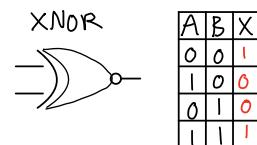
$$\frac{360^\circ}{256 \text{ sectors}} = \underbrace{1.4^\circ}_{??}$$

what?? 

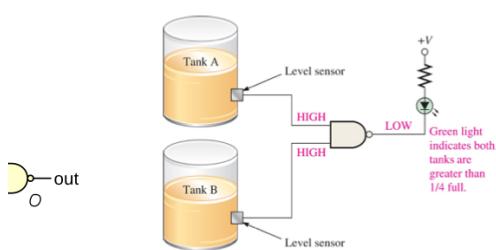
ch 3 :

2) Suppose signals D_0 and D_1

are connected to $a = b$ in figure
3 \Rightarrow XNOR gate. generate
the timing diagram



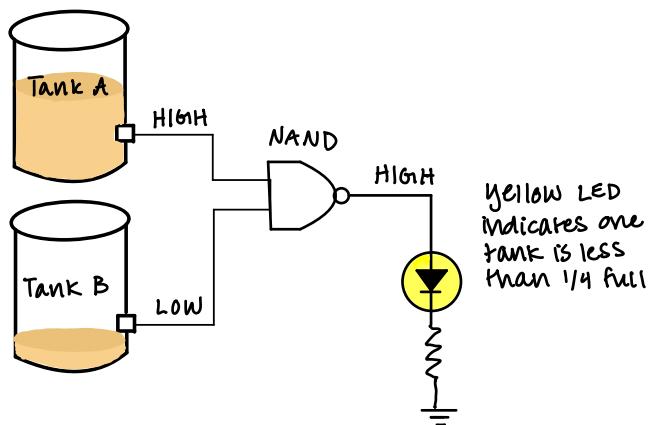
3. **Design problem.** A liquid tank system is depicted in Fig. 3 (right). The sensors are HIGH when the liquid is above the level. (a) Create and display a red LED system that activates when both tanks are *below* the level. (b) Create and display a yellow LED system that activates when one tank is below and one tank is above the level. (c) Add a third tank with two pipes guiding liquid to tanks A and B. Each pipe should have a valve. Add logic that opens the correct valve so as to fill only the low tank until it is no longer below the level.



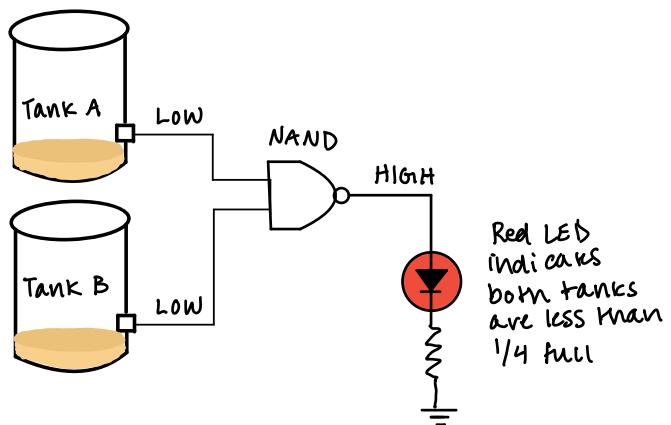
work on
next
page

(Right) A liquid tank-level system built from a NAND gate.

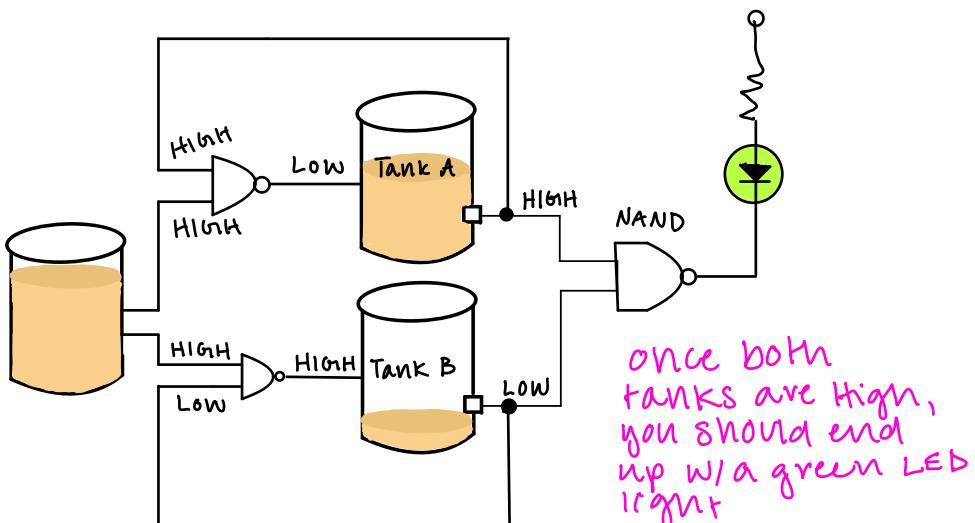
b)



a)



c)



Ch. 4

1)

$$ON = ABCD + \bar{A}\bar{B}CD + \bar{A}BC\bar{D} + A\bar{B}C\bar{D}$$

CD AB	00	01	11	10
00	OFF	OFF	ON	OFF
01	OFF	OFF	ON	OFF
11	OFF	OFF	ON	OFF
10	OFF	OFF	ON	OFF

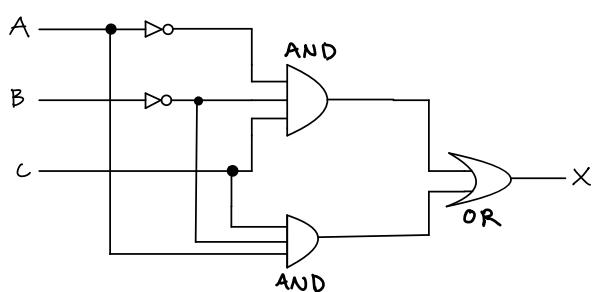
$$ON = CD$$

2. A circuit contains three main branches leading to one output. The output is observed to fail under the following conditions below. (a) Use the domain-3 Karnaugh map to determine the conditions under which it does succeed, and write an S-SOP expression for the circuit. (b) Draw the circuit using gates.

- A: false, B: false, C: false
- A: false, B: true, C: false
- A: true, B: true, C: false
- A: true, B: false, C: false
- A: false, B: true, C: true
- A: true, B: true, C: true

C AB	0	1
00	0	1
01	0	0
11	0	0
10	0	1

$$\{ X = \bar{A}\bar{B}C + A\bar{B}C \}$$



Ch. 5

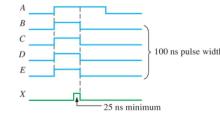
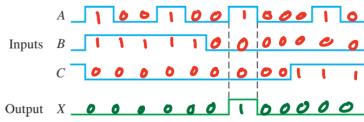
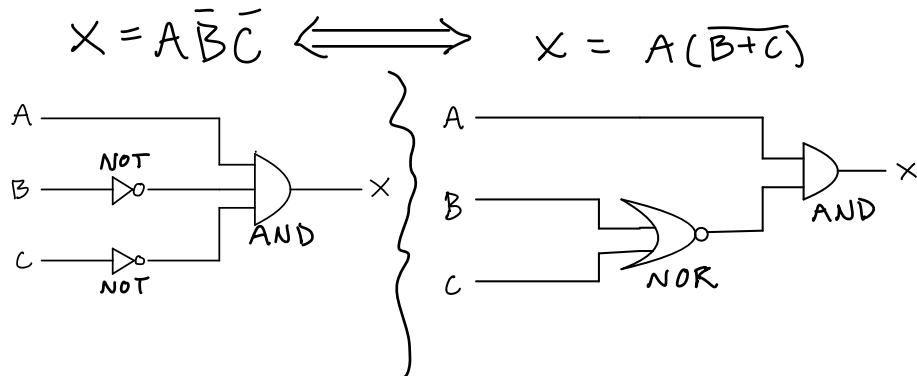


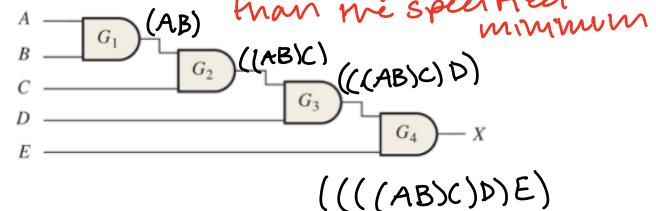
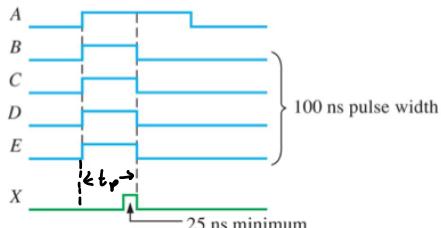
Figure 4: Diagrams for Sec. 5. (Left) Inputs are ABC, and the output is X. (Right) The inputs are ABCDE, and the output is X.

- For the input waveforms shown in Fig. 4 (left), what logic circuit will generate the output waveform?

A	B	C	X
1	1	0	0
0	1	0	0
1	0	0	1
1	0	1	0



- Bonus:** Assuming a propagation delay of 10 ns through each gate in Fig. 4, determine if the *desired* output waveform X will be generated. The desired output is a pulse with a minimum width of 25 ns.



$$X = ABCDE$$

$$t_w = 100 \text{ ns}$$

$$t_p = 10 \text{ ns}$$

propagation delay time : $t_p = 10 \text{ ns}$
time interval between transition of input pulse & the occurrence of the resulting transition of the output pulse

output pulse width would be
 $t_w - t_p = 100 \text{ ns} - 10 \text{ ns} = 90 \text{ ns}$ which is greater than the desired output waveform minimum