Homework 5 Solutions for Computer Logic and Circuit Design: PHYS306/COSC330

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1 6-2: Parallel Binary Adders

1. Exercise 4: $C_{out} = 1$, $\Sigma_3 = 1$, $\Sigma_2 = 0$, $\Sigma_1 = 0$.
2. Exercise 5: $\Sigma_6 = 1$, $\Sigma_5 = 1$, $\Sigma_4 = 1$, $\Sigma_3 = 0$, $\Sigma_2 = 0$, $\Sigma_1 = 0$.
3. Exercise 8: See Fig. 1.

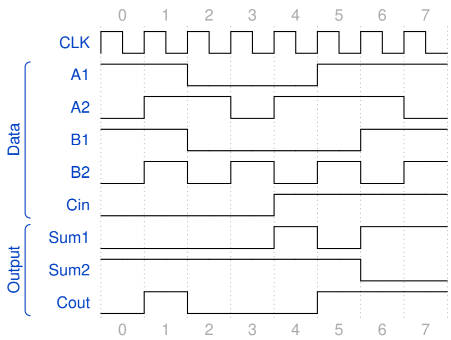

Figure 1: Solution to exercise 8.

2 6-3: Ripple-Carry Adders

1. Exercise 11: The first stage is limited by 40 ns delay between inputs and C_{out}. Then, each in-between stage is limited by the 25 ns delay between C_{in} and C_{out}. The exception is the last one, which is limited only by C_{in} to Σ. Thus, $40 + 6 * 25 + 35$ ns $= 225$ ns.

3 6-4: Comparators

1. Exercise 13: See Fig. 2.

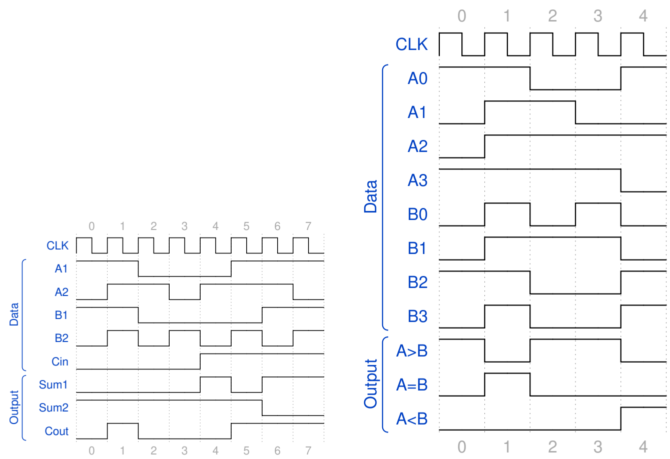

Figure 2: (Left) Solution to E xercise 13. (Right) Solution to Exercise 14.

2. Exercise 14: See Fig. 2.

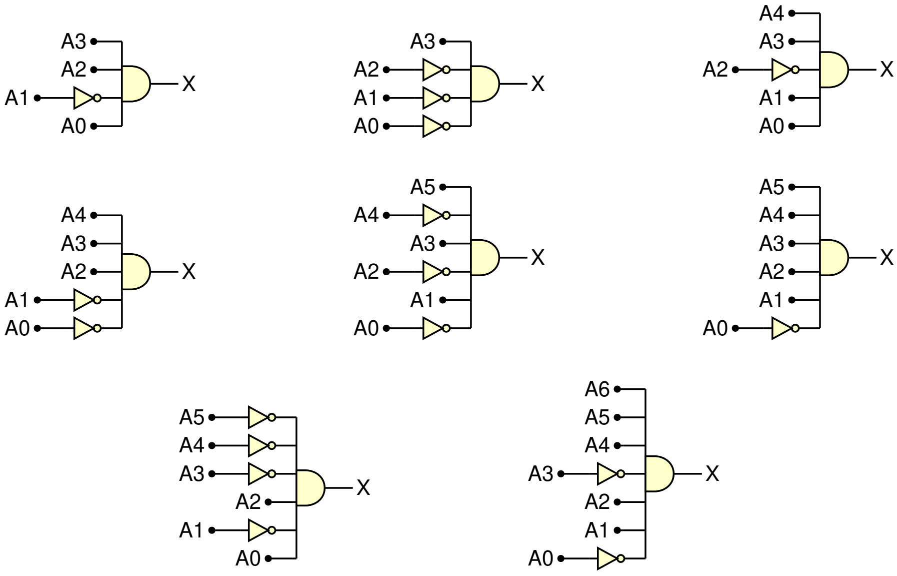

Figure 3: Solution to Exercise 17.

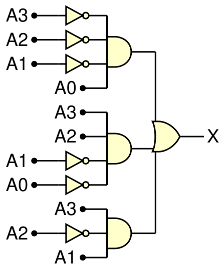

Figure 4: Solution to Exercise 19.

4 6-5: Decoders

1. Exercise 16: a) 1110 b) 1100 c) 1111 d) 1000
2. Exercise 17: See Fig. 3.
3. Exercise 19: Using the Karnaugh map, and the starting expression $X = A_3\bar{A}_2A_1\bar{A}_0 + A_3A_2\bar{A}_1\bar{A}_0 + \bar{A}_3\bar{A}_2\bar{A}_1A_0 + A_3\bar{A}_2A_1A_0$, we can show that the minimum logic is $X = \bar{A}_3\bar{A}_2\bar{A}_1A_0 + A_3A_2\bar{A}_1\bar{A}_0 + A_3\bar{A}_2A_1$. See Fig. 4.

5 6-6: Encoders

1. No, because the output would be $A_3A_2A_1A_0 = 1011$, or 11, which is not a valid BCD code.