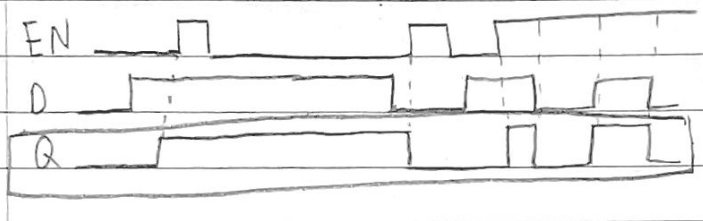
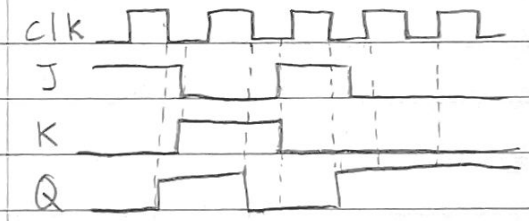
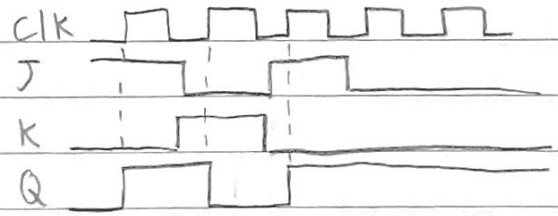
7. EN HIGH, D HIGH -> Q HIGH
EN HIGH, D LOW -> Q LOW
EN LOW -> No change



8.





The output of the negative edge-triggered clock is delayed by the clock pulse width.

12.