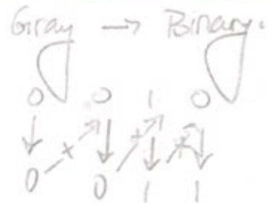

00	00
01	01
11	10
10	11

Midterm 2 for COSC330/PHYS306 - Fall 2021

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November 18, 2021

1 Chapter 6 - Functions of Combinational Logic

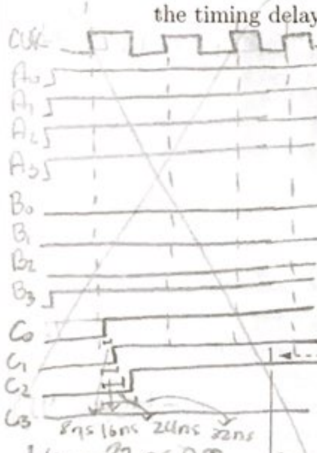
1. Consider Fig. 1, in which a 4-bit adder is depicted. Assuming a uniform worst-case delay of 8 ns from carry-in to carry-out for each stage, the total delay is 32 ns. (a) At what maximum frequency can this circuit perform additions, if the delay must be less than a clock period? (b) What would the result in (a) be if the adder was extended to 8 bits? (c) Create a timing diagram showing the addition of the numbers in Fig. 1. **Bonus:** include the timing delays, and indicate the clock period.

(a) $f = \frac{1}{32}$ GHz (b) $f = \frac{1}{64}$ GHz

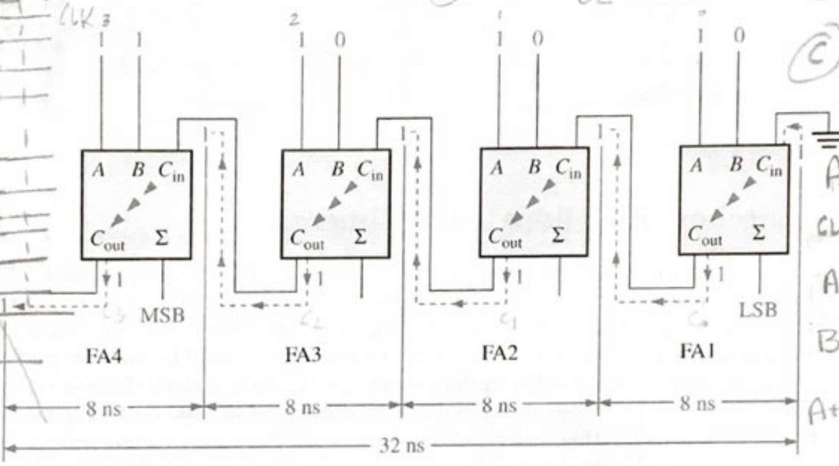
(c) $A = 1111$

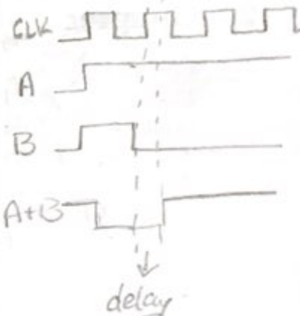
$B = 1000$

$A+B = 10111 = C$



$1/f = 32$ns per pulse



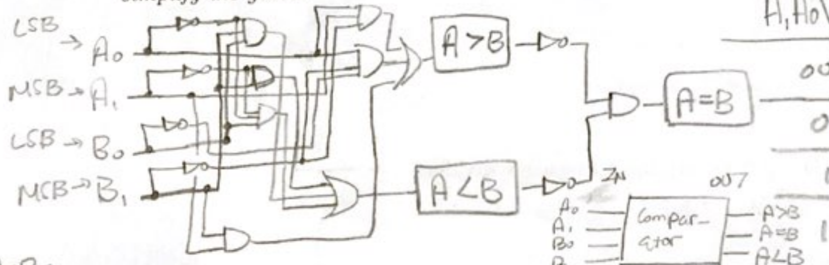


CLK period must be > 32ns ✓

Figure 1: A schematic of a 4-bit adder with delays marked in nanoseconds.

$A > B = A_1\overline{B_1} + A_0\overline{B_1}\overline{B_0} + A_1A_0\overline{B_0}$, $A < B = B_1\overline{A_1} + \overline{A_1}\overline{A_0}B_0 + B_1B_0\overline{A_0}$ $A = B = \overline{(A > B)}\,\overline{(A < B)}$

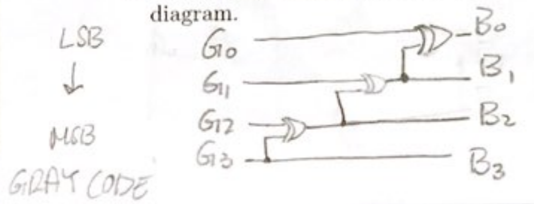
2. Using AND, OR, XNOR, and inverter gates, (a) create a 2-bit comparator that yields True if $A > B$, (b) True if $A = B$, and (c) True if $A < B$. For each circuit, assume both A and B are 2-bit binary positive numbers. (d) Wrap this all into one circuit with three outputs and 4 inputs. *Hint: use Karnaugh maps for parts (a)-(c) to simplify the gates.*

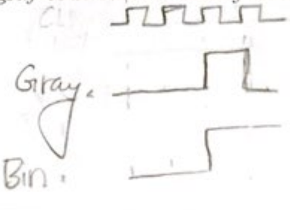


$A_1A_0 \backslash B_1B_0$	00	01	11	10
00	A=B	A<B	A<B	A<B
01	A>B	A=B	A<B	A<B
11	A>B	A>B	A=B	A>B
10	A>B	A>B	A<B	A=B

A=B:

3. Generate the logic gates that convert 4-bit gray code to 4-bit binary code, and show that it works with a timing diagram.

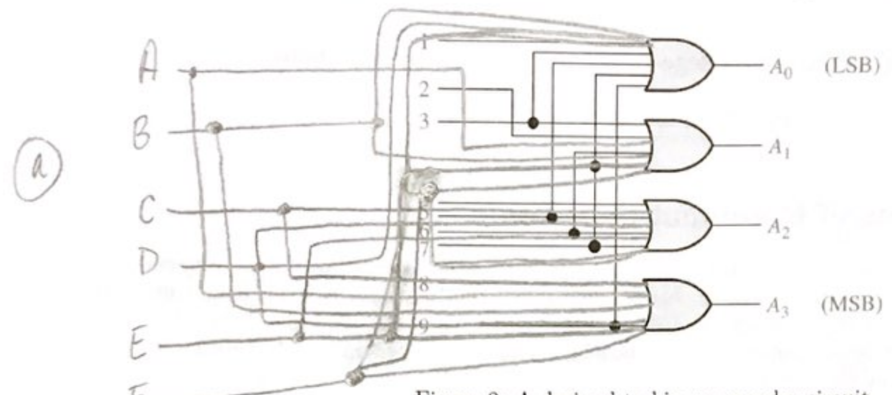




CLK
G_0
G_1
G_2
G_3
B_0
B_1
B_2
B_3

A = 10 = 1010	D = 13 = 1101	1 = 0001	4 = 0100	7 = 0111
B = 11 = 1011	E = 14 = 1110	2 = 0010	5 = 0101	8 = 1000
C = 12 = 1100	F = 15 = 1111	3 = 0011	6 = 0110	9 = 1001

4. Consider Fig. 2, in which a decimal to binary conversion circuit is shown. (a) Add logic to the circuit such that it becomes a hexadecimal to binary converter. (b) Draw a logic symbol for this circuit with the correct number of inputs and outputs. (c) Connect two hex-to-bin converters to a symbolic 2-to-1 multiplexer with the correct number of data select line(s) to form a system that can send two-digit hex numbers over one output line.



$A_0 = 1+3+5+7+9+B+D+F$

$A_1 = 2+3+6+7+A+B+E+F$

$A_2 = 4+5+6+7+C+D+E+F$

$A_3 = 8+9+A+B+C+D+E+F$

15 inputs → 4 outputs

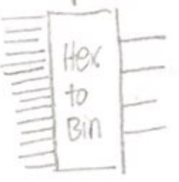
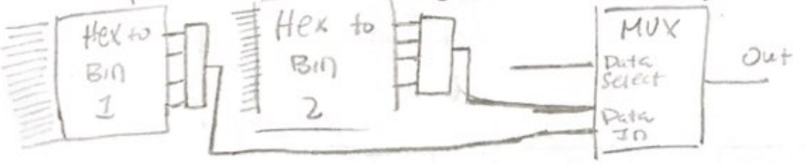
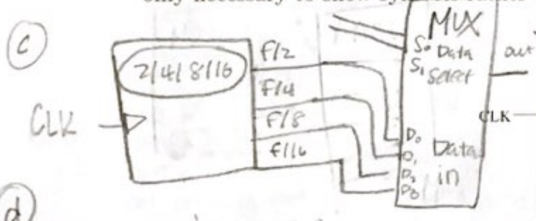


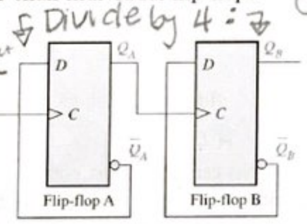
Figure 2: A decimal to binary encoder circuit.



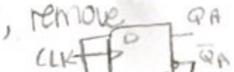
2 Chapter 7 - Latches, Flip-flops, and Timers

1. Consider Fig. 3, in which a divide-by-four frequency divider is depicted with D flip-flops and a CLK signal. (a) Elaborate on this circuit to create a circuit that can divide the clock frequency by 2, 4, or 8. Show the flip-flops explicitly. (b) Develop a symbol for the 2-4-8-16 divider, with CLK signal input and four ouputs (one each for $f/2$, $f/4$, $f/8$, and $f/16$ where f is the clock frequency). (c) Connect the symbol for the new part to a symbolic 4-to-1 multiplexer with the appropriate number of data select lines to form a clock division system. (d) Show with a timing diagram the output if the user changes the data select lines at least once. For parts (b)-(d), it is only necessary to show symbols rather than individual flip-flops.

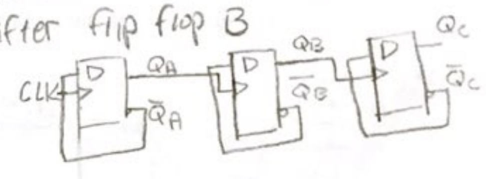


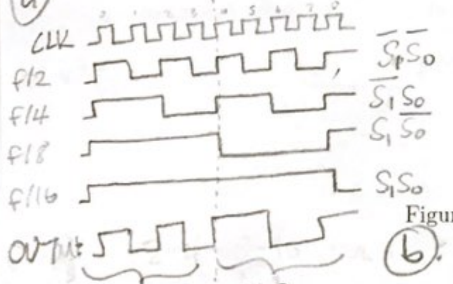


(a) To divide by 2, remove flip flop B.



To divide by 8, add an additional flip flop (C) after flip flop B





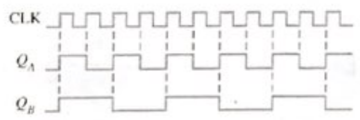
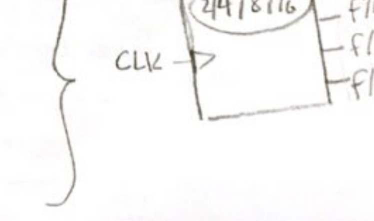


Figure 3: Two D flip-flops forming a frequency divider.

(b). (SYMBOL: 2/4/8/16)



$\bar{S_1}\bar{S_0}$ $\bar{S_1}S_0$

user data select

user changed data select from $\bar{S_1}\bar{S_0}$ to $\bar{S_1}S_0$ on clock pulse 4

3 Chapters 8 and 9 - Shift Registers and Counters

1. Consider the timing diagram in Fig. 4. Using any combination of *shift registers* and supporting gates, create a circuit with 8-outputs that produces this timing diagram.

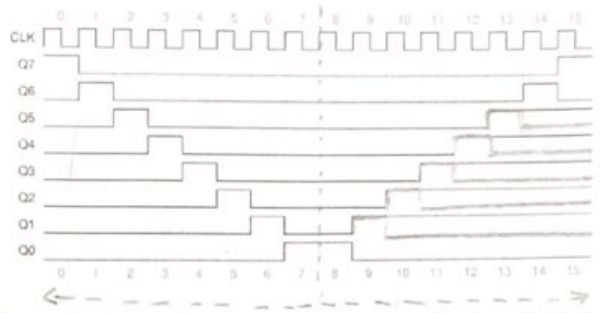
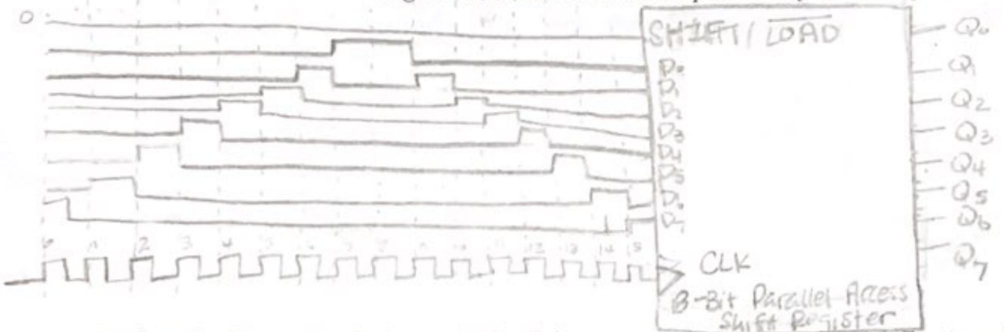


Figure 4: A waveform that repeats every 16 clock periods.



2. Consider Fig. 5, in which 4 and 5-bit Johnson counters are depicted. (a) Create a circuit based on Fig. 5 called a *combinatoric trigger*. Imagine four digital channels A, B, C, and D, as inputs. The output of the circuit should be True if *any two* of the four channels is True *within 100 ns of each other*. Develop any necessary logic symbols, and use the appropriate clock frequency. The Johnson counter(s) can have any number of bits.

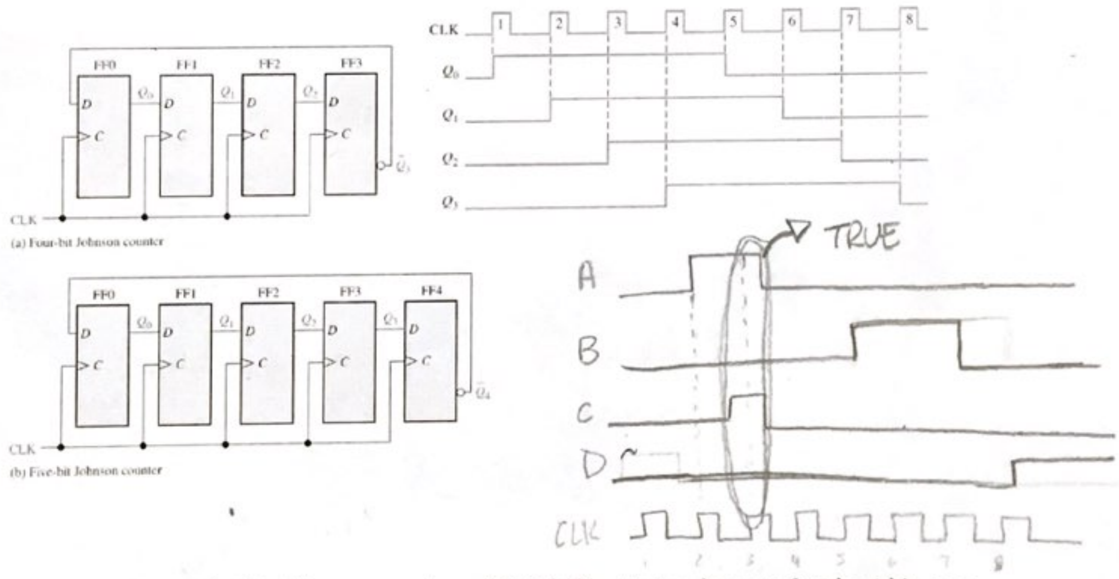
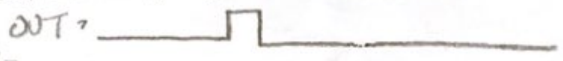


Figure 5: (Left) 4 and 5-bit Johnson counters. (Right) The timing diagram for the 4-bit case.



CLK frequency = $\frac{1}{100}$ GHz

(1 pulse per 100 ns)