Tuesday Reading Assessment: Chapter 8-1 through 8-4

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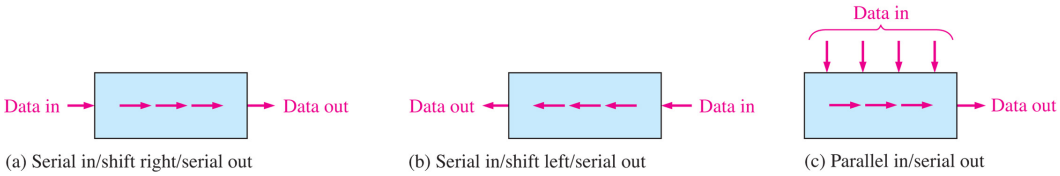

Figure 1: Topologies for 4-bit shift registers.

1 Shift Registers from D Flip-Flops

1. (a) Consider Fig. 1 (a), the 4-bit serial-in/serial-out shift register. If the initial input is a 1, followed by 0's only, how many clock cycles before the 1 reaches the output? Assume all flip-flops are initially reset. (b) If the clock frequency is 5 MHz, how long before the initial 1 reaches the output? (c) Consider Fig. 1 (c), the 4-bit parallel in/serial out shift register. If 4 1's are on the inputs initially, how many clock cycles will pass before a 1 appears one the output? (d) If the clock frequency is 2 MHz, how long before the first 1 appears on the output?

2. (a) Consider Fig. 2. Will the data bits D_i be loaded into the register when the SHIFT signal is LOW, or HIGH? (b) To shift data to the right, which two signals have to be activated, and with what values?

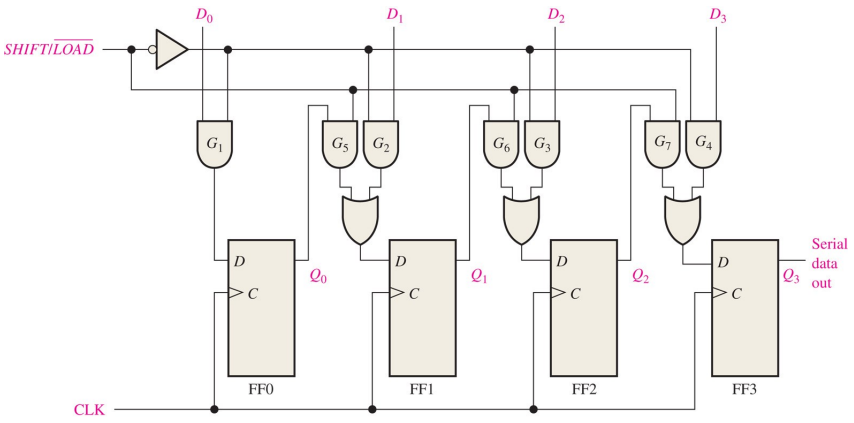

Figure 2: A 4-bit parallel-in/serial out shift register.