CH. 6

1) (a) $T = \frac{1}{F}$ $T = 32$ ns   (b) Delay = 8 ns per bit

32 ns $\cdot \frac{1}{F}$ 8 bits = 64 ns total delay

$f = \frac{1}{32 \text{ ns}}$ $f = \frac{1}{64 \text{ns}}$

$f = \frac{1}{32}$ GHz $f = \frac{1}{64}$ GHz

$\boxed{f = 0.03125 \text{ GHz}}$ $\boxed{f = 0.01563 \text{ GHz}}$

(c)

A

B

C_{in}

C_{out}

Σ

CLK

H
8 ns
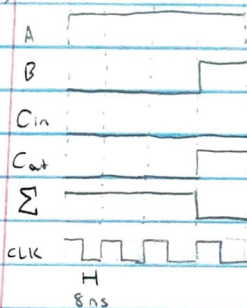
2)   Truth table for $A > B$, $A = B$, $A < B$

A_1	A_0	B_1	B_0	$A > B$	$A = B$	$A < B$
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

$A > B$

$x = A_1 \bar{B_1} + A_0 \bar{B_1} \bar{B_0} + A_1 A_0 \bar{B_0}$

$A = B$

$x = \bar{A_1} \bar{A_0} \bar{B_1} \bar{B_0} + \bar{A_1} A_0 \bar{B_1} B_0 + A_1 A_0 B_1 B_0 + A_1 \bar{A_0} B_1 \bar{B_0}$

$A < B$

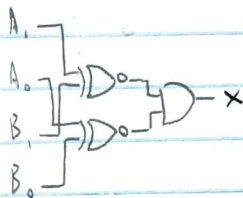$x = \bar{A_1} \bar{A_0} B_0 + \bar{A_1} B_1 + \bar{A_0} B_1 B_0$

(a) True when $A > B$

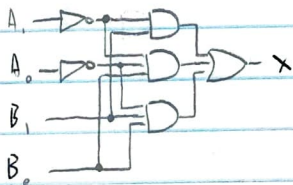$$x = A_1 \bar{B}_1 + A_0 \bar{B}_1 \bar{B}_0 + A_1 A_0 \bar{B}_0$$

(b) True when $A = B$

$$x = \bar{A}_1 \bar{A}_0 \bar{B}_1 \bar{A}_0 + \bar{A}_1 A_0 \bar{B}_1 B_0 + A_1 A_0 B_1 B_0 + A_1 \bar{A}_0 B_1 \bar{B}_0$$
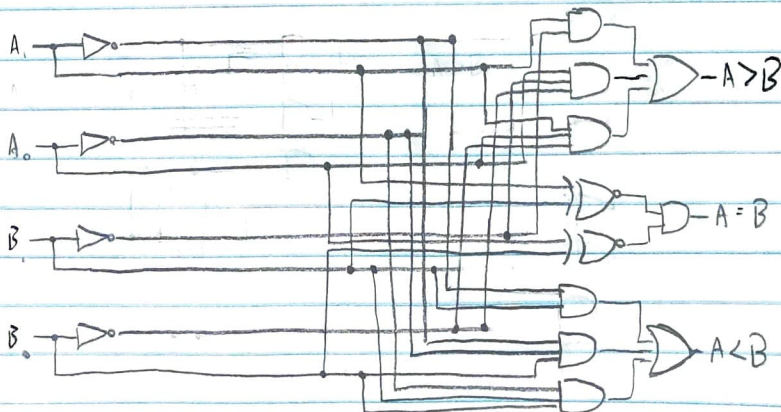

(c) True when $A < B$

$$x = \bar{A}_1 B_1 + \bar{A}_1 \bar{A}_0 B_0 + \bar{A}_0 B_1 B_0$$

(d)

3)

Binary	Gray
0 0 0 0	0 0 0 0
0 0 0 1	0 0 0 1
0 0 1 0	0 0 1 1
0 0 1 1	0 0 1 0
0 1 0 0	0 1 1 0
0 1 0 1	0 1 1 1
0 1 1 0	0 1 0 1
0 1 1 1	0 1 0 0
1 0 0 0	1 1 0 0
1 0 0 1	1 1 0 1
1 0 1 0	1 1 1 1
1 0 1 1	1 1 1 0
1 1 0 0	1 0 1 0
1 1 0 1	1 0 1 1
1 1 1 0	1 0 0 1
1 1 1 1	1 0 0 0

Binary: $A_0 B_0 C_0 D_0$ Gray: $A_1 B_1 C_1 D_1$

if $C_0 \neq D_0 \rightarrow D_1 = 1$
if $C_0 = D_0 \rightarrow D_1 = 0$ } XOR

if $B_0 \neq C_0 \rightarrow C_1 = 1$
if $B_0 = C_0 \rightarrow C_1 = 0$ } XOR

if $A_0 \neq B_0 \rightarrow B_1 = 1$
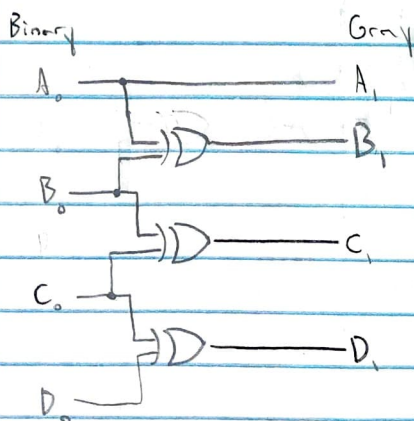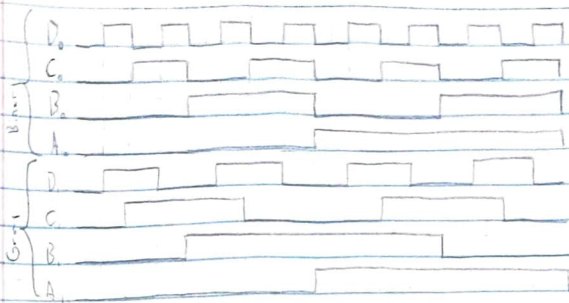if $A_0 = B_0 \rightarrow B_1 = 0$ } XOR

$A_0 = A_1$

$A_1 = A_0$

$B_1 = (A_0 \bar{B_0} + \bar{A_0} B_0)$

$C_1 = B_0 \bar{C_0} + \bar{B_0} C_0$

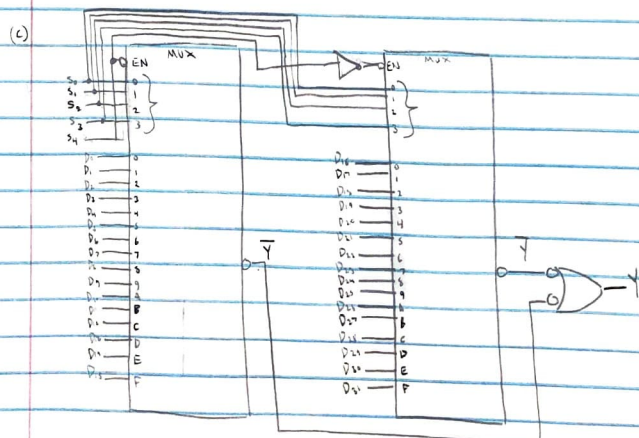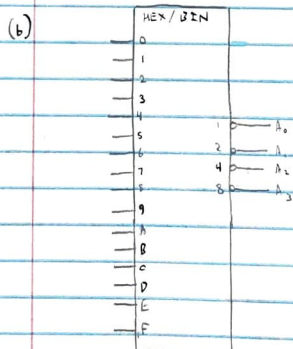$D_1 = C_0 \bar{D_0} + \bar{C_0} D_0$

Binary   Gray

A_0 ──────────────── A_1

B_1

Timing diagram on next page

B_0

C_1

C_0

D_1

D_0

4)

HEX	BINARY
	$A_3 A_2 A_1 A_0$
	0 0 0 1
2	0 0 1 0
3	0 0 1 1
4	0 1 0 0
5	0 1 0 1
6	0 1 1 0
7	0 1 1 1
8	1 0 0 0
9	1 0 0 1
A	1 0 1 0
B	1 0 1 1
C	1 1 0 0
D	1 1 0 1
E	1 1 1 0
F	1 1 1 1

$A_0 = 1 + 3 + 5 + 7 + 9 + B + D + F$

$A_1 = 2 + 3 + 6 + 7 + A + B + E + F$

$A_2 = 4 + 5 + 6 + 7 + C + D + E + F$

$A_3 = 8 + 9 + A + B + C + D + E + F$

(a)

(b)

(c)

(a & b)

Flip-Flop A   Flip-Flop B   Flip-Flop C   Flip-Flop D
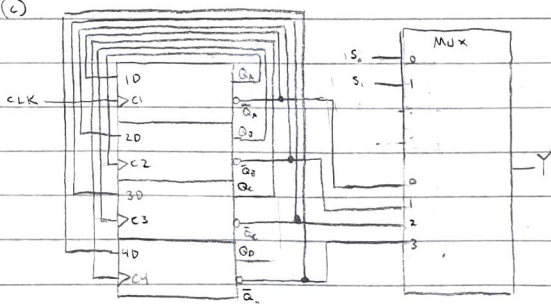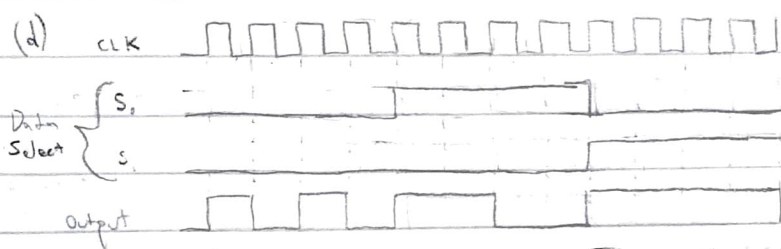
CLK
Q_A
Q_B
Q_C
Q_D

(c)

(d)

CLK

Data
Select

S₁

S

output
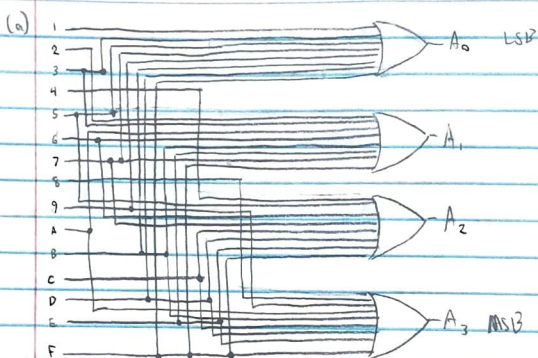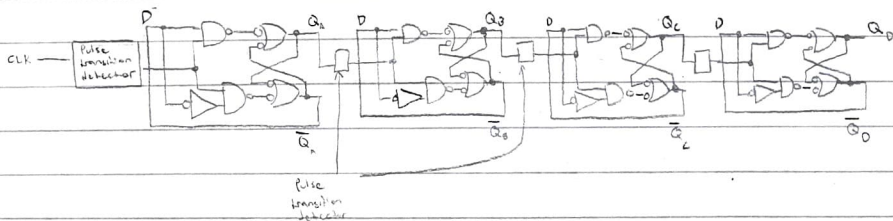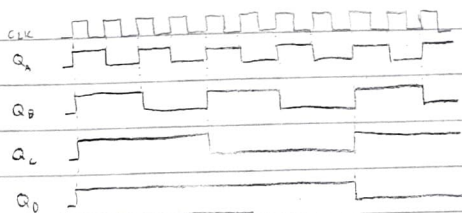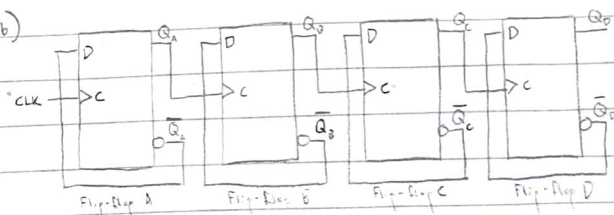
CH. 8 & 9

1) This is a bidirectional shift register that shifts the first half of the bits to the left and the second half to the right (assuming Q_0 is the beginning) and Q_1 is after the first shift.

RIGHT/
LEFT

Serial
Data in

CLK

Q_0 Q_1 Q_2 Q_3 Q_4 Q_5 Q_6 Q_7

2)

CLK
100 ns