Midterm 2 for Computer Logic and Circuit Design: PHYS306/COSC330

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This take-home midterm exam is open-note. It is due Monday, May 14th, 2018 in SLC 212 mail slot by end of the day.

1 Karnaugh maps and POS/SOP expressions

1. A remote weather station meant to alert residents of tornados appears to be malfunctioning. Four sensors pass data to a machine learning algorithm trained to send a FALSE signal when there is a tornado and remain TRUE otherwise. There is a temperature sensor, a windspeed sensor, a humidity sensor, and a barometer. There must be some electrical problem, because the system sends a FALSE with no tornado present under the following conditions. 1) The temperature sensor is powered, and the other sensors are off. 2) The temperature and barometer are powered, but the other sensors are off. 3) All sensors are off. 4) The barometer is powered, and the other sensors are off. Determine the simplest condition that leads to this erroneous FALSE signal when powering the sensors.

2. Suppose you remove the two sensors that are malfunctioning by causing the machine learning algorithm to report FALSE, indicating a tornado when there is none. Now, the machine learning system sends TRUE (correct, since there's no tornado around), when both sensors are powered. A replacement wind sensor is added. Later that month, a tornado approaches the area around the station. The wind, temperature and barometer sensors are activated remotely. The following conditions produce a FALSE machine learning output. 1) The temperature, wind and barometer sensors are powered, and 2) the temperature and wind sensors are powered while the barometer is not powered. Determine the simplest logic expression representing this state. Which device is malfunctioning?

2 Combinational logic with gates, tables, and expressions

1. Implement the logic circuit in Fig. 1 using only NAND gates. Draw a diagram and show that that the truth tables match.

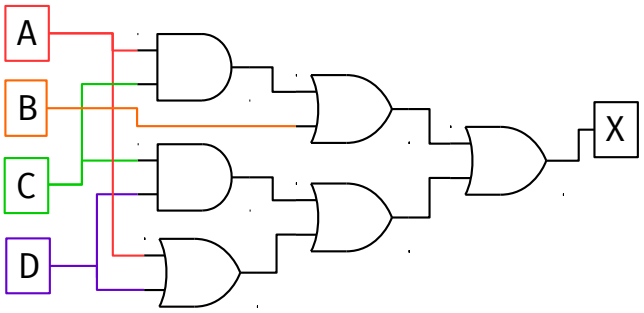

Figure 1: A combinatorial logic circuit.

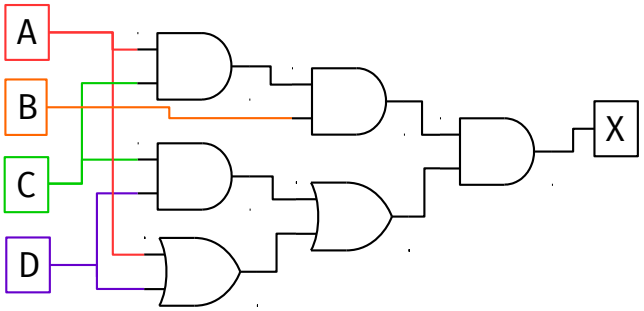

Figure 2: A combinatorial logic circuit.

2. Create a Karnaugh map for the fail conditions, and create a Karnaugh map for the succeed conditions. Express the corresponding Boolean expression to simplest POS or SOP form.

3. Implement the logic circuit in Fig. 2 using only NAND gates. Draw a diagram and show that that the truth tables match.

4. Create a Karnaugh map for the fail conditions, and create a Karnaugh map for the succeed conditions. Express the corresponding Boolean expression to simplest SOP or POS form.

3 Laboratory investigation of NAND and XOR gates

1. Design a 2 bit adder from DIP IC gates, using quad-NAND ICs only. Use any number of quad-NAND ICs, and indicate the meaning of each pin (NAND input or output).

2. Add LEDs to indicate the result of the addition. Provide a table of each possible input and output combination and show which LEDs would be **lit**.

4 Laboratory investigation of flip-flops

1. *Recall that counting in binary amounts to dividing the frequency of the last significant bit to get the frequency of the current bit.* Using D-type flip flops, create an 8 bit counter and provide a timing diagram, including a clock and each output pin.

2. *A data **latch*** is a usage of a flip-flop that remembers a bit of data for at least one clock cycle. A row of n flip-flops can form an n-bit latch if they are clocked at the same time. Using the type of counter in the previous problem, create a latch that remembers a 4-bit number for 8 clock cycles.[1]

[1] Feel free to design a block called *counter* and use it as necessary. Also, feel free to use single logic gates for convenience.

5 Laboratory investigation of counters

1. Suppose we have a 16-bit counter clocked at 2 MHz. Assuming it is enabled and cleared at $t = 0$, what is the output of each pin after 617 μs? [2]

[2] *Think about how many clock cycles this is.* What's the binary number?