Two Stage Operational Transconductance Amplifier Design

Project Report

Submitted in partial fulfillment of requirements of the course EL-GY 6403 Fundamentals of Analog Integrated Circuit Design under guidance of

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1. Specifications and Background:

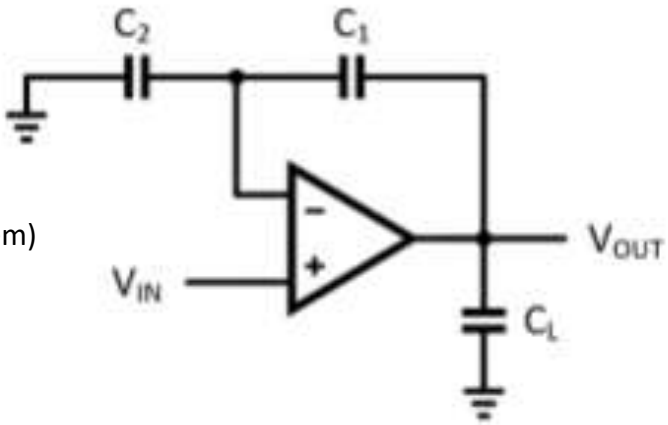

Fig 1: Given Amplifier Schematic

The given design requirements are as follows:

- $A_{CL}(s) = 2$ (in-band gain for the closed-loop system)

- ω_{-3dB} (upper bandwidth limit for the closed-loop system)

  $= 2\pi * 15 * 10^6$ rad/s

- Slew Rate = 30 V/µs

- PM > 70°

- C_L = 2 pF (load of the closed-loop system)

- $C_1 = C_2$ = 2 pF

The implementation of a CMOS OPAMP that combines a considerable dc gain with a high unity gain frequency is a challenge. The approach to this design has been by hand calculating and evaluating the deduced equations from the behavioral characteristics of NMOS and PMOS transistors followed by simulations using Cadence.

As per the given constraints for the circuit to be designed, it is supposed to be designed for a feedback factor $\beta = C_1/(C_1+C_{2)} = 1/2$. To achieve a closed loop gain of $A_{CL} = 2$ with the given β factor the circuit is supposed to have a very high open loop gain of the order of approximately $10^2 \sim 10^6$or higher.

High gain being a major requirement of the system a two stage Operational Transconductance Amplifier (OTA) topology, which offers many advantages over its counter parts, has been chosen for the design.

For a closed loop system the upper bandwidth limit is multiplied by the feedback factor, i.e., Unity Gain Bandwidth Product (GBW) = feedback factor (β) * ω_{-3dB}(given)

Hence, GBW = 2*2*pi*15*10^6.

To meet the requirements of Phase Margin (PM) and stability for the circuit, the concept of Pole splitting was incorporated in the design using a compensation capacitor C_C between first and second stages of the amplifier.

Process parameters like μC_{ox}, V_{th}, Input common mode ranges (ICMR min and max) for both NMOS and PMOS transistors were determined by pre-design simulations.

2. Existing Optimized Solutions:

To design a two stage operational amplifier various approaches are available which can be studied or chosen based on the requirements/constraints of the application. Few of the following methods that caught our attention can be used to optimize the design after following the standard hand calculation approach:

A. Nulling Resistor Approach

A two stage OTA has a Right Hand Plane (RHP) zero in its transfer function which harms the Phase Margin and thus the stability of the system. Adding a resistance R_c in series with the compensation capacitor C_c can help improve Phase Margin of the design. The value of R_c is usually decided by the transconductance of the input transistor of the second stage $gm_{in,2}$.

- For a value $R_C = 1/gm_{in,2}$ removes the RHP zero effectively.
- For $R_c > 1/gm_{in,2}$ pushes the RHP zero to a higher frequency.
- R_c can also be tuned to cancel the non-dominant pole of the system and thus stabilize it.

An optimized approach considering the different design trade-offs of Nulling resistor can result in an improved Gain Bandwidth Product (GBW).

B. Voltage Buffer Approach

In this approach a Common Drain stage along with the compensation capacitor C_c is usually employed to break the forward path. The output of the first stage is given as input to the source of this stage via C_c and the output of the whole system is taken from the gate of this stage. This buffer stage introduces a Left half plane Zero which can be tuned to compensate with the 2^{nd} pole of the system. This approach works similar to the Nulling resistor approach; however it greatly reduces the output swing barring its use in many applications.

C. Current Buffer Approach

This method employs a common gate stage, receiving the output of the first stage at its drain as the input and gives out the output via C_C. at source. In this case the open loop gain is characterized by a dominant pole, a zero and two complex conjugate poles which on tuning and considering the necessary tradeoffs help optimizing the GBW. Unlike the voltage buffer approach it preserves the output swing.

3. Justifications for designed architecture:

A. Choice of Topology:

Performing standard hand calculations and simulations over a single stage amplifier [Reference Fig 6,7], gave us an insight over the fact that maintaining a good swing and achieving high gain at the same time using a single stage is not easy. Thus design of a two stage amplifier was decided upon to meet the gain and swing requirements.

Telescopic topology has limited output swing. It cannot be used as a unity gain buffer, i.e., we cannot short the output to the input as it may drive one of the cascode transistors into triode region due to limited V_{in} range. Also the analysis of a telescopic topology suggests that it has a medium gain.

As far a unity gain buffer and output swing limitations go, a Folded Cascode can be used more effectively instead of the telescopic topology. But Folded cascode consumes higher power due to additional current sources needed for biasing of the transistors. Also we only achieve a slightly higher gain as compared to telescopic topology but at the cost of more power consumption.

An Operational Transconductance Amplifier (OTA), has higher gain and better output swing as compared to its counter parts, *viz*, Telescopic and Folded Cascode topology. Also it can be used as a unity gain amplifier. Thus a two Stage OTA topology was selected for this design.

B. Schematic:

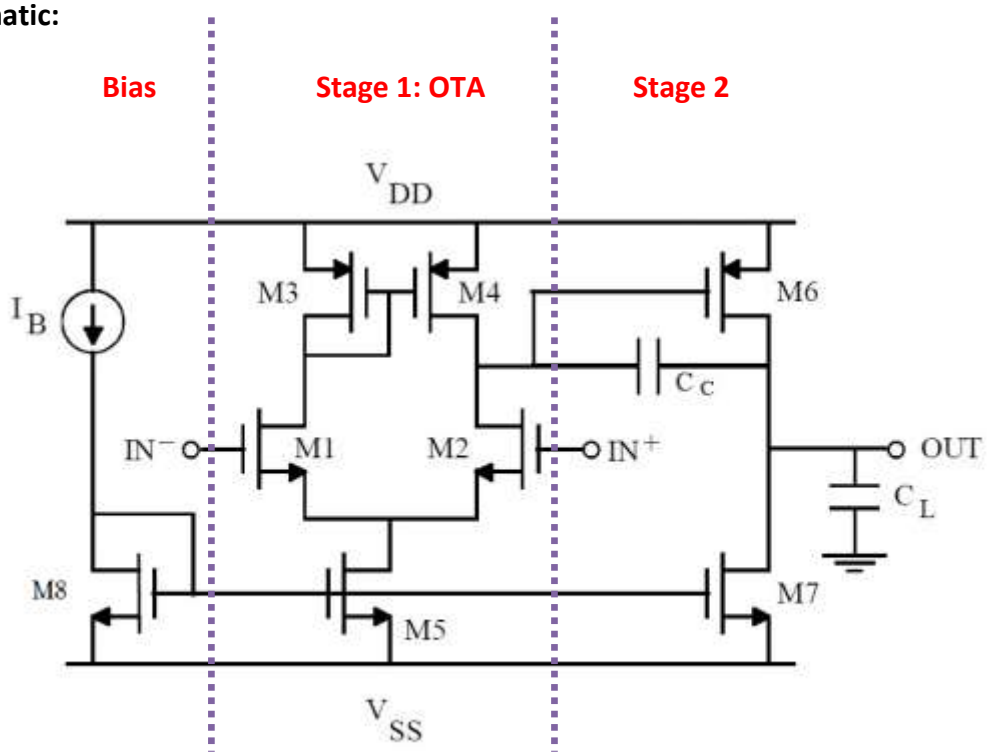

Fig 2: Schematic

M1-M2 => Input MOS (Stage 1)

M3-M4 => mirrors output of M1 to output of M1 to make circuit have single ended differential output

M5 => MOS used as current source for biasing of M1-M2

M6-M7 => CS Amplifier (Stage 2)

M8 and I_B => Provide bias for the current source loads M5 and M7

- Stage 1 is a differential amplifier with single ended output. For Stage2 we use a PMOS (M6) for higher swing and M7 is the current source load for M6.
- C_C is the compensation capacitor for effective pole splitting. It is a feedback from output to input in the second stage.

C. Small Signal Model:

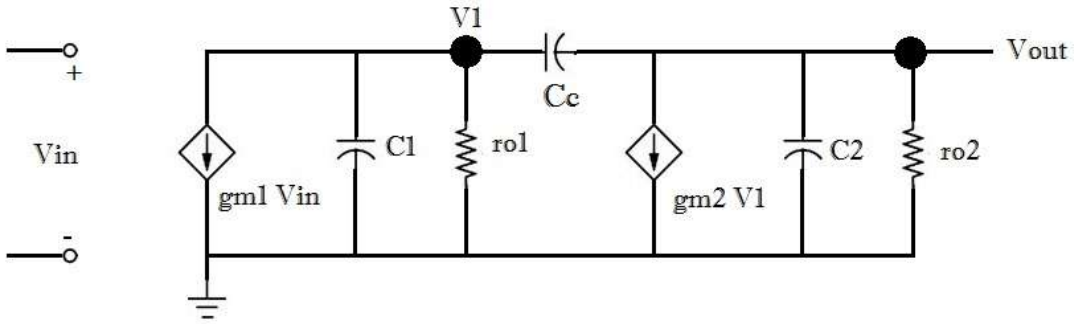

Fig 3: Small signal model for 2 stage OTA

[Stage 1 parameters are denoted by subscript 1, Stage2 parameters are denoted by subscript 2]

- C1 represents parasitic capacitances by $C_{GS,}$ C_{DS4} and C_{DS2}. C2 is dominated by load capacitance C_L and hence other parasitic capacitances around C_2 can be ignored. 'ro1' and 'ro2' are represented here as output resistances of the Stage 1 and Stage 2 respectively.
- With each stage we introduce a pole in the system. Thus our circuit is a 2 pole system.

4. Design Approach:

Analysis of the circuit:

Considering the Small signal model in Fig 3,

The general equation for a 2 pole system is given as:

$$\frac{V_0}{V_{in}} = \frac{A_{DC}(1-s/z)}{(1+s/p_1)(1+s/p_2)} = \frac{A_{DC}(1-s/z)}{1+s(1/p_1+1/p_2)+s^2(1/p_1p_2)}$$

Considering P_1 to be the dominant pole

$$\boxed{P_1 = \frac{1}{R_2(C_2+C_c)+R_1(C_1+C_c)+gm_2R_2R_1C_c} \approx \frac{1}{gm_2R_2R_1C_c}}$$

$$P_1P_2 = \frac{1}{R_1R_2(C_1C_2+C_1C_c+C_2C_c)} \qquad \boxed{\therefore p_2 = \frac{gm_2}{C_2}}$$

$$z = \frac{gm_2}{C_c} \qquad \therefore A_{DC} = gm_1 R_1 gm_2 R_2 \qquad GBW = A_{DC} \times P_1 = \frac{gm_1}{C_c} \qquad SR = I_5 / C_c$$

$$\angle V_o / V_{in} = -\tan^{-1}(\omega / z) - \tan^{-1}(\omega / P_1) - \tan^{-1}(\omega / P_2)$$

Considering $\omega = GBW$ and minimum value of $z \geq 10 \times GBW$

$$\angle V_o / V_{in} = -\tan^{-1}(1/10) - \tan^{-1}(A_{DC}) - \tan^{-1}(GBW / P_2)$$

Now, for a single pole system, the value of $\tan^{-1}(A_{DC})$ nearly equal to 90^o and

$$\angle V_o / V_{in} = -180 + PM$$

Thus for a PM of around 80^o and making a design assumption of $gm_2 \tilde{} 10 * gm_1$

We get,

- $C_C = 3pF$
- I_B = Slew Rate (SR) * C_C = 90 μA

Manipulating above given equations and values along with

- $I_D = \mu C_{ox} * W * (V_{gs}-V_{th})^2/2*L$
- $gm = 2* I_D /(V_{gs}-V_{th})$

We deduce aspect ratios for our transistors.
Value of V_{DD} was chosen to be 3V since we expected and derived high aspect ratios and I_B for our transistors.

Pre-Design Test 1: Diode connected NMOS and PMOS are supplied with 50 μA of current and then $\mu_n C_{ox}$ and $\mu_p C_{ox}$ is calculated using Cadence. [Refer Fig 4]

Pre-Design Test 2: To determine Input common mode range (ICMR), the test bench for the two stage amplifier is constructed on cadence and with a common mode input given to both the input terminals, the region for which all transistors work as per requirement is found out. [Refer Fig 5]

Design Tests: Iterate for (W/L) ratios for various transistors by observing circuit's behavior over a range of frequencies.

5. Simulations:

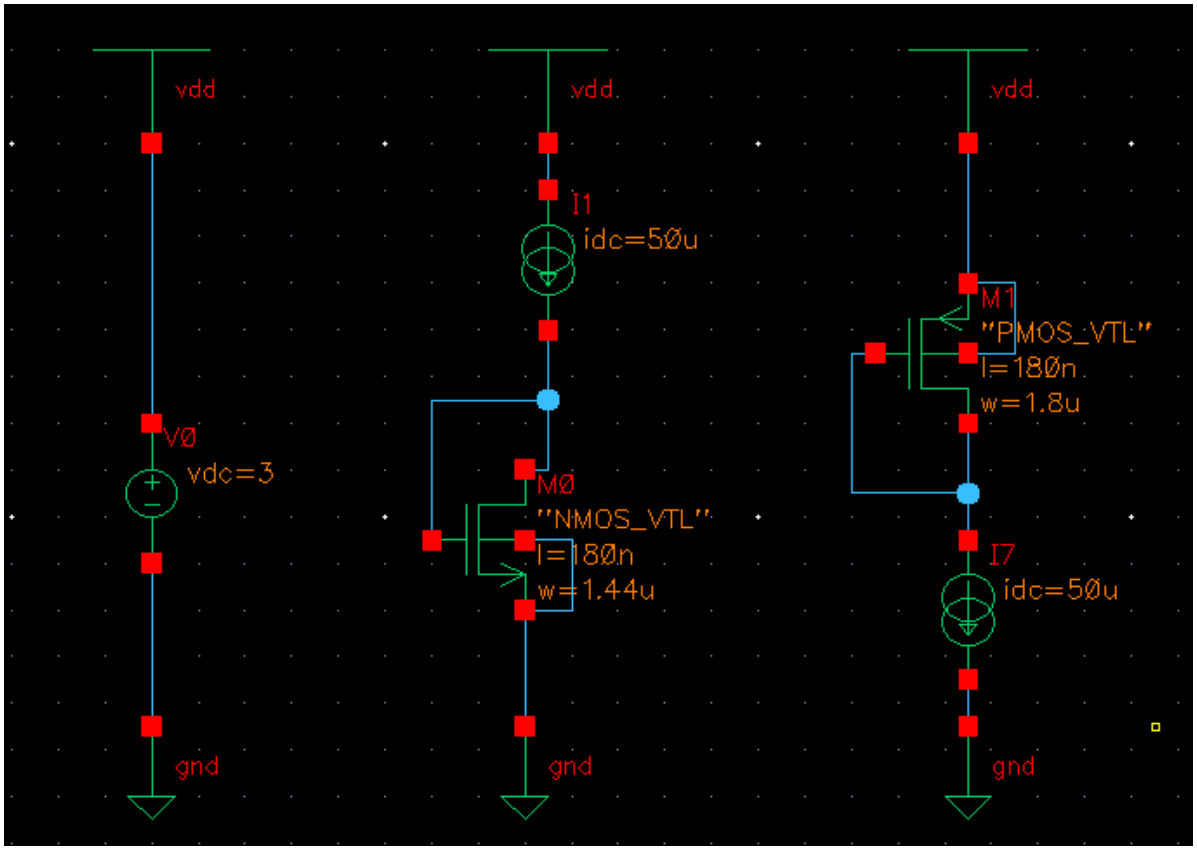

Fig 4: Pre-Design Test 1:

Fig 5: Output: Pre-Design Test 2

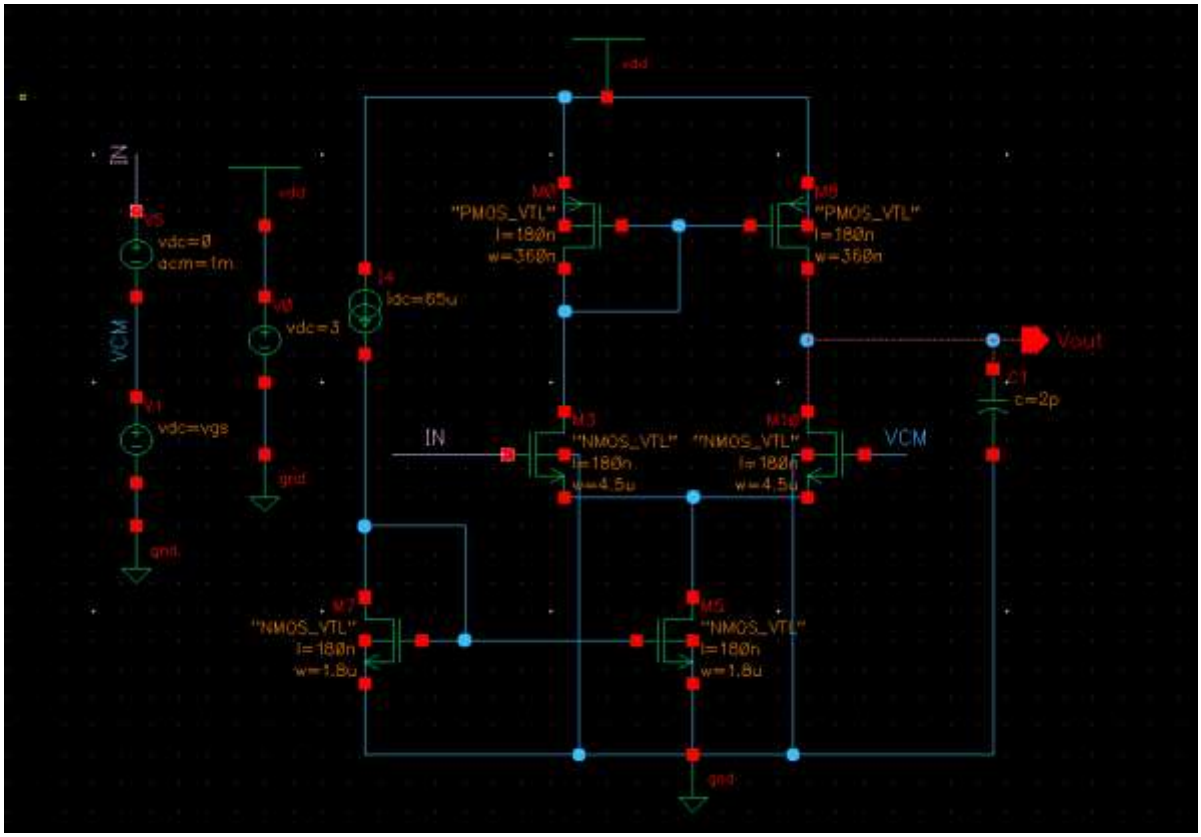

Fig 6: Design of single stage OTA

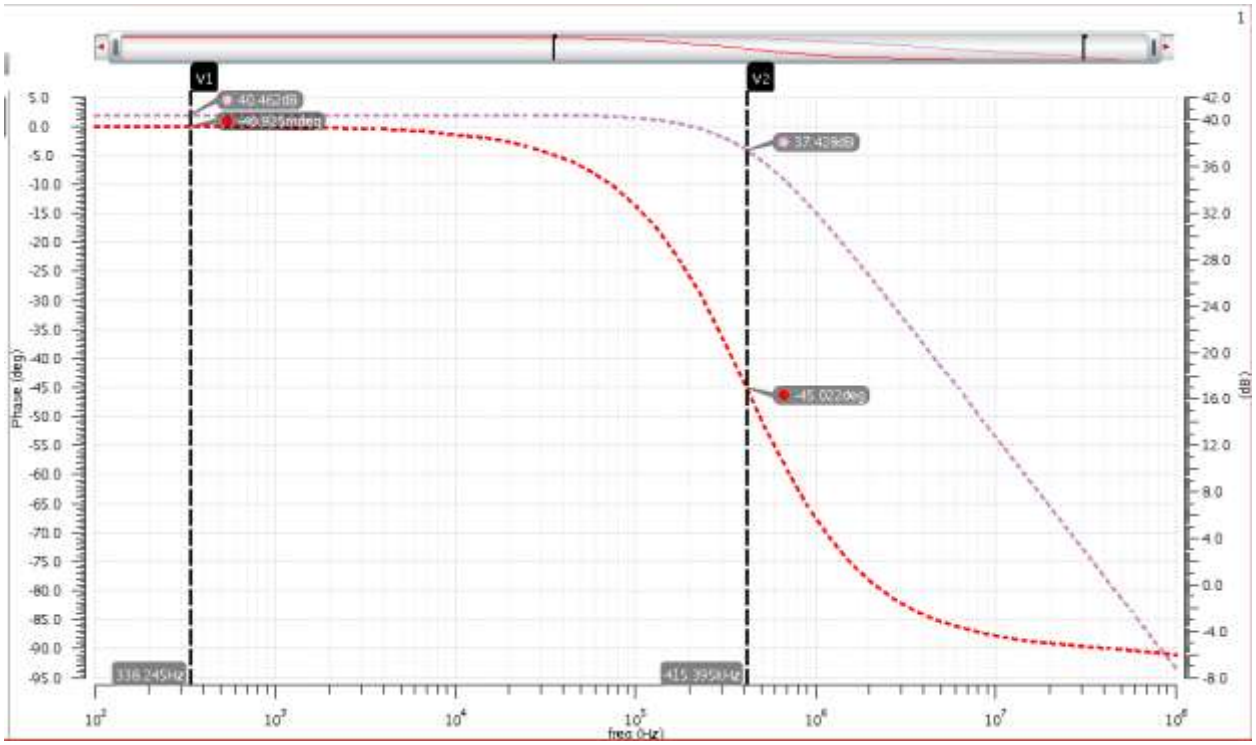

Fig 7: Gain and Phase for Single stage OTA

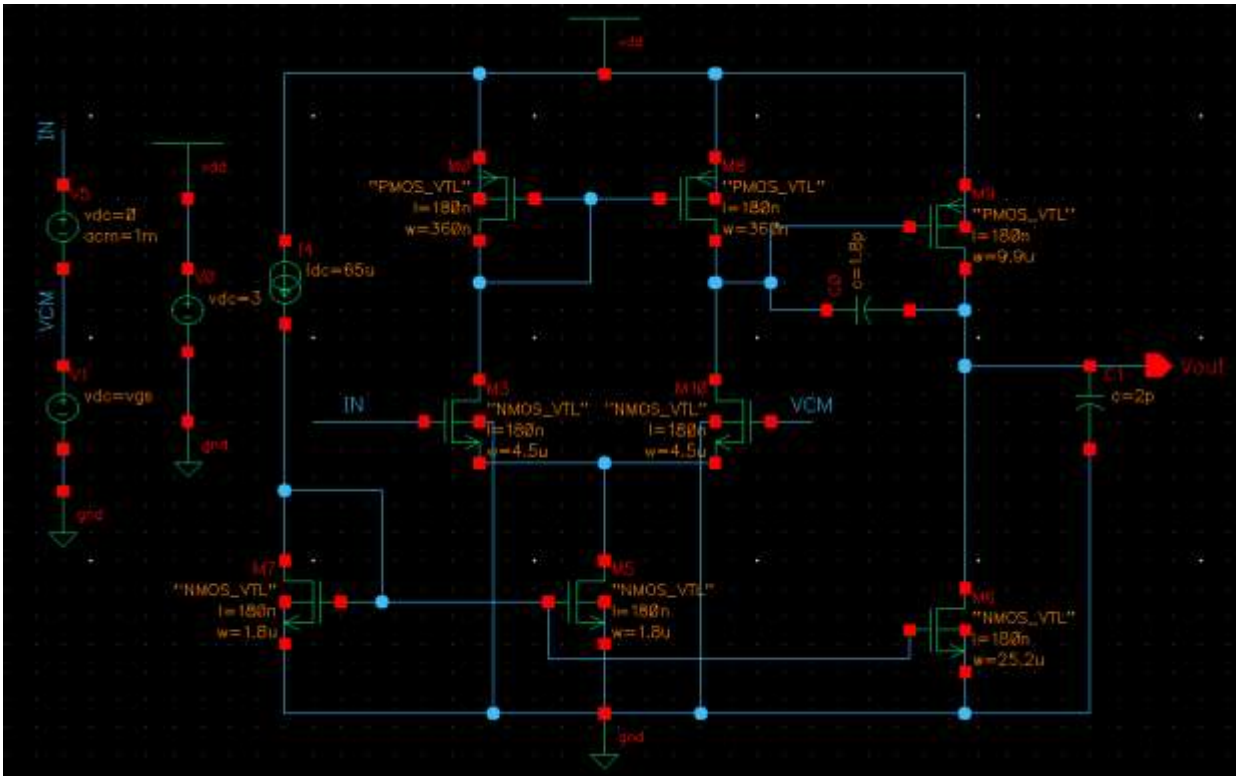

Fig 8: Designed two stage OTA

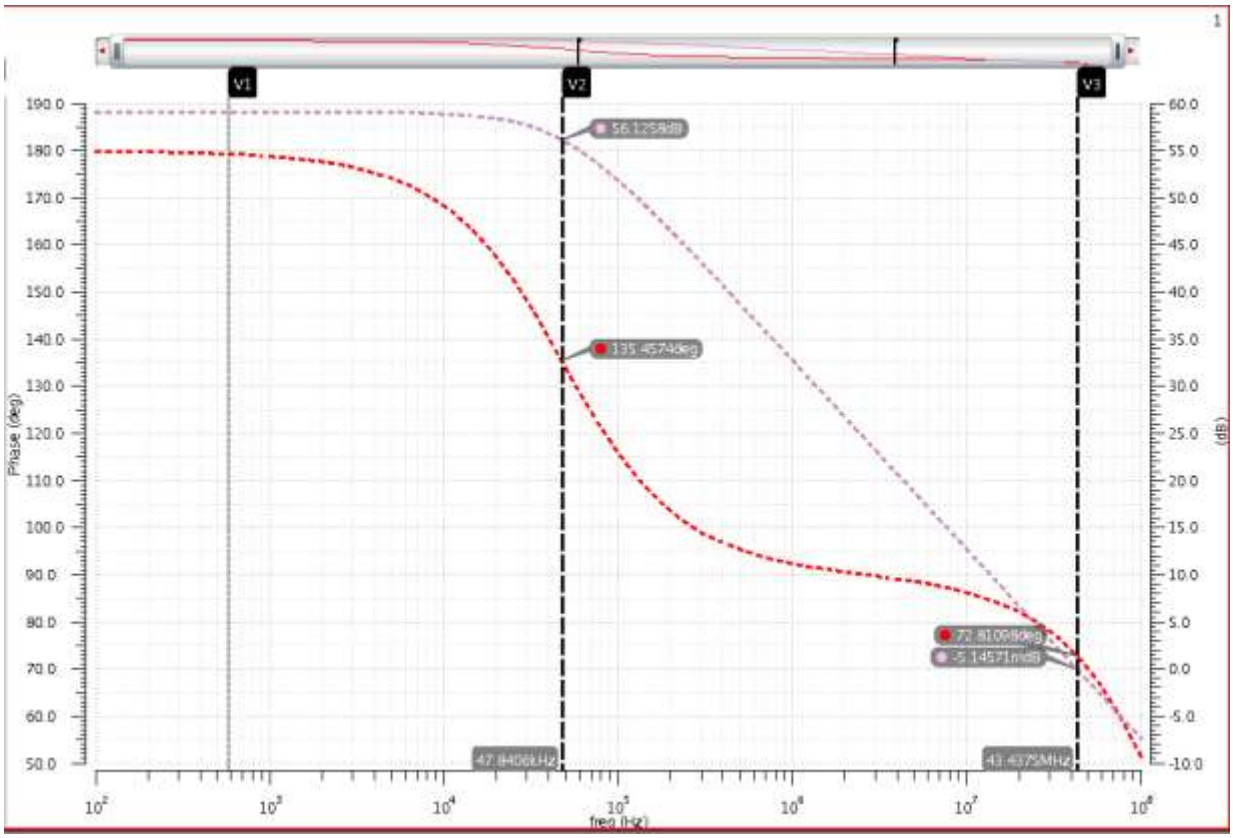

Fig 9: Gain and Phase for two stage OTA

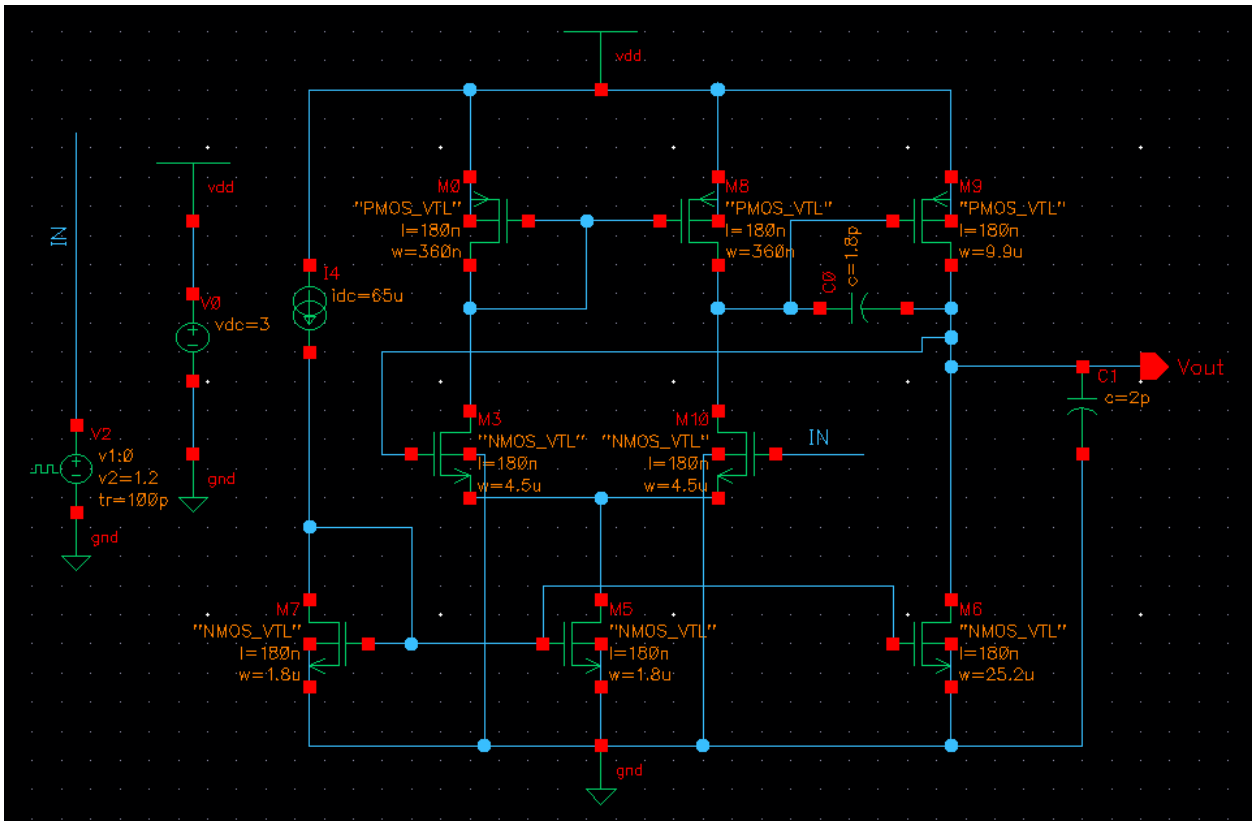

Fig 10: Circuit to calculate Slew Rate

Slew Rate

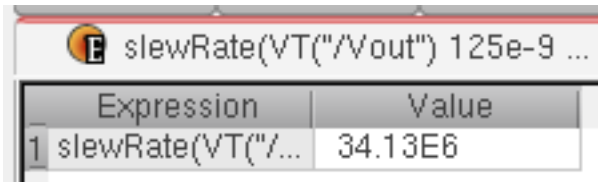

Fig 11: Calculated Slew Rate value

6. Observations:

Pre-Design Test1: To find μC_{ox} and V_{th} for NMOS and PMOS at I_B = 50µA

W/L	$\mu_n C_{ox}$	$\mu_p C_{ox}$
1	500 µA/V	141 µA/V
3/2	551 µA/V	160 µA/V
5	683 µA/V	210 µA/V
8	815 µA/V	260 µA/V

- Threshold voltage values deduced for NMOS and PMOS are V_{thn} = 0.322V and V_{thp} = -0.302V respectively. They are obtained by saving operating point of the MOS, by including a script 'save M0:oppoint' for each MOS in the model libraries.

Pre-Design Test2: To determine Input Common Mode Range [Refer Fig 5]

- Set V_{DD} = 3V, use the designed schematic for a two stage OTA with a difference that a common mode signal (V_{gs}) is given as input to both the terminals and is sweeped from 0V-3V. All transistors remain in saturation for a common mode input voltage range (ICMR) of 1V to 2.9V

Design Tests: To determine aspect ratios, compensation capacitor and current bias for the designed circuit [Refer Fig 8-11]

Variable Parameters								Output Parameters				
$(W/L)_{1,2}$	$(W/L)_{3,4}$	$(W/L)_{5,8}$	$(W/L)_6$	$(W/L)_7$	L [nm]	C_C [pF]	I_B [µA]	Gain [dB]	PM [degree]	GBW_{0dB} [MHz]	GBW_{-3dB} [MHz]	SR V/µS
5	1.5	10	50	170	500	3	90	53.66	84	8.329	9.89	25.91
5	1.5	10	50	170	180	3	90	55.6	82.52	15	10.67	26.58
5	2	10	55	140	180	3	90	57.27	82.43	15.63	10.8	26.96
5	2.5	10	60	120	180	3	90	56.78	82.76	15.34	10.98	27.4
5	2	10	55	140	180	1.35	90	57.3	78.6	34.19	24.07	61.31
5	2	10	55	140	180	1.6	65	58.9	80.26	25.84	18.2	31.9
15	2	10	55	140	180	2	65	59.76	75.9	33.68	23.7	30.54
25	2	10	55	140	180	1.8	65	59.1	72.8	43.26	30.6	34.13

****Fields in RED denote final selected values**

7. Deductions:

For Pre Design Test 1, the final approximate value chosen for μC_{ox} was for an aspect ratio of W/L = 8, as this aspect ratio is in range with calculated aspect ratios for transistors in the circuit.

Thus: $\mu_n C_{ox} = 815\mu A/V$; $\mu_p C_{ox} = 260\mu A/V$

and $V_{thn} = 0.322V$; $V_{thp} = -0.302V$

For Pre Design Test 2: The ICMR range chosen as per the simulation in FIG 5 was 1.2V – 2.5V, as for this range of $V_{in,CM}$ all transistors remain in saturation (denoted by the value 2 on the graph).

As evident from Design Test table in Observations:

- Purely based on hand calculations and assumptions we selected $L_{min} = 500nm$, $I_B = 90\ \mu A$ and C_C=3pF. Simulation and designing with these values resulted in lower Gain Values and GBW_{0dB} and hence they had to be modified.
- L_{min} was changed to 180nm to reduce the size of transistors M6 and M7 for which the calculated aspect ratios were too high.
- To boost the gain of the circuit we initially improve on 'gm' of second stage for which we modify aspect ratios of transistors M6, M7 and hence M3 and M4. But this can be improved only till a particular limit as it affects 'ro2' which in turn reduces the gain.
- To boost the Gain and obtain a higher GBW_{0dB}, we then increase the aspect ratios of input transistors M1 and M2.
- The values of C_C and I_B have been modified to adjust the ω_{-3dB} and the Slew Rate.
- Value of C_C does not affect gain, but $I_B \propto$ 1/Gain
- Slew Rate $\propto 1/C_C \propto$ 1/PM

8. Conclusion:

An overview of a general approach to design a two stage Operational Transconductance Amplifier has been described in this report. The procedure presented follows a pencil-and-paper method wherein the general equations obtained from behavioral characteristics of CMOS transistors are used to determine various design parameters of the transistor, to meet the prescribed system constraints. Necessary simulations and schematic diagrams implemented in Cadence have been added to the report. As for the future scope of the project optimized designs for lower power dissipation and higher gain bandwidth product can be obtained with fine tuning of the trade-offs involved in the design.

9. Contribution:

Mohit Lala (N12051916)	=> 35%
Varun Sharma (N15177570)	=> 35%
Sagar Panchal (N18051845)	=> 30%
Total:	=> 100%

10. References:

[1] G. Palmisano, G. Palumbo and S. Pennisi, “Design Procedure for Two-Stage CMOS Transconductance Operational Amplifiers: A Tutorial”, Analog Integrated Circuits and Signal Processing, 27, 179–189, 2001.
[2] B. Razavi, “Design of Analog CMOS Integrated Circuits”, New York: Mc-Graw Hill,2001.
[3] Anchal Verma, Deepak Sharma, Rajesh K. Singh and Mukul K. Yadav, “Design of Two-Stage CMOS Operational Amplifier”, IJETAE, vol 3, issue 12, December 2013.
[4] Palmisano, G. and Palumbo, G., “An optimized compensation strategy for two-stage CMOS OP AMPS.” IEEE Trans. on Circuits and Systems (part I) 42(3), pp. 178–182, March 1995.
[5] Palmisano, G. and Palumbo, G., “A compensation strategy for two-stage CMOS opamps based on current buffer.” IEEE Trans. on Circuits and Systems (part I) 44(3), pp. 257–262, March 1997.