

Universidad de las Americas Puebla

School of Engineering

Department of computing, electronics, and  
mechatronics



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**Pre-lab #4**

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**Course: Digital design LRT2022-2**

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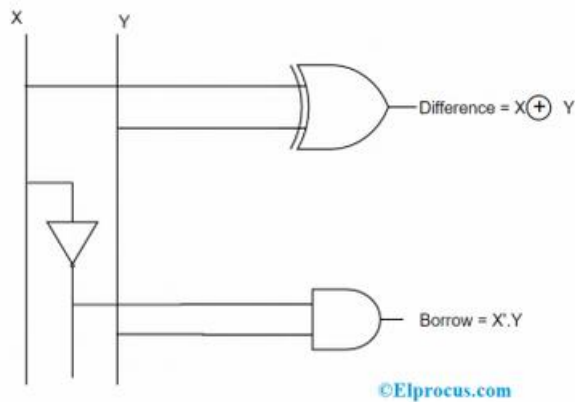
September 15, 2022, San Andrés Cholula, Puebla

### Steps to program Basys 3

1. After starting Vivado select "Start a New Project".
2. Select the location of your project.
3. Name the project.
4. Select the project type (in this case RTL).
5. Select the parts. This appears on the serial numbers of the FPGA on this order: Family, Package, Speed Grade and Temp Grade.
6. Of the two options below the filter, select the first one.
7. Open "Add Sources".
8. Select "Add or Create Constraints".
9. Select "Add Files".
10. Go to the location of the master .xdc file and select it (the file name must not have spaces).
11. Press "Finish".
12. Open "Add Sources".
13. Select "Add or Create Design Sources".
14. Select "Add Files".
15. Go to the location and select all source files needed.
16. Check "Copy sources into project".
17. Press "Finish".
18. Select the top module.
19. Make sure that the inputs and outputs are named the same as the pins in the master.
20. Select all the required signals in the master and uncomment them (ctrl + /).
21. Select "Tools".
22. Select "Project Settings".
23. Select "Bitstream".
24. Check "bin\_file".
25. Press "Run Synthesis".
26. After it finishes, select "Open Synthesized Design".
27. Select "Tools".
28. Open "Edit Device Properties".
29. Make sure that "Bitstream Compression" is true.
30. Change "Configuration Rate" to 33 mhz.
31. In "Configuration Mode" choose SPI x4.
32. Close and save the synthesized design.
33. Press "Generate Bitstream".
34. Open "Hardware Manager".
35. Open "Hardware Target".
36. Make sure the FPGA is turned on and plugged in via the USB port.
37. Change the "JTAG Clock Frequency" to 30 mhz.
38. Select the device and click next.
39. Press "Finish".
40. Select "Program Device".
41. Modify the top module bit file by selecting your desired bit file.
42. Press "Program".
43. After it finished the FPGA will be programmed.

## Half-subtractor Circuit

This circuit does the job of subtracting a value with another, though in binary form. It does this by using a XOR Gate, a NOT Gate and an AND Gate.



*Half Subtractor Logical Circuit*

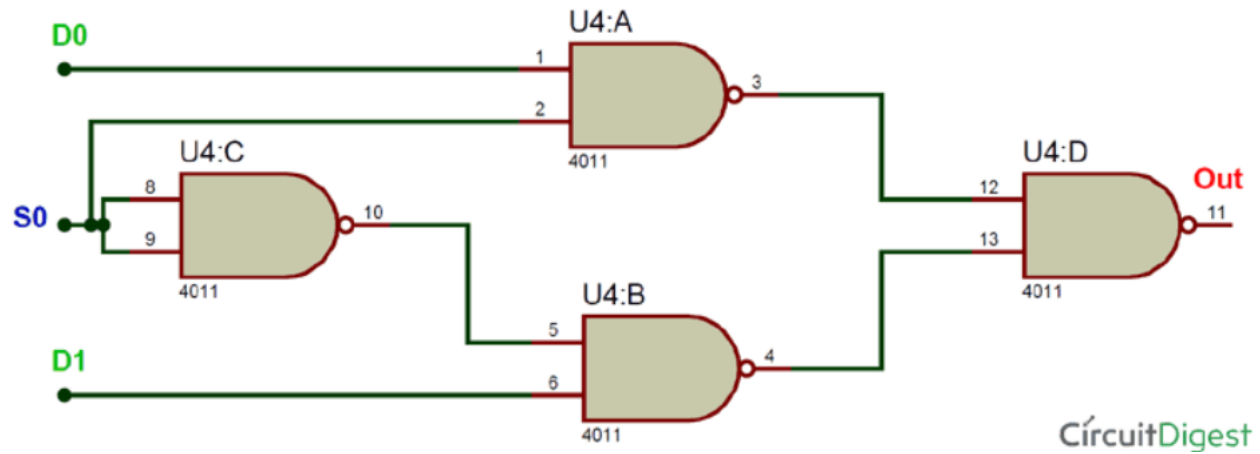
## Magnitude Comparator Circuit

This is a circuit that compares two binary numbers and checks which one is bigger than the other, or if they are equal. It means it has two inputs and three possible outputs.



## Multiplexer Circuit

This circuit is a system to choose from  $2n$  inputs depending on the  $n$  control inputs. In the case where there is only one control input, the value of the input will determine which of the inputs will be passed through to the output of the whole system. The system will grow with whatever amount of inputs are necessary to choose from.



## Demultiplexer Circuit

This is basically the contrary to a Multiplexer, as it chooses a specific output for the input. It has  $2^n$  of outputs, one input, and  $n$  control inputs. It also always has one enabler input, which enables the rest of the circuit only when its 1.

