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Ch : 3 : Sequential Circuits & Systems.

* Overview of Combinational Circuits:

→ In combinational circuits the output depends only on the present inputs.
→ It does not depend on the past status of inputs.
→ So, there is no need to store the past inputs or outputs.
→ Therefore, combinational circuits does not require any memory.
→ Also, In these circuits we do not use any timing and synchronization signal such as clock signal.
→ combinational circuits are faster in speed and easy to design.
→ examples, Adders, subtracters etc.

* Introduction to sequential circuits

→ In sequential circuits, output depends on the present time inputs, the previous output (past) and the sequence in which inputs are applied.

→ So, to provide the past input or output a memory element is required.
→ In these circuits timing signal (clocks) are used.

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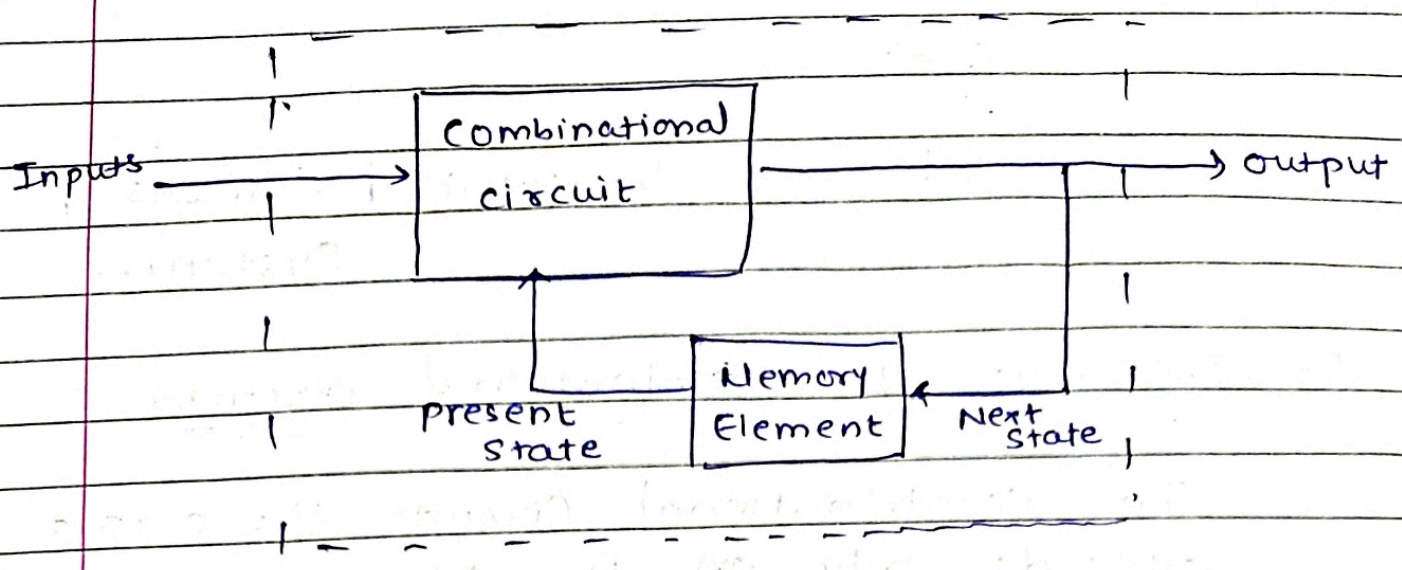

* present state :-

→ Data stored by the memory element at any given time is called present state

* Next state :-

→ - The combinational circuit in this block Diagram takes external inputs & present state, and produces outputs.

→ some of these new outputs are stored in memory element called as next state.

→ The memory element is known as Flip-flop (FF)

* examples of sequential circuits.
  - counters & Registers.

* ~~clock signals~~

→ Types of sequential circuits

(1) Asynchronous

(2) Synchronous.

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* Asynchronous Sequential Circuits:-

→ Outputs changes at any time

→ There is no clock. so, output can not be controlled

→ ~~example, [illegible]~~.

* Synchronous sequential circuits:-

→ output changes only on clock pulse. so, outputs are controlled.

→ ~~example, [illegible]~~.

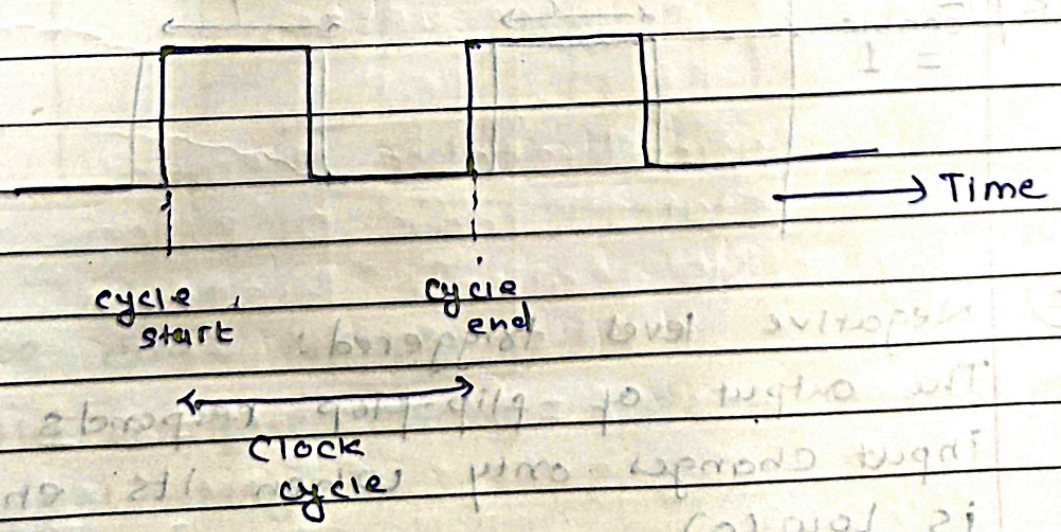
* Clock Signal:-

→ Clock signal is a timing signal.

→ It is input to the sequential circuit.

→ It is Rectengular signal, with the duty cycle of 50%.

→ The time required to complete one cycle is called 'clock period' or 'clock cycle'.



Clock Signal

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→ Triggering Methods :-

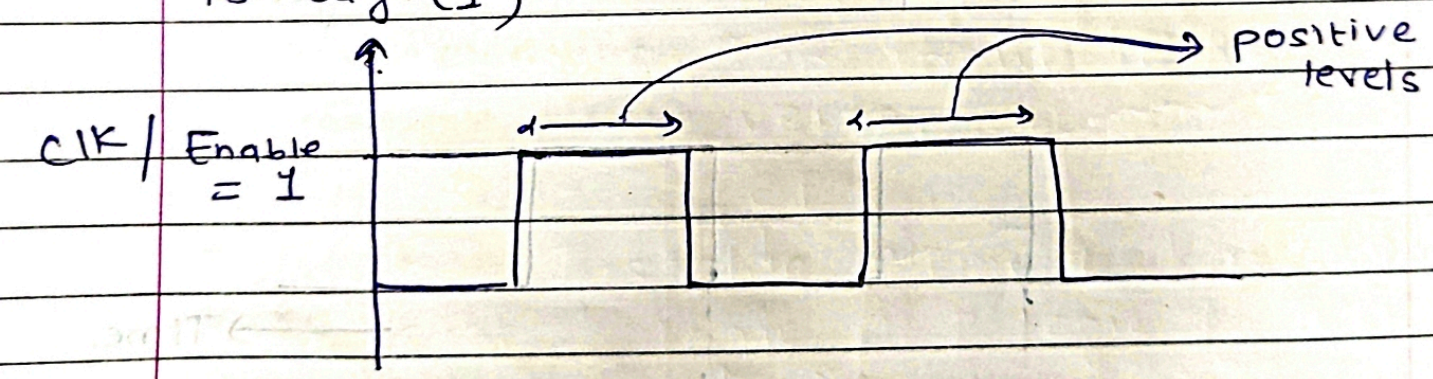
→ Depending on which portion of the signal the latch or flip-flop responds to we can classify them into two types.

1. Level ~~triggered~~ triggering.

→ In the level triggering the output state is allowed to change according to input(s) when there is active level of enable.

→ Active level can be positive level or Negative level.

(1) Positive level triggered :-
The output of flip-flop responds to the input changes only when its enable input is high (1)



(2) Negative level triggered :
The output of flip-flop responds to the input changes only when its enable input is Low (0)

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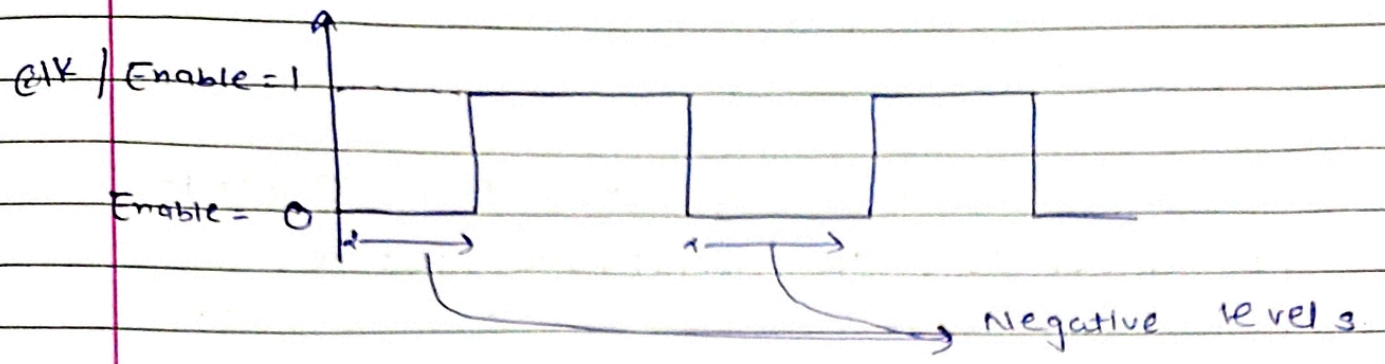


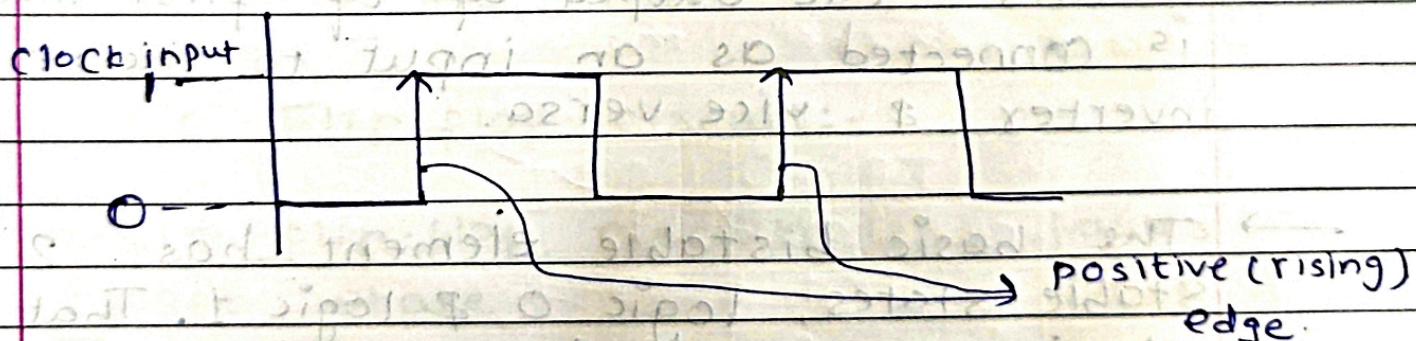
2. Edge Triggering:

→ The flip-flops will only change its state at the Edge of the clock input.

→ Clock input have 2 Edges, positive (rising) and Negative (Falling)

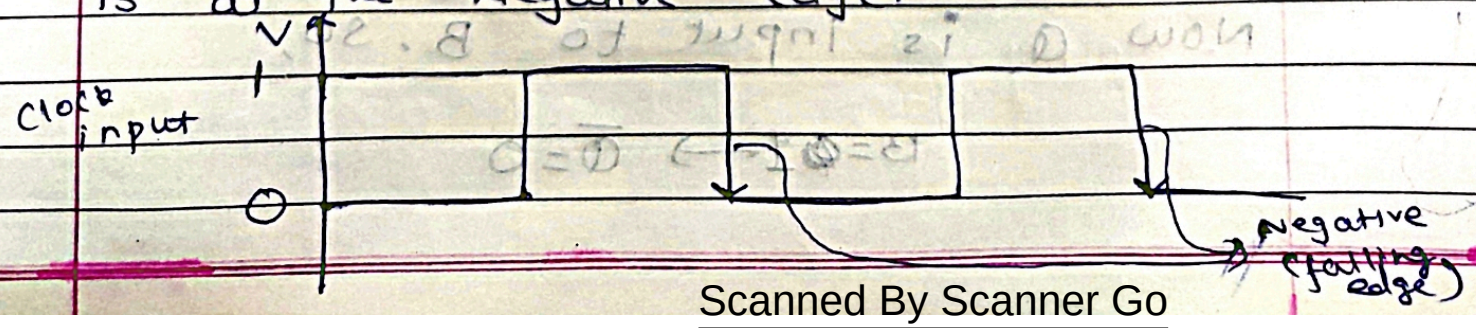
(1) Positive Edge Triggering:-

~~[illegible]~~ The output changes only when the input is at the positive edge of the clock pulse.



(2) Negative edge triggering:

Here, the output changes, when the input is at the Negative Edge.



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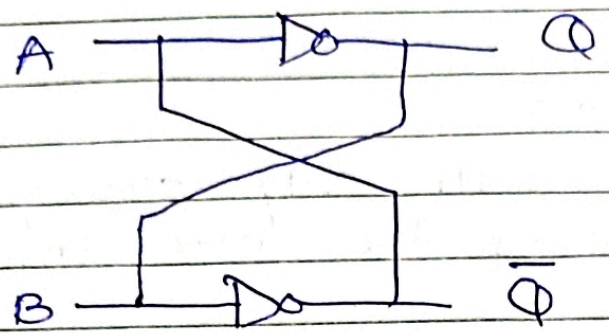
Flipflops

→ One-bit Memory and the Circuit properties of Bistable latch.



Basic bistable element (1-bit memory cell)

→ The basic bistable element has 2 outputs Q & $\overline{Q}$.

→ It has two cross-coupled inverter. means the output of of first inverter is connected as an input to the second inverter & vice versa.

→ The basic bistable element has 2 stable states, logic 0 & logic 1. That is why it is called "bistable".

→ Here, for A = 0 → Q = 1

Now Q is input to B. so,

B = 1 → $\overline{Q}$ = 0

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→ So, Here property is satisfied that Q and $\overline{Q}$ are complements of each other

→ for $A = 1 \longrightarrow Q = 0$, so

$B = 0 \longrightarrow \overline{Q} = 1$ (satisfied).

Same way one can try for $B=0$ & $B=1$.

→ The 1-bit information in the circuit is locked or latched in the circuit. Therefore this circuit is also reffered as latch.

* Flip-flops

→ A flip-flop circuit will maintain binary state until any input signal is given to switch the state.

* Basic Flip-flop circuit:-

→ Basic flip-flop circuit has four states

1. Set state
2. Reset state
3. No change / previous state (Same as previous state)
4. Indeterminate state. (when both o/p is same)

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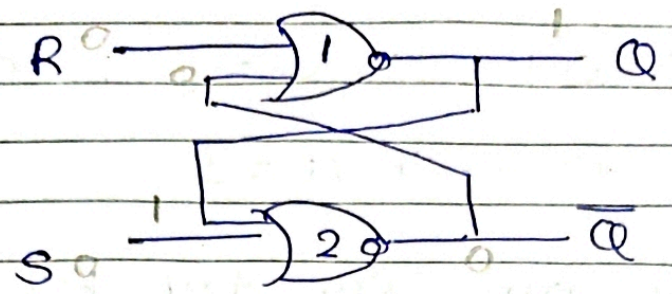
→ Basic SR flip-flop / Direct-coupled SR Latch / RS flip-flop.

(1) RS flip-flop Using NOR gates.



→ Here, the R is Reset state & S is state state.

→ In this flipflop 2 inputs are given R and S, and two outputs are present Q & $\overline{Q}$.

→ two nor gates are cross-coupled

→ First, Let's make the TT of NOR gate

IP		OP
0	0	1
0	1	0
1	0	0
1	1	0

Here, the output of NOR gate is 0 if any one input is 1.

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Case 1: $S = 1$ & $R = 0$

→ since, gate 2 has input 1, so $\overline{Q}$ must be 0 (As per NOR gate condition).

$$\boxed{S = 1} \rightarrow \boxed{\overline{Q} = 0}$$

→ Now, $\overline{Q}$ is input to gate 1.
so, $\boxed{R = 0}$ & $\boxed{\overline{Q} = 0}$ will give the output $\boxed{Q = 1}$

→ So, when $S = 1$ & $R = 0$ outputs are $Q = 1$ & $\overline{Q} = 0$

→ This condition of $Q = 1$ & $\overline{Q} = 0$ is called set state

→ So, set state is achieved when set input $\boxed{S = 1}$.

Case 2: $S = 0$ & $R = 0$

Now, let's check how FF gives some output as previous state.

Here, from case 1 we have $\boxed{Q = 1 \text{ \& } \overline{Q} = 0}$ previous state.

→ So, gate 2 will have 2 inputs $S = 0$ & $Q = 1$.

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→ From NOR gate table 01 = 0.

so, $\boxed{\overline{Q} = 0}$

→ Now for gate 2 Has 2 inputs

$R = 0$ & $\overline{Q} = 0$

→ From TT 00 = 1 so $\boxed{Q = 1}$

so, Here, output is $\boxed{Q = 1 \ \& \ \overline{Q} = 0}$

which is same as previous state.

so, In NOR gated SR flip-flop will give previous state when $S = 0$ & $R = 0$

<u>case 3:</u> $S = 0$ $R = 1$

→ gate 1: - $R = 1$ → any one i/p = 1 the op = 0 (NOR TT)

so $\boxed{Q = 0}$

→ $Q = 0$ is input to gate 2:

gate 2: $Q = 0$ $S = 0$ so $\overline{Q} = 1$ (NOR TT)

→ so, final o/p $Q = 0$ & $\overline{Q} = 1$

→ $R = 1$ & $S = 0$ will give output $Q = 0$ & $\overline{Q} = 1$

→ This state is called Reset State.

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Case 4: $S=0$ & $R=0$

Let's check this condition again

Here, previous state from case 3

$Q=0$ & $\overline{Q}=1$

check like case 2

After applying input $S=0$ & $R=0$ the O/P will be $Q=0$ & $\overline{Q}=1$ same as previous state.

→ So, In NOR gate $S=0$ & $R=0$ will give previous state.

Case 5: $S=1$ & $R=1$

Here, for gate 2 $S=1$ give O/P $\boxed{\overline{Q}=0}$

(O/P = 0 if any 1 input is 1)

Now, Gate 1 has 2 inputs

$R=1$ & $\overline{Q}=0$

→ $1 \mid 0 = 0$ so O/P $\boxed{Q=0}$

Here we note that when $S=1$ & $R=1$ both the O/P Q & $\overline{Q}$ will be 0.

→ This case does not satisfy the condition that Q & $\overline{Q}$ are complement of each other.

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So, In NOR gate SR flipflop the

$\boxed{S = 1 \ \& \ R = 1}$ gives $\boxed{Q = 0 \ \& \ \bar{Q} = 0}$

that is invalid / Indeterminate state.

→ This state is undefined and usually avoided.

S	R	Q	$\bar{Q}$	
1	0	1	0	(set)
0	0	1	0	(previous)
0	1	0	1	(Reset)
0	0	0	1	(previous)
1	1	0	0	(Indeterminate)

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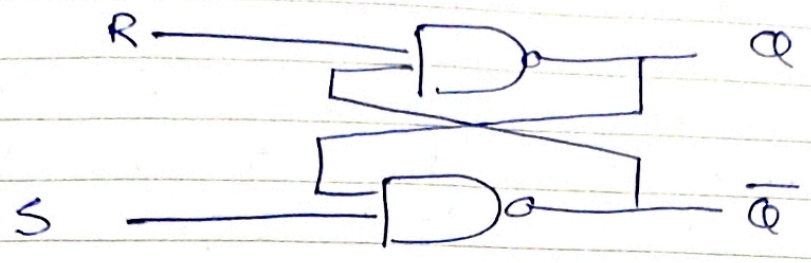
★ SR Flip flop / Basic SR flipflop using NAND gate



NAND gate

I/P		O/P
0	0	1
0	1	1
1	0	1
1	1	0

O/P = 1 if any one input is 0.

Truth Table:-

S	R	Q	$\overline{Q}$	
1	0	1	0	set
1	1	1	0	No change
0	1	0	1	Reset
1	1	0	1	No change
0	0	1	1	Indeterminate.

→ when S = 1 & R = 0, Q = 1 & $\overline{Q}$ = 0 meaning set state

→ when S = 1 & R = 1 O/P → No change state

→ when S = 0 & R = 1, Q = 0 & $\overline{Q}$ = 1 meaning Reset state

→ when S = 0 & R = 0, Q = 1 & $\overline{Q}$ = 1 that gives Invalid state.

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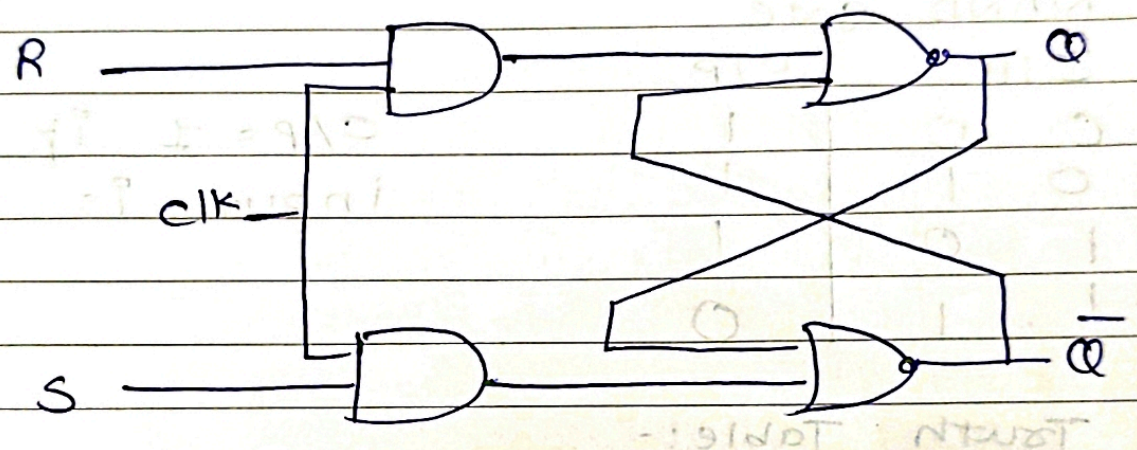
Clocked RS flipflop:- (NOR)

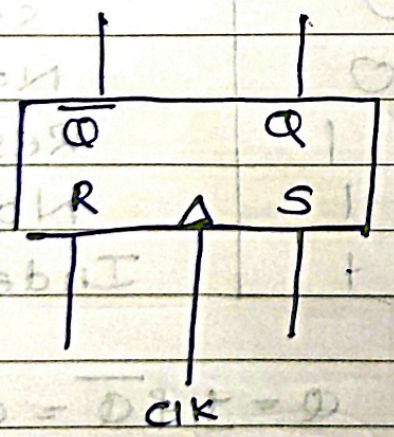
→ In clocked RS flip flop 2 and gates & 2 NOR gates are connected

→ NOR gates are cross coupled & 2 AND gates will be given input R & S with clock signal.

→ Diagram:-



→ logic Diagram



→ graphic symbol

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Inputs			outputs	
Q	S	R	Q(t+1)	
0	0	0	0	(No change)
0	0	1	0	(Reset)
0	1	0	1	(set)
0	1	1	x	(Indeterminate)
1	0	0	1	(No change)
1	0	1	0	(Reset)
1	1	0	1	(set)
1	1	1	x	(Indeterminate)

→ Q is the binary state of the flip-flop at a given time named as present state

→ Q(t+1) is the state of the flip-flop after occurrance of flip flop refrred as next state.

→ Here, when S=0 R=0, gives NC state
S=0 R=1, gives Reset state
S=1 R=0, gives set state
S=1 R=1, gives Invalid state.

→ The triangle symbol in the graphic symbol of clock pulse. & responds to an input clock transition from low level (0) to high level (1).

→

Q \ SR				
	0	0	X	1
	1	0	X	1

$Q(t+1) = S + \overline{R}Q$

SR = 0

(means S & R can not be 1 together

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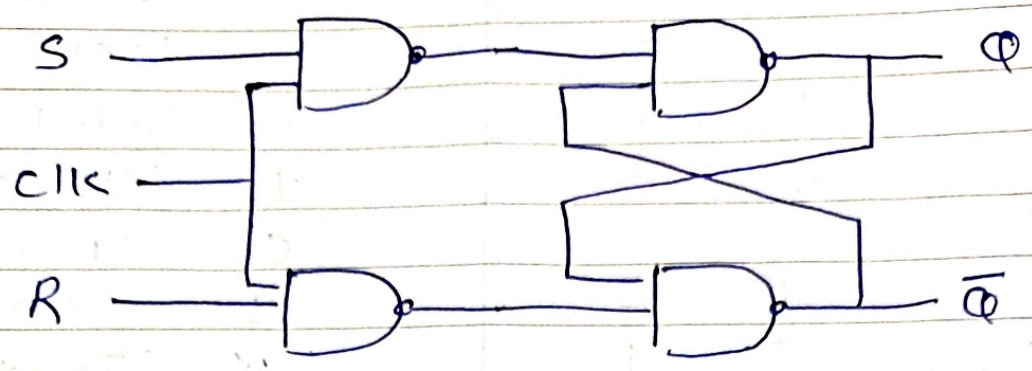
→ Clocked RS flipflop using NAND.

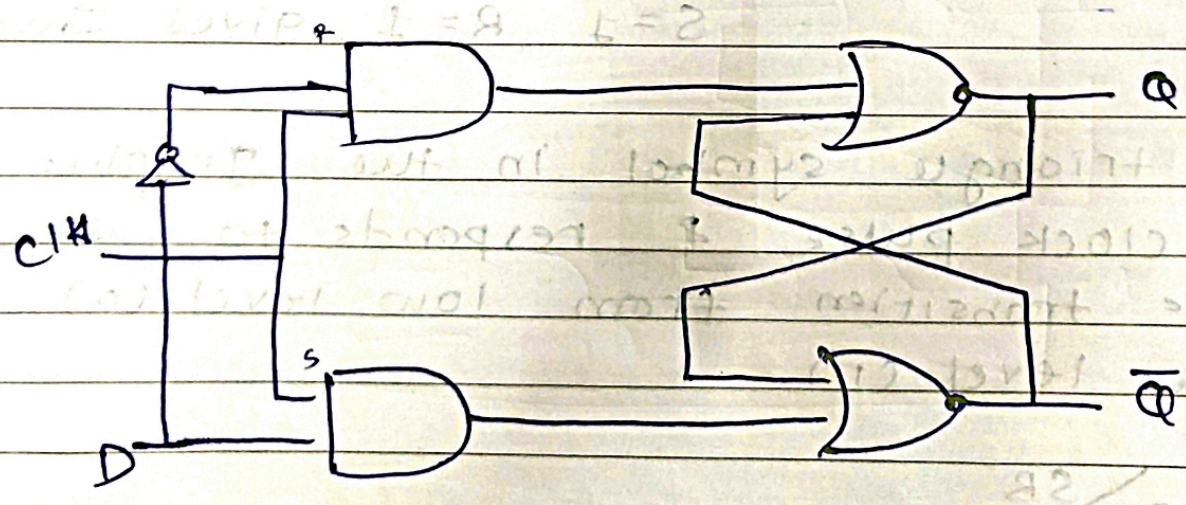


* D-flip flop (Delay flip-flop)

→ In D flip-flop we connect the Inverter between the set and Reset inputs.

→ D flip-flop ensures that, at the same time S & R are never equal to 1.

* D flip-flop using NOR :-



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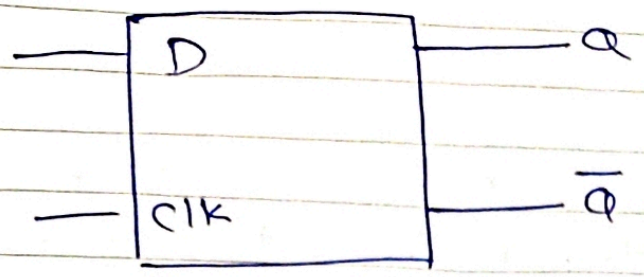


graphic symbol

Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

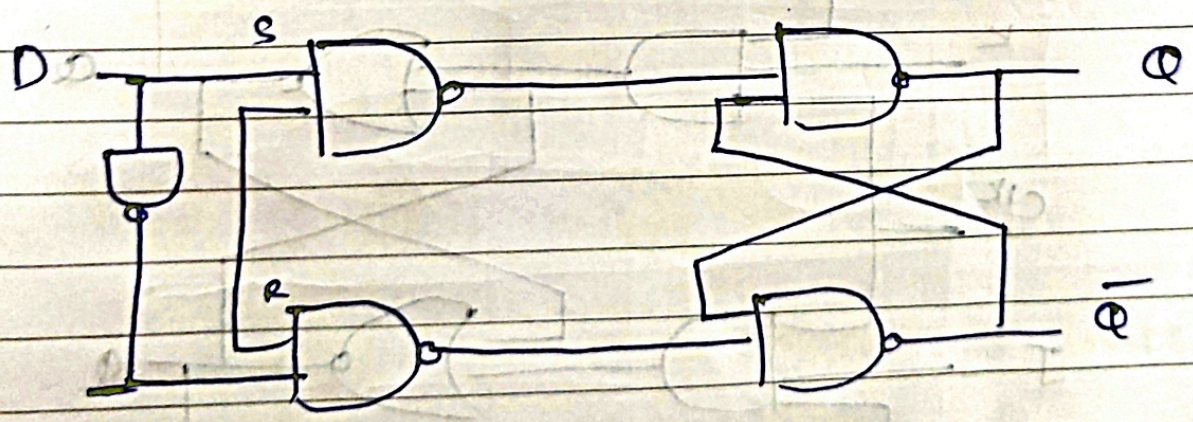
Q \ D	$\overline{D}$	D
$\overline{Q}$	0	1
Q	0	1

$$\boxed{Q(t+1) = D}$$

so, when $D = 0$ $Q(t+1) = 0$

$D = 1$ $Q(t+1) = 1$

D flip-flop using NAND:



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J - Set
K - Reset

* JK flip-flop

→ Works same as SR flip-flop.

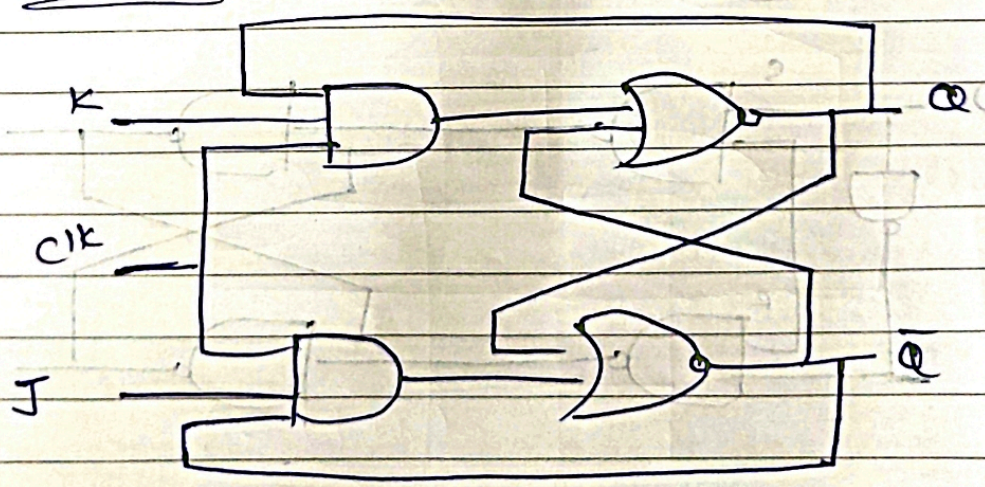
→ The only difference between JK flip flop and SR flipflop is that when both inputs of SR is set to 1, the circuit produces the invalid states.

→ But in JK flip-flop, there are NO invalid states even if both 'J' & 'K' flip-flop are set to 1.

→ 11 input will produce Toggle condition

for toggle { so, when $Q = 0$ (prev state) $Q(t+1) = 1$
$Q = 1$ (prev state) $Q(t+1) = 0$

* JK flip flop Using NOR gates.



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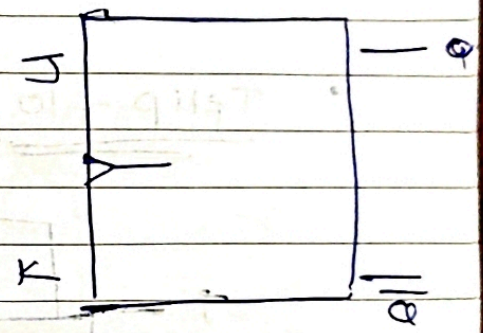
Q	J	K	Q(t+1)	
0	0	0	0	NC
0	0	1	0	Reset
0	1	0	1	set
0	1	1	1	Toggle
1	0	0	1	NC
1	0	1	0	Reset
1	1	0	1	set
1	1	1	0	toggle

J \ KQ	$\bar{K}\bar{Q}$	$\bar{K}Q$	KQ	$K\bar{Q}$
$\bar{J}$	0	0	1	1
J	1	0	0	1



Q \ JK				
	0	0	1	1
	1	0	0	1

$Q(t+1) = \bar{Q}J + K\bar{Q}$

When $J=0$ $K=0$ State is NC
$J=0$ $K=1$ " Reset
$J=1$ $K=0$ " set
$J=1$ $K=1$ " toggle

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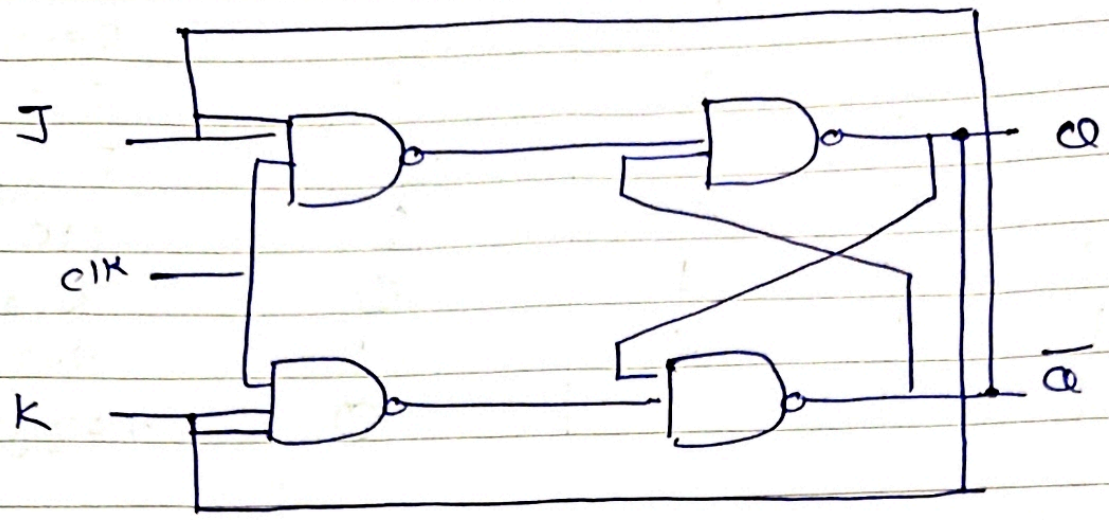
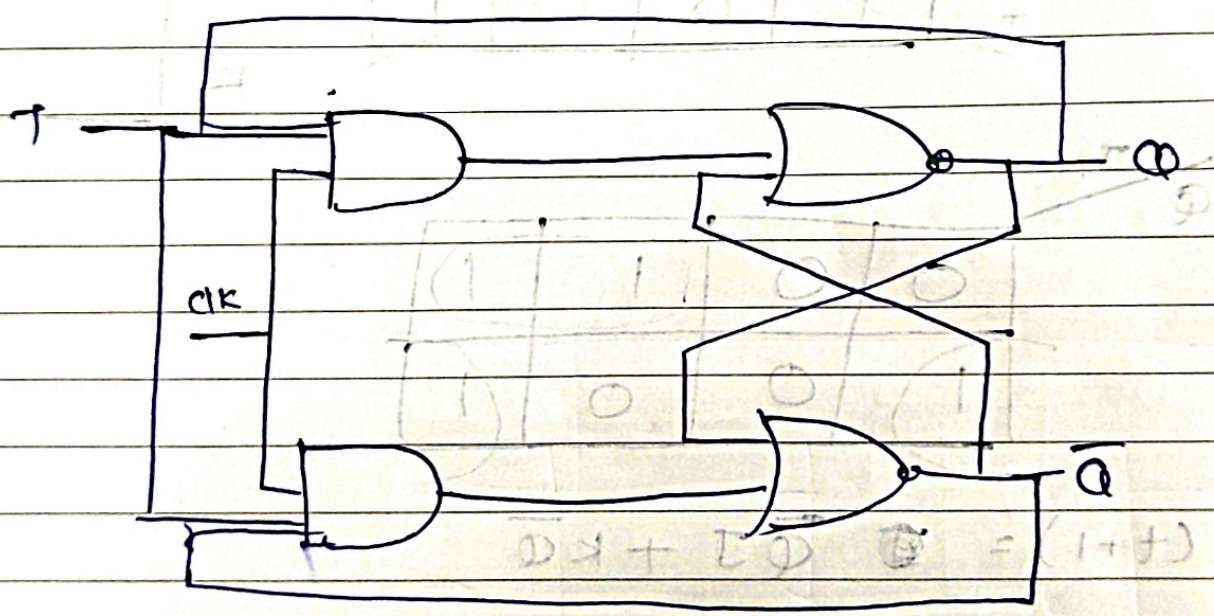
JK-flipflop using NAND:



Tflip-flop (Toggle flipflop).



Q	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

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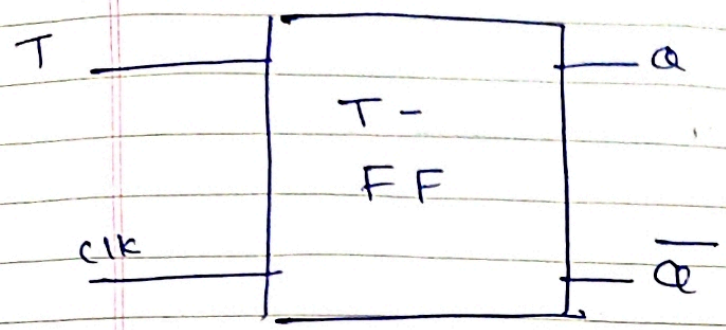
when $T = 0 \rightarrow Q(t+1) \rightarrow$ No change
$T = 1 \rightarrow Q(t+1) \rightarrow$ Toggle



$Q \backslash T$	$\overline{T}$	T
$\overline{Q}$	0	1
Q	1	0

$$Q(t+1) = \overline{Q}T + Q\overline{T}$$

Race Around Condition :-

→ In JK flip flop, outputs are connected to inputs. i.e outputs are feed back to inputs.

→ when J & K both will be 1 (toggle), if clk = 1 for a long period of time, then Q output will toggle as long as the clk is high which makes the output of the flip-flop unstable or uncertain.

→ This problem is called Race around condition.

→ To overcome this problem Master-slave flipflop is used.

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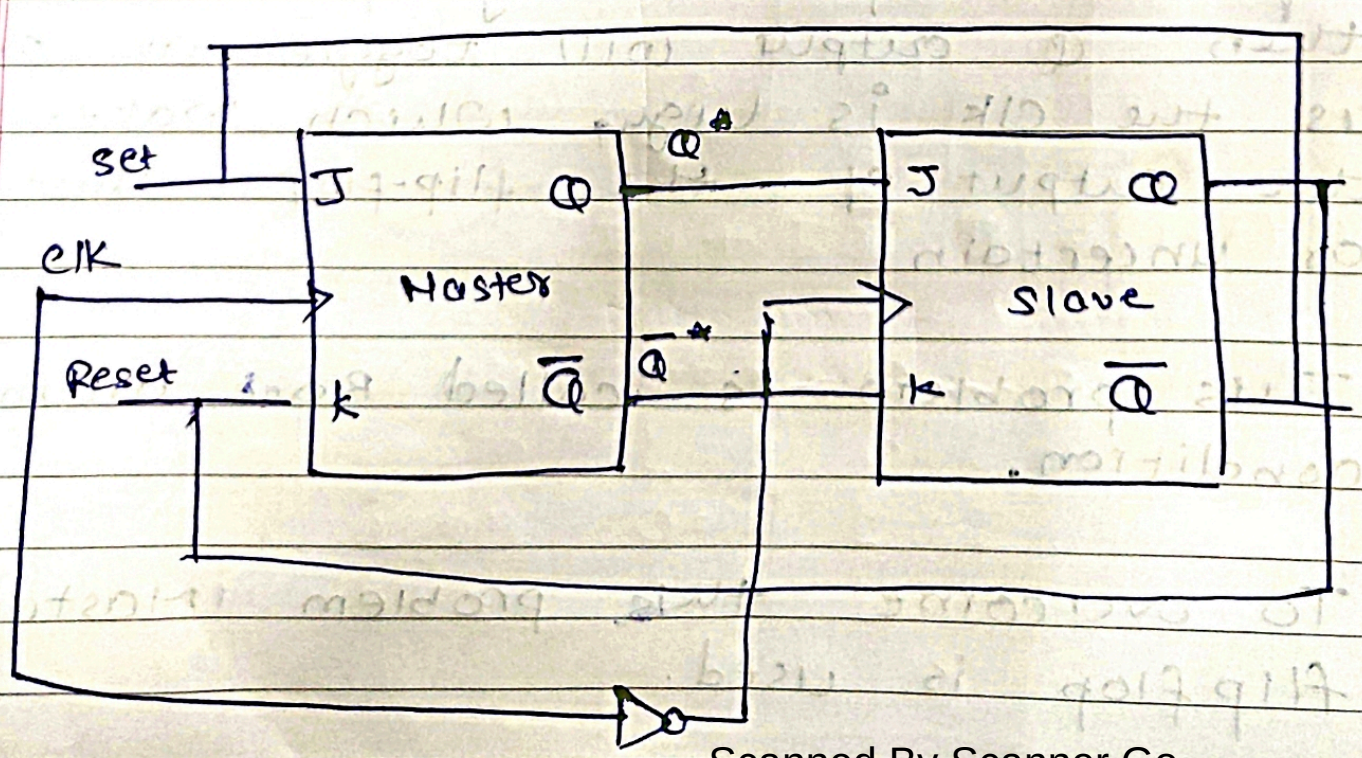
Master-Slave Flip-flop.

- A Master-slave flip flop is constructed from two separate flipflops.
- One circuit serves as a master and the other as a slave. so, the overall circuit is referred to as master-slave flip-flop.



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→ In addition of these two flipflops, the circuit also includes an inverter.

→ Here, Inverter is connected with clk pulse of slave flipflop.

→ So, when clk = 1 for master flipflop,
clk = 0 for slave flipflop & vice versa.

Working:

→ When the clk = 1, Master FF will work & slave FF will be isolated.

→ So, the outputs of Master FF (Q^* & $\overline{Q}^*$) will be generated according to the JK flipflop TT.

→ When clk = 0, Master FF will be isolated & slave FF will work

→ Now, the outputs of Master FF (Q^* & $\overline{Q}^*$) will be input to the slave FF & outputs will be produced according to JK flipflop.

→ Since, the second flipflop follows the first one, it is referred as the slave & first one as the master.

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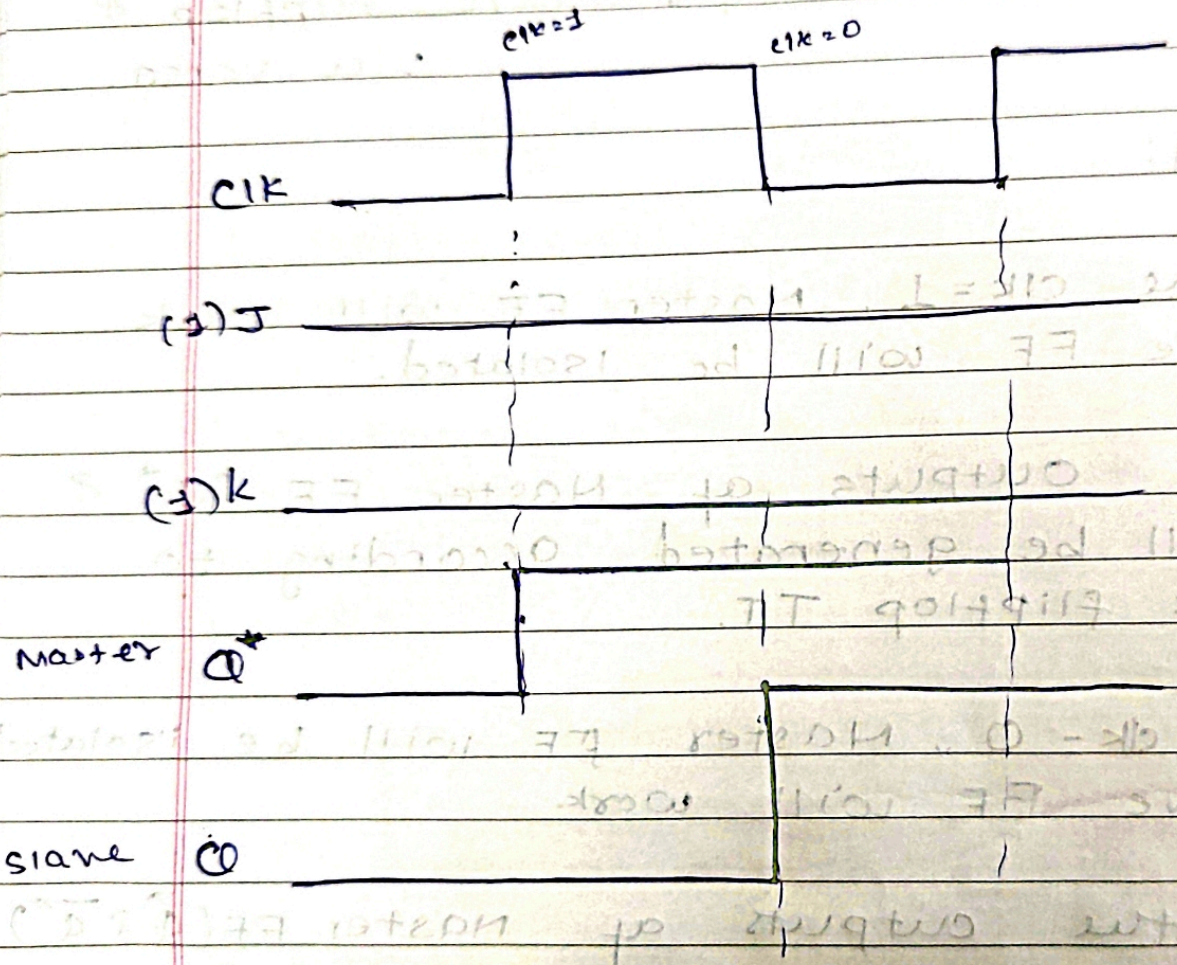
→ In master-slave JK flip-flop state change occurs when flip-flop goes through both positive transition (First half) of clock and negative transition of the clock (second half). Thus, race-around condition does not exist in Master slave JK flip flop.



Timing Diagram of Master-slave J-k flip flop.

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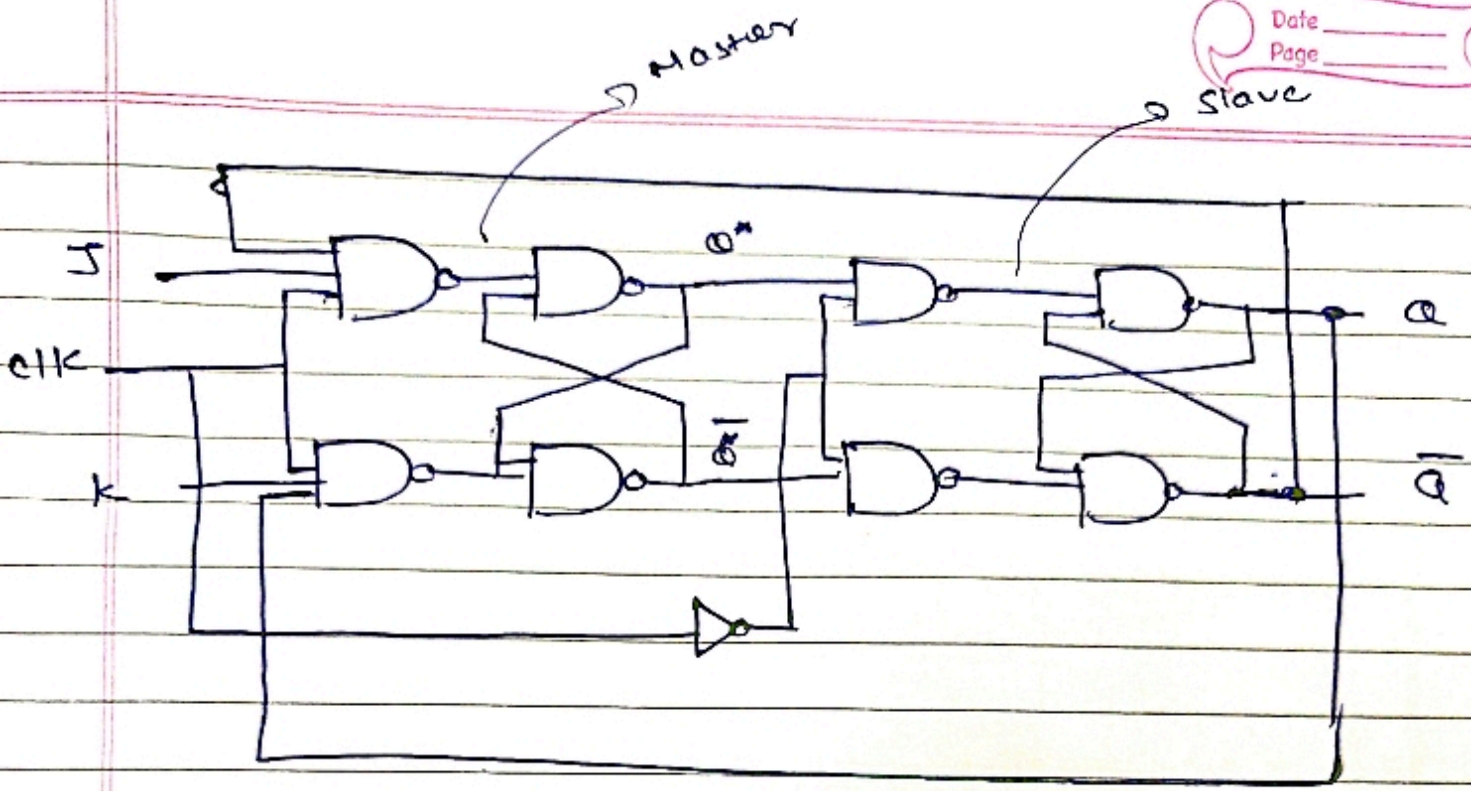

Master slave JK flipflop.

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