





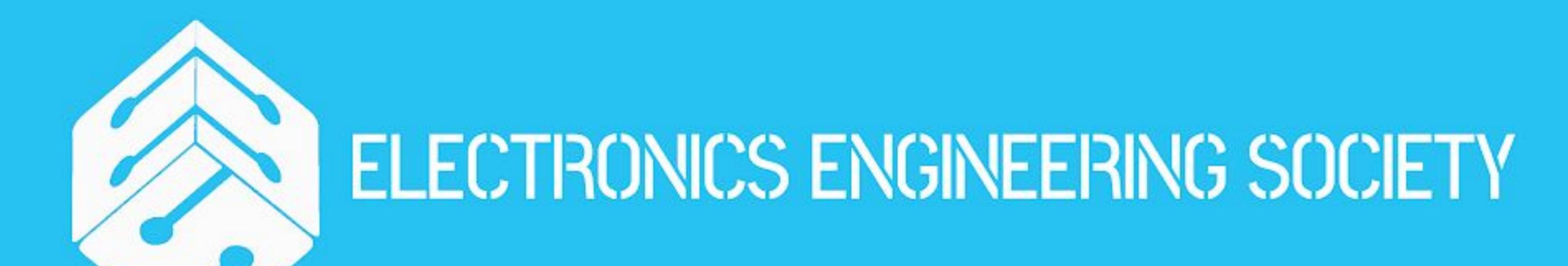
ROUND-1

The government is now focussing on developing Varanasi into a smart city and has decided to deploy a network of wireless sensor nodes in various parts of the city. The sensor nodes are supposed to sense the humidity and temperature of the region and forward it to the Central network connecting all citizens of the city. Knowing the weather conditions, people can easily decide the appropriate mode of transportation for them.

To fulfill PM's vision of self-reliability in semiconductor manufacturing, our government has decided to design all the components in Varanasi itself. So they asked IIT Varanasi to develop the microprocessor required to process the sensory data.

Your fellow engineers have preprocessed the raw sensory data and converted the analog output of the sensors into an 8-bit wide digital signal.

Your seniors are designing a control unit for such microprocessors and they need engineers who can design a digital circuit that can be used in these processors without needing to alter the current design of the control unit, they call this circuit a CalC. The control unit they are designing will generate six single-bit control signals for each function performed by CalC and will receive two single-bit status signals after the completion of every function.



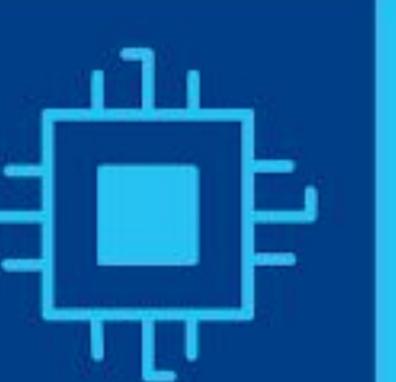
















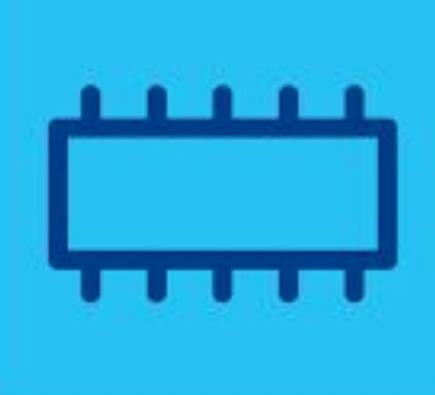






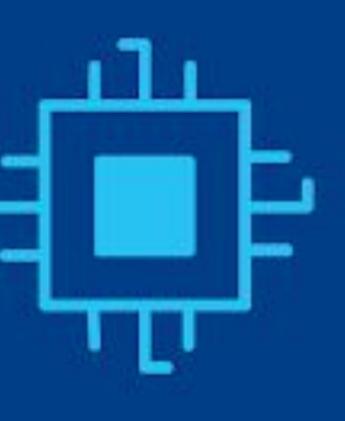












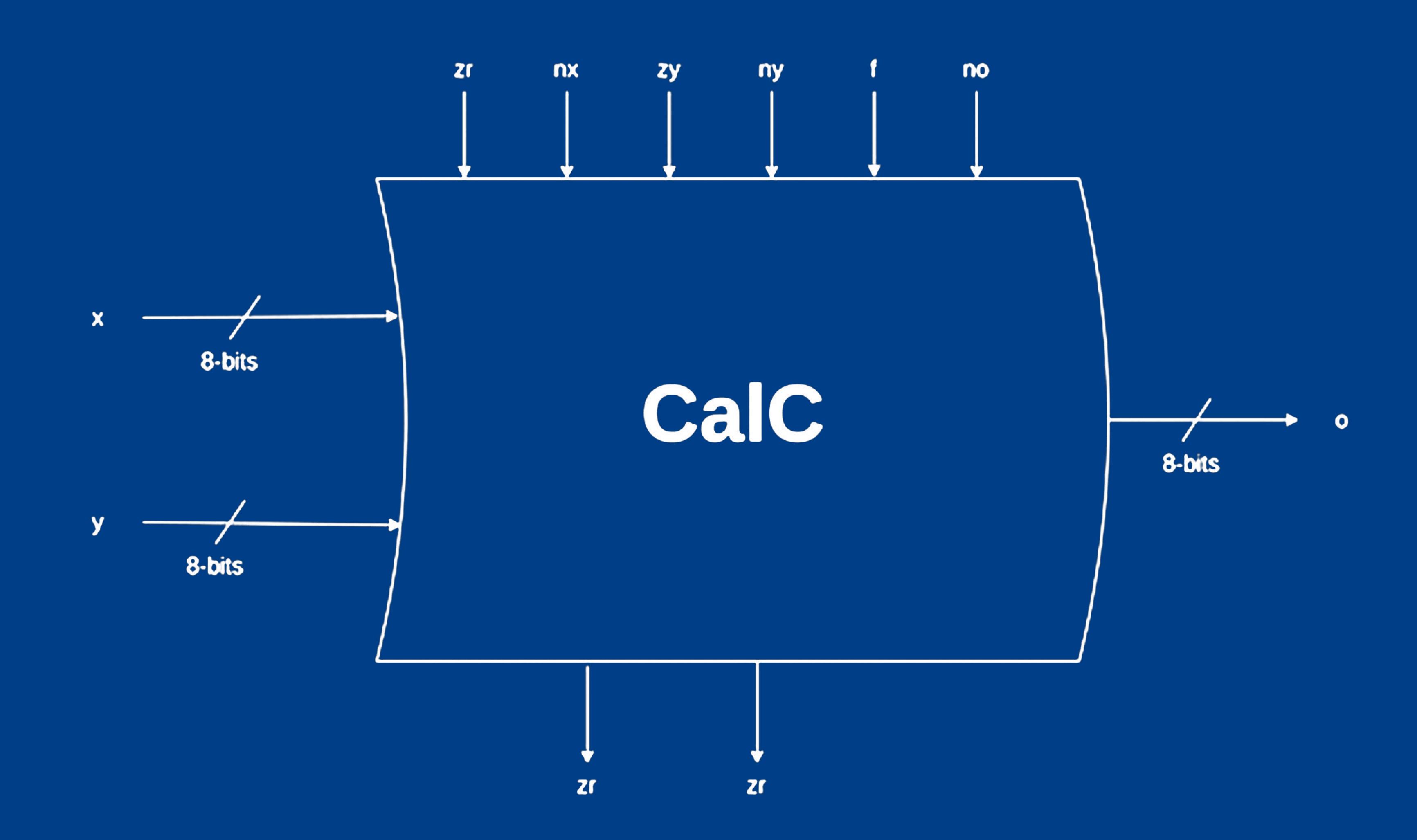






TASK:

You have been assigned to design CalC which will perform arithmetic and logical operations on 8-bit digital inputs and return an 8-bit digital output.



Each control signal represents a basic operation on inputs as mentioned:

zx: Changes the x input to a numerical equivalent to zero.

nx: Inverts all the bits of input x.

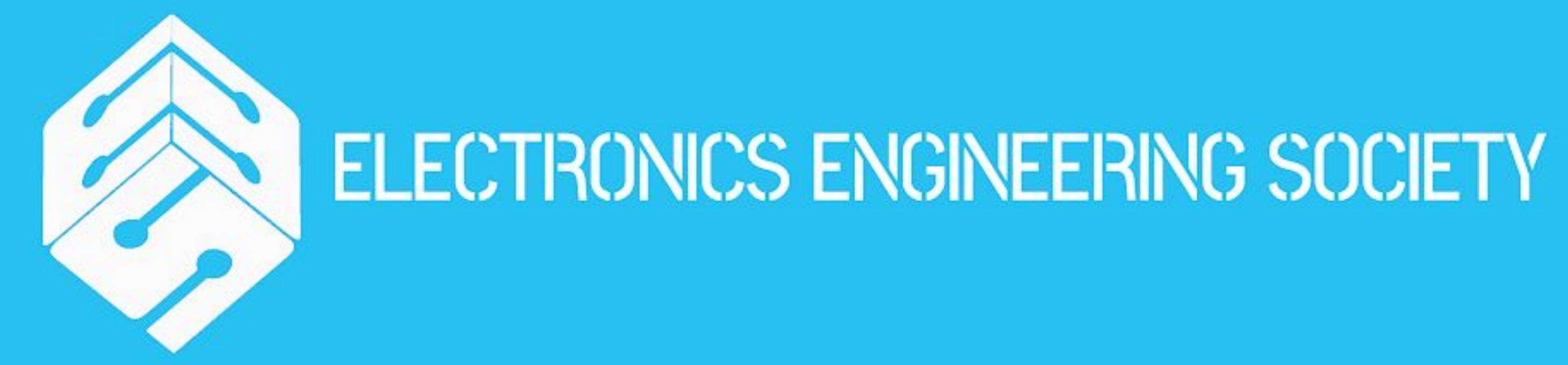
zy: Changes the yinput to a numerical equivalent to zero.

ny: Inverts all the bits of input y.

f: if f = 0, then o = x&y If f = 1, then o = x + y

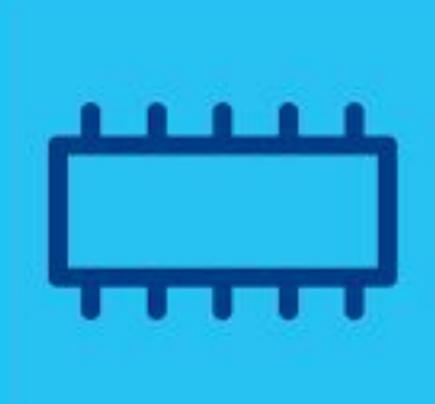
no: Inverts all the bits of computed output o.

Inputs are processed according to control signals in sequential order.



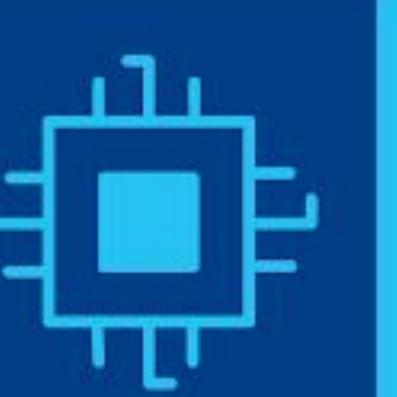






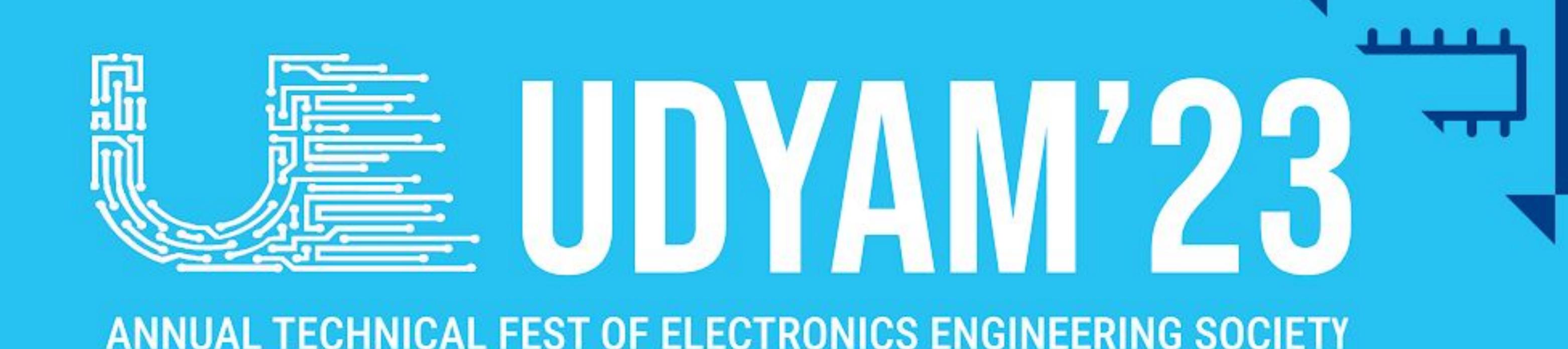








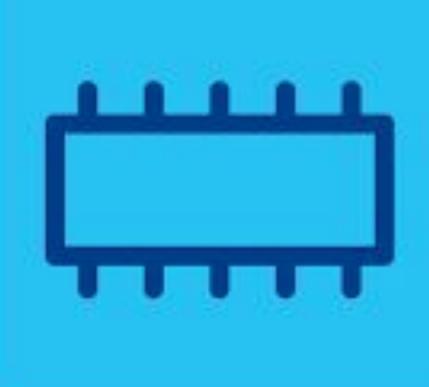






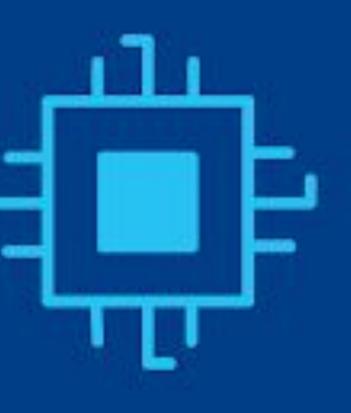


















Let's say, the control unit generates '001101' as a combination of control bits for CalC, this combination will give output o = 1x.

Here,

zx=0: No change in xnx=0: No change in xzy=1: Change y to 0

ny=1: Invert all bits of y (Now all bits of y are 1)

f=0 : o=x&y (Now o is equivalent to x)

no=1: Invert all bits of o (Now the final output is the negation of x)

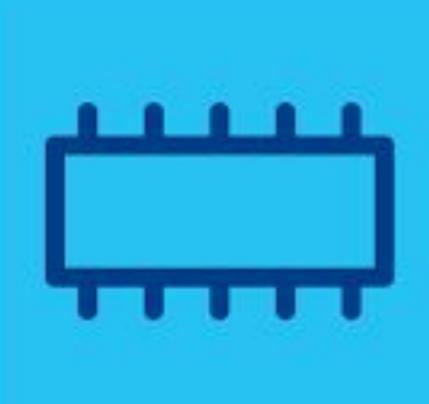
Along with the output, the CalC also generates two status signals:

zr: If the final output is zero, then 'zr' bit changes to 1, else it will remain 0. ng: If the final output is negative, the 'ng' bit changes to 1, else it will remain 0.

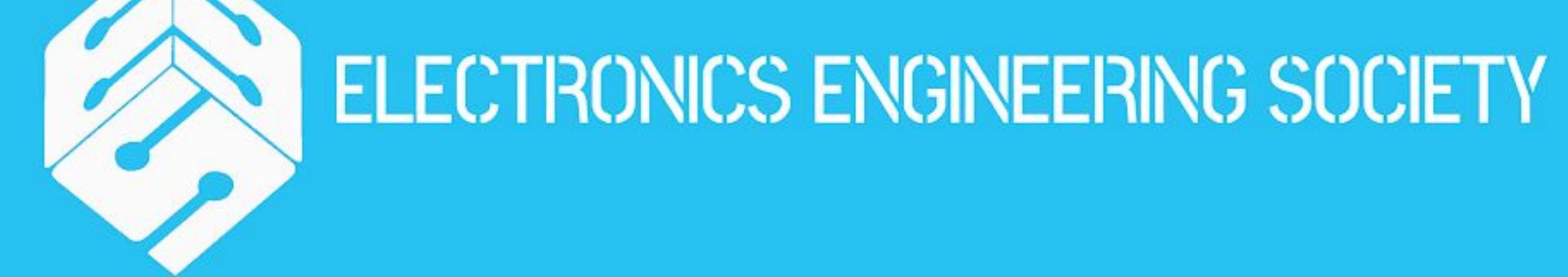
Your task is to design the CalC such that it outputs the following 18 functions corresponding to 18 different combinations of control signals {zx,nx,zy,ny,f,no}.



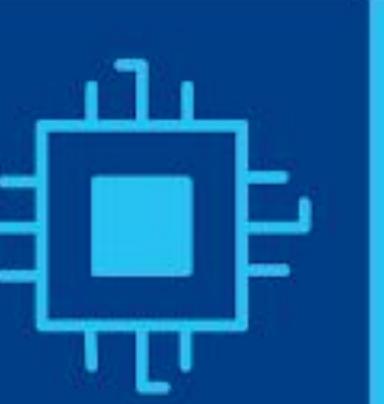


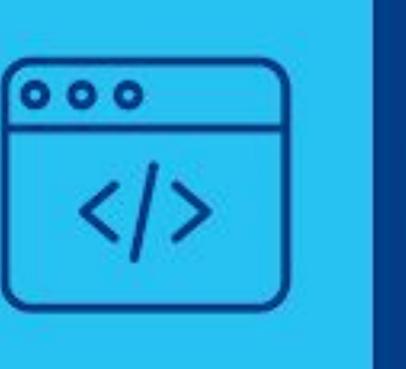














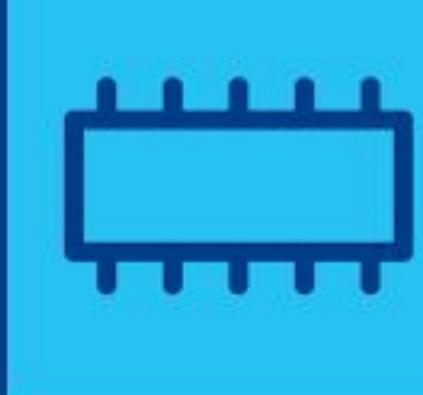






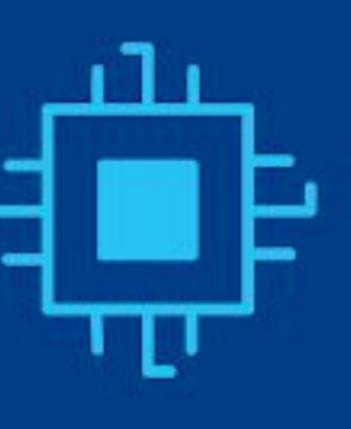












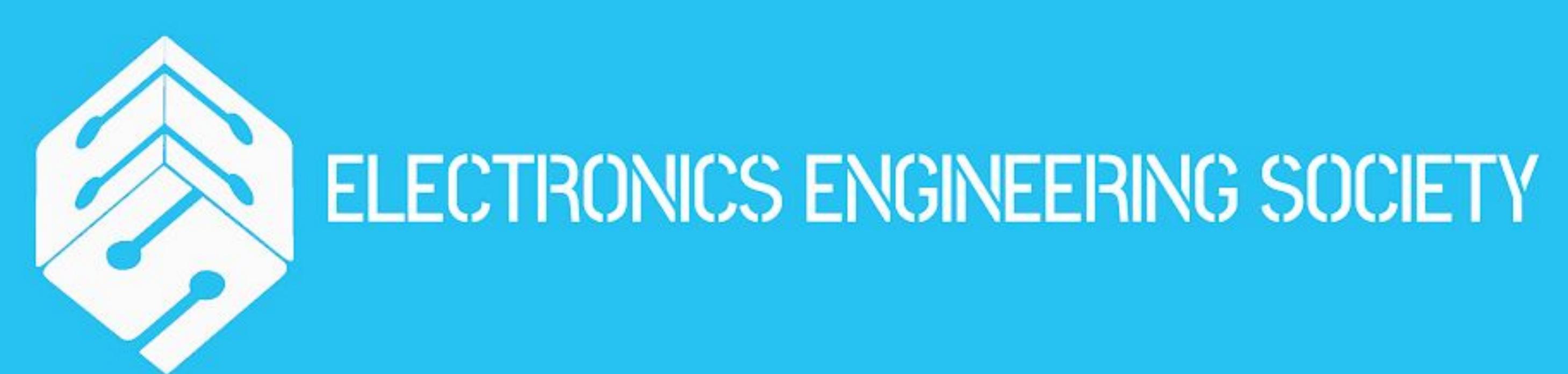






	x+1
1	y+1
-1	x-1
X	y-1
y	X+y
	X-y
	y-X
-X	x&y
- y	Xy

Hint: You have to determine appropriate combinations of control bits which will result the above functions as the final output of CalC.



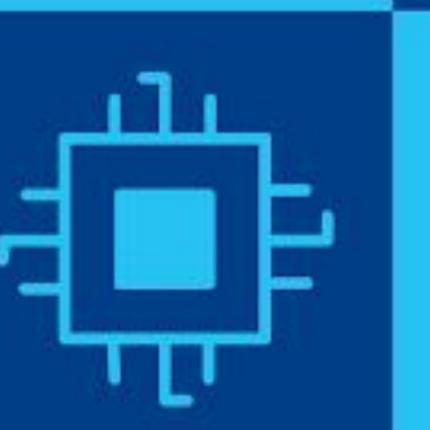
















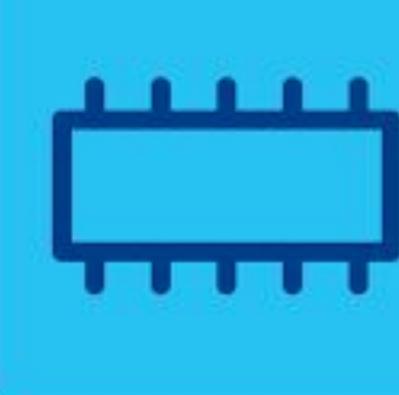






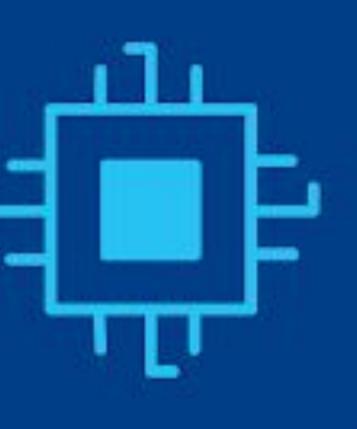
















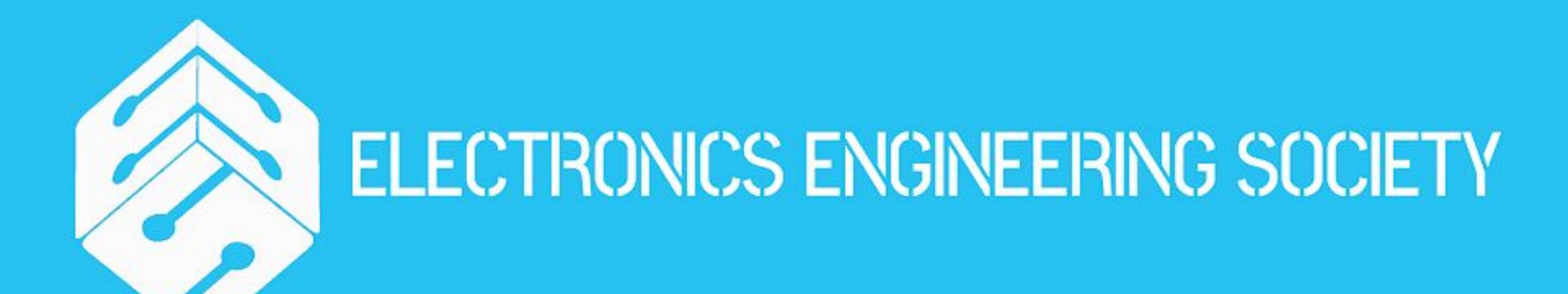


TESTING:

Create a testbench with a clock cycle of 100MHz and test the following sets of inputs-

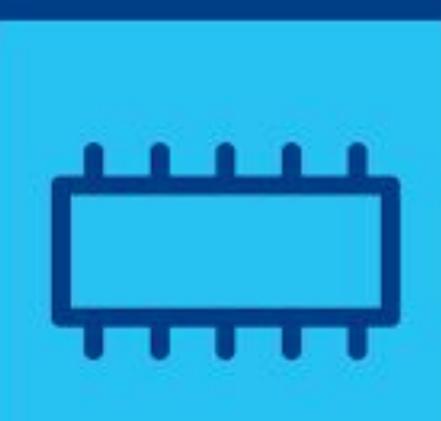
X	y
1111111	11001111
01110110	00101010
11100111	11010101
11000111	11001010
00011100	11110101
11011011	00101011
11110111	11011100
01010101	10011011
10101010	11011010
11001101	1111111

Use \$writememb to write the outputs(corresponding to each set of input) in a text file.



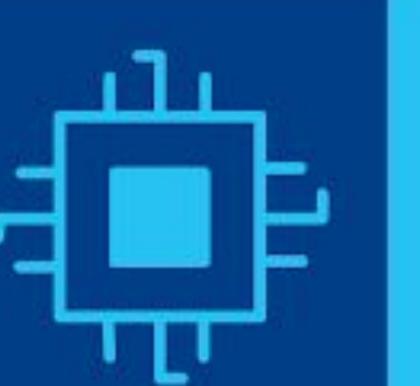














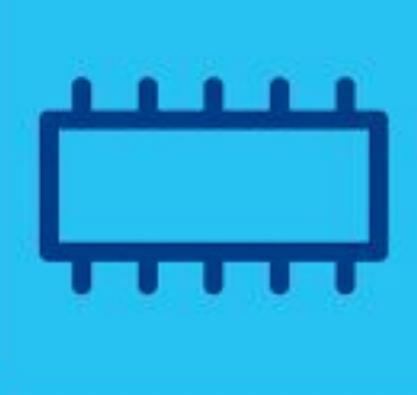






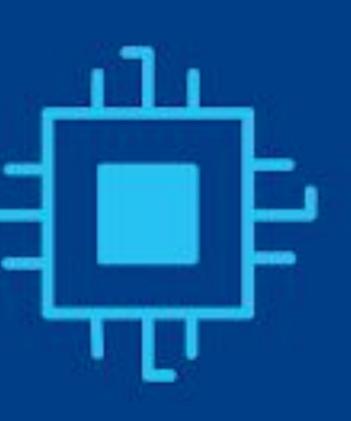


















EVALUATION SCHEME:

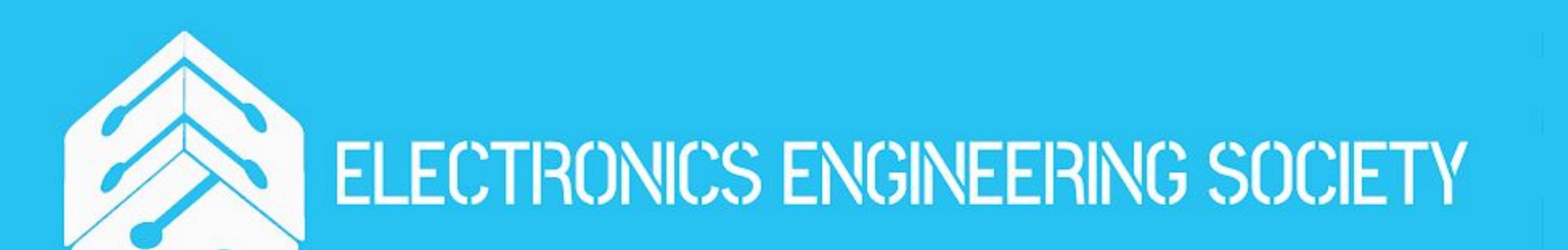
- 1. 10 points for successful implementation of each function.
- 2. 50 additional points for performing at least 9 functions.
- 3. In case of a tie (or complete implementation of all the functions), a design that uses fewer hardware resources will be prioritized.

SUBMISSION:

- 1. Submit the Verilog files of the main design module and the test bench.
- 2. Submit the output text file containing the results of test inputs.
- 3. Submit a pdf file explaining your approach to design the CalC (Simple writeup required, no need of decorating it).

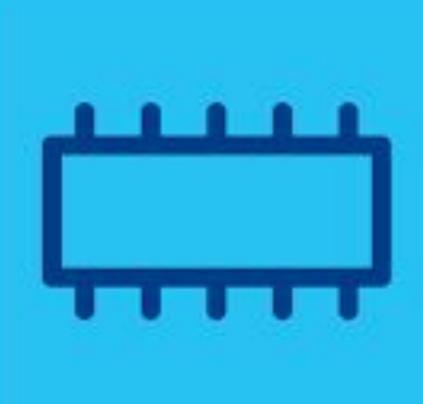
Submission Link-

https://forms.gle/65XAU12595GCyU3k8



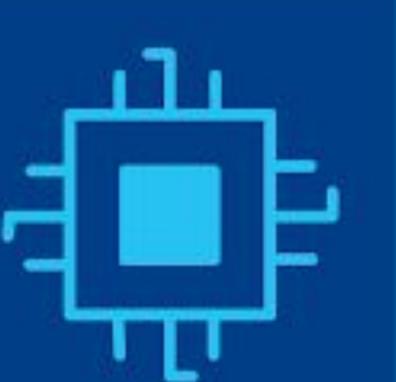














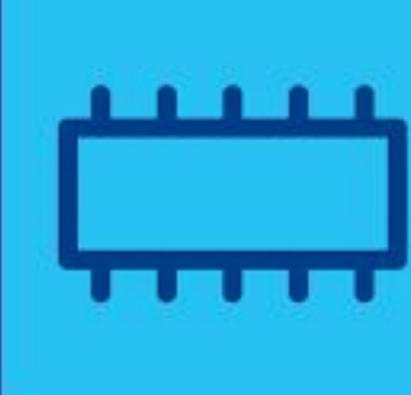






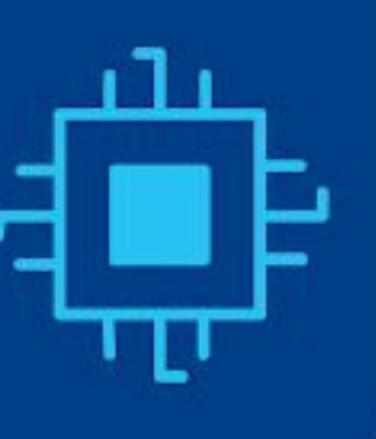


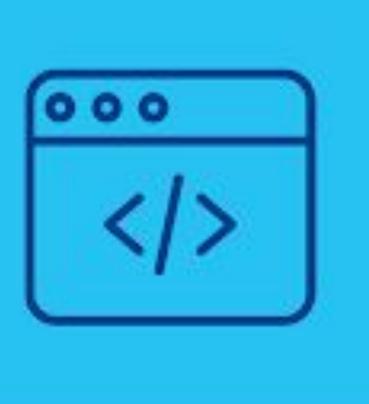




















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