GC032A CSP

1/10’’ VGA CMOS Image Sensor

Datasheet

Rev.1.0

2016-05-24

Ordering Information

◆ **GC032A**

(Colored, 20PIN-csp)

GENERATION REVISION HISTORY

REV.	*EFFECTIVE DATE*	*DESCRIPTION OF CHANGES*	*PREPARED BY*
1.0	*2016-05-24*	*Document Release*	*AE Dept.*

Content

1. Sensor Overview

1.1 General Description

The GC032A features 640H x 480V resolution with 1/10-inch optical format, and 4-transistor pixel structure for high image quality and low noise variations. It delivers superior image quality by powerful on-chip design of a 10-bit ADC, and embedded image signal processor.

The full scale integration of high-performance and low-power functions makes the GC032A best fit the design, reduce implementation process, and extend the battery life of cell phones, PDAs, and a wide variety of mobile applications.

The on-chip ISP provides a very smooth AE (Auto Exposure) and accurate AWB(Auto White Balance) control. It provides various data formats, such as Bayer RGB, RGB565, YCbCr 4:2:2. It has a commonly used two-wire serial interface for host to control the operation of the whole sensor. It's also offer DVP and SPI interface with BB.

1.2 Features

- Standard optical format of 1/10 inch
- Various output formats: YCbCr4:2:2, RGB565, Raw Bayer
- Interface support: DVP, SPI
- Power supply requirement: AVDD28: 2.7~3.0V
  IOVDD: 1.7~3.0V
- Windowing support
- Horizontal/Vertical mirror
- Image processing module
- Package: CSP

1.3 Application

- Cellular Phone Cameras
- Notebook and desktop PC cameras
- PDAs
- Toys
- Digital still cameras and camcorders
- Video telephony and conferencing equipments
- Security systems
- Industrial and environmental systems

1.4 Technical Specifications

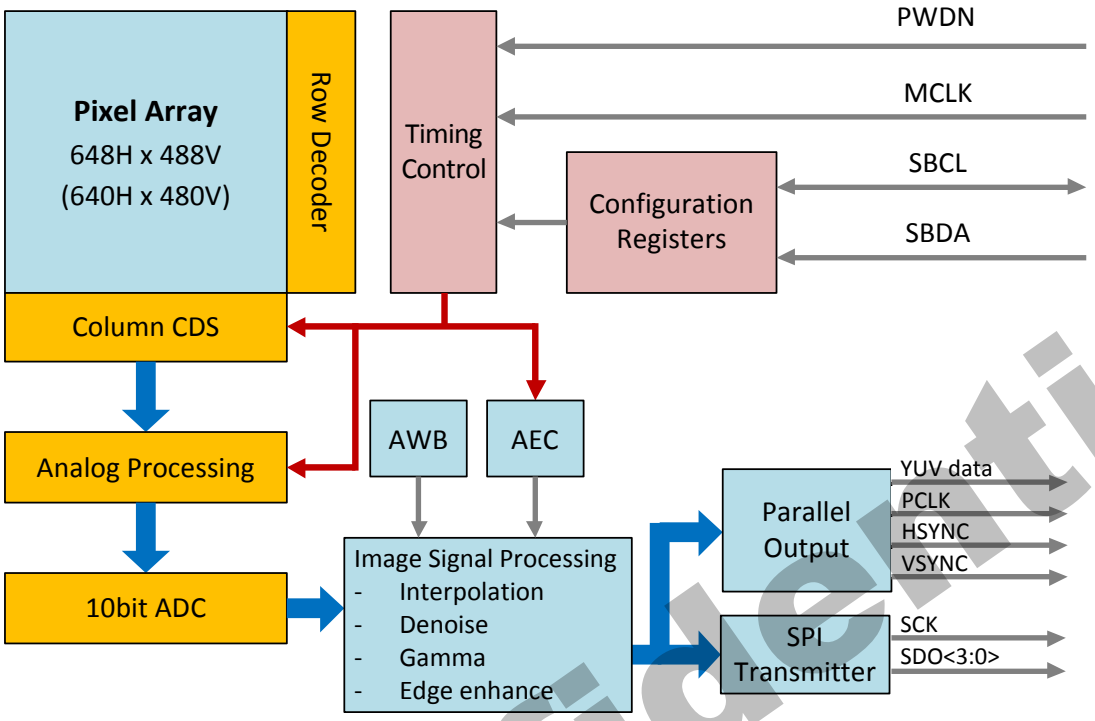
Parameter	Typical value
Optical Format	1/10 inch
Pixel Size	2.2um x 2.2um
Active pixel array	648 x 488
ADC resolution	10 bit ADC
Max Frame rate	30fps@24Mhz,VGA
Power Supply	AVDD28: 2.7~3.0V IOVDD: 1.7~3.0V
Power Consumption	TBD
SNR	TBD
Dark Current	TBD
Sensitivity	TBD
Operating temperature:	-20~70℃
Stable Image temperature	0~50℃
Optimal lens chief ray angle(CRA)	30°(linear)
Package type	CSP

2. DC Characteristics

Symbol		Parameter	Min	Typ	Max	Unit
Supply						
V_{AVDD28}		Power supply	2.7	2.8	3.0	V
V_{IOVDD}		Power Supply(Digital I/O)	1.7	1.8	3.0	V
I_{AVDD28}		Active(operating) current	TBD	TBD	TBD	mA
I_{IOVDD}	1.8V		TBD	TBD	TBD	mA
	2.8V		TBD	TBD	TBD	mA
I_{DDS_PWD}		Standby Current	TBD	TBD	TBD	uA
Digital Input(Typical conditions: AVDD28=2.8V，IOVDD=1.8V)						
V_{IH}		Input voltage HIGH	1.4			V
V_{IL}		Input voltage LOW			0.6	V
Digital Output(Typical conditions: AVDD28=2.8V，IOVDD=1.8V)						
V_{OH}		Output voltage HIGH	1.6			V
V_{OL}		Output voltage LOW			0.2	V

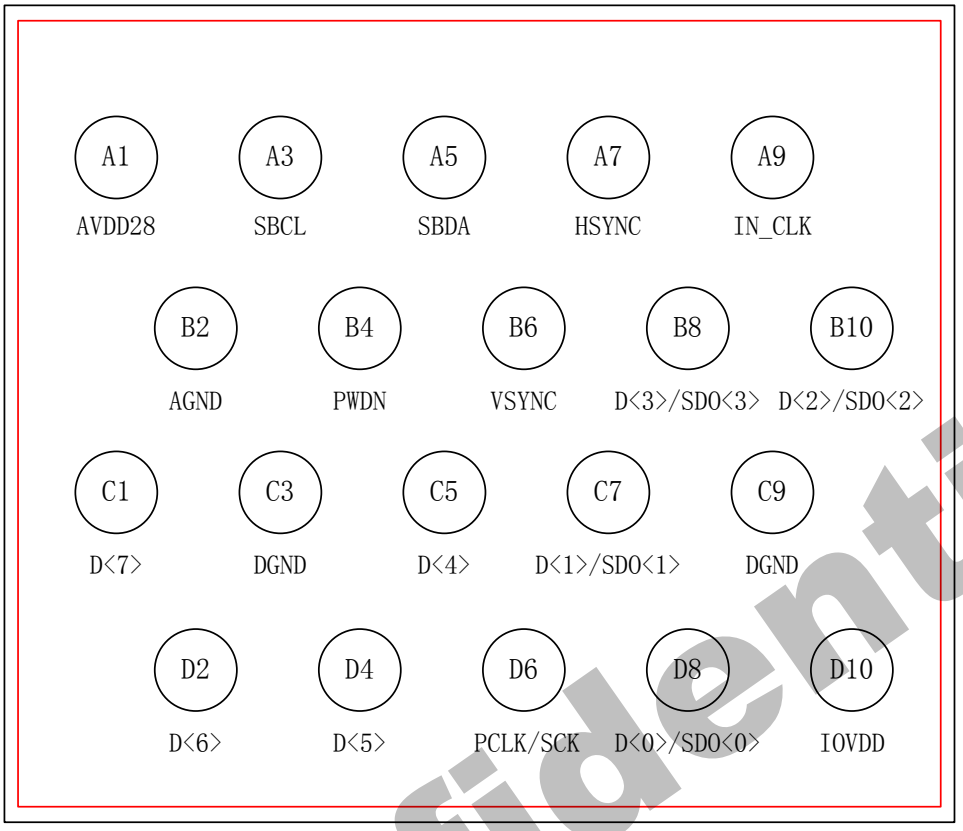
3. Block Diagram

3.1 Block Diagram



GC032A has an active image array of 648x488 pixels. The active pixels are read out progressively through column/row driver circuits. In order to reduce fixed pattern noise, CDS circuits are adopted. The analog signal is transferred to digital signal by 10 bit A/D converter. The digital signals are processed in the ISP Block, including Bayer interpolation, denoise, color correction, gamma correction, data format conversion and so on. Users can easily control these functions via two-wire serial interface bus.

3.2 Pin Diagram



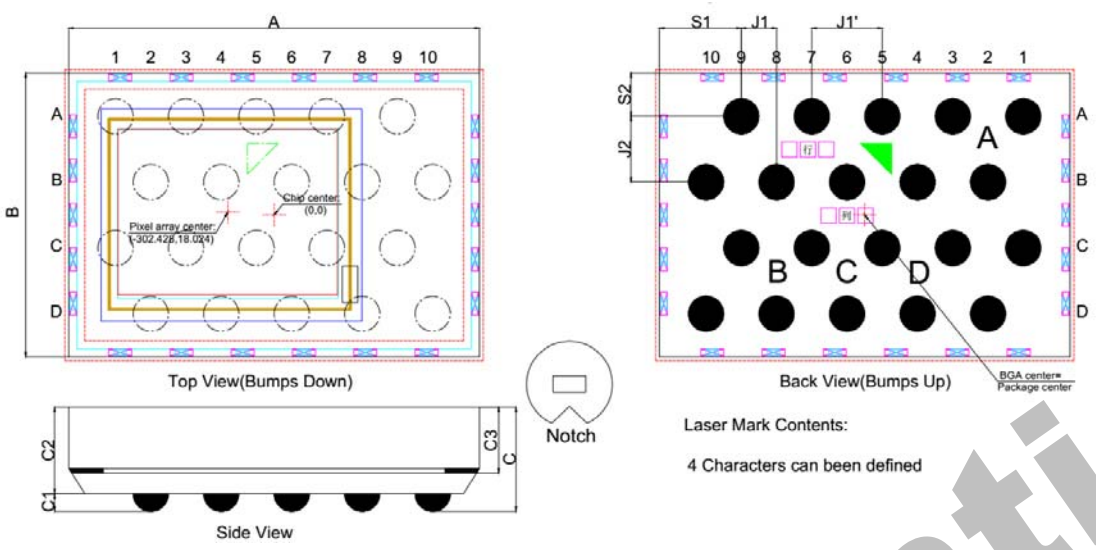
Top View (Bumps Down)

3.3 Signal Descriptions

Pin	Name	Pin Type	Function
A1	**AVDD28**	Power	Main power supply pin, 2.7~3.0V, please connect capacity to ground.
A3	**SBCL**	Input	Two-wire serial bus, clock
A5	**SBDA**	I/O	Two-wire serial bus, data
A7	**HSYNC**	Output	HSYNC output
A9	**IN_CLK**	Input	Main clock
B2	**AGND**	Ground	AGND
B4	**PWDN**	Input	Sensor power down control: 0: normal work 1: standby
B6	**VSYNC**	Output	VSYNC output
B8	**D<3>**	Output	YUV/RGB data output bit[3]
	SDO<3>		SPI data[3]
B10	**D<2>**	Output	YUV/RGB data output bit[2]
	SDO<2>		SPI data[2]
C1	**D<7>**	Output	YUV/RGB data output bit[7]
C3	**DGND**	Ground	DGND

C5	**D<4>**	Output	YUV/RGB data output bit[4]
C7	**D<1>**	Output	YUV/RGB data output bit[1]
	SDO<1>		SPI data[1]
C9	**DGND**	Ground	DGND
D2	**D<6>**	Output	YUV/RGB data output bit[6]
D4	**D<5>**	Output	YUV/RGB data output bit[5]
D6	**PCLK**	Output	Pixel clock output
	SCK		SPI Clock
D8	**D<0>**	Output	YUV/RGB data output bit[0]
	SDO<0>		SPI data[0]
D10	**IOVDD**	Power	Power Supply for I/O circuits, 1.7~3.0V, please connect capacity to ground.

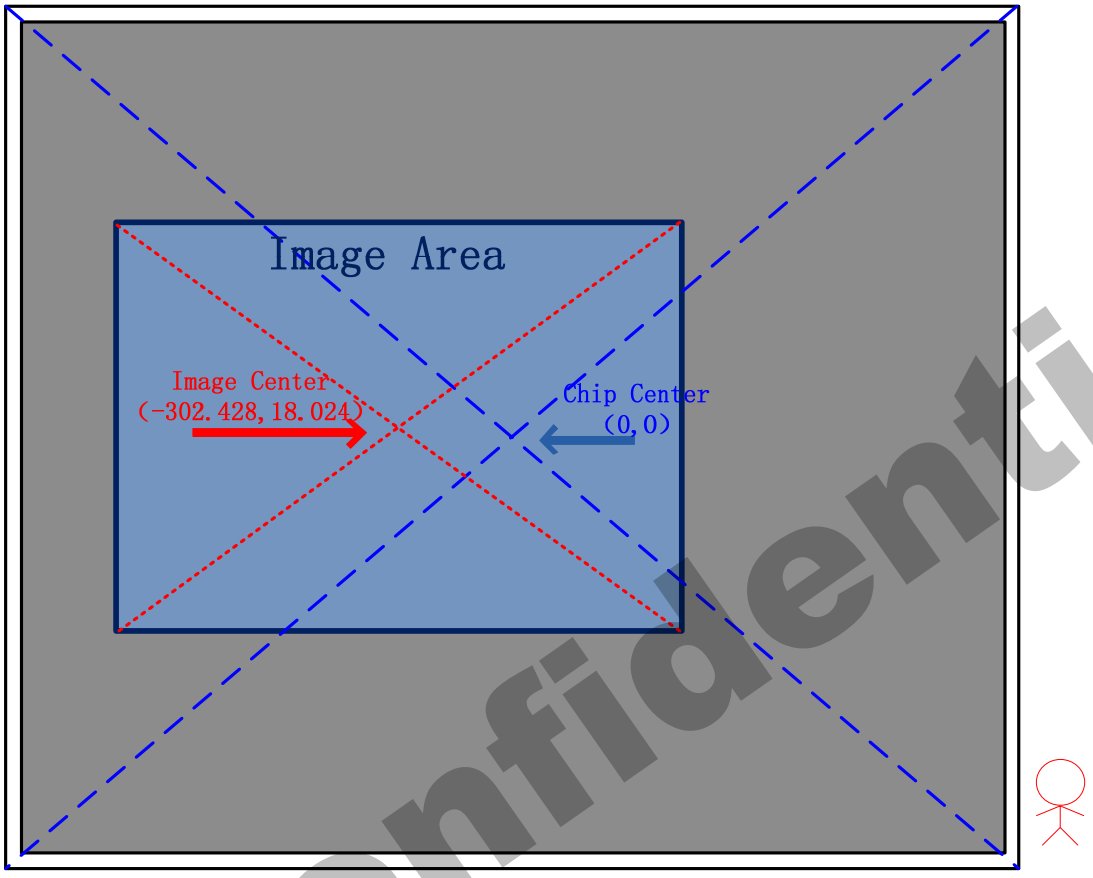
4. Package Specification



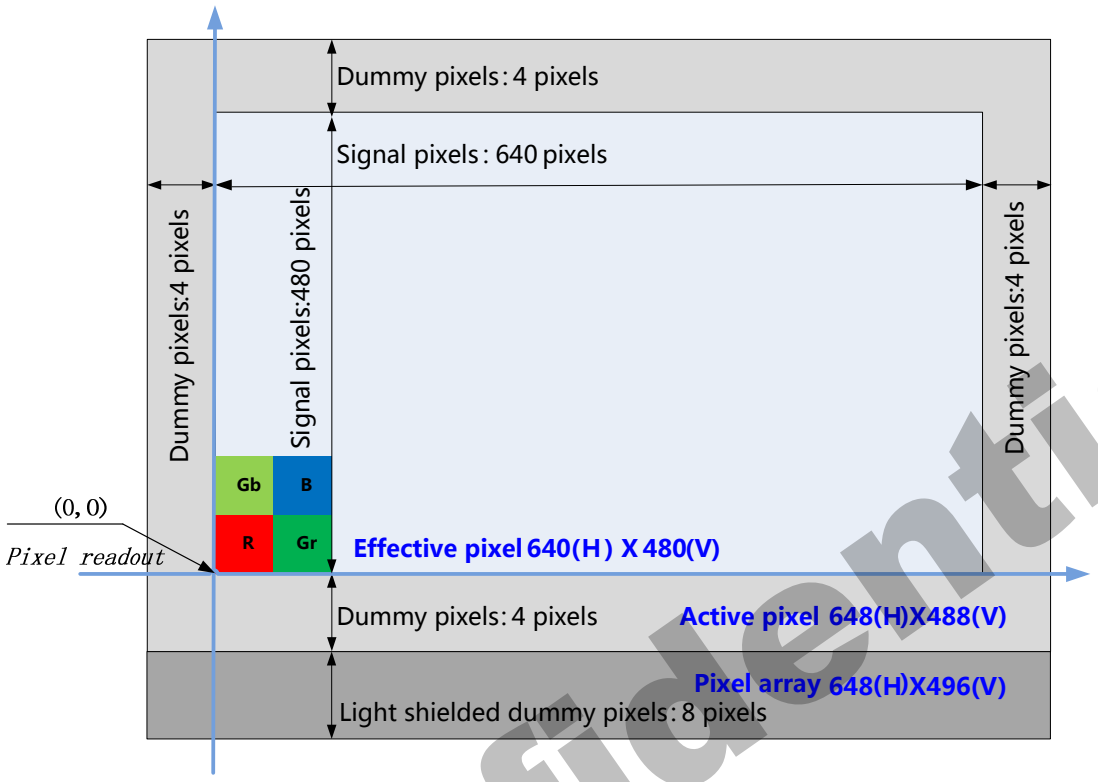
Parameter	Symbol	Nominal	Min.	Max.
		mm		
Package Body Dimension X	A	2.680	2.655	2.705
Package Body Dimension Y	B	1.854	1.829	1.879
Package Height	C	0.680	0.620	0.740
Ball Height	C1	0.120	0.090	0.150
Package Body Thickness	C2	0.560	0.525	0.595
Glass Thickness	C3	0.435	0.415	0.455
Ball Diameter	D	0.230	0.200	0.260
Total Ball Count	N	20		
Pins Pitch X axis	J1/JI’	0.230/ 0.460		
Pins Pitch Y axis	J2	0.430		
Edge to Pin Center Distance along X	S1	0.535	0.505	0.565
Edge to Pin Center Distance along Y	S2	0.282	0.252	0.312

5. Optical Specifications

5.1 Sensor Array Center



5.2 Pixel Array

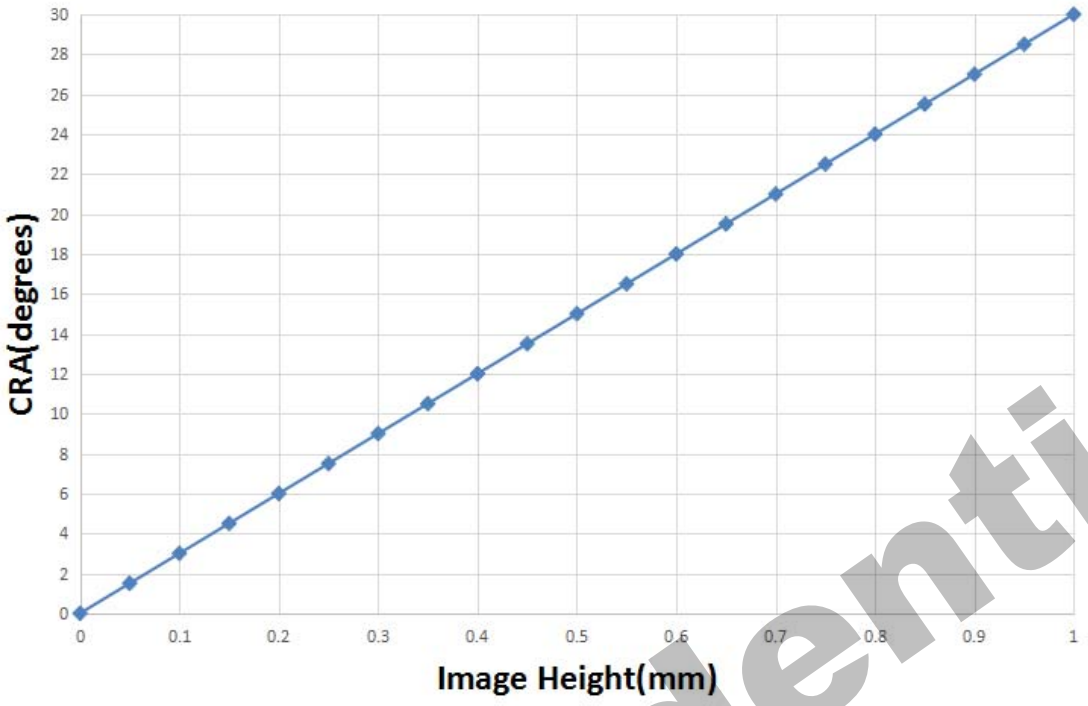


Pixel array is covered by Bayer pattern color filters. The primary color BG/GR array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 647. If flip in column, column is read out from 647 to 0.

If no flip in row, row is read out from 0 to 487. If flip in row, row is read out from 487 to 0.

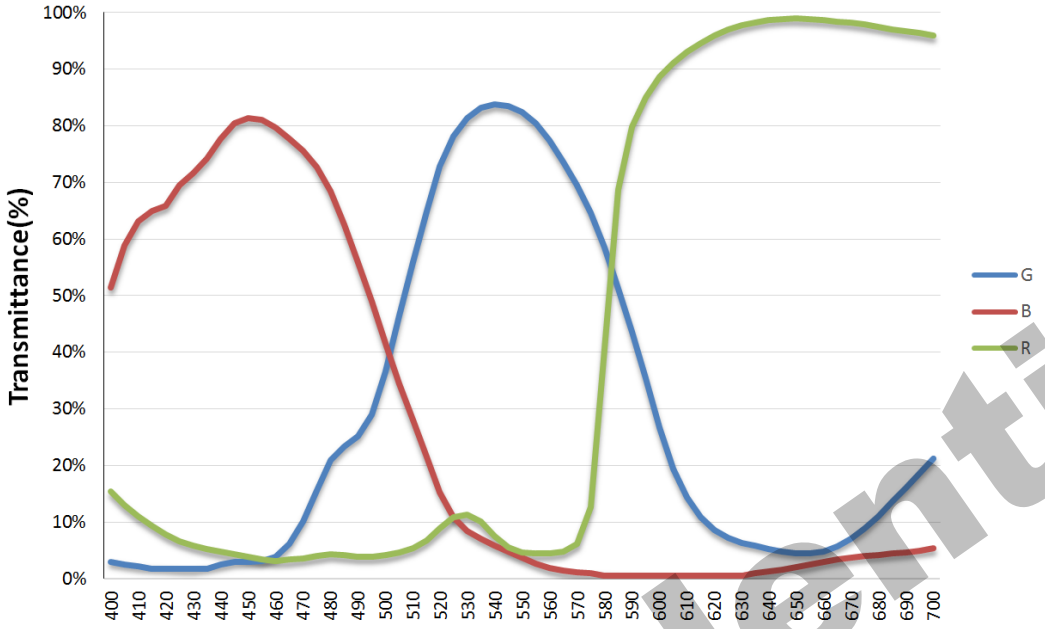
5.3 Lens Chief Ray Angle (CRA)



Field(%)	Image Height(mm)	CRA(degrees)
0	0	0.0
5	0.0442	1.5
10	0.0884	3.0
15	0.1326	4.5
20	0.1768	6.0
25	0.221	7.5
30	0.2652	9.0
35	0.3094	10.5
40	0.3536	12.0
45	0.3978	13.5
50	0.442	15.0
55	0.4862	16.5
60	0.5304	18.0
65	0.5746	19.5
70	0.6188	21.0
75	0.663	22.5
80	0.7072	24.0
85	0.7514	25.5
90	0.7956	27.0
95	0.8398	28.5
100	0.884	30.0

5.4 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below:



6. Two-wire Serial Bus Communication

GC032A Device Address:

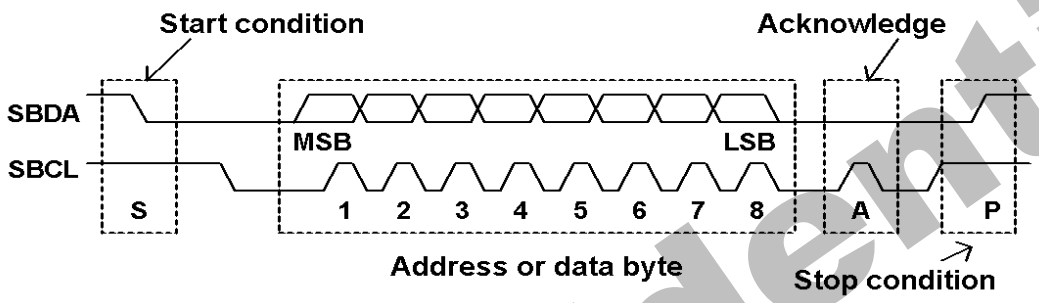
serial bus write address = 0x42, serial bus read address = 0x43

6.1 Protocol

The host must perform the role of a communications master and GC032A acts as either a slave receiver or transmitter. The master must do

◆Generate the **Start(S)/Stop(P)** condition

◆Provide the serial clock on **SBCL**.



Single Register Writing:

S	42H	A	Register Address	A	Data	A	P

Incremental Register Writing:

S	42H	A	Register Address	A	Data(1)	A	……	Data(N)	A	P

Single Register Reading:

S	42H	A	Register Address	A	S	43H	A	Data	NA	P

Notes:

From master to slave From slave to master

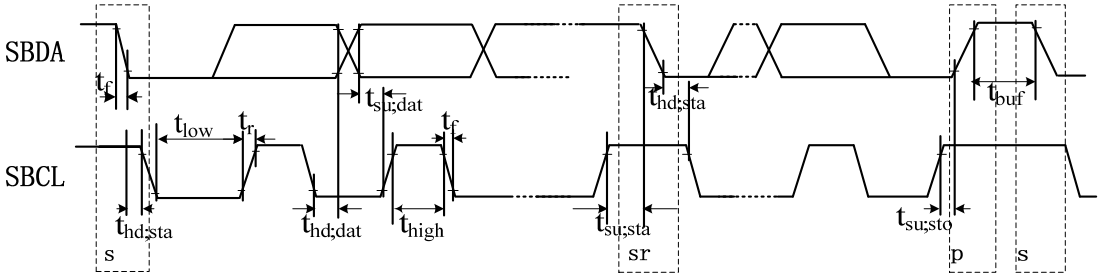
S: Start condition **P:** Stop condition

A: Acknowledge bit **NA:** No acknowledge

Register Address: Sensor register address

Data: Sensor register value

6.2 Serial Bus Timing

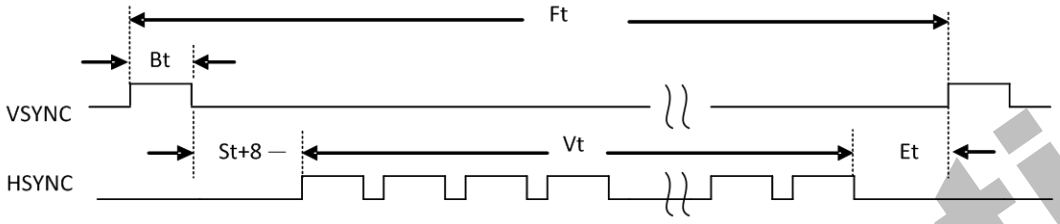


Parameter	Symbol	Min.	Typ.	Max.	Unit
SBCL clock frequency	F_{scl}	0	--	400	KHz
Bus free time between stop and start condition	t_{buf}	1.3	--	--	μs
Hold time for a repeated start	$t_{hd;sta}$	0.6	--	--	μs
LOW period of SBCL	t_{low}	1.3	--	--	μs
HIGH period of SBCL	t_{high}	0.6	--	--	μs
Set-up time for a repeated start	$t_{su;sta}$	0.6	--	--	μs
Data hold time	$t_{hd;dat}$	0	--	0.9	μs
Data Set-up time	$t_{su;dat}$	100	--	--	ns
Rise time of SBCL, SBDA	t_r	--	--	300	ns
Fall time of SBCL, SBDA	t_f	--	--	300	ns
Set-up time for a stop	$t_{su;sto}$	0.6	--	--	μs
Capacitive load of bus line (SBCL, SBDA)	C_b	--	--	--	pf

7. Application

7.1 Timing

Suppose Vsync is low active and Hsync is high active, and output format is YCbCr/RGB565, then the timing of Vsync and Hsync is bellowing (take capture mode for example，preview mode is the same):



Ft =VB+ Vt +8 (unit is row_time)

VB = Bt + St + Et, Vblank/Dummy line, setting by register P0:0x07 and P0:0x08.

Ft -> Frame time, one frame time.

Bt -> Blank time, Vsync no active time.

St -> Start time, setting by register P0:0x12.

Et –> End time, setting by register P0:0x13.

Vt -> valid line time. VGA is 480, Vt = win_height-8, win_height is setting by register P0:0x0d and P0:0x0e.

When exp_time ≤ win_height+VB, Bt = VB – St - Et. Frame rate is controlled by window_height + VB.

When exp_time > win_height + VB, Bt = exp_time - win_height – St - Et. Frame rate is controlled by exp_time.

The following is row_time calculate:

row_time = Hb + Sh_delay + win_width + 4.

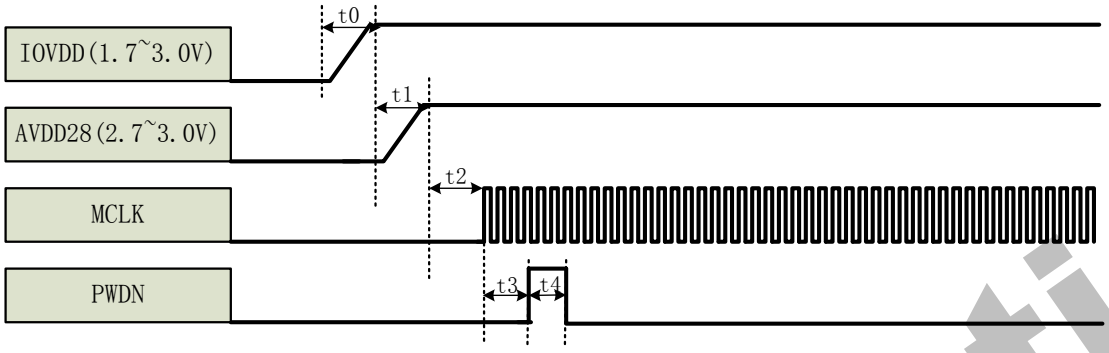
Hb –> HBlank or dummy pixel，Setting by register P0:0x05 and P0:0x06.

Sh_delay -> Setting by register P0:0x11.

win_width -> Setting by register P0:0x0f and P0:0x10, win_width = final_output_width + 8. So for VGA, we should set win_width as 648.

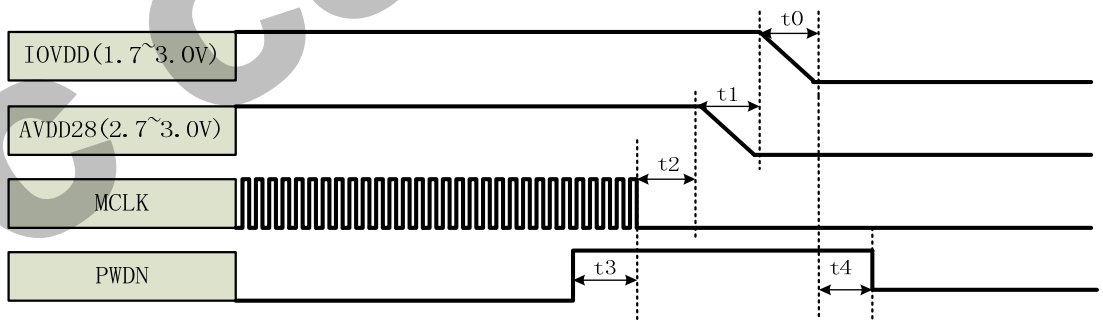
8. Power On/Off Sequence

8.1 Power On Sequence



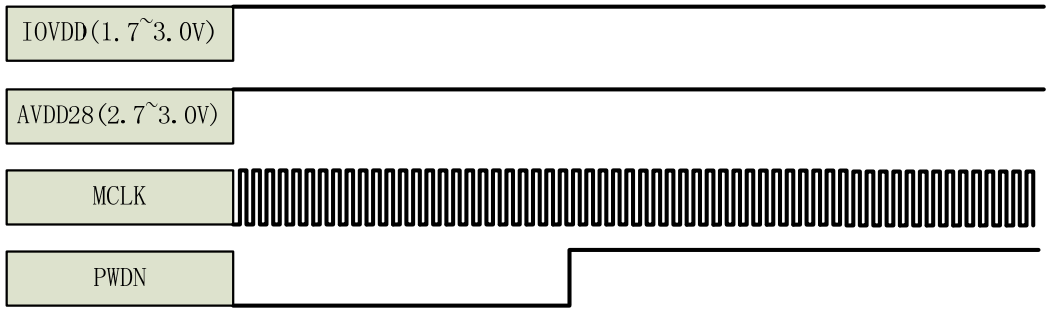
Parameter	Description	Min.	Max.	Unit
t0	IOVDD rising time	50		us
t1	From IOVDD to AVDD28	≥0		us
t2	From AVDD28 to MCLK applied	≥0		us
t3	From MCLK applied to PWDN pull high	≥0		us
t4	PWDN from pull high to pull low	>1		us

8.2 Power Off Sequence



Parameter	Description	Min.	Max.	Unit
t0	From AVDD28 to IOVDD falling time	≥0		us
t1	AVDD28 falling time	≥0		us
t2	From MCLK disable to sensor AVDD28 power down	≥0		us
t3	From sensor disable to MCLK disable	≥0		us
t4	From power off to PWDN pull low	≥0		us

8.3 Standby Sequence



- **Recommended power on/off sequence is above.**
- **If you have special requirements in application, please contact with us to confirm.**

9. Register List

System Register

Address	Name	Width	Default Value	R/W	Description
0xf0	**Sensor_ID_high**	**8**	**0x23**	**RO**	**Sensor_ID high**
0xf1	**Sensor_ID_low**	**8**	**0x2a**	**RO**	**Sensor_ID low**
0xf2	pad_vb_hiz_mode oen_flop_mode	8	0x01	RW	[3] pad_vb_hiz_mode [0] oen_flop_mode
0xf3	sync_output_en data_output_en	8	0x00	RW	[7:5] sync_output_en [7] pclk_en [6] hsync_en [5] vsync_en [4:0] data_output_en
0xf4	I2C_open_en up_dn pwd_dn	5	0x00	RW	[4] I2C_open_en [3:2] up_dn 00: not pull 01: pull down 10: pull up 11: illegal [1] NA [0] PWD dn 0: pull down 1: not pull
0xf5	spi_pad_mode sck_delay_mode	3	0x00	RW	[3] SPI pad mode [2:0] sck_delay_mode
0xf6	sync_hiz data_hiz	8	0x00	RW	[7:5] sync_hiz [4:0] data_hiz
0xf7	PLL_mode1	8	0x00	RW	[6:4] serial_clk_div [1] div2en [0] pll_en
0xf8	PLL_mode2	8	0x00	RW	[7] freq_div2_en [6] freq_div2_close frame mode [5:0] divx4
0xf9	cm_mode	8	0x00	RW	[7] regf clk enable [6] mipi clk div [5] clk div sel [4] NA [3] isp all clock enable

					[2] serial_clk_enable [1] re_lock_pll [0] not_use_pll
0xfa	isp_div_mode	8	0x00	RW	[7:4] +1 represent the frequency division number [3:0] represent the high level in one pulse after frequency division
0xfb	I2c_device_id	8	0x42	RO	[7:1] i2c_device_id, can write once [0] NA
0xfc	analog_pwc	8	0x03	RW	[7:6] mp18_r [5:4] da18_r [3] mp18_en [2] NA [1] da18_en [0] apwd
0xfd	isp_div_mode2	8	0x11	RW	[7:4] +1 represent the frequency division number [3:0] represent the high level in one pulse after frequency division
0xfe	Reset related	8	0x00	RW	[7] soft_reset [6] cm_rst [5] SPI_rst [4] CISCTL_rst [3] PLL_rst [2:0] page_select 000: registers in REGF0 001: registers in REGF1 010: registers in REGF2 011: registers in REGF3

Analog & CISCTL

Address	Name	Width	Default Value	R/W	Description
P0:0x03	Exposure _high	4	0x00	RW	[3:0] Exposure [11:8]
P0:0x04	Exposure _low	8	0x10	RW	[7:0] Exposure [7:0]
P0:0x05	HB_high	4	0x01	RW	[3:0] HB[11:8]
P0:0x06	HB_low	8	0xa4	RW	[7:0] HB[7:0]
P0:0x07	VB_high	4	0x00	RW	[3:0] VB[11:8]
P0:0x08	VB_low	8	0x0a	RW	[7:0] VB[7:0]
P0:0x09	Row_start_high	1	0x00	RW	[0] Row_start[8]
P0:0x0a	Row_start_low	8	0x00	RW	[7:0] Row_start[7:0]

P0:0x0b	Column_start_high	2	0x00	RW	[1:0] Column _start[9:8]
P0:0x0c	Column_start_low	8	0x00	RW	[7:0] Column _start[7:0]
P0:0x0d	window_height_high	1	0x01	RW	[0] window_height [8]
P0:0x0e	window_height_low	8	0xe8	RW	[7:0] window_height [7:0]
P0:0x0f	window_width_high	2	0x02	RW	[1:0] window_width [9:8]
P0:0x10	window_width_low	8	0x8c	RW	[7:0] window_width [7:0]
P0:0x11	sh_delay	8	0x2a	RW	sh_delay
P0:0x12	vs_st	8	0x09	RW	vs_st
P0:0x13	vs_et	8	0x04	RW	vs_et
P0:0x17	CISCTL_mode1	7	0x00	RW	[7:2] Reserved [1] updown [0] mirror

BLK

Address	Name	Width	Default Value	R/W	Description
P2:0x40	Blk_mode1	8	0x23	RW	[7:2] Reserved [1] dark_current_en [0] offset_en
P2:0x44	global_offset	8	0x00	RW	[7:0]global_offset
P2:0x45	exp_rate_darkc	8	0x04	RW	[7:0]exp_rate_darkc
P2:0x46	offset_ratio_G1	6	0x10	RW	[5:0]offset_ratio_G1
P2:0x49	dark_current_ratio_G1	6	0x10	RW	[5:0]dark_current_ratio_G1
P2:0x4d	manual_G1_offset manual_R1_offset	8	0x00	RW	[7:4] manual_G1_offset [3:0] manual_R1_offset
P2:0x4e	manual_B2_offset manual_G2_offset	8	0x00	RW	[7:4] manual_B2_offset [3:0] manual_G2_offset

ISP Related

Address	Name	Width	Default Value	R/W	Description
P0:0x40	Block_enable_1	8	0xff	RW	[7:6] Reserved [5] CC_en [4] EE_en [3] INTP_en [2] DN_en [1] DD_en [0] LSC_en
P0:0x42	AAAA_enable	8	0xcf	RW	[7:2] Reserved [1] AWB enable [0] Reserved
P0:0x43	special_effect	7	0x00	RW	[7:4] Reserved [3:2] only_edge_map [1] CrCb_ fixed_en [0] inverse color
P0:0x46	sync_mode	8	0x0f	RW	[7] data delay half [6] hsync delay half [5] odd_even_col_switch [4] odd_even_row_switch [3] opclk gated in HB [2] opclk polarity [1] hsync polarity [0] vsync polarity
P0:0x48	gain_code	8	0x00	RW	[3:0] gain_code
P0:0x4c	debug_mode2	8	0x00	RW	[7:4] Reserved [3] OUT_test_image [2] input_test_image [1] LSC_test_image [0] test_image after EEINTP
P0:0x50	win_mode	1	0x01	RW	[0] Crop out Window mode
P0:0x51	out_win_y1_high	1	0x00	RW	[0] out_win_y1[8]
P0:0x52	out_win_y1_low	8	0x00	RW	[7:0] out _win_y1[7:0]
P0:0x53	out_win_x1_high	2	0x00	RW	[1:0] out_win_x1[9:8]
P0:0x54	out_win_x1_low	8	0x00	RW	[7:0] out_win_x1[7:0]
P0:0x55	out_win_height	1	0x01	RW	[0] out window height[8]

	_high				
P0:0x56	out_win_height _low	8	0xe0	RW	[7:0] 0ut window height[7:0]
P0:0x57	out win_width _high	2	0x02	RW	[1:0] out window width[9:8]
P0:0x58	out win_width _low	8	0x80	RW	[7:0] out window width[7:0]

AUTO GAMMA

Address	Name	Width	Default Value	R/W	Description
P0:0x5a	Y_Gamma_1	8	0x09	RW	At point 2
P0:0x5b	Y_Gamma_2	8	0x14	RW	At point 4
P0:0x5c	Y_Gamma_3	8	0x19	RW	At point 6
P0:0x5d	Y_Gamma_4	8	0x1f	RW	At point 8
P0:0x5e	Y_Gamma_5	8	0x26	RW	At point 12
P0:0x5f	Y_Gamma_6	8	0x32	RW	At point 16
P0:0x60	Y_Gamma_7	8	0x45	RW	At point 20
P0:0x61	Y_Gamma_8	8	0x53	RW	At point 24
P0:0x62	Y_Gamma_9	8	0x69	RW	At point 32
P0:0x63	Y_Gamma_10	8	0x7d	RW	At point 40
P0:0x64	Y_Gamma_11	8	0x8f	RW	At point 48
P0:0x65	Y_Gamma_12	8	0x9d	RW	At point 56
P0:0x66	Y_Gamma_13	8	0xa9	RW	At point 64
P0:0x67	Y_Gamma_14	8	0xbd	RW	At point 80
P0:0x68	Y_Gamma_15	8	0xcd	RW	At point 96
P0:0x69	Y_Gamma_16	8	0xd9	RW	At point 112
P0:0x6a	Y_Gamma_17	8	0xe3	RW	At point 128
P0:0x6b	Y_Gamma_18	8	0xea	RW	At point 144
P0:0x6c	Y_Gamma_19	8	0xef	RW	At point 160
P0:0x6d	Y_Gamma_20	8	0xf5	RW	At point 192
P0:0x6e	Y_Gamma_21	8	0xf9	RW	At point 224
P0:0x6f	Y_Gamma_22	8	0xff	RW	At point 256

GLOBAL/PRE/POSTGAIN

Address	Name	Width	Default Value	R/W	Description
P0:0x70	Global_gain	8	0x70	RW	Global gain
P0:0x71	Auto_pregain	8	0x20	RW	Auto_pregain

P0:0x72	Auto_postgain	8	0x40	RW	Auto_postgain
P0:0x73	Channel_gain_R	8	0x80	RW	Channel_gain_R
P0:0x74	Channel_gain_G1	8	0x80	RW	Channel_gain_G1
P0:0x75	Channel_gain_G2	8	0x80	RW	Channel_gain_G2
P0:0x76	Channel_gain_B	8	0x80	RW	Channel_gain_B
P0:0x77	AWB_R_gain_low	8	0x64	RW	AWB_R_gain[7:0]
P0:0x78	AWB_G_gain_low	8	0x40	RW	AWB_G_gain[7:0]
P0:0x79	AWB_B_gain_low	8	0x60	RW	AWB_B_gain[7:0]
P0:0x4e	AWB_R_gain_high AWB_G_gain_high AWB_B_gain_high	3	0x00	RW	[2]AWB_R_gain[8] [1]AWB_G_gain[8] [0]AWB_B_gain[8]
P0:0x7a	R_ratio	8	0x80	RW	R_ratio
P0:0x7b	G_ratio	8	0x80	RW	G_ratio
P0:0x7c	B_ratio	8	0x80	RW	B_ratio

DNDD/DITHER

Address	Name	Width	Default Value	R/W	Description
P0:0x82	DN_signal_a	6	0x1a	RW	DN_signal_a
P0:0x83	DN_signal_b	7	0x0b	RW	DN_signal_b
P0:0x8c	DD_signal_a	6	0x08	RW	DD_signal_a
P0:0x8d	DD_signal_b	7	0x10	RW	DD_signal_b

INTPEE （Interpolation and Edge Enhancement）

Address	Name	Width	Default Value	R/W	Description
P0:0x95	edge1 effect edge2 effect	8	0x32	RW	[7:4] edge1 effect [3:0] edge2 effect

Y gamma

Address	Name	Width	Default Value	R/W	Description
P0:0xba	Gamma_1	8	0x10	RW	At input 2
P0:0xbb	Gamma_2	8	0x12	RW	At input 4
P0:0xbc	Gamma_3	8	0x16	RW	At input 6
P0:0xbd	Gamma_4	8	0x1b	RW	At input 8
P0:0xbe	Gamma_5	8	0x29	RW	At input 12
P0:0xbf	Gamma_6	8	0x37	RW	At input 16
P0:0xc0	Gamma_7	8	0x46	RW	At input 20
P0:0xc1	Gamma_8	8	0x54	RW	At input 24
P0:0xc2	Gamma_9	8	0x6b	RW	At input 32
P0:0xc3	Gamma_10	8	0x79	RW	At input 40
P0:0xc4	Gamma_11	8	0x85	RW	At input 48
P0:0xc5	Gamma_12	8	0x90	RW	At input 56
P0:0xc6	Gamma_13	8	0x9a	RW	At input 64
P0:0xc7	Gamma_14	8	0xaa	RW	At input 80
P0:0xc8	Gamma_15	8	0xb8	RW	At input 96
P0:0xc9	Gamma_16	8	0xc3	RW	At input 112
P0:0xca	Gamma_17	8	0xcc	RW	At input 128
P0:0xcb	Gamma_18	8	0xd3	RW	At input 144
P0:0xcc	Gamma_19	8	0xdb	RW	At input 160
P0:0xcd	Gamma_20	8	0xe9	RW	At input 192
P0:0xce	Gamma_21	8	0xf6	RW	At input 224
P0:0xcf	Gamma_22	8	0xff	RW	At input 256

YCP

Address	Name	Width	Default Value	R/W	Description
P0:0xd0	Global saturation	8	0x40	RW	Global saturatio
P0:0xd1	saturation_Cb	8	0x36	RW	Cb saturation
P0:0xd2	saturation_Cr	8	0x36	RW	Cr saturation
P0:0xd3	luma_contrast	8	0x3d	RW	Luma_contrast
P0:0xd4	Contrast_center	8	0x80	RW	Contrast center value
P0:0xd5	Luma_offset	8	0x00	RW	Add offset on luma value.
P0:0xda	Fixed_Cb	8	0x00	RW	Fixed_Cb
P0:0xdb	Fixed_Cr	8	0x00	RW	Fixed_Cr

AEC

Address	Name	Width	Default	R/W	Description

			Value		
P0:0x4f	AEC_en	1	0x00	RW	[0] AEC enable
P1:0x05	AEC_center_x1	8	0x30	RW	[7:0] AEC_center_x1, X4
P1:0x06	AEC_center_x2	8	0x75	RW	[7:0] AEC_center_x2, X4
P1:0x07	AEC_center_y1	8	0x40	RW	[7:0] AEC_center_y1, X2
P1:0x08	AEC_center_y2	8	0xb0	RW	[7:0] AEC_center_y2, X2
P1:0x1f	AEC_max_pre_dg_gain	8	0x20	RW	AEC_max_pre_dg_gain,
P1:0x20	AEC_max_post_dg_gain	8	0x40	RW	AEC_max_post_dg_gain
P1:0x25	AEC_anti_flicker_step[11:8]	4	0x00	RW	[7:4] NA [3:0] AEC anti flicker step[11:8]
P1:0x26	AEC_anti_flicker_step[7:0]	8	0x6a	RW	AEC anti flicker step[7:0]
P1:0x27	AEC_exp_level_1[11:8]	4	0x02	RW	[7:4] NA [3:0] AEC exp level1[11:8]
P1:0x28	AEC_exp_level_1[7:0]	8	0x12	RW	AEC exp level1[7:0]
P1:0x29	AEC_exp_level_2[11:8]	4	0x03	RW	[7:4] NA [3:0] AEC exp level2[11:8]
P1:0x2a	AEC_exp_level_2[7:0]	8	0x50	RW	AEC exp level2[7:0]
P1:0x2b	AEC_exp_level_3[11:8]	4	0x05	RW	[7:4] NA [3:0] AEC exp level3[11:8]
P1:0x2c	AEC_exp_level_3[7:0]	8	0xcc	RW	AEC exp level_3[7:0]
P1:0x2d	AEC_exp_level_4[11:8]	4	0x07	RW	[7:4] NA [3:0] AEC exp level 4[11:8]
P1:0x2e	AEC_exp_level_4[7:0]	8	0x74	RW	AEC exp level 4 [7:0]
P1:0x2f	AEC_exp_level_5[11:8]	4	0x09	RW	[7:4] NA [3:0] AEC exp level 5[11:8]
P1:0x30	AEC_exp_level_5[7:0]	8	0x1c	RW	AEC exp level 5 [7:0]
P1:0x31	AEC_exp_level_6[11:8]	4	0x0c	RW	[7:4] NA [3:0] AEC exp level 6[11:8]
P1:0x32	AEC_exp_level_6[7:0]	8	0x20	RW	AEC exp level 6[7:0]
P1:0x33	AEC_exp_level_7[11:8]	4	0x0d	RW	[7:4] NA [3:0] AEC exp level7[11:8]
P1:0x34	AEC_exp_level_7[7:0]	8	0x40	RW	AEC exp level 7[7:0]

P1:0x35	AEC_max_dg_gain1	8	0x40	RW	5.3bits, AEC max dg gain1,x16
P1:0x36	AEC_max_dg_gain2	8	0x40	RW	5.3bits, AEC max dg gain2,x8
P1:0x37	AEC_max_dg_gain3	8	0x40	RW	5.3bits, AEC max dg gain3,x8
P!:0x38	AEC_max_dg_gain4	8	0x40	RW	5.3bits, AEC max dg gain4,x8
P1:0x39	AEC_max_dg_gain5	8	0x40	RW	5.3bits, AEC max dg gain5,x8
P1:0x3a	AEC_max_dg_gain6	8	0x40	RW	5.3bits, AEC max dg gain6,x8
P1:0x3b	AEC_max_dg_gain7	8	0x40	RW	5.3bits, AEC max dg gain7,x8
P1:0x3c	AEC_max_exp_level AEC_exp_min_l[11:8]	6	0x20	RW	[5:4] Max level setting [3:0] exp min[11:8]
P1:0x3d	AEC_exp_min_l[7:0]	8	0x04	RW	AEC_exp_min_l[7:0]

AWB

Address	Name	Width	Default Value	R/W	Description
P1:0x76	AWB_R_gain_limit	8	0x80	RW	Channel gain limit for R, G, B.
P1:0x77	AWB_G_gain_limit	8	0x2c	RW	
P1:0x78	AWB_B_gain_limit	8	0xaf	RW	
P1:0x79	AWB_R_gain_out_h_limit	8	0x75	RW	outdoor R high limit
P1:0x7a	AWB_G_gain_out_h_limit	8	0x40	RW	outdoor G high limit
P1:0x7b	AWB_B_gain_out_h_limit	8	0x50	RW	outdoor B high limit

LSC

Address	Name	Width	Default Value	R/W	Description

P1:0xc1	LSC_row_center	7	0x3c	RW	LSC row center
P1:0xc2	LSC_col_center	8	0x50	RW	LSC col center
P1:0xc3	LSC_dark_dec_mode LSC_dark_pixel_select_mode LSC_b4_sign	3	0x00	RW	[2] LSC_dark_dec_mode [1] LSC_dark_pixel_select_mode [0] sign of b4
P1:0xc4	LSC_red_b2	8	0x50	RW	b2 for channel red
P1:0xc5	LSC_green_b2	8	0x34	RW	b2 for channel green
P1:0xc6	LSC_blue_b2	8	0x32	RW	b2 for channel blue
P1:0xc7	LSC_red_b4	8	0x14	RW	b4 for channel red
P1:0xc8	LSC_green_b4	8	0x00	RW	b4 for channel green
P1:0xc9	LSC_blue_b4	8	0x10	RW	b4 for channel blue
P1:0xca	LSC_Y_dark_th	8	0x20	RW	LSC_Y_dark_th
P1:0xcb	LSC_Y_dark_slope	8	0x10	RW	LSC_Y_dark_slope

AUTO_CC

Address	Name	Width	Default Value	R/W	Description
P1:0xd0	CC_CT1_11	8	0x40	RW	CC_CT1
P1:0xd1	CC_CT1_12	8	0xfa	RW	
P1:0xd2	CC_CT1_13	8	0x01	RW	
P1:0xd3	CC_CT1_21	8	0xfa	RW	
P1:0xd4	CC_CT1_22	8	0x40	RW	
P1:0xd5	CC_CT1_23	8	0xfb	RW	
P1:0xd6	CC_CT2_11	8	0x36	RW	CC_CT2
P1:0xd7	CC_CT2_12	8	0x00	RW	
P1:0xd8	CC_CT2_13	8	0x02	RW	
P1:0xd9	CC_CT2_21	8	0x08	RW	
P1:0xda	CC_CT2_22	8	0x38	RW	
P1:0xdb	CC_CT2_23	8	0xfe	RW	

CSI/PHY1.0

Address	Name	Width	Default Value	R/W	Description
P3:0x6a	fifo_prog_full_level	7	0x01	RW	[6:0]fifo_prog_full_level
P3:0x5f	fifo_error log	1	--	RW	[0]

					W:clear fifo error R: fifo error valid

SPI

Address	Name	Width	Default Value	R/W	Description
P3:0x51	spi_mode_buf	1	0x00	RW	[0] spi_enable
P3:0x52	spi_global_mode	8	0xd8	RW	[7] msb_first [6] read_gate_mode [5] ddr_mode [4] write_gate_mode [3] clk gate [2] fifo rst mode [1] CPHA [0] CPOL
P3:0x53	spi_data_mode	8	0x20	RW	[7] add CRC [6] line number mode [5] add_sync_sign [4] data_idle_status [3:2] data_bandwidth [1:0] data_sequnce
P3:0x54	spi_master_mode	8	0x20	RW	[7] pause_enable [6] pause_reg [5] master_outformat [4] ssn_polarity [3:0] NA
P3:0x55	spi_master_mode1	8	0x81	RW	[7] data_start_finish_mode [6] ddr_4line_mode [5] free clk_mode [4] ddr_switch_mode [3] status_tail_enable [2] allow_pause_timer [1] spi_enable_buf_mode [0] high_bandwidth
P3:0x57	pause_number	8	0x20	RW	pause_number, once transfer numbers, then pause
P3:0x58	timer_number	8	0x20	RW	timer_number, pause number clock,then restart transfermation
P3:0x59	MIPI_wdiv_setwordout_mode	8	0x00	RW	[7:4] MIPI_wdiv_set [3] data_size [2] line_number

					[1] height [0] width
P3:0x5a	sync_format	8	0x01	RW	[7:0]sync_format
P3:0x5b	image_width[7:0]	8	0x80	RW	image_width[7:0]
P3:0x5c	image_width[15:8]	8	0x02	RW	image_width[15:8]
P3:0x5d	image_height[7:0]	8	0Xe0	RW	image_height[7:0]
P3:0x5e	image_height[15:8]	8	0x01	RW	image_height[15:8]
P3:0x60	SYNC_code0	8	0x01	RW	SYNC_code0
P3:0x61	SYNC_code1	8	0x02	RW	SYNC_code1
P3:0x62	SYNC_code2	8	0x40	RW	SYNC_code2
P3:0x63	SYNC_code3	8	0x00	RW	SYNC_code3
P3:0x64	hsync_delay_mode sck_always bt656_mode	4	0x04	RW	[3:2] hsync_delay_mode [1] sck_always [0] bt656_mode
P3:0x65	SYNC_HEADER[23:16]	8	0xff	RW	SYNC_HEADER[23:16]
P3:0x66	SYNC_HEADER[15: 8]	8	0xff	RW	SYNC_HEADER[15: 8]
P3:0x67	SYNC_HEADER[7: 0]	8	0xff	RW	SYNC_HEADER[7: 0]
P3:0x68	spi_status[7:5]	8		RO	[7:5] spi_status[7:5] [4:0] NA
P3:0x69	Frame_counter	8		RO	frame_counter