

GC6133 CSP

1/13" QVGA CMOS Image Sensor

Data Sheet

Rev.1.01

2015-12-1



Ordering Information

♦ GC6133C

(Color, 8PIN)

GENERATION REVISION HISTORY

REV.	EFFECTIVE DATE	DESCRIPTION OF CHANGES	PREPARED BY
1.0	2015-11-11	Document Release	AE Dept.
1.01	2015-12-1	Change order information From GC6133 to GC6133C	Change order information
	14C0		



Content

1.	Sens	sor Overview4
	1.1	General Description
	1.2	Features
	1.3	Application
	1.4	Technical Specifications
2		
2.		Parameters5
	2.1	Standby Current
	2.2	Operation Current
	2.3	DC Characteristics6
3.	Bloc	ck Diagram6
4.	CSF	Package7
	4.1	Pin Diagram
	4.2	Pin Descriptions
	4.3	Package Specification (unit: mm)
5.	Opt	ical Specifications9
	5.1	Optical Center (unit: µm)9
	5.2	Readout Position
	5.3	Pixel Array11
	5.4	Lens Chief Ray Angle (CRA)
	5.5	Color Filter Spectral Characteristics
		o-wire Serial Bus Communication14
	6.1	Protocol
	6.2	Serial Bus Timing
		olications16
1	7.1	Timing 16
8.	Pow	ver On/Off Sequence17
0	Pog	istar I ist



1. Sensor Overview

1.1 General Description

The GC6133 is a highly integrated CMOS image sensor, active pixel is 244 x 328. GC6133 outputs YUV/YCrCb 4:2:2 or RGB 565 data through the serial data bus. GC6133 supports SPI interface.

The on-chip ISP provides a very smooth AE (Auto Exposure) and accurate AWB (Auto White Balance) control. It has a commonly used two-wire serial interface for host to control the operation of the whole sensor.

1.2 Features

- Standard optical format of 1/13 inch
- Various output formats: YCbCr4:2:2 / RGB565 / Raw Bayer
- Windowing support
- ◆ SPI interface: 1-wire, 2-wire
- Horizontal/Vertical mirror
- Image processing module
- Package: CSP

1.3 Application

- Cellular Phone Cameras
- Notebook and desktop PC cameras
- PDAs
- Toys
- Digital still cameras and camcorders
- Video telephony and conferencing equipment



1.4 Technical Specifications

Parameter	Typical value
Optical Format	1/13 inch
Pixel Size	2.5um x 2.5um
Active pixel array	244 x 328
ADC resolution	10 bit ADC
Max Frame rate	QVGA: 30fps
Power Supply	AVDD28: 2.7~3.0V(Typ.2.8V)
Power Consumption	45mW@30fps, QVGA
	<25μA@standby
SNR	TBD
Dark Current	TBD
Sensitivity	TBD
Dynamic range	TBD
Operating temperature:	-20~70°C
Stable Image temperature	0~50℃
Optimal lens chief ray angle(CRA)	21.6°(linear)
Package type	CSP

2. DC Parameters

2.1 Standby Current

Hardware PWDN

Item	Symbol	Min	Тур	Max	Unit
Analog	I_{AVDD}	_	25	TBD	uA
Power off					uA

PWND: H

Typ. Analog: 2.8V, T_i=25 °C

Software PWDN

Item	Symbol	Min	Тур	Max	Unit
Analog	I_{AVDD}	_	7	TBD	mA
Power off	-				mA

PWND: L

Typ. Analog: 2.8V, T_i=25℃



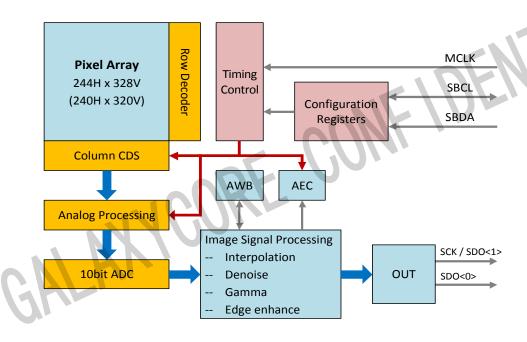
2.2 Operation Current

Item	Symbol	Min	Typ Max		Unit			
Analog	I_{AVDD}		14	TBD	mA			
INCLK: 24MI	Hz, Frame rate: 3	30fps , YU	V, SPI-1w	ire				
DCLK: 24MHz								
Typ. Analog: $2.8V$, $T_i=25^{\circ}C$								
DC Charact	teristics	Cl	Mr	IV				

2.3 DC Characteristics

Item	Symbol	Min	Тур	Max	Unit			
Power supply	V_{AVDD}	2.7	2.8	3.0	V			
Digital Input(Conditions: AVDD = 2.8V)								
Input voltage HIGH	$ m V_{IH}$	1.4			V			
Input voltage LOW	$\mathbf{V}_{\mathbf{IL}}$			0.6	V			
Digital Output(Conditions: AVDD = 2.8V, standard Loading 25PF)								
Output voltage HIGH	V _{OH}	1.6			V			
Output voltage LOW	V_{OL}			0.2	V			

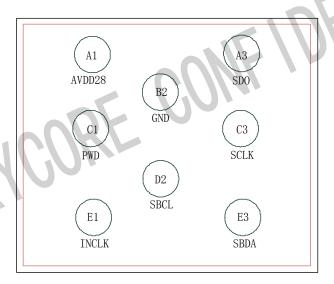
3. Block Diagram





4. CSP Package

4.1 Pin Diagram



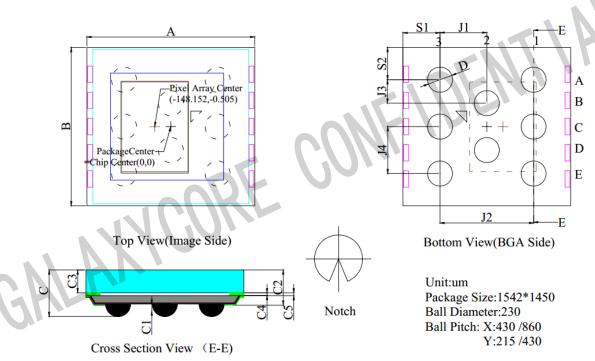
Top View

4.2 Pin Descriptions

Pin	Name	Pin Type	Description
A1	AVDD28	Power	Power for analog circuit and sensor array,
			2.7~3.0V, connect Capacitor (≥0.1uF) to
			ground
A3	SDO	Output	SPI data
B2	GND	Ground	Ground
C1	PWDN	Input	Power down (active high)
C3	SCLK	Output	SPI clock
D2	SBCL	Input	SCCB input clock
E1	INCLK	Input	Sensor input clock
E3	SBDA	I/O	SCCB data



4.3 Package Specification (unit: um)

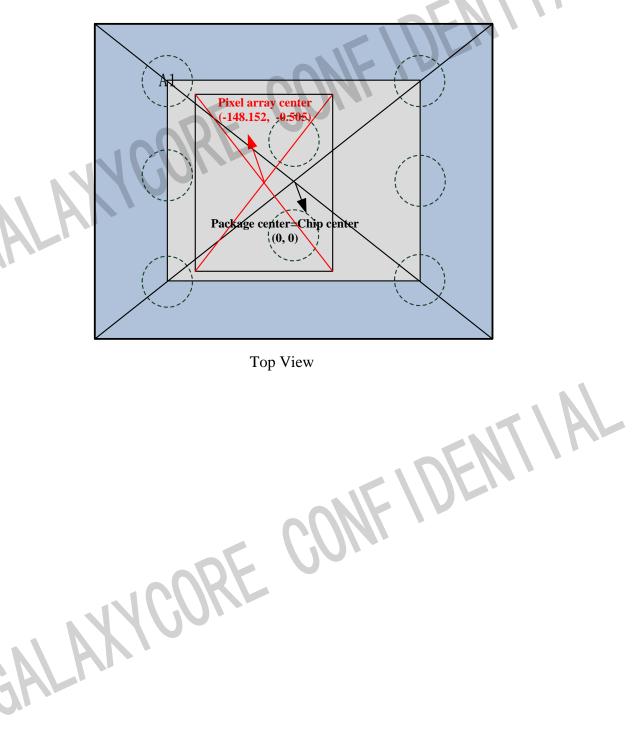


Description	Crossb ol	Nominal	Min.	Max.		
Description	Symbol	Millimeters				
Package Body Dimension X	A	1.5420	1.5170	1.5670		
Package Body Dimension Y	В	1.4500	1.4250	1.4750		
Package Height	С	0.6800	0.6250	0.7350		
Ball Height	C1	0.1200	0.0900	0.1500		
Package Body Thickness	C2	0.5600	0.5250	0.5950		
Thickness from top glass surface to	C3	0.4000	0.3900	0.4100		
wafer	C3	0.4000	0.3900	0.4100		
Ball Diameter	D	0.2300	0.2000	0.2600		
Total Ball Count	N	8				
Pin Pitch X axis	J1	0.4300	0.4200	0.4400		
Pin PitchY axis	J2	0.8600	0.8500	0.8700		
Edge to Pin Center Distance along X	S1	0.3410	0.3110	0.3710		
Edge to Pin Center Distance along Y	S2	0.2950	0.2650	0.3250		



5. Optical Specifications

5.1 Optical Center (unit: μm)

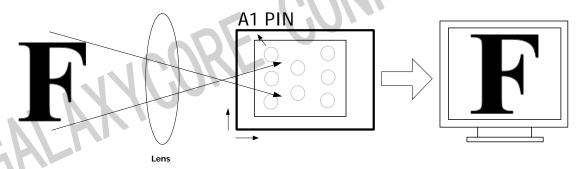


Top View



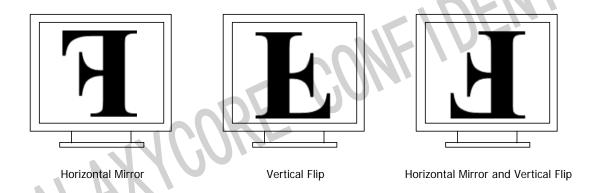
5.2 Readout Position

The GC6133 default status is readout from the lower left corner with pin A1 located in the upper left corner. The image is inverted vertically and horizontally by the lens, so mirrored image output results when Pin A1 is located in the upper left corner.



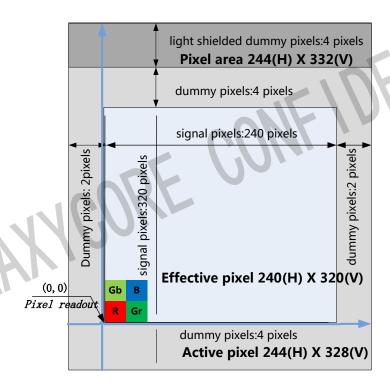
Readout direction can be set by the registers.

Function	Register Address	Register Value	First Pixel
Normal	P0:0x14[1:0]	00	R
Horizontal mirror	P0:0x14[1:0]	01	Gr
Vertical Flip	P0:0x14[1:0]	10	Gb
Horizontal Mirror and Vertical Flip	P0:0x14[1:0]	11	В





5.3 Pixel Array



Pixel array is covered by Bayer pattern color filters. The primary color BG/GR array is arranged in line-alternating way.

If no flip in column, column is read out from 0 to 239. If flip in column, column is read out from 239 to 0.

If no flip in row, row is read out from 0 to 319.If flip in row, row is read out from 319 to 0.



5.4 Lens Chief Ray Angle (CRA)

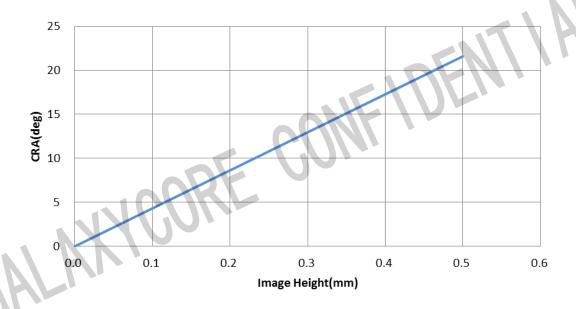
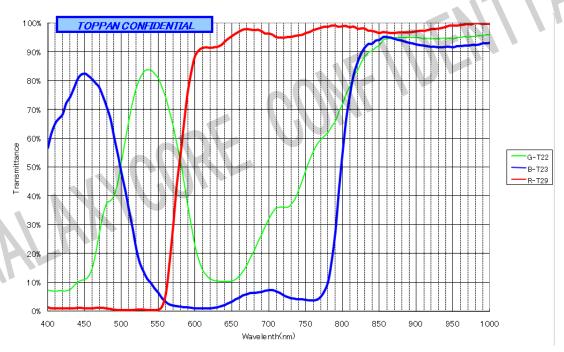


Image Height	Image Height(mm)	CRA(degree)
0	0.00000	0.00
10	0.04998	2.16
20	0.09996	4.32
30	0.14994	6.48
40	0.19992	8.64
50	0.24990	10.80
60	0.29988	12.96
70	0.34986	15.12
80	0.39984	17.28
90	0.44982	19.44
100	0.49980	21.60



5.5 Color Filter Spectral Characteristics

The optical spectrum of color filters is shown below



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6. Two-wire Serial Bus Communication

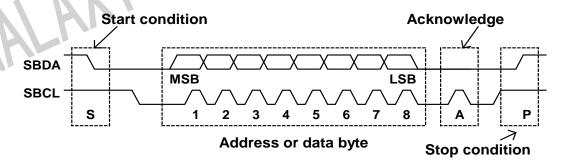
GC6133 I2C Address:

Serial bus write address = 0x80, serial bus read address = 0x81

6.1 Protocol

The host must perform the role of a communications master and GC6133 acts as either a slave receiver or transmitter. The master must do

- ♦ Generate the **Start(S)/Stop(P)** condition
- ◆ Provide the serial clock on **SBCL**.



Single Register Writing:

SII	bligic register writing.											
S	80H	A	Register Address	A	Data	A	P					
Incremental Register Writing:												
S	80H	A	Register Address	A	Data(1)	A		Data	(N)	A	P
Single Register Reading:												
S	80H	A	Register Address	A	S 81	Н	A	Data	NA	P		
No	Notes:											
_												

From master to slave From slave to master

S: Start condition P: Stop condition

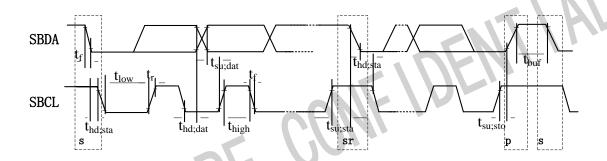
A: Acknowledge bt **NA:** No acknowledge

Register Address: Sensor register address

Data: Sensor register value



6.2 Serial Bus Timing



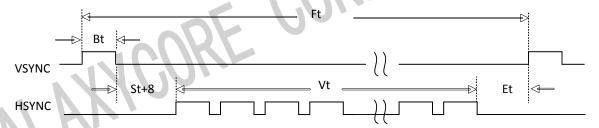
Parameter	Symbol	Min.	Typ.	Max.	Unit
SBCL clock frequency	F _{scl}	0		400	KHz
Bus free time between stop and start	$t_{ m buf}$	1.3			μs
condition					
Hold time for a repeated start	t _{hd;sta}	0.6			μs
LOW period of SBCL	$t_{ m low}$	1.3			μs
HIGH period of SBCL	t _{high}	0.6			μs
Set-up time for a repeated start	t _{su;sta}	0.6			μs
Data hold time	t _{hd;dat}	0		0.9	μs
Data Set-up time	t _{su;dat}	100			ns
Rise time of SBCL, SBDA	t _r			300	ns
Fall time of SBCL, SBDA	t_{f}			300	ns
Set-up time for a stop	t _{su;sto}	0.6		+	μs
Capacitive load of bus line (SBCL, SBDA)	C_b				pf
CALLANY CORF. C			V •		



7. Applications

7.1 Timing

Suppose Vsync is low active and Hsync is high active, and output format is YCbCr / RGB565, then the timing of vsync and hsync is bellowing(take capture mode for example, preview mode is the same):



Ft = VB + Vt + 8 (unit: row time)

VB = Bt + St + Et, Vblank/Dummy line, setting by register P0:0x0f[7:4] and P0:0x02.

- ◆ Ft -> Frame time, one frame time.
- ◆ Bt -> Blank time, Vsync no active time.
- \bullet St -> Start time, setting by register 0x0e[7:4].
- \bullet Et -> End time, setting by register 0x0e[3:0].
- ◆ Vt -> valid line time. QVGA is 320, Vt=win_height-8, win_height is 328.

When exp_time <= win_height+VB, Bt=VB-St-Et. Frame rate is controlled by window_height+VB.

When exp_time > win_height+VB, Bt=exp_time-win_height-St-Et. Frame rate is controlled by exp_time.

The following is row_time calculate:

 $row_time = Hb + Sh_delay + win_width + 4.$

Hb -> HBlank or dummy pixel, Setting by register P0:0x0f[3:0] and 0x01.

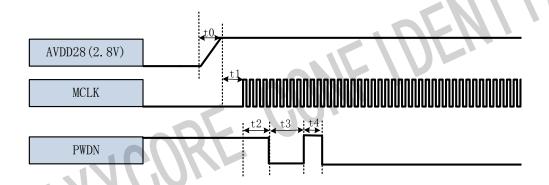
Sh_delay -> Setting by internal.

win_width -> win_width = final_output_width(240) + 4. So for QVGA, we should set win_width as 244.



8. Power On/Off Sequence

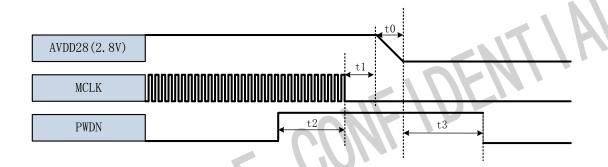
Power On Sequence



	Parameter	Description	Min.	Max.	Unit
Oil	t0	AVDD28 rising time	35		μs
	t1	From AVDD28 to MCLK applied	10		μs
	t2	From MCLK applied to PWDN pull low	10		μs
	t3	From PWDN pull low to PWDN pull high	10		μs
	t4	From PWDN pull high to PWDN pull low	10		μs
G		VCORF COM			



4 Power Off Sequence

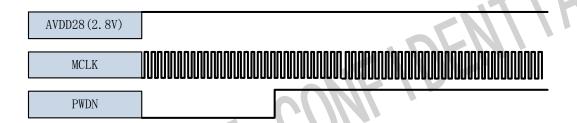


Parameter	Description	Min.	Max	Unit
t0	AVDD28 falling time	0		μs
t1	From MCLK disable to sensor AVDD28	0		μs
	power down			
t2	From sensor disable to MCLK disable	0		μs
t3	From sensor disable to PWDN pull low	0		μs

♦ Recommended power on/off sequence is above.



Standby Sequence



- ◆ If the sensor's power cannot be cut off, please keep power supply, then set PWDN pin high. It will make sensor standby
- **♦** If you have special requirements in application, please contact with us to confirm.

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9. Register List

System Register

Address	Name	Width	Default	R/W	Description
			Value		
0xf0	ChipID_low	8	0xba	RO	[7:0] Chip ID
0xf1	pad_updn	4	0x40	RW	[7]NA
	output_en				[6] pwd_dnb
				M	[5:4] updn
					[3:2] NA
				V	[1] sck_en
	-10				[0] sdo0_en
0xf6	pad_test_value	8	0x02	RW	[7:6] pad_test_value
1 1	pad_test_valid				[5:4] pad_test_valid
	div_en				[3] div_en
	sck_delay_mod				[2:0] sck_delay_mode
	e				
0xfa	Clk_div_mode	8	0x00	RW	[7:4] represents the frequency division
					number: a1/(N+1)
					[3:0] represent the high level in one pulse
					after frequency division.
0xfb	i2c_device_id	7	0x80	RO	[7:1] i2c_device_id
					[0] NA
0xfc	Digital_clk_ena	5	0x0b		[7:5] NA
	ble				[4] digital clock enable
	wclk_div				[3] wclk_select
	Analog_pwc				[2] NA
					[1] DAC18 enable
				_	[0] analog power down enable
0xfe	Reset related &	8	0x00		[7] soft_reset
	page select				[6] NA
	-310	-			[5] spi_soft_reset
	IVV	10			[4] CISCTL_rst
. 1	VVI				[3] NA
	W.				[2:0] page_select
H					000: page 0
					010: page 2(SPI)



Analog & CISCTL

Address	Name	Width	Default	R/W	Description
			Value		1
P0:0x01	Hb[7:0]	8	0x36	RW	Horizontal blanking, unit pixel clock
P0:0x02	Vb[7:0]	8	0x02	RW	Vertical blanking, if current exposure <
					(Vb + window Height), frame rate will be
					(Vb + window Height); otherwise frame
					rate will be determined by exposure
P0:0x03	CISCTL_exp[1	4	0x00	RW	disable AEC_en to write this register
	1:8]			$igcup_{i}$	by i2c
P0:0x04	CISCTL_exp[7	8	0x10	RW	2. enable AEC_en to write this register by
	:0]				AEC module
	O Y V				need 2 frame to update the exp data
P0:0x0f	vb[11:8]	8	0x01	RW	[7:4] Vb high 4 bits
	hb[11:8]				[3:0] Hb high 4 bits
P0:0x14	Updown and	7	0x00	RW	[7:2] Reserved
	mirror				[1] updown
					[0] mirror
P0:0x1f	ANALOG_PA	8	0x15	RW	[7:6] Reserved
	D_drv				[5:4] drv_sck
					[3:2] drv_sdo
					[1:0] drv_sda

ISP Related

Address	Name	Width	Default	R/W	Description
Address	Name	Width	Value	14/ 11	Description
P0:0x20	Block_enable_	8	0x7e	RW	[7:6] gamma mode
	1				[5] gamma enable
					[4] Edge enhancement enable
			28		[3] Interpolation enable
	-310				[2] DN enable
1	VVV	70			[1] DD enable
					[0] Reserved
P0:0x22	AAAA_enable	8	0x00	RW	[7] auto_SA enable
177					[6] AWB enable
N.					[5] auto_DN_en
					[4] auto_DD_en
					[3:0] Reserved
P0:0x23	buff_special_ef	8	0x40	RW	[7:4] Reserved
	fect				[3:2] only_edge_map
					[1] CbCr fixed enable



					EO. Y 1
7000			0.74		[0] Inverse color
P0:0x24	Output_format	8	0x54	RW	[7:5] Reserved
					[3] smooth_Y
					[2] croma_avg_two_neightbor
					[1:0] output_bus_mode
					11: DNDD_out
					10: PreGain_out
					01: RGB_out
				\mathbb{N}	00: YCbCr_out
P0:0x26	bypass_mode	8	0x83	RW	[7] updata_gain_mode
		50		V	[6] single_2_double_mode
	10				[5] first_second_switch
	1111	())			[4] odd even col switch
. 1	1 10				[3] is_8bit_bypass
					[2] skin_en
					[1:0] If is_8bit_bypass, this setting
					means: bypass which 8bits from 11bit.
					11: [10:3]default
					10: [9:2]
					01: [8:1]
					00: [7:0]
					If PreGain_out_data choosed, this
					setting means:
					[1]: 1'b1: bypass[9:2]
					1'b0: bypass[7:0]
					[0]: NA
P0:0x29	debug_mode2	8	0x30	RW	[7] BFF_gate_mode
0.0112				22,,,	[6] CTL_pipe_gate_mode
					[5] ISP_quiet_mode
					[4] DIV_gatedclk_en
					[3] only_skin_map
		\Box	75		[2] OUT_test_image
	-310				[1] GRAB_test_image, test image before
1	IVV	10			SRAM
. 1					[0] test image after EEINTP
P0:0x39	out_win_y1[7:0	8	0x00	RW	out_win_y_start
1 0.0X33		٥	UAUU	17. 44	out_wiii_y_start
P0:0x3a	win_mode	8	0x80	RW	[7] win_mode
ı v.uxsa	out_win_x1[6:0		UAGU	17. 44	[6:0] out_win_x_start
					Lo.01 out_win_x_start
P0:0x3b	Out window	1	0x01	PW/	[7:1] NA
u 0.0x30	height[8]	1	UXUI	17. 44	[0] Out window height[8]
D0.0-2-	+ -	o	0 40	DW	-
P0:0x3c	Out window	8	0x40	RW	Out window height[7:0]



	height[7:0]				
P0:0x3e	Out window	8	0xf0	RW	Out window width[7:0]
	width[7:0]				

BLK

Address	Name	Width	Default	R/W	Description
			Value	6	
P0:0x2a	BLK_mode	7	0x23	RW	[7] NA
					[6:4] BLK smooth speed
					[3:2] Reserved
	101				[1] dark_current_mode
	MMM	9,			[0] BLK offset enble
P0:0x2b	BLK_limit_val	7	0x10	RW	BLK_limit_value
	ue				
P0:0x30	current_R_dark	6	0x00	RW	current_dark_current
	_current				
P0:0x31	BLK_limit_col	5	0x02	RW	BLK_limit_col_gain
	_gain				
P0:0x33	gain_rate_dark	8	0x00	RW	[7:4] Reserved
	c				[3:0] exp_rate_darkc
	exp_rate_darkc				
P0:0x34	offset_ratio	6	0x20	RW	[5:0] offset_ratio
P0:0x36	manual_offset	6	0x00	RW	manual_offset
			S	6	ONFIDENI
	MAN	Ui'	111		



GLOBAL/PRE/POSTGAIN

Address	Name	Width	Default	R/W	Description
			Value		
P0:0x3f	Global_gain	6	0x10	RW	[7:6] NA
					[5:0] global_gain
P0:0x40	auto_pregain	8	0x20	R-W	Controlled by AEC, can be manually
					controlled when disable AEC, 3.5 bits
P0:0x41	col_code	3	0x00	R-W	Col_code
P0:0x42	Channel_gain_	8	0x80	RW	1.7 bits, G1/G2 channel pre gain
	G1			7	
P0:0x43	Channel_gain_	8	0x80	RW	1.7 bits, R/B channel pre gain
4	R				
P0:0x46	R_ratio	8	0x80	RW	1.7 bits, R_ratio
P0:0x48	B_ratio	8	0x80	RW	1.7 bits, B_ratio
P0:0x49	AWB_R_gain	8	0x50	RO	disable AWB_en to write those register
P0:0x4a	AWB_G_gain	8	0x40	RO	by i2c
P0:0x4b	AWB_B_gain	8	0x48	RO	

DNDD

Address	Name	Width	Default	R/W	Description
			Value		
P0:0x50	DN_mode_en	8	0x34	RW	[7] on_edge_adaptive_mode
					[6] max_min_used_adaptive_mode
					[5] DD_Y_value_op_mode
					[4] DN_b_mode
					[3] NA
					[2] c_weight_adaptive_mode
					[1:0] NA
P0:0x51	DN_mode_rati	6	0x22	RW	[7:6] NA
	О		70		[5:4] C_weight_adaptive_ratio
	- 11				[3:0] Reserved
P0:0x52	DN_b_slope	8	0x4f	RW	[7:4] ASDE_DN_b_slope
	DN_bilat_b_ba				[3:0] DN_bilat_b
\mathbb{N}	se				
P0:0x53	DN_C_slope	8	0x81	RW	[7:4] ASDE_DN_C_slope
7/1	DN_C_weight				[3:0] base center pixel weight
P0:0x54	DD_dark_brigh	8	0x54	RW	[7:4] dark threshold
	t_TH				[3:0] bright threshold
P0:0x55	DD_flat_TH	8	0x86	RW	DD_flat_TH
P0:0x56	DN_inc_or_dec	7	0x68	RW	[7] NA
	DD_ratio				[6] ASDE_DN_inc_or_dec



	DD_limit				[5:4] DD_ratio
					[3:0] DD_limit
P0:0x57	DD_on_edge_t	8	0x55	RW	[7:4] DD_on_edge_th_H
	h				[3:0] DD_on_edge_th_L
P0:0x58	DD_is_bright_	8	0x64	RW	[7:4] bright_th
	dark_th				[3:0] dark_th
P0:0xc3	Reserved	8	0x96	RW	Reserved

INTPEE (Interpolation and Edge Enhancement)

Address	Name	Width	Default	R/W	Description
	-10		Value		•
P0:0x5e	Reserved	6	0x05	RW	Reserved
P0:0x5f	Reserved	5	0x05	RW	Reserved
P0:0x60	direction TH1	7	0x05	RW	[6] Reserved
HI-					[5:0] Lower Criteria for direction
					detection
P0:0x61	Direction TH2	6	0x3f	RW	[7:6] NA
					[5:0] Upper Criteria for direction
					detection
P0:0x62	Reserved	8	0x05	RW	Reserved
P0:0x63	Edge effect	8	0x11	RW	[7:4] Reserved
					[3:0] edge effect: use 3x3 template
					Controlled by user or ASDE
P0:0x64	Edge_max	8	0x43	RW	[7:4] edge max
	Edge_min				[3:0] edge min

CC Matrix

Address	Name	Width	Default	R/W	Description
			Value		
P0:0x65	CC Matrix C11	8	0x13	RW	CC Matrix C11, S1.6
P0:0x66	CC Matrix C12	8	0x26	RW	CC Matrix C12, S1.6
P0:0x67	CC Matrix C13	8	0x07	RW	CC Matrix C13, S1.6
P0:0x68	CC Matrix C21	8	0xf5	RW	CC Matrix C21, S1.6
P0:0x69	CC Matrix C22	8	0xea	RW	CC Matrix C22, S1.6
P0:0x6a	CC Matrix C23	8	0x21	RW	CC Matrix C23, S1.6
P0:0x6b	CC Matrix C31	8	0x21	RW	CC Matrix C31, S1.6
P0:0x6c	CC Matrix C32	8	0xe4	RW	CC Matrix C32, S1.6
P0:0x6d	CC Matrix C33	8	0xfb	RW	CC Matrix C33, S1.6

YCP



Address	Name	Width	Default	R/W	Description
			Value		
P0:0x80	Global	8	0x40	RW	Global saturation
	saturation				
P0:0x81	saturation_Cb	8	0x38	RW	Cb saturation
P0:0x82	saturation_Cr	8	0x38	RW	Cr saturation
P0:0x83	luma_contrast	8	0x4b	RW	Luma_contrast
P0:0x84	contrast center	8	0x90	RW	Contrast center value
P0:0x85	luma_offset	8	0x06	RW	luma offset
P0:0x86	skin_Cb_center	8	0xfb	RW	Cb criteria for skin detection.
P0:0x87	skin_Cr_center	8	0x1d	RW	Cr criteria for skin detection
P0:0x88	Skin radius	6	0x18	RW	Defines skin range
	square	5			
P0:0x89	Skin brightness	8	0xe3	RW	[7:4] skin brightness high threshold
NN F	high				[3:0] skin brightness low threshold
W.	Skin brightness				
	low				
P0:0x8a	fixed_Cb	8	0x00	RW	fix CbCr
P0:0x8b	fixed_Cr	8	0x00	RW	

AEC

Address	Name	Width	Default	R/W	Description
			Value		
P0:0x90	Reserved	8	0x3c	RW	Reserved
P0:0x92	AEC_target_Y	8	0x40	RW	read adaptive data
P0:0x93	Y_average	8	0x80	RO	Current frame luminance average
P0:0x99	AEC_step2_su	8	0x02	RW	AEC_step2_sunlight
	nlight		70		
P0:0x9d	AEC_anti_flike	8	0x65	RW	[7:0] flicker step [8:0]
	r_step [7:0]	10			
P0:0x9e	AEC_I_stop_m	8	0x63	RW	[7:4] AEC_I_stop_margin
M_{\perp}	argin				[3:0] AEC_exp_level_1[11:8]
171	AEC_exp_levle				
N.	_1[11:8]				
P0:0x9f	AEC_exp_levle	8	0xf2	RW	AEC_exp_level_1[7:0]
	_1[7:0]				
P0:0xa0	AEC_Exp_min	6	0x20	RW	[7:4] Reserved
	_1[11:8]				[3:0] minimum exposure level high 4 bits
P0:0xa1	Exp_min_1[7:0]	8	0x04	RW	minimum exposure level lower 8 bits



Address	Name	Width	Default	R/W	Description
AWB					
					[0] AEC_enable
P0:0xa4	AEC_enable	1	0x00	RW	[7:1] NA
	_dg_gain				
P0:0xa3	AEC_max_pre	8	0x30	RW	Digital pre gain limit, float 3.5

AWB

Address	Name	Width	Default Value	R/W	Description		
P0:0xb0	Reserved	8	0xf8	RW	Reserved		
P0:0xb1	Reserved	8	0x1e	RW	Reserved		
P0:0xb2	Reserved	8	0x10	RW	Reserved		
P0:0xb3	Reserved	8	0x20	RW	Reserved		
P0:0xb4	Reserved	8	0x2d	RW	Reserved		
P0:0xb5	Reserved	8	0x1b	RW	Reserved		
P0:0xb6	Reserved	8	0x2e	RW	Reserved		
P0:0xb7	Reserved	8	0x18	RW	Reserved		
P0:0xb8	Reserved	8	0x13	RW	Reserved		
P0:0xba	Reserved	3	0x20	RW	Reserved		
P0:0xbb	AWB_adjust_s	7	0x62	RW	[7] NA		
	peed				[6:4] AWB gain adjust speed		
	AWB_adjust_				[3:0] AWB adjust margin		
	margin						
P0:0xbd	AWB_R_gain_	8	0x70	RW	Channel gain limit for R, G, B.		
	limit				Float 2.6		
P0:0xbe	AWB_G_gain_	8	0x58	RW			
	limit						
P0:0xbf	AWB_B_gain_	8	0x80	RW			
	limit						
SPI module							
Address	Name	Width	Default	R/W	Description		

SPI module

Address	Name	Width	Default	R/W	Description
			Value		
P2:0x01	spi_mode	1	0x00	RW	[7:1] NA
					[0] spi_enable
					1: enable
					0: disable
P2:0x02	spi_global_mo	8	0xb2	RW	[7] msb_first
	de				1: msb first on sdo
					0: lsb first on sdo
					[6] NA
					[5] ddr_mode



		I			
					[4] ddr_switch_mode
					[3] status_tail_enable
					[2] high_bandwidth
					[1] CPHA
					1:sck back edge sample
					0:sck first edge sample
					[0] CPOL
					1: sck idle is 1
					0: sck idle is 0
P2:0x03	spi_data_mode	8	0x20	RW	[7] add_CRC
				V	[6] ssn_out_mode
	101				[5] add_sync_sign
	.1117				1: package the data
. 1	$X \setminus A$				0: not package the data
					[4] data_idle_status
					1: data idle is 1
					0: data idle is 0
					[3:2] data_bandwidth
					00: 1bit bus
					01: 2bit bus
					[1:0] data_sequence
					00: sdo[3:0]-→4/5/6/7—0/1/2/3
					01: sdo[3:0]-→4/5/7/60/1/3/2
					10: sdo[3:0]-→7/6/5/43/2/1/0
					11: sdo[3:0]-→5/4/7/61/0/3/2
P2:0x04	spi_master_mo	6	0x20	RW	[7:6]NA
	de				[5] master_outformat
					1: size equal width X2
					0: not
					[4] ssn_polarity
					1: high valid
			70		0: low valid
	-310				[3:0] frequency divider
P2:0x09	Wordout_mode	4	0x00	RW	[7:4] NA
2.0009	in ordout_mode	7	UAUU	17. 44	[3] data_start_size_H or L
					[2] line_start_line_H or L
AM					[1] frame_start_height_H or L
77,					[0] frame_start_width_H or L
P2:0x0a	sync_format	8	0x01	RW	Only for package sign, YUV or RAW or
1 2.UAUa	sync_rormat	O	UAUI	17. 44	JPEG
P2:0x13	Fife prog full	8	0x03	RW	Fifo_prog_full_level
r 2.0x13	Fifo_prog_full_ level	O	UXUS	IX VV	i-no_prog_run_ievei
D2.0v20	 	o	0.01	DW	SVNC code0
P2:0x20	SYNC_code0	8	0x01	RW	SYNC_code0



P2:0x21	SYNC_code1	8	0x02	RW	SYNC_code1
P2:0x22	SYNC_code2	8	0x40	RW	SYNC_code2
P2:0x23	SYNC_code3	8	0x00	RW	SYNC_code3
P2:0x24	sck_always,	8	0x00	RW	[7] fifo full error bit
	bt656_mode				[6] fifo empty error bit
					[5] fifo ready bit
					[4:2] NA
					[1] sck_always
				\mathcal{M}	[0] BT656 mode
P2:0x25	SYNC_HEAD	8	0xff	RW	SYNC_HEADER[23:16]
	ER[23:16]				
P2:0x26	SYNC_HEAD	8	0xff	RW	SYNC_HEADER[15:8]
	ER[15:8]	9,			
P2:0x27	SYNC_HEAD	8	0xff	RW	SYNC_HEADER[7:0]
	ER[7:0]				
P2:0x28	fifo_switch	8	0x01	RW	[7:6] fifo_switch
	clock_div_spi				[5:0] clock_div_spi
					=

