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Advanced Hardware Design
September 24, 2021

Homework 2

Deliverables-

4. Simulation Screenshots

4.1 Counter A

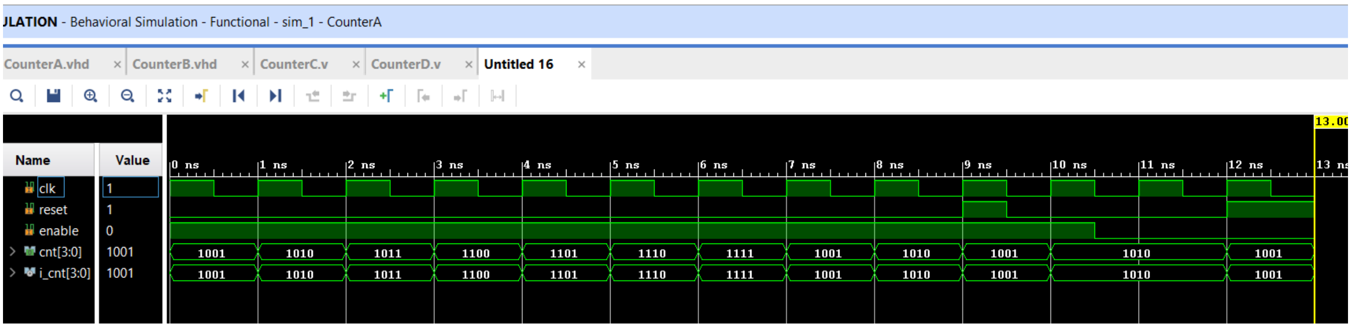


Image 1: Simulation of CounterA.vhd

Counter A works as follows –

In the beginning it has the value of 9 and then it adds 1 each time (0ns – 8ns) a positive edge of clock is given then it progresses to 15 adding 1 each time. When counter reaches 15 then it goes back to 9 and start repeating the sequence 9-10-11-12-13-14-15-9-10…..

It is worth noting that when reset is high (9ns, 12ns) counter goes to its reset value 9, irrespective of the state of enable, but counter does not progress when enable is low (11ns -13ns).

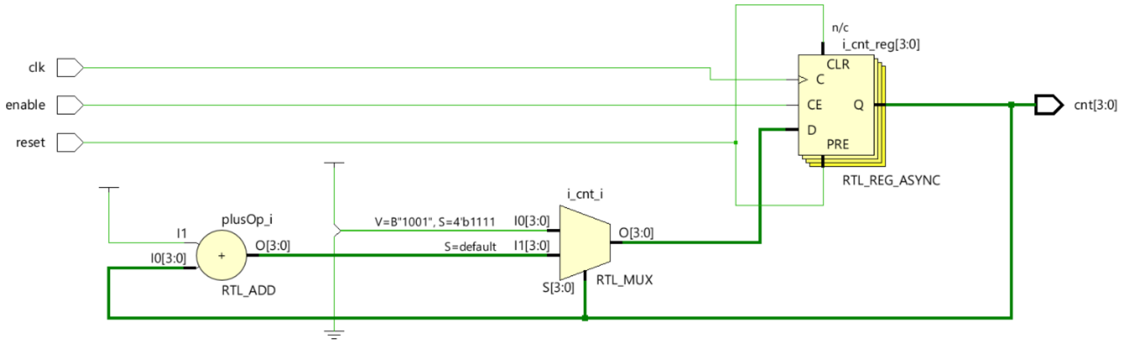


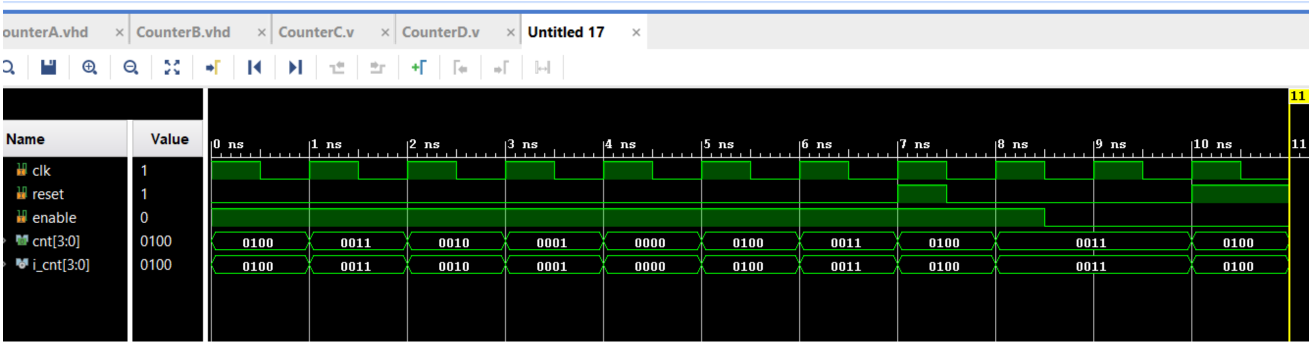
Image 2: Schematic of CounterA.vhd

Counter A schematics –

It contains a Register made up of 4 filpflops, an Adder, and a Multiplexer with an asynchronous Reset. Enable pin controls the flipflops i.e., when enable is low flipflop don't work and output remains the same. When Reset is high all the flipflops resets to the pre-set value.

Adder adds 1 to counter output and feeds into multiplexer, the Multiplexer does the job of resetting the counter to 9 on overflow condition based on value of current output of counter, if its overflow condition it selects the reset value otherwise it selects the value from Adder.

4.2 Counter B



Name	Value
clk	1
reset	1
enable	0
cnt[3:0]	0100
i_cnt[3:0]	0100

Image 1: Simulation of CounterB.vhd

Counter B works as follows –

In the beginning it has the value of 4 and then it subtracts 1 each time (0ns – 6ns) a positive edge of clock is given then it progresses to 0 subtracting 1 each time. When counter reaches 0 then it goes back to 4 and start repeating the sequence 4-3-2-1-0-4-3…..

It is worth noting that when reset is high (7ns, 10ns) counter goes to its reset value 4, irrespective of the state of enable, but counter does not progress when enable is low (9ns -11ns).

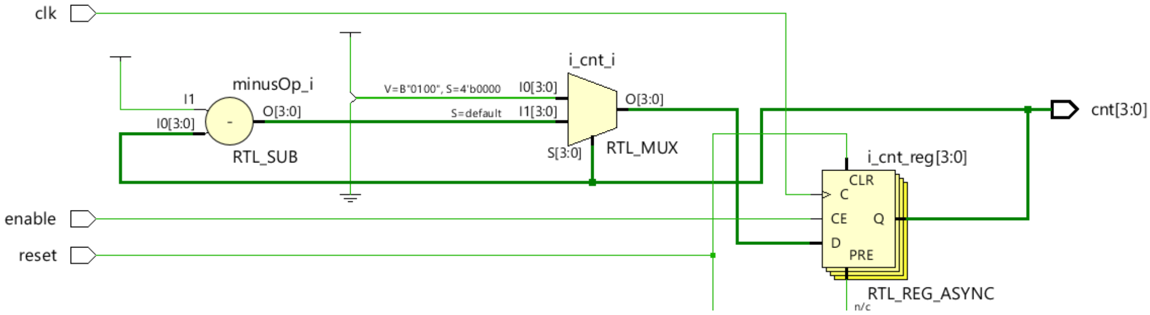


Image 2: Schematic of CounterB.vhd

Counter B schematics –

It contains a Register made up of 4 filpflops, an Subtractor, and a Multiplexer with an asynchronous Reset. Enable pin controls the flipflops i.e., when enable is low flipflop don't work and output remains the same. When Reset is high all the flipflops resets to the pre-set value.

Subtracter subtracts 1 to counter output and feeds into multiplexer, the Multiplexer does the job of resetting the counter to 4 on overflow condition based on value of current output of counter, if its overflow condition it selects the reset value otherwise it selects the value from Subtracter.

4.3 Counter C

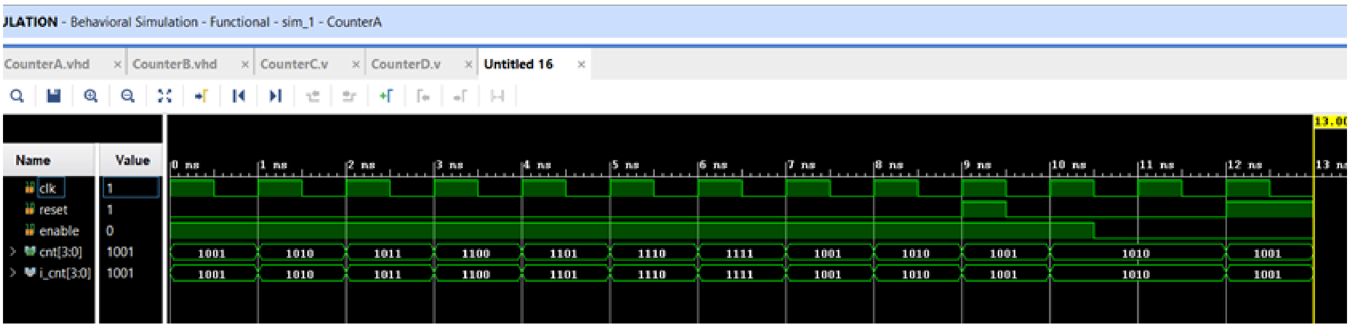


Image 1: Simulation of CounterC.v

Counter C works as follows –

In the beginning it has the value of 9 and then it adds 1 each time (0ns – 8ns) a positive edge of clock is given then it progresses to 15 adding 1 each time. When counter reaches 15 then it goes back to 9 and start repeating the sequence 9-10-11-12-13-14-15-9-10…..

It is worth noting that when reset is high (9ns, 12ns) counter goes to its reset value 9, irrespective of the state of enable, but counter does not progress when enable is low (11ns -13ns).

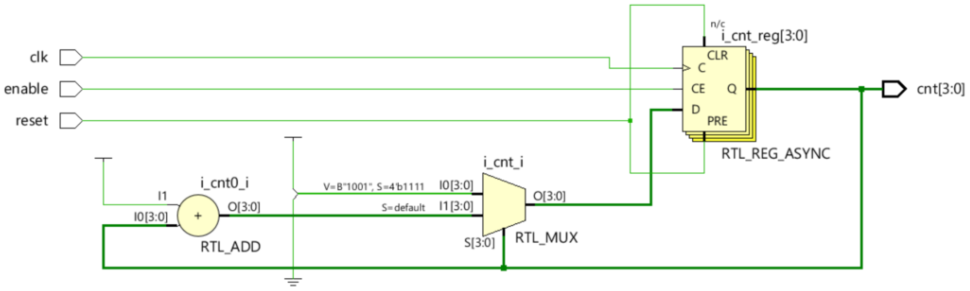


Image 2: Schematic of CounterC.v

Counter C schematics –

It contains a Register made up of 4 filpflops, an Adder, and a Multiplexer with an asynchronous Reset. Enable pin controls the flipflops i.e., when enable is low flipflop don't work and output remains the same. When Reset is high all the flipflops resets to the pre-set value.

Adder adds 1 to counter output and feeds into multiplexer, the Multiplexer does the job of resetting the counter to 9 on overflow condition based on value of current output of counter, if its overflow condition it selects the reset value otherwise it selects the value from Adder.

4.2 Counter D

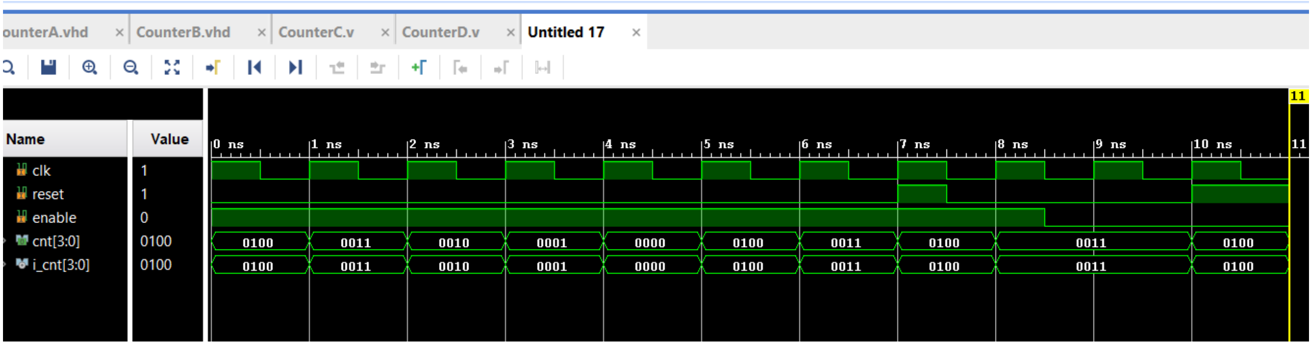


Image 1: Simulation of CounterD.v

Counter D works as follows –

In the beginning it has the value of 4 and then it subtracts 1 each time (0ns – 6ns) a positive edge of clock is given then it progresses to 0 subtracting 1 each time. When counter reaches 0 then it goes back to 4 and start repeating the sequence 4-3-2-1-0-4-3…..

It is worth noting that when reset is high (7ns, 10ns) counter goes to its reset value 4, irrespective of the state of enable, but counter does not progress when enable is low (9ns -11ns).

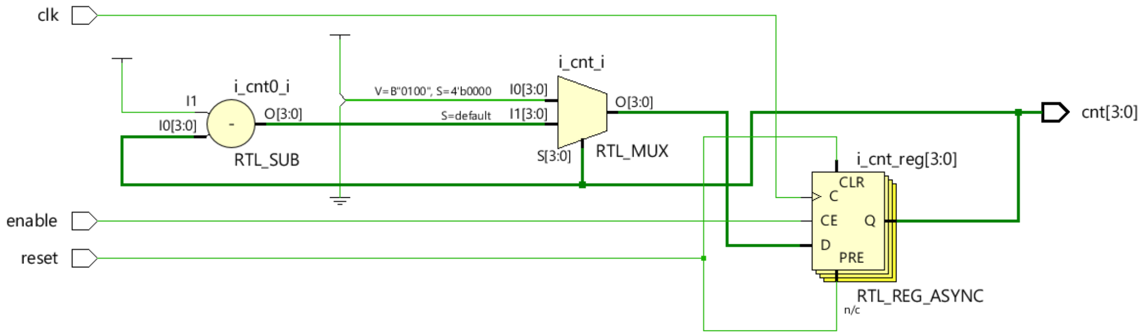


Image 2: Schematic of CounterD.v

Counter D schematics –

It contains a Register made up of 4 filpflops, an Subtractor, and a Multiplexer with an asynchronous Reset. Enable pin controls the flipflops i.e., when enable is low flipflop don't work and output remains the same. When Reset is high all the flipflops resets to the pre-set value.

Subtracter subtracts 1 to counter output and feeds into multiplexer, the Multiplexer does the job of resetting the counter to 4 on overflow condition based on value of current output of counter, if its overflow condition it selects the reset value otherwise it selects the value from Subtracter.

4.5 Differences in VHDL and Verilog Schematics

There was no difference in schematics of Counters synthesized from Verilog and VHDL, except the names of Adder and Subtracter, in VHDL the name was – icnt0_i but in Verilog they were – plusOp_i and minusOp_i.