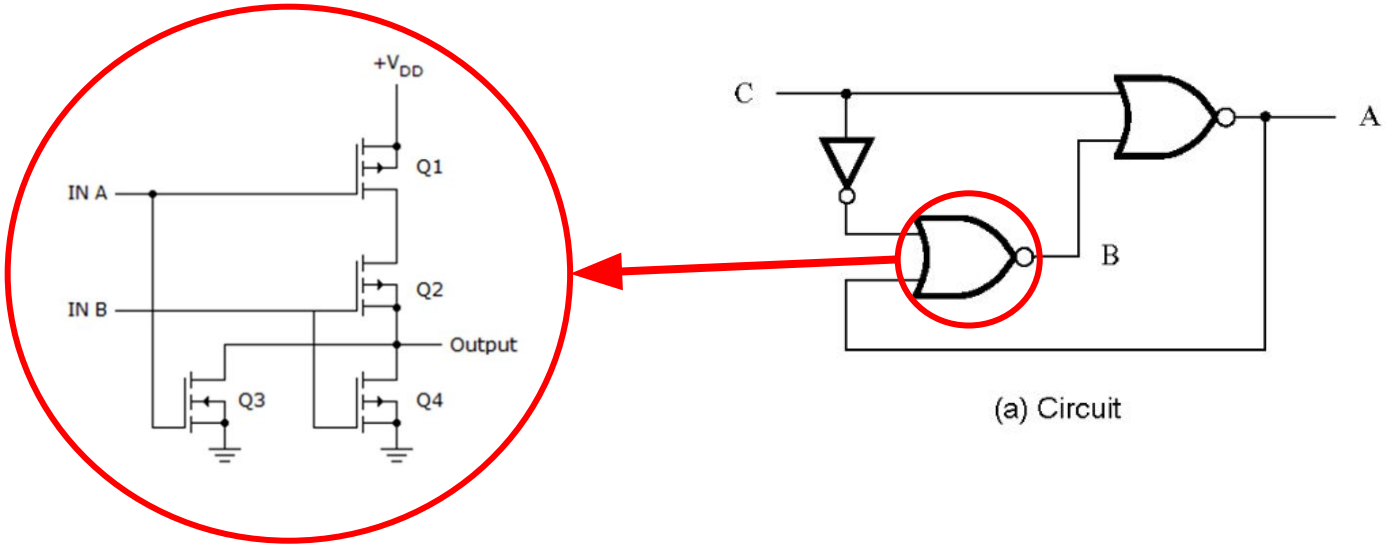
Delays in Digital Designs

2021

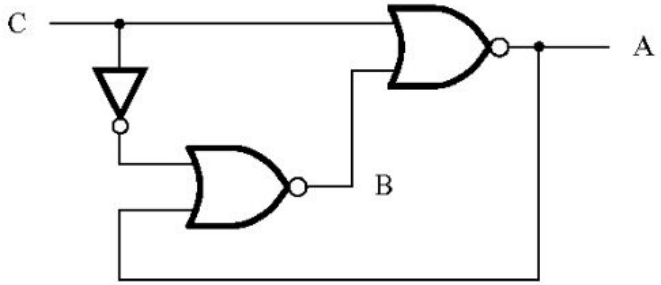
EL6463: Advanced Digital Design

Slides: Hammond Pearce

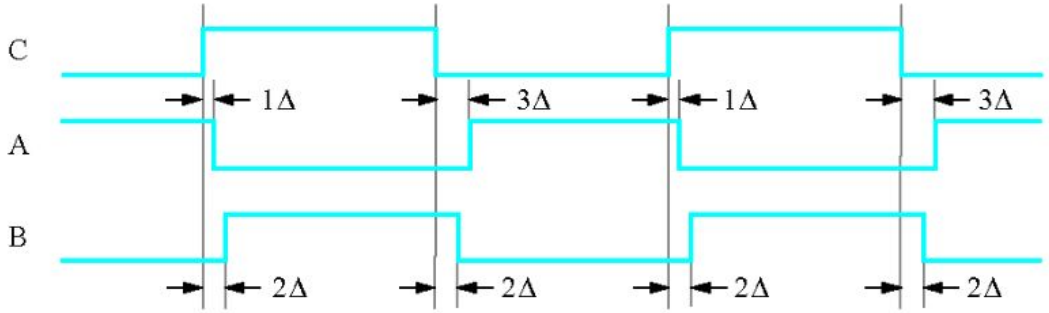
Real components take TIME to execute - propagation delay



Combinatorial Logic can be examined to find longest path

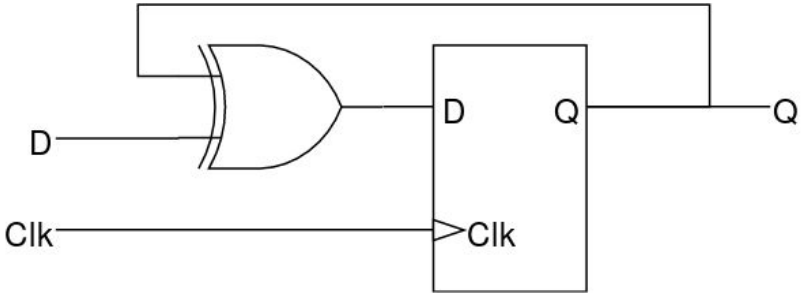


(a) Circuit



(b) Timing diagram

Test your understanding



Given T_{xor} = 0.2*ns,* and assuming an *ideal register* (no delays)

What is the maximum clock frequency this system can safely operate at?

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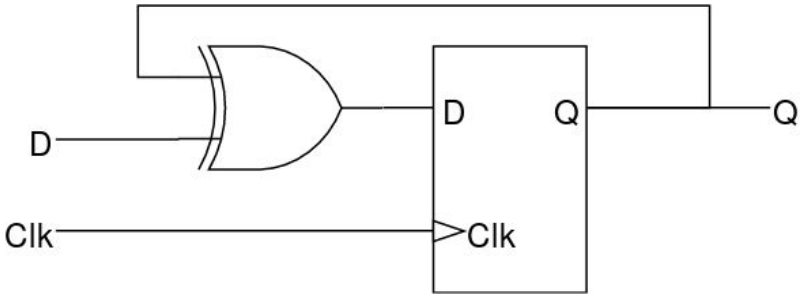


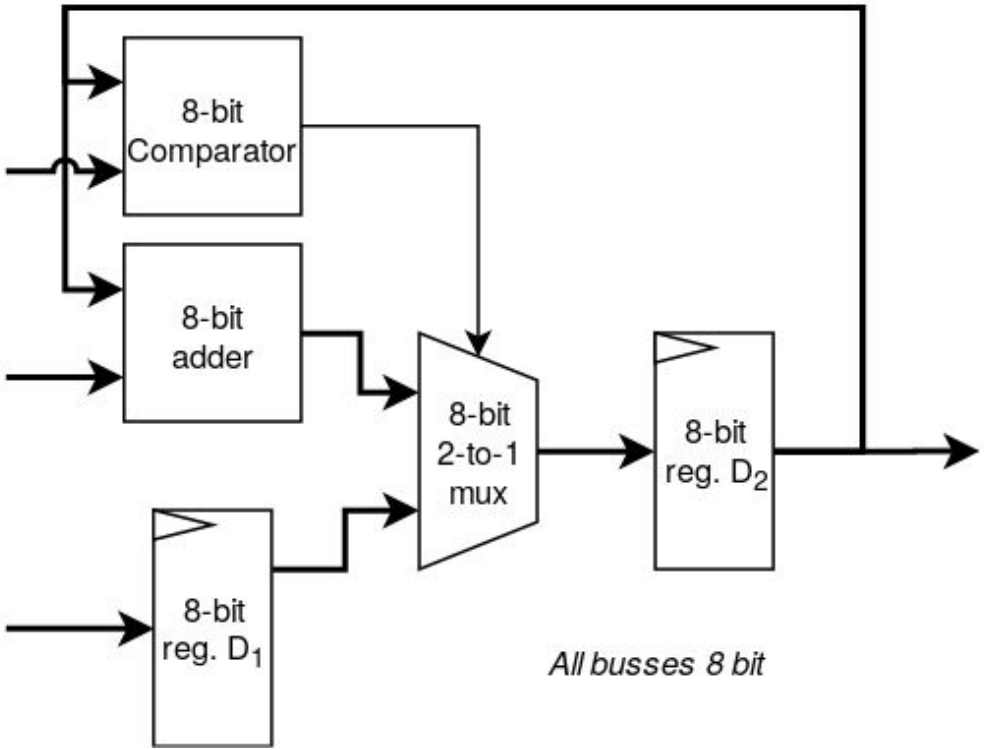
Given T_{xor} = 0.2*ns,* and assuming an *ideal register* (no delays)

What is the maximum clock frequency this system can safely operate at?

The loop has T_{xor} = 0.2*ns*

1 / 0.2*ns* = **5000 MHz = 5 GHz**

Test your understanding 2



Given

comparator propagation delay T_{cmp} is 4*ns*,

the adder propagation delay T_{add} is 6*ns*,

the multiplexer propagation delay T_{mux} is 3*ns*,

and the registers are ideal (i.e. no delay at all)...

Specify the critical path and find the maximum clock frequency this circuit can operate properly.

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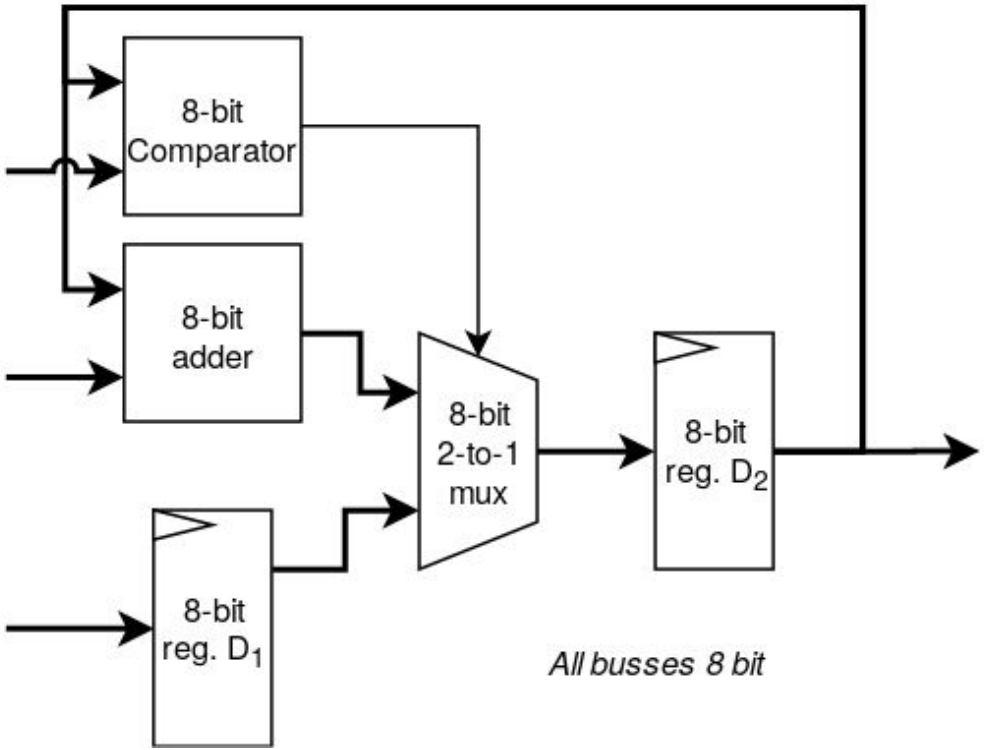

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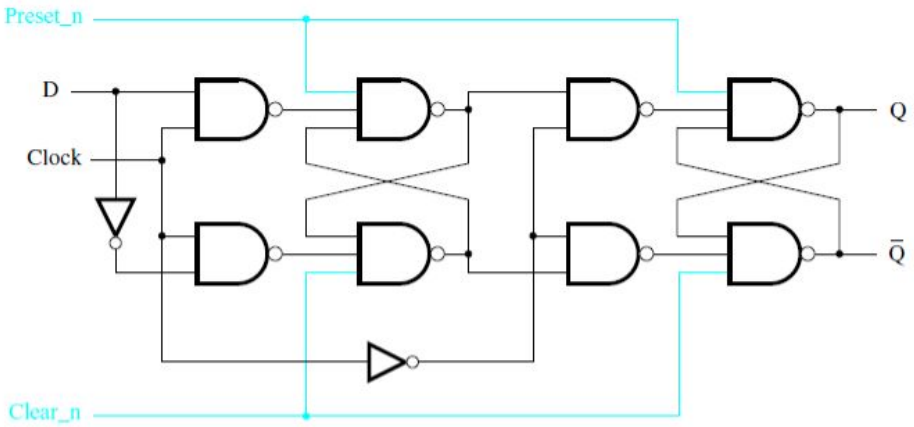
and the registers are ideal (i.e. no delay at all)...

Specify the critical path and find the maximum clock frequency this circuit can operate properly.

Comparator and Adder operate in parallel, Adder is slower.

Delay = Tadd + Tmux = 9ns,
1/9ns = **111MHz**

Registers are made of real components



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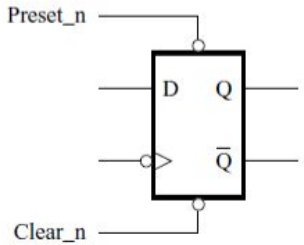
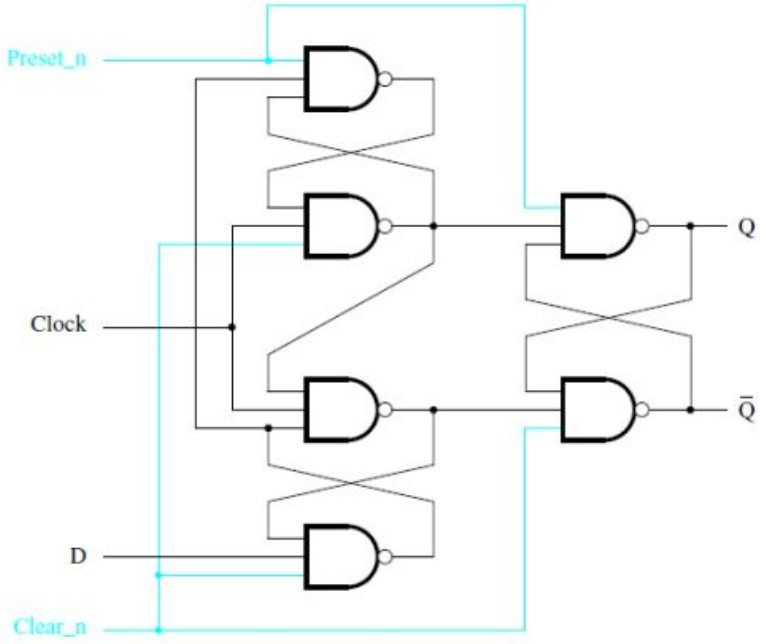


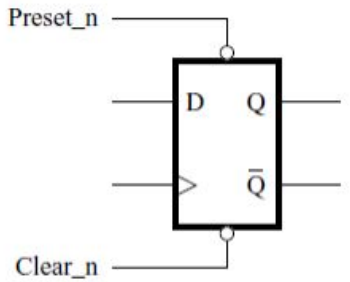
(b) Graphical symbol

- This design is called the Master/Slave Flip-Flop
- How does it work?

Many possible register layouts



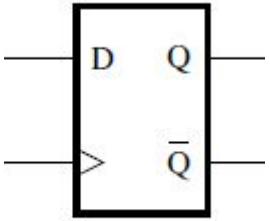
(a) Circuit

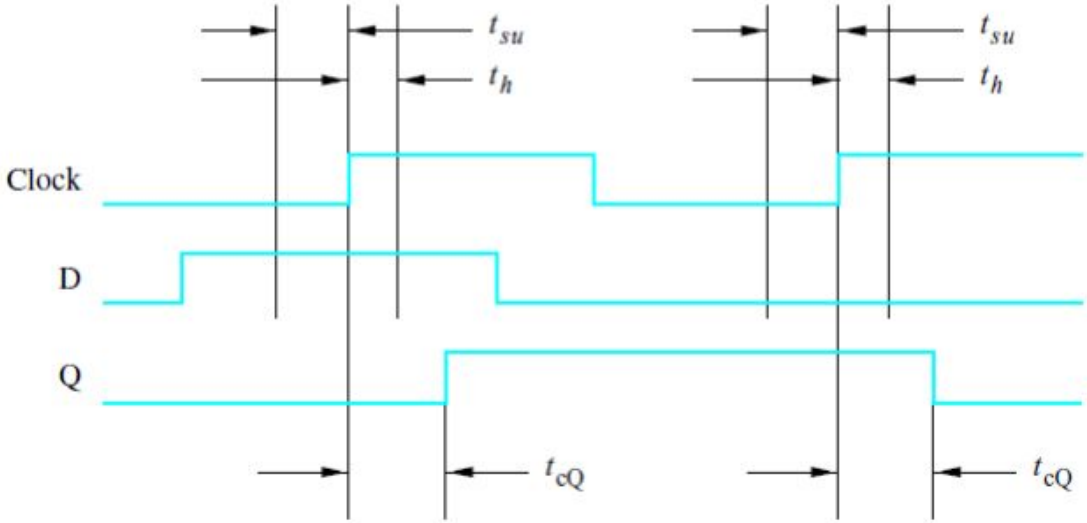


(b) Graphical symbol

- Reduced gates = Reduced cost

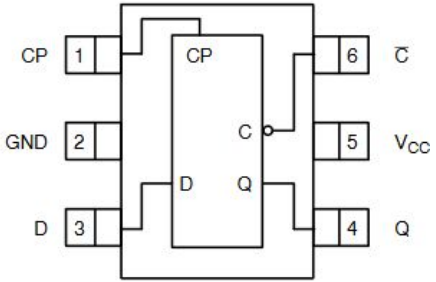
Characteristic Timing of a Register

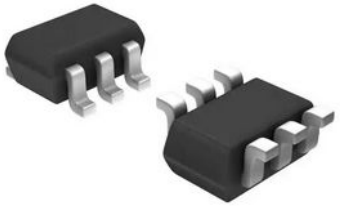




- tsu = set up time
- th = hold time
- tcQ = time to Q

Example - NC7SZ175P6S D-Type Flip Flop





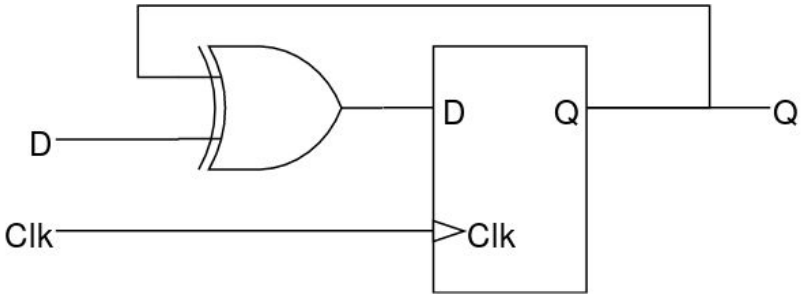
Symbol	Parameter	V_{CC} (V)	Conditions	T_A = +25°C Min	T_A = +25°C Typ	T_A = +25°C Max	T_A = −40 to +85°C Min	T_A = −40 to +85°C Max	Unit
t_{PLH}, t_{PHL}	Propagation Delay CP to Q (Figures 5, 7)	1.65	C_L = 15 pF, R_L = 1 MΩ	–	9.8	15.0	–	16.5	ns
		1.8		–	6.5	10.0	–	11.0	
		2.5 ±0.2		–	3.8	6.5	–	7.0	
		3.3 ±0.3		–	2.8	4.5	–	5.0	
		5.0 ±0.5		–	2.2	3.5	–	3.8	
		3.3 ±0.3	C_L = 50 pF, R_L = 500 Ω	–	3.4	5.5	–	6.2	
		5.0 ±0.5		–	2.6	4.0	–	4.7	
t_S	Setup Time, CP to D (Figures 5, 8)	2.5 ±0.2	C_L = 50 pF, R_L = 500 Ω	–	–	–	2.5	–	ns
		3.3 ±0.3		–	–	–	2.0	–	
		5.0 ±0.5			–	–	1.5	–	
t_H	Hold Time, CP to D (Figures 5, 8)	2.5 ±0.2	C_L = 50 pF, R_L = 500 Ω	–	–	–	1.5	–	ns
		3.3 ±0.3		–	–	–	1.5	–	
		5.0 ±0.5		–	–	–	1.5	–	

NC7SZ175P6X

Datasheet

Digi-Key Part Number	NC7SZ175P6XTR-ND - Tape & Reel (TR) NC7SZ175P6XCT-ND - Cut Tape (CT) NC7SZ175P6XDKR-ND - Digi-Reel®
Manufacturer	ON Semiconductor
Manufacturer Product Number	NC7SZ175P6X
Supplier	ON Semiconductor
Description	IC FF D-TYPE SNGL 1BIT SC70-6
Manufacturer Standard Lead Time	4 Weeks
Detailed Description	Flip Flop Element D-Type Bit Positive Edge 6-TSSOP, SC-88, SOT-363

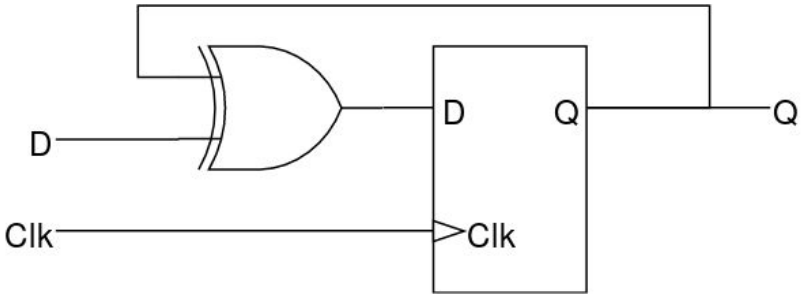
Test your understanding



Given $T_{xor} = 0.2ns$ and $T_{su} = 0.8ns$, $T_h = 0.3ns$, $0.8ns \leq T_{cQ} \leq 1ns$,

What is the maximum clock frequency this system can safely operate at?

Test your understanding



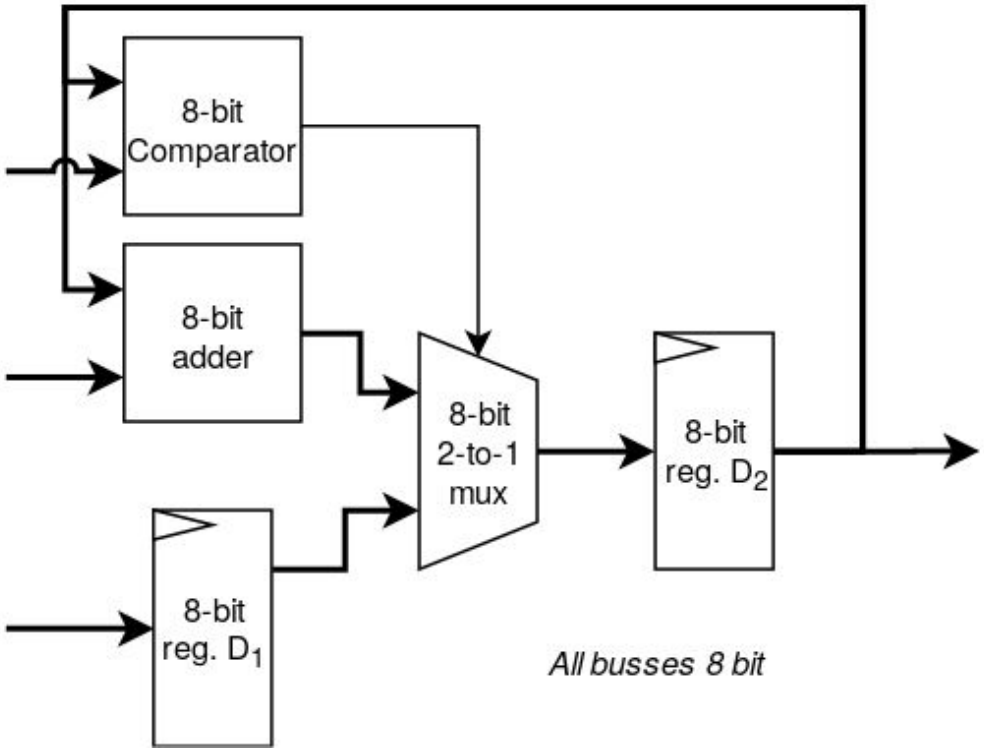
Given $T_{xor} = 0.2ns$ and $T_{su} = 0.8ns$, $T_h = 0.3ns$, $0.8ns \leq T_{cQ} \leq 1ns$,

What is the maximum clock frequency this system can safely operate at?

The loop has $T_{cQ} + T_{xor} + T_{su}$ (T_h is dominated) = 1 + 0.2 + 0.8 = 2*ns*

1 / 2*ns* = **500 MHz**

Test your understanding 2



Given

comparator propagation delay T_{cmp} is 4*ns*,

the adder propagation delay T_{add} is 6*ns*,

the multiplexer propagation delay T_{mux} is 3*ns*,

D_1 and D_2 have these timing characteristics:

$T_{su} = 0.8ns$, $T_h = 0.3ns$, $1ns \le T_{cQ} \le 1.2ns$.

Specify the critical path and find the maximum clock frequency this circuit can operate properly.

Comparator and Adder operate in parallel, Adder is slower. TcQ dominates Th.

Delay = Tadd + Tmux + Tsu + TcQ = 11ns,

1/11ns = **90.9MHz**

Clock Trees

- Wires themselves have propagation delay, meaning the *Clock* can *Skew*
- I.e. the same clock arrives at different times - causes cascaded errors
- Solution: H-Tree Clock Distribution