Anant Singh
Advanced Hardware Design
September 15, 2021

Homework 1

Deliverables-

1.a.i: Simulation Screenshots

Image 1: Simulation of And_Or_Verilog.v

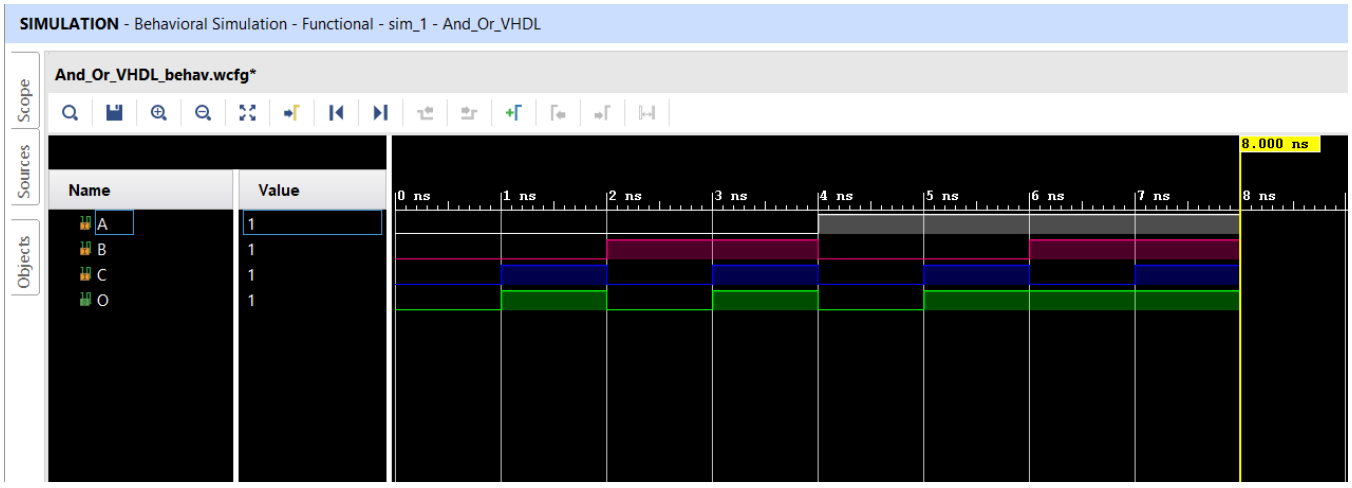

Image 2: Simulation of And_Or_VHDL.vhd

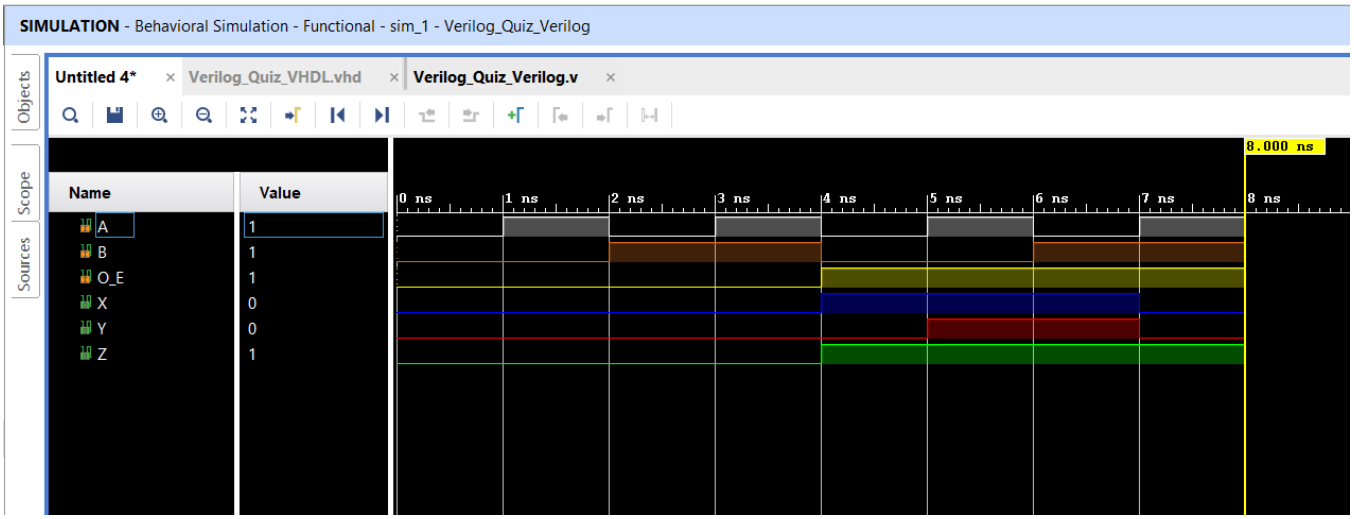

Image 3: Simulation of Verilog_Quiz_Verilog.v

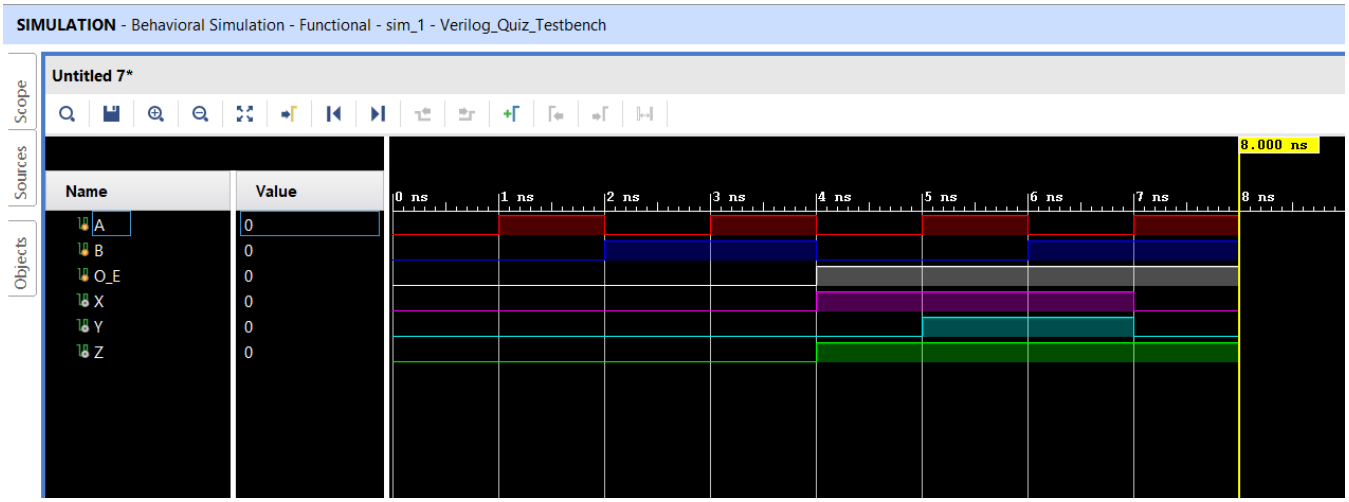

Image 4: Simulation of Verilog_Quiz_VHDL.vhd

1.b.i: Equivalent Logic Gate Circuit

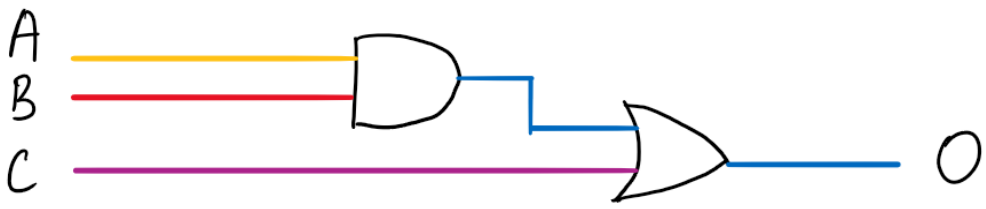

Image 5: Equivalent Logic Gate Circuit for And_Or_VHDL.vhd and And_Or_Verilog.v

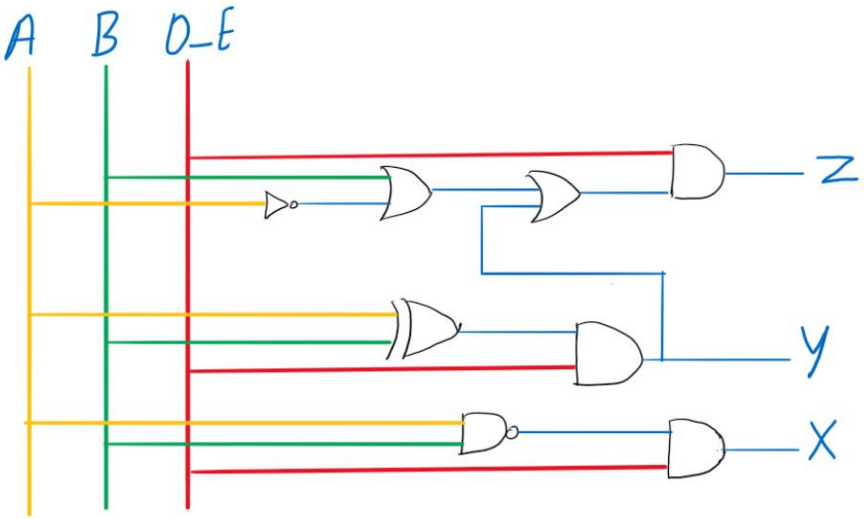

Image 6: Equivalent Logic Gate Circuit for Verilog_Quiz_VHDL.vhd and Verilog_Quiz_Verilog.v

1.c: Are the logic gates derived from the Verilog and VHDL equivalent?

1. And OR – Yes, the logic gates derived from the Verilog and VHDL are equivalent.

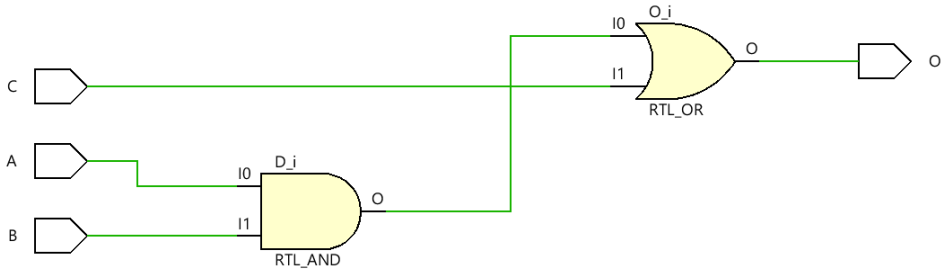

Image 7: Schematic of And_Or_VHDL.vhd and And_Or_Verilog.v

2. Verilog Quiz – Yes, the logic gates derived from Verilog and VHDL are equivalent, although schematics differ a bit in the logic implementation of NOT gate.

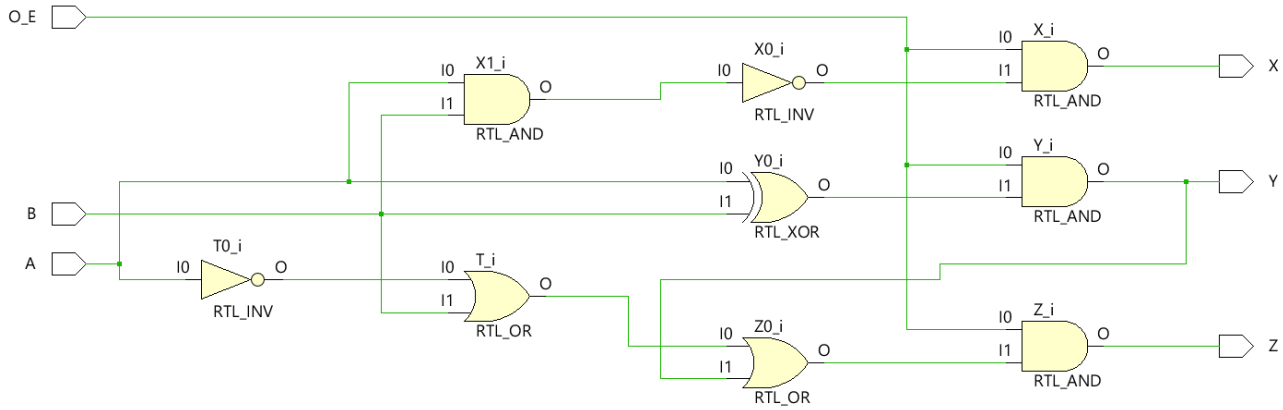

Image 8: Schematic of Verilog_Quiz_Verilog.v

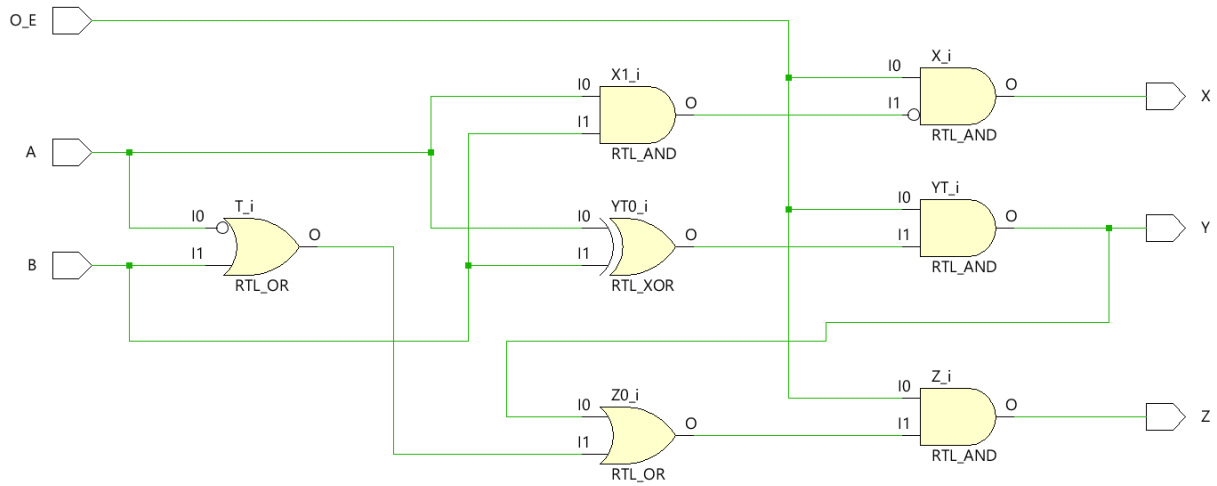

Image 9: Schematic of Verilog_Quiz_VHDL.vhd

2. Video Explanation of Designing and Simulating XYZ function using Vivado

Video Link: https://youtu.be/6D5etWOyZjs