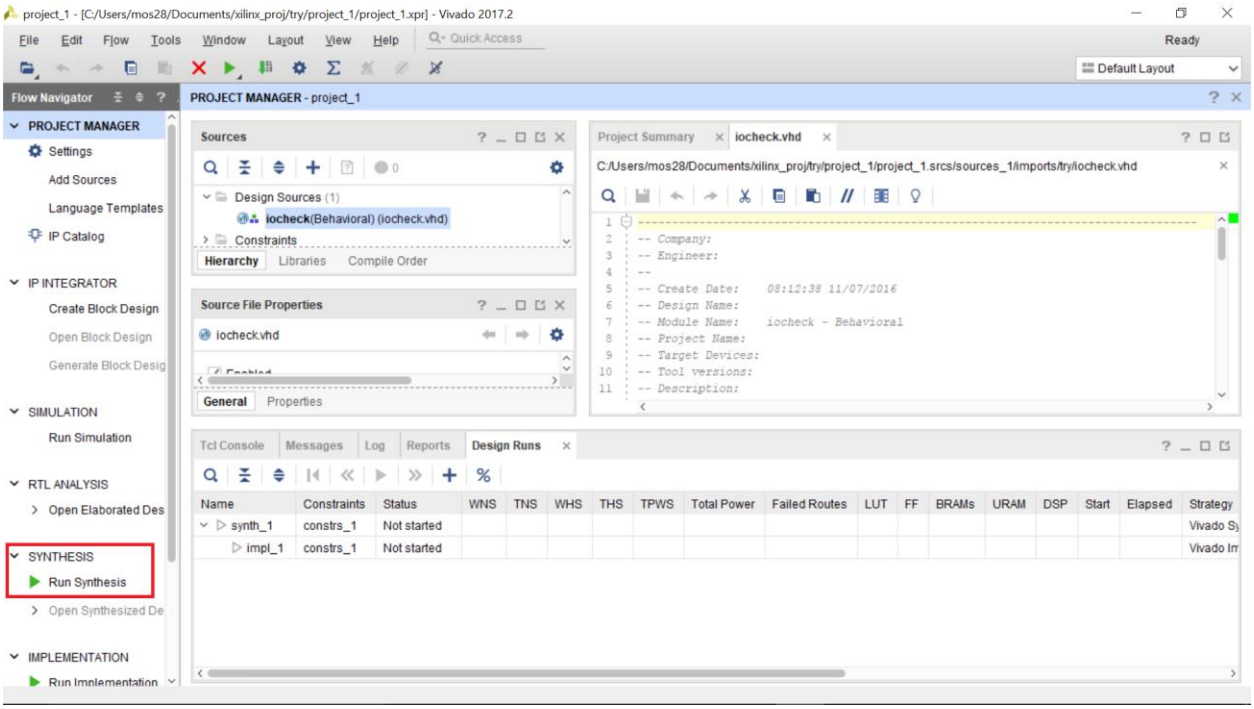
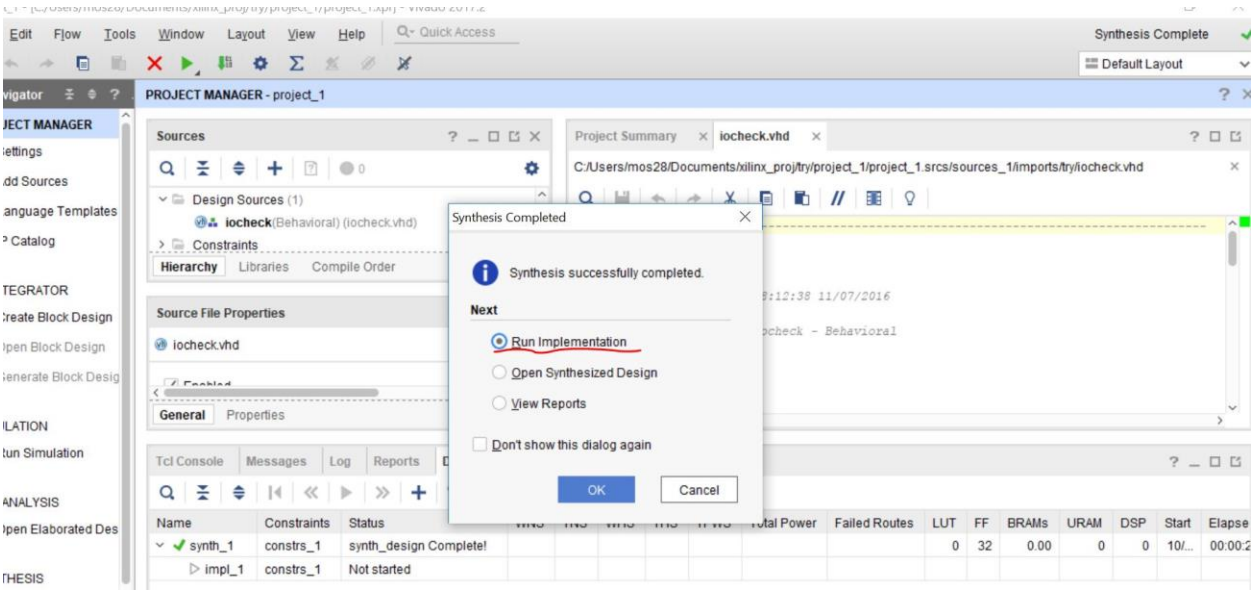
This tutorial deals with timing simulation and timing analysis on Vivado design suite.

After creating RTL project and source VHDL files follow the below steps for timing simulation:

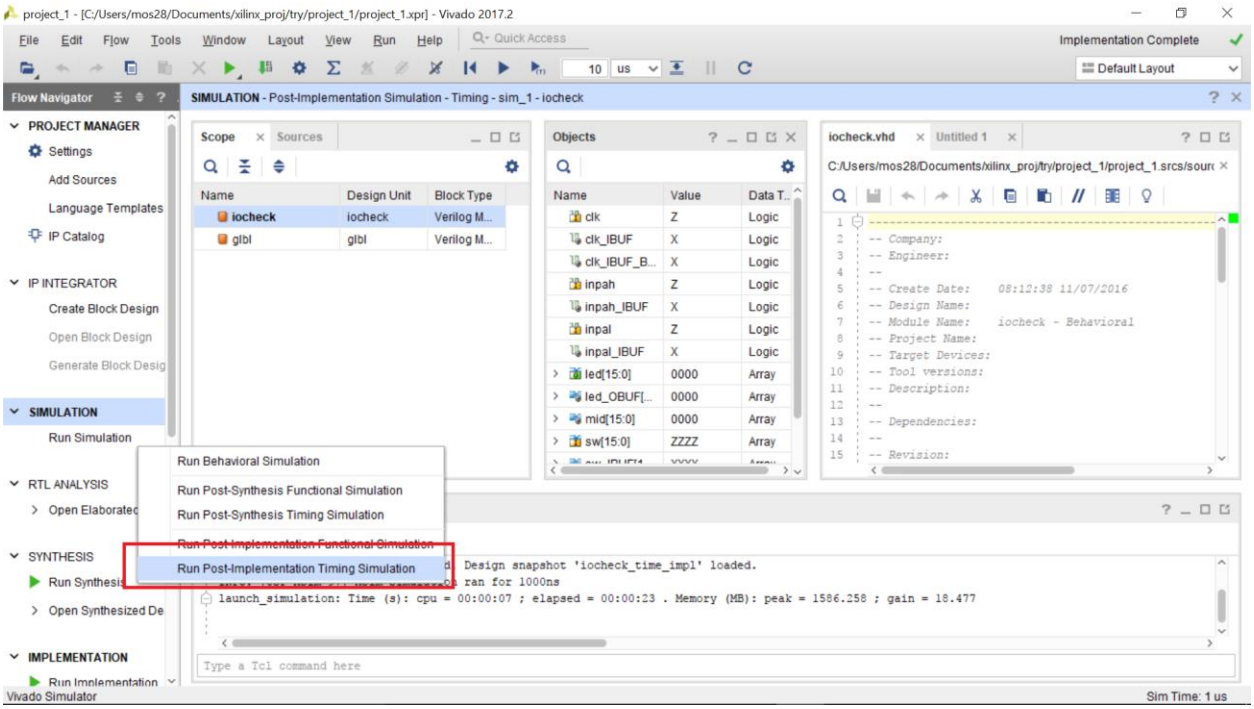
Step 1: Run synthesis:



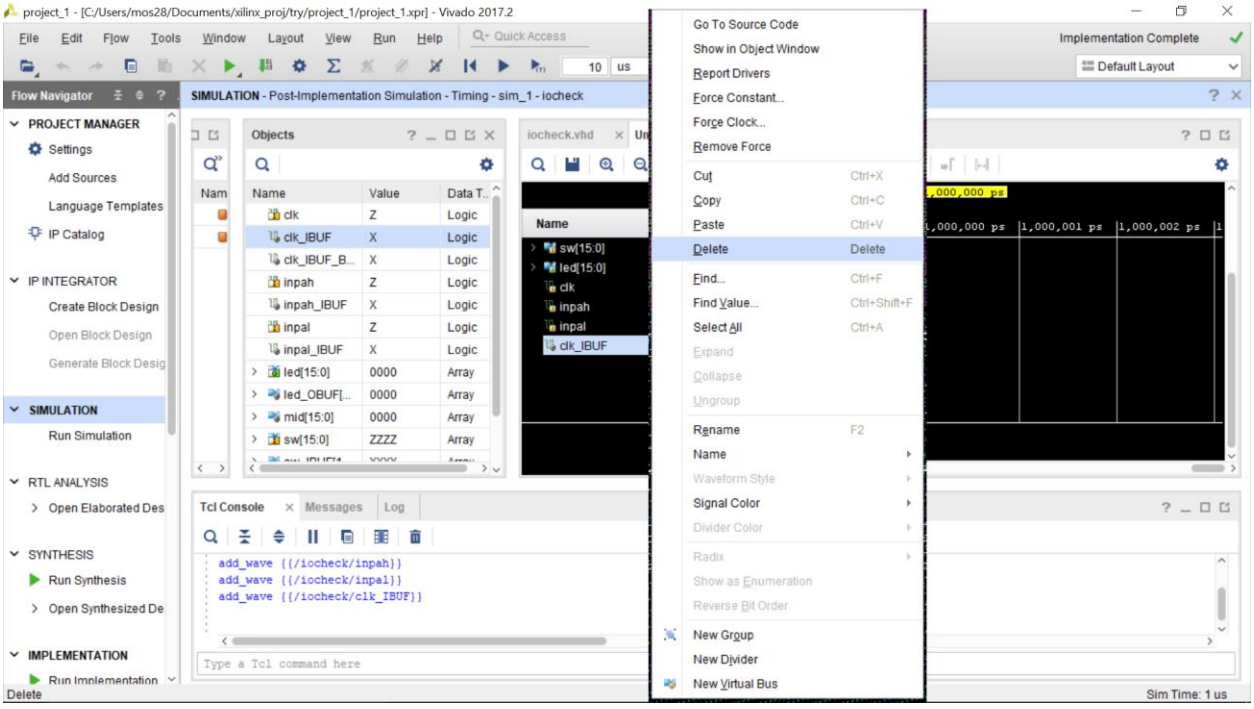
Step 2: after successful synthesis run implementation

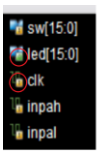


Step 3: Click on Simulation and select Run Post-implementation Timing Simulation



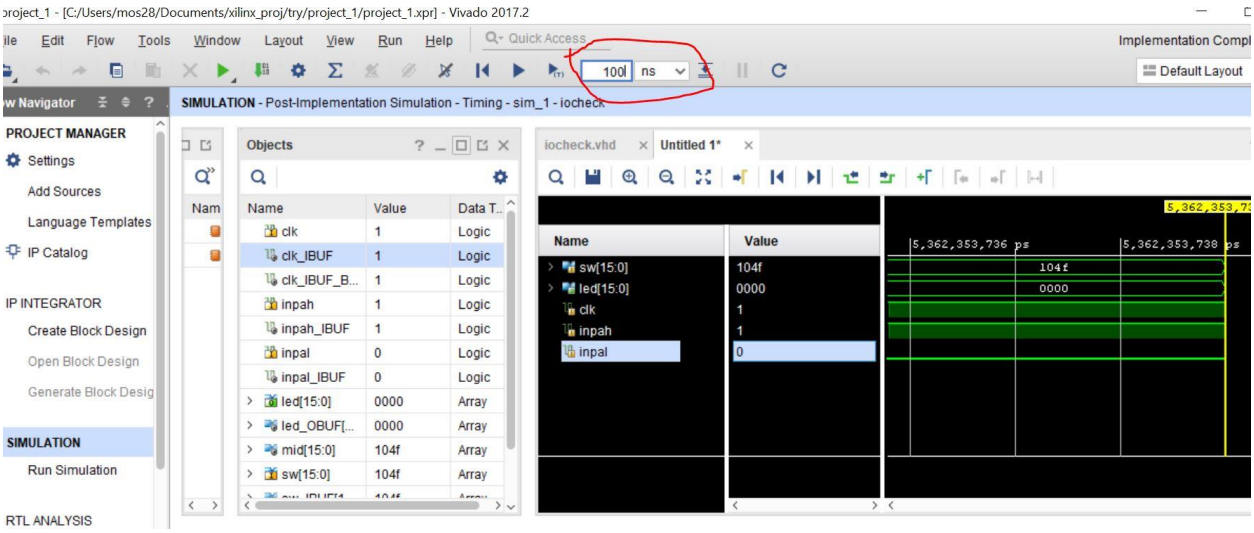
Step 4: The simulation window shows all the objects including internal signals. You select all and delete them and then add only the input and output objects.



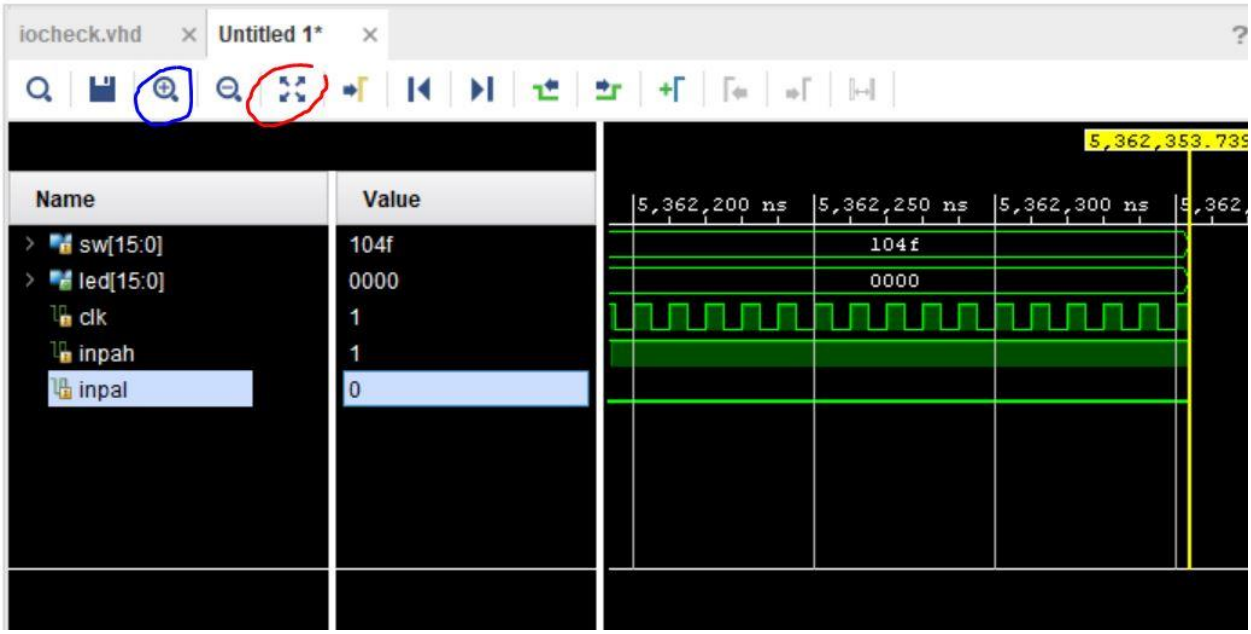


<- Input/outputs have these markings

Step 5: Force constant and clock as you did for functional simulation. Make sure you adjust the run time to as minimum as possible. The timing simulation does all delay computation hence takes time.



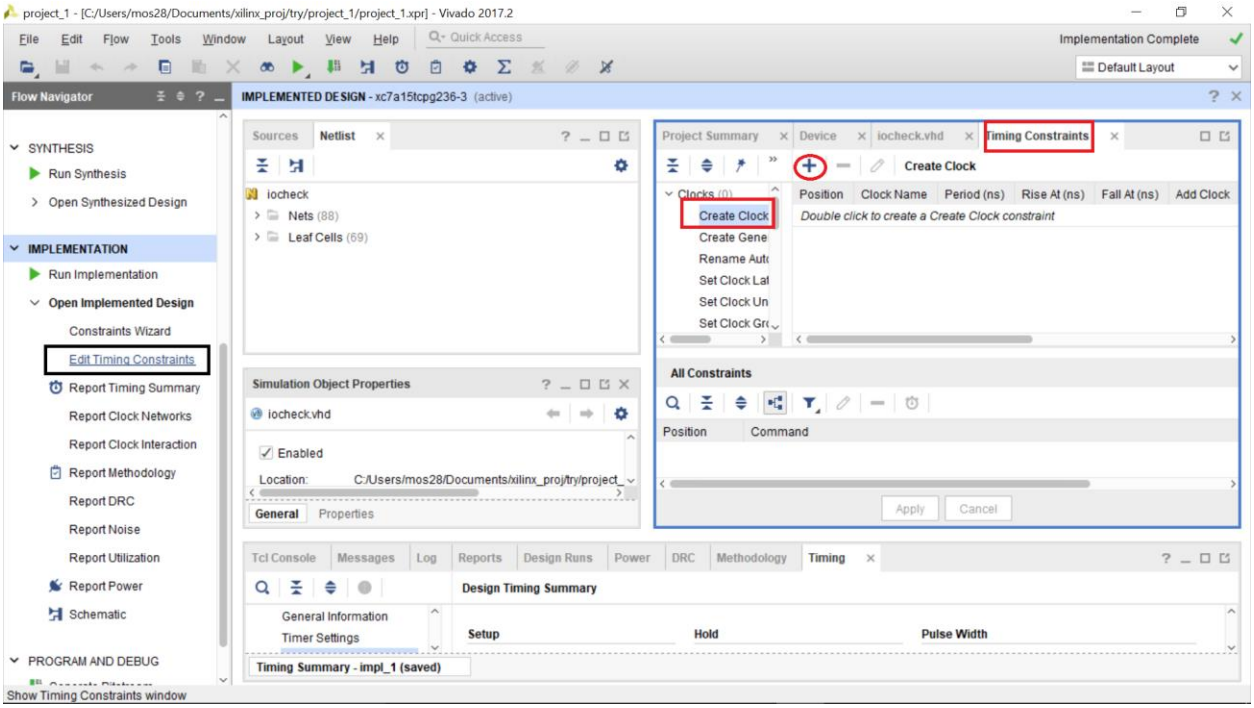
Step 6: Use the fit to screen button (in red circle) and zoom button to scroll through.



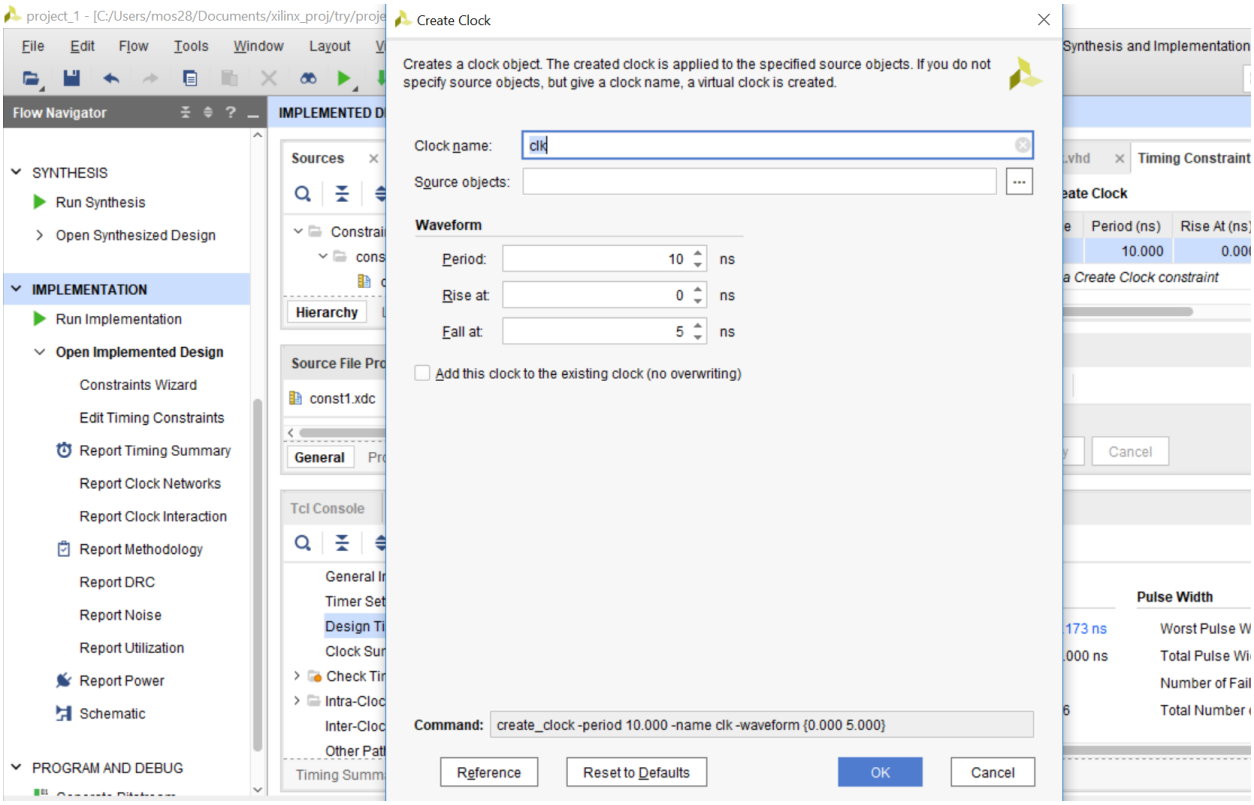
Timing Analysis, also known as static timing analysis gives worst case timing and critical path information

For timing analysis follow below steps:

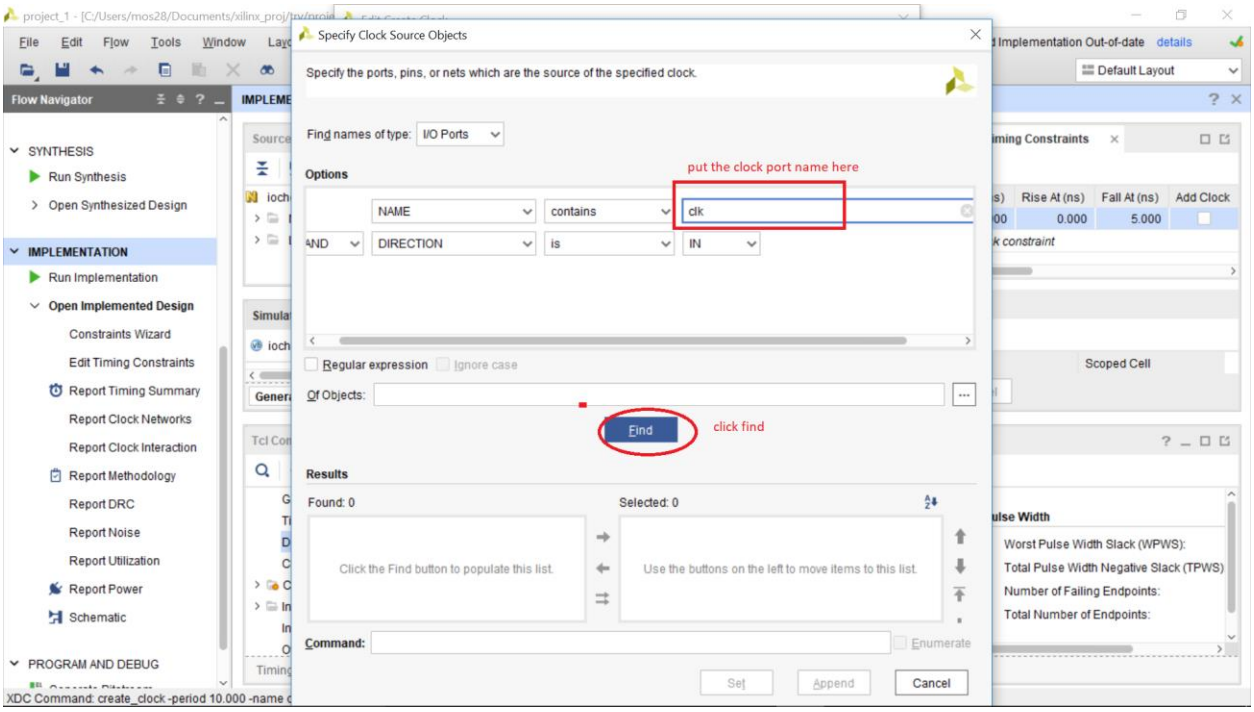
Step 1: edit timing constraints, where you give a targeted cycle time for design. Click on edit constraint. A window pops up, go to create clock tab and add a clock.



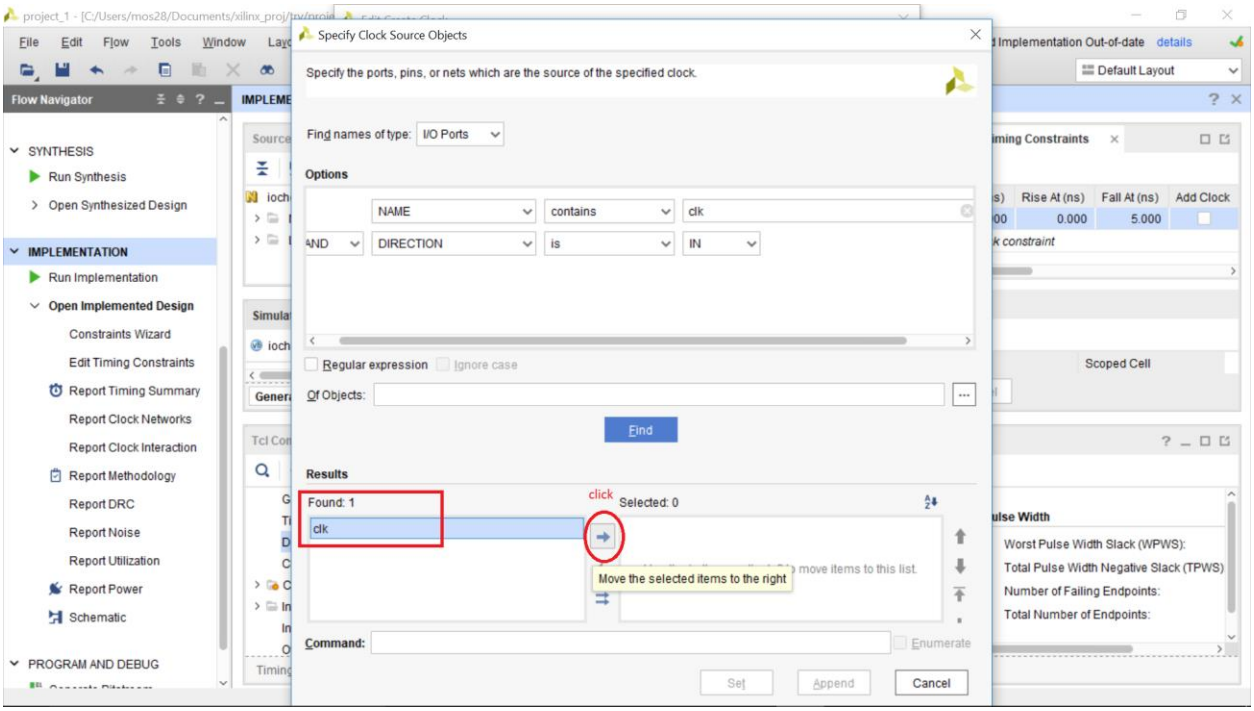
Step 2: add your clock name and time period: for example below add “clk” of period 10 ns.



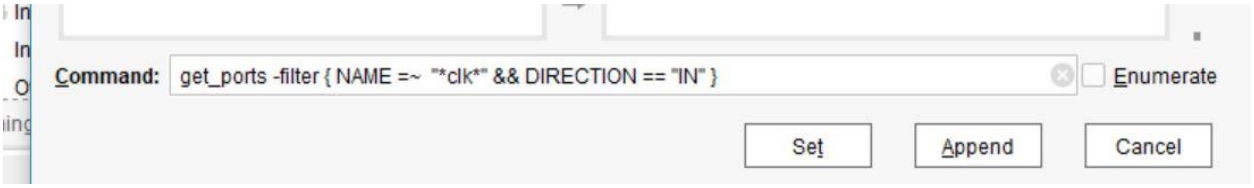
Step 3: click on source objects, a prompt like below pops up. Put your clock name and click find



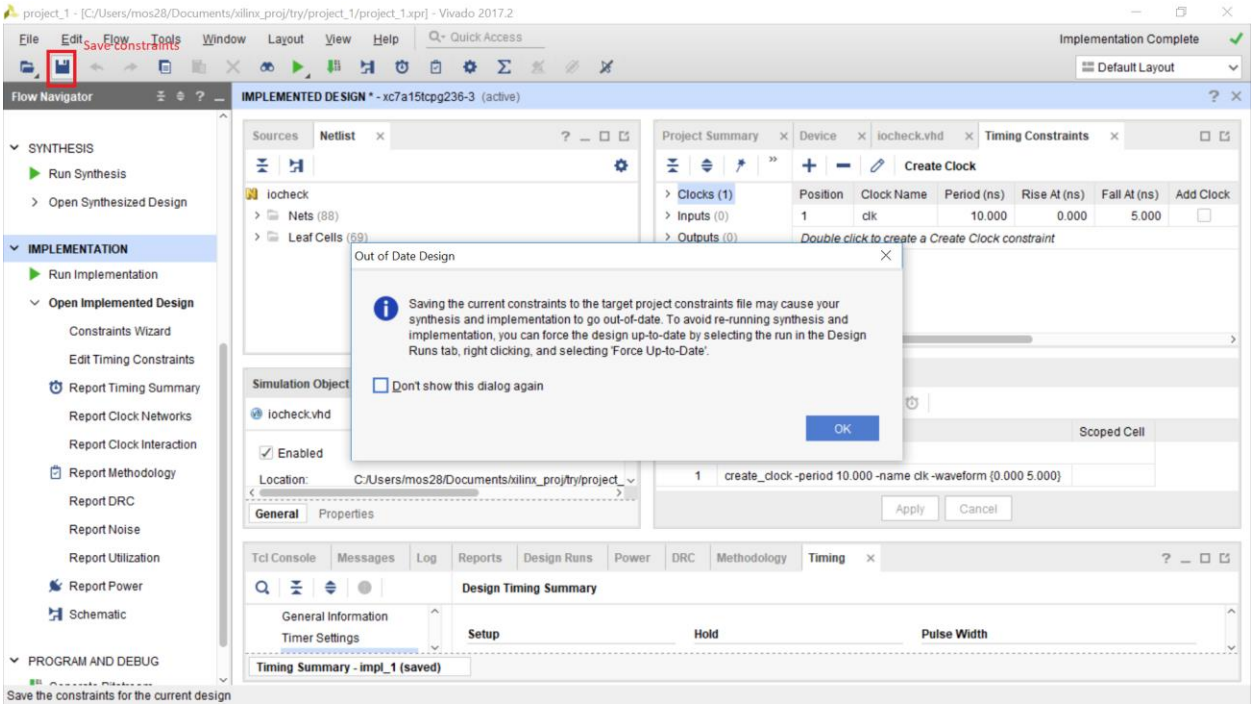
Step 4: It searches for clk name you provided among the source objects. Click on it and click on the move sign



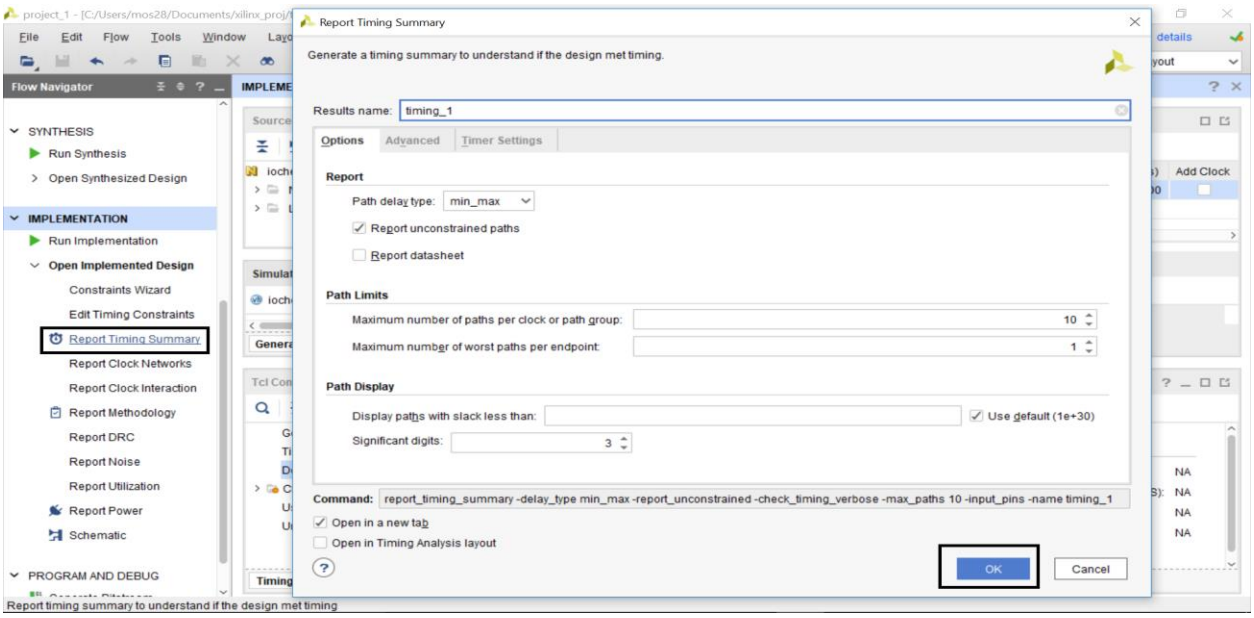
This gives a command like this, Click on “Set”



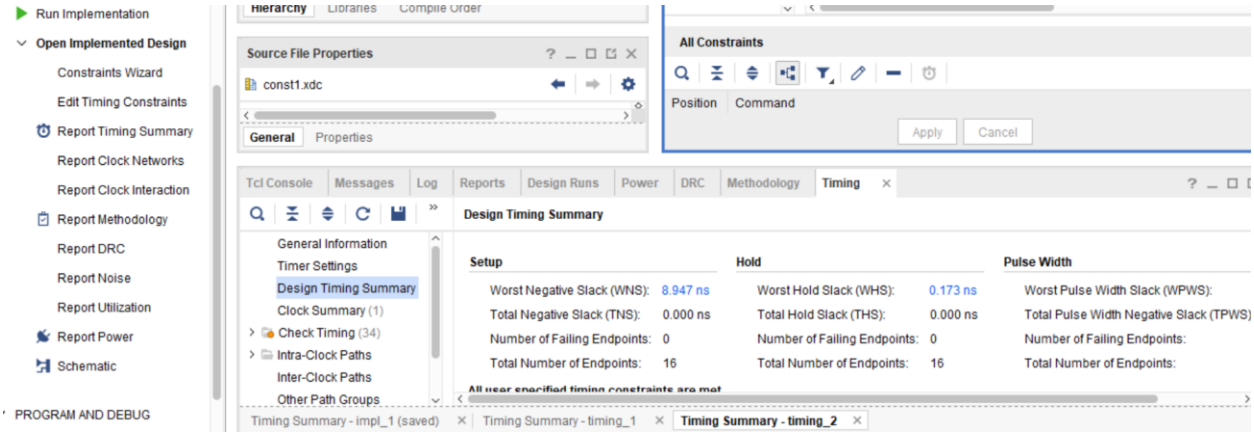
Step 5: save constraints



Step 6: You are set to run the timing reports, click on Timing Report Summary



Step 7: It shows a summary like this: with worst negative slack and number of failing paths with respect to your targeted clock speed.



Additional Reading:

https://www.xilinx.com/support/documentation/sw_manuals/xilinx2012_2/ug938-vivado-design-analysis-closure-tutorial.pdf