Homework 2 (5%) Due: 11:59 PM, Friday 24 Sept.

Counting and Functional Simulation

Overview

The purpose of this homework is to make a sequential counter design with multiple features.

Universal Counter Features

All counters that you will implement will output a 4-bit unsigned number. They will have the following I/O:

- clk: input clock
- rst: input active-high reset signal (i.e. reset upon "1")
- cnt_en: input enable signal for counting (i.e. when this is "1", count upon the rising clock edge)
- cnt: output 4-bit unsigned vector

Tasks:

1) Produce the following 4 counters.
   a) CounterA: VHDL, Counts UP, Upon reset: sets its value to the FIRST digit of your N number
   b) CounterB: VHDL, Counts DOWN, Upon reset: sets its value to the LAST digit of your N number
   c) CounterC: Verilog, Counts UP, Upon reset: sets its value to the FIRST digit of your N number
   d) CounterD: Verilog, Counts DOWN, Upon reset: sets its value to the LAST digit of your N number

Note: For the VHDL you may use either std_logic_unsigned or numeric_std.

2) Perform a functional simulation of each of the 4 counters. Ensure you test all functionality. Capture a screenshot of the functional simulation for each counter.

3) Synthesize the design to the schematic. Capture a screenshot of the schematic for each counter.

4) Write a short report which includes the figures from "2)" and "3)" and explains them (i.e. explain the key features in the schematics). If there are differences between the Verilog and VHDL hardware, note them and try to explain the differences.

Deliverables:

1. Submit a zip file with your Xilinx projects (including the VHDL and Verilog files) and the PDF report.