Homework 1 (5%) Due: 2:00 PM, Friday 17 Sept.

Basic Combinational Design (e.g, OR-AND and FULL ADDER) and Functional Simulation

Overview

The purpose of this homework is to encourage you to familiarise yourself with the tools and languages used in this course.

Part 1: Set up Vivado Tools

In this course, we will be using Xilinx Vivado Design Suite tools for our digital design. Vivado provides synthesis and simulation functionality. There are two options for you to use Vivado tools:

1. Through VPN + Han Solo (Preferred)
    - https://www.nyu.edu/life/information-technology/getting-started/network-and-connectivity/vpn.html
    - In this course, we will be providing you with a remote environment (a research server) where the Vivado tools come pre-installed. To use this environment, follow the instructions (provided separately). This is a linux-based environment. See the FastX3 User Guide on BrightSpace under the Resources folder.
2. On your own machines
    - Xilinx offers a free version of the tools that you can download and install on your own computers.
    - YouTube instructions: https://www.youtube.com/watch?v=ZTAfESmWKXE
    - Vivado can be installed on Windows and Linux platforms
    - If you use a Mac, you will need to use BootCamp or set up a Virtual Machine with a Windows or Linux guest (VirtualBox and VMware (Workstation Player) are free options).

Check that you have a working setup using at least one of these options.

Part 2: Model simple designs and test them

In the lectures, you have been introduced to concepts around modeling digital hardware designs using a Hardware Description Language (HDL). Your task is to model the following using **both VHDL and Verilog**.

Tasks:

1. Implement and Simulate a design (in **both** VHDL and Verilog) that can perform a simple AND-OR operation
   Note: Output function should be O = (A and B) or C;
2. Implement and Simulate a design (in **both** VHDL and Verilog) that can perform the *xyz* function on slide 23 of the Lecture1_slide.pptx
   Note: you may reuse the provided Verilog, but you will need to translate it to the equivalent VHDL
3. Film a short video explaining the design and simulation process you used. You may choose to use the recording system built in to Powerpoint, or a screen recording software such as OBS (https://obsproject.com/) (which is free and open source).

Deliverables:

1. Submit a zip file with your VHDL and Verilog files and a PDF report containing:
    a. Screenshots of your simulation outputs
        i. Test cases: All possibilities of all inputs
    b. Submit Block Diagram.
        i. Draw the equivalent logic gates for each of your four codes.
    c. Answer the question: are the logic gates derived from the Verilog and VHDL equivalent?
2. Upload a video to YouTube, include the link to that video in the PDF.
    a. Video can be 3 minutes max.
    b. Explain the process of the design and simulation of the *xyz* function.