Instructors:

Ramesh Karri rkarri@nyu.edu, cell: 917 363 9703 (Prof. Karri)

In Class Lecture Times: Friday, 14:00--16:30 ET (New York Time)

Location: 2 MetroTech Center Room 9.009

Office hours (will be online): TBD

For appointments: please send email

Teaching Support Team:

- Hammond Pearce (hp2265@nyu.edu)
- *Jitendra Bhandari (jb7410@nyu.edu)*
- Animesh Basak Chowdhury (abc586@nyu.edu) For 1-2 Lectures
- TBD

Integrated Circuits and Field Programmable Gate Arrays (FPGAs) are useful in telecommunication, video processing, cryptography, control, and biomedical applications. This course will provide an understanding of FPGA-based design starting from a VHDL/Verilog (An industry standard) hardware description language specification of a design or starting with c specification. One will learn how to model, simulate, and synthesize digital logic using a hardware description language (VHDL/Verilog). Initially, you will model simple digital logic building blocks (AND, OR, XOR, Multiplexer, Demultiplexer, Flip Flop, etc.). You will then model larger digital logic building blocks (Rotate by a fixed amount, Data dependent rotate, Add, and Subtract). You will then model controllers. You will compose the building blocks into a digital logic datapath + controller and implement it on an FPGA. The course is structured as a combination of lectures and homeworks (labs). By the end of the course, students should be able to:

1. (a) Design a complex digital system using VHDL Hardware Description Language. (b) Validate using VHDL Testbenches

2. (a) Design a complex digital system using Verilog Hardware Description Language. (b) Validate using Verilog Testbenches

3. (a) Design a complex digital system using c-based specification as a HDL. (b) Validate using c/RTL Testbenches

Lecture Schedule (Tentative)

Week	Instr.	Lecture - Fridays (2-4.30)	Mode	Assessments Start/End on Fridays		Topics/Notes (Tentative) *Timing/order might vary depending on how the semester progress*
				Release	Due	
1	RK	HDL: Sept 3	In Person	HW1		**Intro to VHDL, Verilog,** FPGA Design I – Model digital logic blocks using VHDL (AND, OR, XOR, MUX, DeMUX, Flip Flop, Rotate input by a fixed amount, data dependent rotate, add, subtract). **Hands-on activity:** Write and compile a VHDL Model, a Verilog Model.

Week	Instr.	Lecture - Fridays (2-4.30)	Mode	Assessments Start/End on Fridays		Topics/Notes (Tentative) *Timing/order might vary depending on how the semester progress*
				Release	**Due**	
2	RK	HDL: Sept 10	In Person			Check models are functionally correct (Functional Simulation) and correct from a timing perspective (Timing simulation) using vivado simulator. Hands-on activity: Check VHDL/Verilog models are functionally correct (Functional Simulation) and correct from a timing perspective (Timing simulation) using vivado simulator.
3	RK	HDL: Sept 17	In Person	HW2	HW1	*Sequential designs in Verilog, Blocking / Non-blocking assignments discussion. Testbenches* in VHDL and Verilog.
4	RK	HDL: Sept 24	In Person			*Sequential Design Principles and Concepts. Finite State Machines (FSMs).* ***Hands-on activity:*** *Paper design of FSMs from Plain Language Descriptions (design specification, peer exchange and draw).* ***Hands-on activity:*** *Write and compile FSMs in HDL, controller + datapath design. Testbench design.*
5	RK	HDL: Oct 1	In Person	HW3	HW2	*Study FPGA development board- What is an FPGA? FPGA Architecture. How to Map a design onto the FPGA development board. Use placement and other constraints.*
6	RK	HDL: Oct 8	In Person			*"Simple Function" (RC5) and its components. Structural Modeling. Simple Testbenches*
7	RK	HDL: Oct 15	In Person		HW3	Real Life Application I - Model RC5 Encryption (with fixed round keys) using HDL. Perform Functional and Timing simulation. *Testbench*
8	RK	HDL: Oct 22	In Person	Project **Exam I**		Real Life Application II – Model RC5 Round Key Generation application and perform Functional and Timing Simulation. Controller modeling. Testbench **Take home exam (One week); 3 problems;**
9	RK	HDL: Oct 29	In Person	HW4	**Exam I**	Structural Modeling – Understand how to connect components structurally. Connect RC5 Encryption with Round-Key generator to create RC5 Encryption Accelerator. *Testbenches*
10	RK	HDL: Nov 5	In Person			No Lecture: CSAW week (attend CSAW events and submit report for participation)
11	RK	HLS: Nov 12	In Person	HW5	HW4	FSM+Datapath Re-cap: Mid-Term Debrief/Walkthrough (support for the project) Intro to C-based Design (or High-Level Synthesis-HLS) (Kastner Chapter 1, 2)
12	RK	HLS: Nov 19	In Person		Project Milestone 1	HLS Continued (Kastner Chapter 2 FIR Filters)

Week	Instr.	Lecture - Fridays (2-4.30)	Mode	Assessments Start/End on Fridays		Topics/Notes (Tentative) *Timing/order might vary depending on how the semester progress*
				Release	Due	
13		November 26				*No class: Thanksgiving*
14	RK	HLS: Dec 3	In Person*		HW5	HLS Continued (Kastner Chapter 5 -- FFT), C-based Co-simulation
15	RK	HLS: Dec 10	In Person		Project Milestone 2	HLS Continued (Kastner Chapter 5 continued), C-based Co-simulation **+ Interviews for Project Milestone II**
16	RK	Dec 17 (exam{ TBD by registrar)	In Person	**Exam II**	Project Final	**Take-home exam (One week); 3 problems** **Exam release no later than Friday, Dec. 18**
	RK	Dec: 21	In Person		**Exam II**	**Project final submission (code + report + video + poster): no later than Monday, December 21 (i.e., you can submit earlier)** **Exam return no later than 11:55 PM, Thursday, Dec. 24th (i.e., you can submit earlier)**

Resources:

- Vivado & Vivado HLS installation video. https://www.youtube.com/watch?v=ZTAfESmWKXE
- NYU VPN access: https://www.nyu.edu/life/information-technology/getting-started/network-and-connectivity/vpn.html
- Han Solo Access Guide: https://drive.google.com/file/d/1V2GAf6lrQXz53uxP5pNh2HQTLqxS1LuH/view?usp=sharing
- NYU Classes: Forums
- Note: No FPGA required this year
- You will need access to the Internet and a computer (laptop).
    - Windows or Linux preferred, Virtual Machine on MacOS is okay

Assessment Overview (Tentative):

- Take-home exams: 2 x 20 -- **40 points**
- Homework Assignments: 5 x 5 -- **25 points**
- Project: 30 -- **30 points**
- Class Participation: 5 -- **5 points**
    - NYU Forums? Set a "discussion" question per lecture for students to answer or ask students to post a question

        - 5: Asks relevant questions in most lectures
        - 3-4: Asks in some lectures
        - 1-2: Asks sporadically
        - 0: Does not engage
- Maximum: **100 points**

Homeworks (Tentative Topics):

- HW 1: Basic Combinational: (e.g, left rotate and right rotate). Function Simulation
    - Part 1: Set up Vivado HLx
    - Part 2: Model a few simple operations
- HW 2: Adv. Combinational
    - Functional Simulation, Timing Simulation
- HW 3: Sequential Logic
    - FSM Design
    - Implement state machines (counters, pattern recognizers, controllers etc. e.g.complete RC5. Testbench Encryption+Decryption function with fixed keys.)
    - Testbench
- HW 4: Hierarchical Designs (putting things together)
    - Control and Datapath Design
    - Structural Modeling – Combine Key Exp, Simple, Inverse Function modules to implement a full RC5 Module; Testbench.
- HW 5: HLS
    - Part 1: Simple C design, explore different optimizations, look at synthesized code
    - Part 2: More complex C design, ask students to come up with the best optimizations OR plot a graph of performance/resource trade-offs
    - C-based design – RC5 encryption/Decryption. Testbench

Exams: This class will have two exams (i) Mid-term Exam [Design and validation of RTL designs (Verilog and VHDL)] and (ii) Final Exam [Covers the whole course, including HLS]

Class Project: Last year it entailed designing and implementing an 8-bit processor on an FPGA (Implementing about ten instructions). The final report included: 1. Overview of the processor. 2. Functional Simulation of the processor; 3 Timing Simulation of the processor, 4. The testbench; 5. This year it may be different (Details to Follow).

Textbooks: This course does not have a mandatory textbook. See course notes in the resources folder. The following texts contain useful material relevant to the course. Some of these books have background information at the level of an undergraduate digital logic design course. So please go over those chapters in case you need a refresher on these topics.

1. VHDL Programming by Example by Douglas L. Perry ISBN 007140070-2

2. VHDL a starters guide by Sudhakar Yalamanchili

3. One more book on VHDL: https://ebookcentral-proquest-com.proxy.library.nyu.edu/lib/nyulibrary-ebooks/detail.action?docID=5921331

4. Another book on Verilog (same author): https://ebookcentral-proquest-com.proxy.library.nyu.edu/lib/nyulibrary-ebooks/detail.action?docID=5918767

5. Book on C-based design: http://kastner.ucsd.edu/hlsbook/