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Advanced Hardware Design
October 1, 2021

Homework 3

Deliverables-

2. Simulation Screenshots

2.1 AND-OR: VHDL Testbench

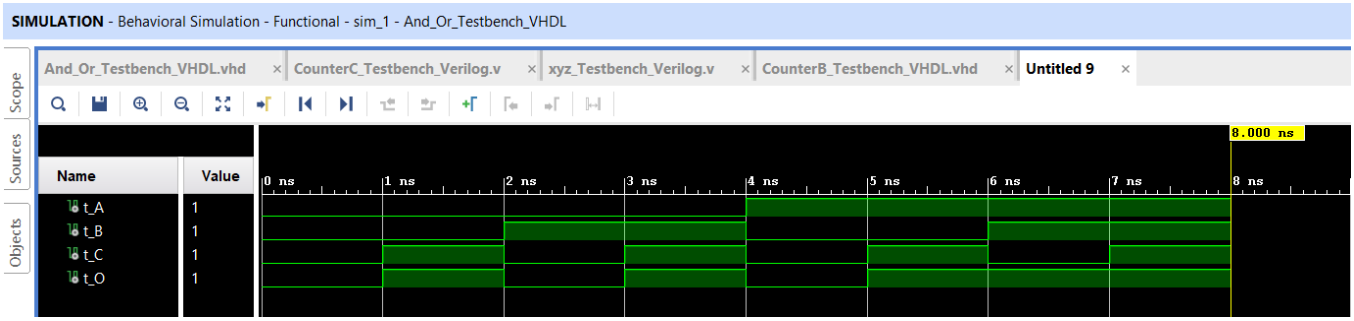

Image 1: Simulation of And_Or_Testbench_VHDL.vhd

2.2 xyz: Verilog Testbench

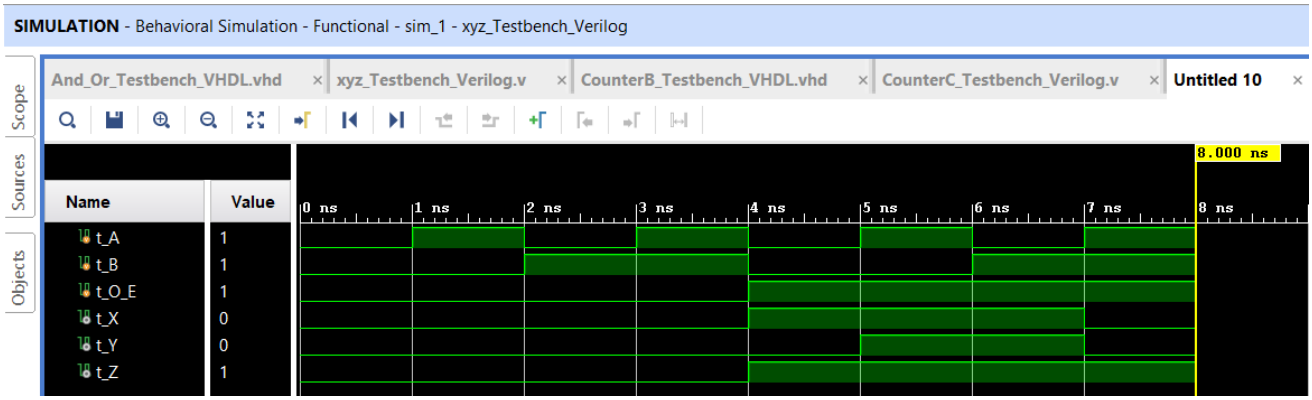

Image 2: Simulation of xyz_Testbench_Verilog.v

2.3 Counter B: VHDL Testbench

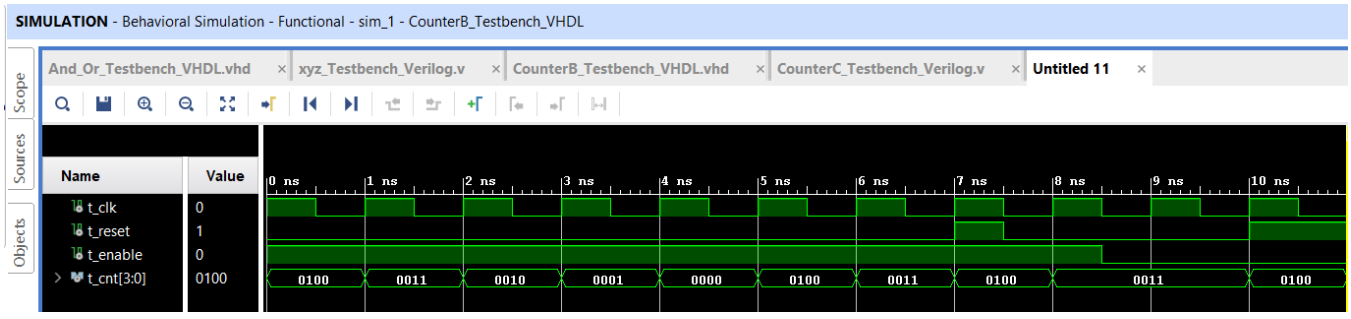

Image 3: Simulation of CounterB_Testbench_VHDL.vhd

2.4 Counter C: Verilog Testbench

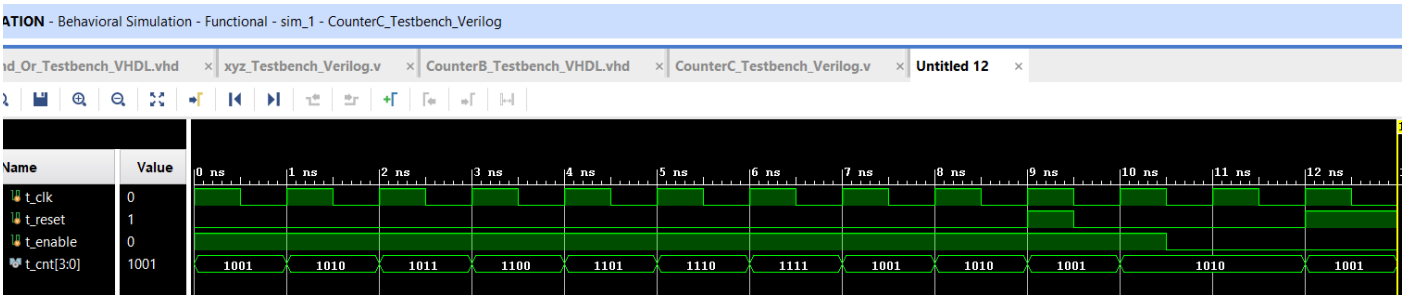

Image 4: Simulation of CounterC_Testbench_Verilog.v

3. Testing VHDL by Verilog Testbench and Vice Versa

Yes, it is possible. All the code to test VHDL code by Verilog Testbench and vice versa is in the testbench files as commented block.