Homework 3 (5%) Due: 11:59 PM, Friday 01 Oct.

Automated Testbenches for Verification

Overview

The purpose of this homework is to learn and practice making testbenches for functional validation of your RTL designs.

Your Current Designs

So far in HW1 and HW2 you have produced the following designs:

1) HW1
   a) AND-OR: VHDL
   b) AND-OR: Verilog
   c) xyz: VHDL
   d) xyz: Verilog
2) HW2
   a) CounterA: VHDL, Counts UP, Upon reset: sets its value to the FIRST digit of your N number
   b) CounterB: VHDL, Counts DOWN, Upon reset: sets its value to the LAST digit of your N number
   c) CounterC: Verilog, Counts UP, Upon reset: sets its value to the FIRST digit of your N number
   d) CounterD: Verilog, Counts DOWN, Upon reset: sets its value to the LAST digit of your N number

In HW3 you will now be producing test benches for these designs. You will need to produce 4 test benches, one for each of the following:

1) HW1 AND-OR (a), testbench written in VHDL
2) HW1 xyz (d), testbench written in Verilog
3) HW2 (b) CounterB, testbench written in VHDL
4) HW2 (c) CounterC, testbench written in Verilog

Tasks

1) Implement the above test-benches as described, using the languages as noted.
   a) The test-benches should be fully automated and test **all** functionality.
      i) **'All** functionality' means every combination of inputs and behaviors.
      ii) For the counters, where the behavior depends on the N number, the test benches should be tailored to the correct values for your N number.
   b) Ensure that the test-benches check the output for correctness at each step of execution, and print 'all tests passed' at the end of the simulation if all tests pass.

2) Using the test-benches, perform simulations and capture screenshots of the waveform output (zoom out to get all data in one screenshot)

3) Using the VHDL test-bench (1), is it possible to validate the AND-OR from HW1 (b) which is written in Verilog? Note in a 'comment block' in **each** of your test-bench files if it is possible to join the Verilog Designs to the respective VHDL test benches and vice versa.

Deliverables:

1. Submit a zip file with your Xilinx projects (including the VHDL and Verilog files) and a PDF file containing the screenshots and captions describing them.