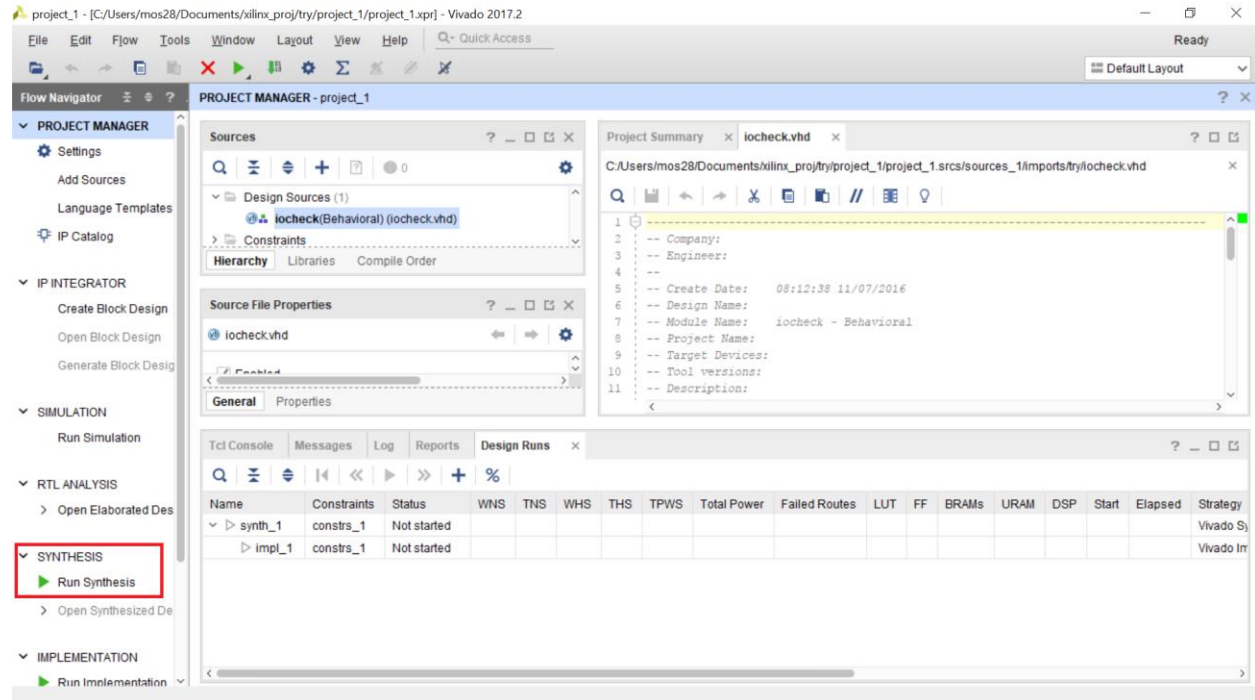
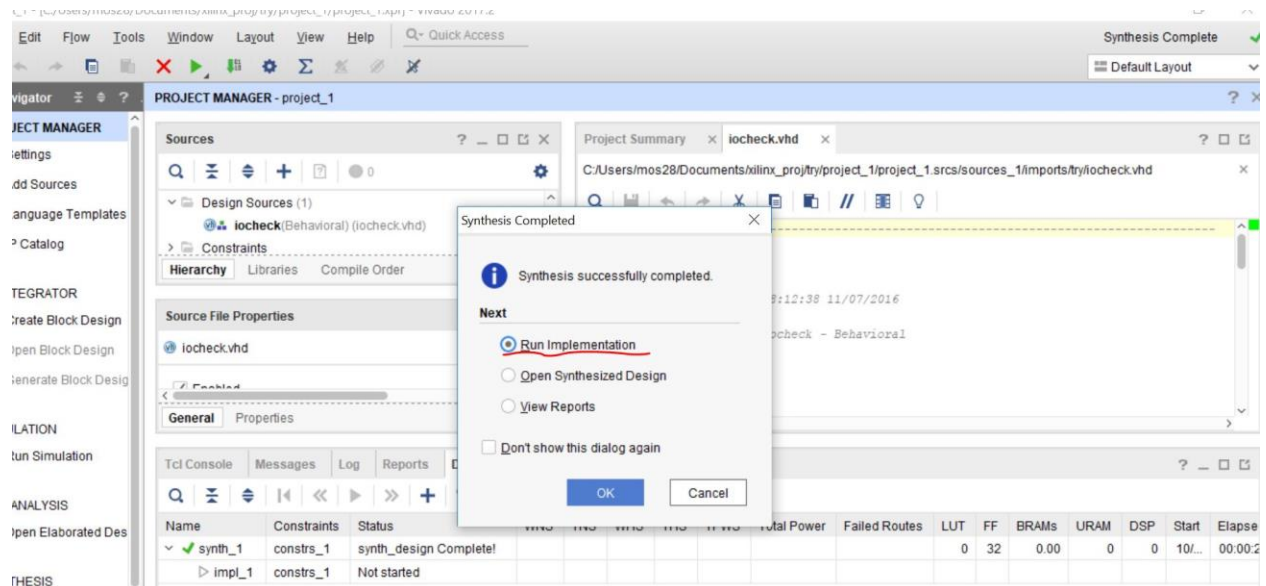


After creating RTL project and source VHDL files follow the below steps for timing simulation:

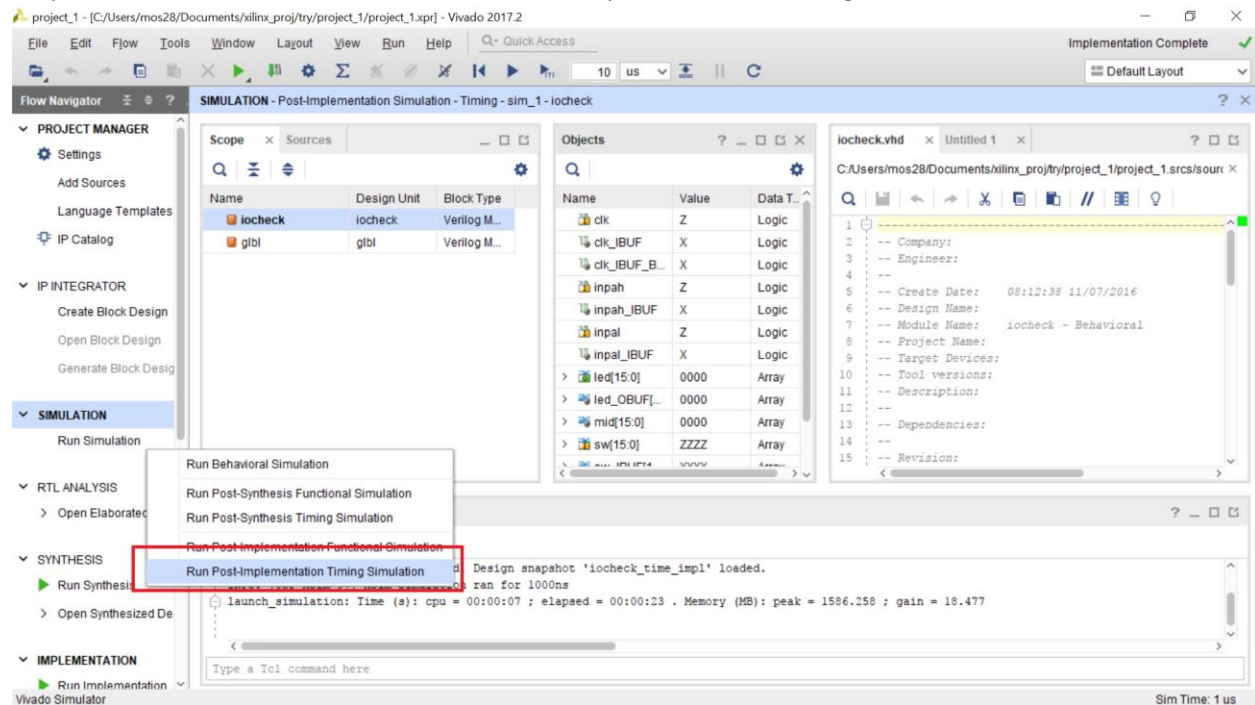
Step 1: Run synthesis:



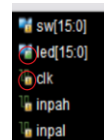
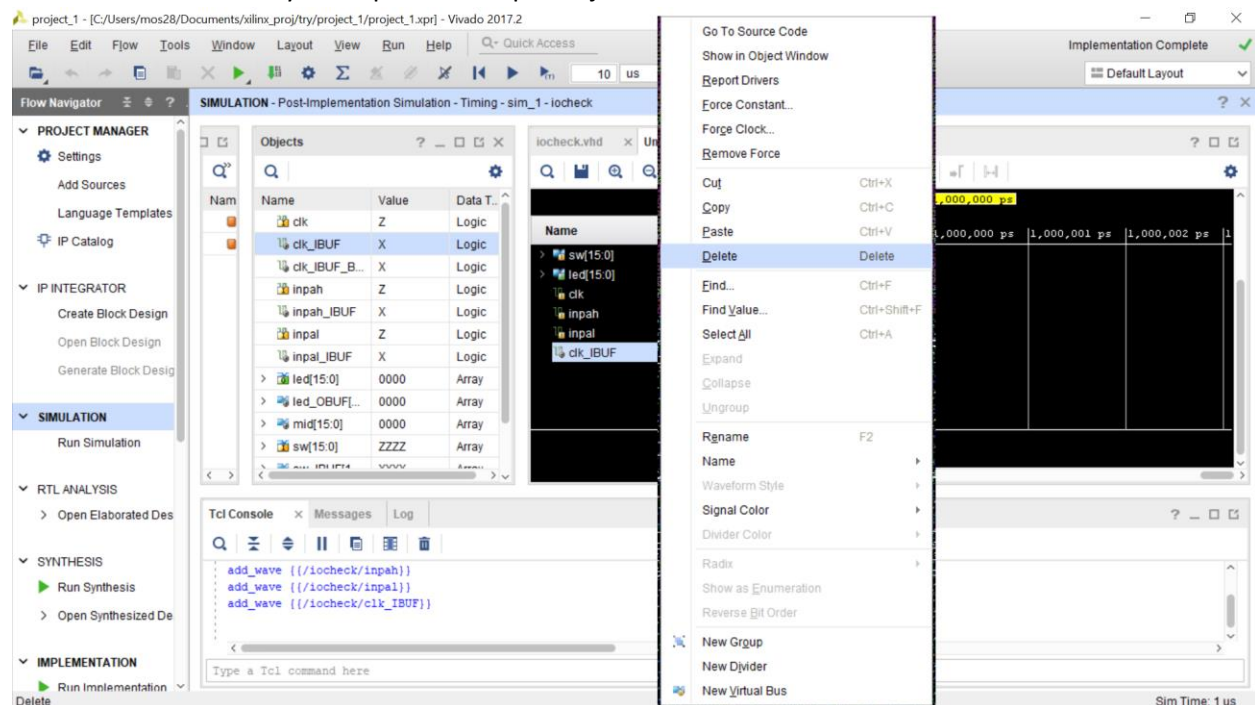
Step 2: after successful synthesis run implementation



Step 3: Click on Simulation and select Run Post-implementation Timing Simulation

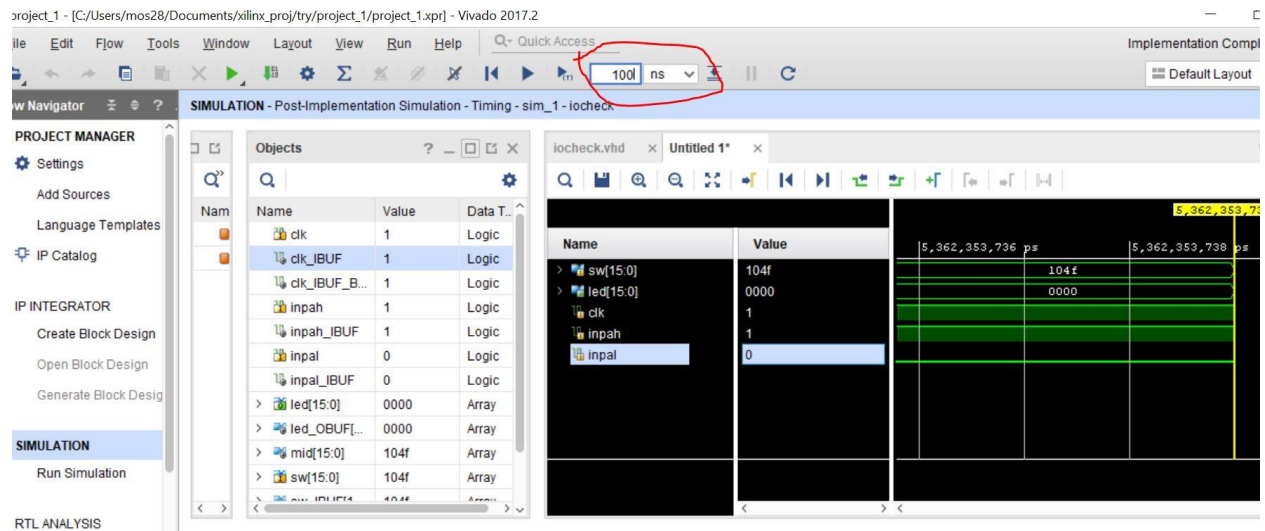


Step 4: The simulation window shows all the objects including internal signals. You select all and delete them and then add only the input and output objects.

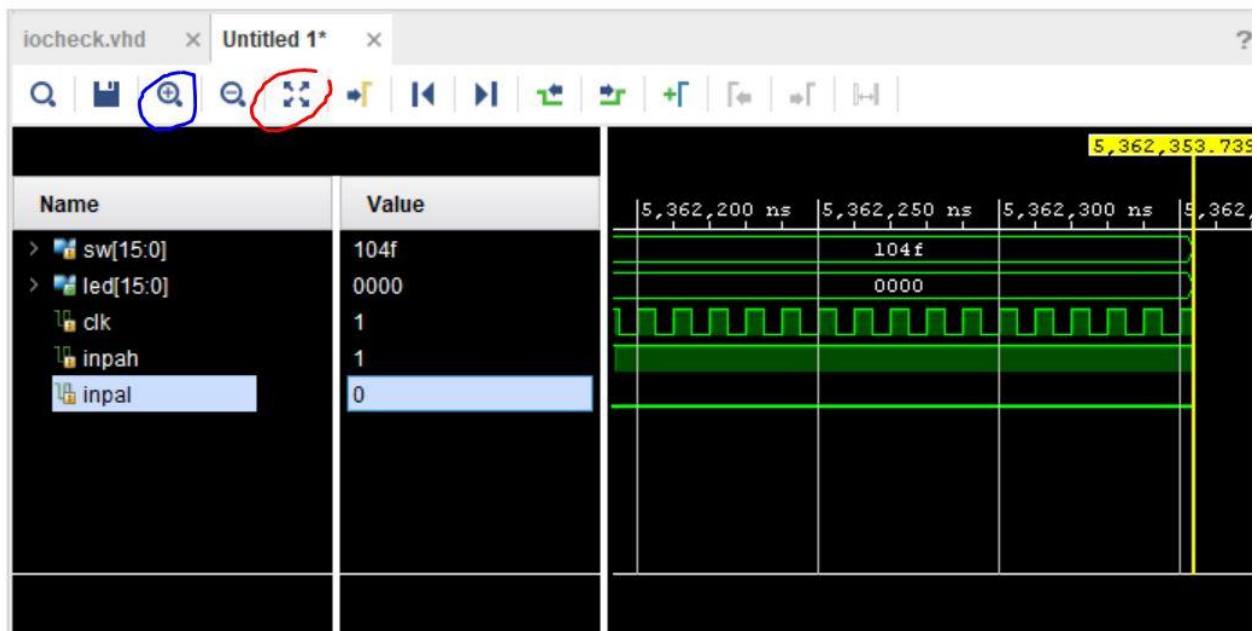


<- Input/outputs have these markings

Step 5: Force constant and clock as you did for functional simulation. Make sure you adjust the run time to as minimum as possible. The timing simulation does all delay computation hence takes time.



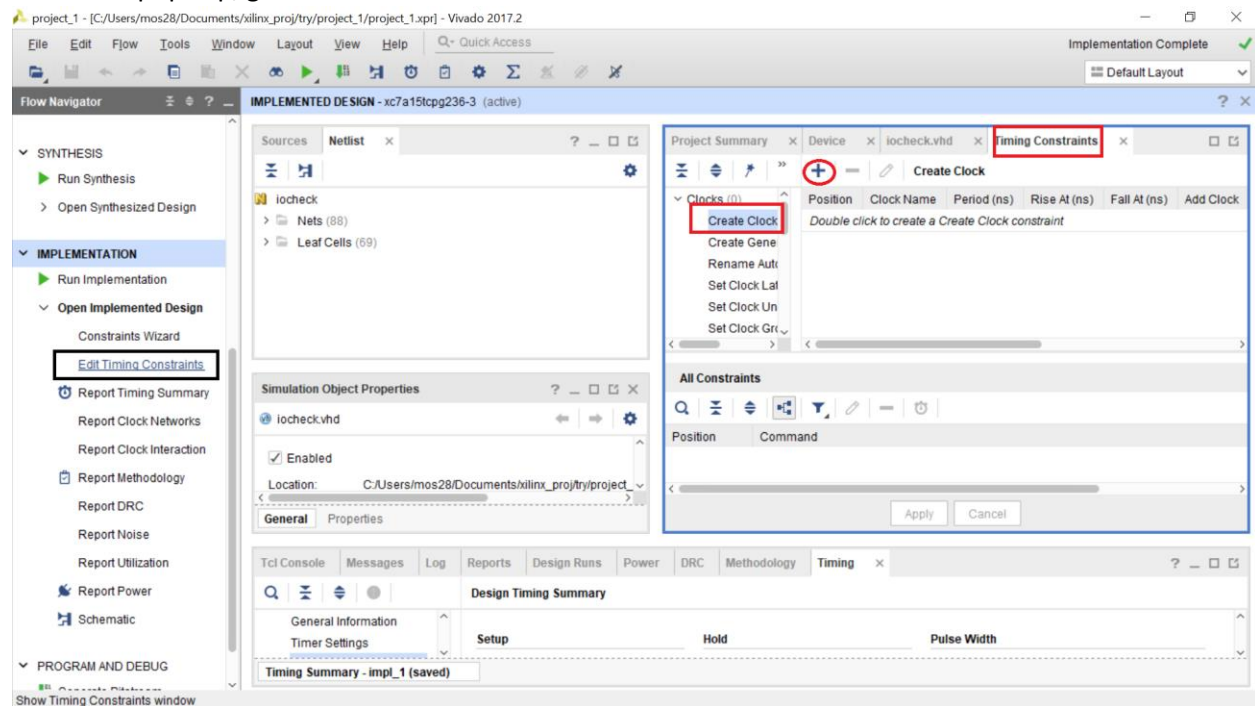
Step 6: Use the fit to screen button (in red circle) and zoom button to scroll through.



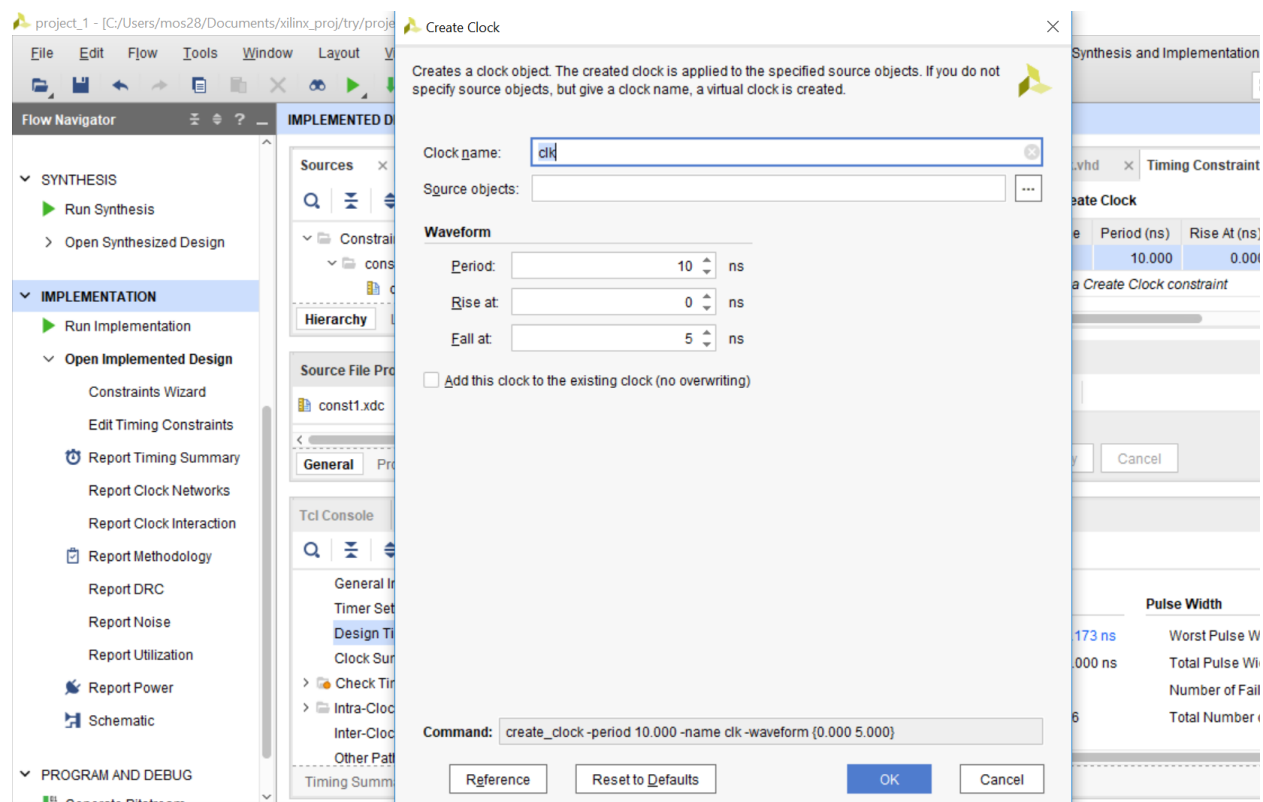
Timing Analysis, also known as static timing analysis gives worst case timing and critical path information

For timing analysis follow below steps:

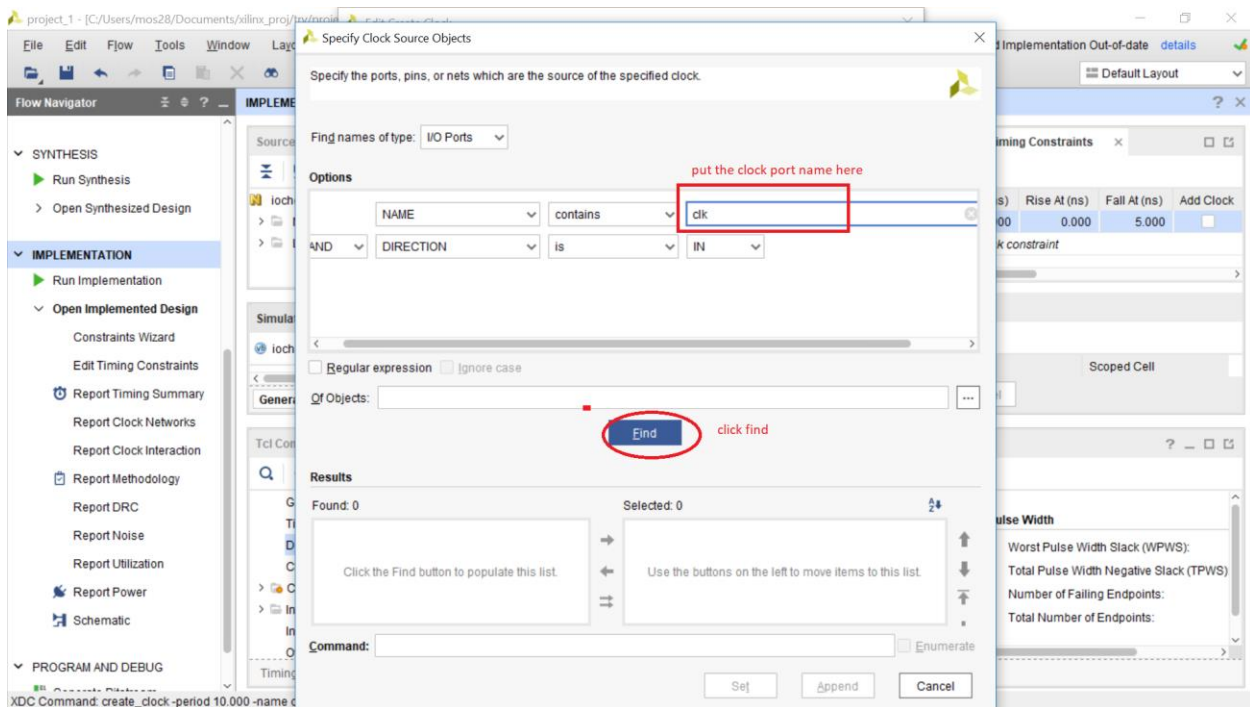
Step 1: edit timing constraints, where you give a targeted cycle time for design. Click on edit constraint. A window pops up, go to create clock tab and add a clock.



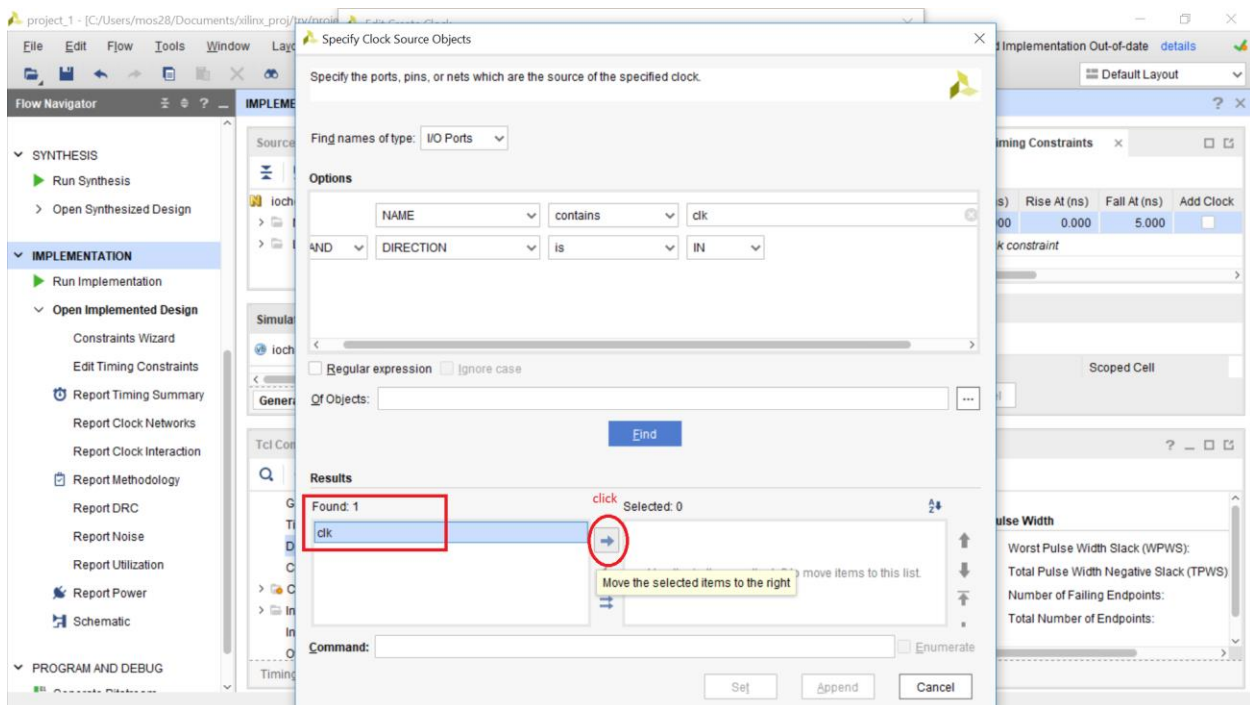
Step 2: add your clock name and time period: for example below add “clk” of period 10 ns.



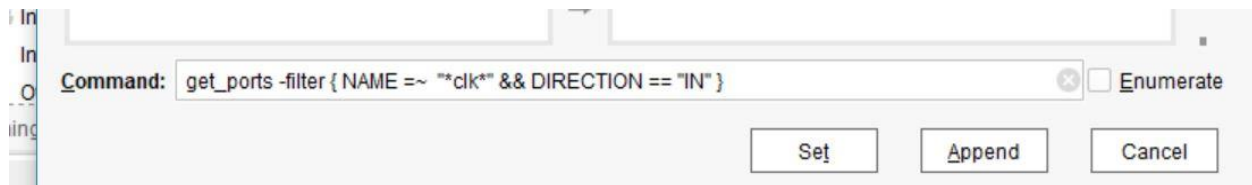
Step 3: click on source objects, a prompt like below pops up. Put your clock name and click find



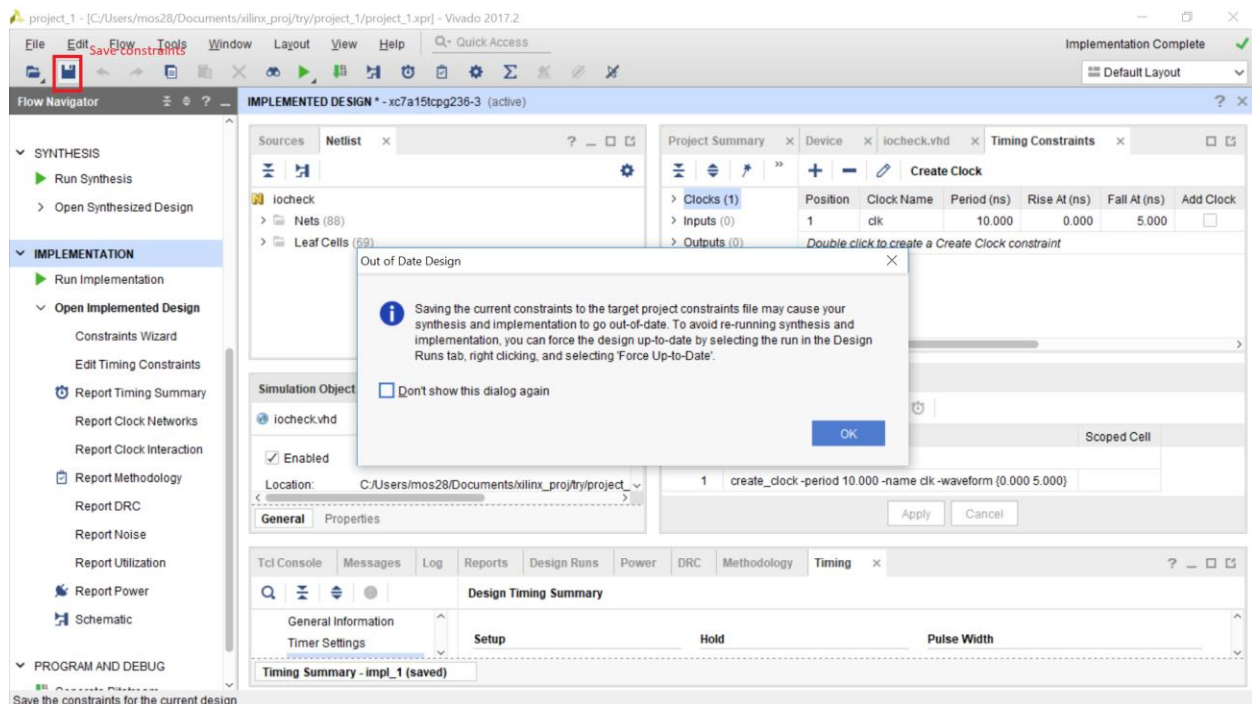
Step 4: It searches for clk name you provided among the source objects. Click on it and click on the move sign



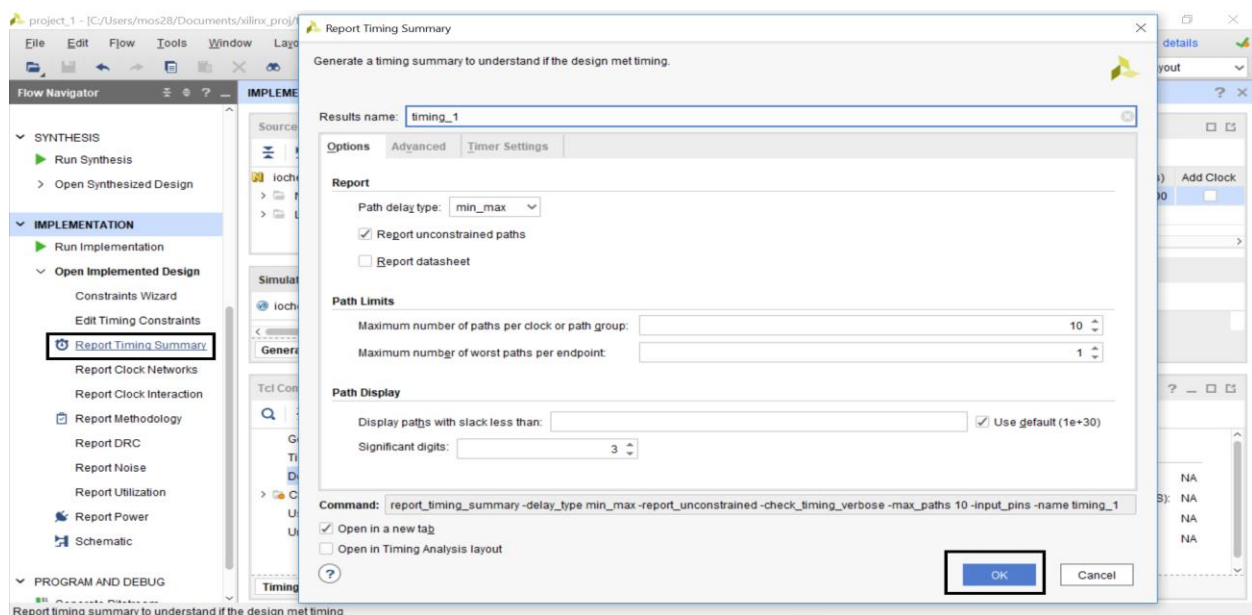
This gives a command like this, Click on “Set”



Step 5: save constraints



Step 6: You are set to run the timing reports, click on Timing Report Summary



Step 7: It shows a summary like this: with worst negative slack and number of failing paths with respect to your targeted clock speed.

The screenshot shows the Xilinx Vivado IDE interface. On the left, the 'Open Implemented Design' menu is expanded, and 'Report Timing Summary' is selected. The main window displays the 'Design Timing Summary' report in the 'Timing' tab. The report is organized into three columns: Setup, Hold, and Pulse Width. Each column contains a table of timing metrics. The 'Setup' column shows Worst Negative Slack (WNS) as 8.947 ns, Total Negative Slack (TNS) as 0.000 ns, and 0 failing endpoints. The 'Hold' column shows Worst Hold Slack (WHS) as 0.173 ns, Total Hold Slack (THS) as 0.000 ns, and 0 failing endpoints. The 'Pulse Width' column shows Worst Pulse Width Slack (WPWS) and Total Pulse Width Negative Slack (TPWS), both with 0 failing endpoints. A note at the bottom states 'All user specified timing constraints are met'.

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	8.947 ns	Worst Hold Slack (WHS):	0.173 ns	Worst Pulse Width Slack (WPWS):	
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	
Total Number of Endpoints:	16	Total Number of Endpoints:	16	Total Number of Endpoints:	

All user specified timing constraints are met

Additional Reading:

https://www.xilinx.com/support/documentation/sw_manuals/xilinx2012_2/ug938-vivado-design-analysis-closure-tutorial.pdf