Designing aapsdkaspokd

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0.1 Analog Input Stage Design

0.1.1 Input AC Coupling

The TLV320AIC series codec has a configurable input impedance of 10 kΩ, 20 kΩ, and 40 kΩ **slaa557**. To minimize loading on the source, the maximum available value of 40 kΩ is chosen.

The AC-coupling capacitor together with the input impedance of the codec ADC forms a simple RC high-pass filter, whose cutoff frequency can be calculated as

$$f_c = \frac{1}{2\pi R_{\text{eq}} C_c}$$

The resulting cutoff frequency f_c should be well below the audible range, typically under 20 Hz, to preserve bass integrity and prevent phase shifts that could degrade the perceived low-frequency response **audio˙phase˙shift**.

With a coupling capacitor of $C_c = 2.2\,\mu\text{F}$ and $R_{\text{eq}} = 40\,\text{k}\Omega$, the cutoff frequency is

$$f_c = \frac{1}{2\pi \cdot 40\,\text{k}\Omega \cdot 2.2\,\mu\text{F}} \approx 1.81\,\text{Hz}$$

0.1.2 Input Scaling

The TLV datasheet specifies a maximum input voltage on the analog pins of $0.5\,V_{\text{RMS}}$ with a common-mode voltage of 0.9 V **slaa557**. To map Eurorack audio levels into this range, the signal must be attenuated appropriately. Typical Eurorack signals reach ±5 V, i.e., $10\,\text{V}_{\text{pp}}$ **doepfer˙a110-2**.

The target ADC peak-to-peak voltage is calculated from the RMS specification:

$$V_{\text{ADC,peak}} = V_{\text{ADC,RMS}} \cdot \sqrt{2} \approx 0.707\,\text{V}$$

$$V_{\text{ADC,pp}} = 2 \cdot V_{\text{ADC,peak}} \approx 1.414\,\text{V}$$

The required attenuation factor is then

$$a = \frac{V_{\text{ADC,pp}}}{V_{\text{Eurorack}}} = \frac{1.414}{5} \approx 0.283$$

To satisfy the input impedance requirements while providing this attenuation, a **unity-gain buffer op-amp** is used before a passive resistor divider. The buffer presents an input impedance equal to the op-amp's own input impedance, which is typically greater than 200 kΩ, thereby easily meeting the desired 100 kΩ input impedance at the module. The resistor divider can then be designed to provide the necessary attenuation without significantly loading the signal source.

0.1.3 Design Rationale

The chosen signal-conditioning approach uses a unity-gain buffer followed by a passive resistor divider. This decision is based on the constraints of the system and the electrical design conclusions of other commonly used amplification circuits. An inverting amplifier topology is unsuitable because its input impedance is determined directly by the input resistor R_{in}. Since the module requires an input impedance on the order of 100 kΩ, the corresponding feedback resistor R_{f} would also need to be of similar magnitude in order to achieve the desired gain. Such large resistor values introduce significant thermal noise, as described by the Johnson noise expression

$$v_{\text{n}} = \sqrt{4kTR},$$

which grows with increasing resistance and would negatively affect the signal-to-noise ratio. Furthermore, due to space and component constraints, adding a dedicated high-impedance buffer stage in front of the inverting configuration is not feasible.

A non-inverting amplifier configuration is also unsuitable because it cannot realize an attenuation. Its closed-loop gain is defined as

$$A_{\text{v,noninv}} = 1 + \frac{R_{\text{f}}}{R_{\text{g}}},$$

and therefore satisfies

$$A_{\mathrm{v,noninv}} \geq 1,$$

which prohibits any gain smaller than unity. Since the ADC input range requires attenuation of the incoming signal, a non-inverting topology cannot be used.

For these reasons, the most practical and robust solution is to use a unity-gain buffer to ensure high input impedance and to isolate the source from the following attenuation network, and then apply a passive resistor divider to scale the signal to the required amplitude. The divider consists of $R_{\mathrm{top}} = 10\,\mathrm{k\Omega}$ and $R_{\mathrm{bot}} = 1.8\,\mathrm{k\Omega}$, resulting in a total resistance of $11.8\,\mathrm{k\Omega}$. The associated divider current is given by

$$I = \frac{V_{\mathrm{in}}}{R_{\mathrm{top}} + R_{\mathrm{bot}}}.$$

Thus, for an input voltage of 5 V the current is $I = 0.424\,\mathrm{mA}$, and for 12 V it increases to $I = 1.017\,\mathrm{mA}$. This power consumption is acceptable within the system's constraints, and the simplicity and predictability of the passive attenuation stage outweigh the modest inefficiency introduced by the resistor divider.

0.1.4 Comparison of Input Stage Circuits

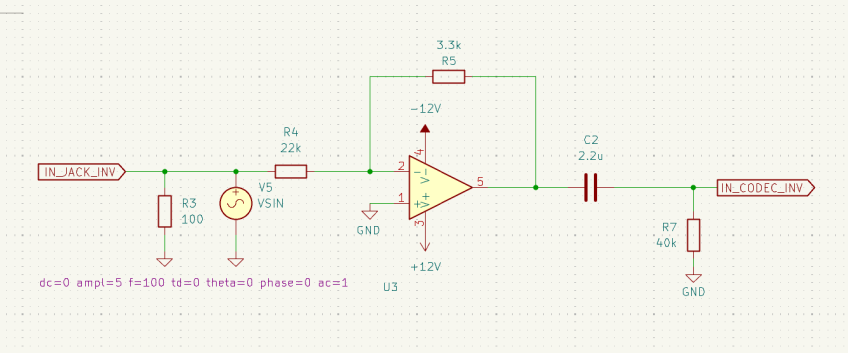
I ran SPICE simulations to compare two input stage approaches:

1. **Inverted Feedback Attenuator**
2. **Buffer to Voltage Divider**

0.2 Circuit Schematics

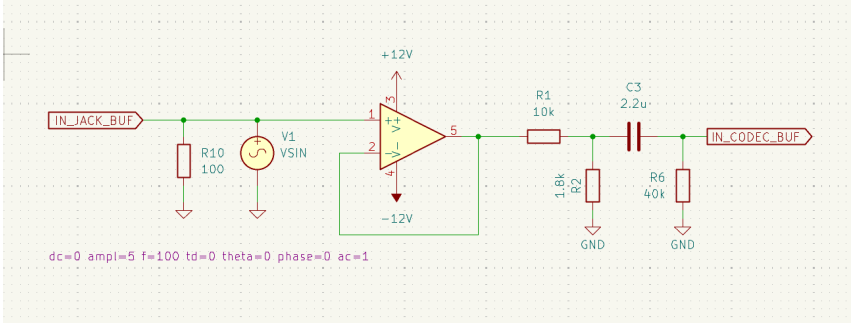
ADC input impedance is $40k\Omega$ and the signal source output impedance is 100Ω. The attenuation factor a is slightly different because of resistor values.

Inverted Feedback Attenuator

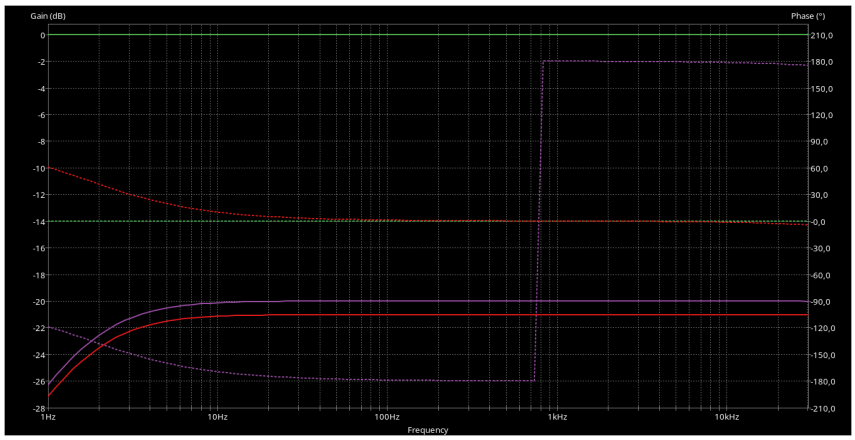


This circuit is used in most Mutable Instruments modules. It only offers $22k\Omega$ input impedance, and probably has higher thermal noise due to the resistors in the feedback path.

Buffer to Voltage Divider



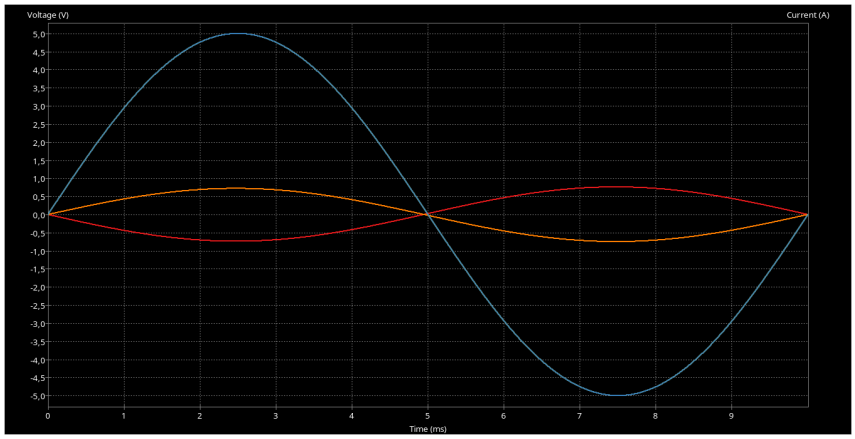
AC Analysis – Bode Plot The Bode plot shows the frequency response of both circuits in audio range ($1Hz - 30kHz$):



- **Green:** Input signal at $0dB$
- **Red:** Output of buffered circuit
- **Purple:** Output of inverted feedback circuit

Observation: Both circuits perform similarly, but the inverted feedback has a strong phase shift at 700–800Hz. The phase shift in the bass frequencies caused by the AC-coupling capacitor is below 10° at $20Hz$.

Transient Analysis – 100 Hz Signal



- **Blue:** Input signal ($10V_{pp}$, $100Hz$)
- **Red:** Output of inverted feedback circuit ($\sim 1.5V_{pp}$)
- **Orange/Red:** Output of buffered circuit ($\sim 1.47V_{pp}$)

0.2.1 ADC Absolute Input Limits:

The input pins of the ADC must remain within -0.3 V to ($A_{\text{VDD}} + 0.3$ V). Since $A_{\text{VDD}} = 1.8$ V, generated by the internal LDO of the TLV320AIC, the maximum allowed input voltage is 2.1 V.
To protect the ADC, a voltage divider with $R_1 = 1.8$ kΩ and $R_2 = 12$ kΩ is used, resulting in an attenuation factor of 0.15. For a maximum input signal of ±10 V, the attenuated voltage reaches approximately 2.11 V, which is just within the ADC limits. Such high input levels are uncommon in practice, as typical Eurorack audio signals are within ±5 V.

0.2.2 Noise Analysis

Inverted Input circuit In order to analyise the noie behaviour of an amplifier circuit, the respective noise components have to be calculated. In an inverted input op-amp circuit, the noise components contain of:

- Resistor Noise (Johnson Noise)
- op-amp voltage input noise
- op-amp current input noise

First the resistor noise aspects are analysed.
All resistors have a voltage noise given by:

$$V_{NR} = \sqrt{4kTBR}$$

where:

- T = absolute temperature in Kelvin, $T = T(^\circ\text{C}) + 273.15$
- B = bandwidth in Hz
- k = Boltzmann's constant, $k = 1.38 \times 10^{-23}$ J/K
- R = resistance in Ohms

With values in the circuit: $R_{in} = 22\text{k}\Omega$ and $R_f = 3.3\text{k}\Omega$.
This yield following Johnson's noise densities:
For R_{in}

$$V_{Rin} = 155.846\text{nV}/\sqrt{Hz}$$

and for the feedback resistor R_f

$$V_{Rf} = 60.359\text{nV}/\sqrt{Hz}$$

at $T(^\circ\text{C}) = 25^\circ\text{C}$ and a bandwith of 20kHz

0.3 Crystal

0.3.1 Calculation to Validate the Crystal Compatibility with STM32

This section follows the procedure and calculations derived from [1].

To ensure the crystal provides enough energy to excite and sustain oscillation, the following condition must be satisfied:

$$\text{Gain Margin} = \frac{g_m}{g_{m,\text{crit}}} \geq 5$$

or equivalently:

$$\text{Gain Margin} = \frac{g_{m,\text{crit max}} \cdot 5}{g_{m,\text{crit}}} \geq 5$$

where g_m is the oscillator transconductance of the product. Each STM32 device specifies g_m in the datasheet. The critical transconductance of the crystal is:

$$gm_{crit} = 4 \cdot ESR \cdot (2\pi F)^2 \cdot (C_0 + C_L)^2$$

with

$$ESR = 100\ \Omega, \quad F = 24\ \text{MHz}, \quad C_0 = 7\ \text{pF}, \quad C_L = 10\ \text{pF}$$

For the STM32H7:

$$gm_{crit\ max} = 1.5\ \text{mA/V}$$

[2, p. 107]

Calculating the critical transconductance:

$$gm_{crit} = 1.0254\ \text{mA/V}$$

and the gain margin:

$$\text{Gain Margin} = \frac{gm_{crit\ max} \cdot 5}{gm_{crit}} = \frac{1.5 \cdot 5}{1.0254} \approx 7.31$$

Since the gain margin is greater than 5, the crystal is compatible with the STM32H7.

0.3.2 Calculation of Capacitors C_{L1} and C_{L2}

Since the chosen crystal is compatible with the STM32H7 MCU, appropriate external load capacitor values have to be calculated.

The formula which describes the relation from the crystals load and shunt capacitance to the external load capacitors is:

$$C_L - C_0 = \frac{C_{L1} \cdot C_{L2}}{C_{L1} + C_{L2}}$$

Since the external load capacitors are generally the same $C_{L1} = C_{L2}$ results in:

$$C_L - C_s = \frac{C_{L1}}{2} = \frac{C_{L2}}{2}$$

which can be transformed in:

$$C_{L1} = C_{L2} = 2 \cdot (C_L - C_s)$$

The stray capacitance C_s is an estimation of the sum of the MCU pins and the parasitic capacitance of the PCB. It usually varies between $2 - 3pF$. In most STM32 datasheets a stray capacitance of $5pF$ is provided, which is a very conservative estimate though. For this calculation $C_s = 3pF$ is angenommen.

NX2520SA-24.000000MHZ-B8

With the crystal's $C_L = 10pF$ and the estimated $C_s = 3pF$, the external load capacitor's value can be calculated:

$$C_{L1} = C_{L2} = 2 \cdot (10pF - 3pF) = 14pF$$

Which yields a reasonable value, that can be purchased on the market.

`https://www.mouser.de/ProductDetail/KYOCERA-AVX/04023U140GAT2A?qs=ZwvTZoB9SO8Z%2FQAWMtnEbw%3D%3D`

References

[1] *How to select a compatible crystal and load capacitors for STM32 with layout guidelines*, https://community.st.com/t5/mcus/how-to-select-a-compatible-crystal-and-load-capacitors-for-stm32/ta-p/780236, Apr. 2025. (visited on 12/29/2025).

[2] STMicroelectronics, *Stm32h7a3ri Datasheet*.