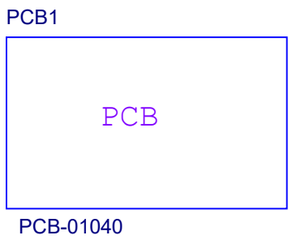
Schematics	Revision	Date	Release Information
SRT-96B-MEZ-CAM1	1.1	JUN 2020	first version release

01	Revision History
02	Block Diagram
03	Baseboard Interface
04	Camera
05	Image Coprocessor
06	Power & RST

Silk:

SRT-96B-MEZ-CAM1
SRT-PCB-01040
REV 1.1



Shiratech Solutions	Revision History		
	SRT-96B-MEZ-CAM1		
Drawn By Moshe Arad	Size A3	CAGE Code <Cage Code>	DWG NO A / Rev 1.1
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SRT-96B-MEZ-CAM1

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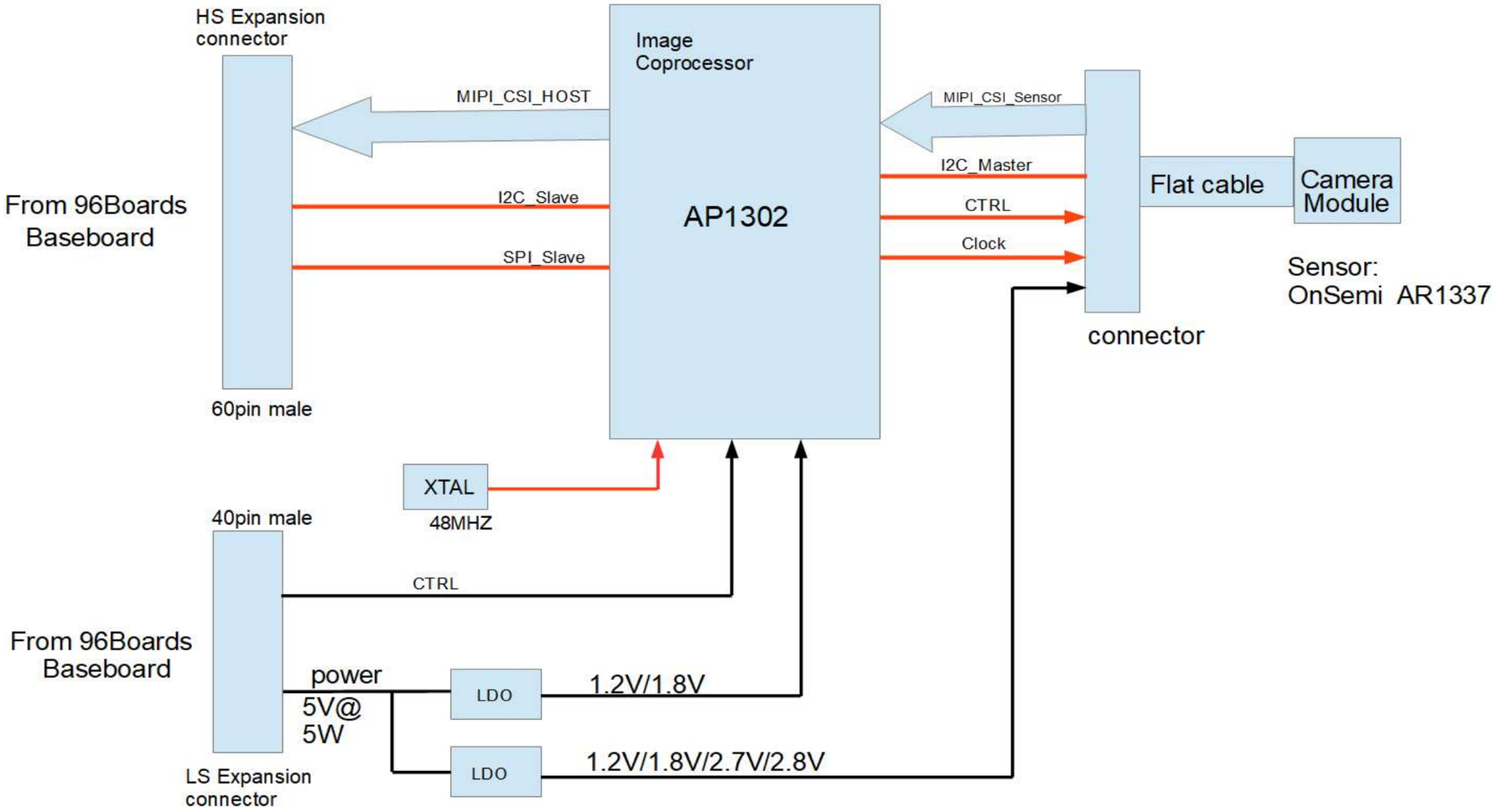

Shiratech Solutions	Block Diagram			
	SRT-96B-MEZ-CAM1			
Drawn By Moshe Arad	Size A3	CAGE Code <Cage Code>	DWG NO A	Rev 1.1
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From 96Boards Baseboard

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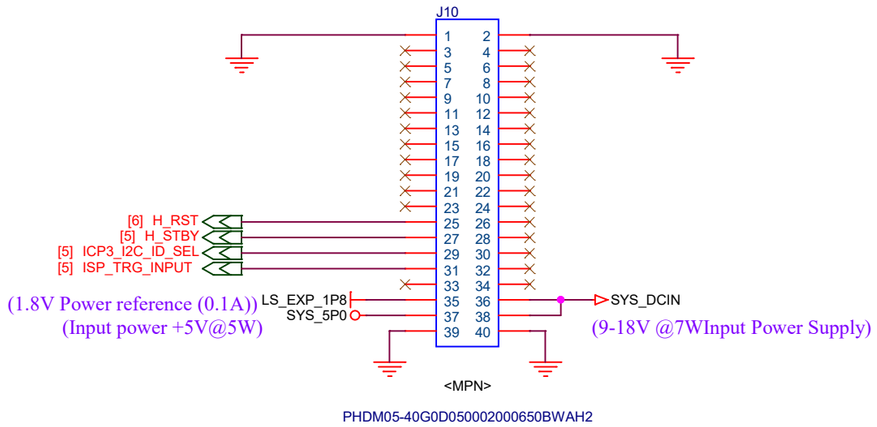
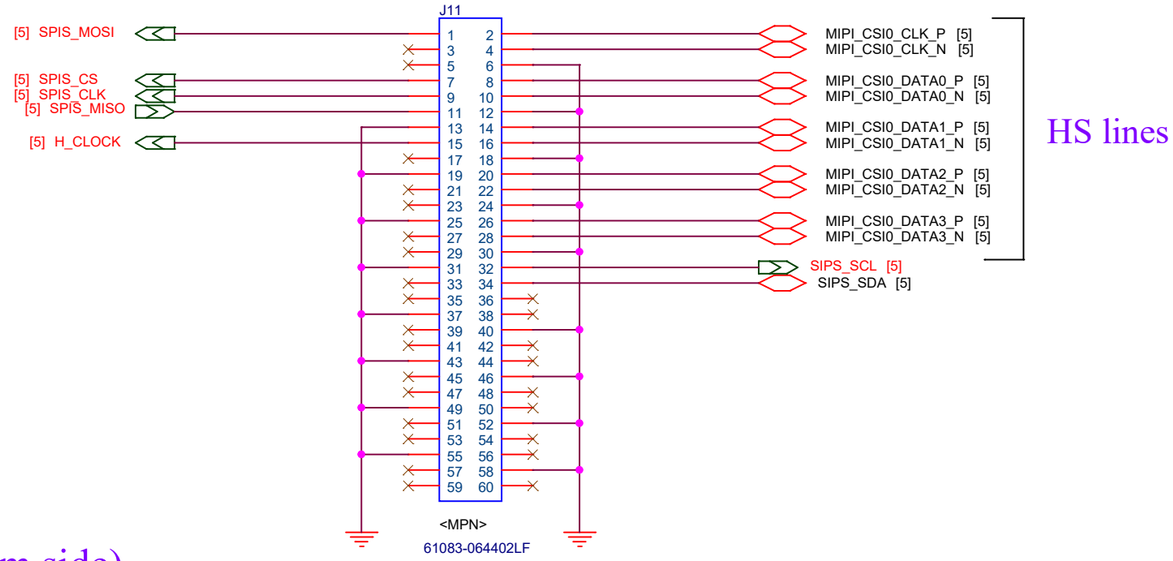
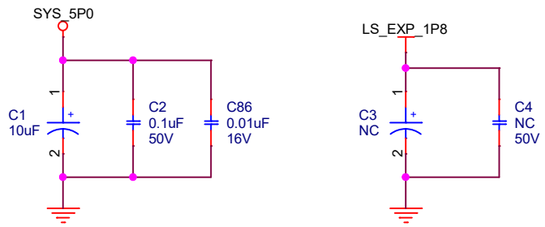
LS EXPANSION CONNECTOR



HS EXPANSION CONNECTOR



male connectors (bottom side)



Add sign "+" near "+" of: C1, C3, C28, C32, C70

Shiratech Solutions	Baseboard Interface			
	SRT-96B-MEZ-CAM1			
Drawn By Moshe Arad	Size A3	CAGE Code <Cage Code>	DWG NO A	Rev 1.1
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AR1337

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U8

COD569-B13BA-E

HS lines

[5] C_MIPI_CSI0_CLK_N
[5] C_MIPI_CSI0_CLK_P
[5] C_MIPI_CSI0_DATA3_N
[5] C_MIPI_CSI0_DATA3_P
[5] C_MIPI_CSI0_DATA1_N
[5] C_MIPI_CSI0_DATA1_P
[5] C_MIPI_CSI0_DATA0_N
[5] C_MIPI_CSI0_DATA0_P
[5] C_MIPI_CSI0_DATA2_N
[5] C_MIPI_CSI0_DATA2_P

R585 NC

J12
SMD
0.4mm Pitch
245804030000829+

R586 NC

1V8_CAMA_PWDN

1V8_FLASH
TP11

DOVDD_1V8
R584 NC
R583 NC

R70 0 SIPM_SCL [5]
R71 0 SIPM_SDA [5]
CSI0_MCLK [5]

AVDD_2V7
C60 1uF 6.3V
C61 0.1uF 50V

DOVDD_1V8
C62 1uF 6.3V
C63 0.1uF 50V

DVDD_1V2
C64 1uF 6.3V
C65 0.1uF 50V

AFVDD_2V8
C68 1uF 6.3V
C69 0.1uF 50V

StubLess resistors R584 & R583

DOVDD_1V8
R78 10k
1V8_CAMA_PWDN
R77 0 SEN_RST1 [5]
C57 0.1uF 50V

3x150mA

+1V8_FIRST
R591 NC Jumper 0402
DOVDD_1V8
R217 0 Jumper 0402
AVDD_2V7
R221 0 Jumper 0402
AFVDD_2V8
R222 0 Jumper 0402

SYS_5P0
C58 1uF 6.3V
C59 0.1uF 50V
R79 0
U9
MIC5387-GMMYMT-TR
VIN
EN2/3
GND
GND_PAD
OUT1
OUT2
OUT3
MIC5387-GMMYMT-TR

VDD_1V2
R592 0 Jumper 0402
DVDD_1V2
R223 NC Jumper 0402

SYS_5P0
C66 1uF 6.3V
C67 0.1uF 50V
U10
AP7313
IN
GND
OUT
NC
AP7313-12SAG-7

150mA

DOVDD_1V8 TP12
AVDD_2V7 TP13
AFVDD_2V8 TP14
DVDD_1V2 TP15

TP12,TP13,TP14,TP15 together
At the same place

Shiratech Solutions	Camera Interface		
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Drawn By Moshe Arad	Size A3	CAGE Code <Cage Code>	DWG NO A / Rev 1.1
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D

C

B

A

StubLess resistors:

R548 & R549 On the same pad
R555 & R556 On the same pad

R549 & R555 Stubless

U1B
AP1302CSSL00SMGA0-DR

100R Diff

100R Diff

VDDIO_1V8

R590 2.2k
R589 2.2k
R588 10k
R587 10k

[4] SIPM_SCL
[4] SIPM_SDA
[3] SIPS_SDA
[3] SIPS_SCL

R1 0 TESTMODE
[6] RST
ICP_MCLK_IN
[3] H_STBY
R3 0
R4 1K

[4] C_MIPI_CSI0_CLK_P
[4] C_MIPI_CSI0_CLK_N
[4] C_MIPI_CSI0_DATA0_P
[4] C_MIPI_CSI0_DATA0_N
[4] C_MIPI_CSI0_DATA1_P
[4] C_MIPI_CSI0_DATA1_N
[4] C_MIPI_CSI0_DATA2_P
[4] C_MIPI_CSI0_DATA2_N
[4] C_MIPI_CSI0_DATA3_P
[4] C_MIPI_CSI0_DATA3_N

B1 TESTMODE
L1 RST
M2 CLK
K1 STANDBY
A4 S0_CLK_DP
B4 S0_CLK_DN
A2 S0_D0_DP
B2 S0_D0_DN
A3 S0_D1_DP
B3 S0_D1_DN
A5 S0_D2_DP
B5 S0_D2_DN
A6 S01_D32_DP
B6 S01_D32_DN
A8 S1_D0_DP
B8 S1_D0_DN
A9 S1_D1_DP
B9 S1_D1_DN
A7 S1_CLK_DP
B7 S1_CLK_DN
B11 SIPM_SCL
C11 SIPM_SDA
D12 SIPS_SDA
C12 SIPS_SCL

H_CLK_DN M7 → MIPI_CSI0_CLK_N [3]
H_CLK_DP L7 → MIPI_CSI0_CLK_P [3]
H_D0_DN M11 → MIPI_CSI0_DATA0_N [3]
H_D0_DP L11 → MIPI_CSI0_DATA0_P [3]
H_D1_DN M10 → MIPI_CSI0_DATA1_N [3]
H_D1_DP L10 → MIPI_CSI0_DATA1_P [3]
H_D2_DN M9 → MIPI_CSI0_DATA2_N [3]
H_D2_DP L9 → MIPI_CSI0_DATA2_P [3]
H_D3_DN M8 → MIPI_CSI0_DATA3_N [3]
H_D3_DP L8 → MIPI_CSI0_DATA3_P [3]

100R Diff

GPIO[11] A11 R566 0 → ICP3_I2C_ID_SEL [3]
GPIO[10] J12 R567 0 TP1
GPIO[9] K12 R557 0 TP4
GPIO[8] L12 R558 0 → ISP_TRG_INPUT [3]
GPIO[7] B12 R559 0 TP5
GPIO[6] L4 R560 0 → SPIS_CLK [3]
GPIO[5] M4 R561 0 → SPIS_MOSI [3]
GPIO[4] M6 R562 0 → SPIS_MISO [3]
GPIO[3] M5 R563 0 → SPIS_CS [3]
GPIO[2] A10 R564 0 TP6
GPIO[1] C10 → SEN_RST1 [4]
GPIO[0] B10 → R554 22R SEN_CLK1

VDDIO_1V8
C7 0.1uF 50V
U2 ASFLMB-48.000MHZ-LC-T
R548 22R
ICP_MCLK_IN
R549 NC
[3] H_CLOCK
R555 NC
CSI0_MCLK [4]
SEN_CLK1 R556 0

VDDIO_1V8
C8 0.1uF 50V
C9 0.1uF 50V
C10 0.1uF 50V
C11 0.1uF 50V
C76 0.01uF 16V

VDD_1V2
C41 2.2uF 16V
C13 1uF 16V
C14 0.1uF 50V
C15 0.1uF 50V
C40 NC 16V
C72 0.01uF 16V

+1V8_FIRST
C12 0.1uF 50V
C38 2.2uF 16V
C73 0.01uF 16V

VDD_1V2
C19 1uF 16V
C20 0.1uF 50V
C21 0.1uF 50V
C42 2.2uF 16V
C43 NC 16V
C71 0.01uF 16V

VDD_1V2
L3 BLM18PG471SN1D
C25 1uF 16V
C26 0.1uF 50V
C27 0.1uF 50V
C35 0.01uF 16V
C36 0.01uF 16V
C37 2.2uF 16V

CORE_VDD

PLL0_VDD
L1 BLM18PG471SN1D
C44 2.2uF 16V
C16 1uF 16V
C17 0.1uF 50V
C18 0.1uF 50V
C74 0.01uF 16V

PLL1_VDD
L2 BLM18PG471SN1D
C39 2.2uF 16V
C22 1uF 16V
C23 0.1uF 50V
C24 0.1uF 50V
C75 0.01uF 16V

C9 CORE_VDD20
D1 CORE_VDD19
E1 CORE_VDD18
E10 CORE_VDD17
E11 CORE_VDD16
E12 CORE_VDD15
F1 CORE_VDD14
F12 CORE_VDD13
G1 CORE_VDD12
G12 CORE_VDD11
H1 CORE_VDD10
H12 CORE_VDD9
J1 CORE_VDD8
J2 CORE_VDD7
J3 CORE_VDD
J10 HMIPI_VDD
J11 HMIPI_VDD5
K9 HMIPI_VDD4
K10 HMIPI_VDD6
C2 SMIPI_VDD1
C3 SMIPI_VDD2
D2 SMIPI_VDD
D3 SMIPI_VDD3
C1 IOVDD
D10 IOVDD_SIPS
K2 IOVDD_HMISC
C8 IOVDD_SMISC
M3 IOVDD_GPIOH
K11 IOVDD_GPIO
L3 PLL0_VDD
K3 PLL1_VDD

D11 I2C_VSS
K4 PLL0_VSS
L2 PLL1_VSS
K6 HMIPI_VSS56
K7 HMIPI_VSS55
K8 HMIPI_VSS54
L6 HMIPI_VSS
C4 SMIPI_VSS53
C5 SMIPI_VSS52
C6 SMIPI_VSS51
C7 SMIPI_VSS
E2 VSS50
E3 VSS49
E5 VSS48
E6 VSS47
E7 VSS46
E8 VSS45
F2 VSS44
F3 VSS43
F5 VSS42
F6 VSS41
F7 VSS40
F8 VSS39
F10 VSS (VBLOW)
F11 VSS38
G2 VSS37
G3 VSS36
G5 VSS35
G6 VSS34
G7 VSS33
G8 VSS32
G10 VSS31
G11 VSS30
H2 VSS29
H3 VSS28
H5 VSS27
H6 VSS26
H7 VSS25
H8 VSS24
H10 VSS23
H11 VSS22
K5 VSS21
L5 VSS

U1A
AP1302CSSL00SMGA0-DR

Shiratech Solutions	Image Coprocessor
	SRT-96B-MEZ-CAM1
Drawn By Moshe Arad	Size A3 · CAGE Code <Cage Code> · DWG NO A · Rev 1.1
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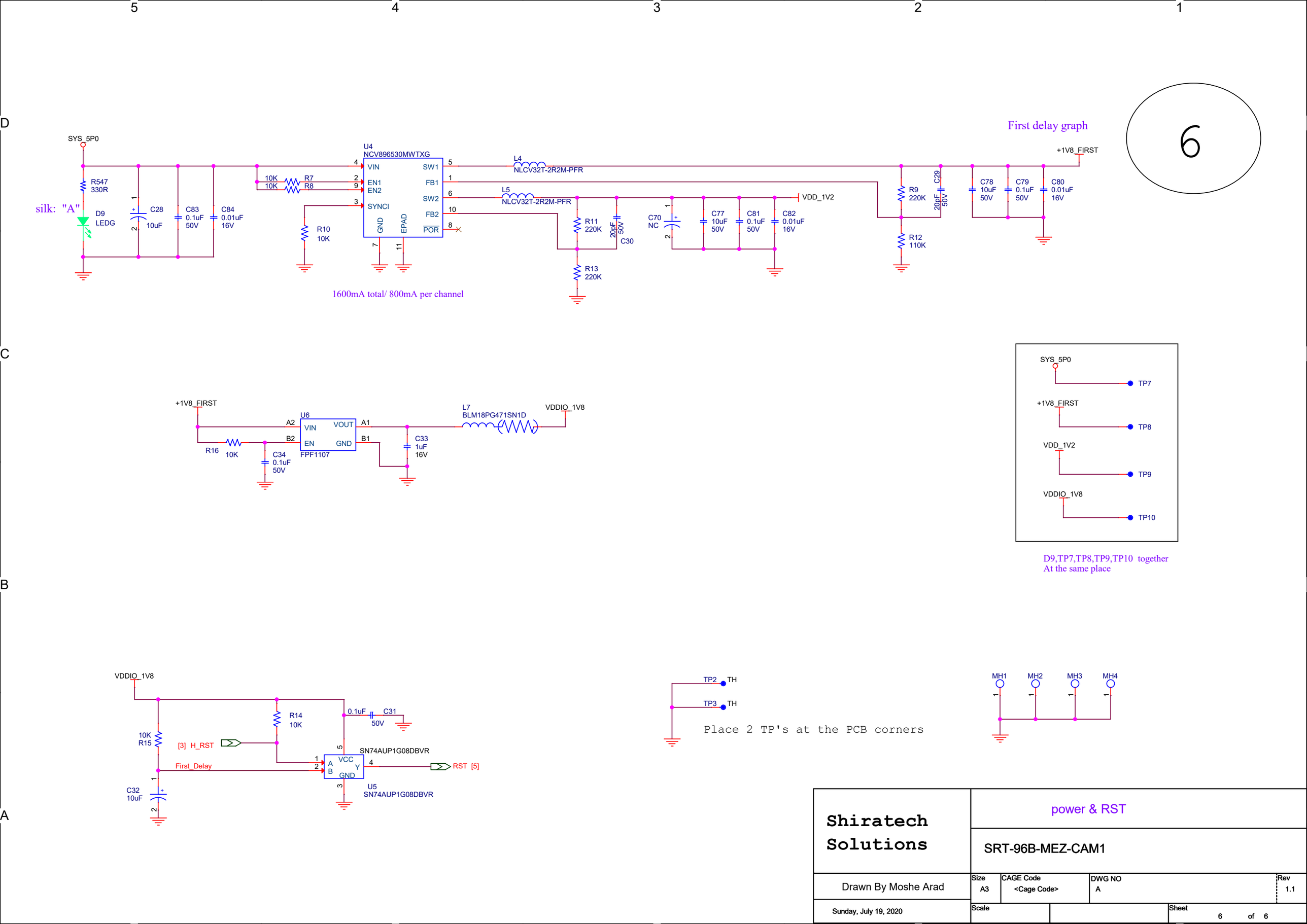

Shiratech Solutions	power & RST			
	SRT-96B-MEZ-CAM1			
Drawn By Moshe Arad	Size A3	CAGE Code <Cage Code>	DWG NO A	Rev 1.1
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