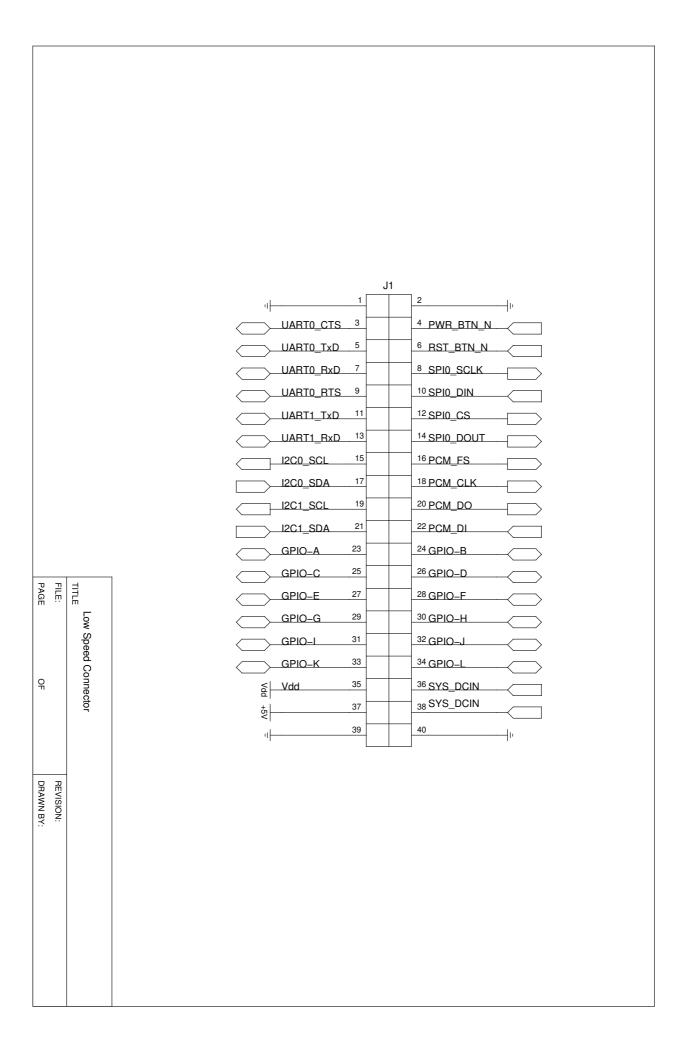
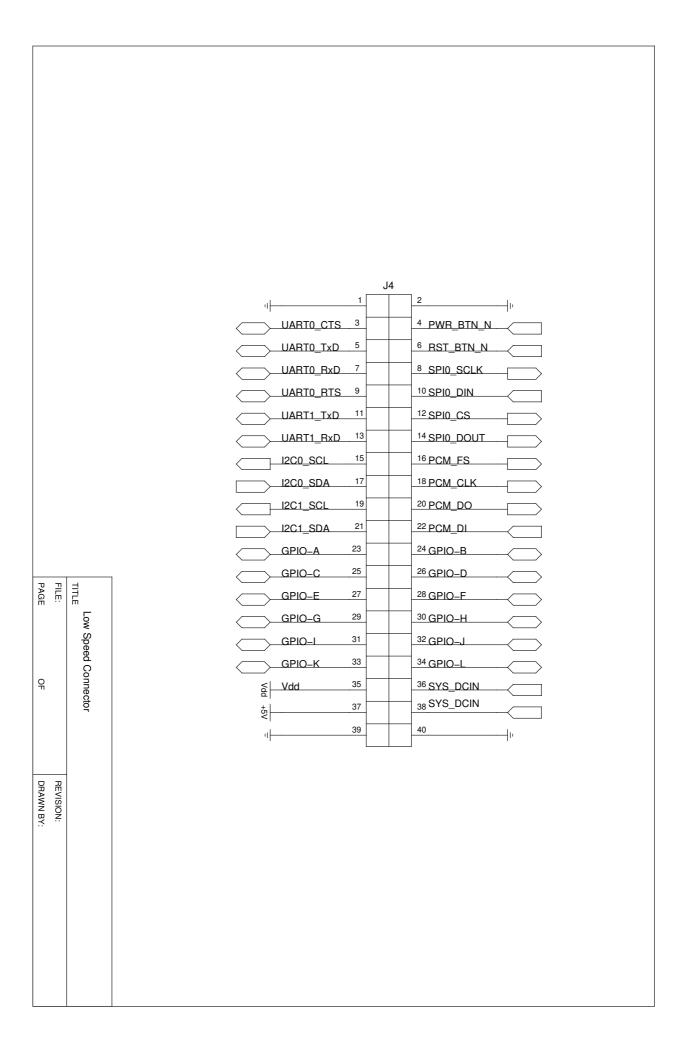
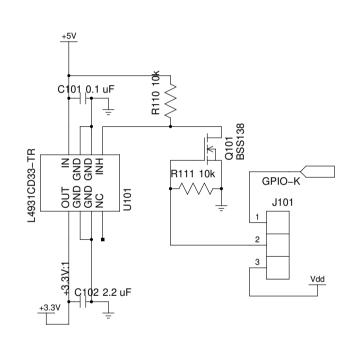
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DSI_D2=  DSI_D2+  DSI_D2+  66  DSI_D1-  DSI_D1+	CSI1_D0-    CSI1_D0+   CSI1_D0+   CSI1_D0+   CSI1_D0+   CSI1_D0+   CSI1_D0+   CSI1_D0+   CSI1_D0+   CSI1_D0+   CSI1_D0-   CSII_D0-   CSII_D0-   CSII_D0-   CSII_D0-   CSII_D0-   CSII_D0-   CSII_D0-   CSII_D0-
DSI_D0- 67  DSI_D0+ 27  DSI_CLK- 57	12C2_SCL
DSI_CLK+	CSI0_D2- CSI0_D2+ 0Z  81  CSI0_D1- 91  CSI0_D1+ 71
SD_CMD/SPI1_DIN  SD_SCLK/SPI1_SCLK  SD_DAT3/SPI1_CS  SD_DAT2  SD_DAT1  E  SD_DAT1  E  SD_DAT0/SPI1_DOUT  I	CSI0_D0- 01 CSI0_D0+ 8 9 

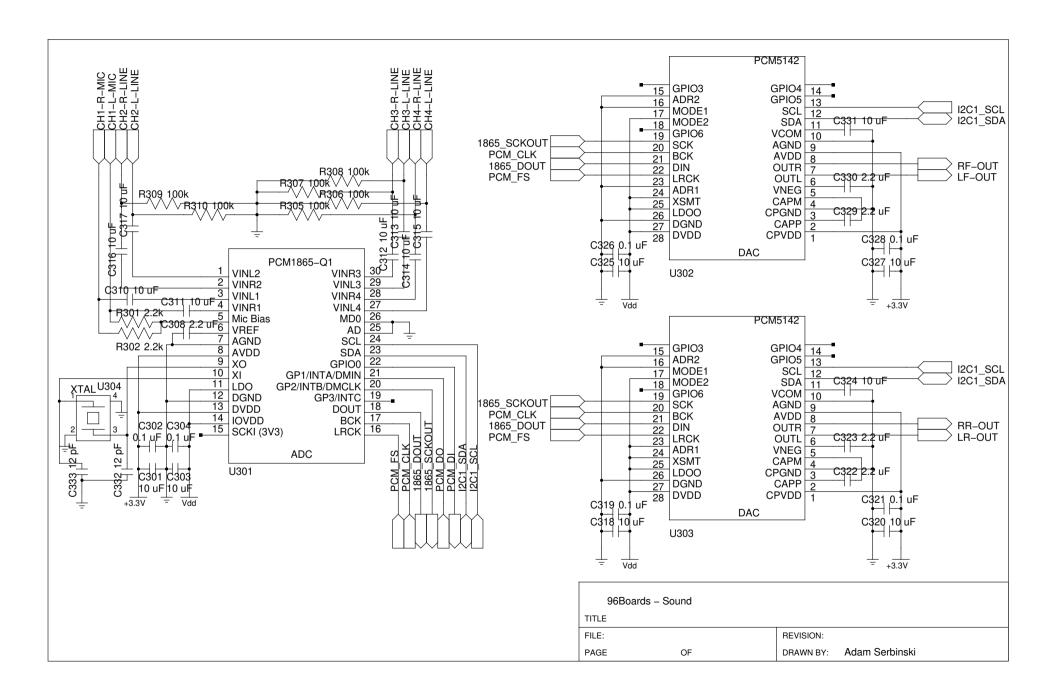
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PAGE TITLE	DSI_CLK-	11
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	SD_DAT3/SPI1_CS	CSI0_D0+
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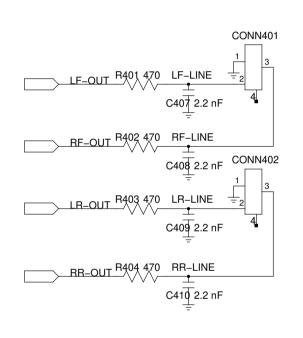


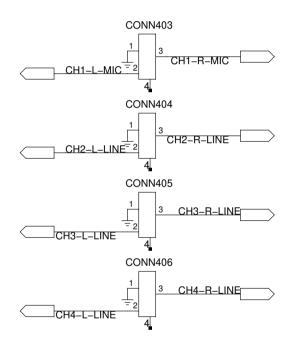




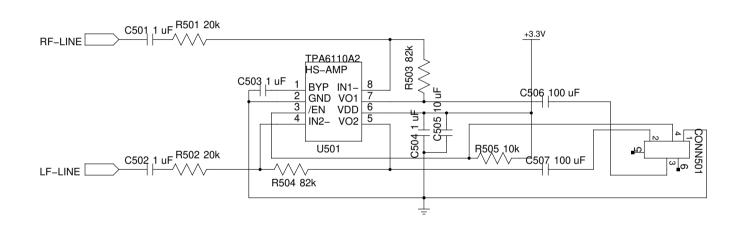
3v3 regulator		
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