03/02/2019 circuit_analysis

Using Laplace Transforms for Circuit Analysis

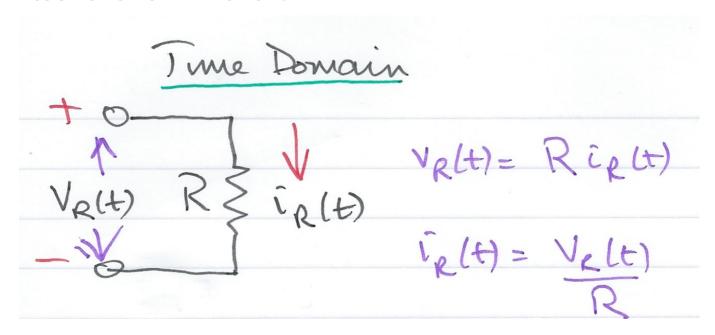
First Hour's Agenda

We look at applications of the Laplace Transform for

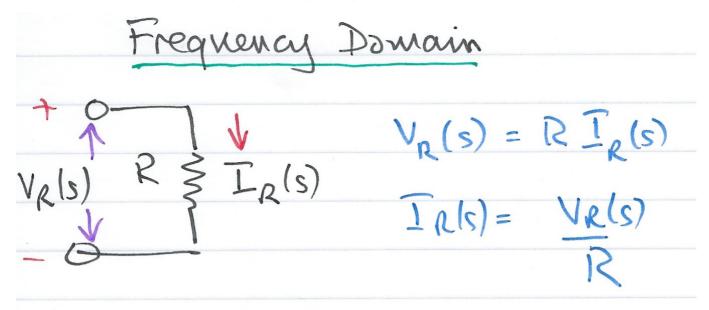
- Circuit transformation from Time to Complex Frequency
- · Complex impedance
- · Complex admittance

Circuit Transformation from Time to Complex Frequency

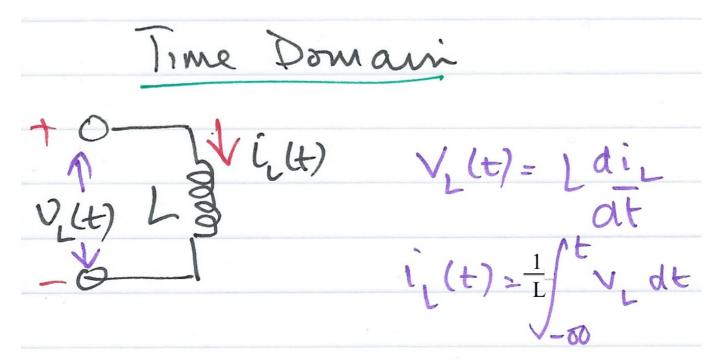
Resistive Network - Time Domain



Resistive Network - Complex Frequency Domain

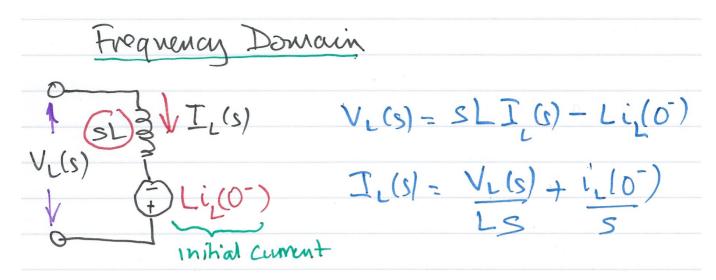


Inductive Network - Time Domain

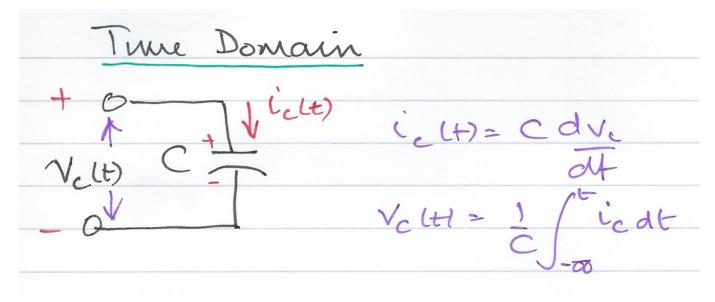


03/02/2019 circuit_analysis

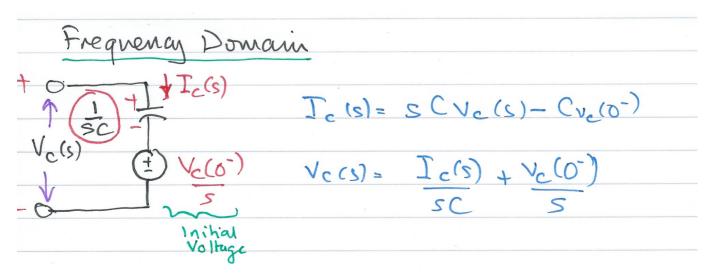
Inductive Network - Complex Frequency Domain



Capacitive Network - Time Domain



Capacitive Network - Complex Frequency Domain



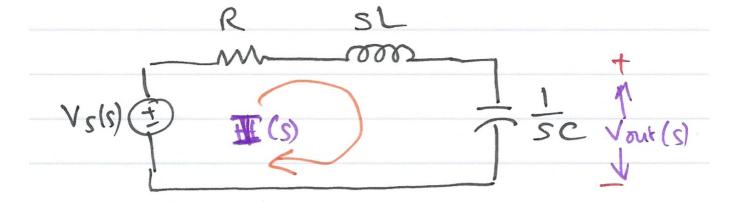
03/02/2019 circuit analysis

Examples

We will work through these in class. See worksheet6 (worksheet6).

Complex Impedance Z(s)

Consider the s-domain RLC series circuit, wehere the initial conditions are assumed to be zero.



For this circuit, the sum

$$R + sL + \frac{1}{sC}$$

represents that total opposition to current flow. Then,

$$I(s) = \frac{V_s(s)}{R + sL + 1/(sC)}$$

and defining the ratio $V_s(s)/I(s)$ as Z(s), we obtain

$$Z(s) = \frac{V_s(s)}{I(s)} = R + sL + \frac{1}{sC}$$

The s-domain current I(s) can be found from

$$I(s) = \frac{V_s(s)}{Z(s)}$$

where

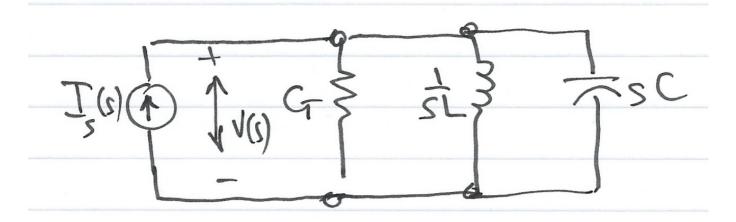
$$Z(s) = R + sL + \frac{1}{sC}.$$

Since $s = \sigma + j\omega$ is a complex number, Z(s) is also complex and is known as the *complex input impedance* of this RLC series circuit.

03/02/2019 circuit_analysis

Complex Admittance Y(s)

Consider the s-domain GLC parallel circuit shown below where the initial conditions are zero.



For this circuit

$$GV(s) + \frac{1}{sL}V(s) + sCV(s) = I_s(s)$$

$$\left(G + \frac{1}{sL} + sC\right)V(s) = I_s(s)$$

Defining the ratio $I_s(s)/V(s)$ as Y(s) we obtain

$$Y(s) = \frac{I_s(s)}{V(s)} = G + \frac{1}{sL} + sC = \frac{1}{Z(s)}$$

The s-domain voltage V(s) can be found from

$$V(s) = \frac{I_s(s)}{Y(s)}$$

where

$$Y(s) = G + \frac{1}{sL} + sC.$$

Y(s) is complex and is known as the *complex input admittance* of this GLC parallel circuit.