SAED 32/28nm Device Formation Document

SAED_EDK32/28_TK_DF

Document #: SAED_EDK32/28_TK_DF
Revision : 1.5
Technology : SAED32/28nm
Process : SAED32/28nm 1P9M 1.05V/1.8V/2.5V

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1. Introduction

This document is the part of SAED_EDK32/28 Educational Design Kit documentation. It represents all available devices in SAED32/28nm 1.05v/1.8v/2.5V Logic process and their formation. These device formation rules are free from intellectual property restrictions.

2. Device Formation

Table 1. MOSFETS

#		NMOS	PMOS
1	1.2V thin oxide standard vth nmos and pmos	n105	p105
2	1.2V thin oxide high vth nmos and pmos	n105_hvt	p105_hvt
3	1.2V thin oxide low vth nmos and pmos	n105_lvt	p105_lvt
4	1.8V thick oxide nmos and pmos	n18	p18
5	2.5V thick oxide nmos and pmos	n25	p25

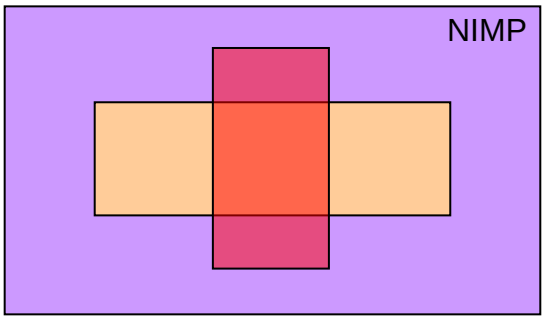

Figure 1. MOSFETS: n105

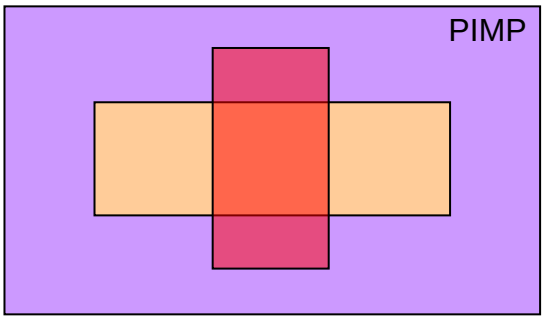

Figure 2. MOSFETS: p105

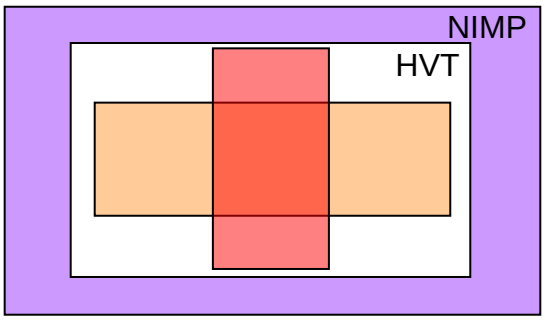

Figure 3. MOSFETS: n105_hvt

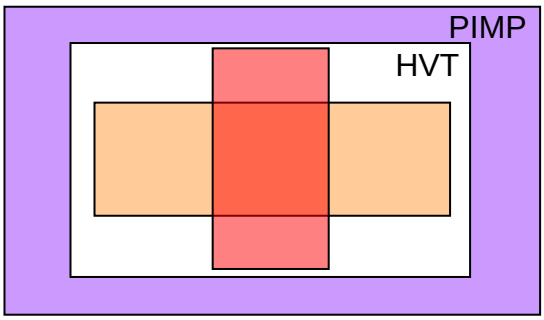

Figure 4. MOSFETS: p105_hvt

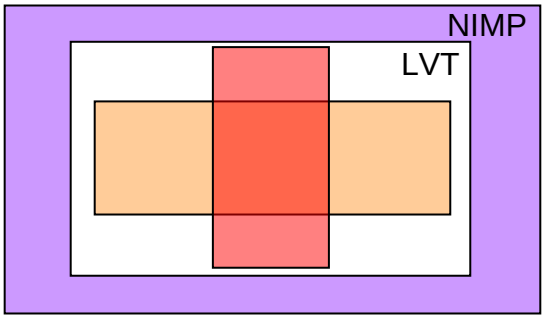

Figure 5. MOSFETS: n105_lvt

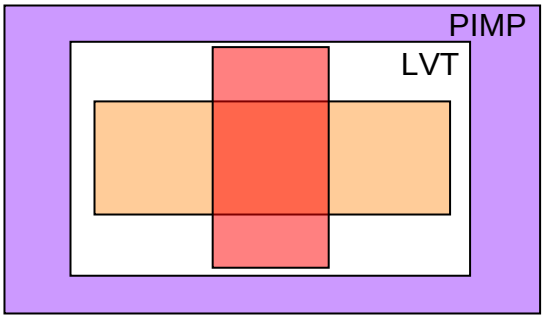

Figure 6. MOSFETS: p105_lvt

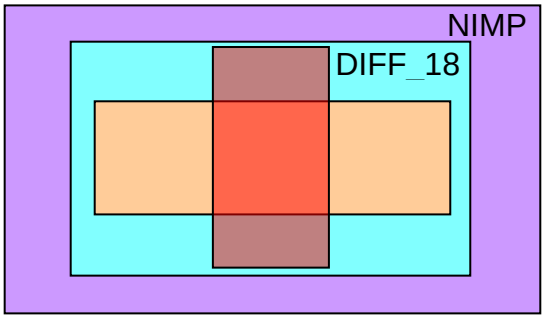

Figure 7. MOSFETS: n18

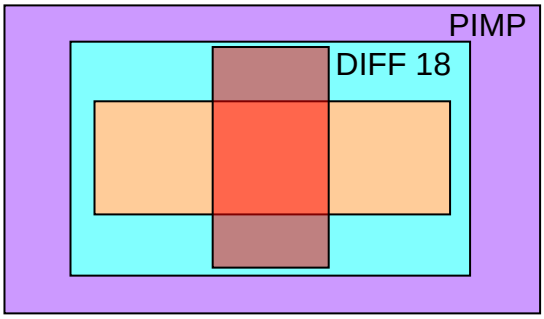

Figure 8. MOSFETS: p18

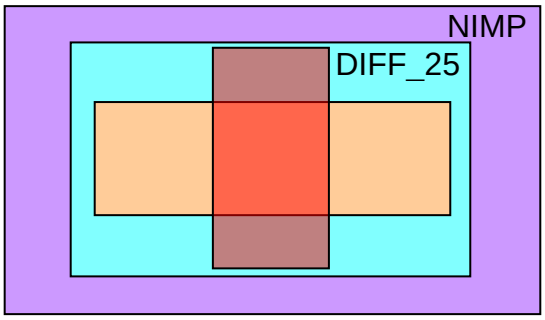

Figure 9. MOSFETS: n25

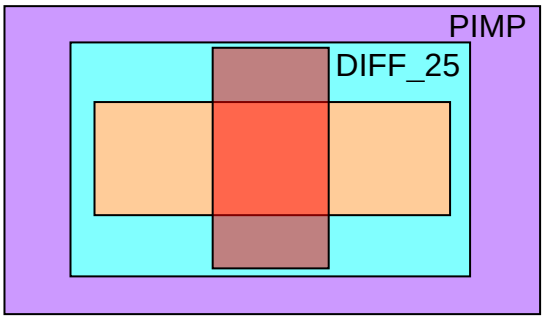

Figure 10. MOSFETS: p25

Table 2. Resistors

#	Device description	
1	Silicided N+ Poly resistor	rnpoly
2	Silicided P+ Poly resistor	rppoly
3	Unsilicided N+ Poly resistor	rnpoly_wos
4	Unsilicided P+ Poly resistor	rppoly_wos

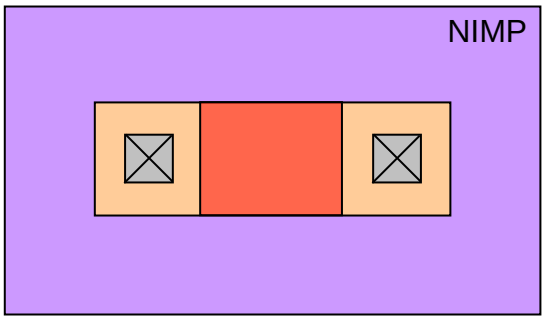

Figure 11. Resistors: rnpoly

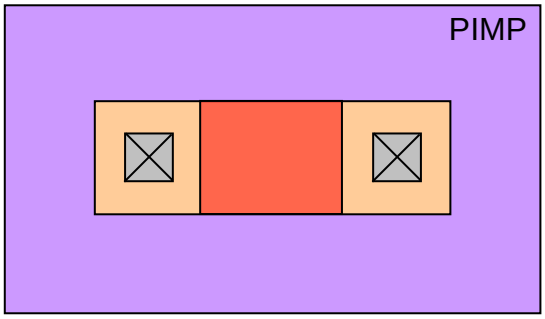

Figure 12. Resistors: rppoly

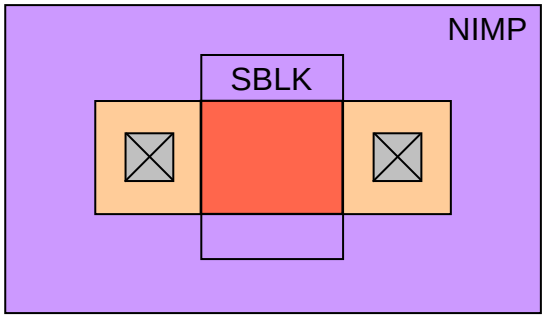

Figure 13. Resistors: rnpoly_wos

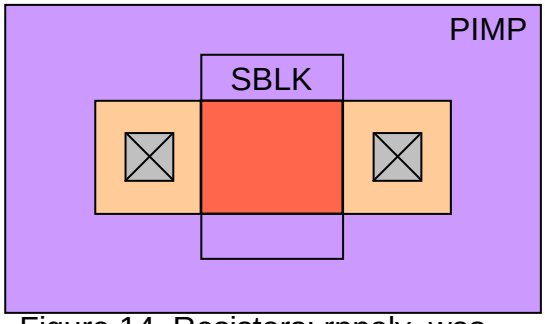

Figure 14. Resistors: rppoly_wos

Table 3. Diodes

#	Rule description	
1	N+/Psub diode	ND
1	P+/Nwell diode	PD

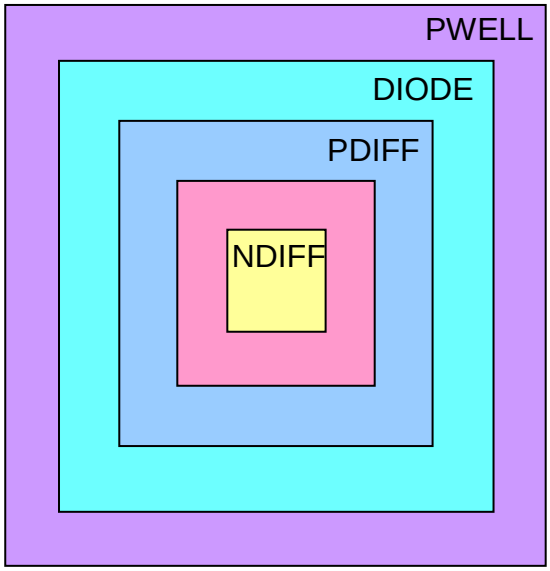

Figure 15. Diodes: ND

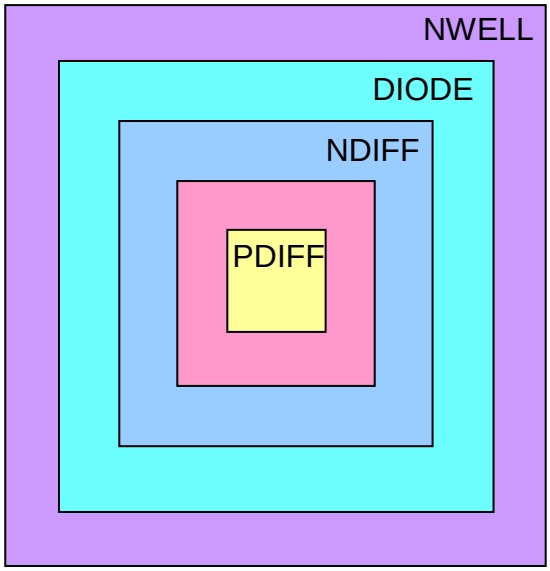

Figure 16. Diodes: PD

Table 4. Diodes

#	Rule description	
1	Metal on metal capactitor	ccap

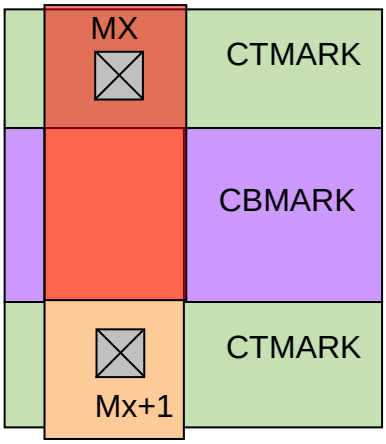

Figure 17. Capacitor: ccap, M_x/M_{x+1} (x=1..3)

4. Revision History

Table 5. Revision History

Revision	Date	Change
A.1	29/12/2010	Initial release
A.1.5	27/04/2016	Added MOM Capacitor