SAED 32/28nm Design Rules Document

SAED_EDK32/28_TK_DR

Document #: SAED_EDK32/28_TK_DR
Revision : 1.5
Technology : SAED32/28nm
Process : SAED32/28nm 1P9M 1.05V/1.8V/2.5V

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

1. Introduction

This document is the part of SAED_EDK32/28 Educational Design Kit documentation. These design rules are free from intellectual property restrictions. It was considered to develop 32/28nm rules but sizes can be larger by 1-5% than in real processes to provide further portability of projects designed by this design rules to real processes (TSMC 28nm or IBM 32/28nm).

As basis for layer names and design rules SAED 90nm process was used, which is based on MOSIS Scalable CMOS rules (SCMOS): http://www.mosis.com/Technical/Designrules/scmos/scmos-main.html. Some layers such as dummy, marking and text, have been added to the layer map. Design rule values for 32/28nm process are obtained by scaling available rules values and addition of known rules specific for 32/28nm. Also 32/28nm advanced rules supported by Synopsys IC Compiler Zroute router were added.

2. Layer Map

Layer #	Data type	Tape Out Layer	Drawing or Composite Layer	Layer name in Tech/Map File	Layer Name in DRC	Layer Name in LVS	Layer usage description
1	0	YES	Drawing	NWELL	NWELLi	NWELLi	NWELL
2	0	YES	Drawing	DNW	DNWi	DNWi	Deep NWELL
3	0	YES	Drawing	DIFF	DIFFi	DIFFi	Active area, thin oxide for device, or interconnection.
3	10	YES	Drawing	DDMY	DDMYi	DDMYi	Dummy DIFF layer; must be added if there's DIFF density rule violation.
4	0	YES	Drawing	PIMP	PIMPi	PIMPi	P+ source/drain ion implantation
5	0	YES	Drawing	NIMP	NIMPi	NIMPi	N+ source/drain ion implantation
6	0	YES	Drawing	DIFF_18	DIFF_18i	DIFF_18i	1.8v thick oxide (second gate oxide)
7	0	YES	Drawing	PAD	PADi	PADi	Pad opening
8	0	YES	Drawing	ESD	ESD	ESD	Layer for DRC and logic operation to form ESD implant. Use “ESD” to cover high voltage tolerant IO
9	0	YES	Drawing	SBLK	SBLKi	SBLKi	Resist protection oxide, non silicided area definition.
10	0	YES	Drawing	PO	POi	POi	Gate poly, poly-silicon
10	1	YES	Drawing	PODMY	PODMYi	PODMYi	Dummy PO layer, must be added if there’s PO density rule violation.
11	0	YES	Drawing	M1	M1i	M1i	Melal1
11	1	YES	Drawing	M1DMY	M1DMYi	M1DMYi	Dummy of metal1
12	0	YES	Drawing	M2	M2i	M2i	Melal2
12	1	YES	Drawing	M2DMY	M2DMYi	M2DMYi	Dummy of metal2
13	0	YES	Drawing	M3	M3i	M3i	Melal3
13	1	YES	Drawing	M3DMY	M3DMYi	M3DMYi	Dummy of metal3
14	0	YES	Drawing	M4	M4i	M4i	Melal4
14	1	YES	Drawing	M4DMY	M4DMYi	M4DMYi	Dummy of metal4
15	0	YES	Drawing	M5	M5i	M5i	Melal5
15	1	YES	Drawing	M5DMY	M5DMYi	M5DMYi	Dummy of metal5
16	0	YES	Drawing	M6	M6i	M6i	Melal6
16	1	YES	Drawing	M6DMY	M6DMYi	M6DMYi	Dummy of metal6
17	0	YES	Drawing	M7	M7i	M7i	Melal7
17	1	YES	Drawing	M7DMY	M7DMYi	M7DMYi	Dummy of metal7
18	0	YES	Drawing	M8	M8i	M8i	Melal8
18	1	YES	Drawing	M8DMY	M8DMYi	M8DMYi	Dummy of metal8
19	0	YES	Drawing	M9	M9i	M9i	Melal9
19	1	YES	Drawing	M9DMY	M9DMYi	M9DMYi	Dummy of metal9
20	0	YES	Drawing	CO	COi	COi	Contact
21	0	YES	Drawing	VIA1	VIA1i	VIA1i	Via12
22	0	YES	Drawing	VIA2	VIA2i	VIA2i	Via23
23	0	YES	Drawing	VIA3	VIA3i	VIA3i	Via34
24	0	YES	Drawing	VIA4	VIA4i	VIA4i	Via45
25	0	YES	Drawing	VIA5	VIA5i	VIA5i	Via56
26	0	YES	Drawing	VIA6	VIA6i	VIA6i	Via67
27	0	YES	Drawing	VIA7	VIA7i	VIA7i	Via78
28	0	YES	Drawing	VIA8	VIA8i	VIA8i	Via89
29	0	YES	Drawing	HVTIMP	HVTIMPi	HVTIMPi	Implant layer for hvt nmos/pmos drawing
30	0	YES	Drawing	LVTIMP	LVTIMPi	LVTIMPi	Implant layer for lvt nmos/pmos drawing
31	0	NO	Drawing	M1PIN	M1PIN	M1PIN	Metal1 text layer
32	0	NO	Drawing	M2PIN	M2PIN	M2PIN	Metal2 text layer
33	0	NO	Drawing	M3PIN	M3PIN	M3PIN	Metal3 text layer
34	0	NO	Drawing	M4PIN	M4PIN	M4PIN	Metal4 text layer
35	0	NO	Drawing	M5PIN	M5PIN	M5PIN	Metal5 text layer
36	0	NO	Drawing	M6PIN	M6PIN	M6PIN	Metal6 text layer
37	0	NO	Drawing	M7PIN	M7PIN	M7PIN	Metal7 text layer
38	0	NO	Drawing	M8PIN	M8PIN	M8PIN	Metal8 text layer
39	0	NO	Drawing	M9PIN	M9PIN	M9PIN	Metal9 text layer
40	0	NO	N/A				Reserved layer.
41	0	YES	Drawing	MRDL	MRDL	MRDL	Redistributional Layer
42	0	YES	Drawing	VIARDL	VIARDL	VIARDL	M9 to MRDL VIA

Layer #	Data type	Tape Out Layer	Drawing or Composite Layer	Layer name in Tech/Map File	Layer Name in DRC	Layer Name in LVS	Layer usage description
43	0	NO	Drawing	MRPIN	MRPIN	MRPIN	MRDL text layer
44	0	NO	Drawing	HOTNWL	HOTNWLi	HOTNWLi	Hot NWELL marking layer for DRC. Use “HOTNWL” to cover hot-NWEL width.
45	0	NO	N/A				Reserved layer.
46	0	NO	Drawing	DIOD	DIODi	DIODi	Diode marking layer for LVS. Cover P+DIFF for P+/NWELL diode, N+DIFF for N+/PWELL diode, and NWELL for NWELL/PWELL diode.
47	0	NO	Drawing	BJTMARK	BJTMARKi	BJTMARKi	BJT marking layer to cover BJT device for analog layout rules.
48	0	NO	Drawing	RNW	RNWi	RNWi	NWELL resistor marking layer for DRC and LVS.
49	0	NO	Drawing	RMARK	RMAR i	RMARKi	Resistor marking layer for LVS. The cutting edge of RPOLY over PO/DIFF determines W/L of resistors.
50	0	NO	Drawing	prBoundary			prBoundary – P&R cell boundary
51	0	NO	Drawing	LOGO	LOGO		DRC dummy layer for product label and logo
52	0	NO	Drawing	IP	IP		IP tagging text layer
53	0	NO	Drawing	RM1	RM1i	RM1i	Metal1 resistor marking layer for LVS. The cutting edge of RM1 over metals determines W/L of metal resistors.
54	0	NO	Drawing	RM2	RM2i	RM2i	Metal2 resistor marking layer for LVS. The cutting edge of RM2 over metals determines W/L of metal resistors.
55	0	NO	Drawing	RM3	RM3i	RM3i	Metal3 resistor marking layer for LVS. The cutting edge of RM3 over metals determines W/L of metal resistors.
56	0	NO	Drawing	RM4	RM4i	RM4i	Metal4 resistor marking layer for LVS. The cutting edge of RM4 over metals determines W/L of metal resistors.
57	0	NO	Drawing	RM5	RM5i	RM5i	Metal5 resistor marking layer for LVS. The cutting edge of RM5 over metals determines W/L of metal resistors.
58	0	NO	Drawing	RM6	RM6i	RM6i	Metal6 resistor marking layer for LVS. The cutting edge of RM6 over metals determines W/L of metal resistors.
59	0	NO	Drawing	RM7	RM7i	RM7i	Metal7 resistor marking layer for LVS. The cutting edge of RM7 over metals determines W/L of metal resistors.
60	0	NO	Drawing	RM8	RM8i	RM8i	Metal8 resistor marking layer for LVS. The cutting edge of RM8 over metals determines W/L of metal resistors.
61	0	NO	Drawing	RM9	RM9i	RM9i	Metal9 resistor marking layer for LVS. The cutting edge of RM9 over metals determines W/L of metal resistors.
62	0	NO	N/A				Reserved layer.
63	0	NO	N/A				Reserved layer.
64	0	NO	Drawing	DM1EXCL	DM1EXCLi	-	Dummy layer to avoid dummy metal1 insertion, used in dummy metal insertion utility.

Layer #	Data type	Tape Out Layer	Drawing or Composite Layer	Layer name in Tech/Map File	Layer Name in DRC	Layer Name in LVS	Layer usage description
65	0	NO	Drawing	DM2EXCL	DM2EXCLi	-	Dummy layer to avoid dummy metal2 insertion, used in dummy metal insertion utility.
66	0	NO	Drawing	DM3EXCL	DM3EXCLi	-	Dummy layer to avoid dummy metal3 insertion, used in dummy metal insertion utility.
67	0	NO	Drawing	DM4EXCL	DM4EXCLi	-	Dummy layer to avoid dummy metal4 insertion, used in dummy metal insertion utility.
68	0	NO	Drawing	DM5EXCL	DM5EXCLi	-	Dummy layer to avoid dummy metal5 insertion, used in dummy metal insertion utility.
69	0	NO	Drawing	DM6EXCL	DM6EXCLi	-	Dummy layer to avoid dummy metal6 insertion, used in dummy metal insertion utility.
70	0	NO	Drawing	DM7EXCL	DM7EXCLi	-	Dummy layer to avoid dummy metal7 insertion, used in dummy metal insertion utility.
71	0	NO	Drawing	DM8EXCL	DM8EXCLi	-	Dummy layer to avoid dummy metal8 insertion, used in dummy metal insertion utility.
72	0	NO	Drawing	DM9EXCL	DM9EXCLi	-	Dummy layer to avoid dummy metal9 insertion, used in dummy metal insertion utility.
73	0	NO	Drawing	DIFFEXCL	DIFF_FM	-	Marking layer to avoid metal fill in metal fill deck
74	0	NO	Drawing	POEXCL	PO_FM	-	Marking layer to avoid OD fill in OD fill deck
75	0	NO	Drawing	DIFF_25	DIFF_25	-	Marking layer for 2.5V MOS
76	0	NO	Drawing	CBMARK	CBMARKi	-	Marking layer for MOM Capacitor body
77	0	NO	Drawing	CTMARK	CTMARKi	-	Marking layer for MOM Capacitor terminals
78	0	NO	Drawing	METDMY	METDMYi	-	Marking layer for MOM Capacitor dummy metals

3. Design Rules

3.1. Definitions

Definitions of basic layout rules terminology Is given in Table 1, and figures 1-6 below.

Table 1. Design Rules Terminology

Rule #	Mark	Rule description
Enclosure	a	distance between inside of the edge of 1st layer and outside of the edge of 2nd layer
Space	b	distance between outside of the edge of 1st layer and outside of the edge of 2nd layer
Overlap	c	distance between inside of the edge of 1st layer and inside of the edge of 2nd layer
Width	d	distance between inside parts of the same layer
Extension	e	distance between inside of the edge of 1st layer and outside of the edge of 2nd layer
Area	h*i	production of objects width and height
Enclosed area	f*g	production of width and height of layer opening
Parallel run length	j (j1)	distance of cross-projection of two outside edges parallel to each other (running in parallel)
Span	k(k1)	the dimension that is perpendicular to the layer's edge used to calculate parallel length to its neighboring metal shapes

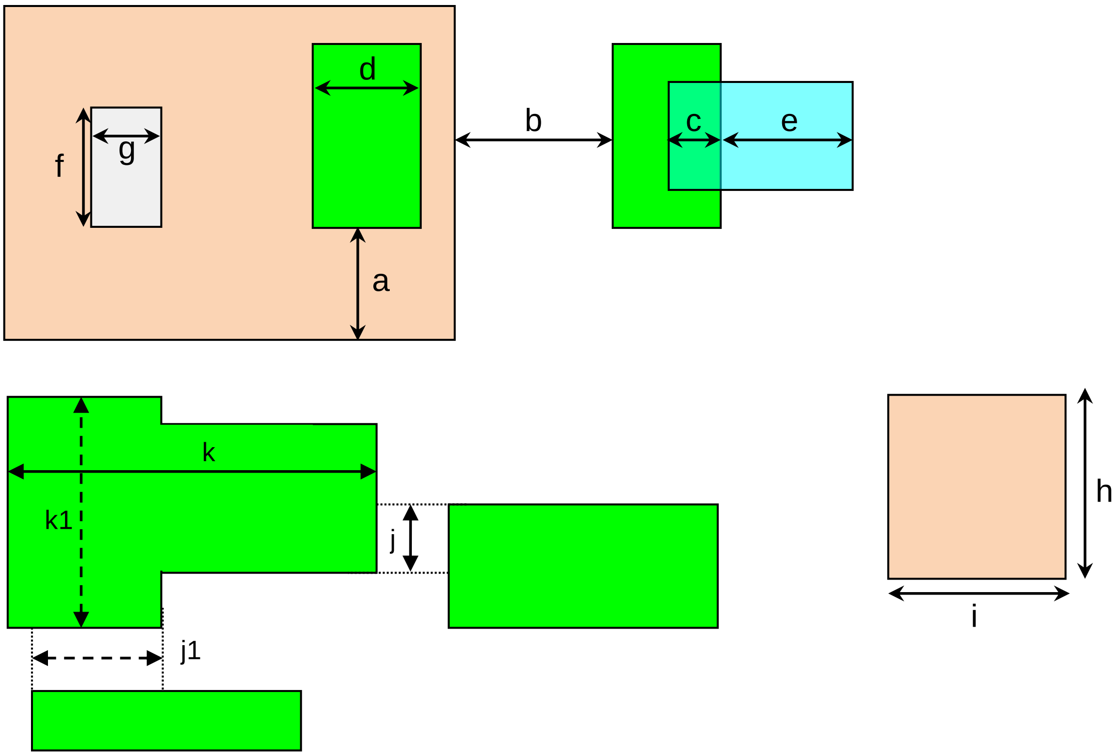
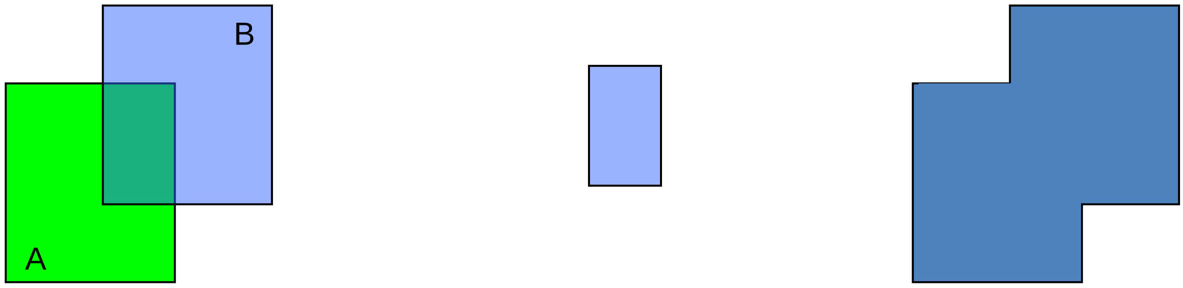


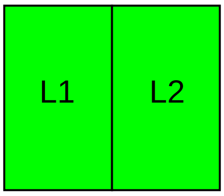
Figure 1. Definitions of layout geometrical terminology

In the definition of design rules layer Boolean operations (AND, OR, etc.) and their relationships is mentioned. The definitions of those are given below.



A AND B A OR B

Figure 2. AND and OR operations



L1 and L2 are butting each other

Figure 3. Butting

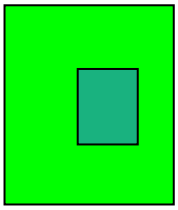


Figure 4. INSIDE

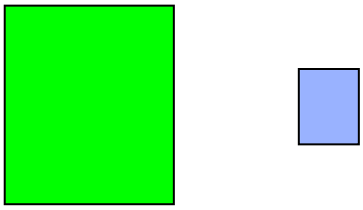


Figure 5. OUTSIDE

Some layers mentioned in the design rules are not process layers but are derived from process layers by Boolean operations. The used derived layers are:

IMP = PIMP or NIMP
NDIFF = DIFF and NIMP
PDIFF = DIFF and PIMP
N+Active = NDIFF and PWELL
P+Active = PDIFF and NWELL
ACTIVE = P+Active or N+Active
PTAP = PDIFF and PWELL
NTAP = NDIFF and NWELL
TAP = PTAP or NTAP
GATE = POLY and ACTIVE
NGATE = POLY and NACTIVE
PGATE = POLY and PACTIVE

3.2. General rules

Table 2. NWELL Rules

Rule #	Rule description	μm	Mark
NWELL.W.1	Minimum width	0.23	a
NWELL.S.1	Minimum spacing between wells at same potential	0.23	b
NWELL.S.2	Minimum spacing between wells at different potential	0.46	c
NWELL.A.1	Minimum Area	0.45	d
NWELL.A.2	Minimum Enclosed area	0.45	e

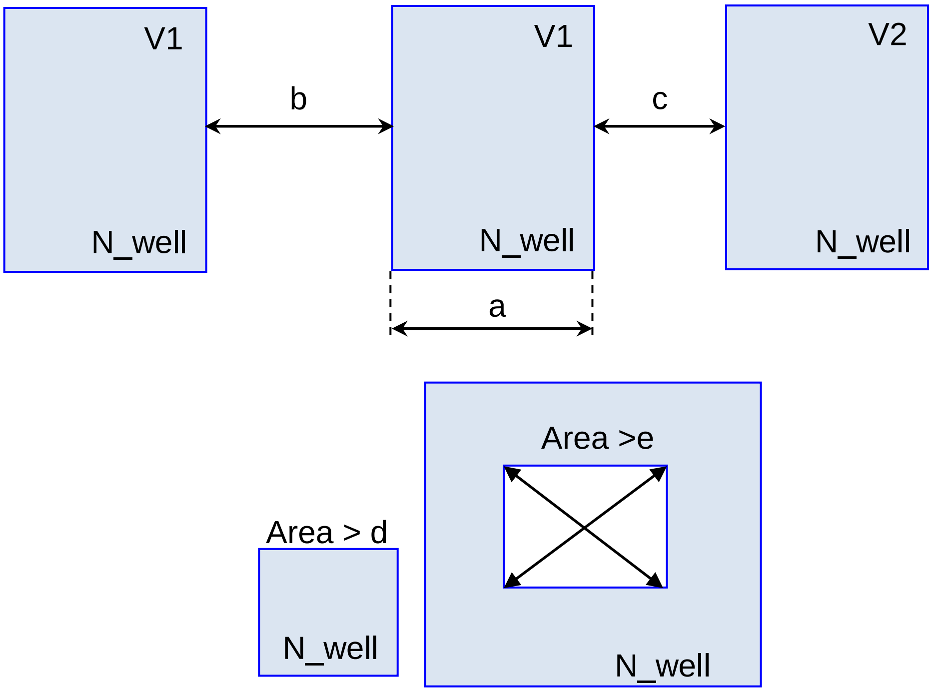


Figure 6. NWELL Rules

Table 3. Deep N Well (DNW) Rules

Rule #	Rule description	µm	Mark
DNW.W.1	Minimum width	3	a
DNW.S.1	Minimum spacing, DNW to DNW	3.5	b
DNW.S.2	Minimum spacing, DNW to unrelated NWELL	2.5	c
DNW.S.3	Minimum spacing, external N+Active to DNW	1.5	d
DNW.S.4	Minimum spacing, P+Active in NWELL to its DNW	1	e
DNW.E.1	Minimum enclosure, N+Active by isolated P-well	0.7	f
DNW.E.2	Minimum enclosure, NWELL beyond DNW edge	1	g
DNW.O.1	Minimum overlap, NWELL over DNW edge	0.4	h

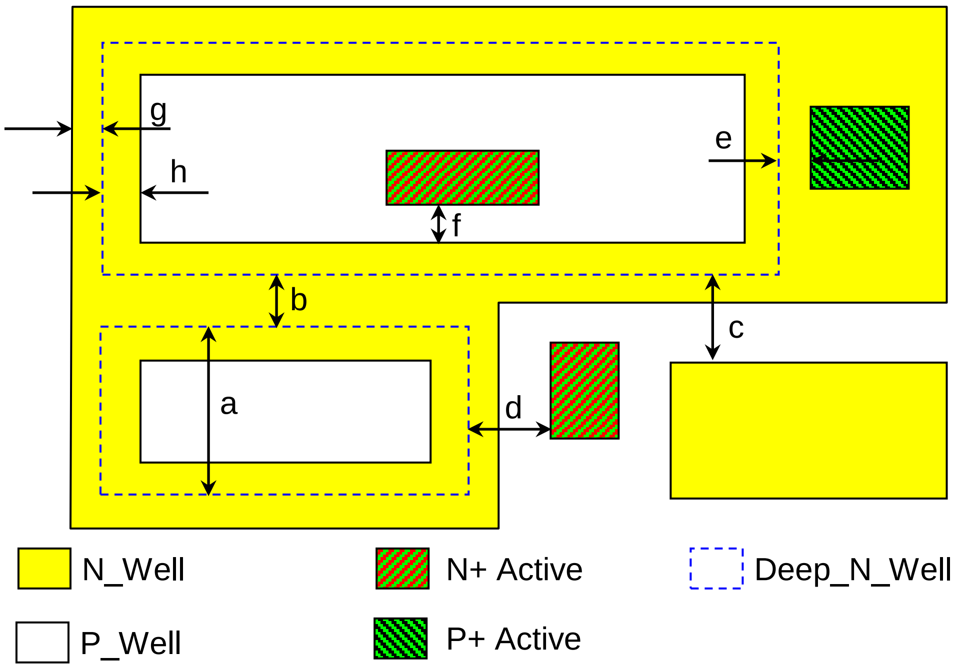


Figure 7. DNW Rules

Table 4. DIFF Rules

Rule #	Rule description	µm	Mark
DIFF.W.1	Minimum width	0.044	a
DIFF.W.2	Minimum span when space on at least one side is > 0.090 µm (for run length > 0.100 µm).	0.055	g
DIFF.W.3	Minimum span when space on at least one side is > 0.150 µm (for run length > 0.100 µm).	0.065	g
DIFF.S.1	Minimum spacing	0.05	b
DIFF.S.1	Minimum spacing if width > 0.1	0.1	b
DIFF.S.2	Minimum spacing to DIFF_18	0.15	c
DIFF.S.3	Minimum spacing to DIFF_25	0.15	c
DIFF.S.4	Minimum spacing of edge with span < 0.080 µm	0.07	f
DIFF.S.5	Minimum spacing of edge with 0.080 < span < 0.150 µm	0.08	f
DIFF.S.6	Minimum spacing of edge with span > 0.150 µm	0.085	f
DIFF.E.1	Source/drain active to well edge (min enclosure by well)	0.065	d
DIFF.E.2	Substrate/well contact diff to well edge (min enclosure by well)	0.07	e
DIFF.A.1	Minimum area	0.02	h
DIFF.A.2	Enclosed Area	0.03	k
DIFF.W.2	Min channel width	0.1	j
DIFF.W.3	Max channel width	3.5	i
DIFF.R.1	DIFF w/o IMP is not allowed	-	

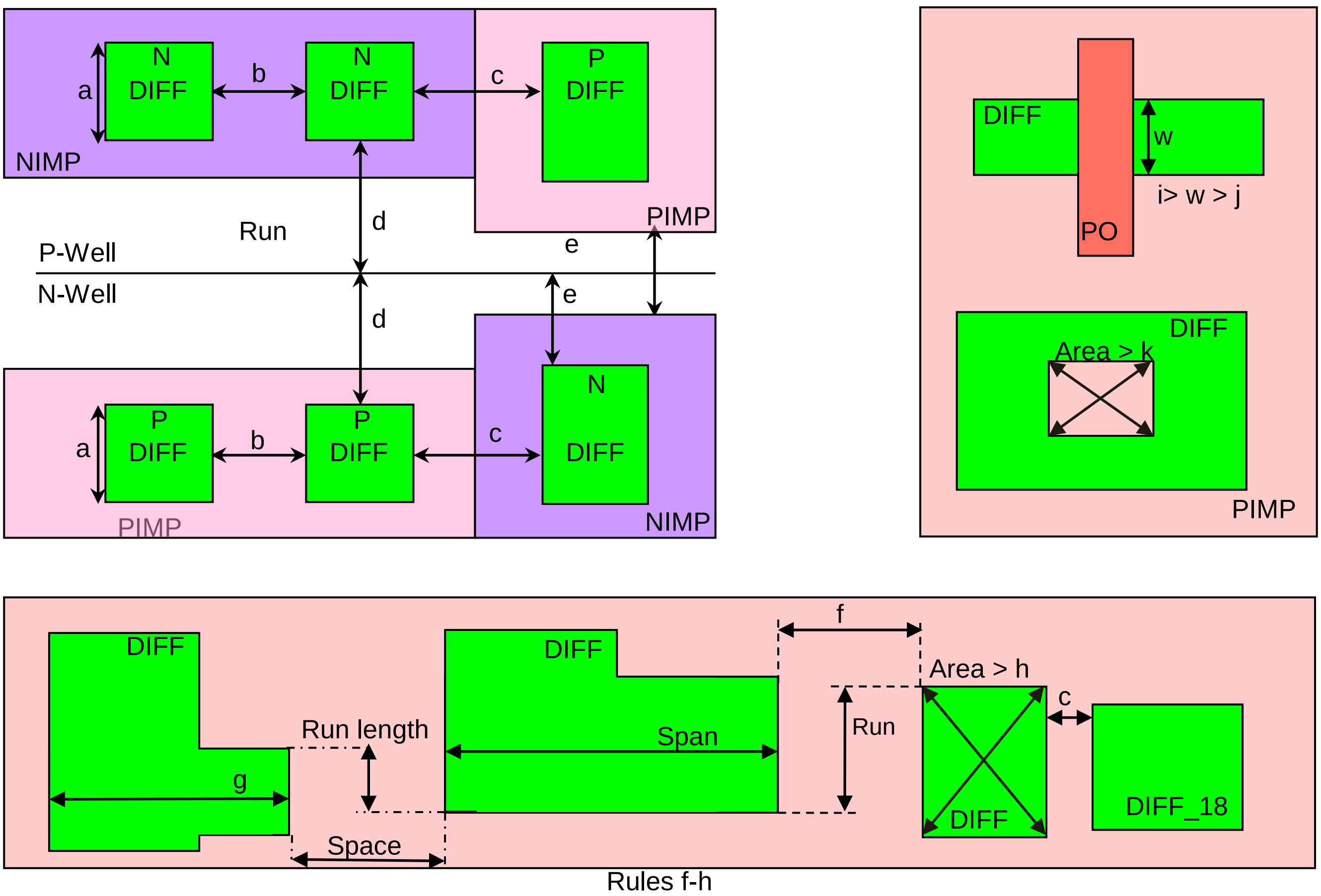


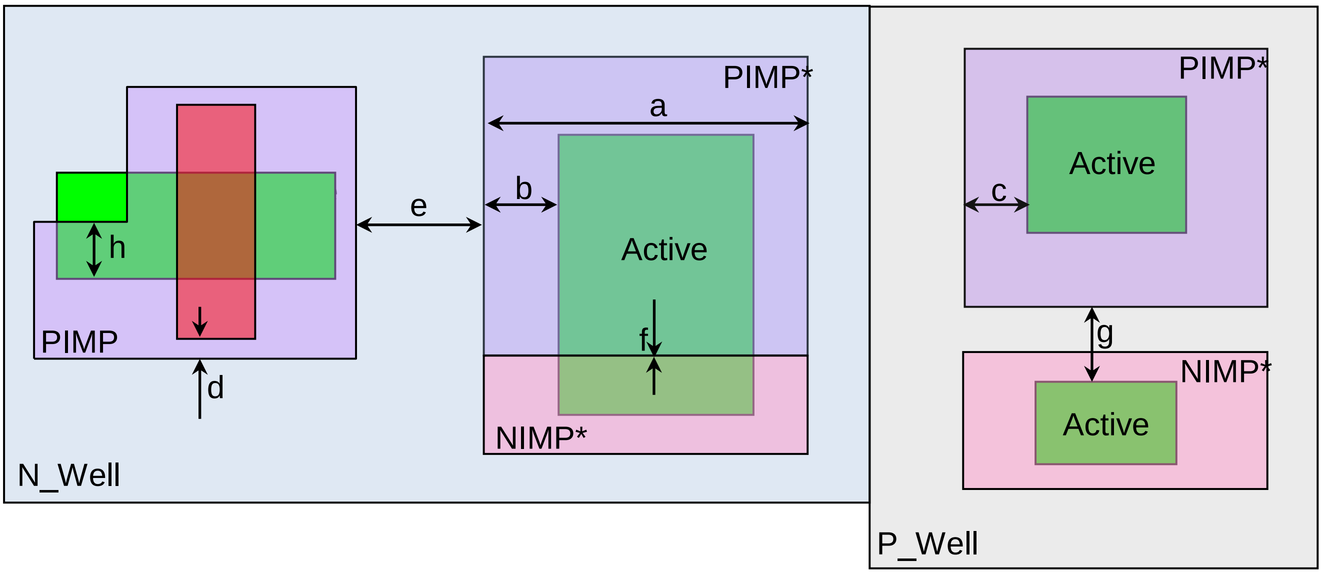
Figure 8.DIFF Rule

Table 5. NIMP Rules

Rule #	Rule description	µm	Mark
NIMP.W.1	Minimum width	0.17	a
NIMP.E.1	Enclosure of N+Active	0.05	b
NIMP.E.2	Enclosure of NTAP	0.02	c
NIMP.E.3	Poly enclosure	0.065	d
NIMP.S.1	Minimum space	0.17	e
NIMP.S.2	Minimum space to butted P+Active	0	f
NIMP.S.3	Minimum space to P+Active in NWELL	0.05	g
NIMP.O.1	Minimum active overlap	0.05	h

Table 6. PIMP Rules

Rule #	Rule description	µm	Mark
PIMP.W.1	Minimum width	0.17	a
PIMP.E.1	Enclosure of P+Active	0.05	b
PIMP.E.2	Enclosure of PTAP	0.02	c
PIMP.E.3	Poly enclosure	0.065	d
PIMP.S.1	Minimum space	0.17	e
PIMP.S.2	Minimum space to butted N+Active	0	f
PIMP.S.3	Minimum space to N+Active in PWELL	0.05	g
PIMP.O.1	Minimum active overlap	0.05	h



Note: The same rules apply to NIMP reversed.

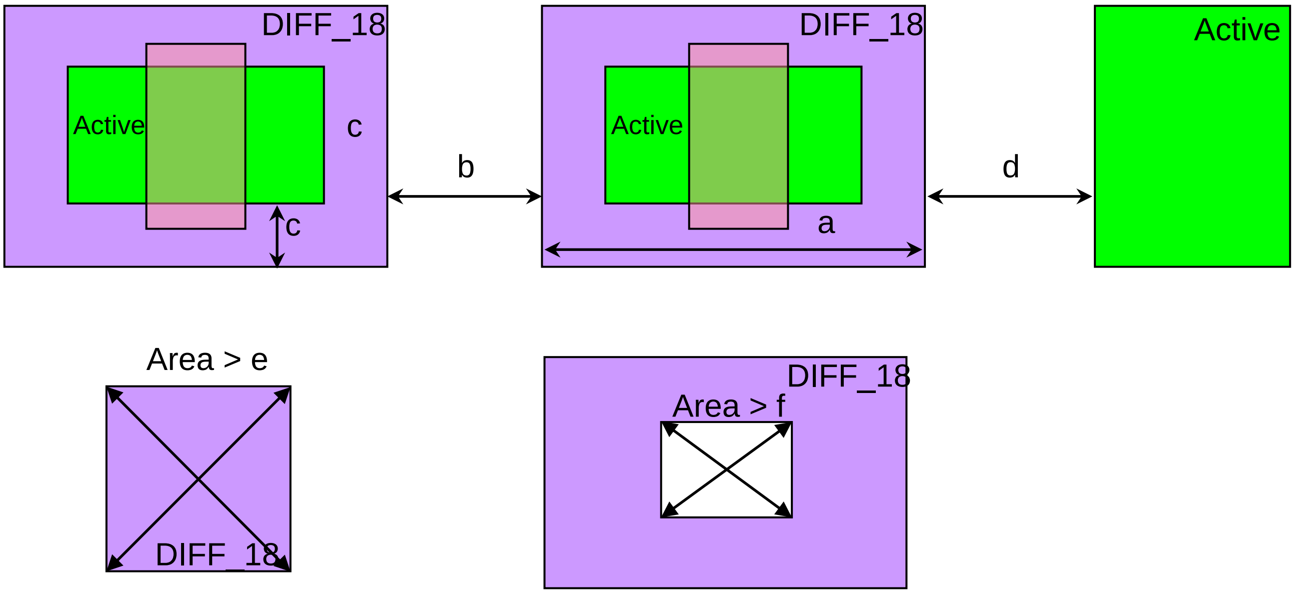
Figure 9. PIMP,NIMP Rules

Table 7. DIFF_18 Rules

Rule #	Rule description	μm	Mark
DIFF_18.W.1	Minimum width	0.33	a
DIFF_18.S.1	Minimum Spacing	0.33	b
DIFF_18.E.1	Minimum DIFF enclosure	0.15	c
DIFF_18.S.2	Minimum space to external DIFF	0.15	d
DIFF_18.A.1	Min area	0.40	e
DIFF_18.A.2	Max enclosed area	0.40	f

Table 8. DIFF_25 Rules

Rule #	Rule description	μm	Mark
DIFF_25.W.1	Minimum width	0.33	a
DIFF_25.S.1	Minimum Spacing	0.33	b
DIFF_25.E.1	Minimum DIFF enclosure	0.15	c
DIFF_25.S.2	Minimum space to external DIFF	0.15	d
DIFF_25.A.1	Min area	0.40	e
DIFF_25.A.2	Max enclosed area	0.40	f



Note: The same rules apply to DIFF_25

Figure 10. DIFF_18 Rules

Table 9. SBLK Rules

Rule #	Rule description	µm	Mark
SBLK.W.1	Minimum SBLK width	0.33	a
SBLK.S.1	Minimum SBLK spacing	0.33	b
SBLK.S.2	Minimum spacing, SBLK to contact (no contacts allowed inside SBLK)	0.13	c
SBLK.S.3	Minimum spacing, SBLK to external diff	0.18	d
SBLK.S.4	Minimum spacing, SBLK to external poly	0.3	e
SBLK.S.5	Minimum spacing of poly resistors (in a single SBLK region)	0.3	f
SBLK.S.6	Minimum spacing, SBLK to poly (in a single active region)	0.4	g
SBLK.C.1	Resistor is poly inside SBLK: poly ends stick out for contacts the entire resistor must be outside well and over field	-	
SBLK.W.2	Minimum poly within unsalicided resistor	0.4	h
SBLK.O.1	Minimum SBLK extension of poly or active	0.18	i
SBLK.O.2	Minimum poly extension of SBLK	0.18	j

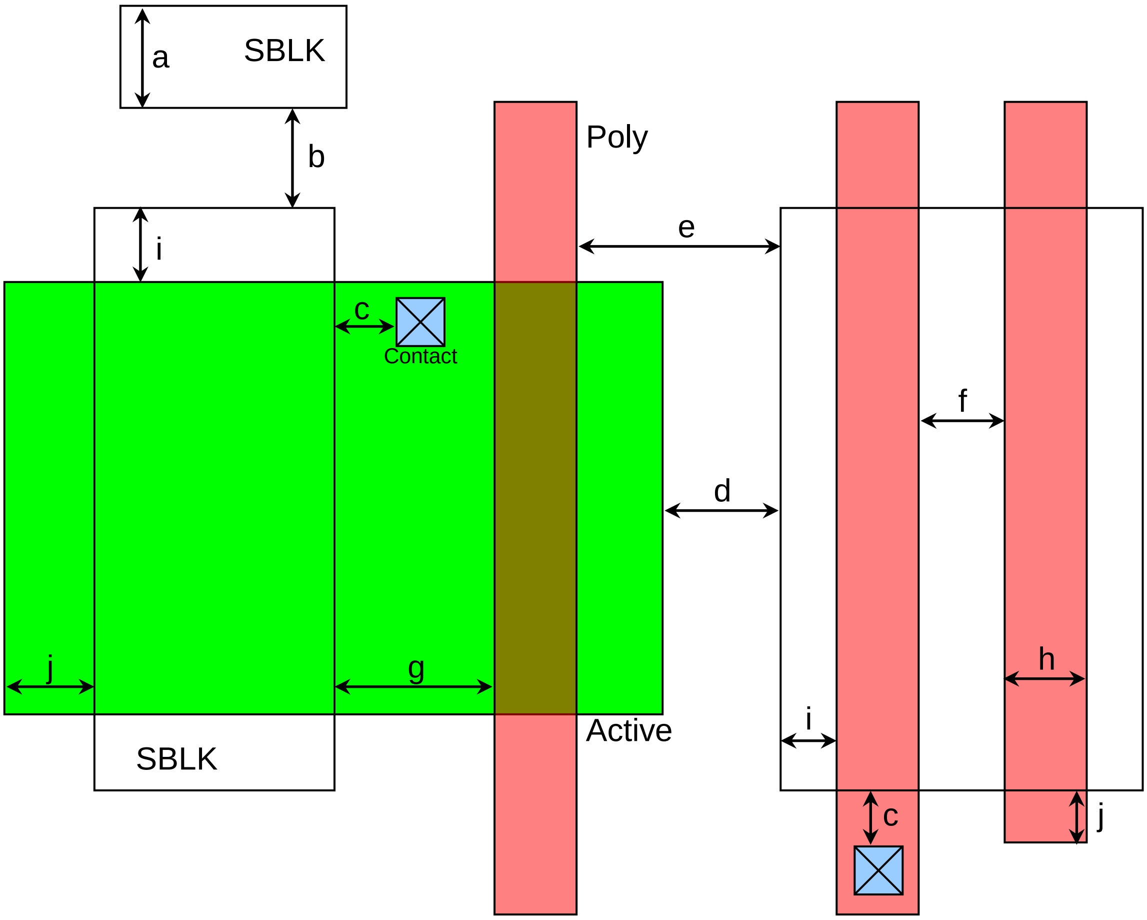


Figure 11. SBLK Rules

Table 10. PO Rules

Rule #	Rule description	μm	Mark
PO.W.1	Minimum width	0.03	a
PO.W.2	Minimum width of horizontal drawn rectangular or L-shape PO	0.04	b
PO.W.3	Minimum width of horizontal drawn PO	0.064	c
PO.W.4	Minimum poly width in a thick oxide gate	0.3	-
PO.S.1	Minimum spacing over field	0.1	e
PO.S.2	Minimum spacing over active	0.086	f
PO.S.3	Minimum spacing over active, if channel length > 0.1	0.13	
PO.S.4	Minimum spacing of edge with span > 0.1 μm, parallel runlength > 0.1μm	0.125	g
PO.S.5	Minimum field poly to DIFF of the same MOS	0.035	h
PO.S.6	Minimum poly to DIFF	0.05	i
PO.S.7	Minimum poly to DIFF with width<0.08 μm, parallel runlength > 0.1 μm	0.035	j
PO.EX.1	Minimum gate extension of active (end cap)	0.08	k
PO.EX.2	Minimum active extension of gate	0.085	l
PO.G.1	45 degree and 90 degree bent gates are not allowed	-	-
PO.A.1	Minimum area (μm^2)	0.012	m
PO.A.2	Maximum Gate area (μm^2)	40	n

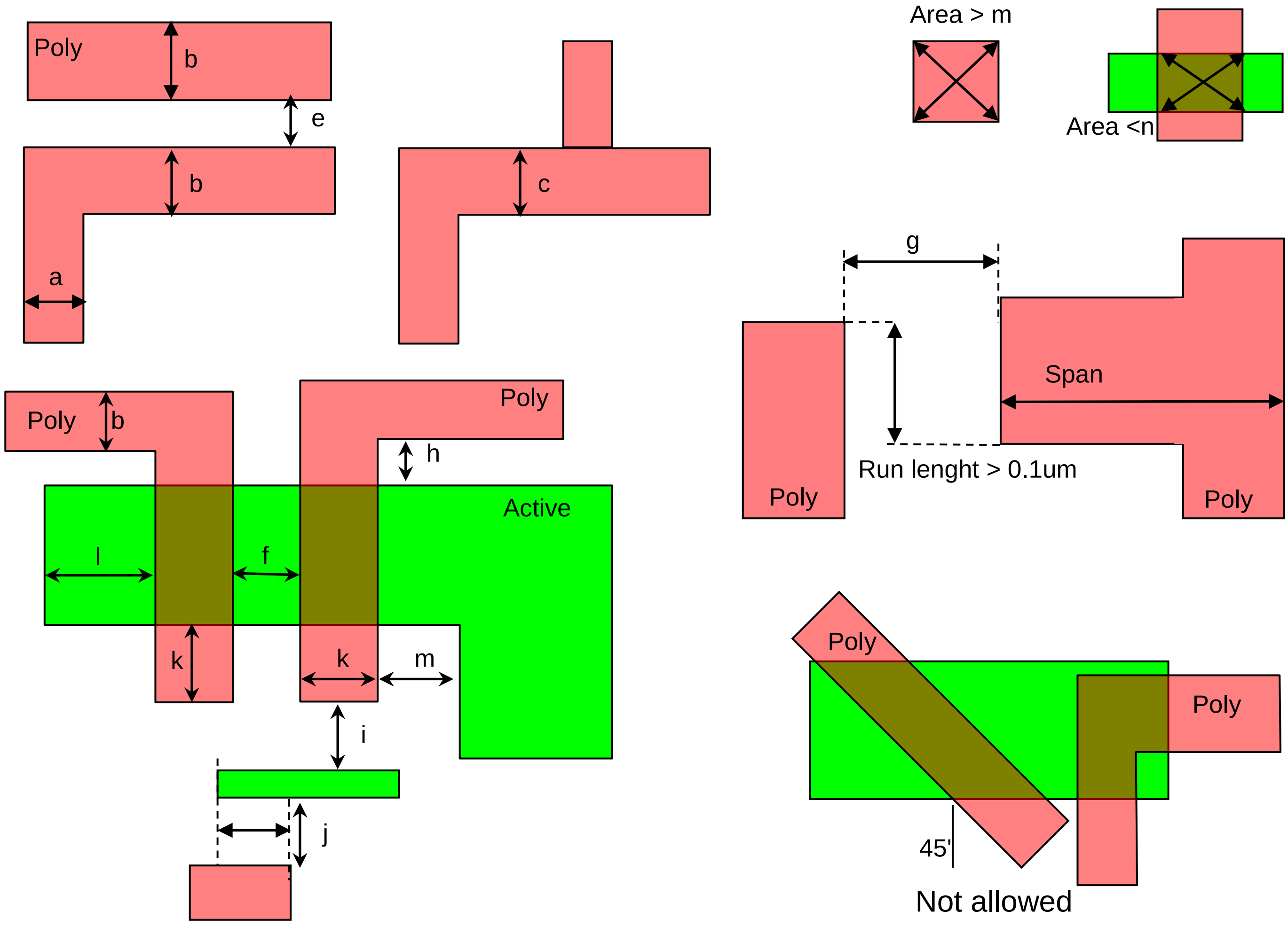


Figure 12. PO Rules

Table 11. M1 Rules

<table>
<tr><th>Rule #</th><th colspan="2">Rule description</th><th>µm</th><th>Mark</th></tr>
<tr><td>M1.W.1</td><td colspan="2">Minimum width</td><td>0.05</td><td>a</td></tr>
<tr><td>M1.W.2</td><td colspan="2">Maximum width</td><td>5</td><td>e</td></tr>
<tr><td>M1.S.1</td><td colspan="2">Minimum spacing</td><td>0.05</td><td>b</td></tr>
<tr><td rowspan="2"></td><td colspan="2">Minimum spacing depending on metal width of one of lines and their parallel run length</td><td rowspan="2"></td><td rowspan="2">j</td></tr>
<tr><td>metal width</td><td>parallel run length</td></tr>
<tr><td>M1.S.2</td><td>> 0.15µm</td><td>> 0.15µm</td><td>0.06</td><td>j1</td></tr>
<tr><td>M1.S.3</td><td>> 0.3µm</td><td>> 0.3µm</td><td>0.1</td><td>j2</td></tr>
<tr><td>M1.S.4</td><td>> 1.5µm</td><td>> 1.5µm</td><td>0.5</td><td>j3</td></tr>
<tr><td>M1.S.5</td><td>> 3µm</td><td>> 3µm</td><td>0.6</td><td>j4</td></tr>
<tr><td>M1.S.6</td><td colspan="2">Minimum spacing of MX with span > 0.075 µm with parallel run length > 0.104 µm</td><td>0.060</td><td>i</td></tr>
<tr><td>M1.S.7</td><td colspan="2">Minimum spacing of MX with span > 0.150 µm with parallel run length > 0.104µm</td><td>0.065</td><td>i</td></tr>
<tr><td>M1.A.1</td><td colspan="2">Minimum Area</td><td>0.01</td><td>f</td></tr>
<tr><td>M1.A.2</td><td colspan="2">Minimum Enclosed area</td><td>0.2</td><td>g</td></tr>
<tr><td>M1.R.1</td><td colspan="2">All M1/DIFF intersections that have a CO shape must have more than 2 COs.</td><td>-</td><td>-</td></tr>
<tr><td>M1.R.2</td><td colspan="2">All M1/PO intersections that have a CO shape must have more than 2 COs.</td><td>-</td><td>-</td></tr>
</table>

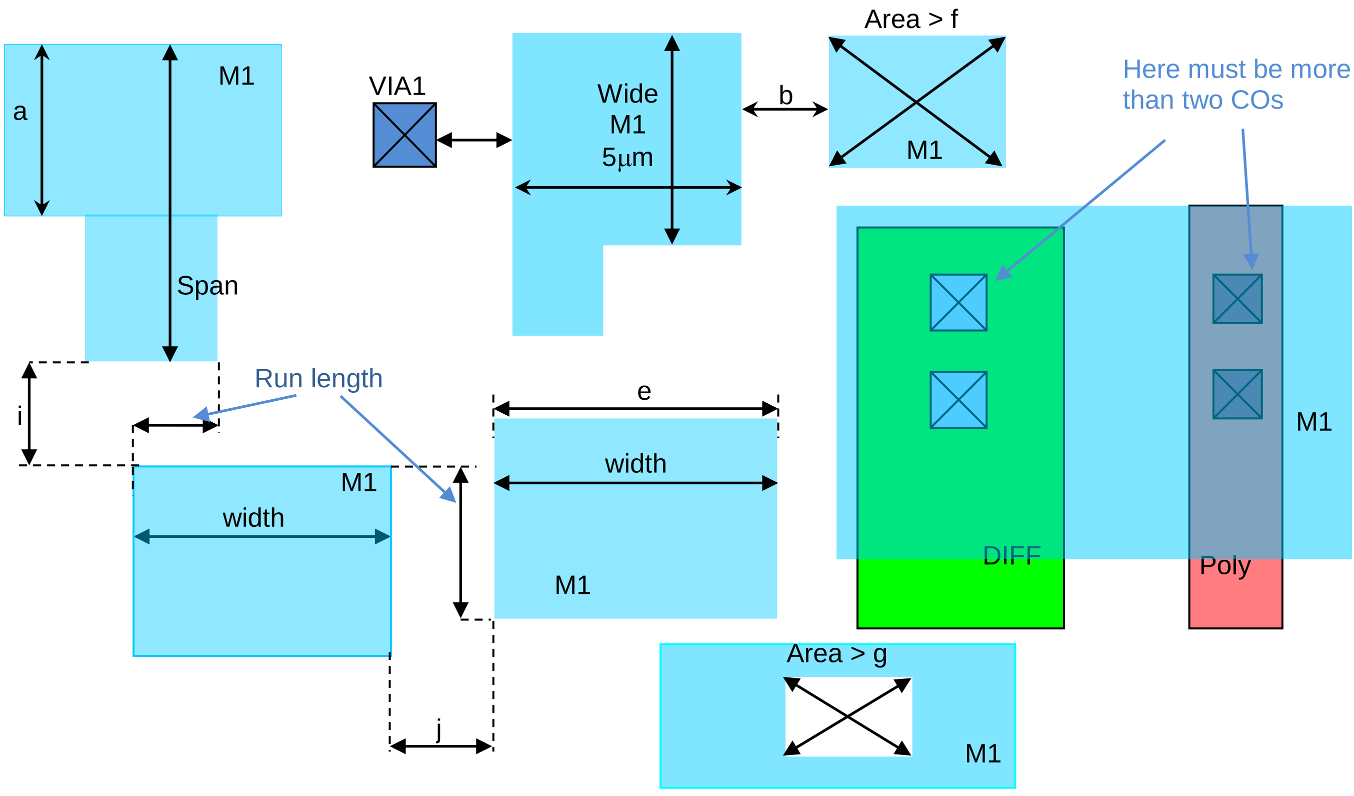


Figure 13. M1 Rules

Table 12. MX Rules, where X=2...T-1

Rule #	Rule description		µm	Mark
MX.W.1	Minimum width		0.056	a
MX.W.2	Maximum width		5	e
MX.S.1	Minimum spacing		0.056	b
MX.S.2	Minimum spacing when either metal line is wider than 0.5 µm		0.12	c
	Minimum spacing depending on metal width of one of lines and their parallel run length			j
	metal width (c)	parallel run length (d)		
MX.S.2	> 0.15µm	> 0.15µm	0.064	j1
MX.S.3	> 0.3µm	> 0.3µm	0.11	j2
MX.S.4	> 1.5µm	> 1.5µm	0.6	j3
MX.S.5	> 3µm	> 3µm	0.7	j4
MX.S.6	Minimum spacing of MX with span > 0.076 µm with parallel run length > 0.104 µm		0.7	i
MX.S.7	Minimum spacing of MX with span > 0.150 µm with parallel run length > 0.104µm		0.76	i
MX.S.8	Minimum spacing to neighboring VIA1 or VIAx		0.08	h
MX.A.1	Minimum Area		0.016	f
MX.A.2	Minimum Enclosed area		0.2	g

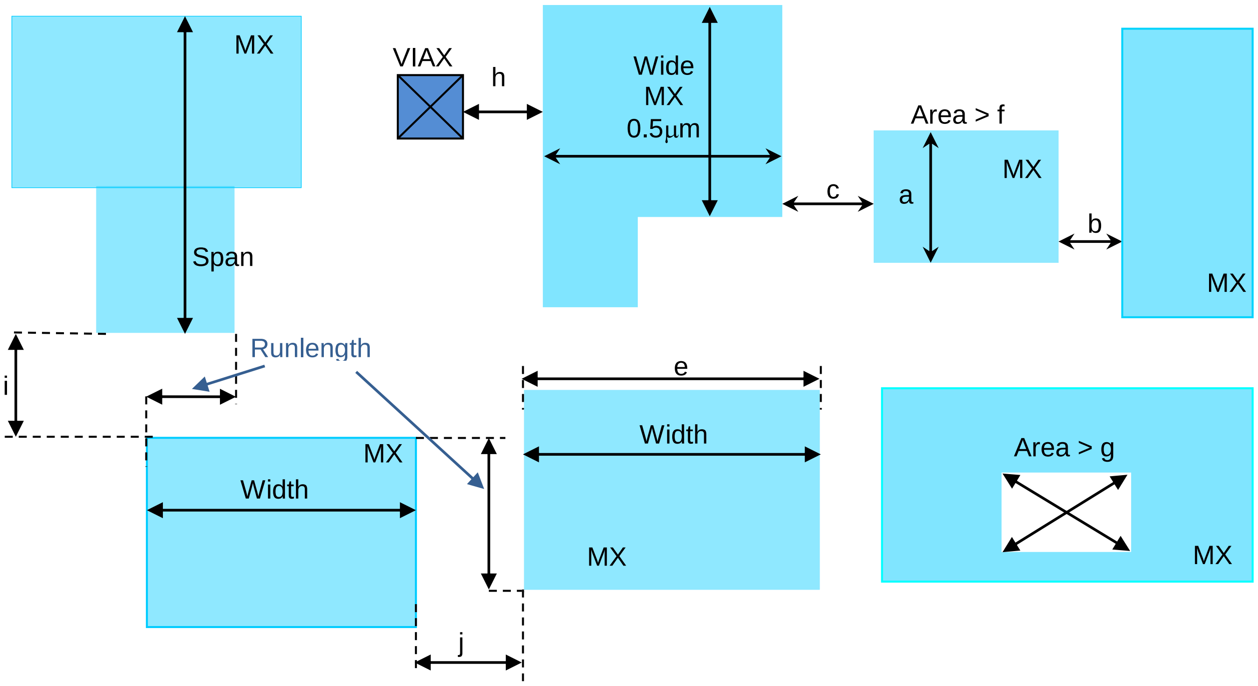


Figure 14. MX Rules

Table 13. MT Rules

Rule #	Rule description	µm	Mark
MT.W.1	Minimum width	0.16	a
MT.W.2	Maximum width	10	b
MT.S.1	Minimum spacing	0.16	c
MT.S.2	Minimum spacing when either metal line is wider than 0.5 µm, when parallel length > 0.5µm	0.18	d
MT.S.3	Minimum spacing when either metal line is wider than 1.7 µm, when parallel length > 1.7µm	0.5	d
MT.S.4	Minimum spacing of MT with span > 0.075 µm with parallel run length > 0.104 µm	0.065	e
MT.S.5	Minimum spacing of MT with span > 0.150 µm with parallel run length > 0.104µm	0.06	e
MT.A.1	Minimum Area	0.055	f
MT.A.2	Minimum Enclosed area	0.2	g

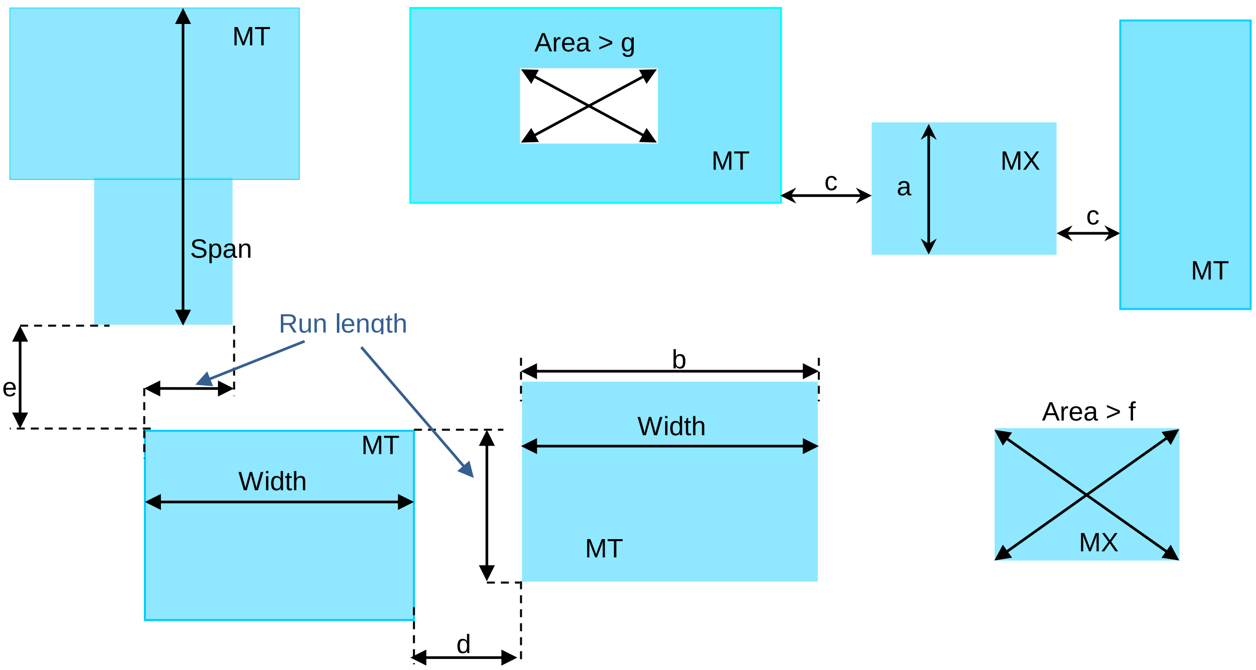


Figure 15. MT Rules

Table 14. MRDL Rules

Rule #	Rule description	µm	Mark
MRDL.W.1	Minimum width	2	a
MRDL.W.2	Maximum width	30	b
MRDL.S.1	Minimum spacing	2	c

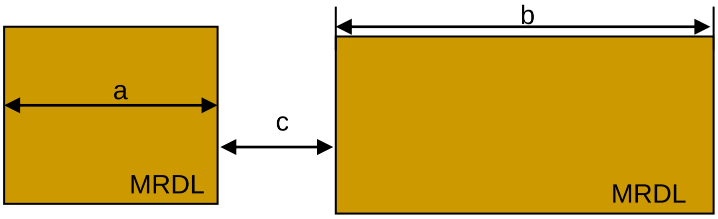


Figure 16. MRDL Rules

Table 15. CO Rules

Rule #	Rule description	µm	Mark
CO.W.1	Exact contact size	0.042	a
CO.S.1	Minimum contact spacing	0.05	b
CO.S.2	Minimum contact spacing to contact on the different net	0.07	c
CO.S.3	(Contact inside DIFF) space to gate	0.04	d
CO.S.4	(Contact inside Poly) space to Active	0.04	e
CO.E.1	Minimum enclosure by poly, if PO width < 0.042	-0.006	f
CO.E.2	Minimum enclosure by poly, if PO 0.042 ≤ width ≤ 0.1	0	f
CO.E.3	Minimum enclosure by poly, if PO width > 0.1	0.02	f
CO.E.4	Minimum enclosure by poly, if PO width ≤ 0.1, at least two opposite sides	0.034	g
CO.E.5	Minimum enclosure by poly if PO width > 0.1, at least two opposite sides	0.05	g
CO.E.6	Minimum enclosure by DIFF	0.01	h
CO.E.7	Minimum enclosure by DIFF at least two opposite sides	0.02	i
CO.E.8	Minimum butted diffusion IMP enclosure of S/D contact	0.06	j
CO.E.9	Minimum enclosure of any contact by M1 (CO outside M1 is not allowed)	0.004	k
CO.E.10	Minimum enclosure of contact by M1 at end of line	0.035	l
CO.R.1	CO must be fully covered by M1, and by PO widened by 0.006	-	-
CO.R.2	It is not allowed to place CO on gate	-	-

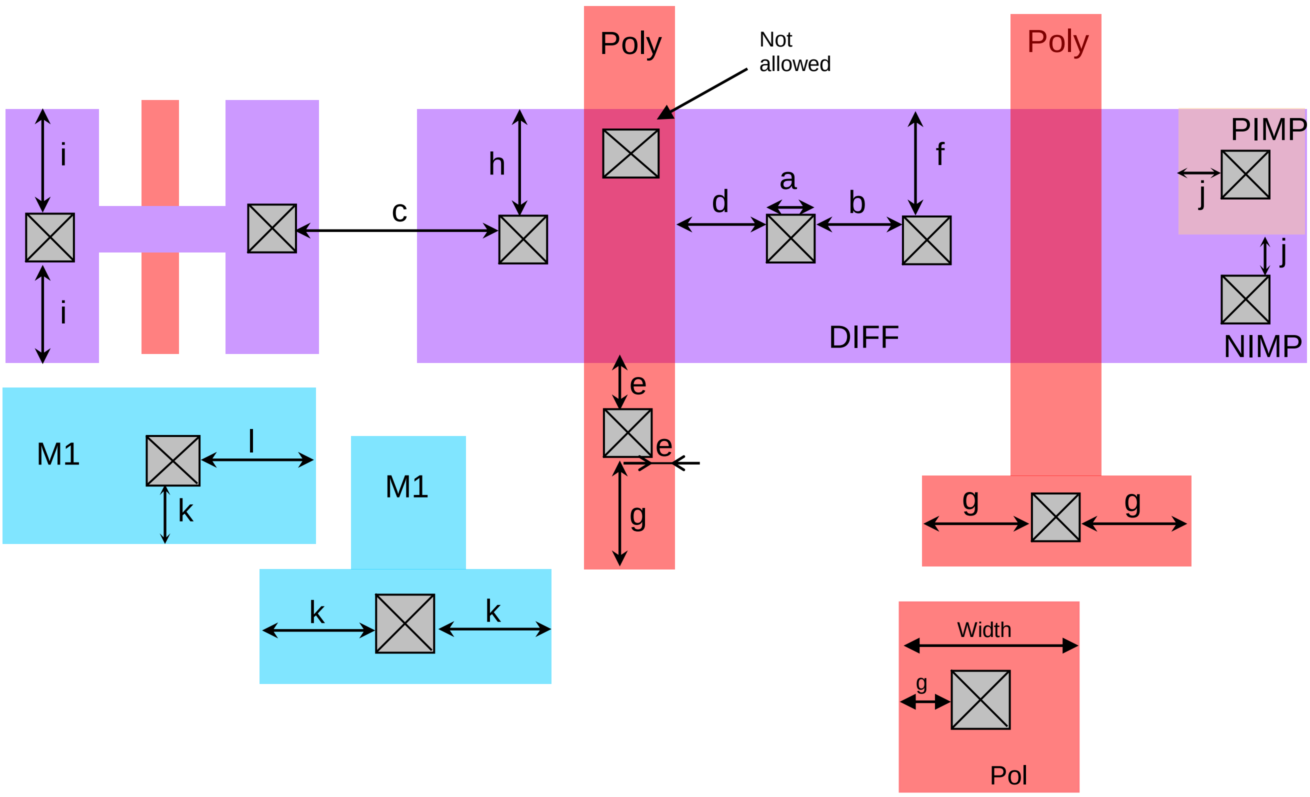


Figure 17. CO Rules

Table 16. VIAX Rules, where X=1..T-2

Rule #	Rule description	µm	Mark
VIAX.W.1	Exact length and width of square cut VIAx (VIAxSQ)	0.05	a
VIAX.W.2	Exact length and width of large square cut VIAx(VIAxLG)	0.10	b
VIAX.W.3	Exact length of rectangular cut VIAx (VIAxBAR)	0.10	c
VIAX.W.4	Exact width of rectangular cut VIAx (VIAxBAR)	0.05	d
VIAX.S.1	Minimum spacing of VIAxSQ to VIAxSQ	0.07	e
VIAX.S.2	Minimum spacing of VIAxSQ to VIAxBAR or VIAxLG	0.08	f
VIAX.S.3	Minimum spacing of VIAxBAR or VIAxLG to VIAxBAR or VIAxLG	0.085	g
VIAX.E.1	Minimum VIAx enclosure by MX and MX+1	0.005	h
VIAX.E.2	Minimum VIAx enclosure by MX and MX+1 at least two opposite sides	0.03	i
VIAX.E.3	Minimum rectangular VIAx enclosure by MX and MX+1 at end of via	0.005	j
VIAX.R.1	When MX or MX+1 width >0.2um, it is a must to have redundant VIAs	-	k
VIAX.R.1.1	At least one rectangular VIAx	-	k1
VIAX.R.1.2	At least two square VIAx with spacing of 0.15um	-	k2
VIAX.R.1.3	At least four square VIAx with spacing of 0.7um	-	k3
VIAX.R.2	VIAx must be fully covered by MX and MX+1	-	-

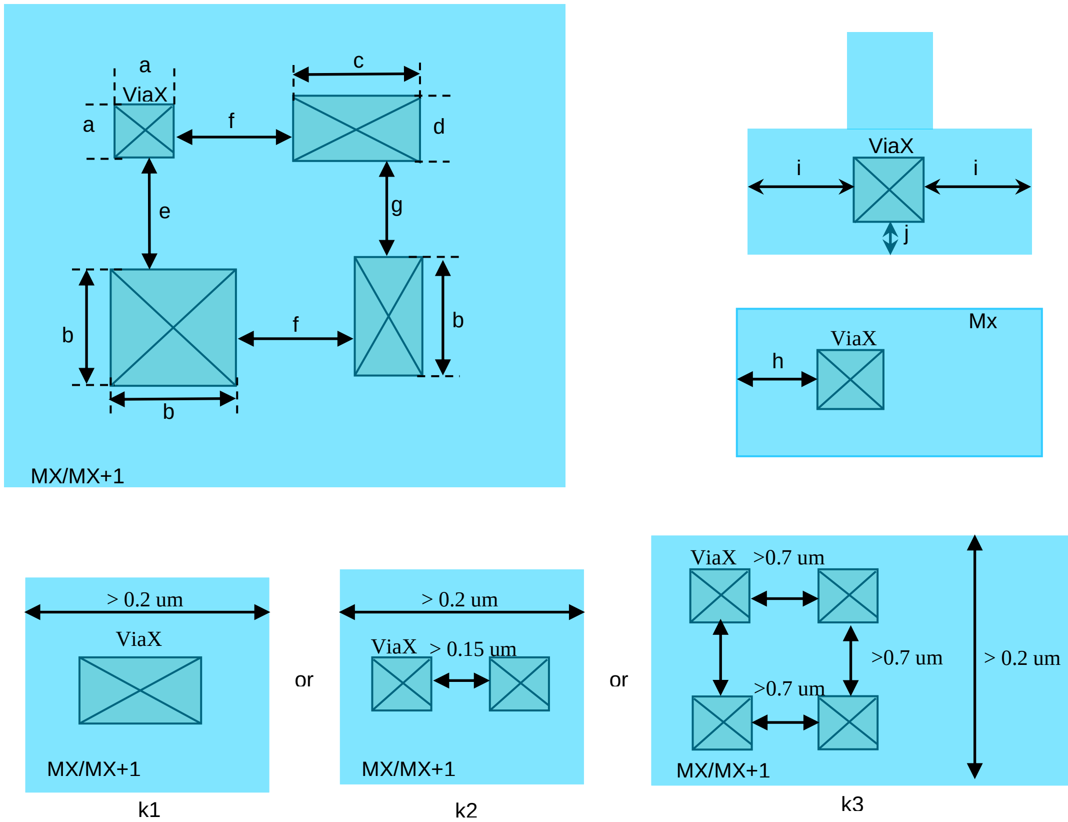
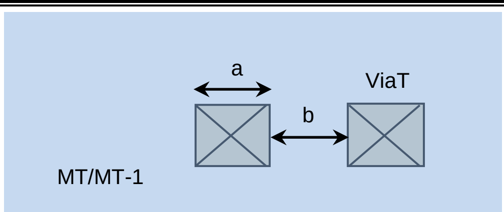
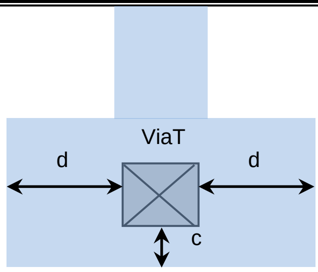


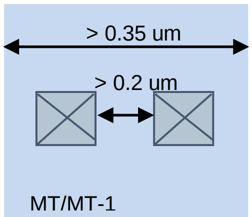
Figure 18. VIAX Rules

Table 17. VIAT Rules

Rule #	Rule description	µm	Mark
VIAT.W.1	Exact size	0.13	a
VIAT.S.1	Minimum viaX spacing	0.12	b
VIAT.E.1	Minimum VIAT enclosure by MT and MT-1	0.015	c
VIAT.E.2	Minimum VIAT enclosure by MT and MT-1 at end of line	0.03	d
VIAT.R.1	Redundant VIAT when MX or MT width >0.35um, it is a must to have 1. At least two VIAT with spacing of 0.2um 2. At least four VIAT with spacing of 0.5um	-	e e1 e2
VIAT.R.2	Redundant VIAT when MX or MT width >0.7um, it is a must to have 1. At least four VIAT with spacing of 0.2um 2. At least nine VIAT with spacing of 0.5um	-	f f1 f2
VIAT.R.3	At least two VIAT are required when connection distance is <3um, from fat wire with WxL=3x3um	-	g
VIAT.R.4	At least two VIAT are required when connection distance is <5um, from fat wire with WxL=10x5um	-	g
VIAT.R.5	VIAT must be placed orthogonal, rotation is not allowed	-	-
VIAT.R.6	VIAT must be fully covered by MX and MX+1	-	-

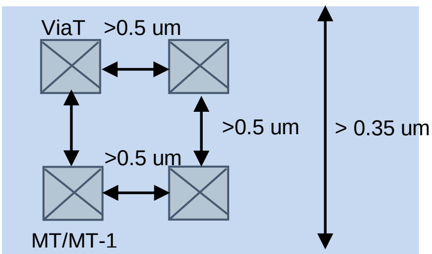




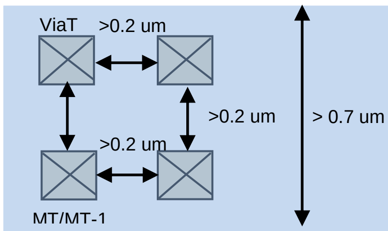


e1

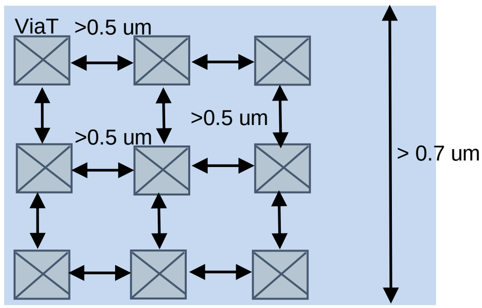
or



e2



f1



f2

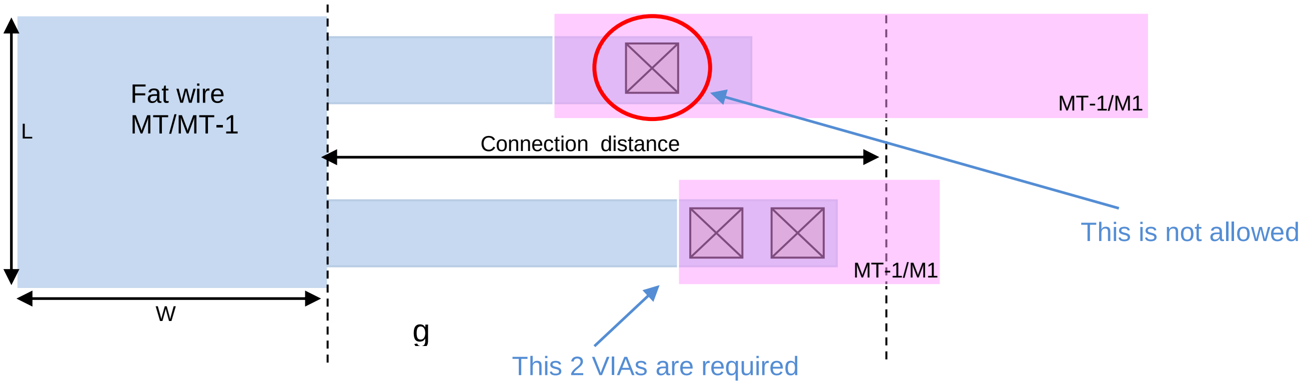


Figure 19. VIAT Rules

Table 18. VIARDL Rules

Rule #	Rule description	µm	Mark
VIARDL.W.1	Exact size	2	a
VIARDL.S.1	Minimum VIARDL spacing	2	b
VIARDL.E.1	Minimum VIARDL enclosure by MRDL	0.5	c

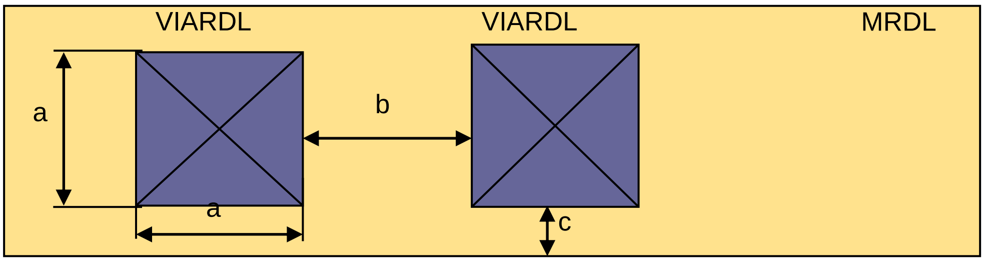


Figure 20. VIARDL Rules

Table 19. HVTIMP Rules

Rule #	Rule description	μm	Mark
HVTIMP.W.1	Minimum width	0.85	a
HVTIMP.S.1	Minimum spacing	0.85	b
HVTIMP.E.1	Minimum enclosure	0.05	c

Table 20. LVTIMP Rules

Rule #	Rule description	μm	Mark
LVTIMP.W.1	Minimum width	0.85	a
LVTIMP.S.1	Minimum spacing	0.85	b
LVTIMP.E.1	Minimum enclosure	0.05	c

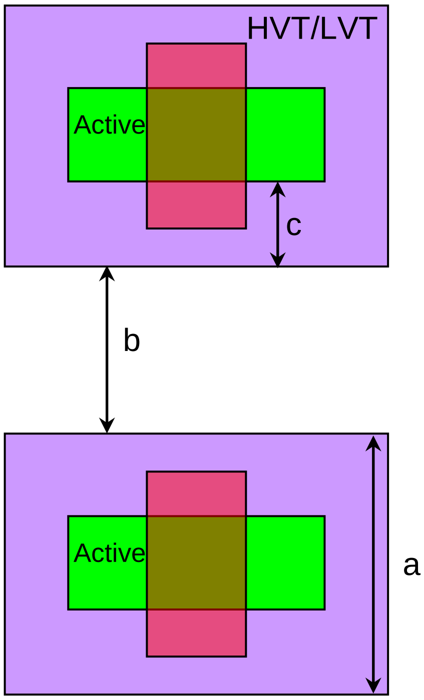


Figure 21. HVTIMP, LVTIMP Rules

Table 21. PAD Rules

Rule #	Rule description	µm	Mark
PAD.W.1	Minimum bonding passivation opening width	30	a
PAD.W.2	Minimum bonding passivation opening length	70	b
PAD.W.3	Flip-chip passivation opening (octagon) width	50	c
PAD.W.4	Flip-chip passivation opening (octagon) length	70	d
PAD.E.1	Pad metal enclose of passivation opening	1	e
PAD.S.1	Minimum space	10	f
PAD.S.2	Minimum pad metal spacing to unrelated metal	2	g

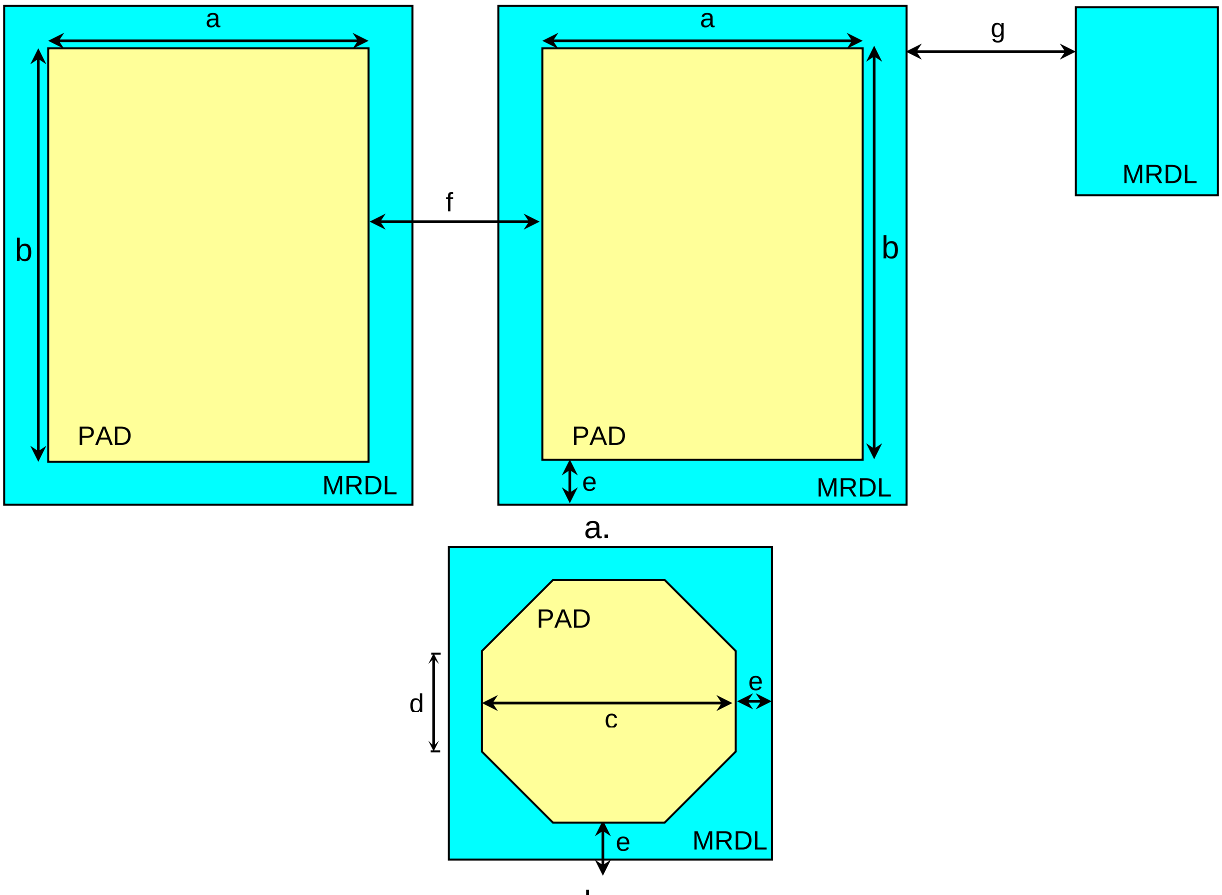


Figure 22. PAD (a. Wire-bond opening, b. Flip-Chip opening)

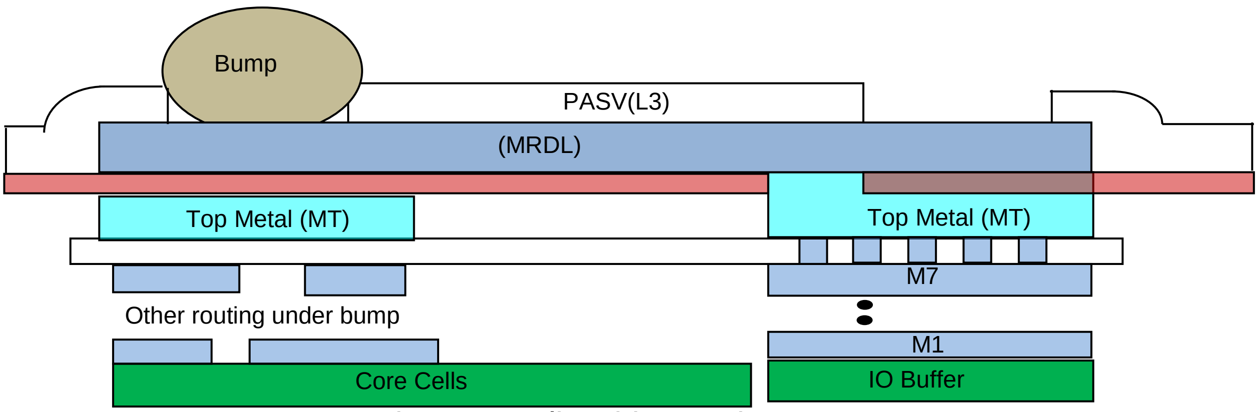


Figure 23. Flip-Chip opening structure

3.3. Antenna rules

Table 22. Antenna Rules

Rule #	Rule description	Minimum Ratio	
PO.AN.1	Minimum poly Ratio	250	
PO.AN.2	Minimum poly perimeter Ratio	500	
CO.AN.3	Minimum Area(CO) / Area(Gate)	10	
		without effective diode	with effective diode
M1.AN.1	Minimum M1 ratio	1000	(diode area)*456+43000
MX.AN.1	Minimum MX ratio	1000	(diode area)*456+43000
VIAX.AN.1	Minimum ViaX ratio	20	(diode area)*210+900

3.4. Density and fill rules

Table 23. Density Rules, where X=2...T-1

Rule #	Rule description		Rule
DIFF.DN.1	DIFF density in whole chip	≥	20%
		≤	80%
DIFF.DN.1	DIFF density over any 130 µm x 130 µm area (checked by stepping in 75 µm increments)	≥	15%
		≤	85%
PO.DN.1	Poly density in whole chip	≥	15%
		≤	40%
M1.DN.1	Minimum metal density over any 130 µm x 130 µm area (checked by stepping in 75 µm increments).		10%
M1.DN.2	Maximum metal density over any 130 µm x 130 µm area (checked by stepping in 75 µm increments).		85%
MX.DN.1	Minimum metal density over any 130 µm x 130 µm area (checked by stepping in 75 µm increments).		10%
MX.DN.2	Maximum metal density over any 130 µm x 130 µm area (checked by stepping in 75 µm increments).		85%
MT.DN.1	Metal density range in whole chip	≥	15% in 100x100
		≤	60% in 200x200
MT.DN.2	Maximum metal density over any 130 µm x 130 µm area (checked by stepping in 75 µm increments). Bond pad is excluded from 90% check.	≤	90%

Table 24. Fill Rules

Rule	Description	μm	Mark
FILL_WIDTH	Tile width	0.35	w
FILL_HEIGHT	Tile height	0.7	h
FILL_SPACE	Tile spacing to signal net	0.18	d
SPACE_X/Y	Tile spacing	0.18	dt
STAGGER_DIST	Minimum stagger dist	0.18	sd
PATTERN_WIDTH	Fill pattern width	1	pattern _w
PATTERN_HEIGHT	Fill pattern height	0.9	pattern _h

$$Fill\ ratio = \frac{2 \bullet h \bullet w}{pattern\_w \bullet pattern\_h} = 0.49/0.9 = 0.54$$

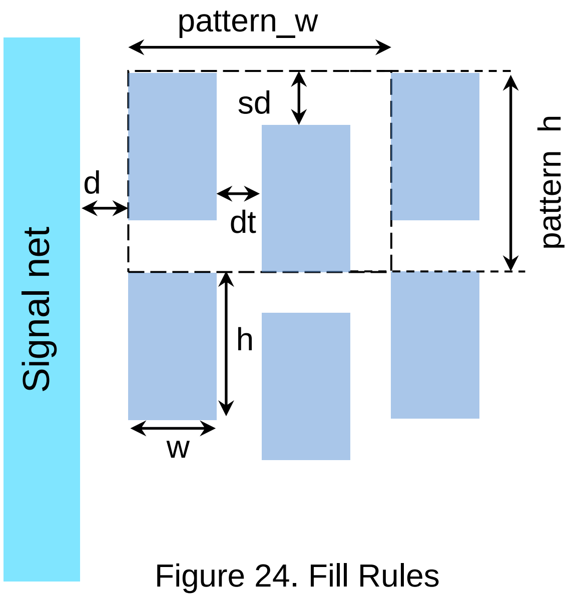


Figure 24. Fill Rules

3.5. Electromigration rules

For DC operation electromigration rules are given by providing I_{max} maximum DC current allowed for conductor with width W. The value of I_{max} is given for 110^0 C temperature depending on layer width W, for other temperatures rating factors F(T) should be used to calculate I_{max}. For example for 125^0 C

$I_{max}(125)=F(125)x\ I_{max}(110),$

Where F(125) is the rating factor for 125^0 C.

Table 25. EM Rating factors (F(T))

Layer(s)	Temperature (°C)						
	95	100	105	110	115	120	125
PO	1.19	1.1	1.05	1	0.93	0.89	0.76
M1, MX, MT	1.55	1.47	1.4	1	0.75	0.55	0.4
MRDL	1.4	1.3	1.2	1	0.8	0.7	0.6

Table 26. Maximum allowed DC current

Rule #	Layer name	I_{max}(mA)
M1.EM.1	M1	0.9 * (W×0.9-0.002)
MX.EM.1	MX	0.9 * (W×0.9-0.002)
MT.EM.1	MT	2 * (W×0.9-0.002)
MRDL.EM.1	MRDL	5 * (W×0.9-0.002)
CO.EM.1	CO	0.1 per contact
VIAX.EM.1	VIAX	0.04 per via
VIAT.EM.1	VIAT	0.08 per via

Table 27. Maximum allowed DC current density for PO

Rule #	Layer name	J_{max}(mA/μm)
PO.EM.1	PO (width ≤ 2μm)	5
PO.EM.1	PO (width > 2μm)	3

For reliability enhancement it is recommended to place VIAs more than it is required by rules.

For AC operation electromigration rules are given for metal layers as maximum allowed AC peak current ($I_{peak} = max(|I(t)|)$) and as a root-mean-square of AC current I_{RMS} ($I_{RMS} = \sqrt{\frac{\int_0^{\tau} I(t)^2 dt}{\tau}}$). The value of root-mean-square is given for 110^0 C, depending on layer width W, for other temperatures the temperature difference ΔT should be used (for 110^0 C ΔT=0, for 115^0 C ΔT=5, etc.).

Table 28. Maximum allowed AC peak current for metal layers

Rule #	Layer name	I_{peak}(mA)
PO.EM.1	PO not SBLK (saliceded)	1.5 * (W×0.9-0.002)
PO.EM.2	PO and SBLK (unsaliceded)	1 * (W×0.9-0.002)
M1.EM.2	M1	18 * (W×0.9-0.002)
MX.EM.2	MX	9 * (W×0.9-0.002)
MT.EM.2	MT	20 * (W×0.9-0.002)
MRDL.EM.3	MRDL	5 * (W×0.9-0.002)

Table 29. Maximum allowed AC current RMS

Rule #	Layer name	I_{RMS}(mA)
PO.EM.3	PO not SBLK (saliceded)	SQRT[0.1 *ΔT* W×0.9× (W×0.9+0.7)]
PO.EM.4	PO and SBLK (unsaliceded)	SQRT[0.05 *ΔT* W×0.9× (W×0.9+1.4)]
M1.EM.3	M1	SQRT[13 *ΔT* (W×0.9-0.003)^2× (W×0.9-0.003+0.2)/ (W×0.9-0.003)]
MX.EM.3	MX	SQRT[2 *ΔT* (W×0.9-0.003)^2× (W×0.9-0.003+0.2)/ (W×0.9-0.003)]
MT.EM.3	MT	SQRT[13 *ΔT* (W×0.9-0.003)^2× (W×0.9-0.003+0.2)/ (W×0.9-0.003)]
MRDL.EM.3	MRDL	SQRT[5 *ΔT* W×0.9 × (W×0.9+2)]

3.6. Layer physical parameters

Table 30. Conductors

Name	Sheet Resistance	Thickness (nm)
DIFF	0.001	50
PO	15	50
M1	0.1	95
M2	0.1	95
M3	0.1	95
M4	0.1	95
M5	0.1	95
M6	0.1	95
M7	0.1	95
M8	0.1	95
M9	0.28	190
MRDL	0.35	280

Table 31. Dielectrics

Name		Thickness (nm)
GOX	3.9	1.5
FOX	3.9	100
D1	3.9	600
D2	3.9	600
D3	3.9	600
D4	3.9	600
D5	3.9	600
D6	3.9	600
D7	3.9	600
D8	3.9	600
D9	3.9	600
PASS	3.9	3000

3.7. Cross section

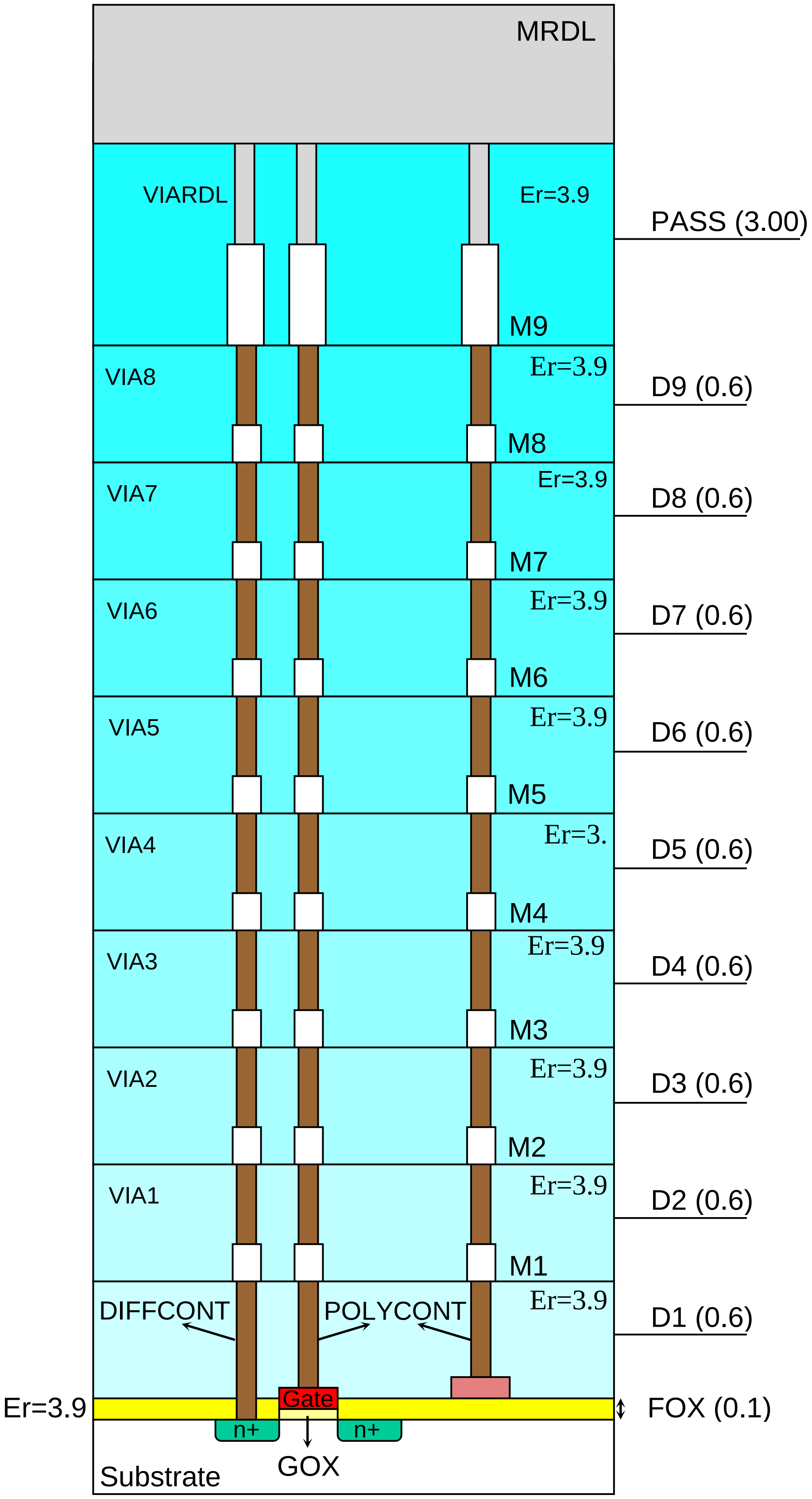


Figure 25. Process Description

4. Revision History

Table 32. Revision History

Revision	Date	Change
A.1	29/12/2010	Initial release
A1.5	27/04/2016	Added capacitor marking layers in layer map