SAED 32/28nm Spice Model Documentation

SAED_EDK32/28_TK_SM

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

1. Introduction

SPICE model library is the part of SAED_EDK32/28 Educational Design Kit and this document is the part of SAED_EDK32/28 Educational Design Kit documentation. It describes the methodology of SPICE model creation and gives the main directions how to use provided files to achieve correct simulation results. Also it is shown the main characteristics of transistors in different operating conditions. These models are obtained from open sources and don't include any confidential or proprietary information of other companies or foundries. However it has characteristics are similar to those of real foundries (TSMC28 or IBM32) for further portability of the projects design by this kit.

1.1. The Structure of Spice Model library

The Spice model library contains following devices, which are also listed in the table below. Addition of additional devices are anticipated.

1. Transistors
   a) 2.5V devices: Thick oxide mosfets
   b) 1.8V devices: Medium oxide mosfets
   c) Three type of 1.05V devices: Thin oxide mosfets
      - standard threshold voltage
      - high threshold voltage
      - low threshold voltage

   For each of these devices it is generated five corner models:
   TT - both mosfets typical,
   FF - both mosfets fast,
   SS - both mosfets slow,
   SF - slow_nmos/fast_pmos,
   FS - slow_pmos/fast_nmos.
2. Diode
3. Unsalicided N+ Poly Resistor
4. Bipolar junction transistor (BJT)

Table 1.1.The list of devices of spice model library

Device name	Model name
PMOS 1.05V standard VTH device	p105
NMOS 1.05V standard VTH device	n105
PMOS 1.05V high VTH device	p105_hvt
NMOS 1.05V high VTH device	n105_hvt
PMOS 1.05V low VTH device	p105_lvt
NMOS 1.05V low VTH device	n105_lvt
PMOS 2.5V device	p25
NMOS 2.5V device	n25
PMOS 1.8V device	p18
NMOS 1.8V device	n18
N+/Psub diode	nd/pd
Usalicided N+ poly resistor	rnpoly_wos
Usalicided P+ poly resistor	rppoly_wos
Salicided N+ poly resistor	rnpoly
Salicided P+ poly resistor	rppoly
HNPN 1.05V device	npn
VPNP 1.05V device	pnp

1.2. Transistors

1.2.1. 1.05V Thin Oxide MOSFETs

As this kit proposed to be used in the low power design and it is aimed to implement the advanced low power design techniques (e. g. multivoltage/multithreshold design digital libraries), the design kit also includes low voltage multi-threshold devices. The 1.05V standard threshold voltage devices are created using the Predictive Technology Model developed by Nanoscale Integration and Modeling (NIMO) Group (http://ptm.asu.edu/). It is taken the typical corner of 32nm process from Latest Models, suggested by NIMO. The high and low threshold devices are obtained by changing the threshold voltage of original (svt) devices by 20%. FF, SS, SF and FS corners are formed by changing the threshold voltage (vth0) and oxide thickness (tox) in the range of +/-5%.

Below it is presented the transfer curves of 1.05V NMOS and PMOS devices.

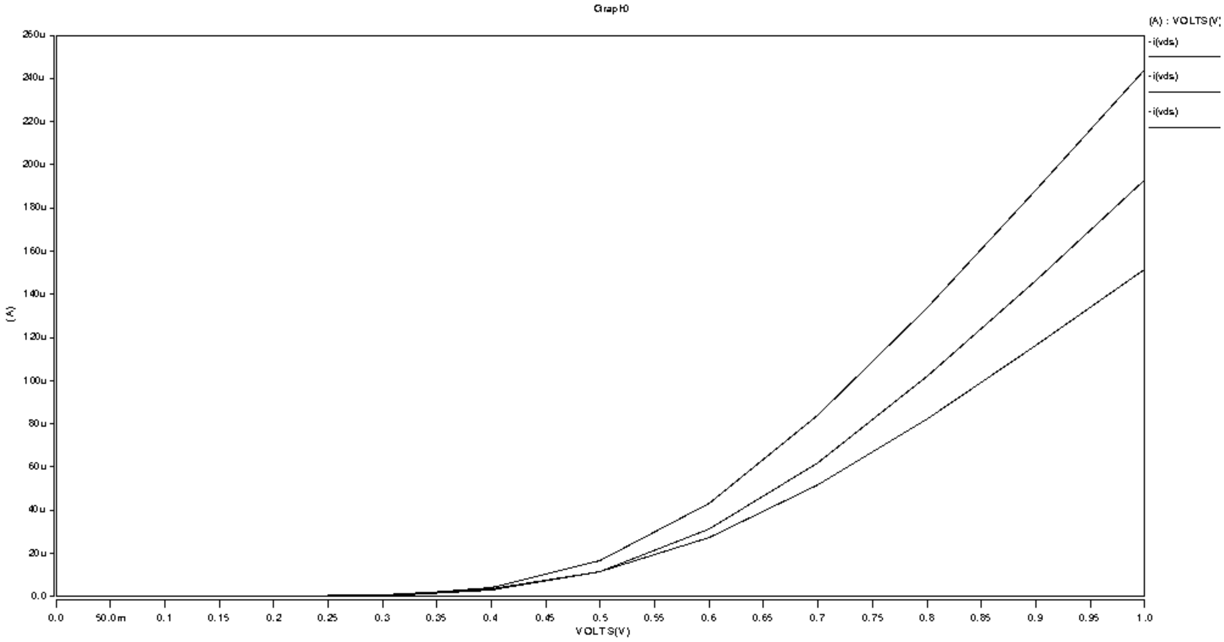

Figure 1.1. TT, FF and SS corners of 1.05V Thin oxide Standard Vth NMOS

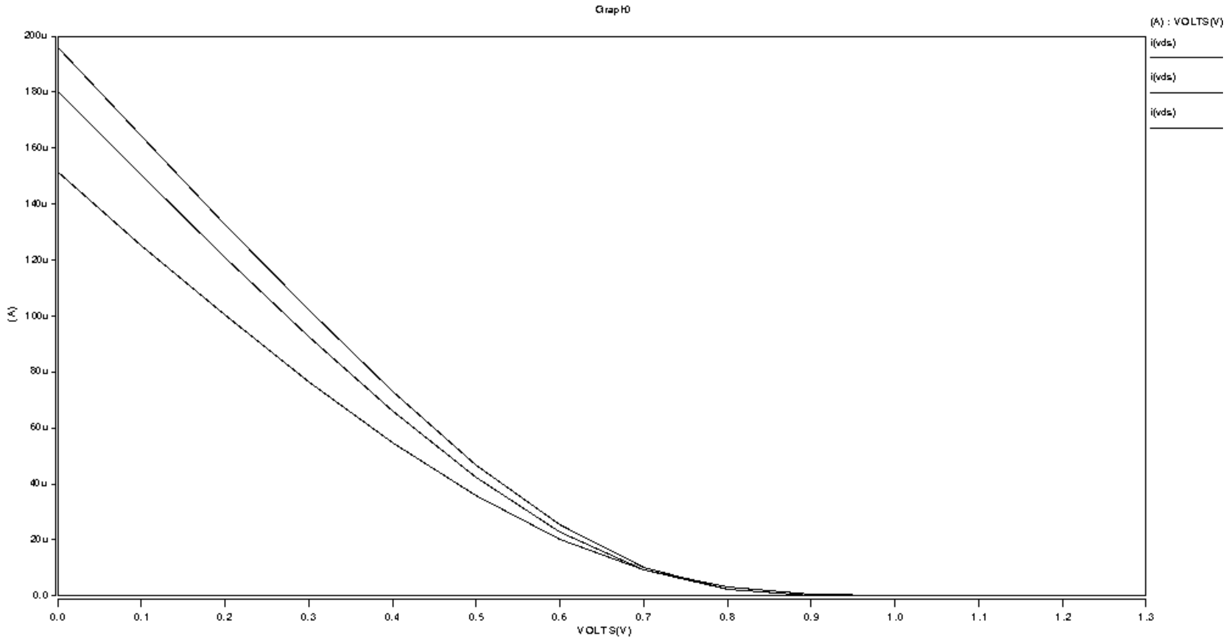

Figure 1.2. TT, FF and SS corners of 1.05V Thin oxide Standard Vth PMOS

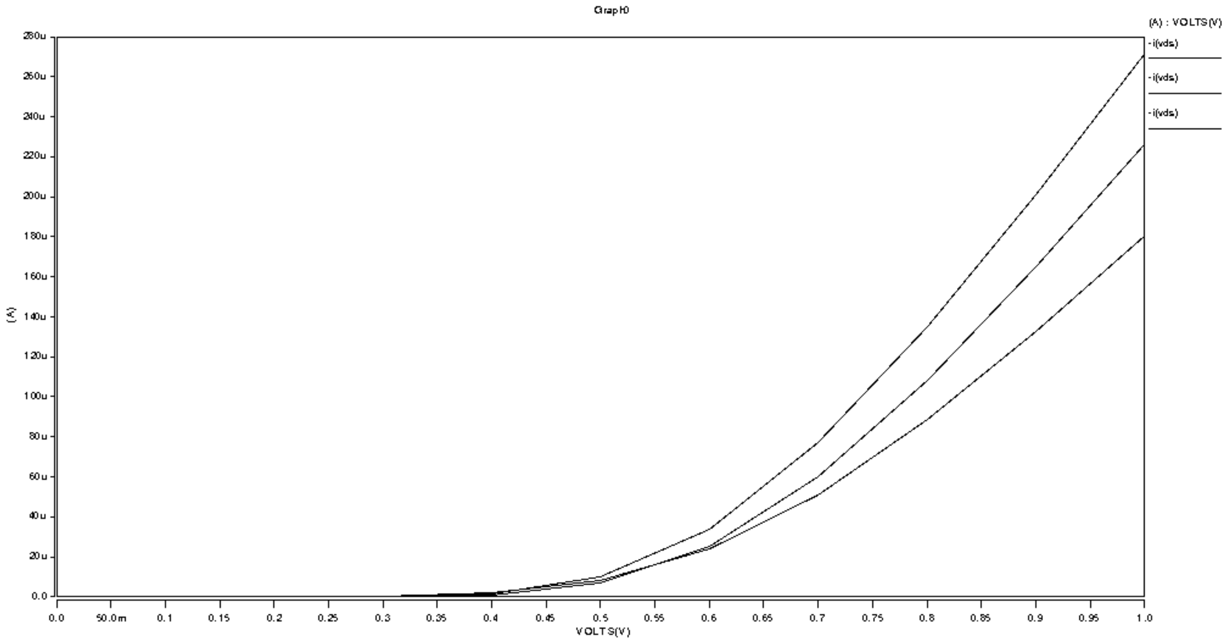

Figure 1.3. TT, FF and SS corners of 1.05V Thin oxide High Vth NMOS

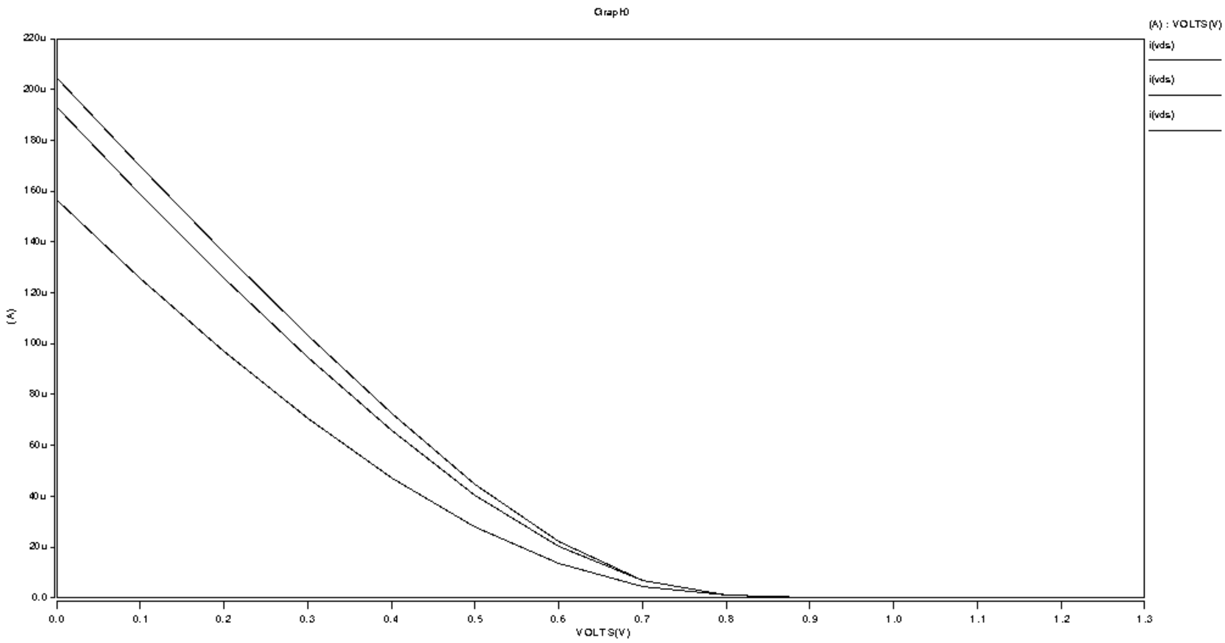

Figure 1.4. TT, FF and SS corners of 1.05V Thin oxide High Vth PMOS

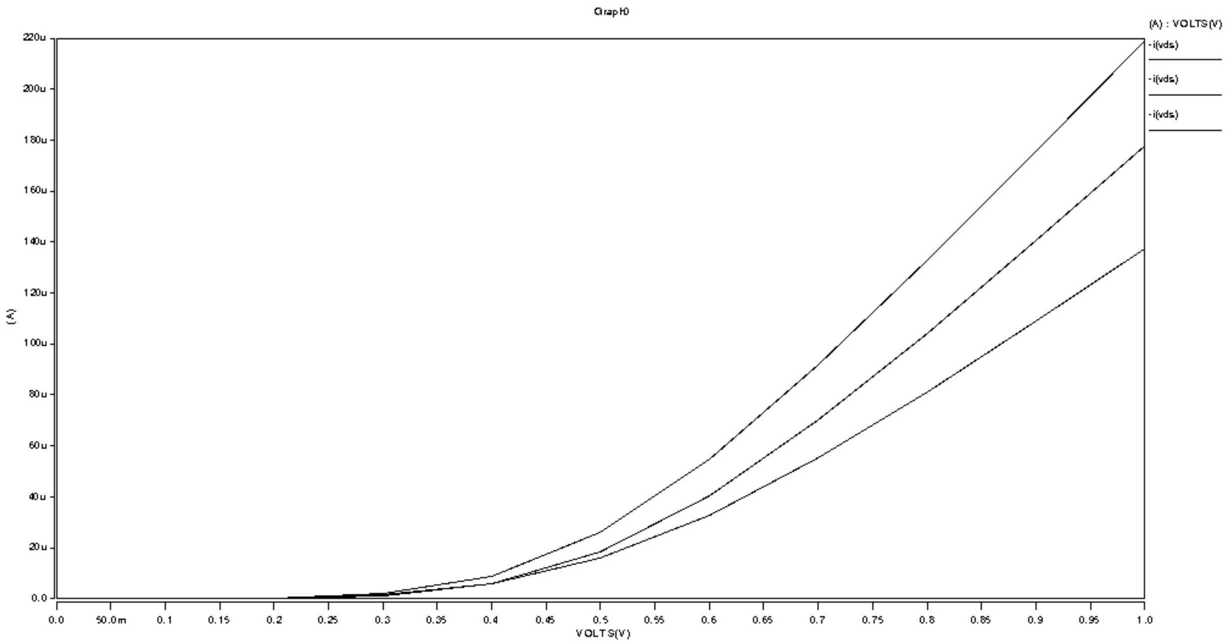

Figure 1.5. TT, FF and SS corners of 1.05V Thin oxide Low Vth NMOS

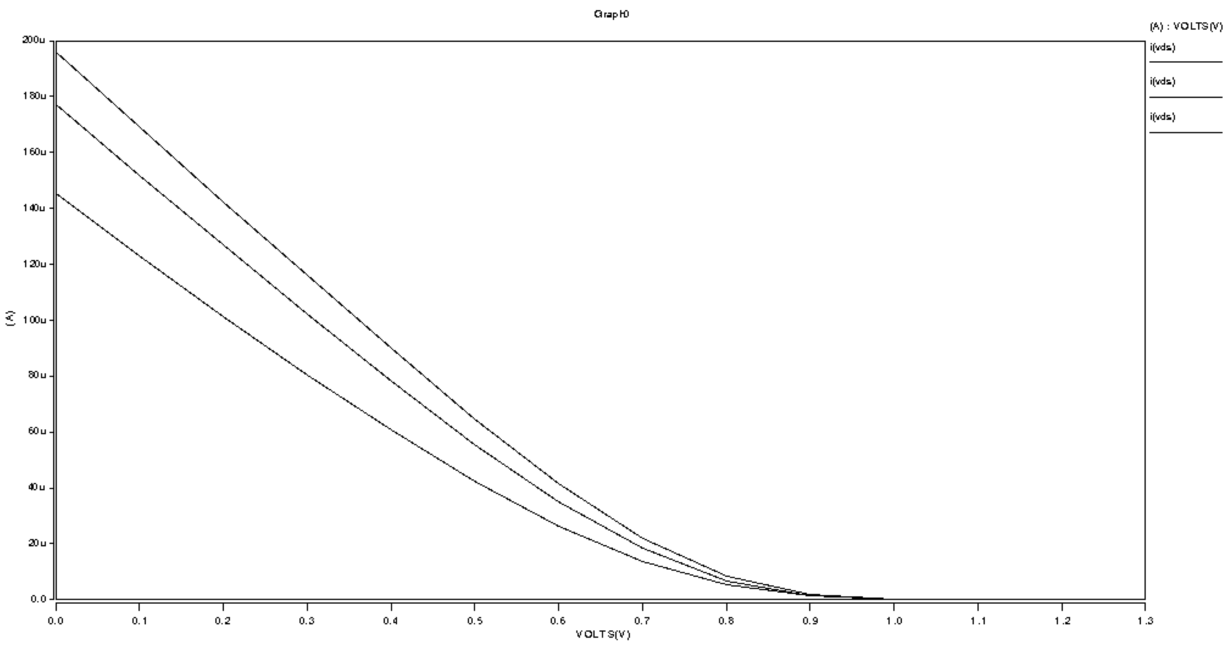

Figure 1.6. TT, FF and SS corners of 1.05V Thin oxide Low Vth PMOS

As the purpose of these 1.05V devices are mainly to reduce the power consumption of the design by using different vth transistors for particular applications. Table below represents cutoff currents for all types of 1.05V devices.

Table 1.2. Cutoff currents for standard and low Vth devices for TT, FF and SS corners. L/W=0.03u/0.3u

	FF, -40 (nA)	TT, 25 (nA)	SS, 125 (nA)
n105_hvt	0.07	0.12	0.61
p105_hvt	0.16	0.18	1.12
n105	0.34	0.49	2.69
p105	0.73	1.04	3.54
n105_lvt	1.19	2.3	11.23
p105_lvt	3.01	3.56	25.3

1.2.2. 1.8V Medium and 2.5V Thick Oxide MOSFETs

The 1.8V and 2.5V devices were created using the data obtained from Wafer Electrical Test Data and SPICE Model Parameters of SAED_EDK90nm which were scaled for SAED_EDK32/28nm.

Simulations were done for model parameters obtained from all lots given in MOSIS for SAED_EDK90nm and have been modified to match with the characteristics of 32/28nm devices known from open sources [1, 2, 3]. The bunch of DC transfer curves was obtained and the middle curve from the bunch was chosen as a typical corner for 1.8V devices, thereby being assured that it will be closer to the real process for further chip implementation.

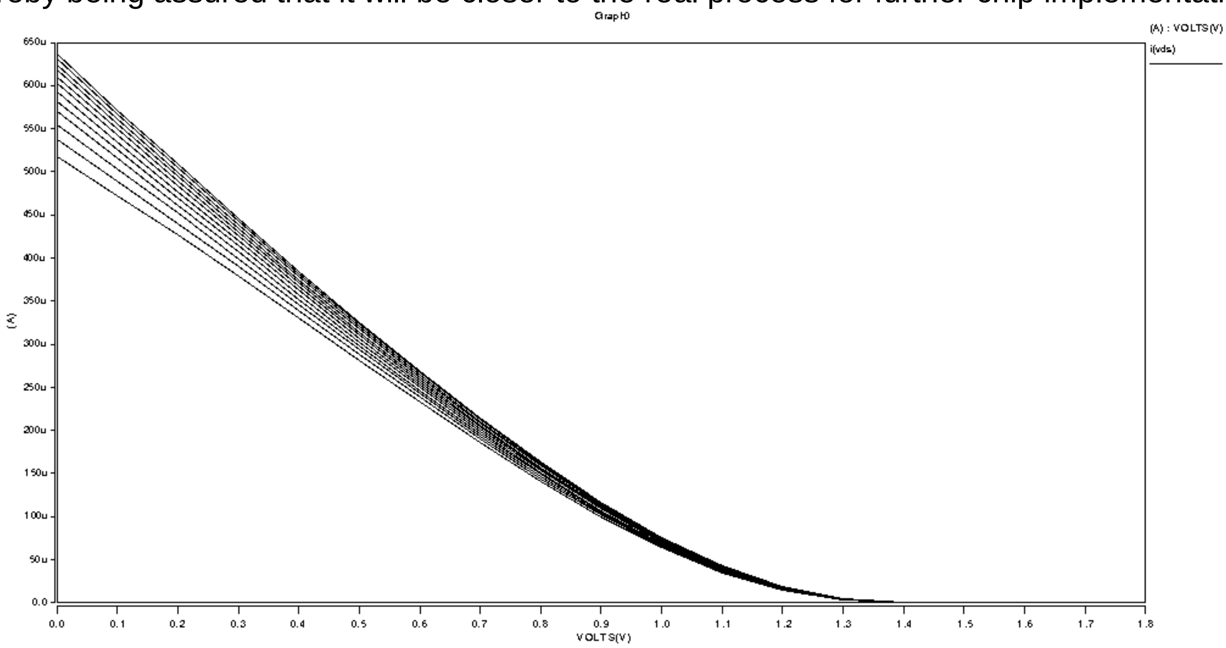

Figure 1.7. Bunch of transfer curves for PMOS models

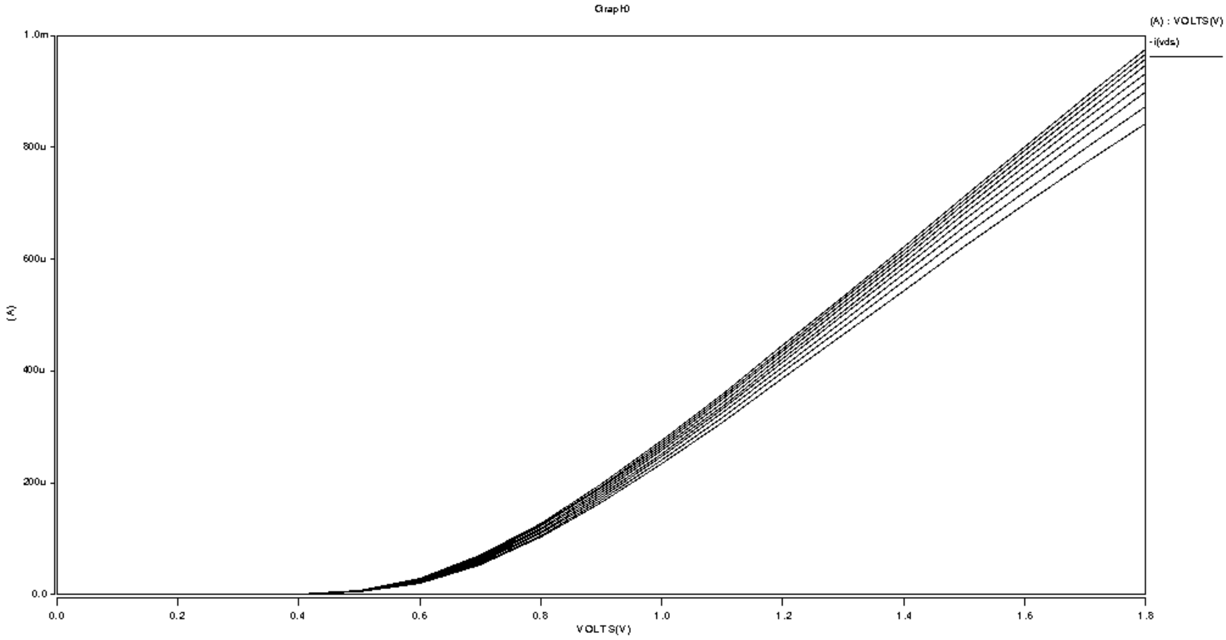

Figure 1.8. Bunch of transfer curves for NMOS models

FF, SS, SF and FS corners are formed by changing the threshold voltage (vth0) and oxide thickness (tox) in the range of +/-5%. Below it is presented the transfer curves of 1.8V PMOS and NMOS devices.

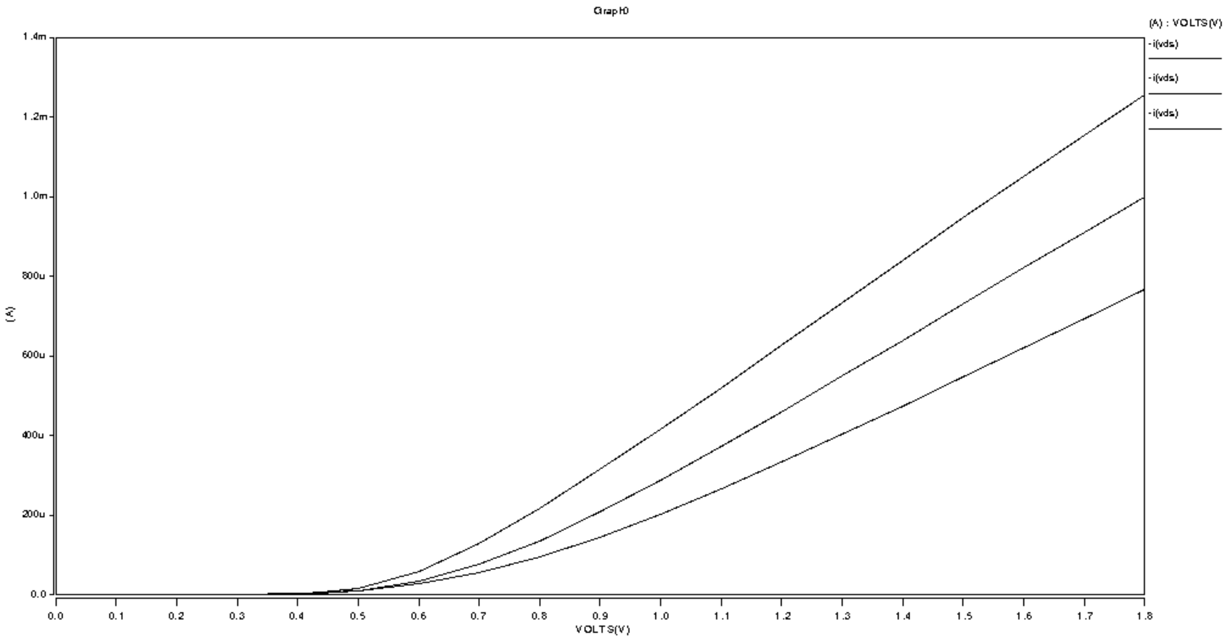

Figure 1.9. TT, FF and SS corners of 1.8V medium oxide NMOS

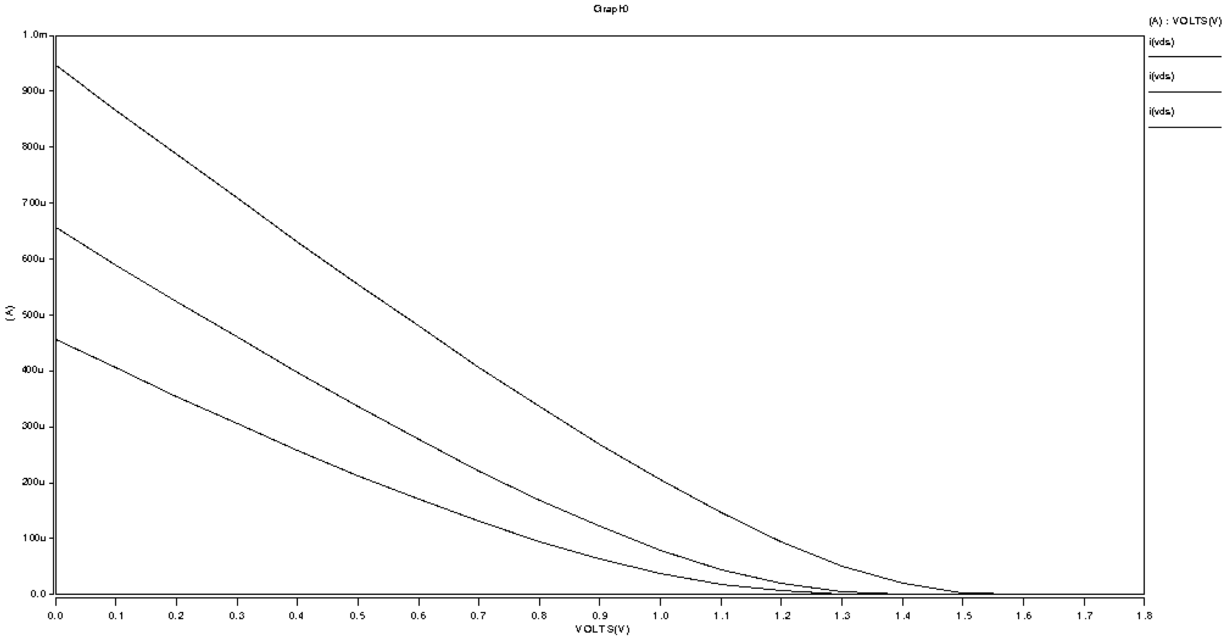

Figure 1.10. TT, FF and SS corners of 1.8V medium oxide PMOS

FF, SS, SF and FS corners are formed by changing the threshold voltage (vth0) and oxide thickness (tox) in the range of +/-5%. Below it is presented the transfer curves of 2.5V PMOS and NMOS devices.

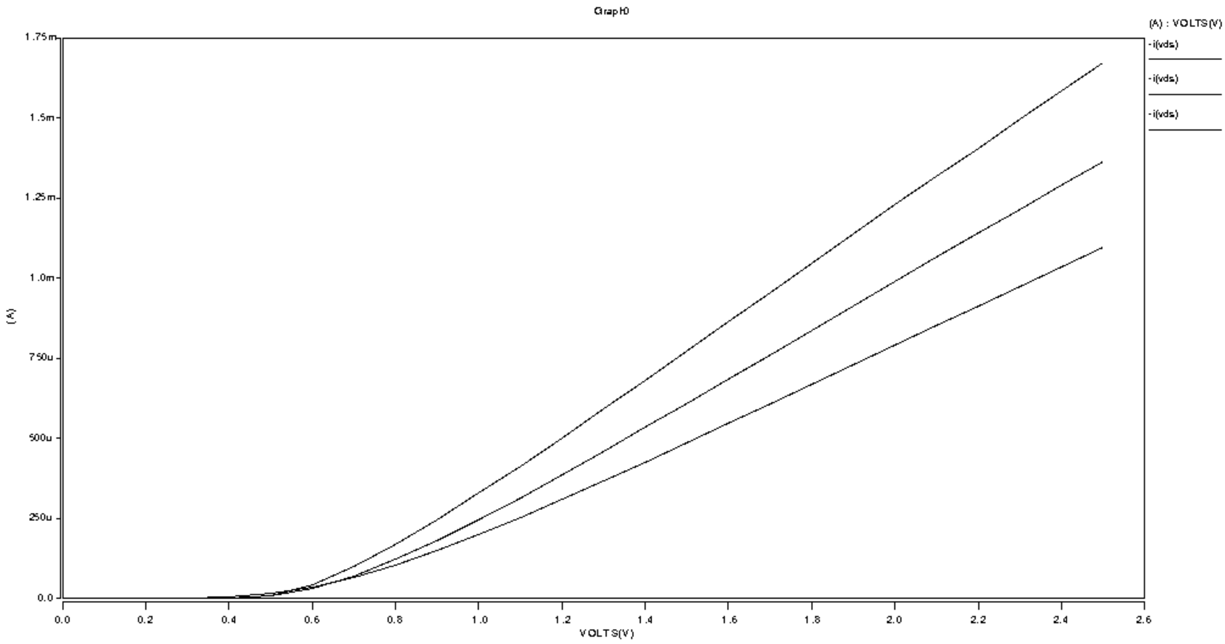

Figure 1.11. TT, FF and SS corners of 2.5V thick oxide NMOS

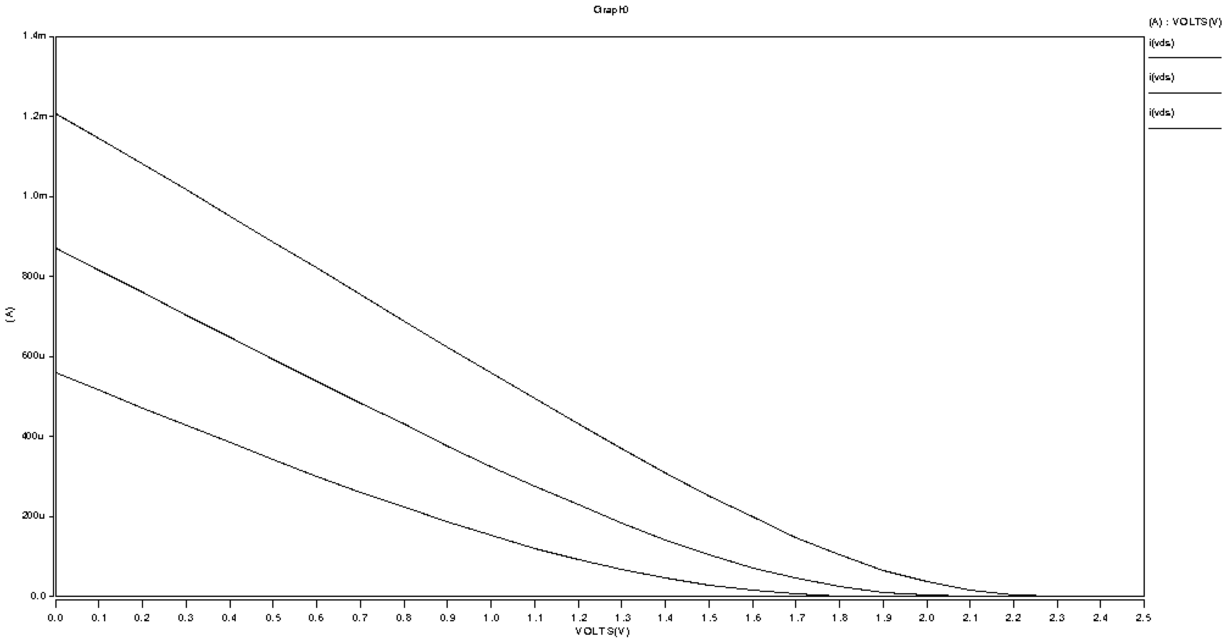

Figure 1.12. TT, FF and SS corners of 2.5V thick oxide PMOS

1.3. Resistor Model

It is created an unsalicided poly resistor model with a typical 620 Ohm sheet resistance. The salicided part of border resistances till the contacts are also considered in the model.

Resistor model corners are created by varying sheet resistance by 15%, temperature and voltage dependence parameters (TCR1, TCR2, VCR1 and VCR2). The values of all mentioned parameters are taken from [4].

Below the resistance dependence from temperature and applied voltage is presented. As it can be seen the simulated value of resistance is different from desired. This is due to the additional resistances on device endings, and its contribution to total resistance is inversely proportional to resistance width.

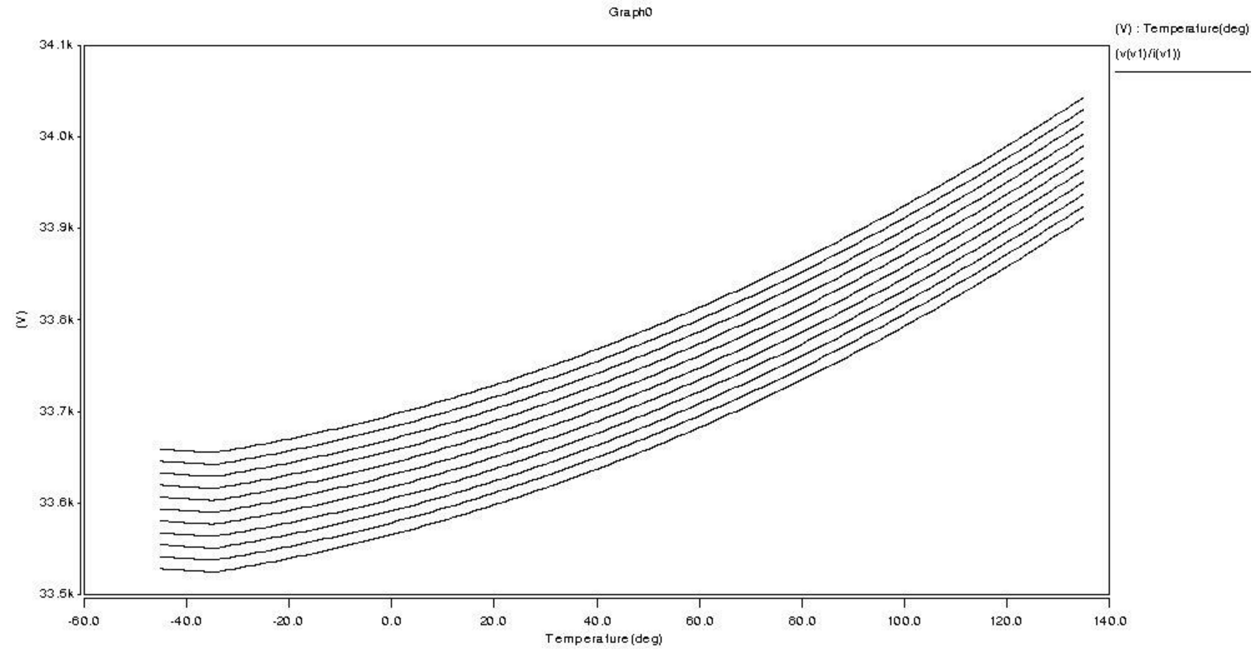

Figure 1.13. Resistance temperature dependence

1.4. Diode Model

The N+/Psub diode model is obtained from the HSPICE documentation. The I/V characteristics for diode different areas are shown in figure 1.14.

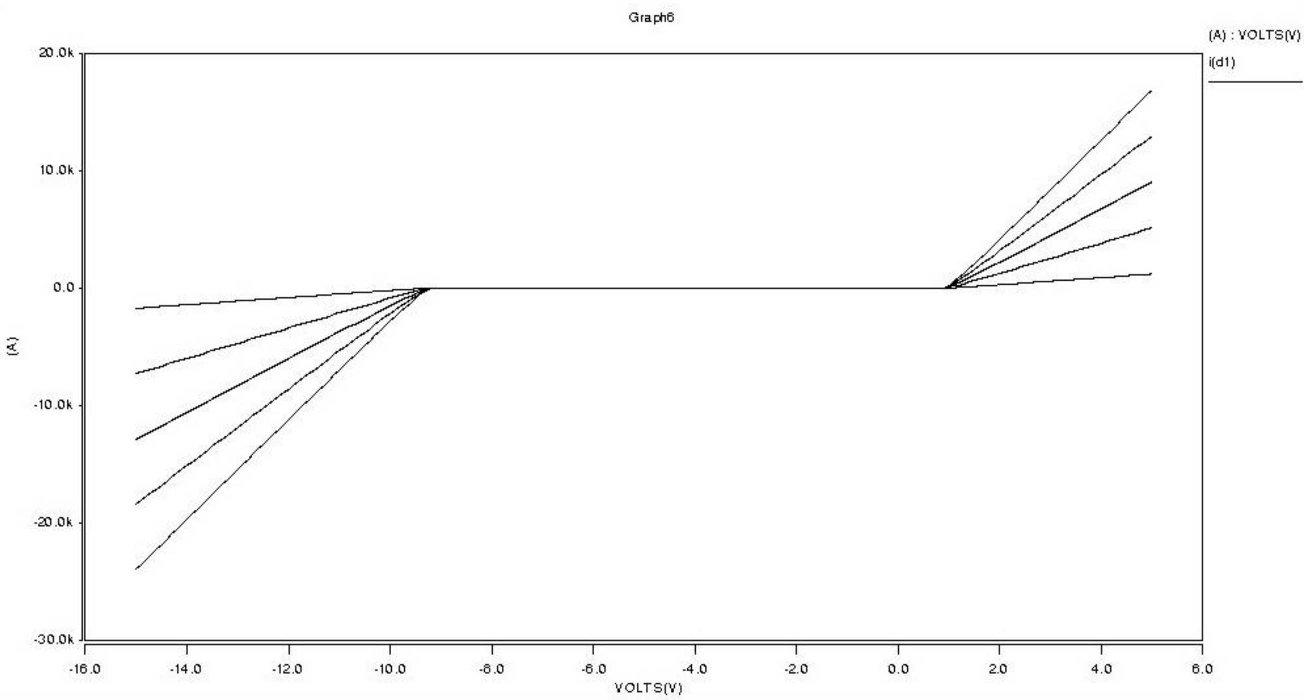

Figure 1.14. I/V characteristic is shown with different areas of diode

1.5. BJT Model

The BJT model is obtained from the HSPICE documentation. Below it is presented the transfer curves of 1.05V HNPN and VPNP devices.

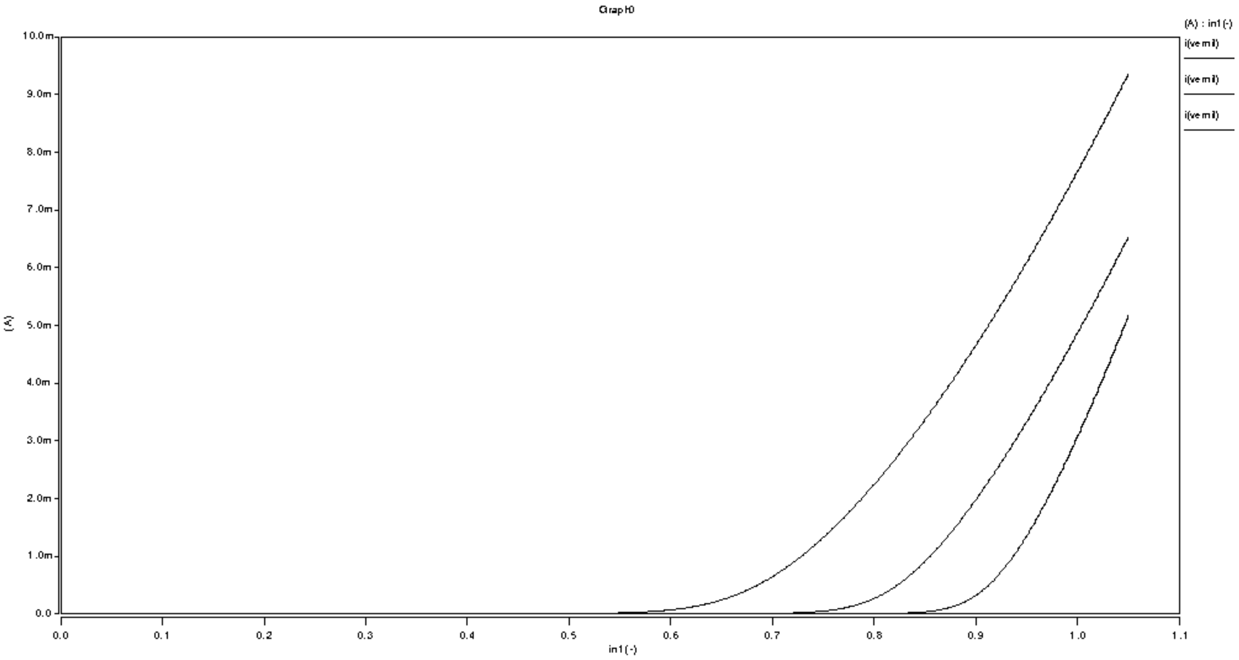

Figure 1.15. TT, FF and SS corners of 1.05V HNPN

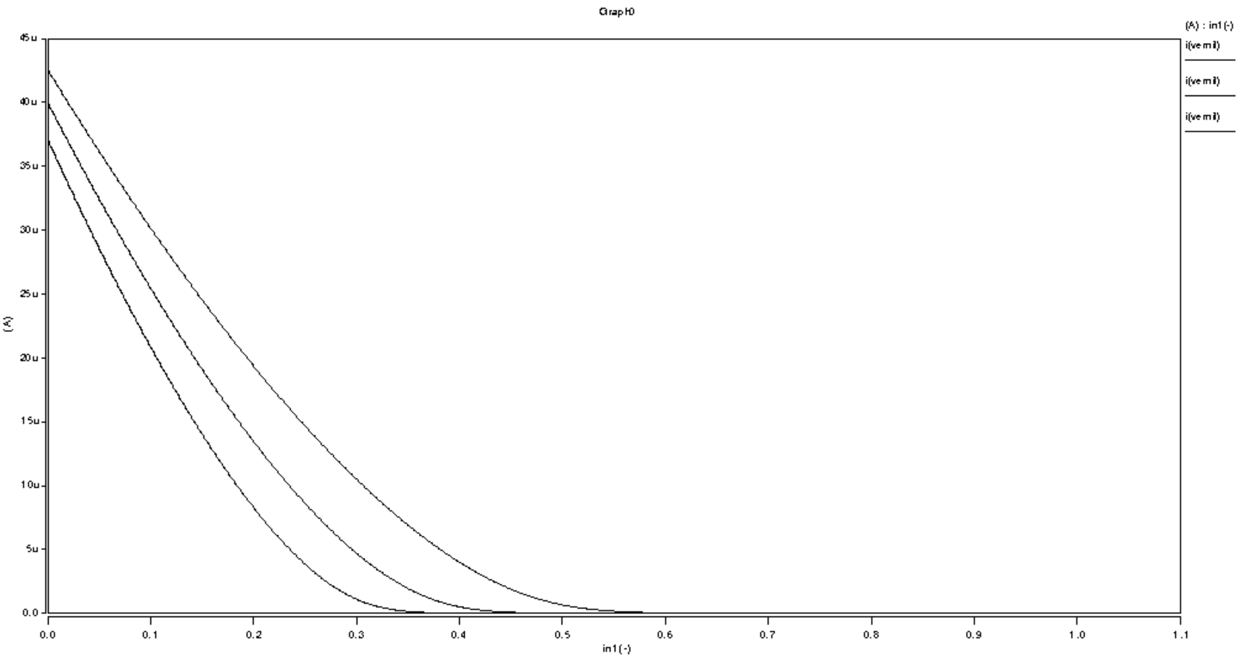

Figure 1.16. TT, FF and SS corners of 1.05V VPNP

1.6. Metal-on-Metal (MOM) Capacitor Model

The ccap MOM capacitor model is obtained from the HSPICE documentation and is available as model name “ccap” and device “Ccap”.

Model Usage

To do simulations using the suggested models, it is needed to:
call the model library using following template

```
*Spice netlist
.lib "../path_to_spice_model/SAED32nm.lib" CORNER_NAME
```

Table 1.3. SAED32/28nm model names

Device type	Device	Model name	Available corner names
Thin Oxide (1.05V) standard vth	NMOS	n105	TT, SS , FF. SF, FS
	PMOS	p105	
Thin Oxide (1.05V) low vth	NMOS	n105_lvt	TT_LVT, SS_LVT, FF_LVT, SF_LVT, FS_LVT
	PMOS	p105_lvt	
Thin Oxide (1.05V) high vth	NMOS	n105_hvt	TT_HVT, SS_HVT, FF_HVT, SF_HVT, FS_HVT
	PMOS	p105_hvt	
Medium Oxide (1.8V)	NMOS	n18	TT_18, SS_18 , FF_18, SF_18, FS_18
	PMOS	p18	
Thick Oxide (2.5V)	NMOS	n25	TT_25, SS_25 , FF_25, SF_25, FS_25
	PMOS	p25	
BJT (1.05 V)	HNPN	npn	TT_BIP, SS_BIP , FF_BIP
	VPNP	pnp	
N+ poly unsalicided/salicided	-	rnpoly_wos rppoly_wos rnpoly rppoly	res_t, res_l, res_h
diode is N+/Psub	-	nd/pd	ND ,PD
MOM Capacitor	CCap	Ccap	TT, SS , FF. SF, FS

2. References

1 P. Packan et al., “High Performance 32nm Logic Technology Featuring 2nd Generation High-k + Metal Gate Transistors”, IEEE International Technical Digest Electron Devices Meeting (IEDM), pp659-662, 2009

2 C. H. Diaz et al., “32 nm gate-first high-k/metal-gate technology for high performance low power applications”, in Proc. IEEE IEDM Tech. Dig., San Francisco, USA, 2008, pp. 629–632.

3 F. Arnaud et al., "32nm General Purpose Bulk CMOS Technology for High Performance Applications at Low Voltage," IEDM Tech. Dig., pp. 633-636, 2008.

4 R.J. Baker, Hary W.Li, David E. Boyce. “CMOS: Circuit Design, Layout, and Simulation.”, 2010

3. Revision History

Table 3.1. Revision History

Revision	Date	Change
A.1	28/12/2010	Initial release
A.1.5	27/04/2016	Added MOM Capacitor