SAED 32/28nm
INTEROPERABLE PROCESS DESIGN KIT

SAED_iPDK32/28

SPECIFICATION

Document #: SAED_iPDK32/28
Revision : 1.5
Technology : SAED32/28nm
Process : SAED32/28nm 1P9M 1.05v/1.8v/2.5v

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1. Introduction

1.1. Goal of PDK development

This document describes possibilities, peculiarities of SAED_iPDK32/28 Process Design Kit and technical parameters of Symbol library and OA Python PCells included in it. SAED_iPDK32/28 is free from intellectual property restrictions and is oriented at Synopsys Custom Designer (CD) tool.
SAED_iPDK32/28 is anticipated for the use of educational purposes and is aimed at training highly qualified specialists in microelectronics at:

- Synopsys Customer Education Services
- Synopsys Global Technical Services
- Universities included in Synopsys University Program

SAED_iPDK32/28 is foreseen to support the trainees to better master:

- Advanced Analog Design Methodologies
- Capabilities of SYNOPSYS Custom Designer and other EDA tools

For the use of PDK it is assumed that European or North American bundle of SYNOPSYS EDA tools, including CD is available to trainees.

SAED_iPDK32/28 Process Design Kit is anticipated for designing different analog/mixed-signal integrated circuits (ICs) or IPs by the application of 32/28nm technology and SYNOPSYS EDA tools.

1.2. Content of PDK

The content of SAED_iPDK32/28 is shown in Table 1.1.

Table 1.1 Content of SAED_iPDK32/28

Description	Directory	Extension(s)
Technology files	./SAED_iPDK32.28/techfiles/	.tcl, .drf, .tf, .map
Physical verification files	./SAED_iPDK32.28/hercules/	*.ev, *.rs
Parasitic Extraction files	./SAED_iPDK32.28/starrcxt/	.nxtgrd, .itf, .map
Symbol library and OA Python PCells	./SAED_iPDK32.28/SAED_iPDK_32/	(OpenAccess database)
HSpice models	./SAED_iPDK32.28/HSpice/	.lib
Documentation	./SAED_iPDK32.28/documentation/	.pdf
Setup files	./SAED_iPDK32.28/	.tcl

1.3. Methodology of getting PDK components

For design of SAED32/28nm Process Design Kit, abstract technology and simulation models were generated using the Predictive Technology Model (PTM) developed by the Nanoscale Integration and Modeling Group (NIMO) of Arizona State University (ASU) (http://ptm.asu.edu/).

Layout design rules for SAED32/28nm educational, abstract technology are obtained by scaling SAED 90nm design rules and using the latest known set of free, vendor-independent, scalable design rules of MOSIS (http://mosis.com/Technical/Design rules/scmos/scmos-main) by scaling them for 32nm technology. Parasitic extraction deck is formed using the models of parasitics estimation developed by NIMO group of ASU. Also 32/28nm advanced rules supported by Synopsys IC Compiler Zroute router were added.

Process Design Kit SAED_iPDK32/28 is build to support key processes as IBM 32nm and TSMC 28nm.

SAED_iPDK32/28 Technology files were generated according to SAED32/28nm 1P9M 1.05v/1.8v/2.5v technology [1] and OpenAccess [2] format specification.

2. SAED_iPDK32/28 Components

SAED_iPDK32/28 contains technology files, physical verification runsets, parasitic extraction files, PCells and symbol library directories.

2.1. Technology files

Technology files include technology, display resource files and layer map files.

2.1.1. Technology file

Technology file contains layer information and design rule definition. It is used for library creation.

2.1.2. Display resources

Contains color, fill and stipple patterns for all the packets used in the technology file in CD format.

2.1.3. Layer map file

Maps layer names with the layer purposes, numbers, data type and stipple patterns used to describe the layout in the layout editor, DRC, LVS and parasitic extraction tools.

2.2. Physical verification files

Physical verification files include Hercules and IC Validator DRC and LVS runset files. DRC Runset file is a command file used by the DRC software program that analyzes the data in the layout and checks design rule violations. LVS runset is a command file used by the LVS software program that extracts the intended devices and their parameters to compare with schematic netlists.

2.3. Parasitic extraction files

Parasitic extract files are used by the parasitic extraction software program that extracts parasitic capacitance, resistance and/or inductance from circuit layout. Parasitic extraction files are given in StarRC format.

- The Interconnect Technology Format (*.itf) is a file which contains specification of each layer's content.
- *.nxtgrd is a database containing capacitance, resistance, inductance and layer information which can be encrypted.
- *.map file maps the devices extracted by StarRC with the interoperable PCells to be used for each device in the StarRC view produced after running StarRC.

2.4. Design environment setup files

SAED_iPDK32/28 Process Design Kit contains scripts for environment setup which assure correct operation of all the components.

3. Supported devices

3.1. MOSFETs

SAED_iPDK32/28 contains MOSFETs which have 3 or 4 terminals. Length and width are given in nanometers, areas are given in square nanometers and perimeters are given in nanometers. Design variables are anticipated for length and width entries. The parameters of area for diffusion are calculated from the width and the number of used fingers. The width per finger is calculated by dividing the width by the number of fingers. This parameter is viewed by the designer.

Table 3.1 MOS list

Symbol Name	Spice model name	Type	Terminals	Voltage (V)
nmos3t	n105	nmos	3 (D G S)	1.05
nmos3t_18	n18	nmos	3 (D G S)	1.8
nmos3t_25	n25	nmos	3 (D G S)	2.5
nmos4t	n105	nmos	4 (D G S B)	1.05
nmos4t_18	n18	nmos	4 (D G S B)	1.8
nmos4t_25	n25	nmos	4 (D G S B)	2.5
nmos4t_hvt	??????????????	nmos 4 (high Vth)	4 (D G S B)	????
nmos4t_lvt	??????????????	nmos 4 (low Vth)	4 (D G S B)	????
pmos3t	n105	pmos	3 (D G S)	1.05
pmos3t_18	n18	pmos	3 (D G S)	1.8
pmos3t_25	n25	pmos	3 (D G S)	2.5
pmos4t	n105	pmos	4 (D G S B)	1.05
pmos4t_18	n18	pmos	4 (D G S B)	1.8
pmos4t_25	n25	pmos	4 (D G S B)	2.5
pmos4t_hvt	??????????????	pmos (high Vth)	4 (D G S B)	????
pmos4t_lvt	??????????????	pmos (low Vth)	4 (D G S B)	????

Table 3.2 MOS PCell parameters

Parameters	Description
model	HSpice model
lvs_model	LVS model
w	Width of each finger
wtot	Total width of MOSFET transistors
l	Length of each finger
entryMode	Gate width divided total width
nf	Number of fingers of gate
m	Multiplicity factor to place number of parallel devices
diffLeftStyle	Left diffusion contact style, for abutment, dummies, etc.
diffRightStyle	Right diffusion contact style, for abutment, dummies, etc.
diffContactOffsets	Diffusion contact position
gateOffsets	Gate contact position

gateContact	Gate Contact
cgSpacingAdd	Additional contact-to-gate spacing
leftDiffAdd	Additional left diffusion extension beyond contact
rightDiffAdd	Additional right diffusion extension beyond contact
guardRing	Specify sides of integrated guard ring
ruleset	Design For Manufacturing Rules

3.2. Resistors

The resistors in the library consist of different poly resistors, which have 2 terminals. All parameters entered into the resistor must be integers or floating-point numbers. No design variables are supported due to calculations that must be performed on the entries. The width and length are snapped to grid, and the resistances are recalculated and updated on the component form based on actual dimensions.

Table 3.3 Resistor list

Symbol name	Description
rnpoly_wos	N+ poly unsalicided 2 terminal (A B) resistor
rppoly_wos	P+ poly unsalicided 2 terminal (A B) resistor
Rnpoly	N+ poly salicided 2 terminal (A B) resistor
Rppoly	P+ poly salicided 2 terminal (A B) resistor

Table 3.4 Resistor PCell parameters

Spice Model	HSpice model name
lvs_model	LVS model
model	HSpice model
r	Resistance
wf	Resistor width
l	Resistor length
lf	Resistor length per finger
entryMode	width (r & w) mode or length and width (l & w) mode and length(r & l) mode
m	Multiplicity factor to place number of parallel devices
fr	Fingers per row
rw	Rows
lcontact	Contact length
wbar	Width of bars
connect	Whether fingers are connected in series or parallel
dummies	Whether dummy fingers are included
deviceType	The type of resistor, used in PCells
ruleset	Design For Manufacturing Rules

3.3. Diodes

The diodes in the PDK library consist of two types which have 2 terminals.

Table 3.5 Diode Spice models list

Symbol name	Description
Nd	N+ 2 terminal (PLUS MINUS) diode
Pd	P+ 2 terminal (PLUS MINUS) diode

Table 3.6 Diode PCell parameters

Parameters	Description
model	HSpice model
lvs_model	LVS model
L	Length of diode
W	Width of diode
Area	Area of the diode
ruleset	Design For Manufacturing Rules
dioType	The type of diode, used in PCells

3.4. BJTs

This PDK contains vertical pnp (vpnp) and horizontal npn (hnpn) transistors. The device has fixed dimensions for its emitter size. This device is typical of a CMOS process. The emitter width for schematic entry is specified in nanometers. All parameters entered into the npn and pnp must be integers or floating point numbers.

Table 3.7 BJT Spice models list

Symbol name	Description
hnpn	3 terminal (C B E) vertical BJT 1.05 volt
vpnp	3 terminal (C B E) vertical BJT 1.05 volt

Table 3.8 BJT PCell parameters

Parameters	Description
model	HSpice model
lvs_model	LVS model
area	Area of the diode
emitterSize	The sizes of BJT will be 2x2, 5x5
m	Multiplicity factor to place number of parallel devices
ruleset	Design For Manufacturing Rules

4. Device Description

4.1. NMOS Transistor

4.1.1. nmos3t, nmos3t_18, nmos3t_25

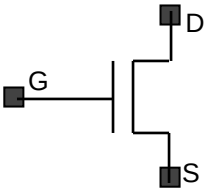

Figure 4.1. Symbol of nmos3t transistor

Table 4.1 nmos3t HSPICE models

Symbol name	Netlist
nmos3t	`m1 D G S gnd! n105 w='0.1u' l='0.03u' m=1`
nmos3t_18	`m1 D G S gnd! n18 w='0.16u' l='0.15u' m=1`
nmos3t_25	`m1 D G S gnd! n25 w='0.36u' l='0.26u' m=1`

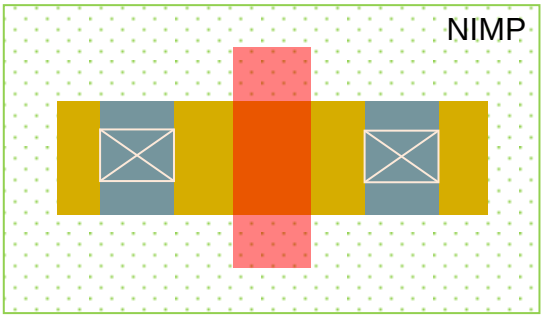

Figure 4.2. Layout of nmos3t transistor

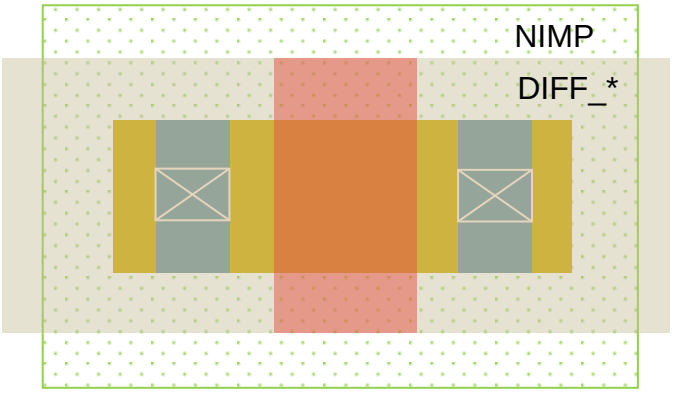

Figure 4.3. Layout of nmos4t_18 nmos4t_25 transistor

Table 4.2 nmos3t Device Layers

Device Layers	Layer Color and Fill
DIFF	
NIMP	
PO	
CO	
M1	
DIFF_* (DIFF_18, DIFF_25)	

Table 4.3 nmos3t Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND NIMP CONTAINS PO
G	PO
D	DIFF AND NIMP NOT PO
S	DIFF AND NIMP NOT PO
B	Substrate

Table 4.4 nmos3t LVS Checking

Parameter Calculation	
Length	PO intersecting DIFF
Width	PO inside DIFF

4.1.2. nmos4t, nmos4t_18, nmos4t_25

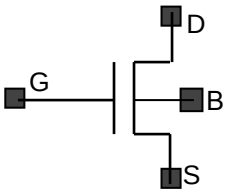

Figure 4.4. Symbol of nmos4t transistor

Table 4.5 nmos4t Spice model

Symbol name	Netlist
nmos4t	`m1 net1 net3 net2 gnd! n105 w='0.1u' l='0.03u' m=1`
nmos4t_18	`m1 net1 net3 net2 gnd! n18 w='0.16u' l='0.15u' m=1`
nmos4t_25	`m1 net1 net3 net2 gnd! n25 w='0.36u' l='0.26u' m=1`

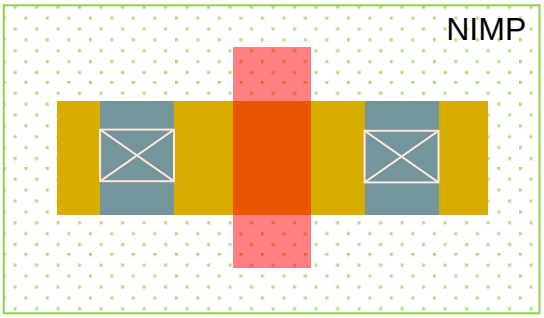

Figure 4.5. Layout of nmos4t transistor

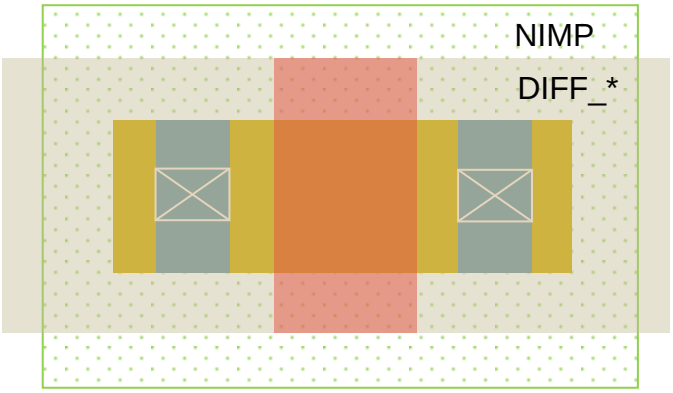

Figure 4.6. Layout of nmos4t_18 nmos4t_25 transistor

Table 4.6 nmos4t Device Layers

Device Layers	Layer Color and Fill
DIFF	
NIMP	
PO	
CO	
M1	
DIFF_* (DIFF_18, DIFF_25)	

Table 4.7 nmos4t Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND NIMP CONTAINS PO
G	PO
D	DIFF AND NIMP NOT PO
S	DIFF AND NIMP NOT PO
B	Substrate

Table 4.8 nmos4t LVS Checking

Parameter Calculation	
Length	PO intersecting DIFF
Width	PO inside DIFF

4.1.3. nmos4t_hvt

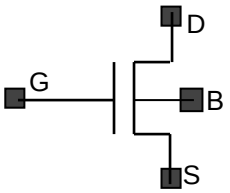

Figure 4.7. Symbol of nmos4t_hvt transistor

Table 4.9 nmos4t_hvt Spice model

Symbol name	Netlist
nmos4t_hvt	`m2 net1 net3 net2 gnd! n105_hvt w='0.1u' l='0.03u' m=1`

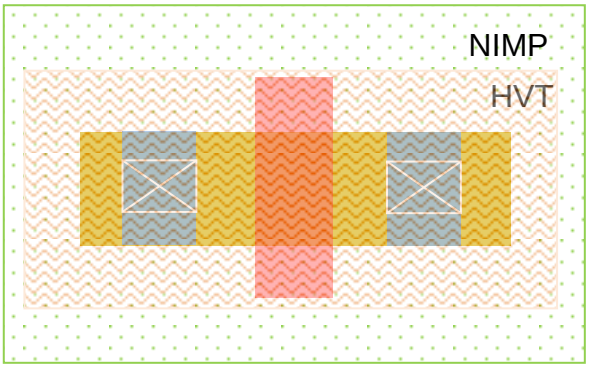

Figure 4.8. Layout of nmos4t_hvt transistor

Table 4.10 nmos4t_hvt Device Layers

Device Layers	Layer Color and Fill
DIFF	
NIMP	
PO	
CO	
M1	
HVTIMP	

Table 4.11 nmos4t_hvt Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND NIMP AND HVTIMP CONTAINS PO
G	PO
D	DIFF AND NIMP AND HVTIMP NOT PO
S	DIFF AND NIMP AND HVTIMP NOT PO
B	Substrate

Table 4.12 nmos4t_hvt LVS Checking

Parameter Calculation	
Length	PO intersecting DIFF
Width	PO inside DIFF

4.1.4. nmos4t_lvt

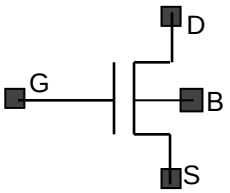

Figure 4.9. Symbol of nmos4t_lvt transistor

Table 4.13 nmos4t_lvt Spice model

Symbol name	Netlist
nmos4t_lvt	`m2 net1 net3 net2 gnd! n105_lvt w='0.1u' l='0.03u' m=1`

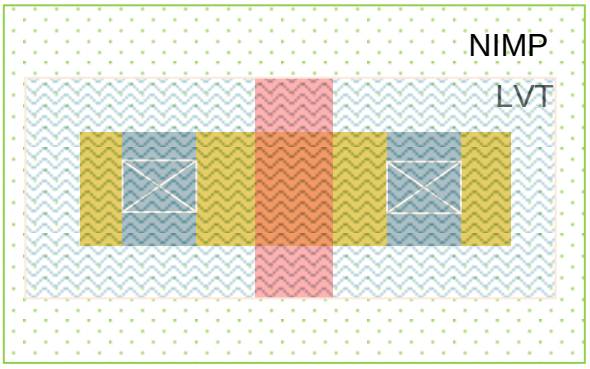

Figure 4.10. Layout of nmos4t_lvt transistor

Table 4.14 nmos4t_lvt Device Layers

Device Layers	Layer Color and Fill
DIFF	
NIMP	
PO	
CO	
M1	
LVTIMP	

Table 4.15 nmos4t_lvt Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND NIMP AND LVTIMP CONTAINS PO
G	PO
D	DIFF AND NIMP AND LVTIMP NOT PO
S	DIFF AND NIMP AND LVTIMP NOT PO
B	Substrate

Table 4.16 nmos4t_lvt LVS Checking

Parameter Calculation	
Length	PO intersecting DIFF
Width	PO inside DIFF

4.2. PMOS Transistor

4.2.1. pmos3t, pmos3t_18, pmos3t_25

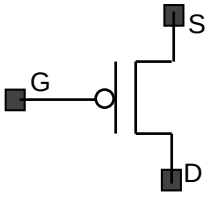

Figure 4.11. Symbol of pmos3t transistor

Table 4.17 pmos3t Spice model

Symbol name	Netlist
pmos3t	`m5 net1 net3 net2 gnd! p105 w='0.1u' l='0.03u' m=1`
pmos3t_18	`m5 net1 net3 net2 gnd! p18 w='0.16u' l='0.15u' m=1`
pmos3t_25	`m5 net1 net3 net2 gnd! p25 w='0.36u' l='0.26u' m=1`

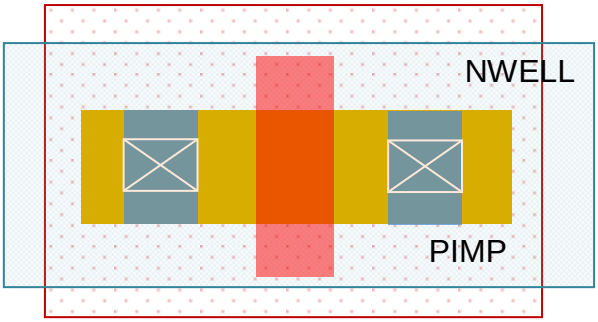

Figure 4.12. Layout of pmos3t transistor

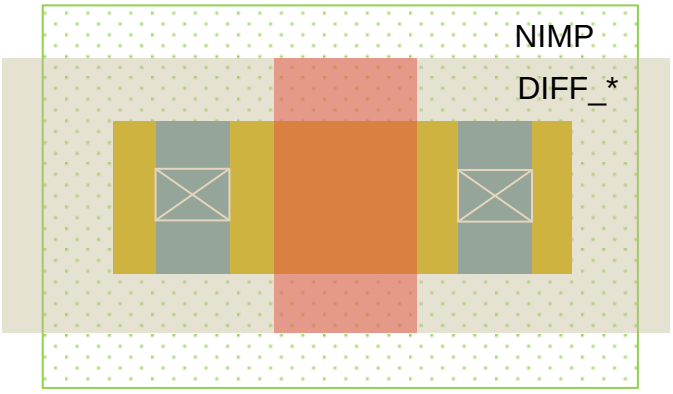

Figure 4.13. Layout of pmos3t_18 pmos3t_25 transistor

Table 4.18 pmos3t Device Layers

Device Layers	Layer Color and Fill
DIFF	
PIMP	
PO	
CO	
M1	
NWELL	
DIFF_* (DIFF_18, DIFF_25)	

Table 4.19 pmos3t Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND PIMP AND NWELL CONTAINS PO
G	PO
D	DIFF AND PIMP AND NWELL NOT PO
S	DIFF AND PIMP AND NWELL NOT PO
B	Substrate

Table 4.20 pmos3t LVS Checking

Parameter Calculation	
Length	PO intersecting DIFF
Width	PO inside DIFF

4.2.2. pmos4t, pmos4t_18, pmos4_25

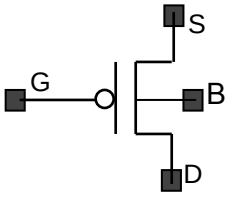

Figure 4.14. Symbol of pmos4t transistor

Table 4.21 pmos4t Spice model

Symbol name	Netlist
pmos4t	`m5 net1 net3 net2 gnd! p105 w='0.1u' l='0.03u' m=1`
pmos4t_18	`m5 net1 net3 net2 gnd! p18 w='0.16u' l='0.15u' m=1`
pmos4t_25	`m5 net1 net3 net2 gnd! p25 w='0.36u' l='0.26u' m=1`

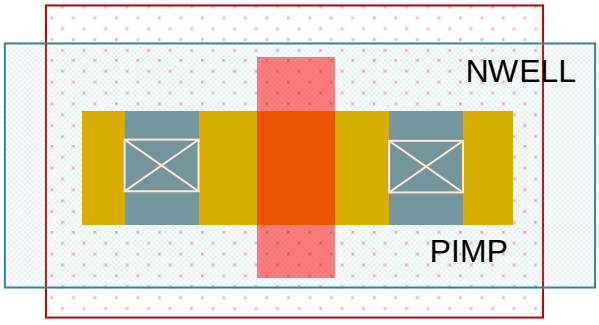

Figure 4.15. Layout of pmos4t transistor

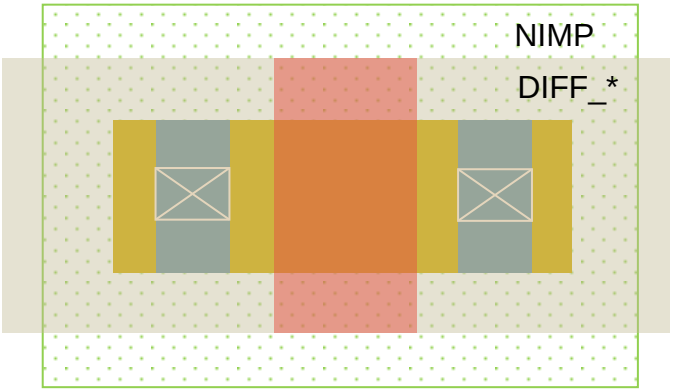

Figure 4.16. Layout of pmos4t_18 pmos4t_25 transistor

Table 4.22 pmos4t Device Layers

Device Layers	Layer Color and Fill
DIFF	
PIMP	
PO	
CO	
M1	
NWELL	
DIFF_* (DIFF_18, DIFF_25)	

Table 4.23 pmos4t Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND PIMP AND NWELL CONTAINS PO
G	PO
D	DIFF AND PIMP AND NWELL NOT PO
S	DIFF AND PIMP AND NWELL NOT PO
B	Substrate

Table 4.24 pmos4t LVS Checking

Parameter Calculation	
Length	PO intersecting DIFF
Width	PO inside DIFF

4.2.3. pmos4t_hvt

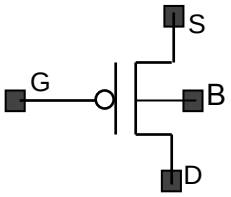

Figure 4.17. Symbol of pmos4t_hvt transistor

Table 4.25 pmos4t_hvt Spice model

Symbol name	Netlist
pmos4t_hvt	`m5 net1 net3 net2 gnd! p105_hvt w='0.1u' l='0.03u' m=1`

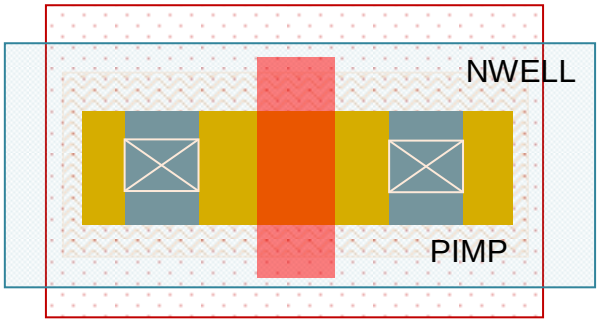

Figure 4.18. Layout of pmos4t_hvt transistor

Table 4.26 pmos4t_hvt Device Layers

Device Layers	Layer Color and Fill
DIFF	
PIMP	
PO	
CO	
M1	
HVTIMP	
NWELL	

Table 4.27 pmos4t_hvt Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND PIMP AND NWELL AND HVTIMP CONTAINS PO
G	PO
D	DIFF AND PIMP AND HVTIMP AND NWELL NOT PO
S	DIFF AND PIMP AND HVTIMP AND NWELL NOT PO
B	Substrate

Table 4.28 pmos4t_hvt LVS Checking

Parameter Calculation	
Length	PO intersecting DIFF
Width	PO inside DIFF

4.2.4. pmos4t_lvt

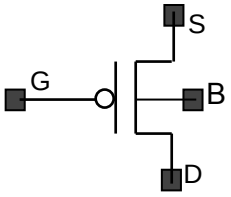

Figure 4.19. Symbol of pmos4t_lvt transistor

Table 4.29 pmos4t_lvt Spice model

Symbol name	Netlist
pmos4t_lvt	`m5 net1 net3 net2 gnd! p105_lvt w='0.1u' l='0.03u' m=1`

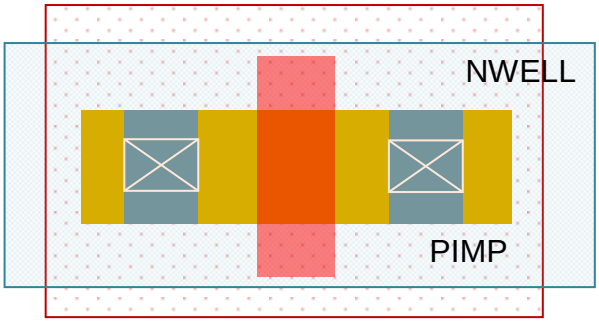

Figure 4.20. Layout of pmos4t_lvt transistor

Table 4.30 pmos4t_lvt Device Layers

Device Layers	Layer Color and Fill
DIFF	
PIMP	
PO	
CO	
M1	
LVTIMP	
NWELL	

Table 4.31 pmos4t_lvt Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND PIMP AND NWELL AND LVTIMP CONTAINS PO
G	PO
D	DIFF AND PIMP AND LVTIMP AND NWELL NOT PO
S	DIFF AND PIMP AND LVTIMP AND NWELL NOT PO
B	Substrate

Table 4.32 pmos4t_lvt LVS Checking

Parameter Calculation	
Length	PO intersecting DIFF
Width	PO inside DIFF

4.3. Resistors

4.3.1. rnpoly

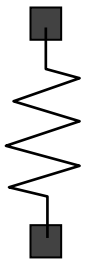

Figure 4.21. Symbol of rnpoly resistor

Table 4.33 rnpoly Spice model

Symbol name	Netlist
rnpoly	`r1 net28 net29 rnpoly w='0.4u' l='2u' m=1`

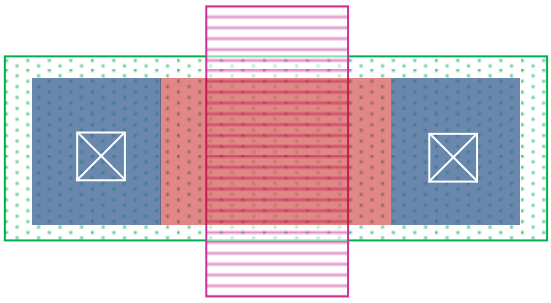

Figure 5.22 Layout of rnpoly resistor

Table 4.34 rnpoly Device Layers

Device Layers	Layer Color and Fill
RPOLY	
PO	
CO	
M1	
NIMP	

Table 4.35 rnpoly Device Derivation

Device Derivation	Device Layer Derivation
Recognition	PO AND RPOLY AND NIMP
PLUS	PO NOT RPOLY
MINUS	PO NOT RPOLY

Table 4.36 rnpoly LVS Checking

Parameter Calculation	
Length	Contact to Contact
Width	PO Width
Resistance	sheet resistance * Length / Width

4.3.2. rppoly

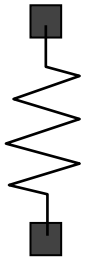

Figure 4.22. Symbol of rppoly resistor

Table 4.37 rppoly Spice model

Symbol name	Netlist
rppoly	`r7 net28 net29 rppoly w='0.4u' l='2u' m=1`

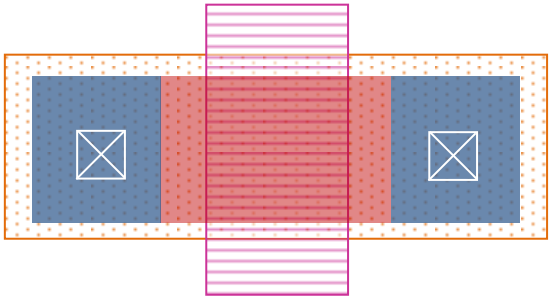

Figure 4.23. Layout of rppoly resistor

Table 4.38 rppoly Device Layers

Device Layers	Layer Color and Fill
RPOLY	
PO	
CO	
M1	
PIMP	

Table 4.39 rppoly Device Derivation

Device Derivation	Device Layer Derivation
Recognition	PO AND RPOLY AND PIMP
PLUS	PO NOT RPOLY
MINUS	PO NOT RPOLY

Table 4.40 rppoly LVS Checking

Parameter Calculation	
Length	Contact to Contact
Width	PO Width
Resistance	sheet resistance * Length / Width

4.3.3. rnpoly_wos

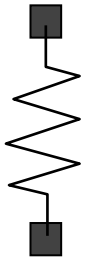

Figure 4.24. Symbol of rnpoly_wos resistor

Table 4.41 rnpoly_wos Spice model

Symbol name	Netlist
rnpoly_wos	`r1 net28 net29 rnpoly_wos w='0.4u' l='2u' m=1`

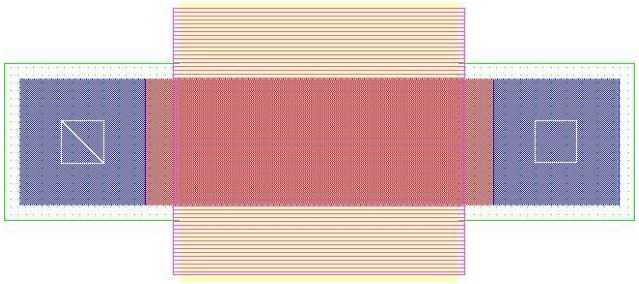

Figure 4.25. Layout of rnpoly_wos resistor

Table 4.42 rnpoly_wos Device Layers

Device Layers	Layer Color and Fill
RPOLY	
PO	
CO	
M1	
NIMP	
SBLK	

Table 4.43 rnpoly_wos Device Derivation

Device Derivation	Device Layer Derivation
Recognition	PO AND RPOLY AND SBLK AND NIMP
PLUS	PO NOT RPOLY NOT SBLK
MINUS	PO NOT RPOLY NOT SBLK

Table 4.44 rnpoly_wos LVS Checking

Parameter Calculation	
Length	Contact to Contact
Width	PO Width
Resistance	sheet resistance * Length / Width

4.3.4. rppoly_wos

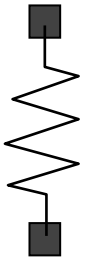

Figure 4.26. Symbol of rppoly_wos resistor

Table 4.45 rppoly_wos Spice model

Symbol name	Netlist
rppoly_wos	`r1 net28 net29 rppoly_wos w='0.4u' l='2u' m=1`

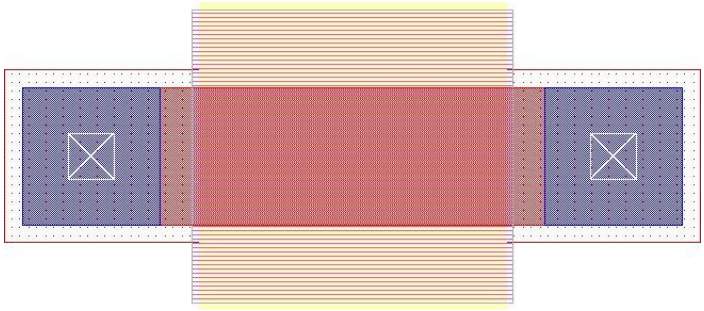

Figure 4.27. Layout of rppoly_wos resistor

Table 4.46 rppoly_wos Device Layers

Device Layers	Layer Color and Fill
RPOLY	
PO	
CO	
M1	
PIMP	
SBLK	

Table 4.47 rppoly_wos Device Derivation

Device Derivation	Device Layer Derivation
Recognition	PO AND RPOLY AND SBLK AND PIMP
PLUS	PO NOT RPOLY NOT SBLK
MINUS	PO NOT RPOLY NOT SBLK

Table 4.48 rppoly_wos LVS Checking

Parameter Calculation	
Length	Contact to Contact
Width	PO Width
Resistance	sheet resistance * Length / Width

4.4. Diode

4.4.1. nd

Figure 4.28. Symbol of nd diode

Table 4.49 nd Spice model

Symbol name	Netlist
nd	`d1 net45 net44 nd area='40.000f' m=1`

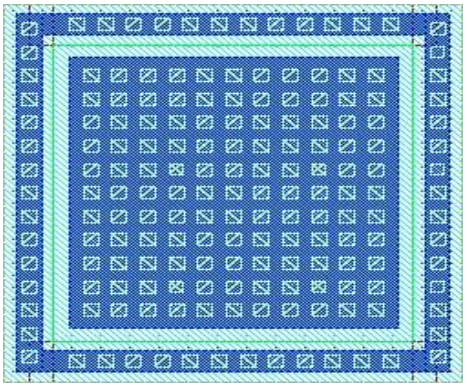

Figure 4.29. Layout of nd diode

Table 4.50 nd Device Layers

Device Layers	Layer Color and Fill
M1	
DIFF	
CO	
NWELL	
PIMP	
NIMP	
DIOD	

Table 4.51 nd Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIOD AND NIMP AND PIMP
PLUS	DIOD AND PIMP
MINUS	DIOD AND NIMP

Table 4.52 nd LVS Checking

Parameter	Calculation
area	Area of MINUS

4.4.2. pd

Figure 4.30. Symbol of pd diode

Table 4.53 pd Spice model

Symbol name	Netlist
pd	`d1 net45 net44 pd area='40.000f' m=1`

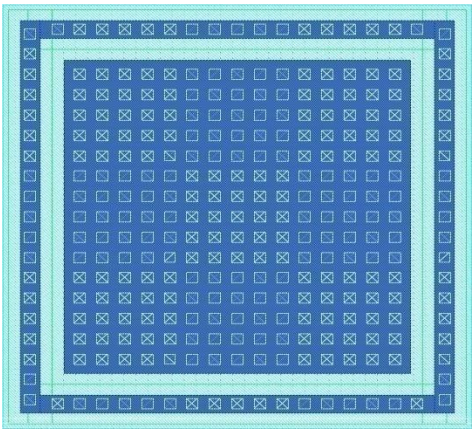

Figure 4.31. Layout of pd diode

Table 4.54 pd Device Layers

Device Layers	Layer Color and Fill
M1	
DIFF	
CO	
NWELL	
PIMP	
NIMP	
DIOD	

Table 4.55 pd Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIOD AND NWELL AND NIMP AND PIMP
PLUS	DIOD AND NWELL AND NIMP
MINUS	DIOD AND NWELL AND PIMP

Table 4.56 pd LVS Checking

Parameter	Calculation
area	Area of MINUS

4.5. BJT

4.5.1. hnpn

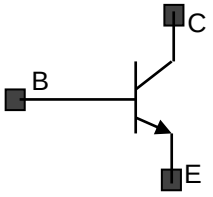

Figure 4.32. Symbol of hnpn transistor

Table 4.57 hnpn Spice model

Symbol name	Netlist
hnpn	`q1 net48 net50 net49 hnpn m=1`

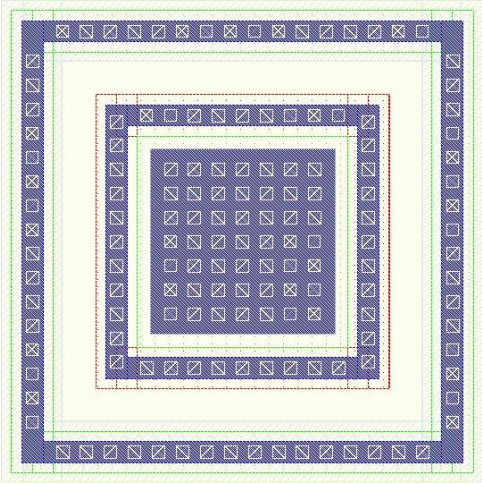

Figure 4.33. Layout of hnpn transistor

Table 4.58 hnpn Device Layers

Device Layers	Layer Color and Fill
DIFF	
NIMP	
PIMP	
NWELL	
CO	
M1	
BJTMARK	

Table 4.59 hnpn Device Derivation

Device Derivation	Device Layer Derivation
Recognition	BJTMARK AND PIMP AND NWELL
E	BJTMARK AND NIMP NOT NWELL
B	BJTMARK AND PIMP
C	BJTMARK AND NIMP AND NWELL

Table 4.60 hnpn LVS Checking

Parameter	Calculation
area	Area of Emitter

4.5.2. vpnp

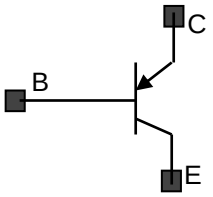

Figure 4.34. Symbol of vpnp transistor

Table 4.61 vpnp Spice model

Symbol name	Netlist
vpnp	`q9 net48 net50 net49 vpnp m=1`

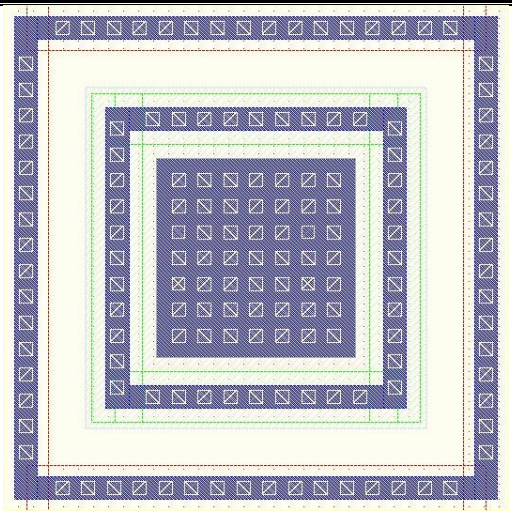

Figure 4.35. Layout of vpnp transistor

Table 4.62 vpnp Device Layers

Device Layers	Layer Color and Fill
DIFF	
NIMP	
PIMP	
NWELL	
CO	
M1	
BJTMARK	

Table 4.63 vpnp Device Derivation

Device Derivation	Device Layer Derivation
Recognition	BJTMARK AND PIMP AND NWELL
E	BJTMARK AND Nburied AND NIMP AND Pwell
B	BJTMARK AND Nburied AND PIMP AND Pwell
C	BJTMARK AND Nburied AND NIMP ANDNOT Pwell

Table 4.64 vpnp LVS Checking

Parameter Calculation	
area	Area of Emitter

5. References

1. SAED32/28nm EDK Documentation
2. OpenAccess (http://www.si2.org/?page=621)

6. Revision history

Table 6.1. Revision history

Revision	Date	Change
A.1	10/02/2011	Initial release