SAED 14nm Design Rules Document

SAED_EDK14_FinFET

Document # : SAED_EDK14_FinFET
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Technology : SAED14nm
Process : SAED14nm 1P9M 0.8V/1.5V/1.8V

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1. Introduction

This document is the part of SAED_EDK14 Educational Design Kit documentation. These design rules are free from intellectual property restrictions. It was considered to develop 14nm rules but sizes can be larger by 1-5% than in real processes to provide further portability of projects designed by this design rules to real processes.

As basis for layer names and design rules SAED 32nm process was used, which is based on MOSIS Scalable CMOS rules (SCMOS): http://www.mosis.com/Technical/Designrules/scmos/scmos-main.html. Some layers such as FIN, FINCUT, AXPOLY, and others have been added to the layer map. Design rule values for 14nm process are obtained by scaling available rules values and addition of known rules specific for 14nm. Also 14nm advanced rules supported by Synopsys IC Compiler Zroute router were added.

2. Layer Map

Layer #	Data type	Tape Out Layer	Drawing or Composite Layer	Layer name in Tech/Map File	Layer Name in DRC	Layer Name in LVS	Layer usage description
1	0	YES	Drawing	FIN	FINi	FINi	FIN
2	0	YES	Drawing	FINCUT	FINCUTi	FINCUTi	FIN cut for printing fine spaces
3	0	YES	Drawing	NWELL	NWELLi	NWELLi	NWELL
4	0	YES	Drawing	DNW	DNWi	DNWi	Deep NWELL
5	0	YES	Drawing	DIFF	DIFFi	DIFFi	Active area, thin oxide for device or interconnection
5	0	YES	Drawing	DDMY	DDMYi	DDMYi	Dummy DIFF layer; must be added if there's DIFF density rule violation
6	0	YES	Drawing	PIMP	PIMPi	PIMPi	P+ source/drain ion implantation
7	0	YES	Drawing	NIMP	NIMPi	NIMPi	N+ source/drain ion implantation
8	0	YES	Drawing	DIFF_15	DIFF_15i	DIFF_15i	1.5v thick oxide (second gate oxide)
9	0	YES	Drawing	DIFF_18	DIFF_15i	DIFF_15i	1.8v thick oxide (second gate oxide)
10	0	YES	Drawing	PAD	PADi	PADi	Pad opening
11	0	YES	Drawing	ESD	ESDi	ESDi	Layer for DRC and logic operation to form ESD implant. Use “ESD” to cover high voltage tolerant IO
12	0	YES	Drawing	SBLK	SBLKi	SBLKi	Resist protection oxide, non silicided area definition
13	0	YES	Drawing	PO	POi	POi	Gate poly, poly-silicon
13	1	YES	Drawing	PODMY	PODMYi	PODMYi	Dummy PO layer, must be added if there's PO density rule violation
14	0	YES	Drawing	POCUT	POCUTi	POCUTi	Poly gate conductor cut mask
15	0	YES	Drawing	TSLCO	TSLCOi	TSLCOi	
16	0	YES	Drawing	TSLCB	TSLCBi	TSLCBi	

Layer #	Data type	Tape Out Layer	Drawing or Composite Layer	Layer name in Tech/Map File	Layer Name in DRC	Layer Name in LVS	Layer usage description
17	0	YES	Drawing	CTM1	CTM1i	CTM1i	Connects trench silicide to M1 through Via0
17	1	YES	Drawing	CTM1_1	CTM1i_1	CTM1i_1	Double-patterned contact for connecting SRAM trench silicide to M1 through Via0, first exposure
17	2	YES	Drawing	CTM1_2	CTM1i_2	CTM1i_2	Double-patterned contact for connecting SRAM trench silicide to M1 through Via0, second exposure
18	0	YES	Drawing	CPO	CPOi	CPOi	Layer for connecting Poly to Metal via VIA0
18	1	YES	Drawing	CPO	CPOi_1	CPOi_1	Double-patterned contact for connecting SRAM Poly to M1 through Via0, first exposure
18	2	YES	Drawing	CPO	CPOi_2	CPOi_2	Double-patterned contact for connecting SRAM Poly to M1 through Via0, second exposure
19	0	YES	Drawing	M1	M1i	M1i	Metal1
19	1	YES	Drawing	M1DMY	M1DMYi	M1DMYi	Dummy of metal1
20	0	YES	Drawing	VIA1	VIA1i	VIA1i	Via12
21	0	YES	Drawing	M2	M2ii	M2i	Metal2
21	1	YES	Drawing	M2DMY	M2DMYi	M2DMYi	Dummy of metal2
22	0	YES	Drawing	VIA2	VIA2i	VIA2i	Via23
23	0	YES	Drawing	M3	M3i	M3i	Metal3
23	1	YES	Drawing	M3DMY	M3DMYi	M3DMYi	Dummy of metal3
24	0	YES	Drawing	VIA3	VIA3i	VIA3i	Via34
25	0	YES	Drawing	M4	M4i	M4i	Metal4
25	1	YES	Drawing	M4DMY	M4DMYi	M4DMYi	Dummy of metal4
26	0	YES	Drawing	VIA4	VIA4i	VIA4i	Via45

Layer #	Data type	Tape Out Layer	Drawing or Composite Layer	Layer name in Tech/Map File	Layer Name in DRC	Layer Name in LVS	Layer usage description
27	0	YES	Drawing	M5	M5i	M5i	Metal5
28	0	YES	Drawing	VIA5	VIA5i	VIA5i	Via56
29	0	YES	Drawing	M6	M6i	M6i	Metal6
29	1	YES	Drawing	M6DMY	M6DMYi	M6DMYi	Dummy of metal6
30	0	YES	Drawing	VIA6	VIA6i	VIA6i	Via67
31	0	YES	Drawing	M7	M7i	M7i	Metal7
31	1	YES	Drawing	M7DMY	M7DMYi	M7DMYi	Dummy of metal7
32	0	YES	Drawing	VIA7	VIA7i	VIA7i	Via78
33	0	YES	Drawing	M8	M8i	M8i	Metal8
33	1	YES	Drawing	M8DMY	M8DMYi	M8DMYi	Dummy of metal8
34	0	YES	Drawing	VIA8	VIA8i	VIA8i	Via89
35	0	YES	Drawing	M9	M9i	M9i	Metal9
35	1	YES	Drawing	M9DMY	M9DMYi	M9DMYi	Dummy of metal9
36	0	YES	Drawing	HVTIMP	HVTIMPi	HVTIMPi	Implant layer for hvt nmos/pmos drawing
37	0	YES	Drawing	LVTIMP	LVTIMPi	LVTIMPi	Implant layer for lvt nmos/pmos drawing
38	0	NO	Drawing	M1PIN	M1PIN	M1PIN	Metal1 text layer
39	0	NO	Drawing	M2PIN	M2PIN	M2PIN	Metal2 text layer
40	0	NO	Drawing	M3PIN	M3PIN	M3PIN	Metal3 text layer

2. Layer Map

Layer #	Data type	Tape Out Layer	Drawing or Composite Layer	Layer name in Tech/Map File	Layer Name in DRC	Layer Name in LVS	Layer usage description
41	0	NO	Drawing	M4PIN	M4PIN	M4PIN	Metal4 text layer
42	0	NO	Drawing	M5PIN	M5PIN	M5PIN	Metal5 text layer
43	0	NO	Drawing	M6PIN	M6PIN	M6PIN	Metal6 text layer
44	0	NO	Drawing	M7PIN	M7PIN	M7PIN	Metal7 text layer
45	0	NO	Drawing	M8PIN	M8PIN	M8PIN	Metal8 text layer
46	0	NO	Drawing	M9PIN	M9PIN	M9PIN	Metal9 text layer
47	0	YES	Drawing	MRDL	MRDL	MRDL	Redistributional Layer
48	0	YES	Drawing	VIARDL	VIARDL	VIARDL	M9 to MRDL VIA
49	0	NO	Drawing	MRPIN	MRPIN	MRPIN	MRDL text layer
50	0	NO	Drawing	HOTNWL	HOTNWLi	HOTNWi	Hot NWELL marking layer for DRC. Use “HOTNWL” to cover hot-NWELL width.
51	0	NO	Drawing	DIOD	DIODi	DIODi	Diode marking layer for LVS. Cover P+DIFF for P+/NWELL diode, N+DIFF for N+/PWELL diode, and NWELL for NWELL/PWELL diode.
52	0	NO	Drawing	BJTMY	BJTMYi	BJTMYi	BJT marking layer to cover BJT device for analog layout rules.
53	0	NO	Drawing	RNW	RNWi	RNWi	NWELL resistor marking layer for DRC and LVS.
54	0	NO	Drawing	RMARK	RMARKi	RMARKi	Resistor marking layer for LVS. The cutting edge of RPOLY over PO/DIFF determines W/L of resistors.
56	0	NO	Drawing	LOGO	LOGO		DRC dummy layer for product label and logo
57	0	NO	Drawing	IP	IP		IP tagging text layer
58	0	NO	Drawing	RM1	RM1i	RM1i	Metal1 resistor marking layer for LVS. The cutting edge of RM1 over metals determinbes W/L of metal resistors.

Layer #	Data type	Tape Out Layer	Drawing or Composite Layer	Layer name in Tech/Map File	Layer Name in DRC	Layer Name in LVS	Layer usage description
59	0	NO	Drawing	RM2	RM2i	RM2i	Metal2 resistor marking layer for LVSA. The cutting edge of RM2 over metals determines W/L of metal resistors.
60	0	NO	Drawing	RM3	RM3i	RM3i	Metal3 resistor marking layer for LVSA. The cutting edge of RM3 over metals determines W/L of metal resistors.
61	0	NO	Drawing	RM4	RM4i	RM4i	Metal4 resistor marking layer for LVSA. The cutting edge of RM4 over metals determines W/L of metal resistors.
62	0	NO	Drawing	RM5	RM5i	RM5i	Metal5 resistor marking layer for LVSA. The cutting edge of RM5 over metals determines W/L of metal resistors.
63	0	NO	Drawing	RM6	RM6i	RM6i	Metal6 resistor marking layer for LVSA. The cutting edge of RM6 over metals determines W/L of metal resistors.
64	0	NO	Drawing	RM7	RM7i	RM7i	Metal7 resistor marking layer for LVSA. The cutting edge of RM7 over metals determines W/L of metal resistors.
65	1	NO	Drawing	RM8	RM8i	RM8i	Metal8 resistor marking layer for LVSA. The cutting edge of RM8 over metals determines W/L of metal resistors.
66	0	NO	Drawing	RM9	RM9i	RM9i	Metal9 resistor marking layer for LVSA. The cutting edge of RM9 over metals determines W/L of metal resistors.
81	0	YES	Drawing	VIA0	VIA0i	VIA0i	Contact
82	0	YES	Drawing	DIFFCUT	DIFFCUTi	DIFFCUTi	When drawn on DIFF cancels it out
83	0	YES	Drawing	AXPOLY	AXPOLYi	AXPOLYi	
84	0	YES	Drawing	SLVTIMP	SLVTIMPi	SLVTIMPi	Marking layer for superlow Vt devices
85	0	YES	Drawing	FGATE	FGATEi	FGATEi	Marks Poly shapes that form a floating Gate
86	0	YES	Drawing	B_VIAO	B_VIA0i	B_VIA0i	Butted VIA_0
90	0	YES	Drawing	M1_3	M1_3i	M1_3i	Red Metal1

Layer #	Data type	Tape Out Layer	Drawing or Composite Layer	Layer name in Tech/Map File	Layer Name in DRC	Layer Name in LVS	Layer usage description
91	0	NO	Drawing	M2_3	M2_3i	M2_3i	Red Metal2
92	0	NO	Drawing	M3_3	M3_3i	M3_3i	Red Metal3

3. Design Rules

3.1. Definitions

Definitions of basic layout rules terminology Is given in Table 1, and figures 1-6 below.

Table 1. Design Rules Terminology

Rule #	Mark	Rule description
Enclosure	a	distance between inside of the edge of 1 st layer and outside of the edge of 2 nd layer
Space	b	distance between outside of the edge of 1 st layer and outside of the edge of 2 nd layer
Overlap	c	distance between inside of the edge of 1 st layer and inside of the edge of 2 nd layer
Width	d	distance between inside parts of the same layer
Extension	e	distance between inside of the edge of 1 st layer and outside of the edge of 2 nd layer
Area	h*i	production of objects width and height
Enclosed area	f*g	production of width and height of layer opening
Parallel run length	j (j1)	distance of cross-projection of two outside edges parallel to each other (running in parallel)
Span	k(k1)	the dimension that is perpendicular to the layer' s edge used to calculate parallel length to its neighboring metal shapes

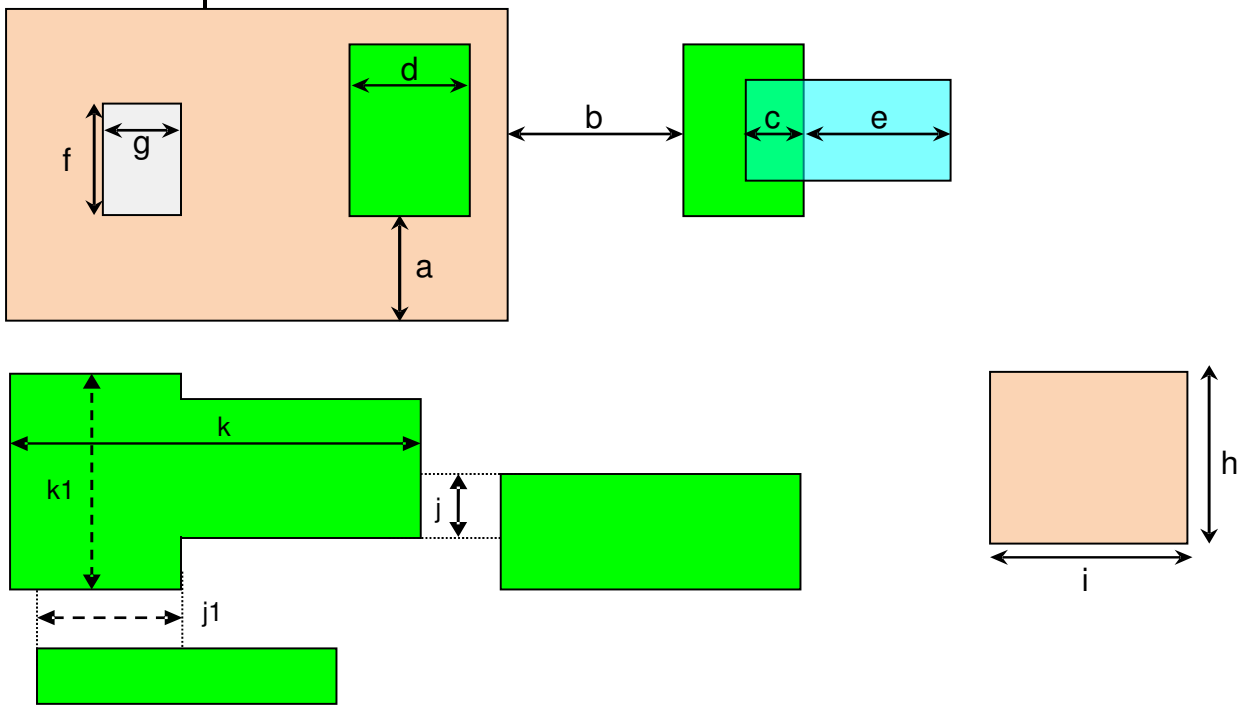
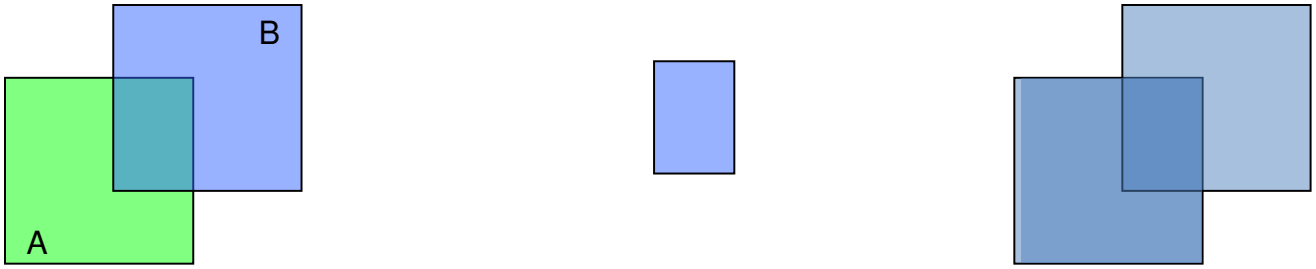


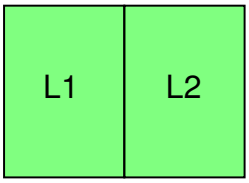
Figure 1. Definitions of layout geometrical terminology

In the definition of design rules layer Boolean operations (AND, OR, etc.) and their relationships is mentioned. The definitions of those are given below.



A AND B A OR B

Figure 2. AND and OR operations



L1 and L2 are butting each other

Figure 3. Butting

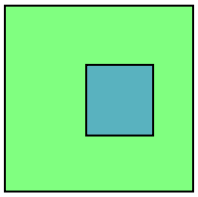


Figure 4. INSIDE

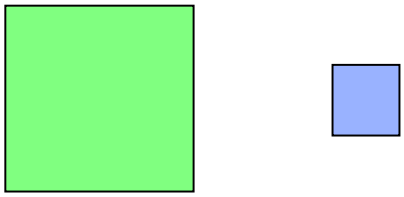


Figure 5. OUTSIDE

Some layers mentioned in the design rules are not process layers but are derived from process layers by Boolean operations. The used derived layers are:

IMP = PIMP or NIMP
NDIFF = DIFF and NIMP
PDIFF = DIFF and PIMP
N+Active = NDIFF and PWELL
P+Active = PDIFF and NWELL
ACTIVE = P+Active or N+Active
PTAP = PDIFF and PWELL
NTAP = NDIFF and NWELL
TAP = PTAP or NTAP
GATE = POLY and ACTIVE
NGATE = POLY and NACTIVE
PGATE = POLY and PACTIVE

Table 2. FIN Rules

Rule #	Rule description	µm	Mark
FIN.W.1	FIN exact vertical width	0.014	a
FIN.S.1	Minimum spacing	0.036	b

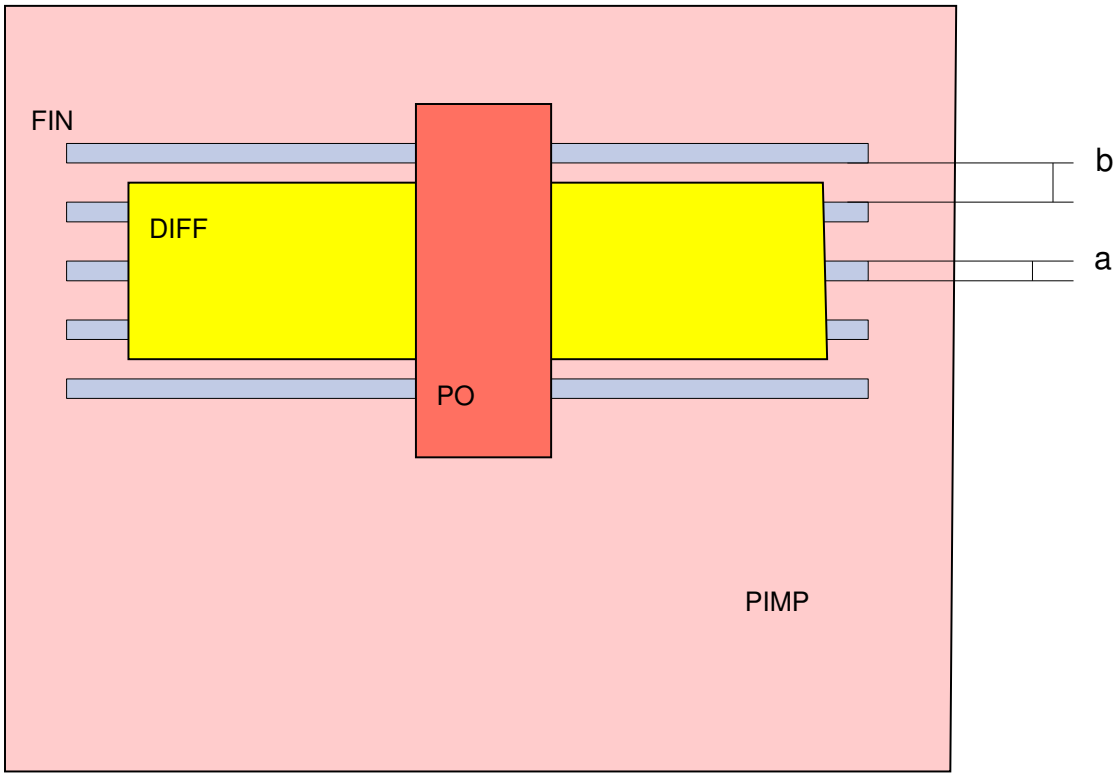


Figure 3. FIN Rules

3.2. General rules

Table 3. NWELL Rules

Rule #	Rule description	µm	Mark
NWELL.W.1	Minimum width	0.1	a
NWELL.A.1	Minimum area	0.23	d
NWELL.A.2	Minimum enclosed area	0.1	e
NWELL.S.1	Minimum spacing between wells at same potential	0.13	b
NWELL.S.2	Minimum spacing between wells at different potential	0.13	c
NWELL.S.3	N+ Active minimum space to N_WELL	0.05	-
NWELL.EN.1	P+ Active minimum within N_WELL	0.05	-

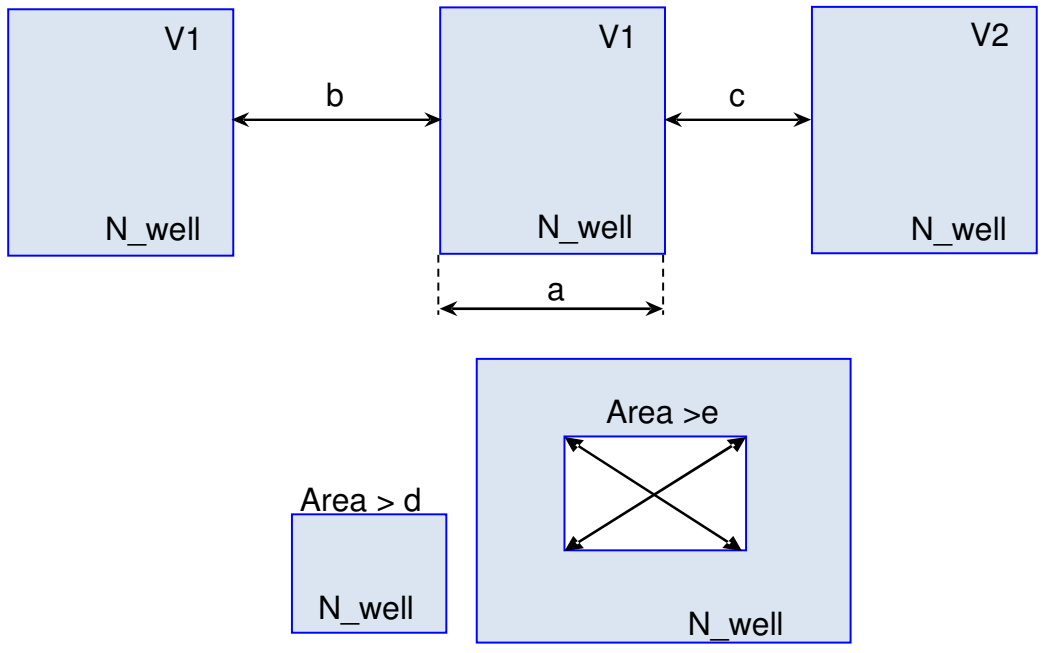


Figure 4. NWELL Rules

Table 4. Deep N Well (DNW) Rules

Rule #	Rule description	µm	Mark
DNW.W.1	Minimum width	1.8	a
DNW.S.1	Minimum spacing, DNW to DNW	3.5	b
DNW.S.2	Minimum spacing, DNW to unrelated NWELL	2.5	c
DNW.S.3	Minimum spacing external N+Active to DNW	1.5	d
DNW.E.1	Minimum enclosure, N+Active by isolated P-well	0.5	f
DNW.O.1	Minimum overlap, NWELL over DNW edge	0.4	e

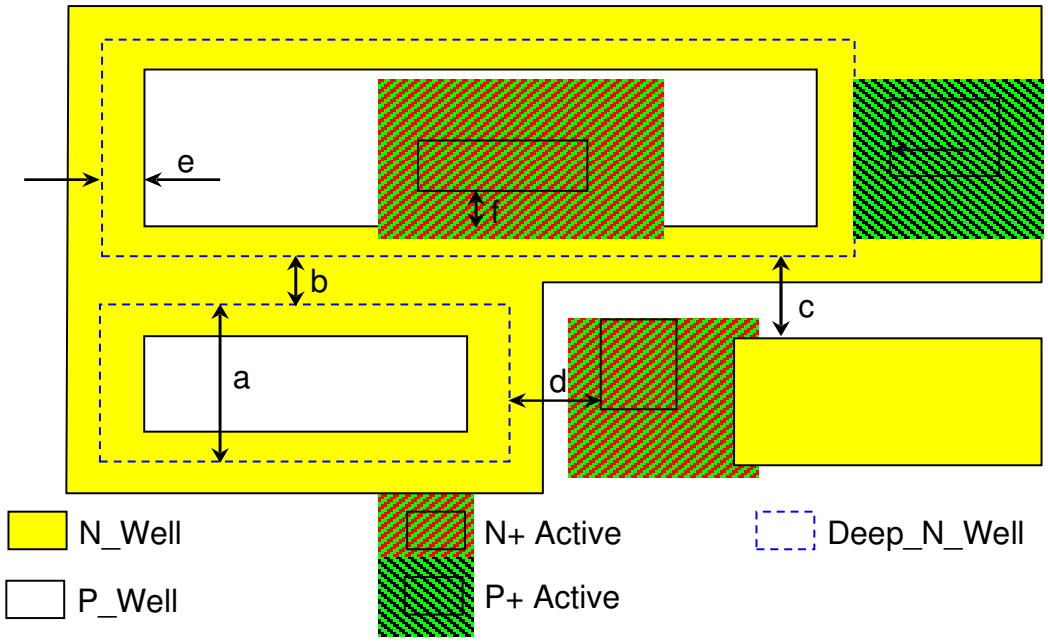


Figure 5. DNW Rules

Table 5. DIFF Rules

Rule #	Rule description	µm	Mark
DIFF.W.1	Minimum width	0.044	a
DIFF.W.2	DIFF not DIFFCUT minimum C_width	0.074	d
DIFF.W.3	Maximum width	23	d
DIFF.S.1	Minimum spacing	0.074	b
DIFF.S.2	Minimum P_space	0.1	b
DIFF.S.3	Minimum notch	0.074	c
DIFF.S.4	Minimum spacing to FIN	0.018	c
DIFF.S.5	Minimum overlap, P_overlap past FIN	0.018	f
DIFF.A.1	DIFF minimum area	0.0066	e

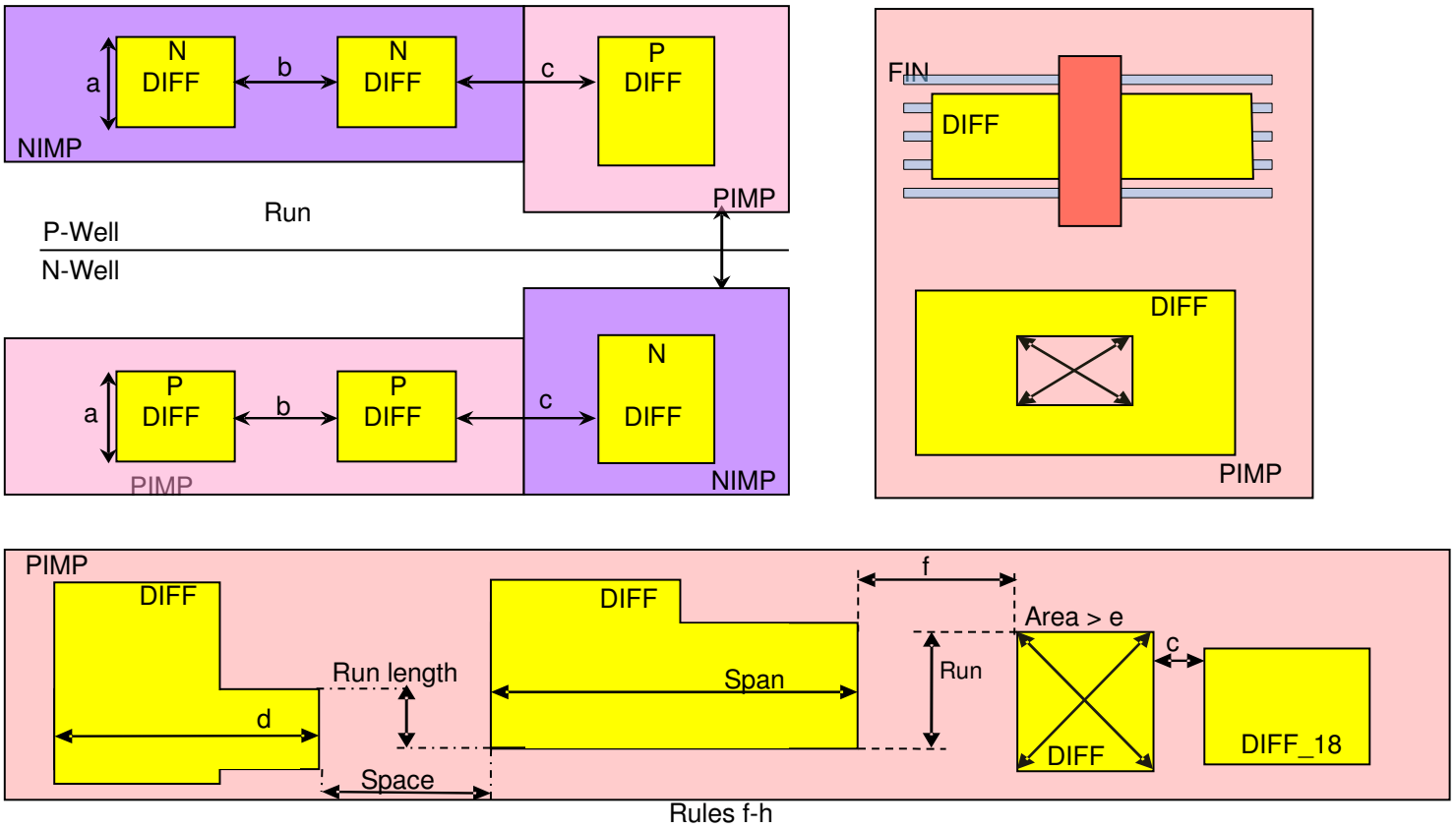


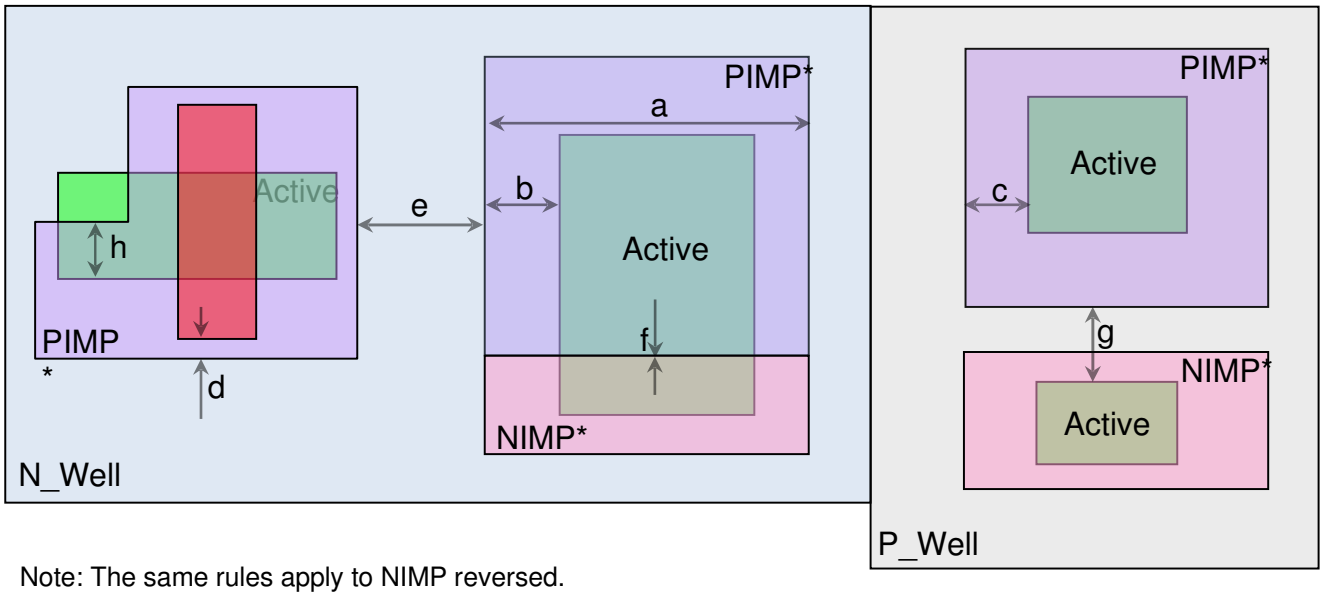
Figure 6.DIFF Rule

Table 6. NIMP Rules

Rule #	Rule description	µm	Mark
NIMP.W.1	Minimum width	0.1	a
NIMP.E.1	Enclosure of N+Active	0.04	b
NIMP.E.2	Enclosure of NTAP	0.02	c
NIMP.E.3	Poly enclosure of NIMP in horizontal direction	0.034	d
NIMP.S.1	Minimum space	0.1	e
NIMP.S.2	Minimum spacing To butted P+Active	0.05	f
NIMP.S.3	Minimum spacing to P+Active in N_Well	0.05	g
NIMP.O.1	Minimum active overlap	0.05	h
NIMP.A.1	Minimum area	0.038	-

Table 7. PIMP Rules

Rule #	Rule description	µm	Mark
PIMP.W.1	Minimum width	0.1	a
PIMP.E.1	Enclosure of P+Active	0.04	b
PIMP.E.2	Enclosure of PTAP	0.02	c
PIMP.S.1	Minimum space	0.1	e
PIMP.S.2	Minimum space to butted N+Active	0.05	f
PIMP.S.3	Minimum spacing to N+Active in P_Well	0.05	g
PIMP.O.1	Minimum active overlap	0.05	h
PIMP.A.1	Minimum area	0.038	-



Note: The same rules apply to NIMP reversed.

Figure 7. PIMP,NIMP Rules

Table 8. DIFF_15 Rules

Rule #	Rule description	µm	Mark
DIFF_15.S.1	Minimum apacing	0.5	a
DIFF_15.S.2	Minimum space external Active	0.2	b
DIFF_15.A.2	Min enclosed area	0.2	c

Table 9. DIFF_18 Rules

Rule #	Rule description	µm	Mark
DIFF_18.S.1	Minimum spacing	0.26	a
DIFF_18.S.2	Minimum space external DIFF	0.1	b
DIFF_18.A.2	Max enclosed area	0.2	c

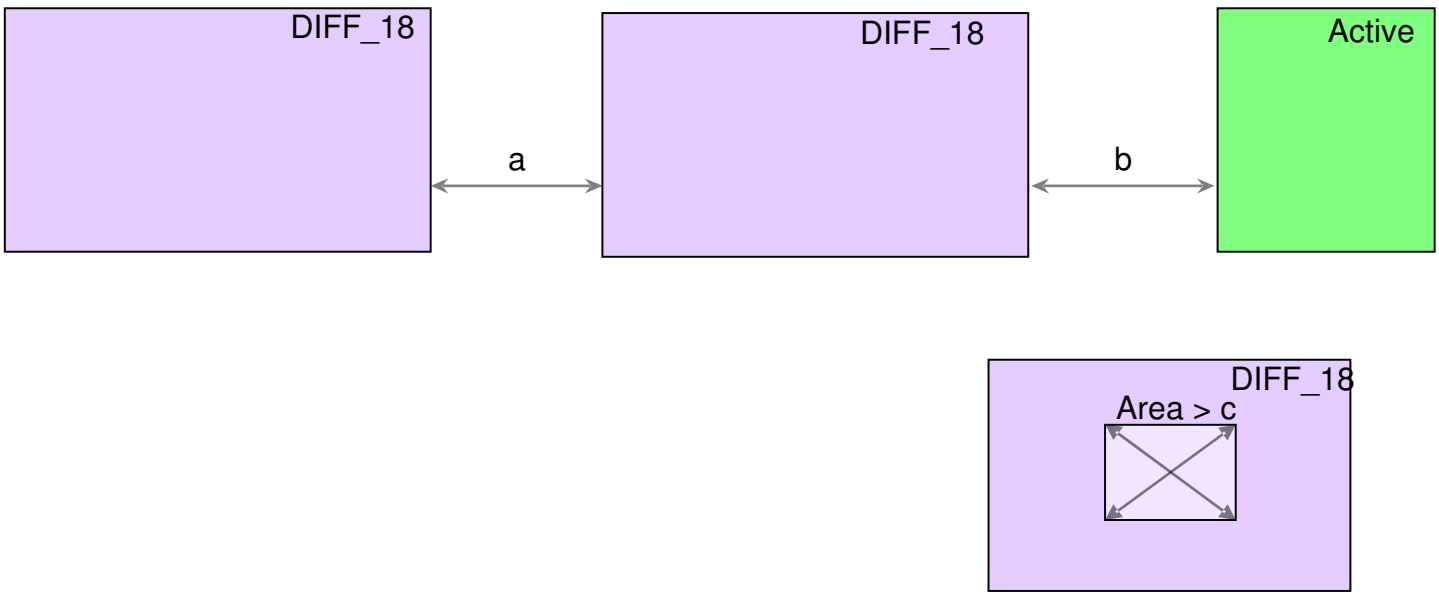


Figure 8. DIFF_18 Rules

Table 10. SBLK Rules

Rule #	Rule description	µm	Mark
SBLK.W.1	Minimum SBLK width	0.07	a
SBLK.S.1	Minimum SBLK spacing	0.02	b

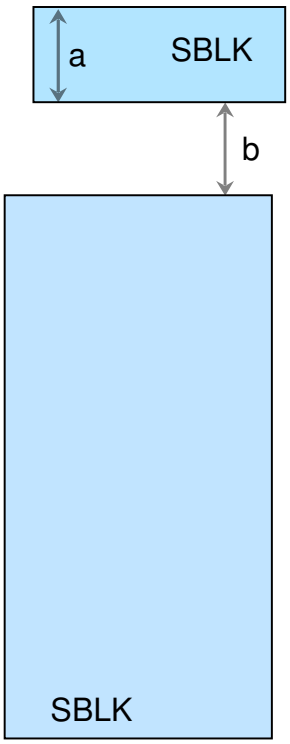


Table 11. PO Rules

Rule #	Rule description	µm	Mark
PO.W.1	Minimum width	0.014	a
PO.W.4.1	Minimum gate_15 length	0.26	b
PO.W.4.1	Minimum gate_18 width	0.16	c
PO.S.1	PO minimum spacing over field	0.05	e
PO.S.2	Gate minimum spacing	0.06	f
PO.S.4	Minimum PO spacing when w=0.014	0.06	g
PO.S.5	Minimum PO spacing when w=0.15	0.11	h
PO.S.6	Minimum space of PO to DIFF	0.03	i
PO.S.7	Minimum space of PO to DIFF with vertically measured width<0.05, parallel runlength >0.1	0.04	d

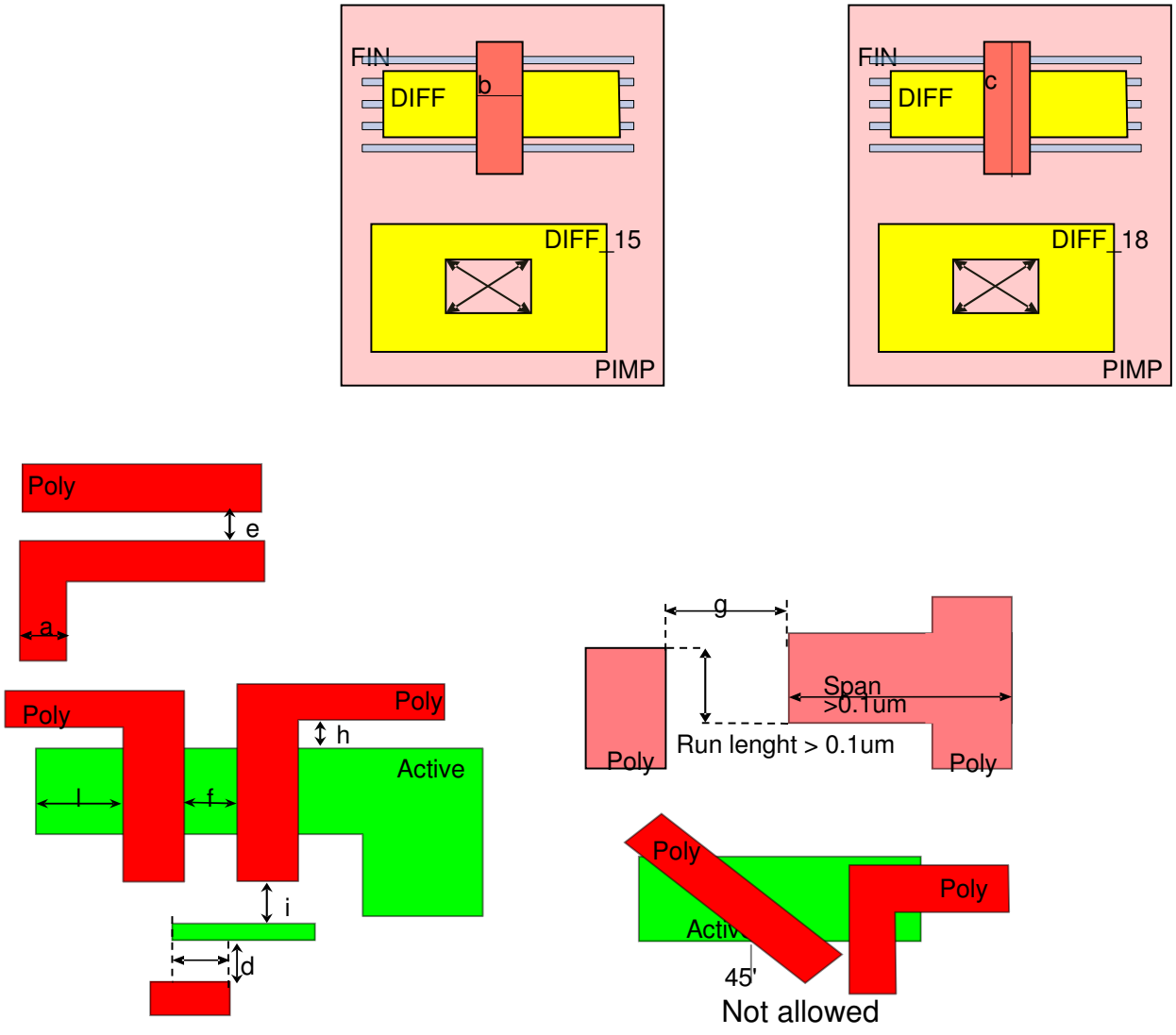


Figure 10. PO Rules

Table 12. M1 Rules

Rule #	Rule description	µm	Mark
M1.W.1	Minimum width	0.03	a
M1.W.2	Maximum width	0.05	e
M1.S.1	Minimum spacing	0.044	b
M1.S.2	Minimum spacing between same masks	0.07	-
M1.S.5	Minimum spacing from CTM1 to TSLO	0.04	-
M1.O.1	Minimum vertical ovrerlap	0.02	-
M1.A.1	Minimum Area	0.0008	f

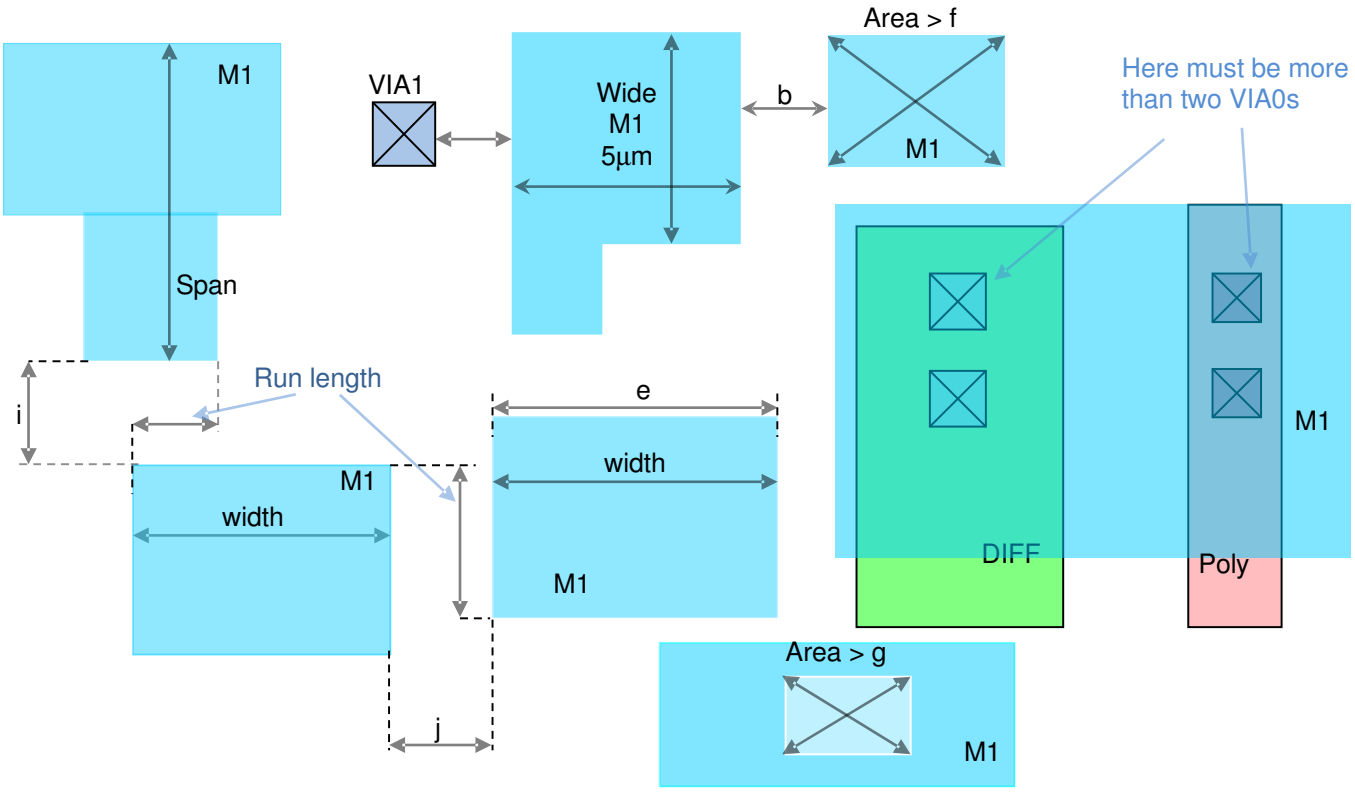


Figure 11. M1 Rules

Table 13. MX Rules, where X=1...3

Rule #	Rule description		µm	Mark
MX.W.1	Minimum width		0.034	a
MX.W.2	Maximum width		0.8	e
MX.S.1	Minimum spacing		0.04	b
MX.S.2	Minimum spacing		0.033	c
	Minimum spacing depending on metal width of one of lines and their parallel run length			j
	metal width (c)	parallel run length (d)		
MX.S.2	>0.058µm	>0.07 µm	0.064	j1
MX.S.3	>0.06µm	>0.07µm	0.065	j2
MX.S.4	>1.5 µm	>0 µm	0.55	j3
MX.S.5	>0.185 µm	>0.25 µm	0.85	j4
MX.S.6	Minimum spacing of MX with span > 0.075 µm with parallel run length > 0.104 µm		0.6	i
MX.S.7	Minimum spacing of MX with span > 0.150 µm with parallel run length > 0.3 µm		0.65	i
MX.A.1	Minimum Area		0.016	f
MX.A.2	Minimum Enclosed area		0.2	g

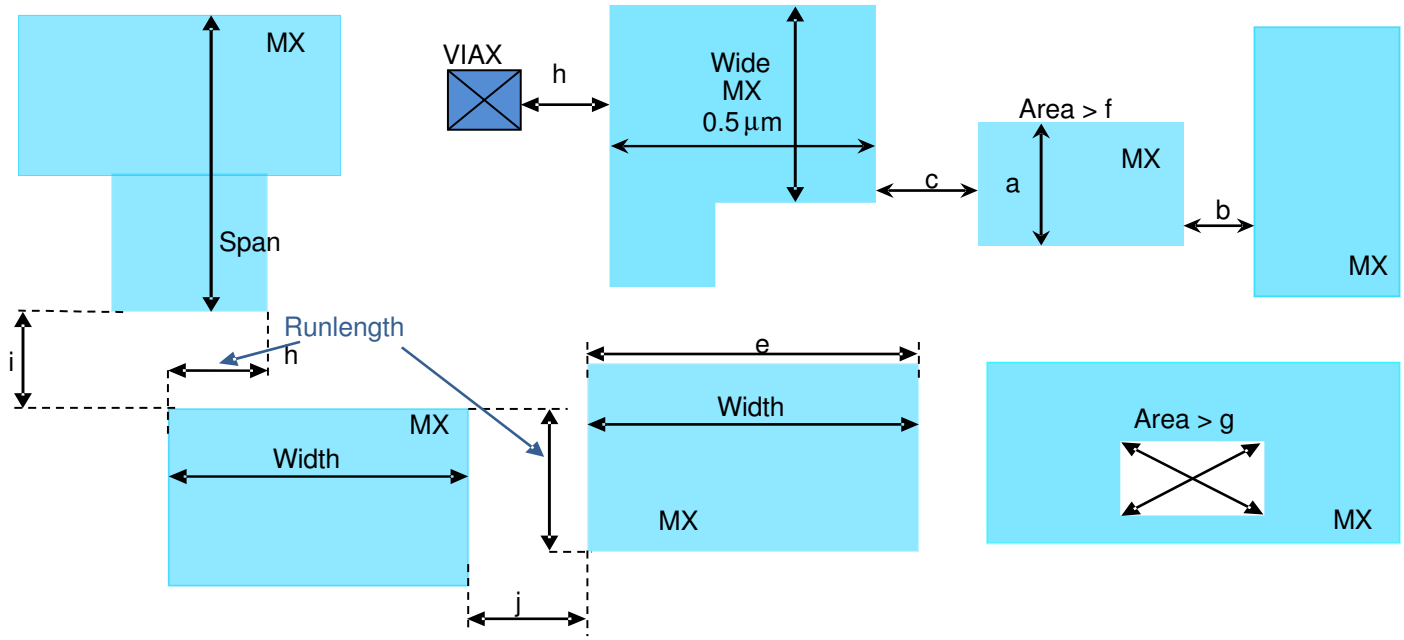


Figure 12. MX Rules

Table 13. MX Rules, where X=4...9

Rule #	Rule description		µm	Mark
MX.W.1	Minimum width		-	a
MX.W.2	Maximum width		3	e
MX.S.1	Minimum spacing		0.04	b
MX.S.2	Minimum spacing		0.06	c
	Minimum spacing depending on metal width of one of lines and their parallel run length			j
	metal width (c)	parallel run length (d)		
MX.S.2	>0.2 µm		0.06	j1
MX.S.3.1	>0.08µm	>0.08µm	0.06	j2
MX.S.3.2	>0.08µm	>0.08µm	0.065	j3
MX.S.3.3	>0.08 µm	>0.08 µm	0.075	j4
MX.S.4	>0.7 µ m	>0.08 µm	0.6	i

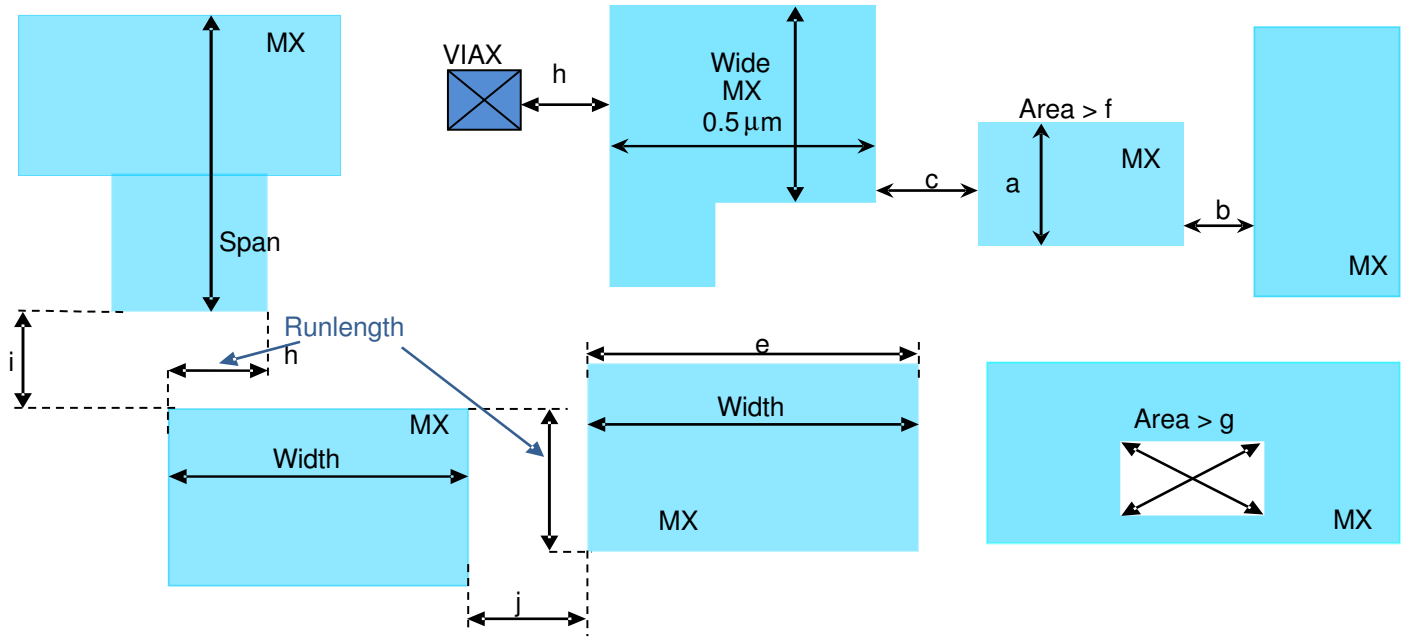


Figure 12. MX Rules

Table 15. M1_3 Rules

Rule #	Rule description	µm	Mark
M1_3.W.1	Minimum width	0.034	
M1_3.W.2	Maximum width	0.8	
M1_3.S.1	Minimum spacing	0.04	
M1_3.S.2	Minimum spacing if metal width of one of lines >0.06 and their parallel run length>0.07	0.06	
M1_3.S.3	Minimum spacing if metal width of one of lines >0.06 and their parallel run length>0.07	0.065	
M1_3.S.4	Minimum spacing if metal width of one of lines>1.5 and their parallel run length>0	0.55	
M1_3.S.5	Minimum spacing if metal width of one if lines>0.185 and their parallel run length>0.25	0.085	
M1_3.S.6	Minimum spacing of M1_3 with span >=0.075 with parallel run length>0.104	0.06	
M1_3.S.7	Minimum spacing of M1_3 with span>0.150 with parallel run length>0.104	0.065	
M1_3.A.1	Minimum area	0.005	
M1_3.A.2	Minimum enclosed area	0.04	

Table 16. M2_3 Rules

Rule #	Rule description	µm	Mark
M2_3.W.1	Minimum width	0.034	
M2_3.W.2	Maximum width	0.8	
M2_3.S.1	Minimum spacing	0.04	
M2_3.S.2	Minimum spacing if methal width of one of lines >0.058 and their parallel run length > 0.07	0.06	
M2_3.S.3	Minimum spacing if methal width of one of lines >0.06 and their parallel run length > 0.07	0.065	
M2_3.S.4	Minimum spacing if methal width of one of lines >1.5 and their parallel run length > 0	0.55	
M2_3.S.5	Minimum spacing if methal width of one of lines >0.185 and their parallel run length > 0.25	0.085	
M2_3.S.6	Minimum spacing of M2_3 with span >= 0.075 and with parallel run length > 0.104	0.06	
M2_3.S.7	Minimum spacing of M2_3 with span >= 0.150 and with parallel run length > 0.3	0.065	
M2_3.A.1	Minimum area	0.005	
M2_3.A.2	Minimum enclosed	0.04	

Table 17. M3_3 Rules

Rule #	Rule description	µm	Mark
M3_3.W.1	Minimum width	0.034	
M3_3.W.1	Maximum widt	0.8	
M3_3.S.1	Minimum spacing	0.04	
M3_3.S.2	Minimum spacing if methal width of one of lines >0.058 and their parallel run length > 0.07	0.06	
M3_3.S.3	Minimum spacing if methal width of one of lines >0.06 and their parallel run length > 0.07	0.065	
M3_3.S.4	Minimum spacing if methal width of one of lines >1.5 and their parallel run length > 0	0.55	
M3_3.S.5	Minimum spacing if methal width of one of lines >0.185 and their parallel run length > 0.25	0.085	
M3_3.S.6	Minimum spacing of M2_3 with span >= 0.075 and with parallel run length > 0.104	0.06	
M3_3.S.7	Minimum spacing of M2_3 with span >= 0.150 and with parallel run length > 0.3	0.065	
M3_3.A.1	Minimum area	0.005	
M3_3.A.2	Minimum enclosed	0.04	

Table 18. MRDL Rules

Rule #	Rule description	µm	Mark
MRDL.W.1	Minimum width	2	a
MRDL.W.2	Maximum width	40	b
MRDL.S.1	Minimum spacing	2	c

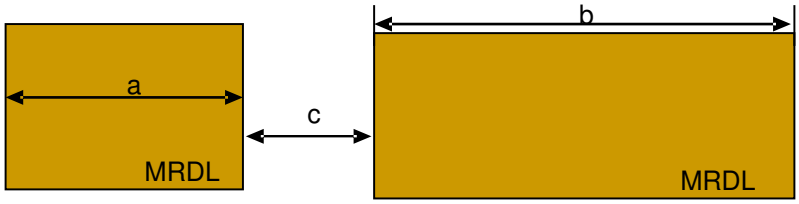


Figure 14. MRDL Rules

Table 19. VIA0 Rules

Rule #	Rule description	µm	Mark
VIA0.W.1	Exact contact size	0.03	
VIA0.S.1	Minimum contakt spacing	0.074	
VIA0.S.2	Minimum contact spacing to contact on the different net	0.05	
VIA0.E.1	Minimum enclosure by M1	0.002	
VIA0.E.2	Minimum enclosure by M1_3	0.002	

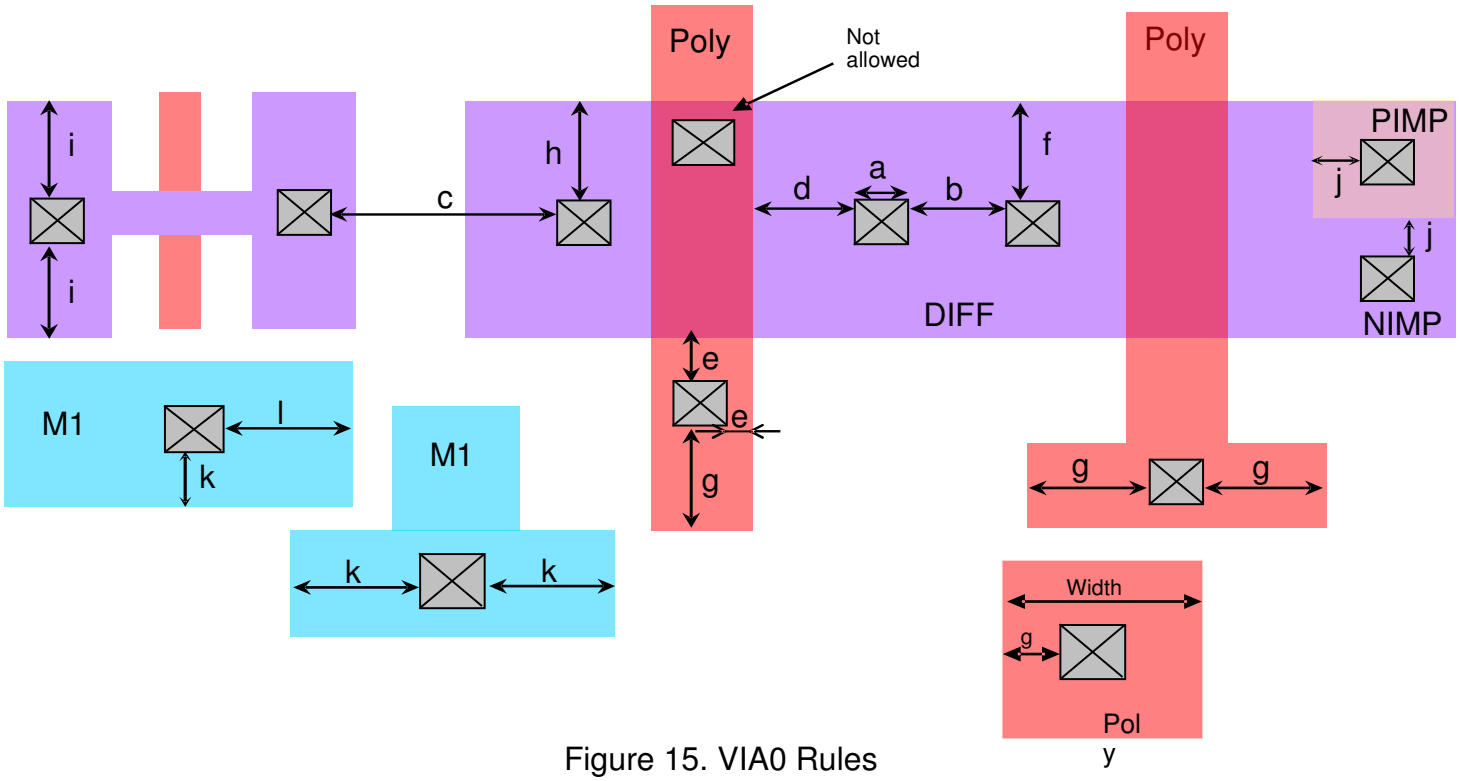


Figure 15. VIA0 Rules

Table 20. VIAX Rules, where X=1..2

Rule #	Rule description	µm	Mark
VIAX.W.1	Exact length and width of square cut VIAx (VIAxSQ)	0.03	a
VIAX.W.2	Exact length and width of large square cut VIAx(VIAxLG)	0.06	b
VIAX.W.3	Exact length of rectangular cut VIAx (VIAxBAR)	0.06	c
VIAX.W.4	Exact width of rectangular cut VIAx (VIAxBAR)	0.03	d
VIAX.S.1	Minimum spacing of VIAxSQ to VIAxSQ	0.074	e
VIAX.S.2	Minimum spacing of VIAxSQ to VIAxBAR or VIAxLG	0.08	f
VIAX.S.3	Minimum spacing of VIAxBAR or VIAxLG to VIAxBAR or VIAxLG	0.08	g
VIAX.E.1	Minimum VIAx enclosure by MX and MX+1	0.002	h
VIAX.E.2	Minimum VIAx enclosure by MX and MX+1 at least two opposite sides	0.003	i

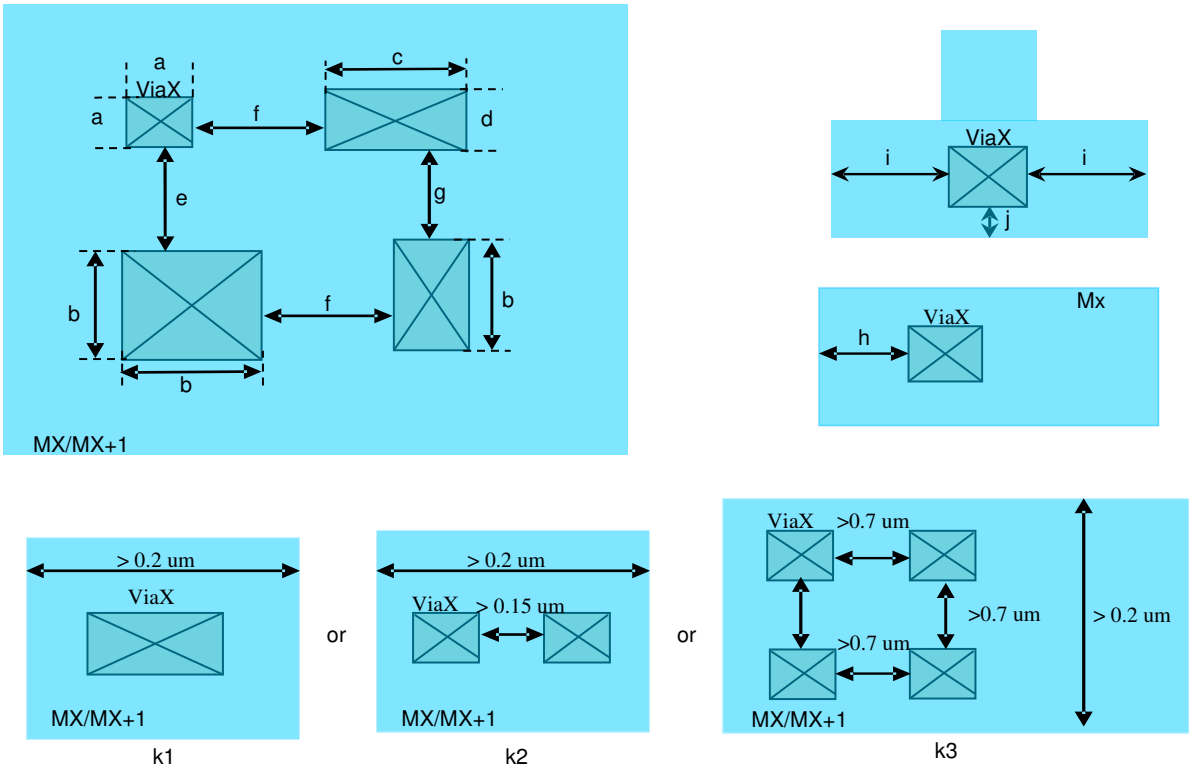


Figure 16. VIAX Rules

Table 20. VIAX Rules, where X=3..4

Rule #	Rule description	µm	Mark
VIAX.W.1	Exact length and width of square cut VIAx (VIAxSQ)	0.06	a
VIAX.W.2	Exact length and width of large square cut VIAx(VIAxLG)	0.12	b
VIAX.W.3	Exact length of rectangular cut VIAx (VIAxBAR)	0.12	c
VIAX.W.4	Exact width of rectangular cut VIAx (VIAxBAR)	0.06	d
VIAX.S.1	Minimum spacing of VIAxSQ to VIAxSQ	0.15	e
VIAX.S.2	Minimum spacing of VIAxSQ to VIAxBAR or VIAxLG	0.08	f
VIAX.S.3	Minimum spacing of VIAxBAR or VIAxLG to VIAxBAR or VIAxLG	0.085	g
VIAX.E.1	Minimum VIAx enclosure by MX and MX+1	0.085	h
VIAX.E.2	Minimum VIAx enclosure by MX and MX+1 at least two opposite sides	0.003	i

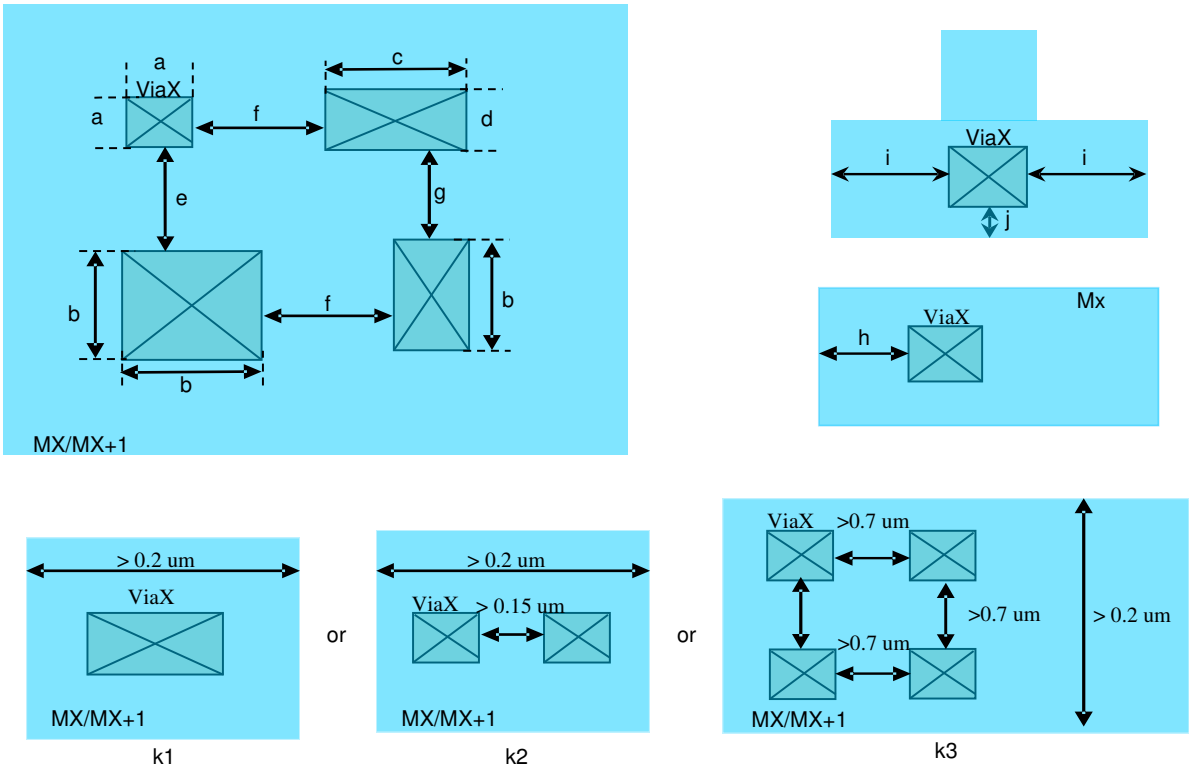


Figure 16. VIAX Rules

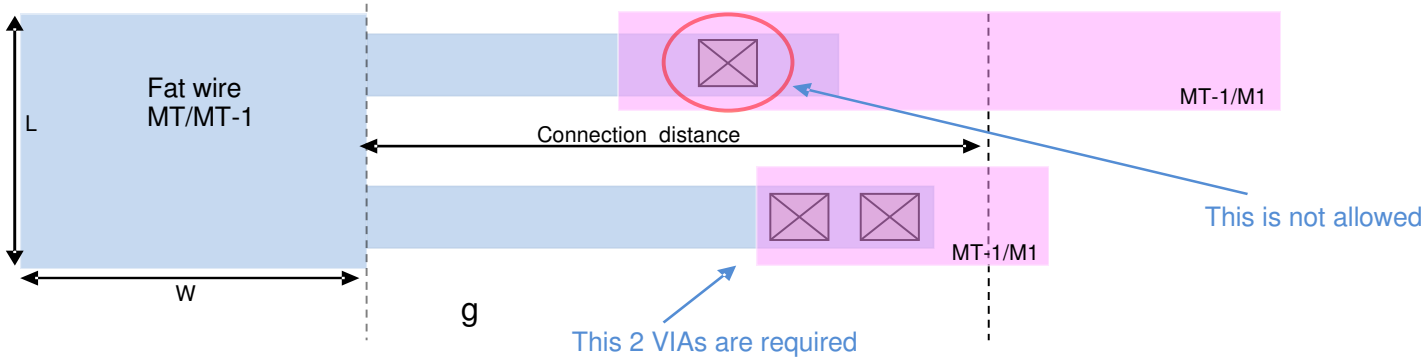


Figure 19. VIAT Rules

Table 22. VIARDL Rules

Rule #	Rule description	µm	Mark
VIARDL.W.1	Exact size	2	a
VIARDL.S.1	Minimum VIARDL spacing	2	b
VIARDL.E.1	Minimum VIARDL enclosure by MRDL	0.5	c

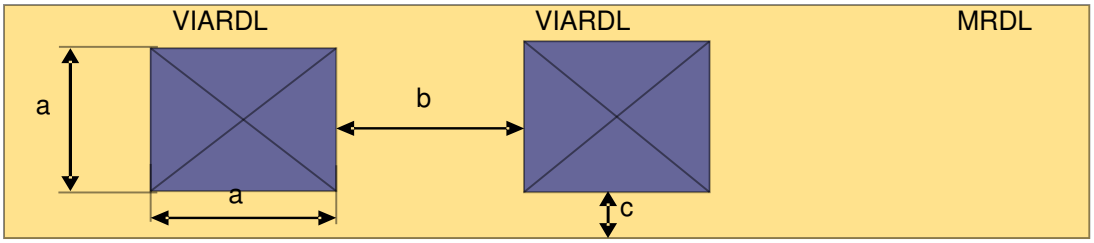


Figure 18. VIARDL Rules

Table 23. HVTIMP Rules

Rule #	Rule description	µm	Mark
HVTIMP.W.1	Minimum width	0.074	a
HVTIMP.S.1	Minimum spacing	0.074	b

Table 24. LVTIMP Rules

Rule #	Rule description	µm	Mark
LVTIMP.W.1	Minimum width	0.074	a
LVTIMP.S.1	Minimum spacing	0.074	b

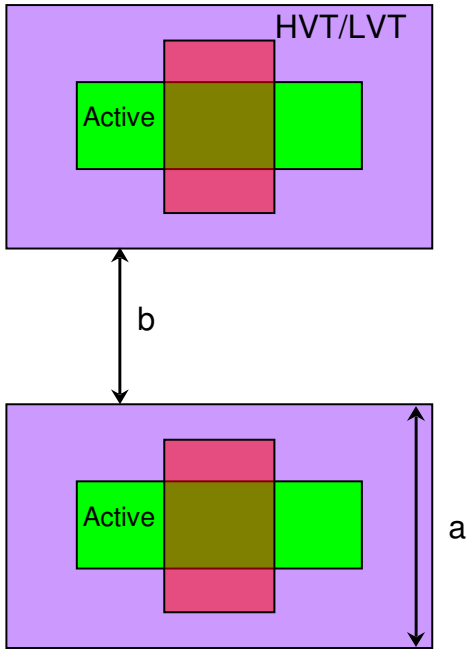


Figure 19. HVTIMP, LVTIMP Rules

Table 25. PAD Rules

Rule #	Rule description	µm	Mark
PAD.W.1	PAD minimum bonding passivation opening width	18	a
PAD.W.2	PAD minimum bonding passivation openind length	70	b
PAD.E.1	Minimum enclosure by MRDL	2	e
PAD.S.1	Minimum spacing	7	f
PAD.S.2	PAD metal minimum space to unrelated MRDL	2	g

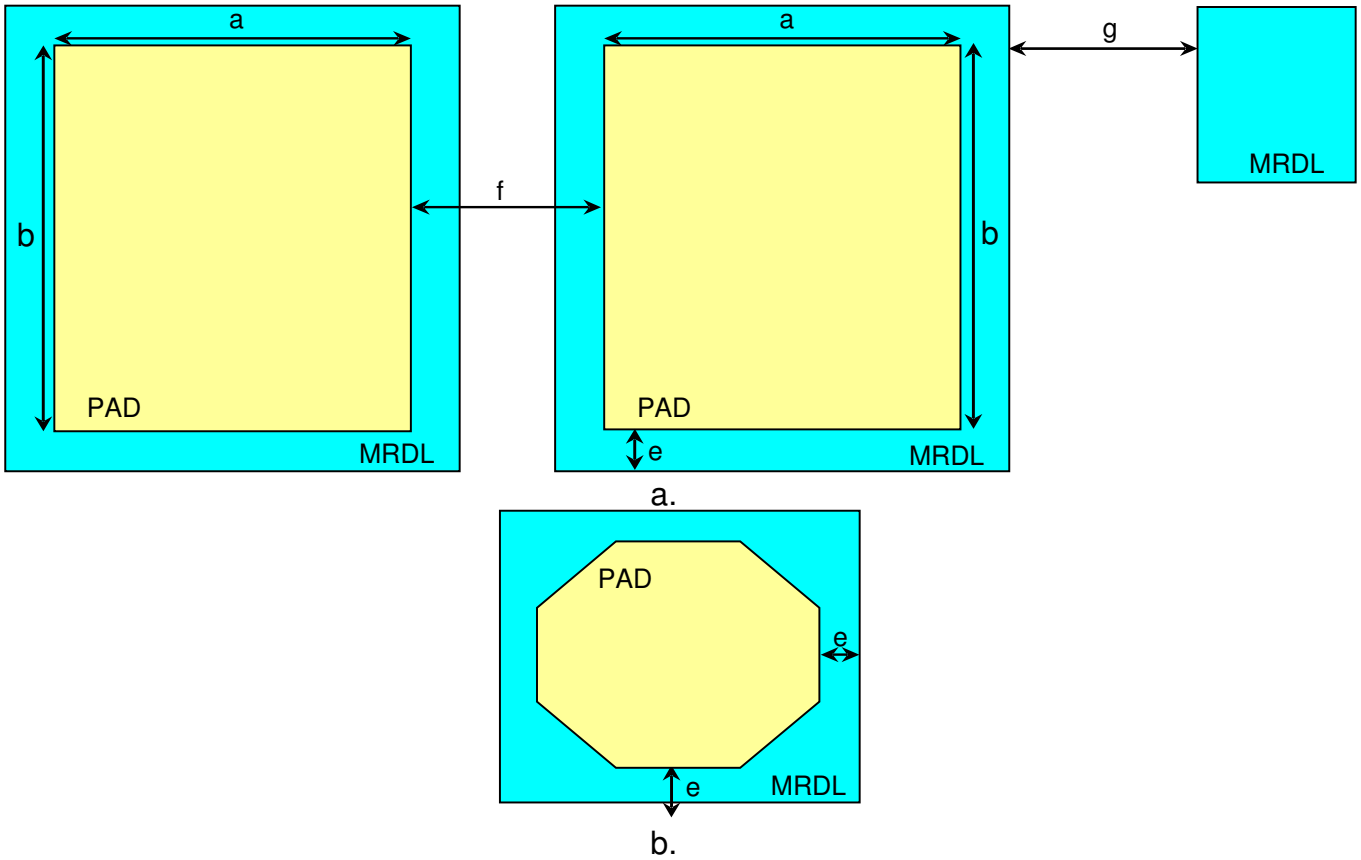


Figure 20. PAD (a. Wire-bond opening, b. Flip-Chip opening)

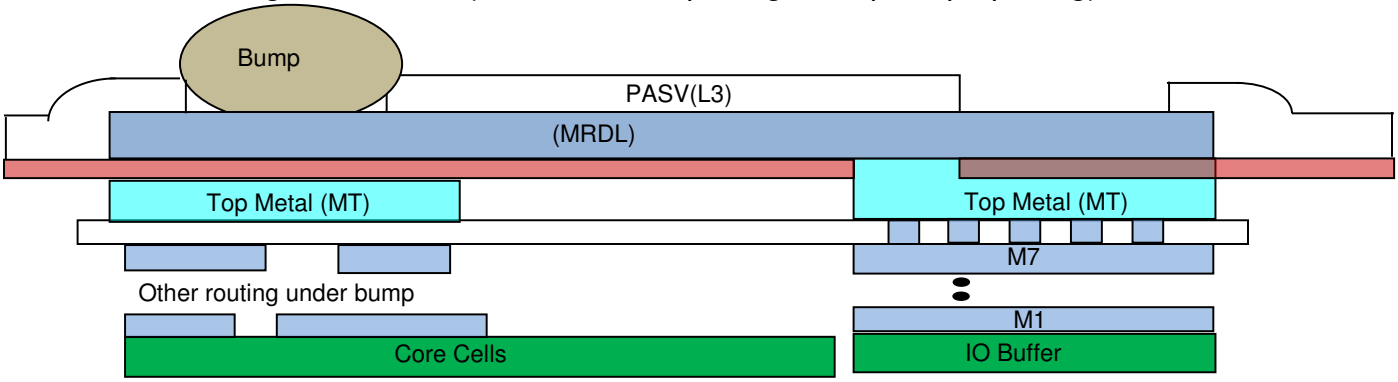


Figure 23. Flip-Chip opening structure

3.3. Antenna rules

Table 26. Antenna Rules

Rule #	Rule description	Minimum Ratio
PO.AN.1	Minimum poly Ratio	250
PO.AN.2	Minimum poly perimeter Ratio	500
CO.AN.3	Minimum Area(CO) / Area(Gate)	4

3.4. Density and fill rules

Table 27. Density Rules, where X=2...8

Rule #	Rule description		Rule
DIFF.DN.1	DIFF density in whole chip	≥	10%
		≤	70%
PO.DN.1	Poly density in whole chip	≥	10%
		≤	45%
M1.DN.1	Minimum metal density over any 130 µm x 130 µm area (checked by stepping in 75 µm increments).		15%
M1.DN.2	Maximum metal density over any 130 µm x 130 µm area (checked by stepping in 75 µm increments).		90%
MX.DN.1	Minimum metal density over any 130 µm x 130 µm area (checked by stepping in 75 µm increments).		25%
MX.DN.2	Maximum metal density over any 130 µm x 130 µm area (checked by stepping in 75 µm increments).		85%

Table 28. Fill Rules

Rule	Description	µm	Mark
FILL_WIDTH	Tile width	0.35	w
FILL_HEIGHT	Tile height	0.7	h
FILL_SPACE	Tile spacing to signal net	0.18	d
SPACE_X/Y	Tile spacing	0.18	dt
STAGGER_DIST	Minimum stagger dist	0.18	sd
PATTERN_WIDTH	Fill pattern width	1	pattern_w
PATTERN_HEIGHT	Fill pattern height	0.9	pattern_h

$$Fill\ ratio = \frac{2 \bullet h \bullet w}{pattern\_w \bullet pattern\_h} = 0.49/0.9 = 0.54$$

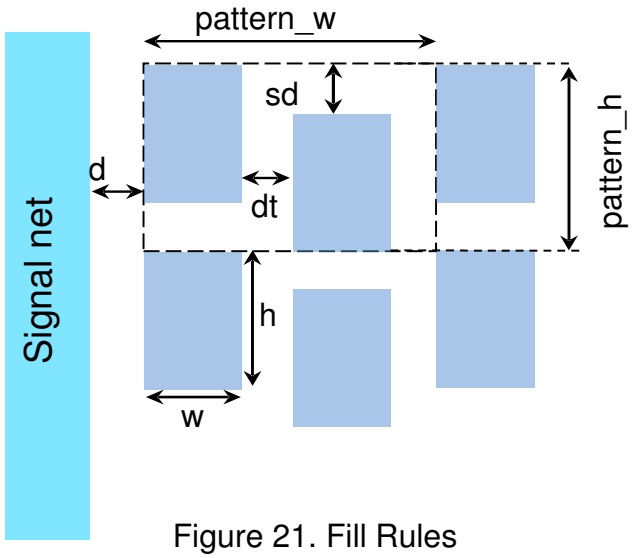


Figure 21. Fill Rules

3.5. Electromigration rules

For DC operation electromigration rules are given by providing I_{max} maximum DC current allowed for conductor with width W. The value of I_{max} is given for 110 ^{0} C temperature depending on layer width W, for other temperatures rating factors F(T) should be used to calculate I_{max}. For example for 125 ^{0} C

$I_{max}(125)=F(125)x\ I_{max}(110),$

Where F(125) is the rating factor for 125 ^{0} C.

Table 29. EM Rating factors (F(T))

Layer(s)	Temperature (°C)						
	95	100	105	110	115	120	125
PO	1.19	1.1	1.05	1	0.93	0.89	0.76
M1, MX, MT	1.55	1.47	1.4	1	0.75	0.55	0.4
MRDL	1.4	1.3	1.2	1	0.8	0.7	0.6

Table 30. Maximum allowed DC current

Rule #	Layer name	I_{max} (mA)
M1.EM.1	M1	0.9 * (W×0.9-0.002)
MX.EM.1	MX	0.9 * (W×0.9-0.002)
MT.EM.1	MT	2 * (W×0.9-0.002)
MRDL.EM.1	MRDL	5 * (W×0.9-0.002)
CO.EM.1	CO	0.1 per contact
VIAX.EM.1	VIAX	0.04 per via
VIAT.EM.1	VIAT	0.08 per via

Table 31. Maximum allowed DC current density for PO

Rule #	Layer name	J_{max} (mA/ µm)
PO.EM.1	PO (width ≤ 2 µm)	5
PO.EM.1	PO (width > 2 µm)	3

For reliability enhancement it is recommended to place VIAs more than it is required by rules.

For AC operation electromigration rules are given for metal layers as maximum allowed AC peak current ($I_{peak} = max(|I(t)|)$) and as a root-mean-square of AC current I_{RMS} ($I_{RMS} = \sqrt{\frac{\int_0^\tau I(t)^2 dt}{\tau}}$). The value of root-mean-square is given for 110 ^{0}C, depending on layer width W, for other temperatures the temperature difference ΔT should be used (for 110 ^{0}C $\Delta T=0$, for 115 ^{0}C $\Delta T=5$, etc.).

Table 32. Maximum allowed AC peak current for metal layers

Rule #	Layer name	I_{peak} (mA)
PO.EM.1	PO not SBLK (saliceded)	1.5 * (W×0.9-0.002)
PO.EM.2	PO and SBLK (unsaliceded)	1 * (W×0.9-0.002)
M1.EM.2	M1	18 * (W×0.9-0.002)
MX.EM.2	MX	9 * (W×0.9-0.002)
MT.EM.2	MT	20 * (W×0.9-0.002)
MRDL.EM.3	MRDL	5 * (W×0.9-0.002)

Table 33. Maximum allowed AC current RMS

Rule #	Layer name	I_{RMS} (mA)
PO.EM.3	PO not SBLK (saliceded)	SQRT[0.1 * ΔT* W×0.9× (W×0.9+0.7)]
PO.EM.4	PO and SBLK (unsaliceded)	SQRT[0.05 * ΔT* W×0.9× (W×0.9+1.4)]
M1.EM.3	M1	SQRT[13 * ΔT* (W×0.9-0.003) ^{2}× (W×0.9-0.003+0.2)/ (W×0.9-0.003)]
MX.EM.3	MX	SQRT[2 * ΔT* (W×0.9-0.003) ^{2}× (W×0.9-0.003+0.2)/ (W×0.9-0.003)]
MT.EM.3	MT	SQRT[13 * ΔT* (W×0.9-0.003) ^{2}× (W×0.9-0.003+0.2)/ (W×0.9-0.003)]
MRDL.EM.3	MRDL	SQRT[5 * ΔT* W×0.9 × (W×0.9+2)]

3.6. Layer physical parameters

Table 34. Conductors

Name	Sheet Resistance	Thickness (nm)
DIFF	0.001	50
PO	15	50
M1	0.1	95
M2	0.1	95
M3	0.1	95
M4	0.1	95
M5	0.1	95
M6	0.1	95
M7	0.1	95
M8	0.1	95
M9	0.28	190
MRDL	0.35	280

Table 35. Dielectrics

Name		Thickness (nm)
GOX	3.9	1.5
FOX	3.9	100
D1	3.9	600
D2	3.9	600
D3	3.9	600
D4	3.9	600
D5	3.9	600
D6	3.9	600
D7	3.9	600
D8	3.9	600
D9	3.9	600
PASS	3.9	3000

3.7. Cross section

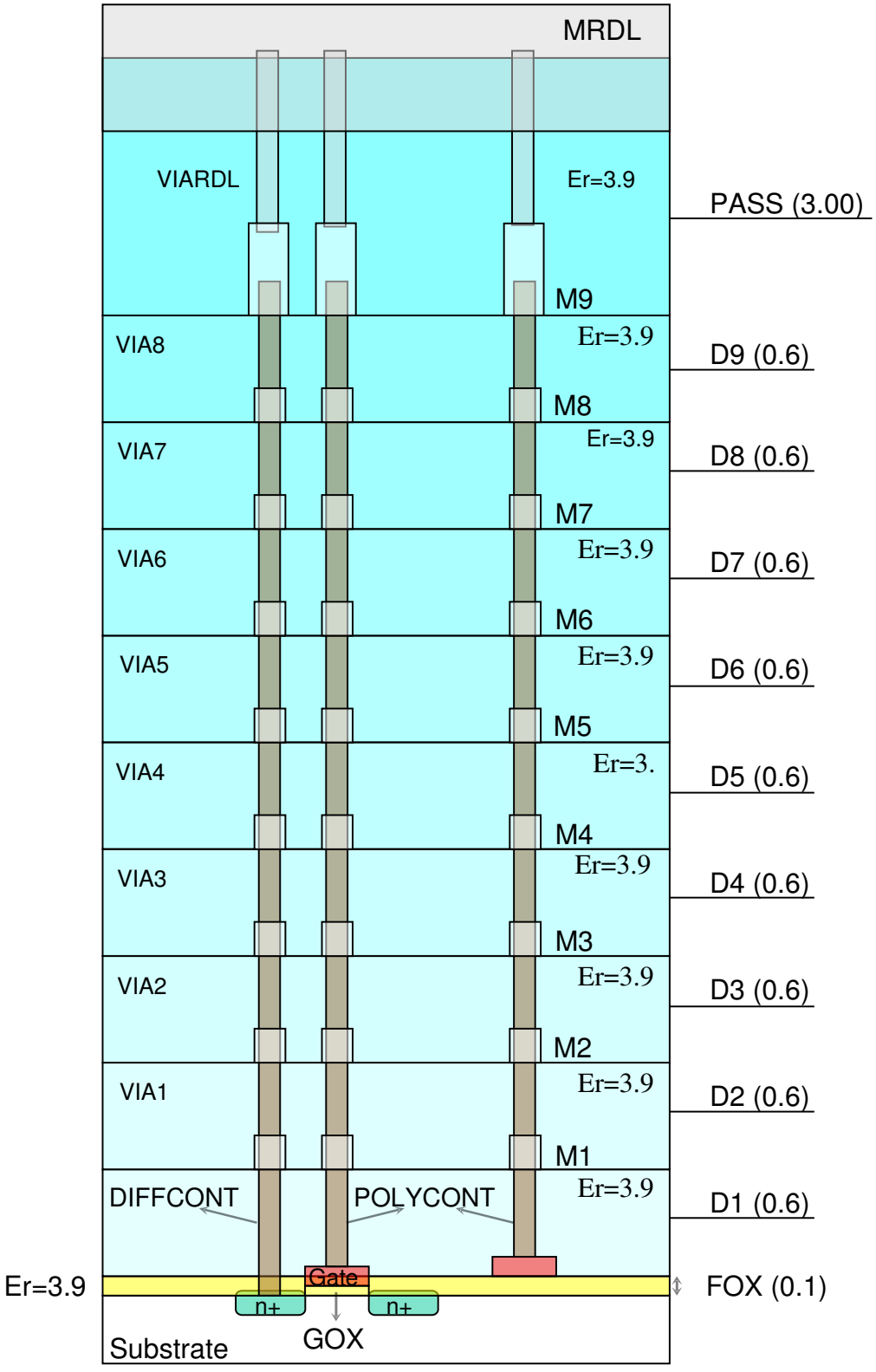


Figure 25. Process Description

4. Revision History

Table 36. Revision History

Revision	Date	Change
A.1.0	29/10/2017	Initial release