SAED 14nm FINFet Device Formation Document

SAED_EDK14_FINFET

Document # : SAED_EDK14_FINFet
Revision : 1.0
Technology : SAED14nm
Process : SAED14nm 1P9M 0.8V/1.5V/1.8V

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1. Introduction

This document is the part of SAED_EDK14 Educational Design Kit documentation. It represents all available devices in SAED14nm 0.8v/1.5v/1.8V Logic process and their formation. These device formation rules are free from intellectual property restrictions.

2. Device Formation

Table 1.FINFETS

#		NFET	PFET
1	0.8V thin oxide standard vth nfet and pfet	n08	n08
2	0.8V thin oxide high vth nfet and pfet	n08_hvt	n08_hvt
3	0.8V thin oxide low vth nfet and pfet	n08_lvt	n08_lvt
4	0.8V thin oxide slow vth nfet and pfet	n08_slvt	n08_slvt
5	1.5V thick oxide nfet and pfet	n15	n15
6	1.8V thick oxide nfet and pfet	n18	n18

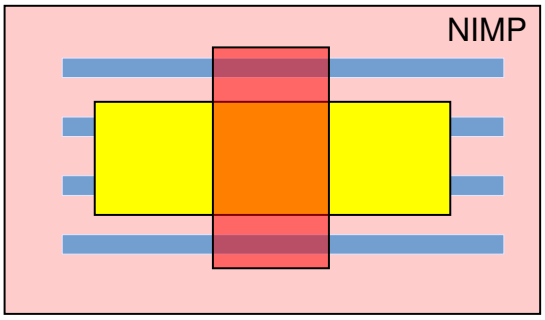

Figure 1. FINFETS: n08

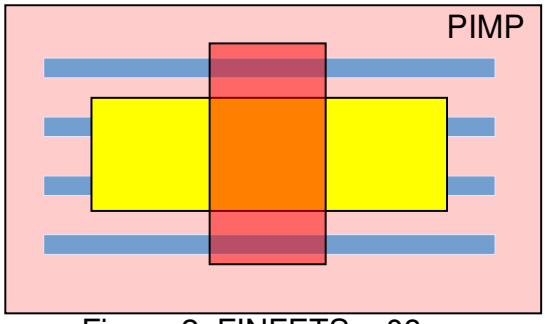

Figure 2. FINFETS: p08

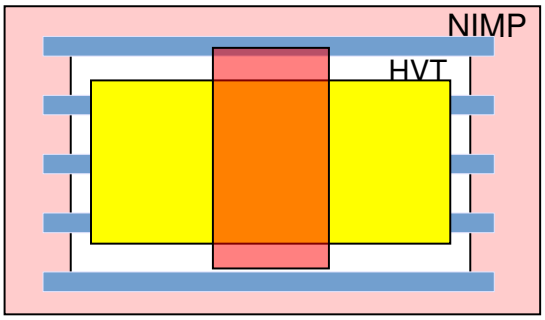

Figure 3. FINFETS: n08_hvt

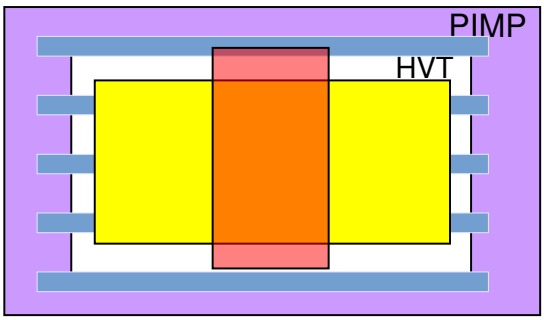

Figure 4. FINFETS: p08_hvt

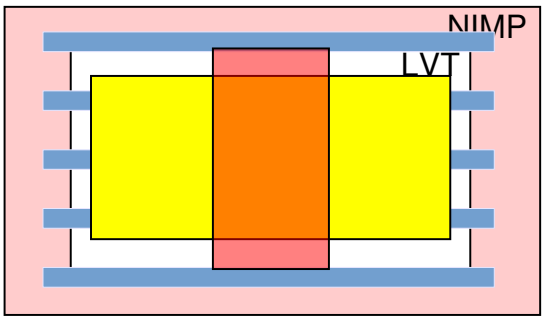

Figure 5. FINFETS: n08_lvt

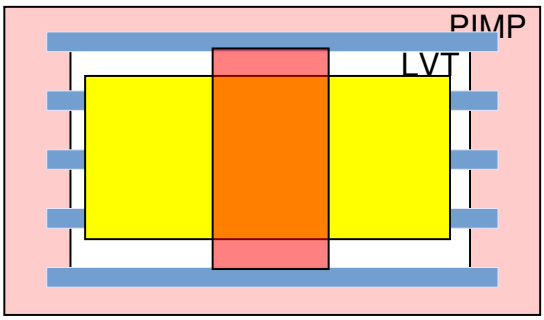

Figure 6. FINFETS: p08_lvt

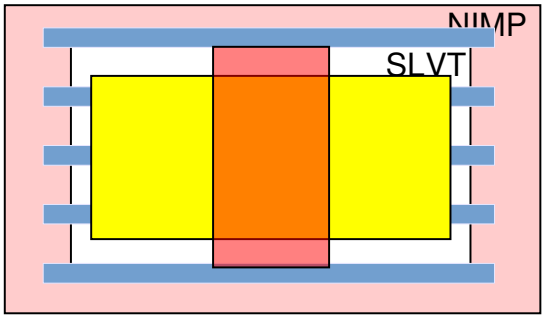

Figure 5. FINFETS: n08_slvt

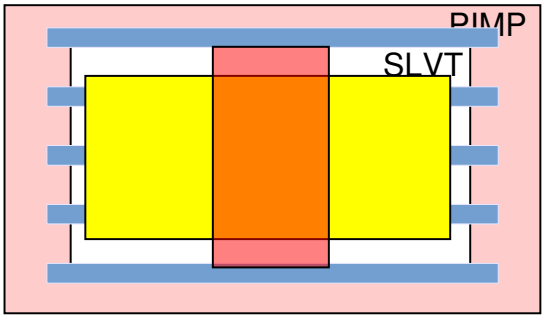

Figure 6. FINFETS: p08_slvt

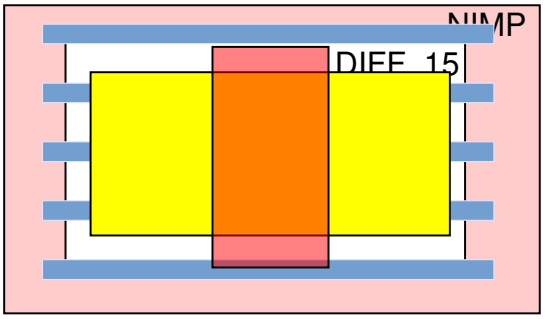

Figure 7. FINFETS: n15

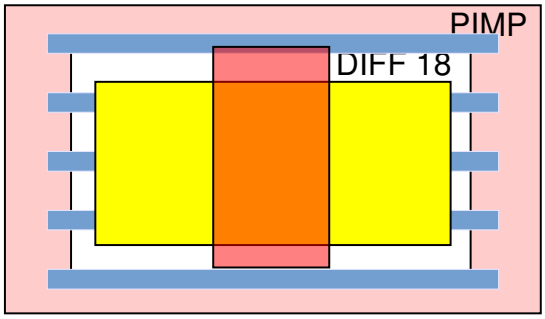

Figure 8.FINFETS: p15

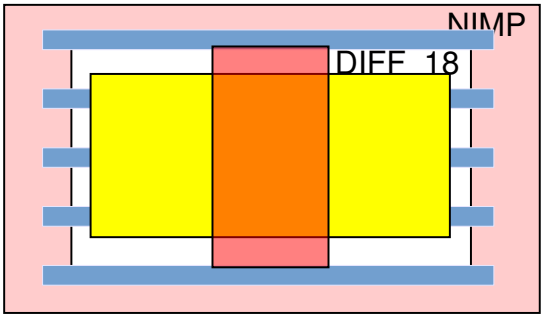

Figure 9.FINFETS: n18

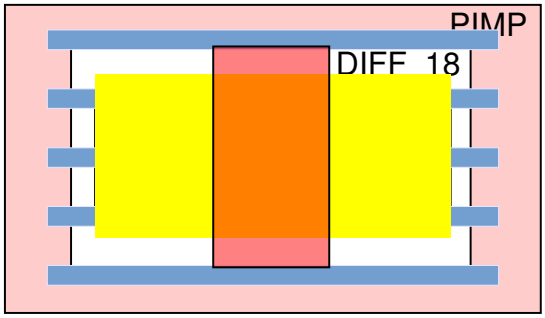

Figure 10. FINFETS: p18

Table 2. Resistors

#	Device description	
1	Poly resistor	rpoly
2	Metal resistor	rmet

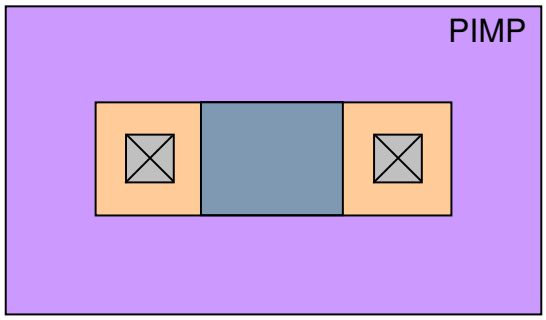

Figure 11. Resistors: rmet

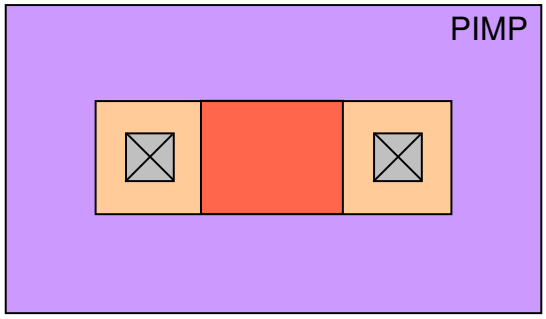

Figure 12. Resistors: rpoly

Table 3. Diodes

#	Rule description	
1	N+/Psub diode	ND
1	P+/Nwell diode	PD

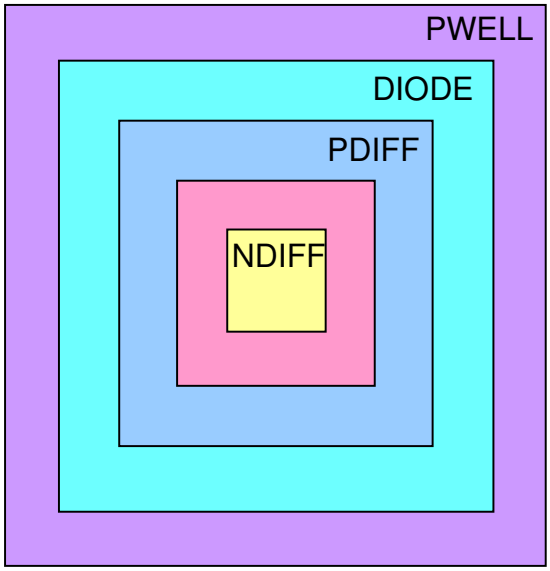

Figure 15. Diodes: ND

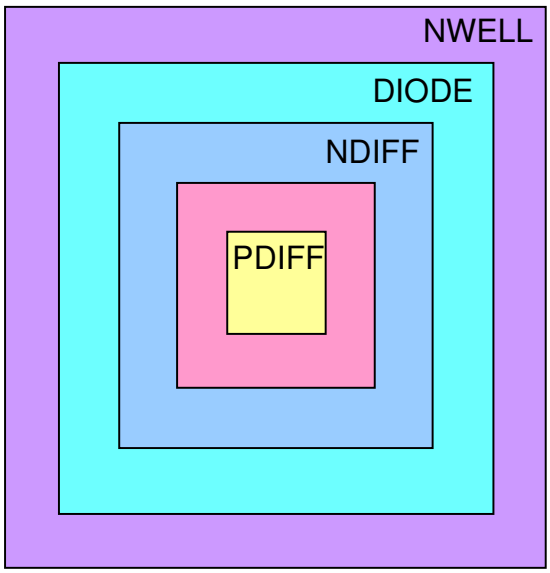

Figure 16. Diodes: PD

4. Revision History

Table 5. Revision History

Revision	Date	Change
A.1	29/10/2017	Initial release