SAED 14nm Spice Model Documentation

SAED_EDK14_TK_SM

Document #: SAED_EDK14_TK_SM
Revision : 1.0
Technology : SAED14nm
Process : SAED14nm 1P9M 0.8v / 1.5v/ 1.8v

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1. Introduction

SPICE model library is the part of SAED_EDK14 Educational Design Kit and this document is the part of SAED_EDK14 Educational Design Kit documentation. It describes the methodology of SPICE model creation and gives the main directions how to use provided files to achieve correct simulation results. Also here is shown the main characteristics of transistors in different operating conditions. These models are obtained from open sources and don't include any confidential or proprietary information of other companies or foundries. However it has characteristics that are similar to those of real foundries (14 nm) for further portability of the projects design by this kit.

1.1. The Structure of Spice Model library

The Spice model library contains following devices, which are also listed in the table below. Addition of additional devices are anticipated.

1. Transistors
   a) 1.8V devices: Thick oxide FinFETs
   b) 1.5V devices: Medium oxide FinFETs
   c) Three type of 0.8V devices: Thin oxide FinFETs
      - standard threshold voltage
      - high threshold voltage
      - low threshold voltage
      - super low threshold voltage

   For each of these devices it is generated five corner models:
   TT - both FinFETs typical,
   FF - both FinFETs fast,
   SS - both FinFETs slow,
   SF - slow_NFET/fast_PFET,
   FS - slow_PFET/fast_NFET.
2. Diode
3. Poly Resistor
4. Bipolar junction transistor (BJT)

Table 1.1.The list of devices of spice model library

Device name	Model name
PFET 0.8V standard VTH device	p08
NFET 0.8V standard VTH device	n08
PFET 0.8V high VTH device	p08_hvt
NFET 0.8V high VTH device	n08_hvt
PFET 0.8V low VTH device	p08_lvt
NFET 0.8V low VTH device	n08_lvt
PFET 1.8V device	p18
NFET 1.8V device	n18
PFET 1.5V device	p15
NFET 1.5V device	n15
N+/Psub diode	nd/pd
N poly resistor	rnpoly
P poly resistor	rppoly
VPNP 0.8V device	pnp

1.2. Transistors

1.2.1. 0.8V Thin Oxide FinFETs

As this kit proposed to be used in the low power design and it is aimed to implement the advanced low power design techniques (e. g. multivoltage/multithreshold design digital libraries), the design kit also includes low voltage multi-threshold devices. The 0.8V standard threshold voltage devices are created using the Predictive Technology Model developed by Nanoscale Integration and Modeling (NIMO) Group (http://ptm.asu.edu/). It is taken the typical corner of 14nm process from Latest Models, suggested by NIMO. The high and low threshold devices are obtained by changing the threshold voltage of original (svt) devices by 20%. FF, SS, SF and FS corners are formed by changing the threshold voltage (vth0) and oxide thickness (tox) in the range of +/-5%.
Below it is presented the transfer curves of 0.8V NFET and PFET devices.

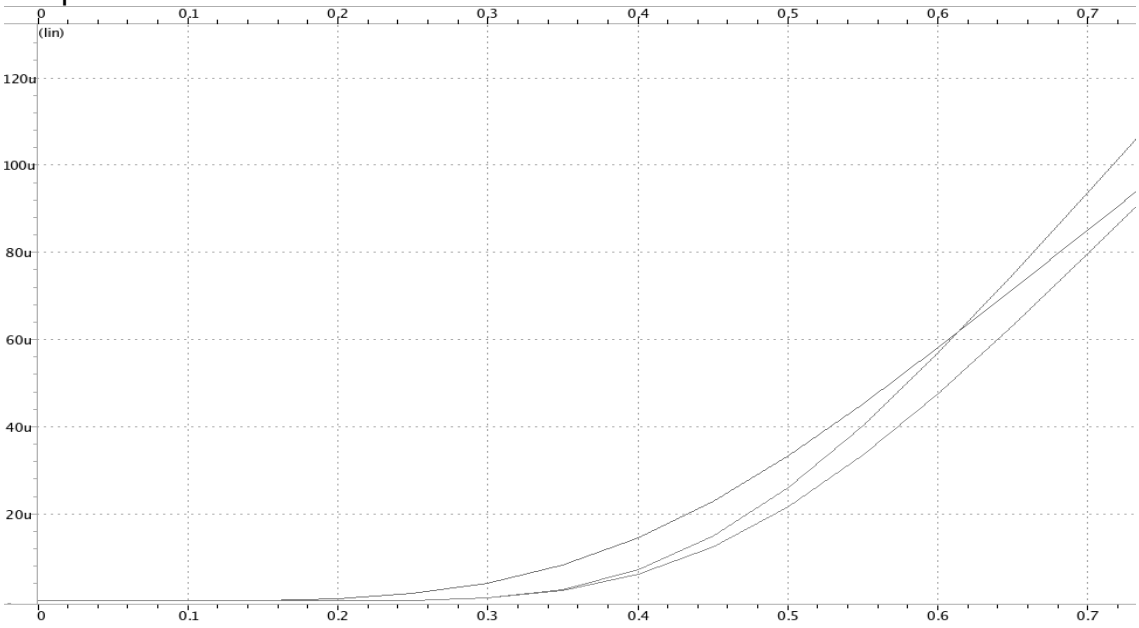

Figure 1.1. TT, FF and SS corners of 0.8V Thin oxide Standard Vth NFET

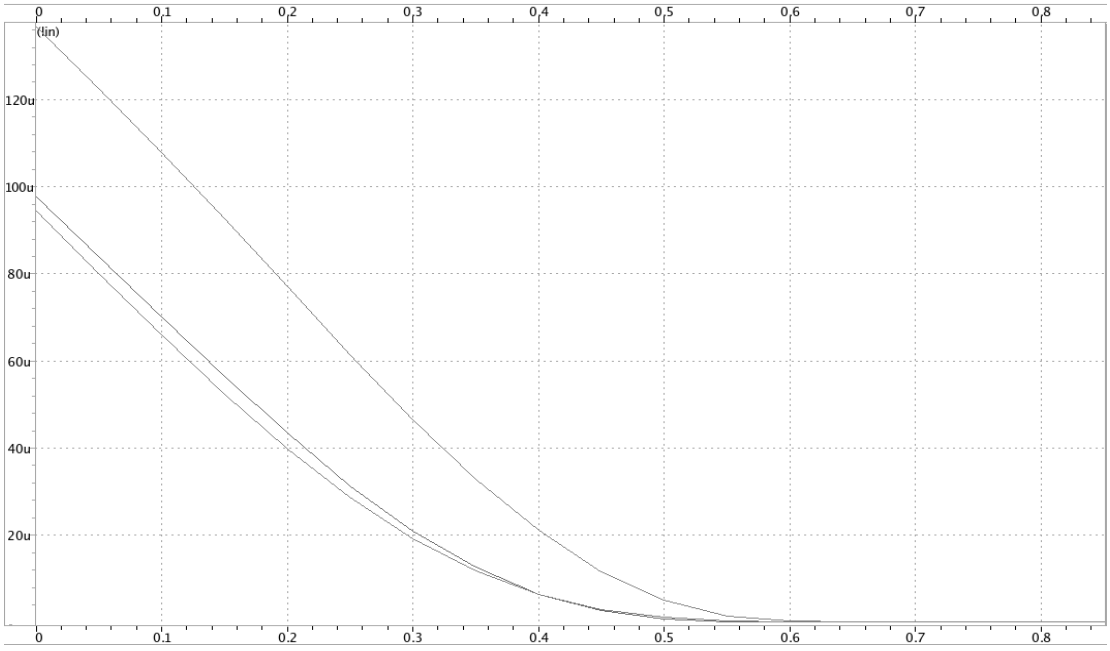

Figure 1.2. TT, FF and SS corners of 0.8V Thin oxide Standard Vth PFET

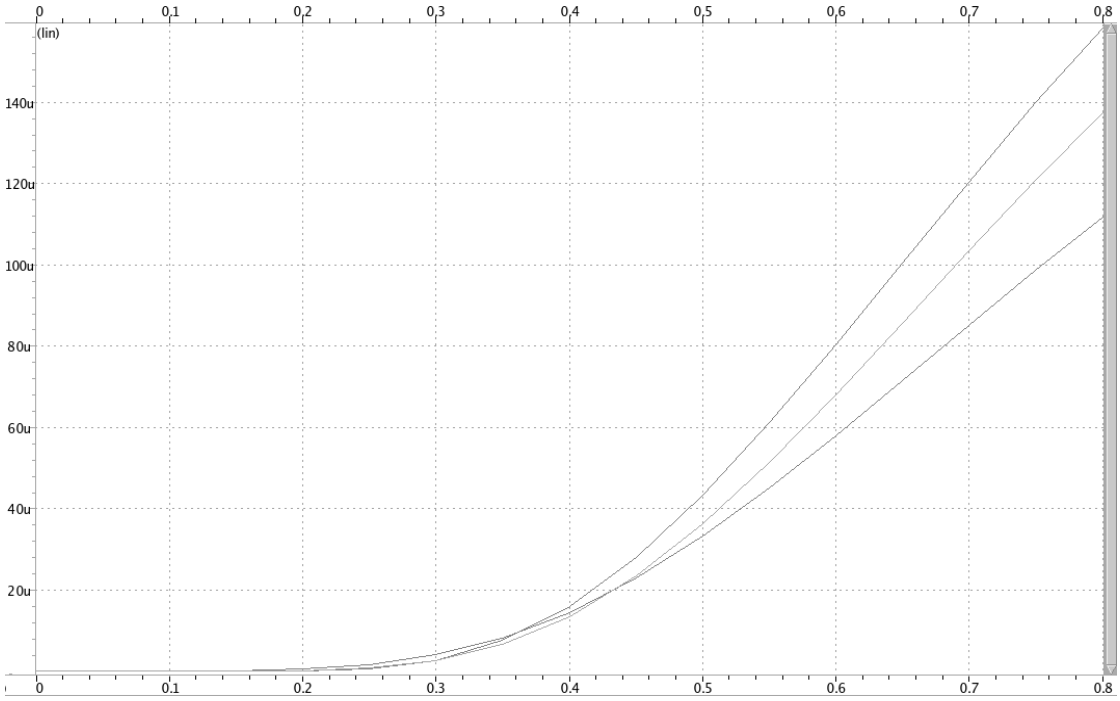

Figure 1.3. TT, FF and SS corners of 0.8V Thin oxide High Vth NFET

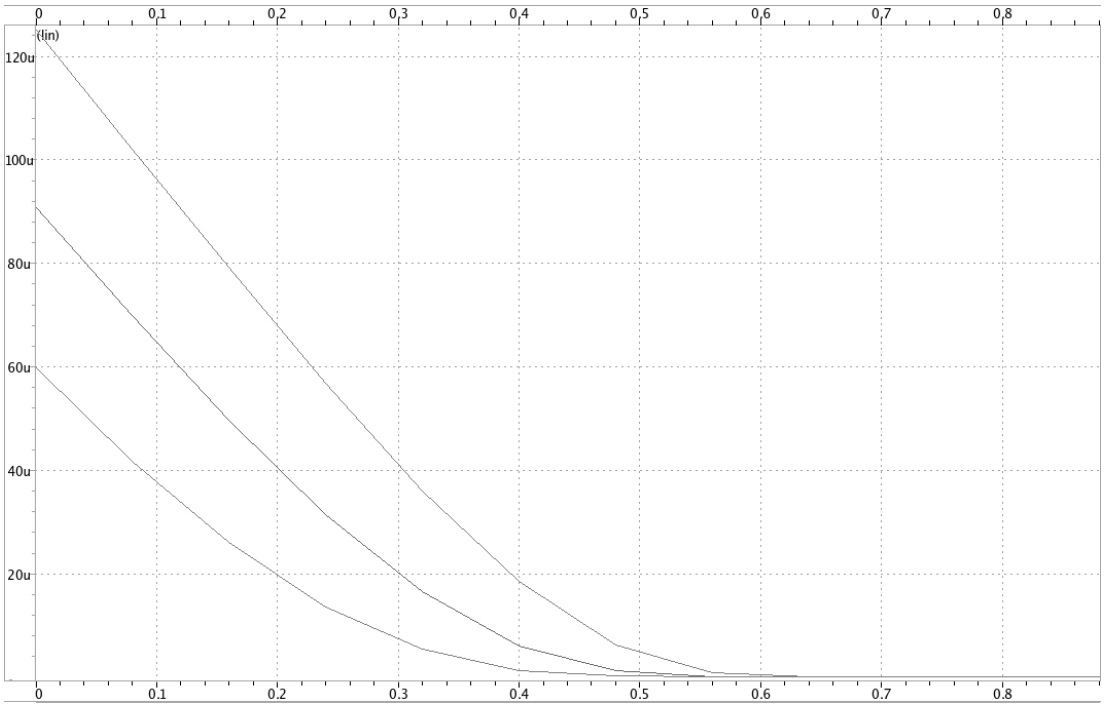

Figure 1.4. TT, FF and SS corners of 0.8V Thin oxide High Vth PFET

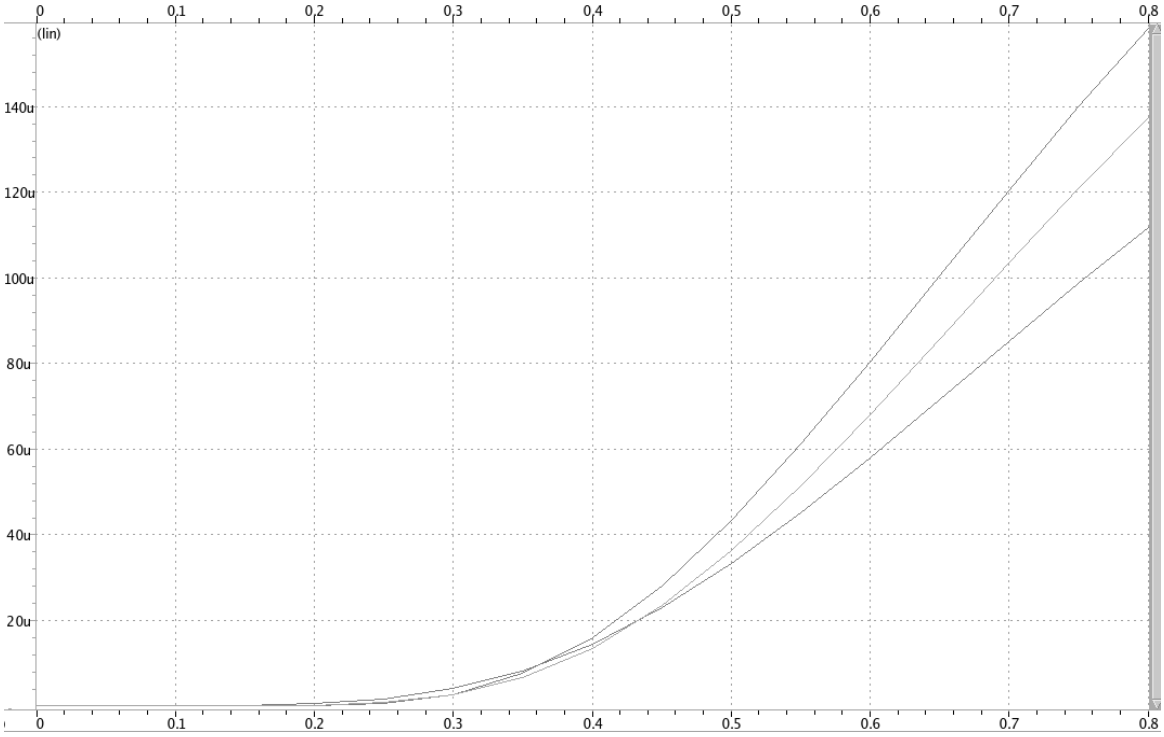

Figure 1.5. TT, FF and SS corners of 0.8V Thin oxide Low Vth NFET

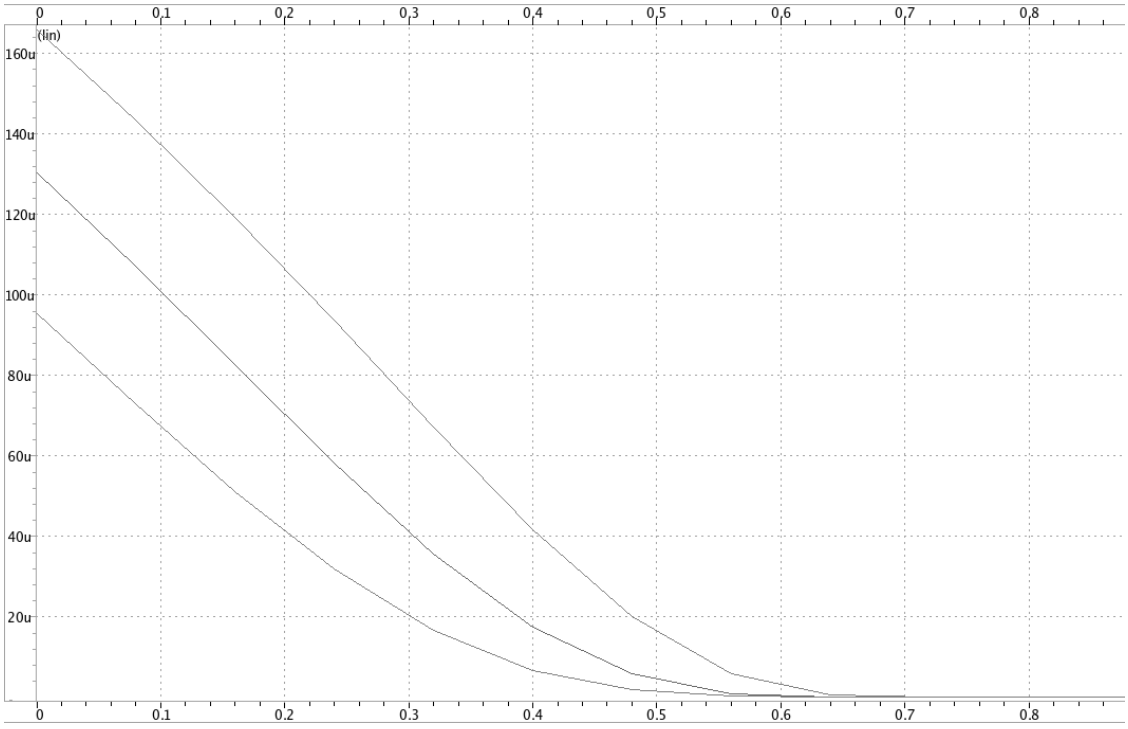

Figure 1.6. TT, FF and SS corners of 0.8V Thin oxide Low Vth PFET

As the purpose of these 0.8V devices are mainly to reduce the power consumption of the design by using different Vth transistors for particular applications. Table below represents cutoff currents for all types of 0.8V devices.

Table 1.2. Cutoff currents for standard and low Vth devices
for (TT, FF and SS corners. L/W=0.03u/0.3u)

	FF, -40 (nA)	TT, 25 (nA)	SS, 125 (nA)
n08_hvt	0.009	0.0163	0.465
p08_hvt	0.040	0.03692	0.315
n08	0.00683	0.0293	1.97
p08	0.03621	0.03968	4.08
n08_lvt	0.0266	0.169	2.3
p08_lvt	0.0528	0.43	5.054
n08_slvt	0.197	0.55	5.24
p08_slvt	0.93	2.923	16.68

1.2.2. 1.5V Medium and 1.8V Thick Oxide FinFETs

Simulations were done for model parameters obtained from all lots given in MOSIS for SAED_EDK14nm and have been modified to match with the characteristics of 14nm devices known from open sources [1, 2, 3]. The bunch of DC transfer curves was obtained and the middle curve from the bunch was chosen as a typical corner for 1.5V and 1.8V devices, thereby being assured that it will be closer to the real process for further chip implementation.

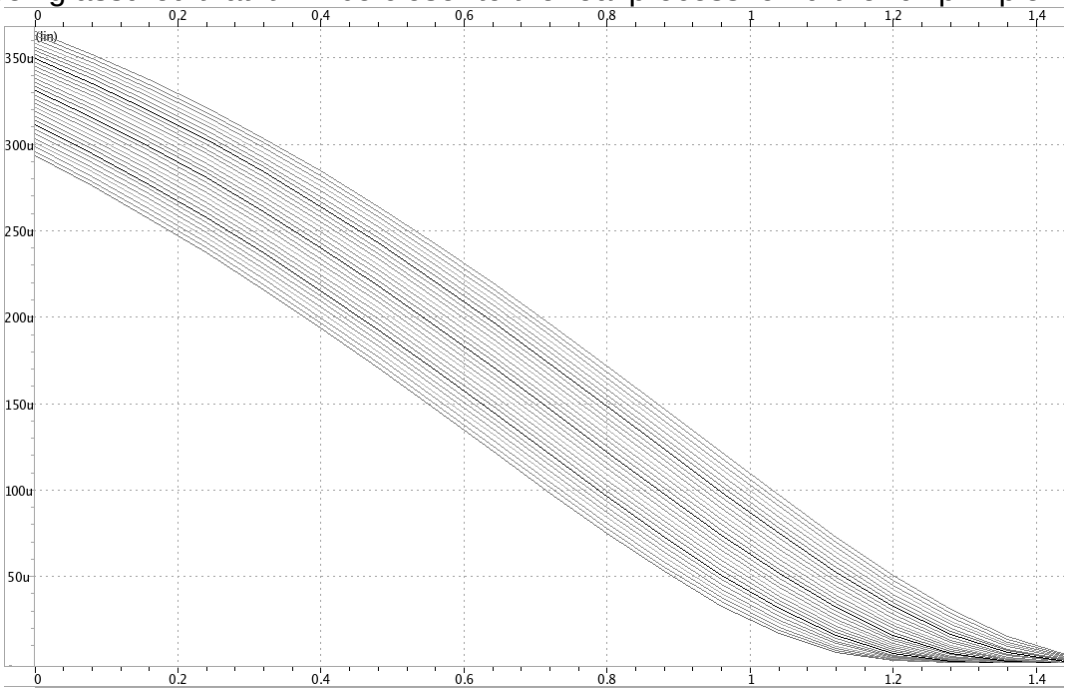

Figure 1.7. Bunch of transfer curves for PFET models

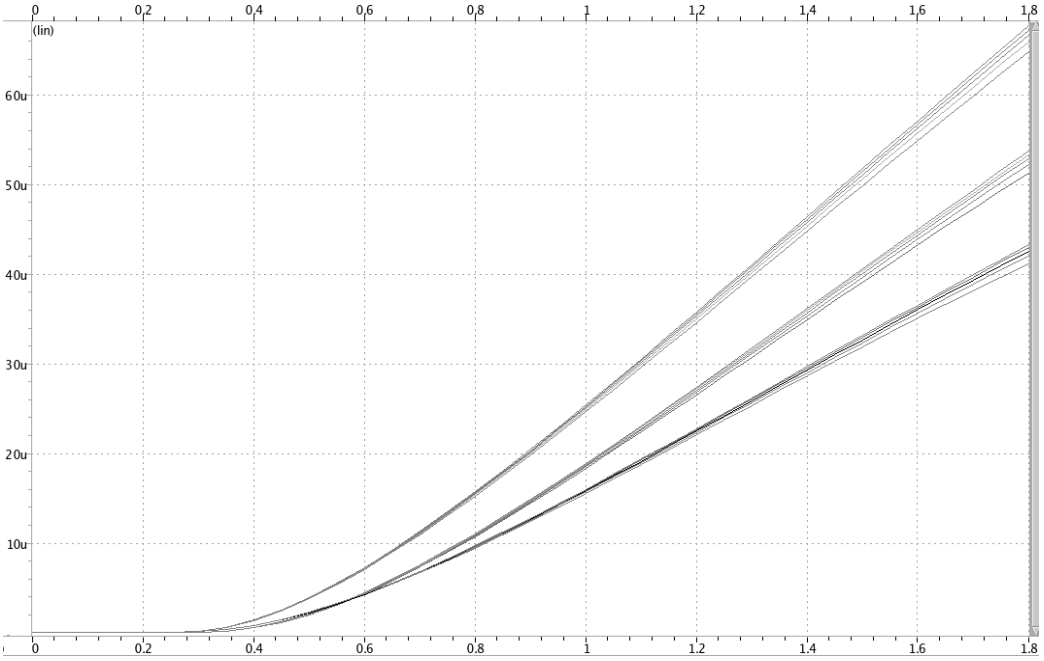

Figure 1.8. Bunch of transfer curves for NFET models

FF, SS, SF and FS corners are formed by changing the threshold voltage (vth0) and oxide thickness (tox) in the range of +/-5%. Below it is presented the transfer curves of 1.5V PFET and NFET devices.

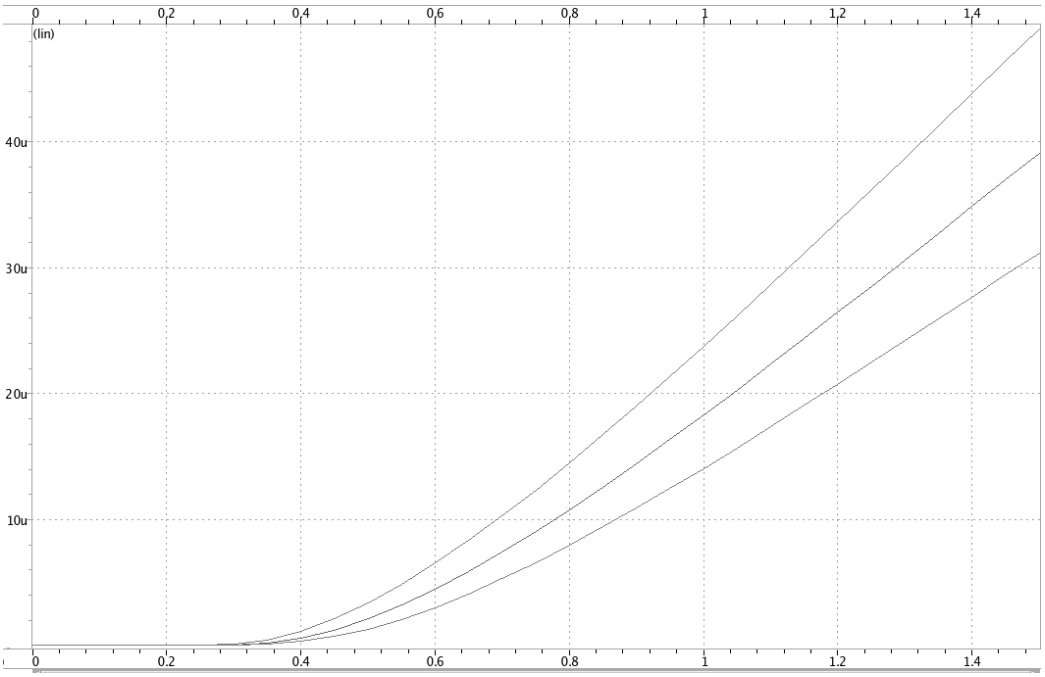

Figure 1.9. TT, FF and SS corners of 1.5V medium oxide NFET

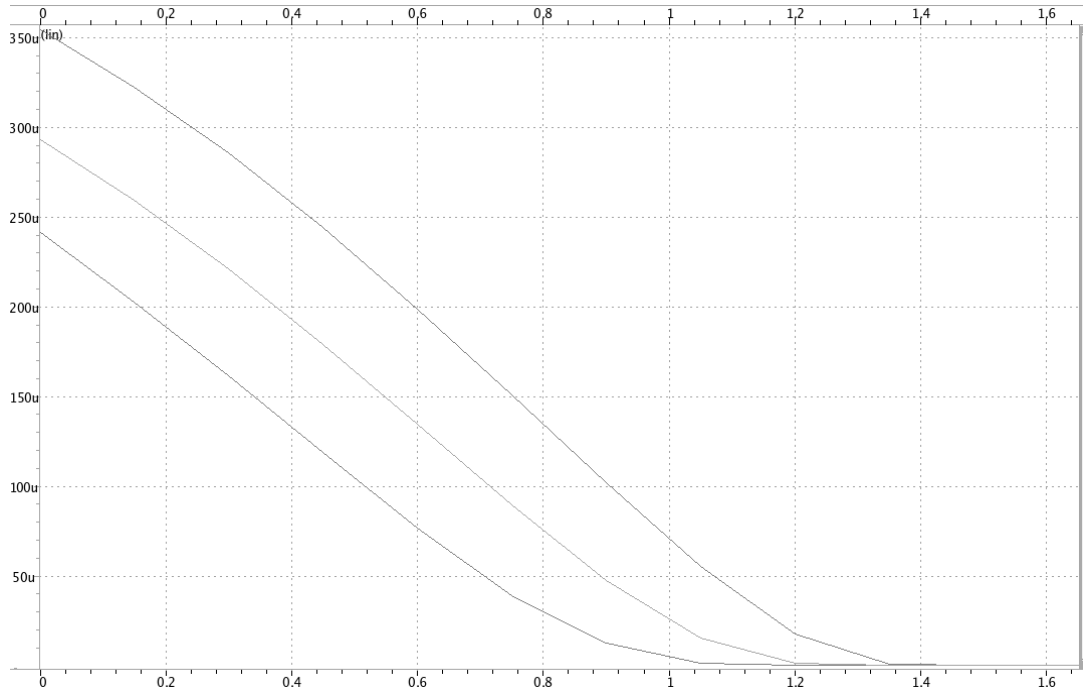

Figure 1.10. TT, FF and SS corners of 1.5V medium oxide PFET

FF, SS, SF and FS corners are formed by changing the threshold voltage (vth0) and oxide thickness (tox) in the range of +/-5%. Below it is presented the transfer curves of 1.8V PFET and NFET devices.

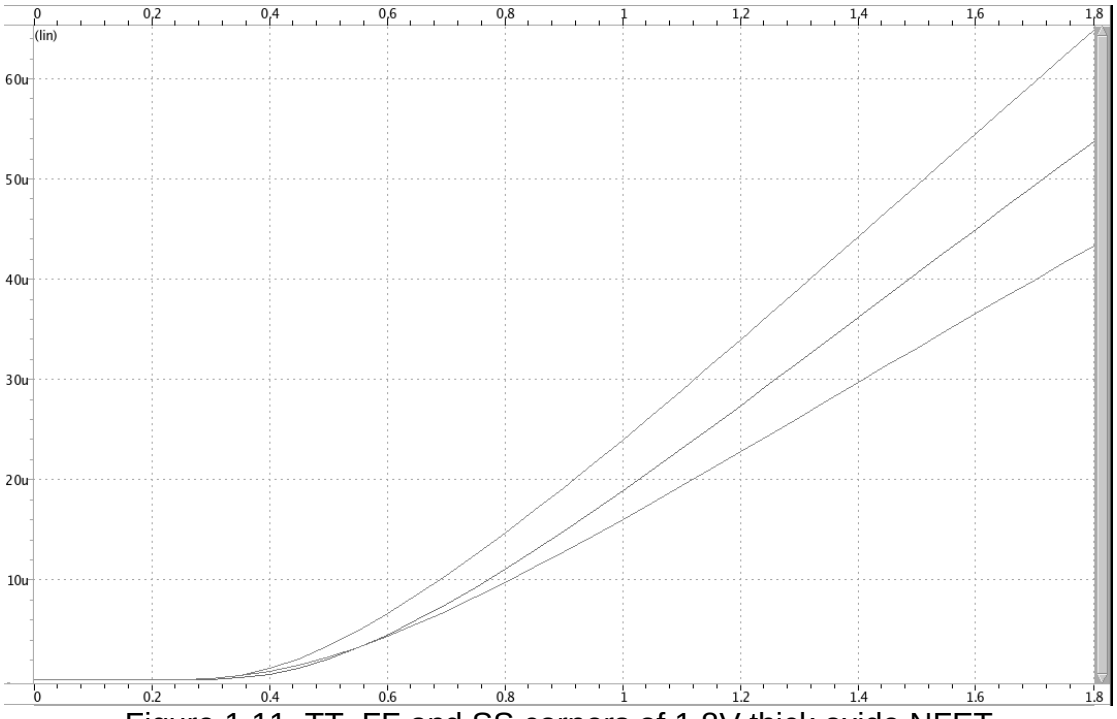

Figure 1.11. TT, FF and SS corners of 1.8V thick oxide NFET

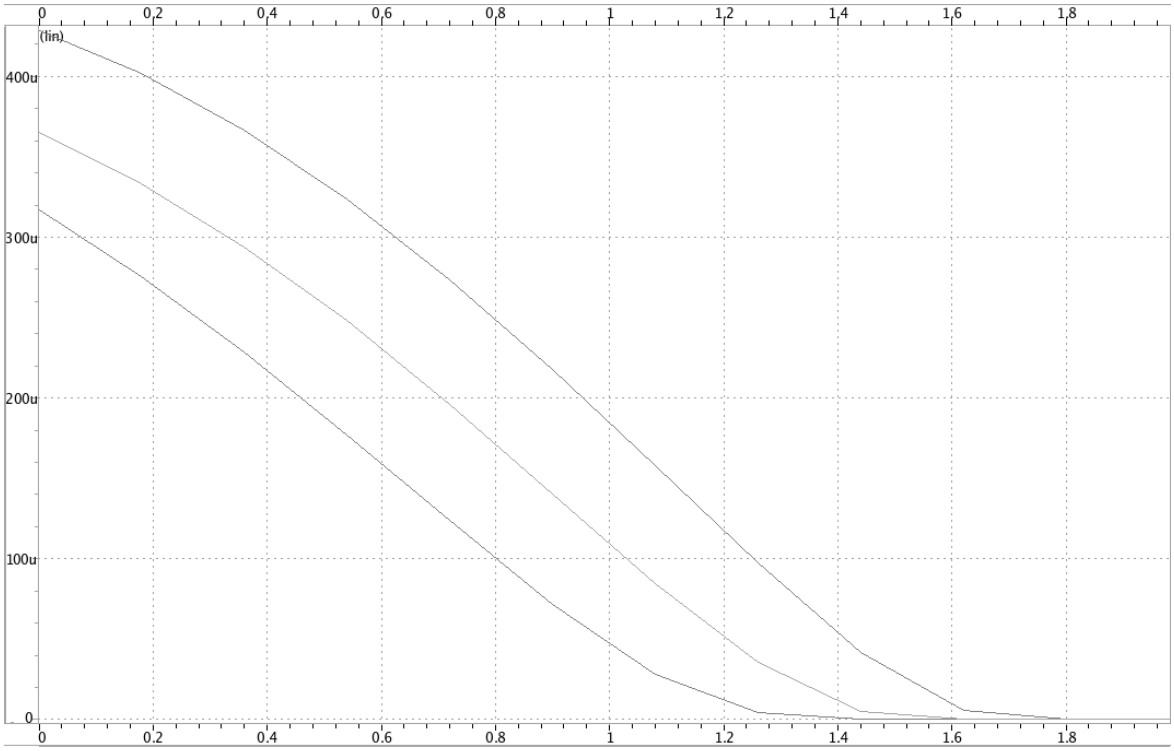

Figure 1.12. TT, FF and SS corners of 1.8V thick oxide PFET

1.3. Diode Model

The N+/Psub diode model is obtained from the HSPICE documentation. The I/V characteristics for diode different areas are shown in figure 1.14.

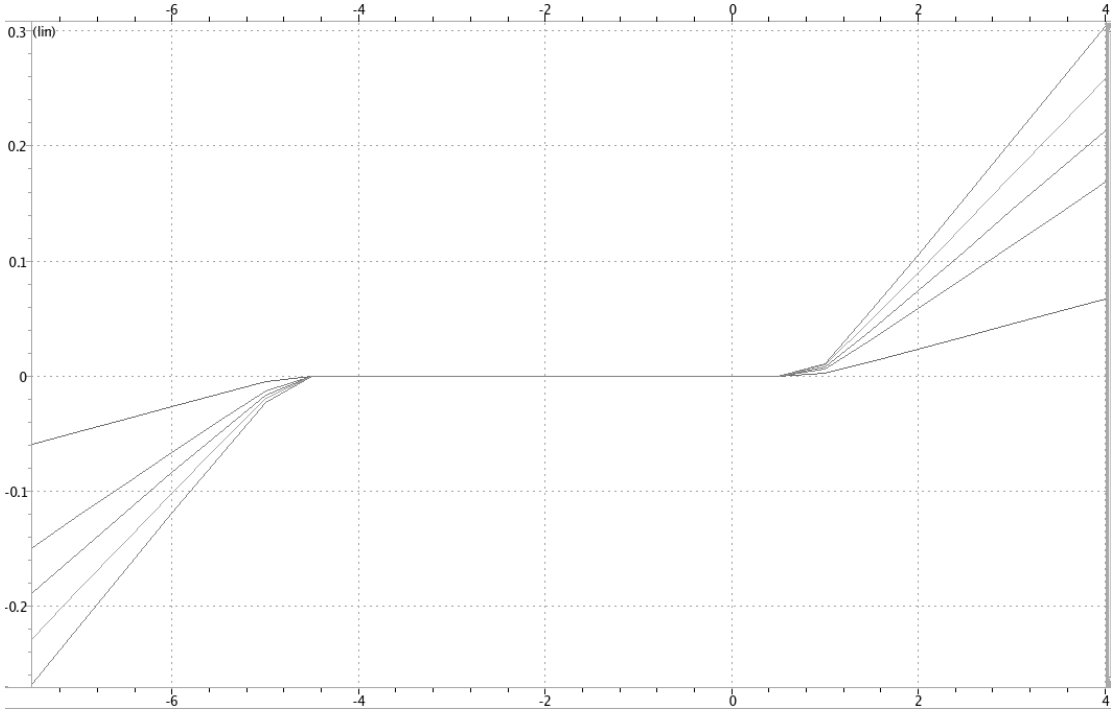

Figure 1.13. I/V characteristic is shown with different areas of diode

Model Usage

To do simulations using the suggested models, it is needed to:
call the model library using following template

```
*Spice netlist
.lib "../path_to_spice_model/saed14nm.lib" CORNER_NAME
```

As models are defined using SPICE .subckt constructs, devices should be instantiated as subcircuit instances i.e.:

```
xm1 d g s b n08
xr1 a b rpoly
```

Table 0.1. SAED14nm model names

Device type	Device	Model name	Available corner names
Thin Oxide (0.8V) standard vth	NFET	n08	TT, SS, FF, SF, FS
	PFET	p08	
Thin Oxide (0.8V) low vth	NFET	n08_lvt	
	PFET	p08_lvt	
Thin Oxide (0.8V) high vth	NFET	n08_hvt	
	PFET	p08_hvt	
Medium Oxide (1.5V)	NFET	n15	
	PFET	p15	
Thick Oxide (1.8V)	NFET	n18	
	PFET	p18	
BJT (0.8 V)			
	VPNP	pnp	
N P poly	-	rnpolyl rppolyl	
diode is N+/Psub	-	nd/pd	

References

1 P. Packan et al., “High Performance 32nm Logic Technology Featuring 2nd Generation High-k + Metal Gate Transistors”, IEEE International Technical Digest Electron Devices Meeting (IEDM), pp659-662, 2009

2 C. H. Diaz et al., “32 nm gate-first high-k/metal-gate technology for high performance low power applications”, in Proc. IEEE IEDM Tech. Dig., San Francisco, USA, 2008, pp. 629–632.

3 F. Arnaud et al., "32nm General Purpose Bulk CMOS Technology for High Performance Applications at Low Voltage," IEDM Tech. Dig., pp. 633-636, 2008.

4 R.J. Baker, Hary W.Li, David E. Boyce. “CMOS: Circuit Design, Layout, and Simulation.”, 2010

2. Revision History

Table 2.1. Revision History

Revision	Date	Change
A.1	17/11/2011	Initial release