SAED 14nm FinFET
PROCESS DESIGN KIT

SAED_PDK14_FinFET

SPECIFICATION

Document #: SAED_PDK14_FinFET
Revision : 1.0
Technology : SAED14nm FinFET
Process : SAED14nm FinFET 1P9M 0.8v/1.5v/1.8v

CONTENTS

LIST OF TABLES

1. Introduction

1.1. Goal of PDK development

This document describes possibilities, peculiarities of SAED_PDK14_FinFET Process Design Kit and technical parameters of Symbol library and OA Python PCELLs included in it.
SAED_PDK14_FinFET is free from intellectual property restrictions and is oriented at Synopsys Custom Compiler (CC) tool.
SAED_PDK14_FinFET is anticipated for the use of educational purposes and is aimed at training highly qualified specialists in microelectronics at:

- Synopsys Customer Education Services and Global Technical Services
- Universities included in Synopsys University Program

SAED_PDK14_FinFET is foreseen to support the trainees to better master:

- Advanced Analog Design Methodologies;
- Capabilities of SYNOPSYS Custom Compiler and other EDA tools.

For the use of PDK it is assumed that European or North American bundle of SYNOPSYS EDA tools, including CC is available to trainees.

SAED_PDK14_FinFET Process Design Kit is anticipated for designing different analog integrated circuits (ICs) or IPs by the application of 14nm FinFET technology and SYNOPSYS EDA tools.

1.2. Content of PDK

The content of SAED_PDK14_FinFET is shown in Table 1.1.

Table 1.1 Content of SAED_PDK14_FinFET

Name	Directory	Extension	Description
Technology files	./techfiles/	.tcl, .tf, .map	The technology file and display resource files
Physical verification files	./icv/drc ./icv/lvs ./icv/antenna ./icv/density ./icv/fill	*.rs	The DRC, LVS, Antenna and density rule runset files and dummy fill file.
Parasitic Extract files	./starrc/	.nxtgrd, .itf, .map, .cmd	Parasitic Extract files for StarRC
Symbol library and OA Python Pcells	./SAED_PDK_14_FinFET/	(OpenAccess database)	Symbols and OA Python Pcells
Standard Symbol Library	./sym_libs	(OpenAccess database)	Standard symbols library from Si2
Sample designs	./reference	(OpenAccess database)	Few sample designs done with this PDK
HSpice models	./hspice/	.lib	The HSPICE models, including MonteCarlo models
Documentation	./documentation/	.pdf	Device formation documentation Design Rule Manual (DRM) PDK documentation (this file) Spice models documentation
Scripts	./scripts/callbacks ./scripts/common	.tcl	Callback scripts for user input validation and common procedures.
Setup files	./install	.sh, lib.defs	Installation script and Custom Compiler lib.defs file

1.3. Methodology of getting PDK components

For design of SAED14nm FinFET Process Design Kit, abstract technology, simulation models will be generated using the Predictive Technology Model (PTM) developed by the Nanoscale Integration and Modeling Group (NIMO) of Arizona State University (ASU) (http://ptm.asu.edu/).

Layout design rules for SAED14nm_FinFET educational, abstract technology should be obtained by considering lithography requirements and restrictions for 14nm FinFET technology. Parasitics extraction deck will be formed using the models of parasitics estimation developed by NIMO group of ASU. Double patterning rules and also 14nm FinFET advanced rules supported by Synopsys IC Compiler Zroute router will be added.

All SPICE model parameter values in device description sections are used to illustrate the instantiation of devices. Part of the values are widely known values from literature and open

materials, the other part of the values are approximate values used as placeholders for illustration purposes only.

Process Design Kit SAED_PDK14_FinFET will support key processes as GF14nm and SEC14nm in the sense of support of double patterning and usage of contactless metal.

SAED_PDK14_FinFET Technology files will be generated according to SAED14nm_FinFET 1P9M 0.8v/1.5v/1.8v technology [1] and OpenAccess [2] format specification.

The SAED_PDK14_FinFET PyCells will be based on IPL 1.0 standard (http://iplnow.com).

2. SAED_PDK14_FinFET Components

SAED_PDK14_FinFET will contain technology files, physical verification runsets, parasitic extraction files, HSPICE models, PCells, symbol library and Scripts directories.

2.1. Technology files

Technology files will include technology, display resource files and layer map files.

2.1.1. Technology file

This file is for library creation for generic process, which will contain layer information and design rule definition.

2.1.2. Display resources

This file will contain color, fill and stipple patterns for all the packets used in the technology file in CC format.

2.1.3. Layer map file

This file will map the layer names with the layer purpose, layer number, layer data type and stipple patterns used to describe the layout for the layout editor, DRC, LVS and parasitic extraction tools.

2.2. Physical verification files

Physical verification files will include IC Validator DRC and LVS runset files. DRC Runset file is a command file used by the DRC software program that analyzes the data in the layout and checks design rule violations. LVS runset is a command file used by the LVS software program that extracts the intended devices and their parameters to compare with schematic netlists.

2.3. Parasitic extraction files

Parasitic extract files are used by the parasitic extraction software program that extracts parasitic capacitance, resistance and/or inductance from circuit layout. Parasitic extraction files will be given in StarRC format.

- *.nxtgrd is a database containing capacitance, resistance, inductance and layer information which can be encrypted.
- The Interconnect Technology Format (*.itf) is a file which will contain specification of each layer's content.
- *.map file maps the devices extracted by StarRC with the interoperable Pcells to be used for each device in the StarRC view produced after running StarRC.

2.4. HSPICE Models

HSPICE models that will be used during simulation of the circuits.

2.5. Scripts' directory

Contains callback scripts for validating user input and scripts with common procedures

2.6. Design environment setup files

SAED_PDK14_FinFET Process Design Kit will contain scripts for environment setup which will assure correct operation of all the components.

3. Supported devices

3.1. FinFETs

SAED_PDK14_FinFET will contain FinFETs which have 4 terminals. Length and width are given in nanometers and areas are given in square nanometers. Design variables are anticipated for length and width entries. The parameters of area for diffusion are calculated from the width and the number of used fingers. The width per finger is calculated by dividing the width by the number of fingers. This parameter is viewed by the designer.

Table 3.1 FET list

Spice models name	Description
nfet	nfet 4 terminal (D G S B) mosfet transistor 0.8 volt
nfet_15	nfet 4 terminal (D G S B) mosfet transistor 1.5 volt
nfet_18	nfet 4 terminal (D G S B) mosfet transistor 1.8 volt
nfet_hvt	nfet 4 terminal (D G S B) high threshold voltage mosfet transistor
nfet_lvt	nfet 4 terminal (D G S B) low threshold voltage mosfet transistor
nfet_slvt	nfet 4 terminal (D G S B) superlow threshold voltage mosfet transistor
pfet	pfet 4 terminal (D G S B) mosfet transistor 0.8 volt
pfet_15	pfet 4 terminal (D G S B) mosfet transistor 1.5 volt
pfet_18	pfet 4 terminal (D G S B) mosfet transistor 1.8 volt
pfet_hvt	pfet 4 terminal (D G S B) high threshold voltage mosfet transistor
pfet_lvt	pfet 4 terminal (D G S B) low threshold voltage mosfet transistor
pfet_slvt	pfet 4 terminal (D G S B) superlow threshold voltage mosfet transistor

Table 3.2 FET symbol parameters

Parameters	Description
model	HSpice model
lvs_model	LVS model
nfin	Number of fins
l	Length of each finger
wdiff	Width of diffusion
nf	Number of fingers of gate
m	Multiplicity factor to place number of parallel devices
Fin pitch	Sum of fin width and fin to fin distance

3.2. Resistors

The resistors in the library will consist of poly resistor and metal resistor, which have 3 terminals. All parameters entered into the resistor must be integers or floating-point numbers. No design variables are supported due to calculations that must be performed on the entries. The width and length are snapped to grid, and the resistances are recalculated and updated on the component form based on actual dimensions.

Table 3.3 Resistor list

Spice models name	Description
rmet	3 terminal (A B BULK) metal resistor
rpoly	3 terminal (A B BULK) poly resistor

Table 3.4 Resistor symbol parameters

Spice Model	HSpice model name
lvs_model	LVS model
model	HSpice model
r	Resistance
w	Resistor width
l	Resistor length
m	Multiplicity factor to place number of parallel devices

3.3. Diodes

The diodes in the PDK library will consist of two types which have 2 terminals.

Table 3.5 Diode Spice models list

Spice models name	Description
nd	N+ 2 terminal (PLUS MINUS) diode
pd	P+ 2 terminal (PLUS MINUS) diode
nd_TO	Thick oxide N+ 2 terminal (PLUS MINUS) diode
pd_TO	Thick oxide P+ 2 terminal (PLUS MINUS) diode

Table 3.6 Diode symbol parameters

Parameters	Description
model	HSpice model
lvs_model	LVS model
l	Length of diode
w	Width of diode
area	Area of the diode
perim	Perimeter of diode

3.4. BJTs

This PDK will contain vertical pnp (vpnp) transistor. The device has fixed dimensions for its emitter size. This device is typical of a FinFET process. The emitter width for schematic entry is specified in nanometers. All parameters entered into the pnp must be integers or floating point numbers.

Table 3.7 BJT Spice models list

Spice models name	Description
vpnp	3 terminal (C B E) vertical BJT 0.8 volt

Table 3.8 BJT symbol parameters

Parameters	Description
model	HSpice model
lvs_model	LVS model
area	Area of the diode
m	Multiplicity factor to place number of parallel devices

4. Device Description

4.1. NFET Transistor

4.1.1. nfet, nfet_15, nfet_18

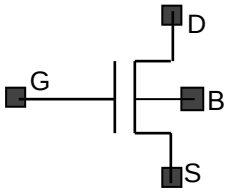


Figure 4.1. Symbol of nfet transistor

Table 4.1 nfet Spice model

Spice models name	Netlist
nfet	xm1 net1 net3 net2 gnd! n08 l=0.014u nfin=3 nf=1 +m=1 fpitch=0.032u plorient=0 cpp=80n
nfet_15	xm1 net1 net3 net2 gnd! n15 l=0.014u nfin=3 m=1 nf=1 m=1 fpitch=0.032u plorient=0 cpp=80n
nfet_18	xm1 net1 net3 net2 gnd! n18 l='0.014u' nfin=3 m=1 nf=1 m=1 fpitch=0.032u plorient=0 cpp=80n

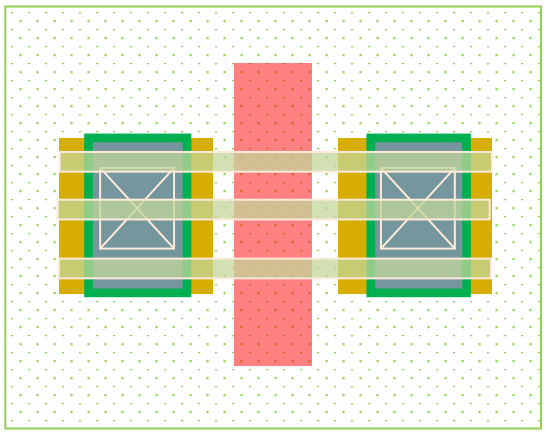


Figure 4.2. Layout of nfet transistor

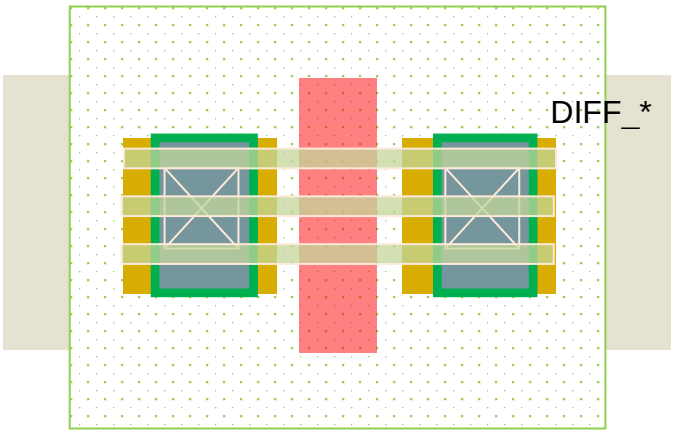


Figure 4.3. Layout of nfet_15 nfet_18 transistor

Table 4.2 nfet Device Layers

Device Layers	Layer Color and Fill
DIFF	
NIMP	
PO	
V0	
CTM1	
M1	
DIFF_* (DIFF_15, DIFF_18)	
FIN	

Table 4.3 nfet Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND NIMP CONTAINS PO
G	PO AND DIFF
D	DIFF AND NIMP AND FIN NOT PO
S	DIFF AND NIMP AND FIN NOT PO
B	Substrate

Table 4.4 nfet LVS Checking

Parameter Calculation	
Length	PO intersecting FIN
Width	PO AND FIN

4.1.2. nfet_hvt

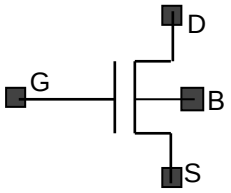


Figure 4.4. Symbol of nfet_hvt transistor

Table 4.5 nfet_hvt Spice model

Spice models name	Netlist
nfet_hvt	xm2 net1 net3 net2 gnd! n08_hvt l=0.014u nfin=3 m=1 nf=1 m=1 fpitch=0.032u plorient=0 cpp=80n

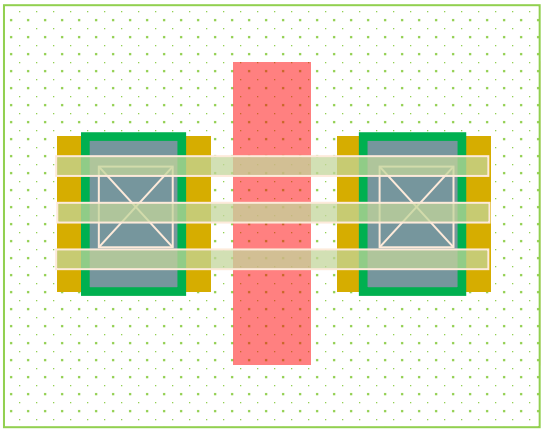


Figure 4.5. Layout of nfet_hvt transistor

Table 4.6 nfet_hvt Device Layers

Device Layers	Layer Color and Fill
DIFF	
NIMP	
PO	
V0	
CTM1	
M1	
HVTIMP	
FIN	

Table 4.7 nfet_hvt Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND NIMP AND HVTIMP CONTAINS PO
G	PO AND DIFF
D	DIFF AND NIMP AND HVTIMP AND FIN NOT PO
S	DIFF AND NIMP AND HVTIMP AND FIN NOT PO
B	Substrate

Table 4.8 nfet_hvt LVS Checking

Parameter Calculation	
Length	PO intersecting FIN
Width	PO AND FIN

4.1.3. nfet_lvt

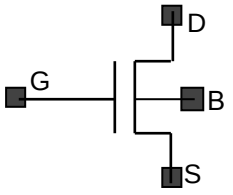


Figure 4.6. Symbol of nfet_lvt transistor

Table 4.9 nfet_lvt Spice model

Spice models name	Netlist
nfet_lvt	xm2 net1 net3 net2 gnd! n08_lvt l=0.014u nfin=3 m=1 nf=1 m=1 fpitch=0.032u plorient=0 cpp=80n

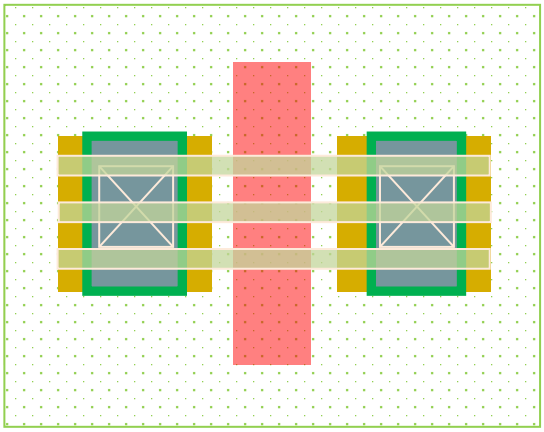


Figure 4.7. Layout of nfet_lvt transistor

Table 4.10 nfet_lvt Device Layers

Device Layers	Layer Color and Fill
DIFF	
NIMP	
PO	
V0	
CTM1	
M1	
LVTIMP	
FIN	

Table 4.11 nfet_lvt Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND NIMP AND LVTIMP CONTAINS PO
G	PO AND FIN
D	DIFF AND NIMP AND LVTIMP AND FIN NOT PO
S	DIFF AND NIMP AND LVTIMP AND NOT PO
B	Substrate

Table 4.12 nfet_lvt LVS Checking

Parameter Calculation	
Length	PO intersecting FIN
Width	PO AND FIN

4.1.4. nfet_slvt

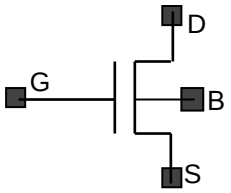


Figure 4.8. Symbol of nfet_slvt transistor

Table 4.13 nfet_slvt Spice model

Spice models name	Netlist
nfet_slvt	xm2 net1 net3 net2 gnd! n08_slvt l=0.014u nfin=3 m=1 nf=1 m=1 fpitch=0.032u plorient=0 cpp=80n

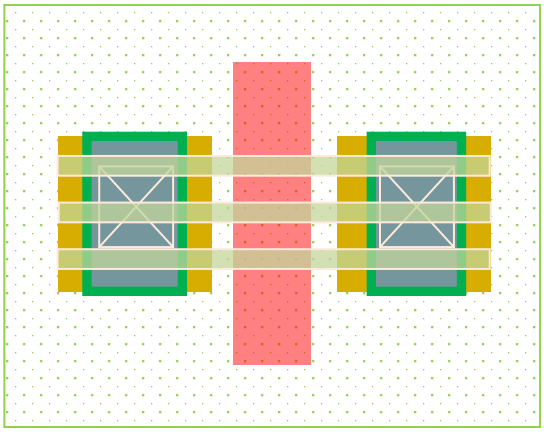


Figure 4.9. Layout of nfet_slvt transistor

Table 4.14 nfet_slvt Device Layers

Device Layers	Layer Color and Fill
DIFF	
NIMP	
PO	
V0	
CTM1	
M1	
SLVTIMP	
FIN	

Table 4.15 nfet_slvt Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND NIMP AND SLVTIMP CONTAINS PO
G	PO AND FIN
D	DIFF AND NIMP AND SLVTIMP AND FIN NOT PO
S	DIFF AND NIMP AND SLVTIMP AND NOT PO
B	Substrate

Table 4.16 nfet_slvt LVS Checking

Parameter Calculation	
Length	PO intersecting FIN
Width	PO AND FIN

4.2. PFET Transistor

4.2.1. pfet, pfet_15, pfet_18

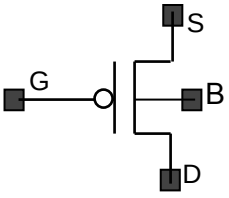


Figure 4.10. Symbol of pfet transistor

Table 4.17 pfet Spice model

Spice models name	Netlist
pfet	xm5 net1 net3 net2 gnd! p08 l=0.014u nfin=3 m=1 nf=1 fpitch=0.032u plorient=0 cpp=80n
pfet_15	xm5 net1 net3 net2 gnd! p15 l=0.014u nfin=3 m=1 nf=1 fpitch=0.032u plorient=0 cpp=80n
pfet_18	xm5 net1 net3 net2 gnd! p18 l=0.014u nfin=3 m=1 nf=1 fpitch=0.032u plorient=0 cpp=80n

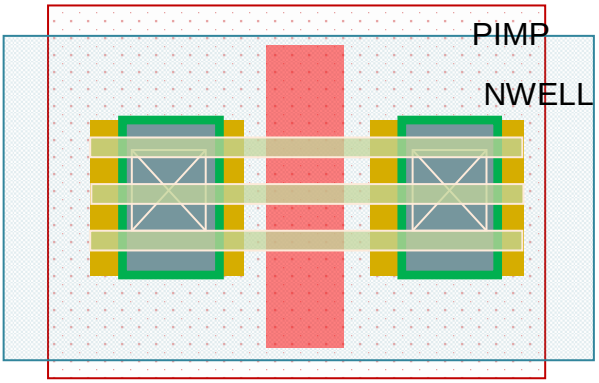


Figure 4.11. Layout of pfet transistor

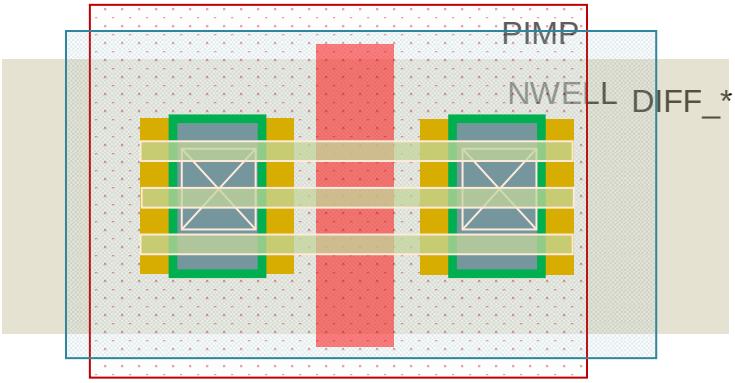


Figure 4.12. Layout of pfet_15 pfet_18 transistor

Table 4.18 pfet Device Layers

Device Layers	Layer Color and Fill
DIFF	
PIMP	
PO	
V0	
CTM1	
M1	
NWELL	
DIFF_* (DIFF_15, DIFF_18)	
FIN	

Table 4.19 pfet Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND PIMP AND NWELL CONTAINS PO
G	PO AND FIN
D	DIFF AND PIMP AND NWELL AND FIN NOT PO
S	DIFF AND PIMP AND NWELL AND FIN NOT PO
B	Substrate

Table 4.20 pfet LVS Checking

Parameter Calculation	
Length	PO intersecting FIN
Width	PO AND FIN

4.2.2. pfet_hvt

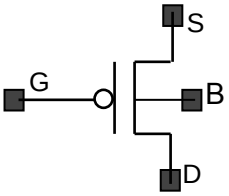


Figure 4.13. Symbol of pfet_hvt transistor

Table 4.21 pfet_hvt Spice model

Spice models name	Netlist
pfet_hvt	xm5 net1 net3 net2 gnd! p08_hvt l=0.014u nfin=3 m=1 nf=1 fpitch=0.032u plorient=0 cpp=80n

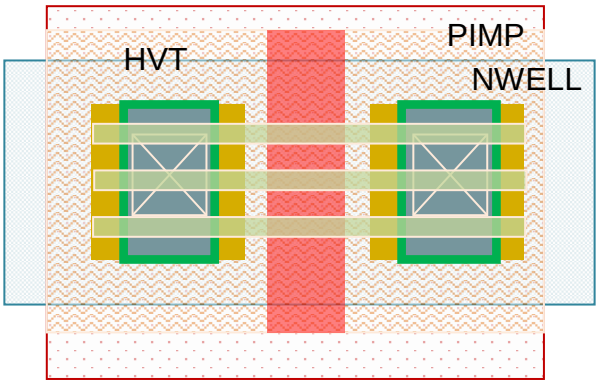


Figure 4.14. Layout of pfet_hvt transistor

Table 4.22 pfet_hvt Device Layers

Device Layers	Layer Color and Fill
DIFF	
PIMP	
PO	
V0	
CTM1	
M1	
HVTIMP	
NWELL	
FIN	

Table 4.23 pfet_hvt Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND PIMP AND NWELL AND HVTIMP CONTAINS PO
G	PO AND FIN
D	DIFF AND PIMP AND HVTIMP AND NWELL AND FIN NOT PO
S	DIFF AND PIMP AND HVTIMP AND NWELL AND FIN NOT PO
B	Substrate

Table 4.24 pfet_hvt LVS Checking

Parameter Calculation	
Length	PO intersecting FIN
Width	PO AND FIN

4.2.3. pfet_lvt

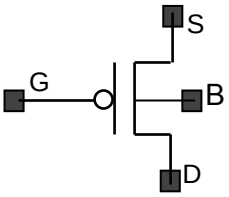


Figure 4.15. Symbol of pfet_lvt transistor

Table 4.25 pfet_lvt Spice model

Spice models name	Netlist
pfet_lvt	xm5 net1 net3 net2 gnd! p08_lvt l=0.014u nfin=3 m=1 nf=1 fpitch=0.032u plorient=0 cpp=80n

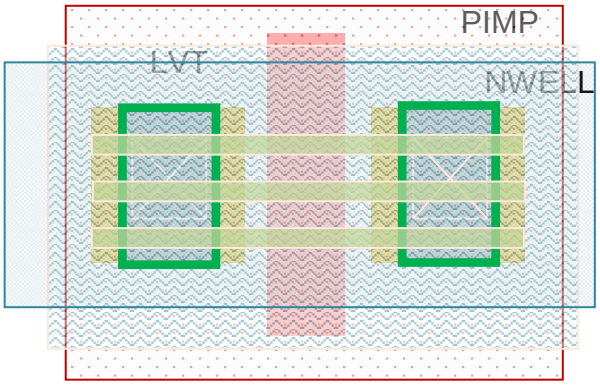


Figure 4.16. Layout of pfet_lvt transistor

Table 4.26 pfet_lvt Device Layers

Device Layers	Layer Color and Fill
DIFF	
PIMP	
PO	
V0	
CTM1	
M1	
LVTIMP	
NWELL	
FIN	

Table 4.27 pfet_lvt Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND PIMP AND NWELL AND LVTIMP CONTAINS PO
G	PO AND FIN
D	DIFF AND PIMP AND LVTIMP AND NWELL AND FIN NOT PO
S	DIFF AND PIMP AND LVTIMP AND NWELL AND FIN NOT PO
B	Substrate

Table 4.28 pfet_lvt LVS Checking

Parameter Calculation	
Length	PO intersecting FIN
Width	PO AND FIN

4.2.4. pfet_slvt

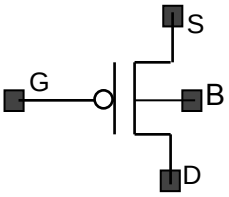


Figure 4.17. Symbol of pfet_slvt transistor

Table 4.29 pfet_slvt Spice model

Spice models name	Netlist
pfet_slvt	xm5 net1 net3 net2 gnd! p08_slvt l=0.014u nfin=3 m=1 nf=1 fpitch=0.032u plorient=0 cpp=80n

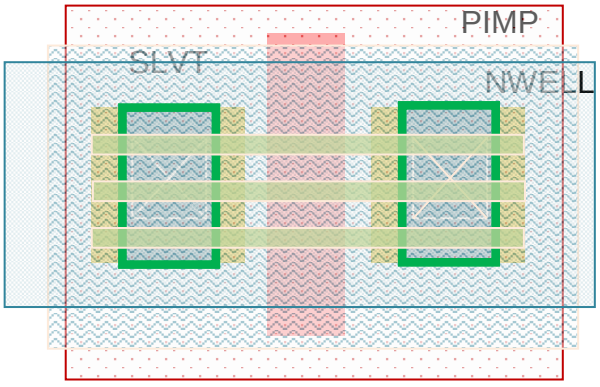


Figure 4.18. Layout of pfet_slvt transistor

Table 4.30 pfet_slvt Device Layers

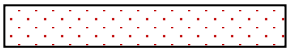
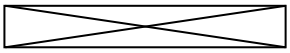
Device Layers	Layer Color and Fill
DIFF	
PIMP	
PO	
V0	
CTM1	
M1	
SLVTIMP	
NWELL	
FIN	

Table 4.31 pfet_slvt Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIFF AND PIMP AND NWELL AND SLVTIMP CONTAINS PO
G	PO AND FIN
D	DIFF AND PIMP AND SLVTIMP AND NWELL AND FIN NOT PO
S	DIFF AND PIMP AND SLVTIMP AND NWELL AND FIN NOT PO
B	Substrate

Table 4.32 pfet_slvt LVS Checking

Parameter Calculation	
Length	PO intersecting FIN
Width	PO AND FIN

4.3. Resistors

4.3.1. rpoly

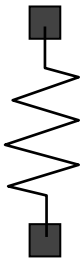


Figure 4.19. Symbol of rpoly resistor

Table 4.33 rpoly Spice model

Spice models name	Netlist
rpoly	xr6 net28 net29 rpoly w=200n l=450n r=1k m=1

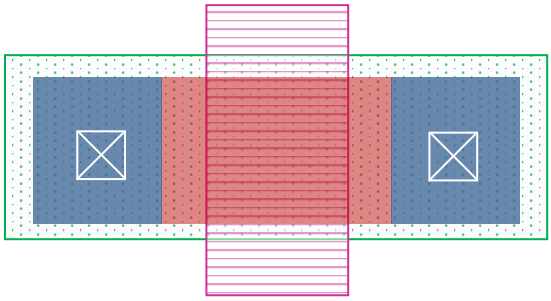


Figure 4.20. Layout of rpoly resistor

Table 4.34 rpoly Device Layers

Device Layers	Layer Color and Fill
RPOLY	
PO	
CO	
M1	

Table 4.35 rpoly Device Derivation

Device Derivation	Device Layer Derivation
Recognition	PO AND RPOLY
PLUS	PO NOT RPOLY
MINUS	PO NOT RPOLY
BULK	Substrate

Table 4.36 rpoly LVS Checking

Parameter Calculation	
Length	Contact to Contact
Width	PO Width
Resistance	sheet resistance * Length / Width

4.3.2. rmet

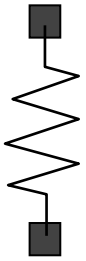


Figure 4.21. Symbol of rmet resistor

Table 4.37 rpoly Spice model

Spice models name	Netlist
rmet	xr6 net28 net29 rmet w=200n l=450n r=1k m=1

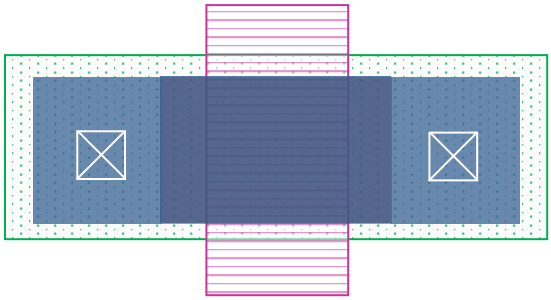


Figure 4.22. Layout of rpoly resistor

Table 4.38 rpoly Device Layers

Device Layers	Layer Color and Fill
RMET	
CO	
M1	

Table 4.39 rpoly Device Derivation

Device Derivation	Device Layer Derivation
Recognition	M1 AND RMET
PLUS	M1 NOT RMET
MINUS	M1 NOT RMET
BULK	Substrate

Table 4.40 rpoly LVS Checking

Parameter Calculation	
Length	Contact to Contact
Width	RMET and M1 Width
Resistance	sheet resistance * Length / Width

4.4. Diode

4.4.1. nd

Figure 4.23. Symbol of nd diode

Table 4.41 nd Spice model

Spice models name	Netlist
nd	d13 net45 net44 nd area=33f m=1 perim=2.5u

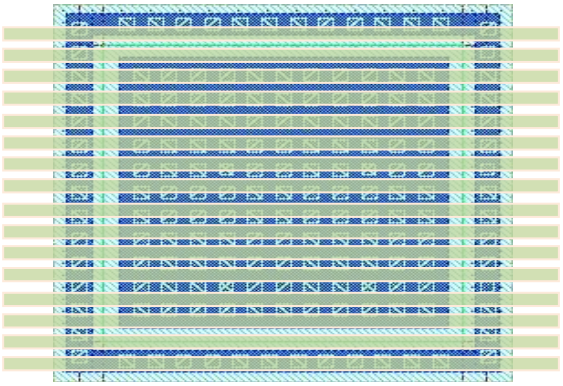


Figure 4.24. Layout of nd diode

Table 4.42 nd Device Layers

Device Layers	Layer Color and Fill
M1	
DIFF	
V0	
CTM1	
NWELL	
PIMP	
NIMP	
DIOD	
FIN	

Table 4.43 nd Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIOD AND NIMP AND PIMP
PLUS	DIOD AND PIMP AND DIFF
MINUS	DIOD AND NIMP AND DIFF

Table 4.44 nd LVS Checking

Parameter Calculation	
area	Area of MINUS
perim	Perimeter of MINUS

4.4.2. pd

Figure 4.25. Symbol of pd diode

Table 4.45 pd Spice model

Spice models name	Netlist
pd	d14 net45 net44 pd area=33f m=1 perim=2.5u

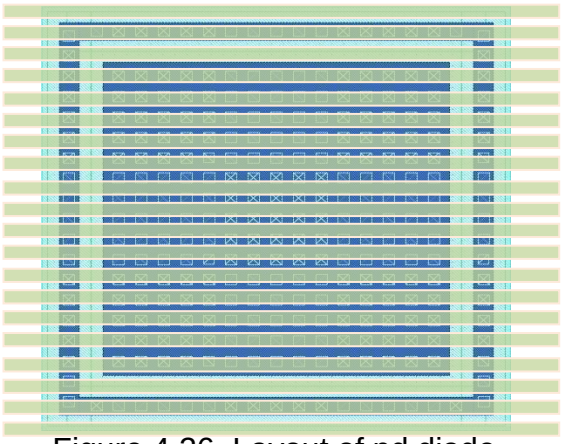


Figure 4.26. Layout of pd diode

Table 4.46 pd Device Layers

Device Layers	Layer Color and Fill
M1	
DIFF	
V0	
CTM1	
NWELL	
PIMP	
NIMP	
DIOD	
FIN	

Table 4.47 pd Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIOD AND NWELL AND NIMP AND PIMP
PLUS	DIOD AND NWELL AND NIMP AND DIFF
MINUS	DIOD AND NWELL AND PIMP AND DIFF

Table 4.48 pd LVS Checking

Parameter Calculation	
area	Area of MINUS
perim	Perimeter of MINUS

4.4.3. nd_TO

Figure 4.27. Symbol of nd_TO diode

Table 4.49 nd Spice model

Spice models name	Netlist
nd	d13 net45 net44 nd_TO area=33f m=1 perim=2.5u

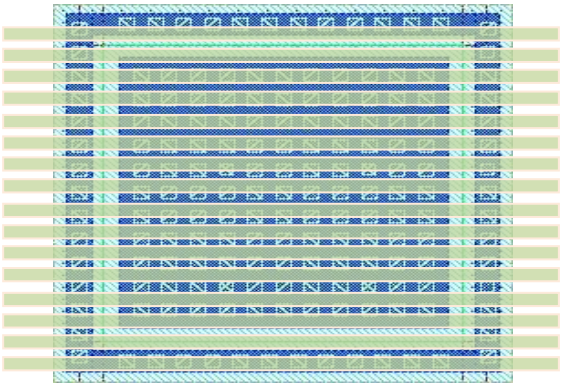


Figure 4.28. Layout of nd_TO diode

Table 4.50 nd_TO Device Layers

Device Layers	Layer Color and Fill
M1	
DIFF_15 DIFF_18	
V0	
CTM1	
NWELL	
PIMP	
NIMP	
DIOD	
FIN	

Table 4.51 nd_TO Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIOD AND NIMP AND PIMP
PLUS	DIOD AND PIMP AND (DIFF_15 OR DIFF_18)
MINUS	DIOD AND NIMP AND (DIFF_15 OR DIFF_18)

Table 4.52 nd_TO LVS Checking

Parameter Calculation	
area	Area of MINUS
perim	Perimeter of MINUS

4.4.4. pd_TO

Figure 4.29. Symbol of pd_TO diode

Table 4.53 pd_TO Spice model

Spice models name	Netlist
pd	d14 net45 net44 pd_TO area=33f m=1 perim=2.5u

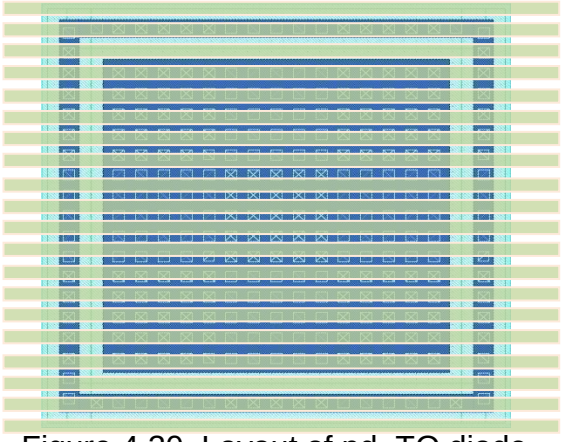


Figure 4.30. Layout of pd_TO diode

Table 4.54 pd_TO Device Layers

Device Layers	Layer Color and Fill
M1	
DIFF_15 DIFF_18	
V0	
CTM1	
NWELL	
PIMP	
NIMP	
DIOD	
FIN	

Table 4.55 pd_TO Device Derivation

Device Derivation	Device Layer Derivation
Recognition	DIOD AND NWELL AND NIMP AND PIMP
PLUS	DIOD AND NWELL AND NIMP AND (DIFF_15 OR DIFF_18)
MINUS	DIOD AND NWELL AND PIMP AND (DIFF_15 OR DIFF_18)

Table 4.56 pd_TO LVS Checking

Parameter Calculation	
area	Area of MINUS
perim	Perimeter of MINUS

4.5. BJT

4.5.1. vpnp

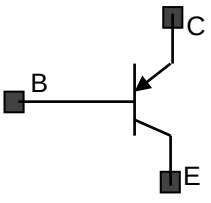


Figure 4.31. Symbol of vpnp transistor

Table 4.57 vpnp Spice model

Spice models name	Netlist
vpnp	q19 net48 net50 net49 vpnp w=2.5u l=2u nf=1

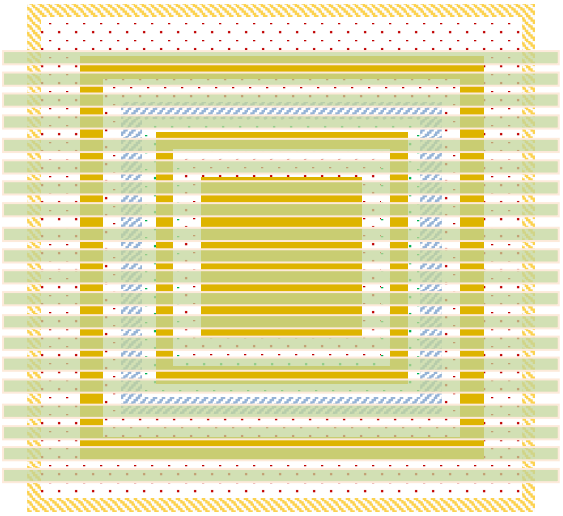


Figure 4.32. Layout of vpnp transistor

Table 4.58 vpnp Device Layers

Device Layers	Layer Color and Fill
DIFF	
NIMP	
PIMP	
NWELL	
V0	
CTM1	
M1	
BJTMARK	
FIN	

Table 4.59 vpnp Device Derivation

Device Derivation	Device Layer Derivation
Recognition	BJTMARK AND PIMP AND NWELL
E	BJTMARK AND Nburied AND NIMP AND Pwell
B	BJTMARK AND Nburied AND PIMP AND Pwell
C	BJTMARK AND Nburied AND NIMP ANDNOT Pwell

Table 4.60 vpnp LVS Checking

Parameter	Calculation
area	Area of Emitter

5. References

1. SAED14nm_FinFET EDK Documentation
2. OpenAccess (http://www.si2.org/?page=621)

6. Design Team and Schedule

SAED_PDK14_FinFET will be developed in SYNOPSYS ARMENIA CJSC Educational Department by Student Working Groups (SWGs) and students.

Head of the project - Director of SYNOPSYS ARMENIA CJSC Educational Department, Sci.D., Professor Vazgen Melikyan.

The list of SAED_PDK14_FinFET developers is shown in Table 6.1.

Table 6.1. The list of developers

Product Name	Student	SWG number	Educational Program	Year
SAED_PDK14_FinFET Process Design Kit	Araks Hovsepyan	1	Bachelor	4
	Shoghik Manukyan	1	Bachelor	4
	Hovhannes Grigoryan	1	Bachelor	3
	Zhirayr Margaryan	1	Bachelor	3

During the development of SAED_PDK14_FinFET several SYNOPSYS ARMENIA CJSC employees, will carry out consultations for the developers. The list of consultants is shown in Table 6.2.

Table 6.2. The list of consultants

Product Name	Consultant
SAED_PDK14_FinFET Process Design Kit	Ararat Khachatryan
	Abraham Balabanyan

SAED_PDK14_FinFET will be developed according to the schedule shown in Table 6.3.

Table 6.3. Schedule

Product Name	Deadline
SAED_PDK14_FinFET Process Design Kit	March 7, 2017
Detailed Schedule	
Technology files	December 1, 2016
HSPICE models (with documentation)	December 1, 2016
Symbol Library and OA Python PCells	January 31, 2017
Scripts	February 28, 2017
Physical Verification files (with documentation)	January 31, 2017
Parasitic extraction files	February 28, 2017
Sample designs	February 28

7. Revision history

Table 7.1. Revision history

Revision	Date	Change
0.1	11/03/2016	
1.0	11/16/2016	Updated PDK components' list; added device description for nd_TO and pd_TO