# FRAME RATE CONVERSION BOARD SPECIFICATION

**MODEL: PL.MS6M30.1X** 

Part Number: PL-11010808

AUTHOR:

CHECKED BY:

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## **REVISION HISTORY**

VERSION	DATE	BOARD ID	PAGE	DISCRIPTION	AUTHOR
V1.0	2010.11.18	PL.MS6M30.1A 10446	All	First issued	Fanny
V1.0	2011.01.08	PL.MS6M30.1B 10512	2	Modify the board picture in part 3;	Fanny

#### 1. GENERAL DESCRIPTION

**PL.MS6M30.1X** doubles the frames (50Hz  $\rightarrow$  100Hz conversion, 60Hz  $\rightarrow$  120Hz conversion, 24Hz  $\rightarrow$  120Hz conversion, frame interpolation) of the video signal output (Full-HD signal by LVDS interface) from a TV control board and then supplies the frame-doubled video signal to a panel provided with LVDS input.

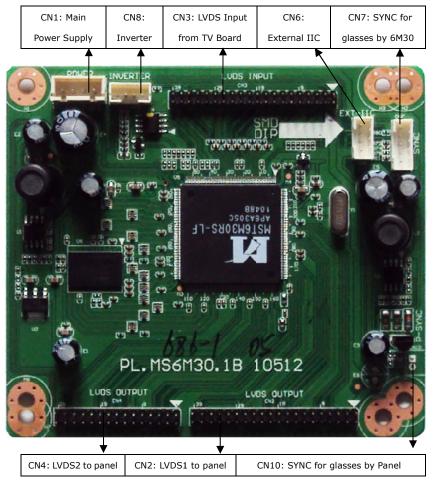
#### 2. FEATURES

CHIPSET	MST6M30QS
POWER REQUIREMENT	12V
MAX POWER CONSUMPTION	4W

	INPUT(50Hz/60Hz)	-	OUTPUT(100Hz/120Hz)
EDECLIENCY	1 phase, Max 83MHz	<b>→</b>	2 phase, Max 83MHz
FREQUENCY	2 phase, Max 74.25MHz	-	4 Phase, Max 74.25MHz
VIDEO SIGNAL	WXGA 768p (1366x768)	-	WXGA 768p (1366x768)
	Full-HD 1080p (1920x1080)	<b>→</b>	Full-HD 1080p (1920x1080)

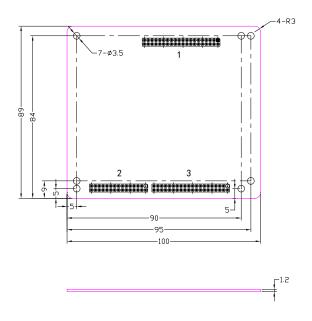
#### 3. FUNCTION LAYOUT

#### **TOP VIEW OF PL.MS6M30.1X**



#### 4. PCB DIMENSIONS

The overall height of PL.MS6M30.1X is 16 mm.



#### **5. INTERFACE DEFINITION**

The optional connectors are marked with "\*".

#### **♦** CN1(4PIN/2.54): MAIN POWER INPUT CONNECTOR

NO.	SYMBOL	DESCRIPTION
1	12V	1121/ Down Input
2	12V	+12V Power Input
3	GND	Constant
4	GND	Ground

### ♦ CN2(2x20PIN/2.0): LVDS1 TO PANEL

NO.	SYMBOL	DESCRIPTION	
1	VCC-PANEL		
2	VCC-PANEL	Power for Panel	
3	VCC-PANEL		
4	GND		
5	GND	Ground	
6	GND		
7	A0M	LVDS 0 A- Signal	
8	A0P	LVDS 0 A+ Signal	

		,	
9	A1M	LVDS 1 A- Signal	
10	A1P	LVDS 1 A+ Signal	
11	A2M	LVDS 2 A- Signal	
12	A2P	LVDS 2 A+ Signal	
13	GND	Ground	
14	GND	Ground	
15	ACKM	LVDS Clock A- Signal	
16	ACKP	LVDS Clock A+ Signal	
17	АЗМ	LVDS 3 A- Signal	
18	АЗР	LVDS 3 A+ Signal	
19	вом	LVDS 0 B- Signal	
20	ВОР	LVDS 0 B+ Signal	
21	B1M	LVDS 1 B- Signal	
22	B1P	LVDS 1 B+ Signal	
23	B2M	LVDS 2 B- Signal	
24	B2P	LVDS 2 B+ Signal	
25	GND	Constant	
26	GND	Ground	
27	BCKM	LVDS Clock B- Signal	
28	BCKP	LVDS Clock B+ Signal	
29	ВЗМ	LVDS 3 B- Signal	
30	ВЗР	LVDS 3 B+ Signal	
31	GND	Crownd	
32	GND	Ground	
33	CON1'	JEDIA/VESA format selection	
34	L/R Sycn	Input signal for left/right eye frame synchronous	
35	2D/3D	Input signal for 2D/3D mode selection	
36	LD_EN	Local dimming enable selection	
37	A4M	TX LVDS 4 A- Signal	
38	A4P	TX LVDS 4 A+ Signal	
39	B4M	TX LVDS 4 B- Signal	
40	B4P	TX LVDS 4 B+ Signal	

# **♦** CN4(2x15PIN/2.0): LVDS2 TO PANEL

NO.	SYMBOL	DESCRIPTION	
1	GND	Constant	
2	GND	Ground	
3	СОМ	LVDS 0 C- Signal	

4	C0P	LVDS 0 C+ Signal
5	C1M	LVDS 1 C- Signal
6	C1P	LVDS 1 C+ Signal
7	C2M	LVDS 2 C- Signal
8	C2P	LVDS 2 C+ Signal
9	GND	Ground
10	GND	Ground
11	CCKM	LVDS Clock C- Signal
12	ССКР	LVDS Clock C+ Signal
13	C3M	LVDS 3 C- Signal
14	СЗР	LVDS 3 C+ Signal
15	C4M	LVDS 4 C- Signal
16	C4P	LVDS 4 C+ Signal
17	D0M	LVDS 0 D- Signal
18	D0P	LVDS 0 D+ Signal
19	D1M	LVDS 1 D- Signal
20	D1P	LVDS 1 D+ Signal
21	D2M	LVDS 2 D- Signal
22	D2P	LVDS 2 D+ Signal
23	GND	Ground
24	GND	Ground
25	DCKM	LVDS Clock D- Signal
26	DCKP	LVDS Clock D+ Signal
27	D3M	LVDS 3 D- Signal
28	D3P	LVDS 3 D+ Signal
29	D4M	LVDS 4 D- Signal
30	D4P	LVDS 4 D+ Signal
		<u>-</u>

# ♦ CN3(2x20PIN/2.0): LVDS FROM LCD BOARD

NO.	SYMBOL	DESCRIPTION	
1	VCC-PANEL		
2	VCC-PANEL	Power for Panel	
3	VCC-PANEL		
4	GND		
5	GND	Ground	
6	GND		
7	RXO0-	LVDS ODD 0- Signal	
8	RXO0+	LVDS ODD 0+ Signal	

9	9	RXO1-	IVDS ODD 1- Signal
11			
12			
13			
Ground   Ground   Ground   Ground   State			LVDS ODD 2+ Signal
15	13		Ground
16         RXOC+         LVDS ODD Clock+ Signal           17         RXO3-         LVDS ODD 3- Signal           18         RXO3+         LVDS ODD 3+ Signal           19         RXE0-         LVDS EVEN 0- Signal           20         RXE0+         LVDS EVEN 0+ Signal           21         RXE1-         LVDS EVEN 1- Signal           22         RXE1+         LVDS EVEN 2- Signal           23         RXE2-         LVDS EVEN 2- Signal           24         RXE2+         LVDS EVEN 2+ Signal           25         GND         Ground           26         GND         Ground           27         RXEC-         LVDS EVEN Clock- Signal           29         RXE3-         LVDS EVEN Glock+ Signal           30         RXE3+         LVDS EVEN 3- Signal           31         GND         Ground           32         GND         Ground           33         CON1'         JEDIA/VESA format selection           34         3D_Flag         The left or right image flag for 6M30           35         IZCS-SCL         Reserved Power or I <sup>2</sup> C SCL           36         12CS-SDA         Reserved Power or I <sup>2</sup> C SDA           37         RXO4-         L	14	GND	
17         RXO3-         LVDS ODD 3- Signal           18         RXO3+         LVDS ODD 3+ Signal           19         RXE0-         LVDS EVEN 0- Signal           20         RXE0+         LVDS EVEN 0+ Signal           21         RXE1-         LVDS EVEN 1- Signal           22         RXE1+         LVDS EVEN 1+ Signal           23         RXE2-         LVDS EVEN 2- Signal           24         RXE2+         LVDS EVEN 2+ Signal           25         GND         Ground           26         GND         Ground           27         RXEC-         LVDS EVEN Clock- Signal           28         RXEC+         LVDS EVEN Clock- Signal           29         RXE3-         LVDS EVEN 3- Signal           30         RXE3+         LVDS EVEN 3+ Signal           31         GND         Ground           32         GND         Ground           33         CON1'         JEDIA/VESA format selection           34         3D_Flag         The left or right image flag for 6M30           35         I2CS-SCL         Reserved Power or I²C SCL           36         12CS-SDA         Reserved Power or I²C SDA           37         RXO4-         LVDS ODD	15	RXOC-	LVDS ODD Clock- Signal
18         RXO3+         LVDS ODD 3+ Signal           19         RXE0-         LVDS EVEN 0- Signal           20         RXE0+         LVDS EVEN 0+ Signal           21         RXE1-         LVDS EVEN 1- Signal           22         RXE1+         LVDS EVEN 1+ Signal           23         RXE2-         LVDS EVEN 2- Signal           24         RXE2+         LVDS EVEN 2+ Signal           25         GND         Ground           26         GND         Ground           27         RXEC-         LVDS EVEN Clock- Signal           29         RXE3-         LVDS EVEN 3- Signal           30         RXE3+         LVDS EVEN 3+ Signal           31         GND         Ground           32         GND         Ground           33         CON1'         JEDIA/VESA format selection           34         3D_Flag         The left or right image flag for 6M30           35         I2CS-SCL         Reserved Power or I²C SCL           36         12CS-SDA         Reserved Power or I²C SDA           37         RXO4-         LVDS ODD4+ Signal	16	RXOC+	LVDS ODD Clock+ Signal
19         RXE0-         LVDS EVEN 0- Signal           20         RXE0+         LVDS EVEN 0+ Signal           21         RXE1-         LVDS EVEN 1- Signal           22         RXE1+         LVDS EVEN 1+ Signal           23         RXE2-         LVDS EVEN 2- Signal           24         RXE2+         LVDS EVEN 2+ Signal           25         GND         Ground           26         GND         Ground           27         RXEC-         LVDS EVEN Clock- Signal           29         RXE3-         LVDS EVEN 3- Signal           30         RXE3+         LVDS EVEN 3+ Signal           31         GND         Ground           32         GND         Ground           33         CON1'         JEDIA/VESA format selection           34         3D_Flag         The left or right image flag for 6M30           35         I2CS-SCL         Reserved Power or I <sup>2</sup> C SCL           36         12CS-SDA         Reserved Power or I <sup>2</sup> C SDA           37         RXO4-         LVDS ODD4- Signal           38         RXO4+         LVDS ODD4+ Signal	17	RXO3-	LVDS ODD 3- Signal
20         RXE0+         LVDS EVEN 0+ Signal           21         RXE1-         LVDS EVEN 1- Signal           22         RXE1+         LVDS EVEN 1+ Signal           23         RXE2-         LVDS EVEN 2- Signal           24         RXE2+         LVDS EVEN 2+ Signal           25         GND         Ground           26         GND         Ground           27         RXEC-         LVDS EVEN Clock- Signal           28         RXE3-         LVDS EVEN Glock+ Signal           29         RXE3-         LVDS EVEN 3- Signal           30         RXE3+         LVDS EVEN 3+ Signal           31         GND         Ground           32         GND         Ground           33         CON1'         JEDIA/VESA format selection           34         3D_Flag         The left or right image flag for 6M30           35         IZCS-SCL         Reserved Power or I <sup>2</sup> C SCL           36         I2CS-SDA         Reserved Power or I <sup>2</sup> C SDA           37         RXO4-         LVDS ODD4+ Signal           38         RXO4+         LVDS ODD4+ Signal	18	RXO3+	LVDS ODD 3+ Signal
21         RXE1-         LVDS EVEN 1- Signal           22         RXE1+         LVDS EVEN 1+ Signal           23         RXE2-         LVDS EVEN 2- Signal           24         RXE2+         LVDS EVEN 2+ Signal           25         GND         Ground           26         GND         Ground           27         RXEC-         LVDS EVEN Clock- Signal           28         RXEC+         LVDS EVEN Clock+ Signal           29         RXE3-         LVDS EVEN 3- Signal           30         RXE3+         LVDS EVEN 3+ Signal           31         GND         Ground           32         GND         Ground           33         CON1'         JEDIA/VESA format selection           34         3D_Flag         The left or right image flag for 6M30           35         I2CS-SCL         Reserved Power or I <sup>2</sup> C SCL           36         12CS-SDA         Reserved Power or I <sup>2</sup> C SDA           37         RXO4-         LVDS ODD4+ Signal           38         RXO4+         LVDS ODD4+ Signal	19	RXE0-	LVDS EVEN 0- Signal
22       RXE1+       LVDS EVEN 1+ Signal         23       RXE2-       LVDS EVEN 2- Signal         24       RXE2+       LVDS EVEN 2+ Signal         25       GND       Ground         26       GND       Ground         27       RXEC-       LVDS EVEN Clock- Signal         28       RXEC+       LVDS EVEN Clock+ Signal         29       RXE3-       LVDS EVEN 3- Signal         30       RXE3+       LVDS EVEN 3+ Signal         31       GND       Ground         32       GND       Ground         33       CON1'       JEDIA/VESA format selection         34       3D_Flag       The left or right image flag for 6M30         35       I2CS-SCL       Reserved Power or I <sup>2</sup> C SCL         36       12CS-SDA       Reserved Power or I <sup>2</sup> C SDA         37       RXO4-       LVDS ODD4- Signal         38       RXO4+       LVDS ODD4+ Signal	20	RXE0+	LVDS EVEN 0+ Signal
23         RXE2-         LVDS EVEN 2- Signal           24         RXE2+         LVDS EVEN 2+ Signal           25         GND         Ground           26         GND         LVDS EVEN Clock- Signal           27         RXEC-         LVDS EVEN Clock+ Signal           28         RXEC+         LVDS EVEN 3- Signal           29         RXE3-         LVDS EVEN 3- Signal           30         RXE3+         LVDS EVEN 3+ Signal           31         GND         Ground           32         GND         Ground           33         CON1'         JEDIA/VESA format selection           34         3D_Flag         The left or right image flag for 6M30           35         I2CS-SCL         Reserved Power or I <sup>2</sup> C SCL           36         12CS-SDA         Reserved Power or I <sup>2</sup> C SDA           37         RXO4-         LVDS ODD4- Signal           38         RXO4+         LVDS ODD4+ Signal	21	RXE1-	LVDS EVEN 1- Signal
24         RXE2+         LVDS EVEN 2+ Signal           25         GND         Ground           26         GND         Ground           27         RXEC-         LVDS EVEN Clock- Signal           28         RXEC+         LVDS EVEN Clock+ Signal           29         RXE3-         LVDS EVEN 3- Signal           30         RXE3+         LVDS EVEN 3+ Signal           31         GND         Ground           32         GND         Ground           33         CON1'         JEDIA/VESA format selection           34         3D_Flag         The left or right image flag for 6M30           35         I2CS-SCL         Reserved Power or I <sup>2</sup> C SCL           36         12CS-SDA         Reserved Power or I <sup>2</sup> C SDA           37         RXO4-         LVDS ODD4- Signal           38         RXO4+         LVDS ODD4+ Signal	22	RXE1+	LVDS EVEN 1+ Signal
25         GND           26         GND           27         RXEC-           28         RXEC+           29         RXE3-           30         RXE3+           31         GND           32         GND           33         CON1'           34         3D_Flag           35         I2CS-SCL           36         12CS-SDA           37         RXO4-           38         RXO4+           LVDS ODD4+ Signal	23	RXE2-	LVDS EVEN 2- Signal
26         GND           27         RXEC-           28         RXEC+           29         RXE3-           30         RXE3+           31         GND           32         GND           33         CON1'           34         3D_Flag           35         I2CS-SCL           36         12CS-SDA           37         RXO4-           38         RXO4+           LVDS ODD4+ Signal	24	RXE2+	LVDS EVEN 2+ Signal
26       GND         27       RXEC-       LVDS EVEN Clock- Signal         28       RXEC+       LVDS EVEN Clock+ Signal         29       RXE3-       LVDS EVEN 3- Signal         30       RXE3+       LVDS EVEN 3+ Signal         31       GND       Ground         32       GND       Ground         33       CON1'       JEDIA/VESA format selection         34       3D_Flag       The left or right image flag for 6M30         35       I2CS-SCL       Reserved Power or I2C SCL         36       12CS-SDA       Reserved Power or I2C SDA         37       RXO4-       LVDS ODD4- Signal         38       RXO4+       LVDS ODD4+ Signal	25	GND	Cround
28 RXEC+ LVDS EVEN Clock+ Signal 29 RXE3- LVDS EVEN 3- Signal 30 RXE3+ LVDS EVEN 3+ Signal 31 GND Ground 32 GND 33 CON1' JEDIA/VESA format selection 34 3D_Flag The left or right image flag for 6M30 35 I2CS-SCL Reserved Power or I <sup>2</sup> C SCL 36 12CS-SDA Reserved Power or I <sup>2</sup> C SDA 37 RXO4- LVDS ODD4- Signal 38 RXO4+ LVDS ODD4+ Signal	26	GND	Ground
29 RXE3-  30 RXE3+  LVDS EVEN 3- Signal  31 GND  Ground  32 GND  33 CON1'  JEDIA/VESA format selection  34 3D_Flag  The left or right image flag for 6M30  35 I2CS-SCL  Reserved Power or I <sup>2</sup> C SCL  36 12CS-SDA  RXO4-  RXO4-  LVDS ODD4- Signal  RXO4+  LVDS ODD4+ Signal	27	RXEC-	LVDS EVEN Clock- Signal
30 RXE3+ LVDS EVEN 3+ Signal  31 GND  Ground  32 GND  33 CON1' JEDIA/VESA format selection  34 3D_Flag The left or right image flag for 6M30  35 I2CS-SCL Reserved Power or I <sup>2</sup> C SCL  36 12CS-SDA Reserved Power or I <sup>2</sup> C SDA  37 RXO4- LVDS ODD4- Signal  38 RXO4+ LVDS ODD4+ Signal	28	RXEC+	LVDS EVEN Clock+ Signal
31 GND  32 GND  33 CON1'  34 3D_Flag  The left or right image flag for 6M30  35 I2CS-SCL  Reserved Power or I <sup>2</sup> C SCL  36 12CS-SDA  Reserved Power or I <sup>2</sup> C SDA  LVDS ODD4- Signal  RXO4-  LVDS ODD4+ Signal	29	RXE3-	LVDS EVEN 3- Signal
Ground  Ground	30	RXE3+	LVDS EVEN 3+ Signal
32 GND  33 CON1' JEDIA/VESA format selection  34 3D_Flag The left or right image flag for 6M30  35 I2CS-SCL Reserved Power or I <sup>2</sup> C SCL  36 12CS-SDA Reserved Power or I <sup>2</sup> C SDA  37 RXO4- LVDS ODD4- Signal  38 RXO4+ LVDS ODD4+ Signal	31	GND	Consumed
34 3D_Flag The left or right image flag for 6M30 35 I2CS-SCL Reserved Power or I <sup>2</sup> C SCL 36 12CS-SDA Reserved Power or I <sup>2</sup> C SDA 37 RXO4- LVDS ODD4- Signal 38 RXO4+ LVDS ODD4+ Signal	32	GND	Ground
35 I2CS-SCL Reserved Power or I <sup>2</sup> C SCL  36 12CS-SDA Reserved Power or I <sup>2</sup> C SDA  37 RXO4- LVDS ODD4- Signal  38 RXO4+ LVDS ODD4+ Signal	33	CON1'	JEDIA/VESA format selection
36 12CS-SDA Reserved Power or I <sup>2</sup> C SDA  37 RXO4- LVDS ODD4- Signal  38 RXO4+ LVDS ODD4+ Signal	34	3D_Flag	The left or right image flag for 6M30
37 RXO4- LVDS ODD4- Signal 38 RXO4+ LVDS ODD4+ Signal	35	I2CS-SCL	Reserved Power or I <sup>2</sup> C SCL
38 RXO4+ LVDS ODD4+ Signal	36	12CS-SDA	Reserved Power or I <sup>2</sup> C SDA
	37	RXO4-	LVDS ODD4- Signal
39 RXE4- LVDS EVEN 4- Signal	38	RXO4+	LVDS ODD4+ Signal
	39	RXE4-	LVDS EVEN 4- Signal
40 RXE4+ LVDS EVEN 4+ Signal	40	RXE4+	LVDS EVEN 4+ Signal

# ♦ CN7(5PIN/2.0): SYNC FOR GLASSES BY 6M30 CONNECTOR

NO.	SYMBOL	DESCRIPTION	
1	GND	Ground	
2	SG_SYNC	Sync for glasses by 6M30	

3	EYE_IN	GPIO for glasses
4	EYE_OUT	GPIO for glasses
5	VCC	VCC Power Supply

#### **◆** \*CN6(4PIN/2.0): EXTERNAL IIC CONNECTOR

NO.	SYMBOL	DESCRIPTION
1	3V3	+3.3V Power Input
2	SCL	DDC CLOCK
3	SDA	DDC DATA
4	GND	Ground

#### **♦** CN8(4PIN/2.0): INVERTER CONNECTOR

NO.	SYMBOL	DESCRIPTION
1	3V3	+3.3V Power Supply
2	ADJ	Brightness Adjustment for Panel
3	GND	Ground
4	GND	

# ◆ CN10(2PIN/2.0): SYNC FOR GLASSES BY PANEL CONNECTOR

NO.	SYMBOL	DESCRIPTION
1	P-SYNC	sync for glasses by panel
2	GND	Ground

#### 6. CONFIGURATION & GENERAL PRECAUTIONS

- Relative humidity: ≤ 80%.
- Storage temperature: -10~60°C.
- Operation temperature: 0~40°C.
- Protect the control board from static, it may cause damage to the IC.
- Disconnect the TV before the power supply of panel is connected correctly.
- Do not drop any metal on the control board when it is working.
- Do not push or pull the connector when the control board is working.
- Do not disassemble the module.
- If the surface or the control board is dirty, clean it with soft dry cloth.
- Can't be pressed and distorted.