UNIVERSITI KUALA LUMPUR

MALAYSIAN SPANISH INSTITUTE

SAB36603

ADVANCE DIGITAL DESIGN AND FPGA

INTRODUCTION TO FPGA EDA TOOL (QUARTUS II)

LAB 1

LECTURER'S NAME: DR MOHD REZAL BIN MOHAMED

PREPARED BY:

NAME	ID	COURSE
MUHAMMAD ADIEL ADAM BIN MOHD NOOR	54222121212	BET AE
KHAIRUL ANWAR BIN KHAIRUL SALLEH	54215121186	BET AE

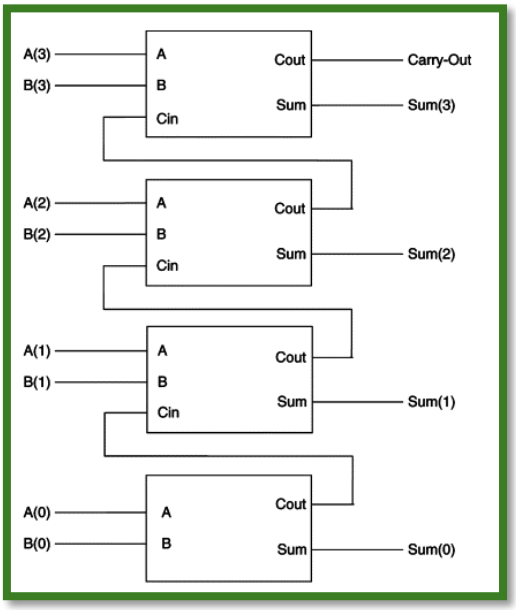
1.0 Introduction

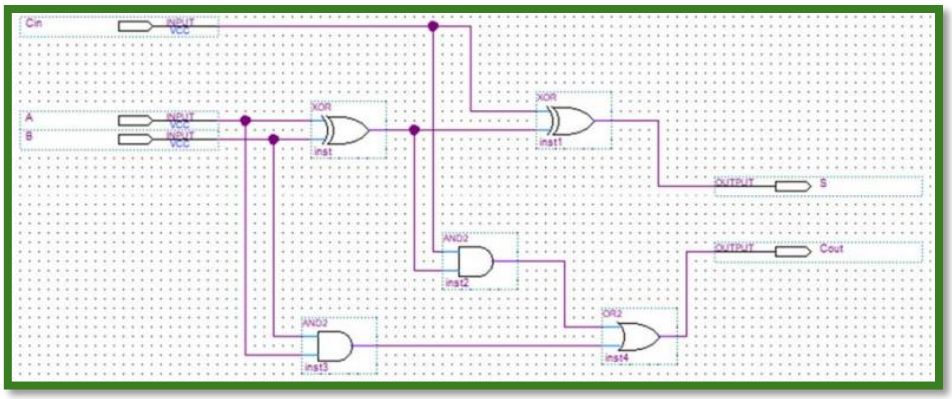
In Quartus II software, a "project" encompasses all design files, configuration details, and hierarchy information. The lab utilizes Block Design Files (*.bdf) to demonstrate the process of developing a full adder project followed by a 4-bit full adder project. The design environment, including the top-down design approach, is introduced using Altera Quartus II. FPGA-based designs are developed using schematic entry methods.

Full Adders are the Digital Logic Circuits used to add three input bits and generate two outputs i.e. the Sum and the resultant Carry.

The further classify the Full Adder into two main types:

- 2-bit Full Adder.
- 4-bit Full Adder.





A 4-bit Full Adder is designed to generate a 4-bit Sum and is designed by combining four 2-bit Full Adders and as a result shows the Four bits output along with the Carry Bit.

2.0 Objectives

The objectives of this lab are as follows:

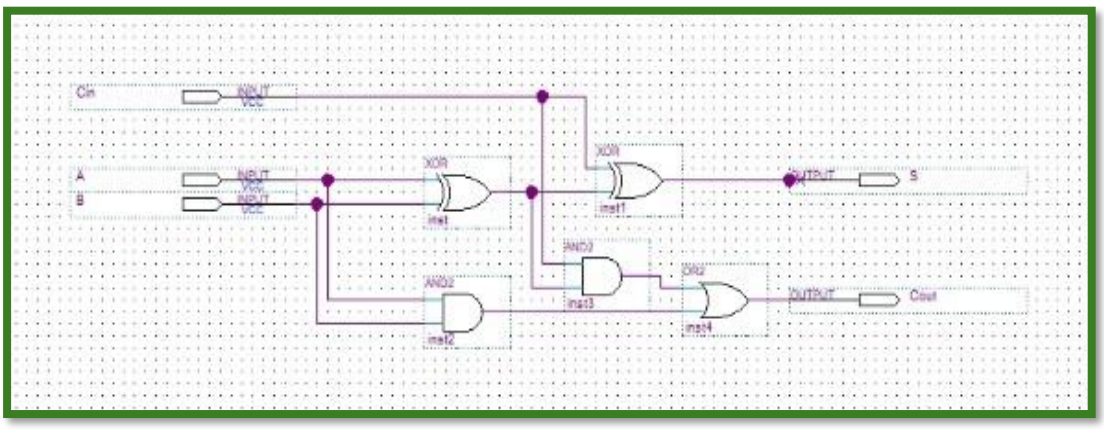
- Learn to create design entries and perform compilation and simulation using Quartus II software.
- Design a simple 4-bit full adder.
- Familiarize with schematic-based design flow for FPGA implementation using logic gates and hierarchical modelling.

3.0 Schematic / HDL Language

3.1 Schematic diagram full_adder.

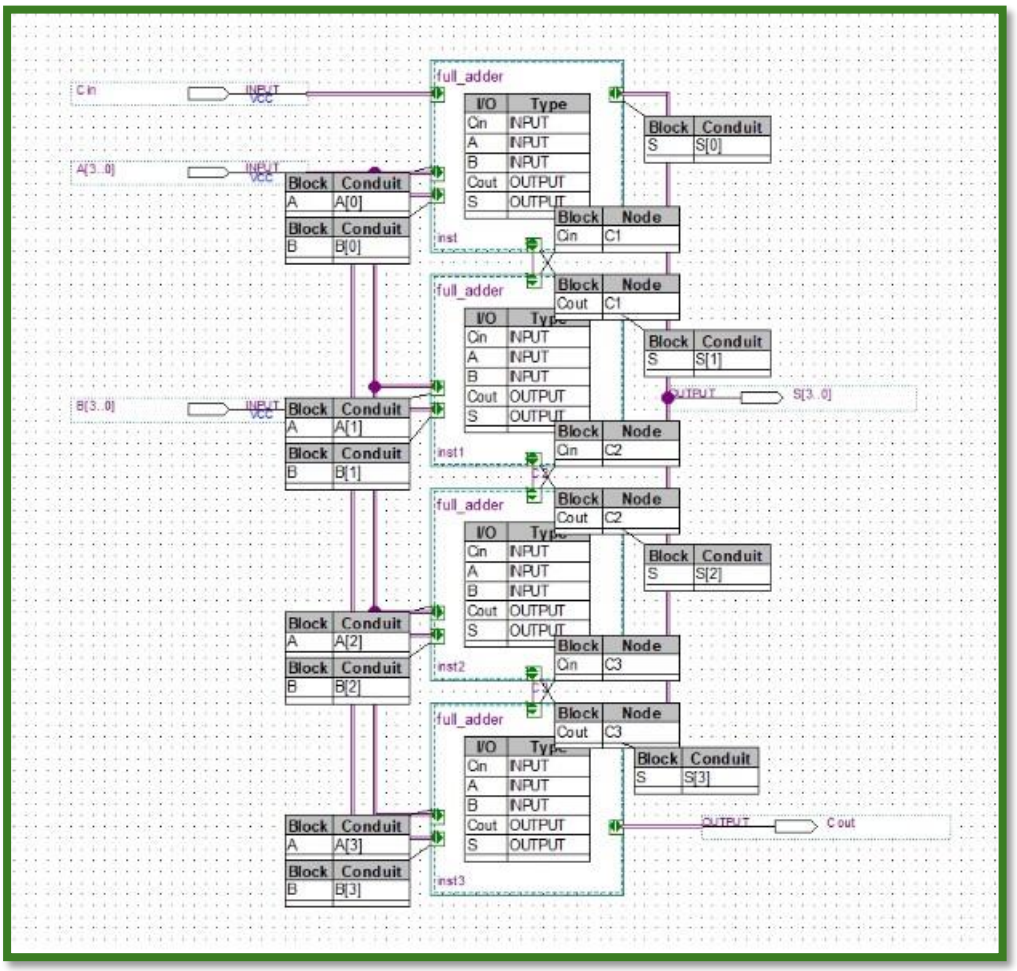
The schematic illustration of a 4-bit complete adder illustrates the complex logic and signal flow required for binary addition in a digital system. The diagram features four interconnected complete adder circuits, each constructed with XOR gates, AND gates, and OR gates to perform precise binary addition.

The input bits, which indicate the operands for addition, are precisely directed to the correct inputs of every entire adder stage. Previous stage carry-in signals are input into the circuit to address carry-over in addition operations with multiple bits. This precise organization guarantees that every whole adder stage handles the right input bits and carry signals to produce correct sum and carry-out signals.



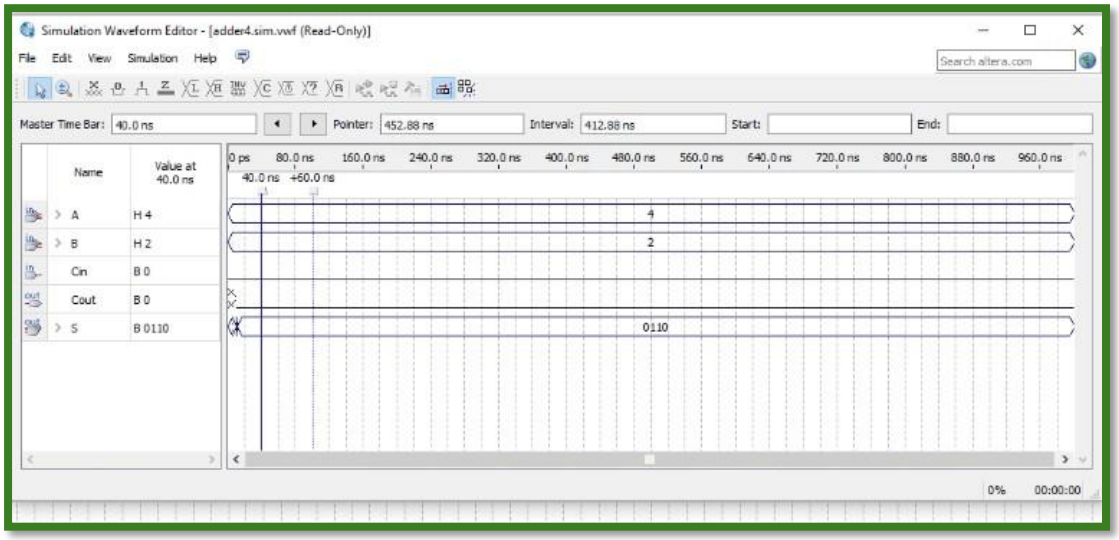
3.2 Block diagram full_adder.

The 4-bit complete adder block diagram is a key component in digital circuit design, particularly in arithmetic units. The figure below demonstrates a methodical method for binary addition using four stages of complete adder circuits. The adder's stages handle two input bits plus a carry-in bit from the previous stage to generate a sum bit and a carry-out bit. The sum bits combine to provide the output of the 4-bit adder, while the carry-out bits enable cascade addition by acting as carry-ins for following stages.



4.0 Simulation Results

Utilizing the **Simulation Waveform Editor** in Quartus II 13.0 software, we obtained the results of a 4-bit full adder, which combines XOR, AND, and OR gates. The diagram accurately records the binary result of 0110 in the output signal 'S'. The inputs A and B represent the 4-bit binary numbers being added, with Cin initially set to 0. However, S represents the least significant 4 bits of the addition result, while Cout signifies the carry-out to the next stage.



5.0 Analysis

The 4-bit full adder operates by combining XOR gates, AND gates, and OR gates to perform binary addition. The simulation results confirmed the functionality of the designed circuit, validating its suitability for addition operations.

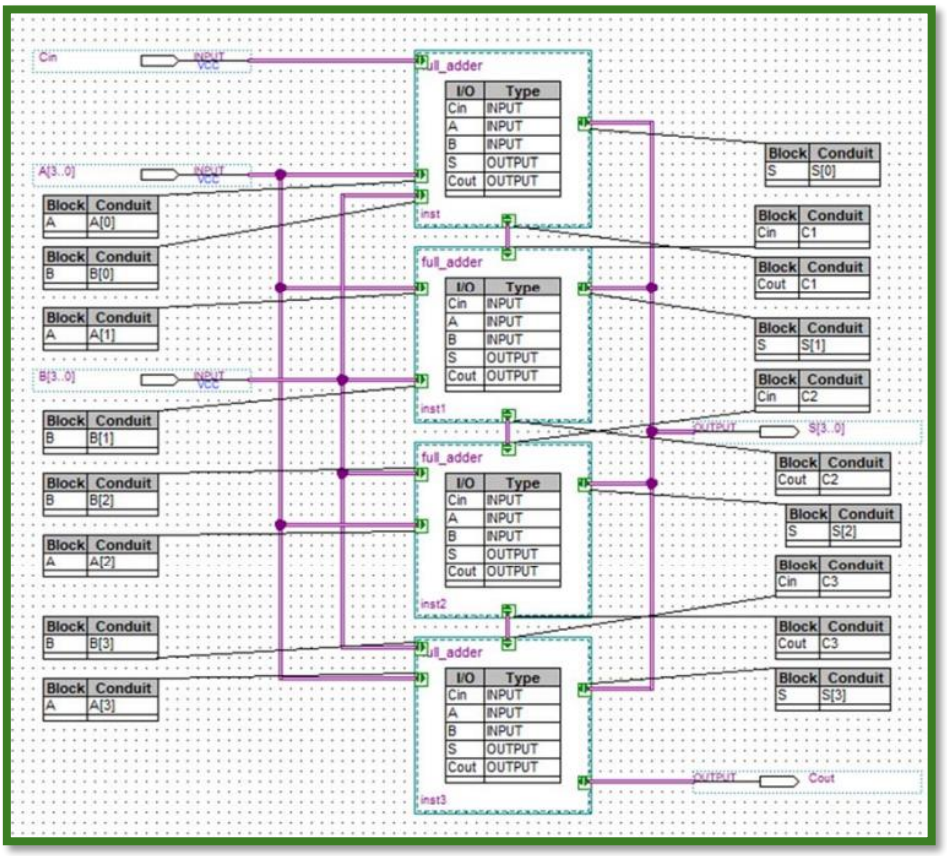
To analyse the 4-bit full adder circuit based on the provided description and simulation waveform, we begin by testing the circuit with a specific example: the addition of two binary numbers, 0100 and 0010. Let A=0100 B=0010

Hence, the result is:

A	0	1	0	0
B	0	0	1	0
S	0	1	1	0

The operation of the 4-bit full adder is when the input bits are combined using XOR gates, and to ensure proper addition, two AND gates are integrated into the circuit to generate a carry, when necessary, which is then fed into the OR gate. To design the circuit, we construct a simple arrangement of AND and XOR gates, forming a basic 2-bit adder. Notably, we replicate this configuration four times, with each block's input

carry serving as its output carry, creating a cascading effect. This process repeats, culminating in the fourth block, where the final carry of the entire calculation is obtained.



6.0 Conclusion

This laboratory provided a comprehensive introduction to the Quartus II software and exemplified the design and simulation process of a 4-bit full adder circuit. By utilizing schematic-based design flow, participants gained valuable insights into the interactions of logic gates and hierarchical modelling essential for FPGA implementation.

The 4-bit full adder circuit demonstrated effective binary addition through the combination of XOR gates, AND gates, and OR gates. Simulation results validated the functionality of the designed circuit, affirming its suitability for addition operations.

In summary, the lab achieved its objectives by equipping participants with the necessary skills to create design entries, perform compilation and simulation tasks, and understand the fundamental concepts underlying digital logic circuits. Through practical implementation and analysis, participants gained hands-on experience in FPGA design, laying a solid foundation for future endeavour in digital design and FPGA programming.