UNIVERSITI KUALA LUMPUR
MALAYSIAN SPANISH INSTITUTE

SAB36603
ADVANCE DIGITAL DESIGN AND FPGA

LAB 3
BASIC LOGIC DESIGN AND I/O INTERFACE

PREPARED BY:

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1. *Introduction*

ME2200 Digital Systems Lab 3 explores the practical implementation of serial data and waveform generation within the realm of digital systems. This lab is structured to provide hands-on experience in designing circuits for generating serial data in a specific format and creating square wave signals with adjustable frequencies. By utilizing FPGA technology and oscilloscope analysis, key concepts such as data transmission, signal processing, and frequency modulation are explored.

Throughout the lab exercises, the creation and deployment of circuits that produce serial data with defined start and stop bits, along with parity bits, will be undertaken. Moreover, the generation of square wave signals with variable frequencies using push buttons for modulation purposes will be examined.

By employing the Altera DE2 Development and Education Board in conjunction with the Keysight MSO6012A/MSO7012A Mixed Signal Oscilloscope, waveforms generated by the circuits can be observed and analyzed. This practical application of digital systems principles aims to reinforce theoretical knowledge and cultivate proficiency in digital systems design and analysis.

ME2200 Digital Systems Lab 3 serves as a platform for exploring the practical aspects of data transmission techniques and waveform generation principles within the context of digital systems.

2. *Objectives*

The objectives of this laboratory are:

- To create designs for serial data and waveform generations and observe the waveforms using an oscilloscope.

Equipment Required:

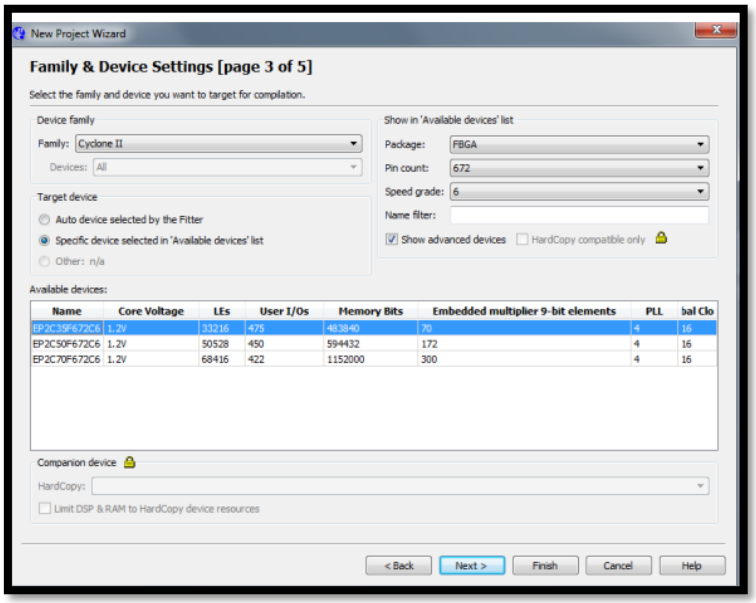
- PC running Microsoft Windows 2000/XP/Vista with Altera Quartus II v13.0 SP1 software.
- Altera DE2 Development and Education Board with a 9 V DC power supply and a USB cable.
- Keysight MSO6012A/MSO7012A Mixed Signal Oscilloscope or equivalent.

3. *Schematic / HDL language*

1) Part A: Creating New Project.

- Create the New Project Wizard, name the project and top-level entity as lab 3.

- In page 3 of New Project Wizard, at the Family list, Cyclone II was selected and make sure the Target device was following the following list:
    1.1 Package FBGA.
    2.1 Pin Count 672.
    3.1 Speed Grade 6.

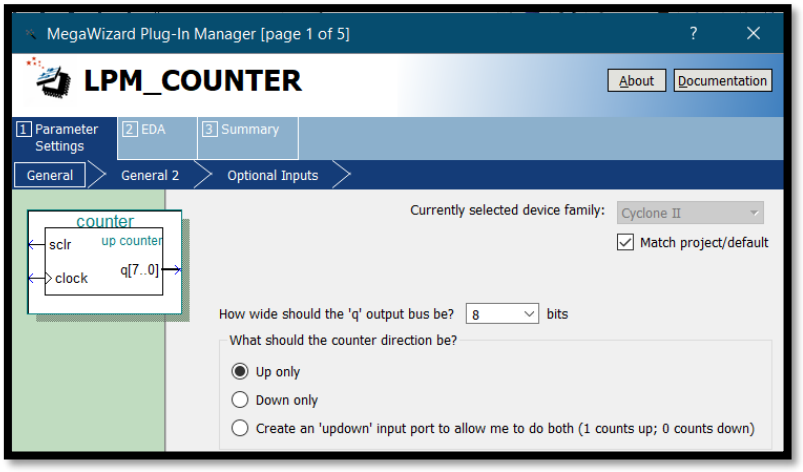


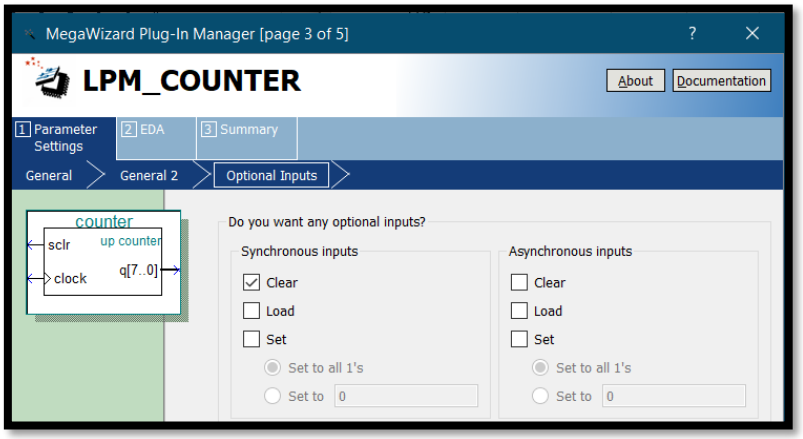
- Click the button Finish if the flows to create the New Project Wizard. Then, create the new BDF called lab 3.bdf.

2) **Part B: Enter counter and comparator symbol that generated by Mega Wizard Plug-In Manager.**

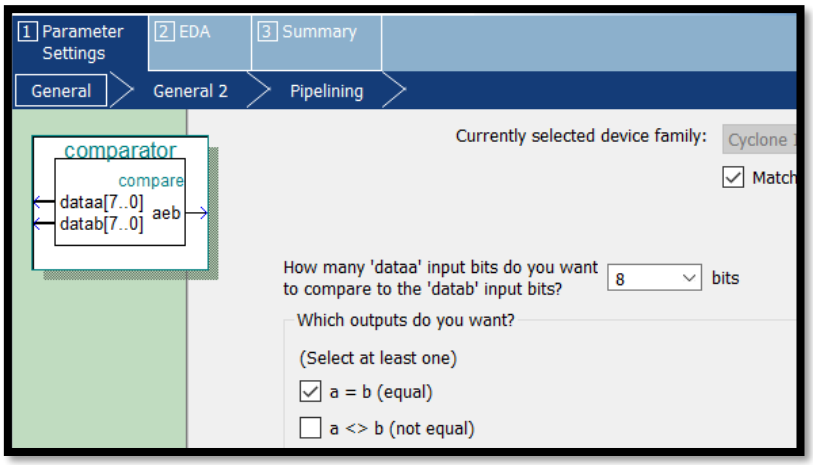
- Double click on empty space in Block editor window.2.
- Then, Mega Wizard Plug-In Manager was clicked. At the first page, create the new mega function. After that, finish the step and the new symbol of counter and comparator were appears.

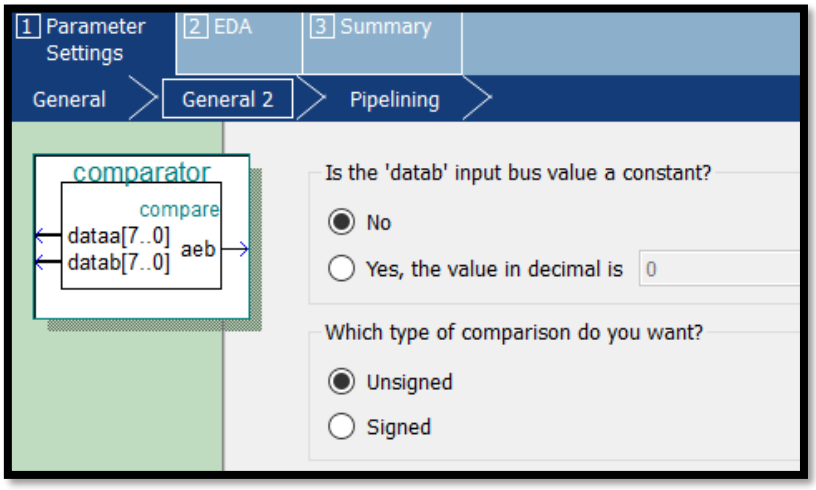
Counter symbol:





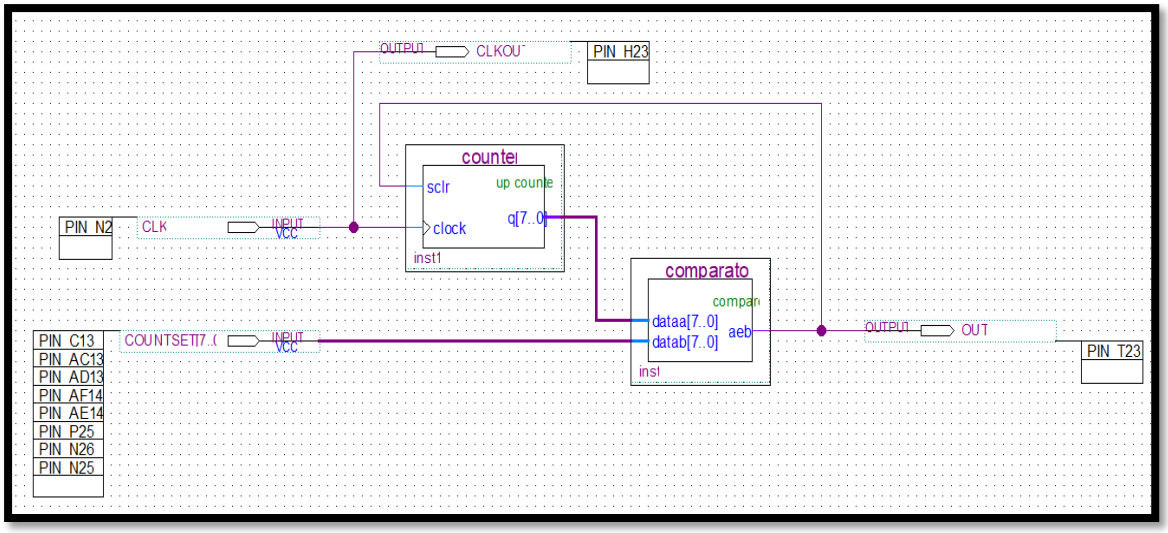
Comparator symbol:





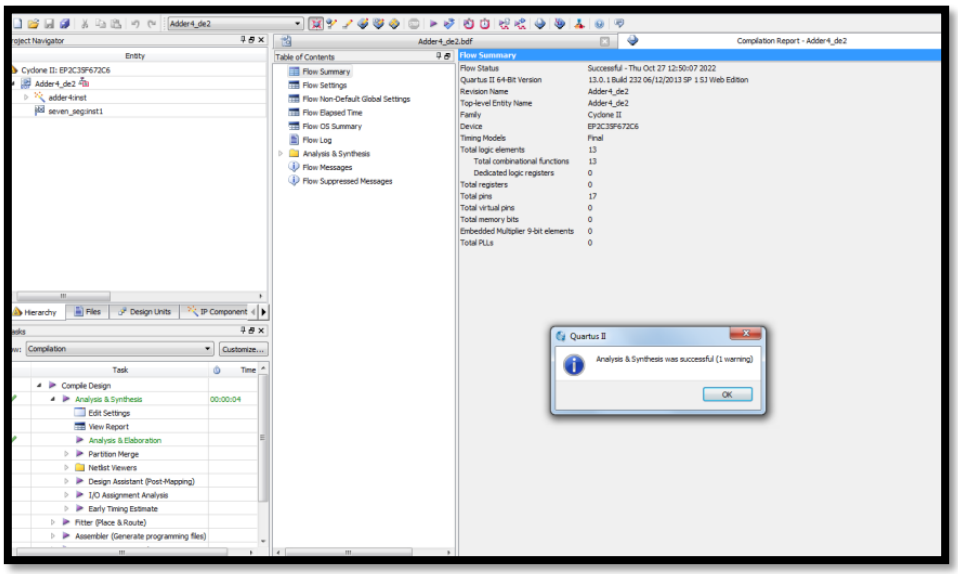
3) Part C: Connecting the counter to the comparator.

The lab 3 circuit was connected as figure below.

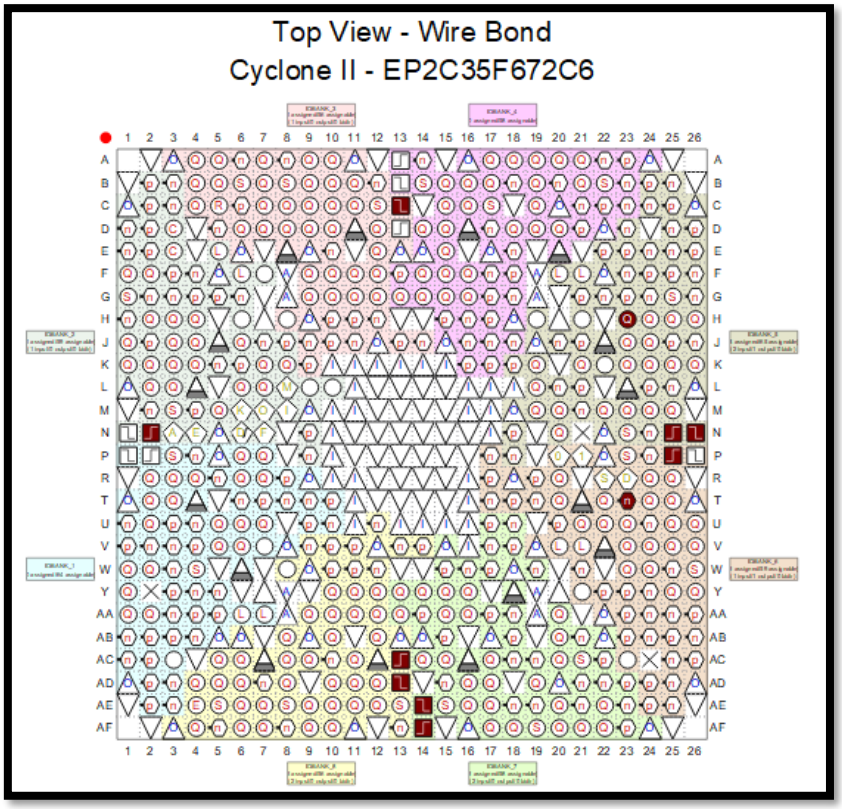


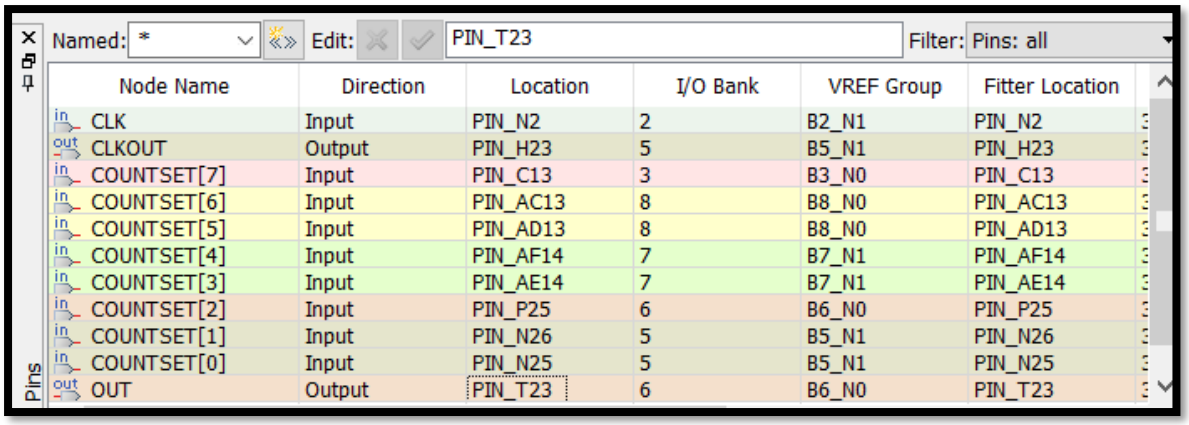
4) **Part D: Pin Assignment.**

- Invoke Start Analysis and Synthesis from the toolbars to generate the project database. The design file must be compiling to detect the error, synthesis the logic and generate a project database.



- The Pin Planner was invoked by select the Assignment>Pin on the schematic windows.
- The figure below shows the all pin that has been assign.

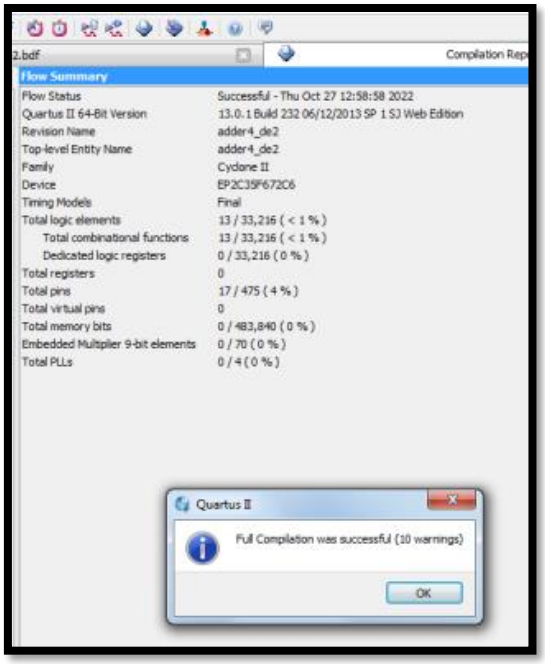


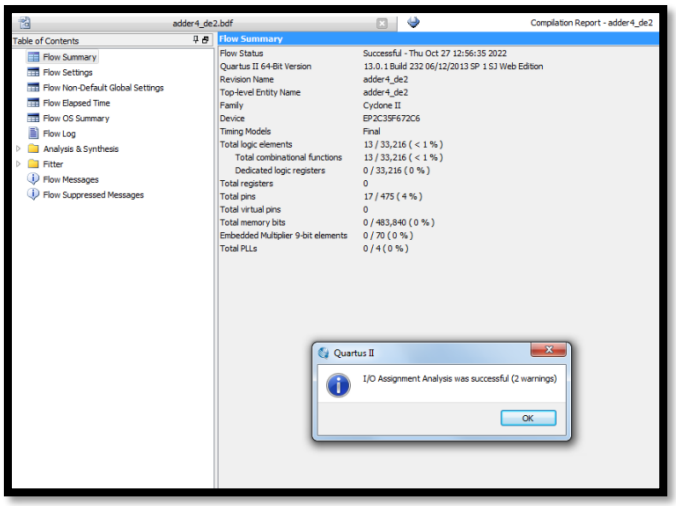


Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location
CLK	Input	PIN_N2	2	B2_N1	PIN_N2
CLKOUT	Output	PIN_H23	5	B5_N1	PIN_H23
COUNTSET[7]	Input	PIN_C13	3	B3_N0	PIN_C13
COUNTSET[6]	Input	PIN_AC13	8	B8_N0	PIN_AC13
COUNTSET[5]	Input	PIN_AD13	8	B8_N0	PIN_AD13
COUNTSET[4]	Input	PIN_AF14	7	B7_N1	PIN_AF14
COUNTSET[3]	Input	PIN_AE14	7	B7_N1	PIN_AE14
COUNTSET[2]	Input	PIN_P25	6	B6_N0	PIN_P25
COUNTSET[1]	Input	PIN_N26	5	B5_N1	PIN_N26
COUNTSET[0]	Input	PIN_N25	5	B5_N1	PIN_N25
OUT	Output	PIN_T23	6	B6_N0	PIN_T23

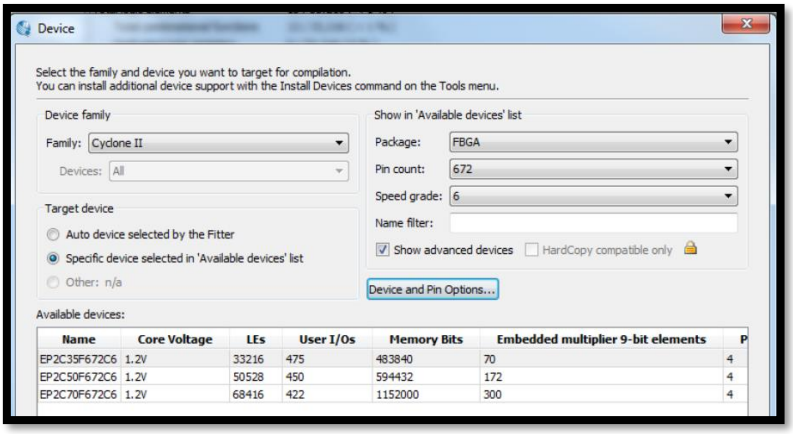
- Perform pin assignment to assign the CLK and COUNTSET input and CLKOUT and OUT output to carry into the toggle switches on the DE2 board.
- For the each connected directly to a pin on the Cyclone II FPGA.
- Consult Appendix A for pin locations and assignments.
- Perform I/O Assignment Analysis to ensure the legality of pin assignment.
- Compile the design.

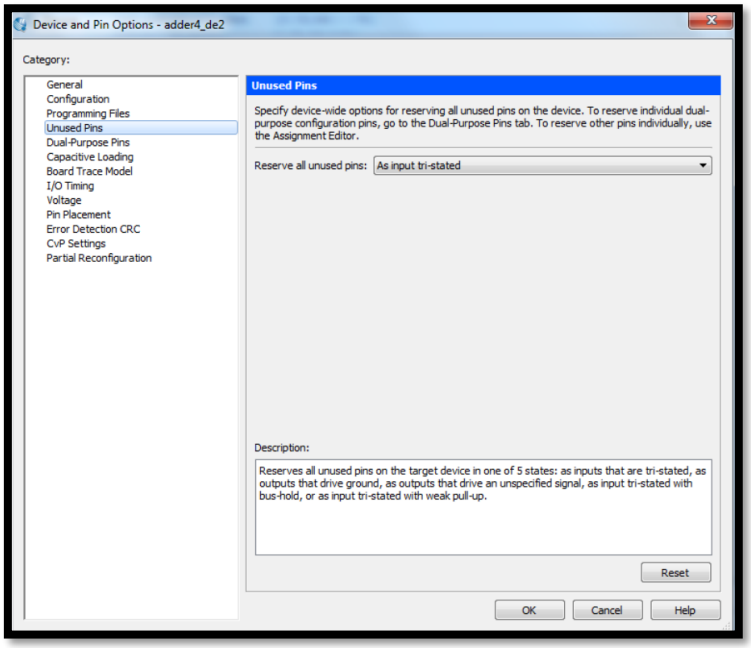
Input Pin Name	Toggle Switch Used	FPGA Pin Number
A[3]	SW[4]	PIN_AF14
A[2]	SW[3]	PIN_AE14
A[1]	SW[2]	PIN_P25
A[0]	SW[1]	PIN_N26
B[3]	SW[8]	PIN_B13
B[2]	SW[7]	PIN_C13
B[1]	SW[6]	PIN_AC13
B[0]	SW[5]	PIN_AD13
Cin	SW[0]	PIN_N25





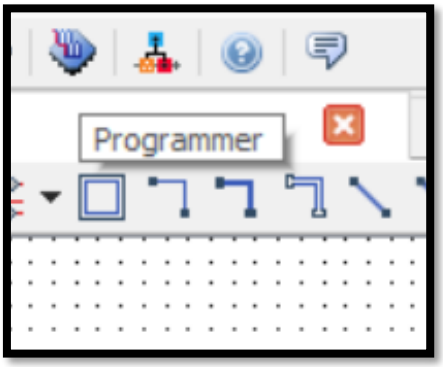
- As a safety measure, configure all unused pins to act as input tri-stated to prevent potential short circuits.

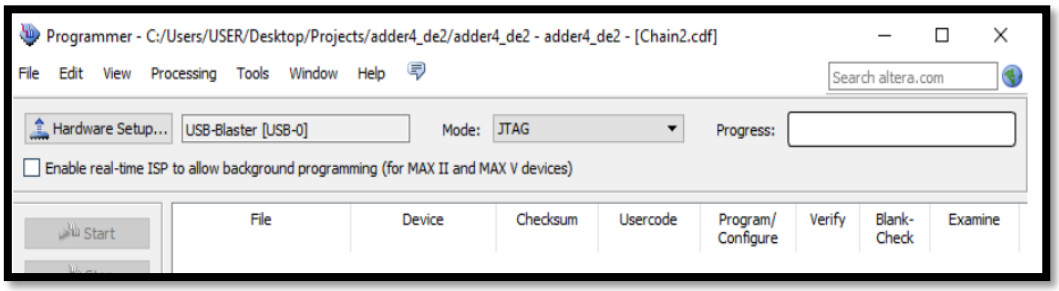


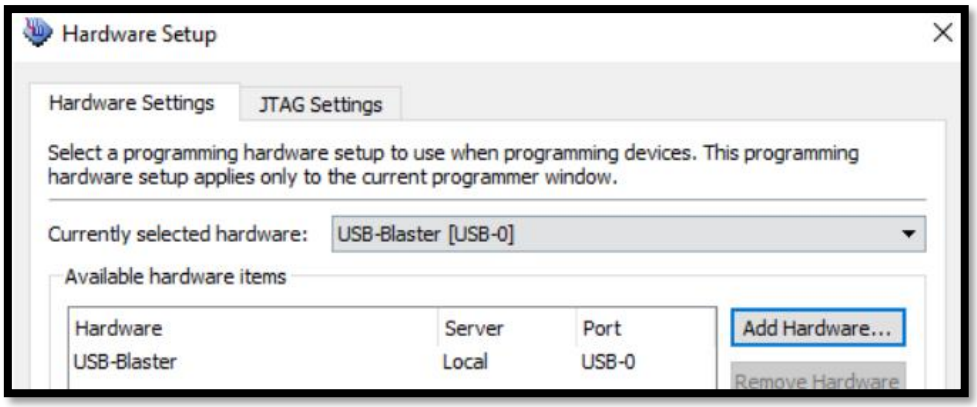


5) Part E: Program the Device

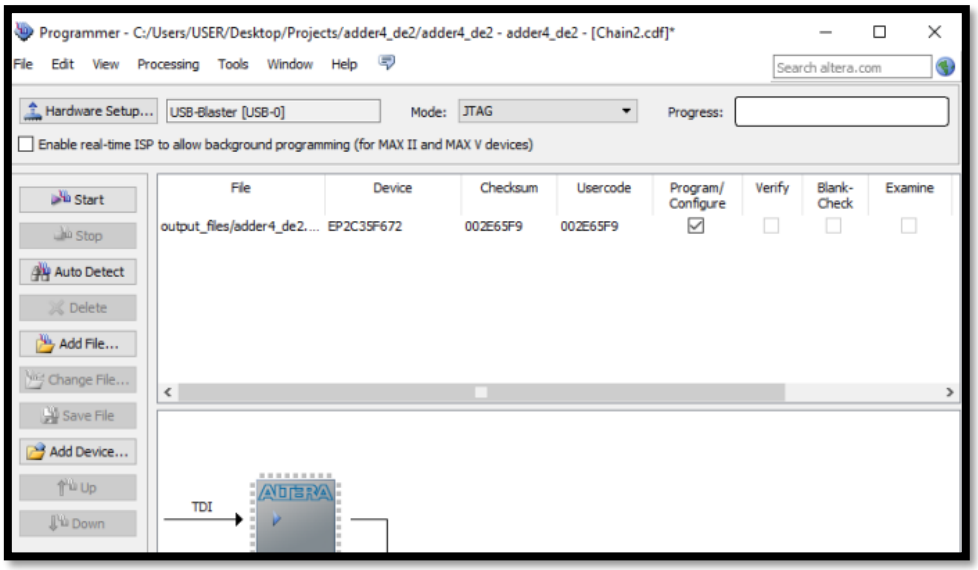
- Connect the USB cable from the DE2 board's USB-Blaster Port to the computer.
- Select the Programmer icon from the toolbar to open the Programmer window, showing the sof file.
- Set the Mode in the Programmer window to JTAG.
- If no hardware is detected, click the Hardware Setup button, and select USB-Blaster.



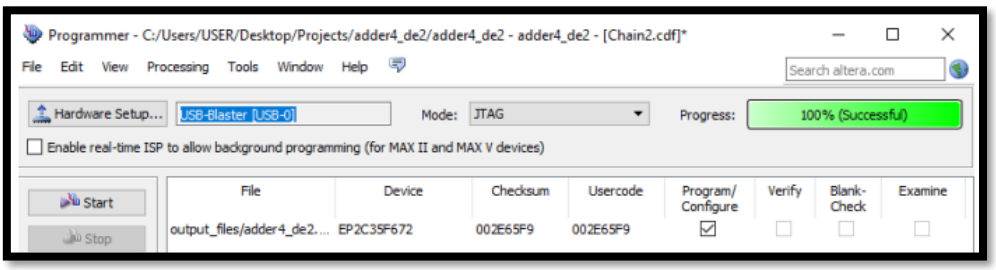




- Mark the Program/Configure checkbox.

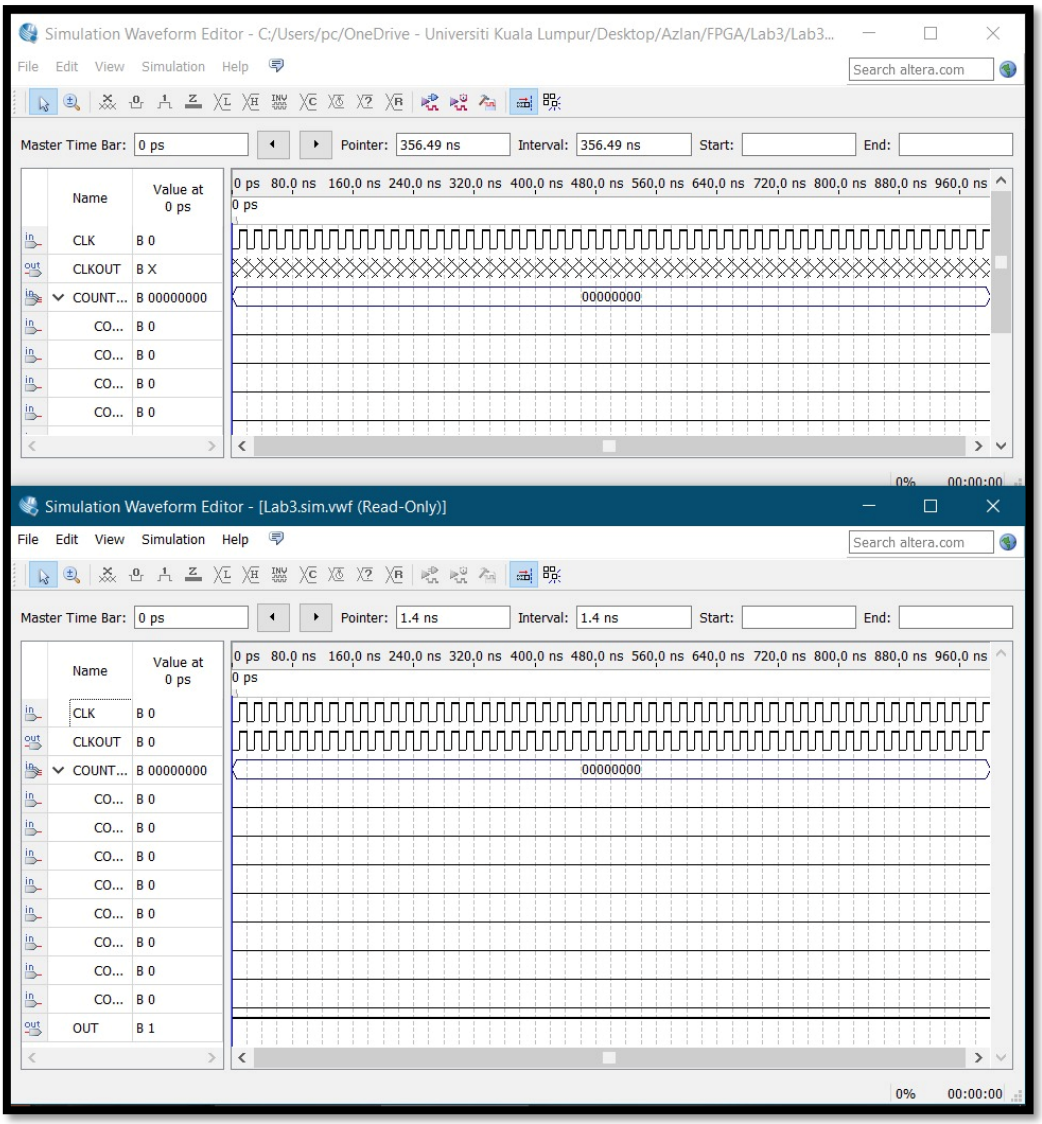


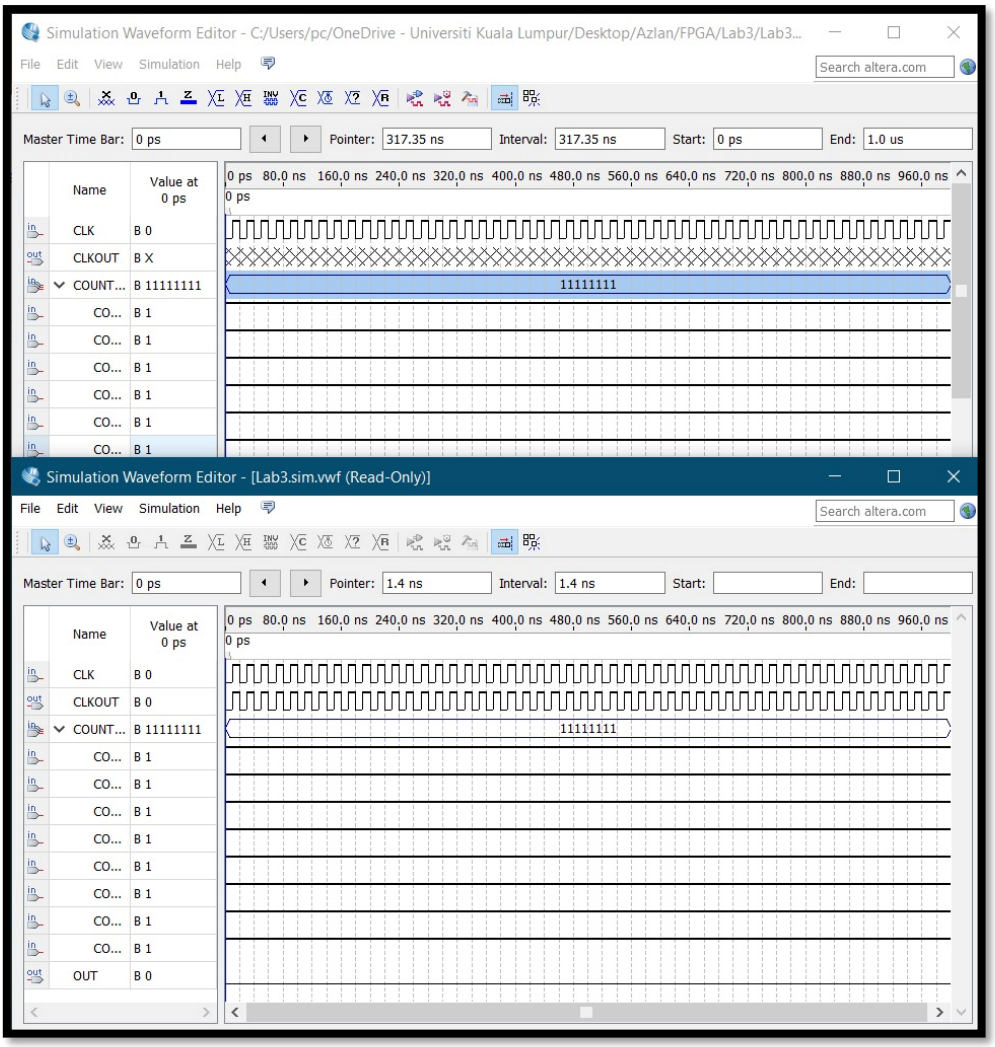
- Click the Start button in the Programmer window to begin the configuration process.
- After receiving a confirmation message indicating completion, click OK.



4. *Result*

Below are the results shown by implementing simulation waveforms in two situations.





The state 11111111 indicates the highest count value (255 in decimal) that an 8-bit counter can reach, signifying the completion of a counting cycle. On the other hand, the state 00000000 represents the starting point or reset state of the counter, marking the beginning of a new counting cycle. These states show the counter's full range from minimum to maximum count values and the transition between counting cycles.

5. Analysis

Waveform Analysis:

This involves examining the waveforms produced by digital circuits, measuring parameters like pulse intervals, and checking the accuracy of the waveforms with oscilloscopes. It's essential for understanding digital signals and ensuring the circuits work correctly.

Frequency Analysis:

In the Variable Frequency Square-Wave Generator task, a circuit that generates an adjustable frequency square wave is created. The frequency changes are analysed using push-button controls to see their effect on the output waveform. This helps in understanding how to manipulate signal frequency in digital systems.

Data Transmission Analysis:

The Serial Data Generation task requires transmitting data in a specific serial format. The transmitted data stream, including start and stop bits, data bits, and parity bit, is analysed to ensure accurate data transmission. This is important for verifying data integrity in digital communication systems.

Comparative Analysis:

Some lab exercises involve comparing calculated values with measured values. For example, in the Interval Pulse Generator task, the expected pulse intervals are calculated and then measured using an oscilloscope. This comparison helps validate calculations and understand any differences between theory and practice.

Error Analysis:

Identifying and analysing any errors during the design and implementation of digital circuits is encouraged. By comparing expected results with actual measurements, potential sources of inaccuracies can be found, circuit issues can be fixed, and design methods can be improved. This process enhances problem-solving skills and understanding of digital systems.

6. Conclusion

By completing the lab tasks and utilizing tools such as Quartus II software, DE2 Development and Education Board, and oscilloscopes, theoretical knowledge can be applied to practical scenarios, circuit designs can be troubleshooted, and waveform outputs can be analysed. The lab encourages critical thinking, problem-solving skills, and hands-on experimentation, fostering a deeper understanding of digital systems and FPGA-based applications.

Overall, the laboratory exercise provides a comprehensive platform for engaging with digital system design, waveform analysis, and FPGA programming, enhancing proficiency in the field of digital electronics and preparing for real-world applications in the industry.