FR. Conceicao Rodrigues College of Engineering
Department of Computer Engineering

2. **A. Realization of Half Adder & Full Adder using Logic Gates.**

B. 4-Bit Adder using IC 7483

1. Course, Subject & Experiment Details

Academic Year	**2023-24**	**Estimated Time**	**Experiment No. 2– 02 Hours**
Course & Semester	**S.E. (Computers) – Sem. III**	**Subject Name**	**Digital Logic & Computer Organization and Architecture**
Chapter No.	**2**	**Chapter Title**	**Data Representation and Arithmetic algorithms**
Experiment Type	**Hardware**	**Subject Code**	**CSC304**

Rubrics

Roll No	**Date of Performance**	**Timeline (2)**	**Practical Skill & Applied Knowledge (4)**	**Output (4)**	**Total (10)**
	Date of Submission				

2. Aim & Objective of Experiment

- To realize Half Adder and Full Adder.
- To design, realize and verify the adder circuit using logic gates.
- To implement 4 bit addition using IC 7483

3. Problem Statement

Design and implement Half Adder & Full Adder.

To verify the operation of IC 7483(4 bit adder)

Implementation of 4-bit adder using IC 7483. Students will learn about the internal structure of IC 7483

4. Hardware Required

A) Power supply, connecting wires.
B) Components: Breadboard, IC 7486, 7408, 7432,7483 LEDs,180Ω resistor.

5. Brief Theoretical Description

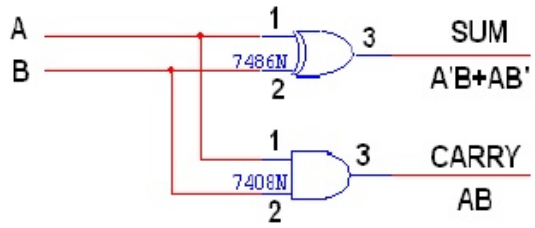
1. ***Half-Adder:*** A combinational logic circuit that performs the addition of two data bits, A and B, is called a half-adder. Addition will result in two output bits; one of which is the sum bit, S, and the other is the carry bit, C.

The Boolean functions describing the half-adder are:

$S = A B' + A'B$

$S = A \oplus B$

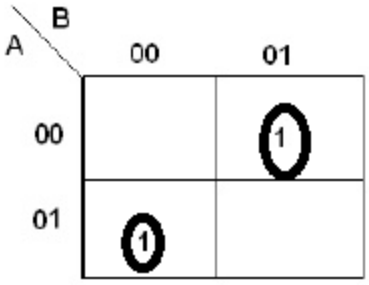
$C = A B$



TRUTH TABLE:

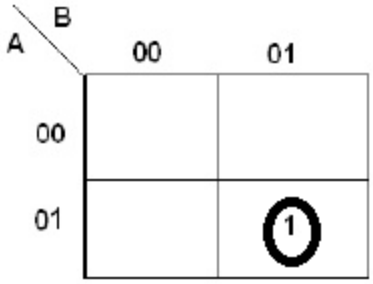
A	B	CARRY	SUM
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

K-Map for SUM:



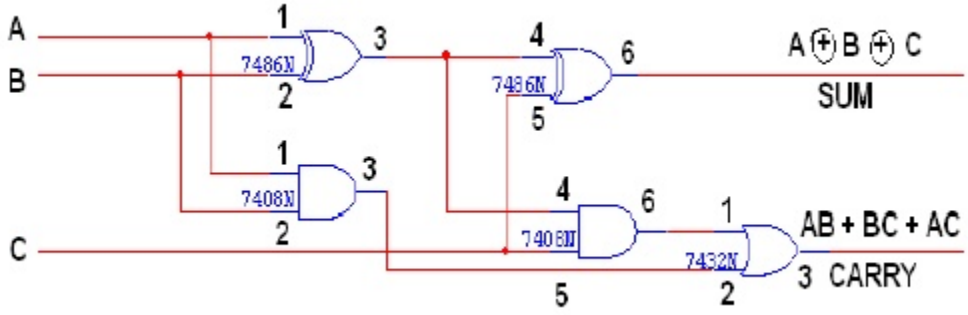
SUM = A'B + AB'

K-Map for CARRY:



CARRY = AB

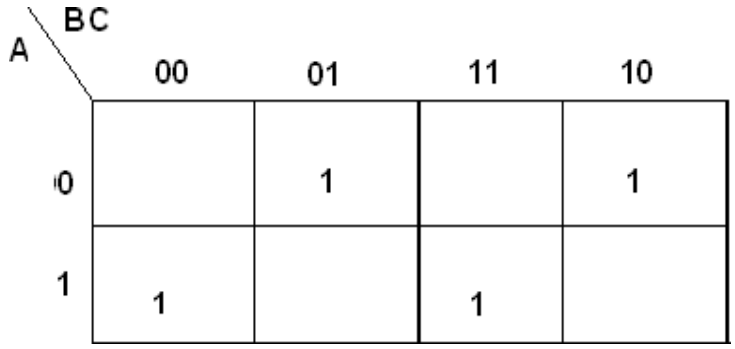
Full-Adder: The half-adder does not take the carry bit from its previous stage into account. This carry bit from its previous stage is called carry-in bit. A combinational logic circuit that adds two data bits, A and B, and a carry-in bit, Cin, is called a full-adder.
The Boolean functions describing the full-adder are:
$S = (x \oplus y) \oplus Cin$
$C = xy + Cin\ (x \oplus y)$



TRUTH TABLE:

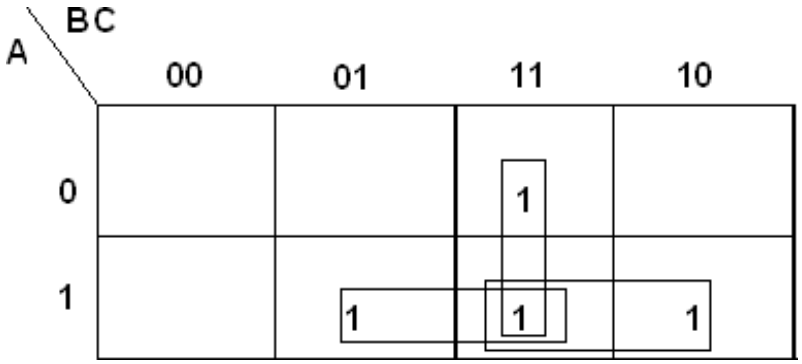
A	B	C	CARRY	SUM
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

K-Map for SUM:



SUM = A'B'C + A'BC' + ABC' + ABC

K-Map for CARRY:



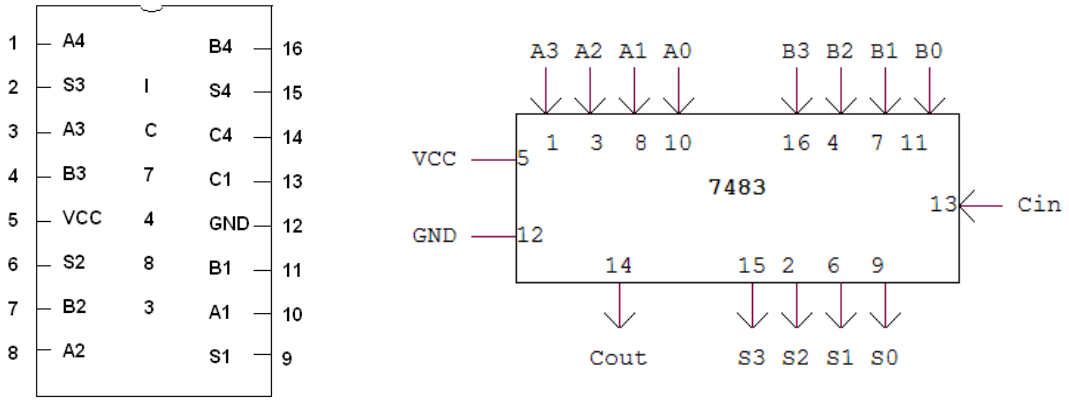
CARRY = AB + BC + AC

SL No.	COMPONENT	SPECIFICATION
1.	AND GATE	IC 7408
2.	OR GATE	IC 7432
3.	NOT GATE	IC 7404
4.	NAND GATE 2 I/P	IC 7400
5.	NOR GATE	IC 7402
6.	X-OR GATE	IC 7486

2. 4 BIT BINARY ADDER:

A binary adder is a digital circuit that produces the arithmetic sum of two binary numbers. It can be constructed with full adders connected in cascade, with the output carry from each full adder connected to the input carry of next full adder in chain. The augends bits of 'A' and the addend bits of 'B' are designated by subscript numbers from right to left, with subscript 0 denoting the least significant bits. The carries are connected in chain through the full adder. The input carry to the adder is C0 and it ripples through the full adder to the output carry C4. 4 BIT ADDER adds two 4 bit numbers A4 A3 A2 A1 and B4 B3 B2 B1 and Cin and result observed as,S4 S3 S2 S1 and output carry denoted as Co.

PIN DIAGRAM FOR IC 7483:



6. Procedure:

Procedure to perform the experiment:

1. Make the connections as shown in the figure.
2. Verify the truth table by giving the various input combination voltages to the input of the IC.
3. Observe the results on the LED.

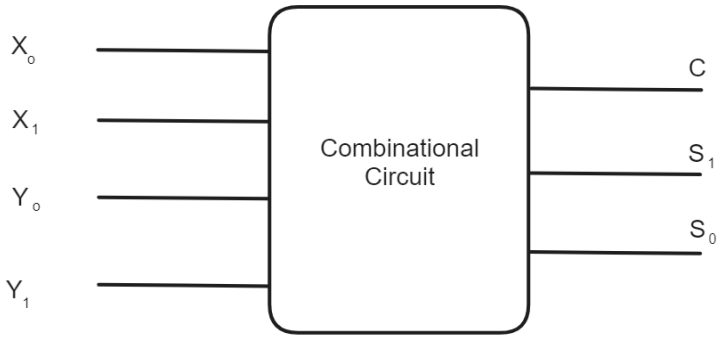
8. Conclusion:

Through this practical we designed and employed logic gates for Half Adder and Full Adder circuits, and efficiently utilized IC 7483 for 4-bit addition.

9. Post-lab:

1. A combinational circuit produces the binary sum of two 2-bit numbers, $X_1 X_0$ and $Y_1 Y_0$. The outputs are C , S1 and S0 Provide a truth table of the combinational circuit.

⇒ Circuit Diagram:

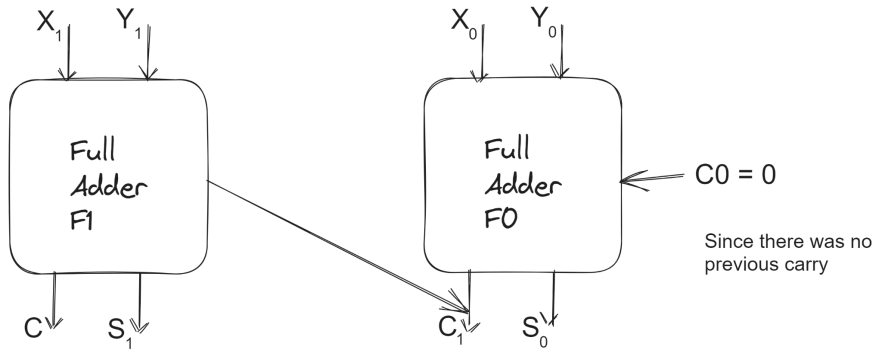


Truth table of the above circuit is:

X1	X0	Y1	Y0	C	S1	S0
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	1	0
0	0	1	1	0	1	1
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	0	1	1
0	1	1	1	1	0	0
1	0	0	0	0	1	0
1	0	0	1	0	1	1
1	0	1	0	1	0	0
1	0	1	1	1	0	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	1
1	1	1	1	1	1	0

2. Design the circuit of above problem no.1 using two full adders.

⇒ The circuit having a full adder for the above problem is given as:



Here C_1 and is the carry from F_0 to F_1 and C is the carry from the table represented by 'C'.