FR. Conceicao Rodrigues College of Engineering
Department of Computer Engineering

4. Ripple Carry Adder

1. Course, Subject & Experiment Details

Academic Year	**2023-24**	**Estimated Time**	**Experiment No. 4– 02 Hours**
Course & Semester	**S.E. (Computers) – Sem. III**	**Subject Name**	**Digital Logic & Computer Organization and Architecture**
Chapter No.	**3**	**Chapter Title**	**Processor Organization and Architecture**
Experiment Type	**Software**	**Subject Code**	**CSC304**

Rubrics

Roll No	Date of Performance	Timeline (2)	Practical Skill & Applied Knowledge (4)	Output (4)	Total (10)
9914	**Date of Submission**				

2. Aim & Objective of Experiment

To Learn how an n-bit Adder can be designed using Full adders.

3. Problem Statement

A) Design a Ripple Carry Adder using Full adders using Simulator. .

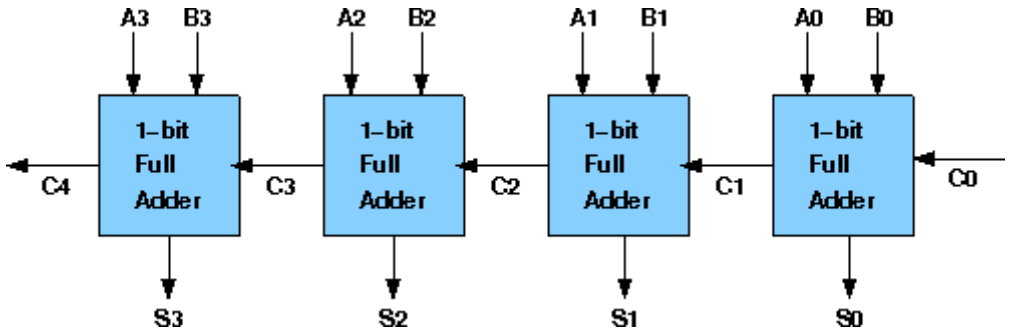
4. Software Required

A) Virtual Lab.

5. Brief Theoretical Description.

Arithmetic operations like addition, subtraction, multiplication, division are basic operations to be implemented in digital computers using basic gates likr AND, OR, NOR, NAND etc. Among all the arithmetic operations if we can implement addition then it is easy to perform multiplication (by repeated addition), subtraction (by negating one operand) or division (repeated subtraction).

Half Adders can be used to add two one bit binary numbers. It is also possible to create a logical circuit using multiple full adders to add N-bit binary numbers.Each full adder inputs a **Cin**, which is the **Cout** of the previous adder. This kind of adder is a **Ripple Carry Adder**, since each carry bit "ripples" to the next full adder. The first (and only the first) full adder may be replaced by a half adder.The block diagram of 4-bit Ripple Carry Adder is shown here below -



The layout of ripple carry adder is simple, which allows for fast design time; however, the ripple carry adder is relatively slow, since each full adder must wait for the carry bit to be calculated from the previous full adder. The gate delay can easily be calculated by inspection of the full adder circuit. Each full adder requires three levels of logic.In a 32-bit [ripple carry] adder, there are 32 full adders, so the critical path (worst case) delay is 31 * 2(for carry propagation) + 3(for sum) = 65 gate delays.

Design Issues :

The corresponding boolean expressions are given here to construct a ripple carry adder. In the half adder circuit the sum and carry bits are defined as

sum = A ⊕B Carry= AB

In the full adder circuit the the Sum and Carry output is defined by inputs A, B and Carryin as

Sum=ABC + ABC + ABC + ABC

Carry=ABC + ABC + ABC + ABC

Having these we could design the circuit.But,we first check to see if there are any logically equivalent statements that would lead to a more structured equivalent circuit.

With a little algebraic manipulation,one can see that

$$\text{Sum} = ABC + ABC + ABC + ABC$$

$$= (AB + AB)\,C + (AB + AB)\,C$$

$$= (A \oplus B)\,C + (A \oplus B)\,C$$

$$= A \oplus B \oplus C$$

$$\text{Carry} = ABC + ABC + ABC + ABC$$

$$= AB + (AB + AB)\,C$$

$$= AB + (A \oplus B)\,C$$

6. Simulation

1- A *Virtual Lab:*

The virtual laboratory is an interactive environment for creating and conducting simulated experiments: a playground for experimentation. It consists of domain-dependent simulation programs, experimental units called objects that encompass data files, tools that operate on the objects.

The objective is to expose the students to various key aspects of Digital Logic and computer organization by enabling them to perform FPGA based prototyping of experiments with support of a virtual environment.

Procedure to perform the experiments

Design of Ripple Carry Adders

1. Start the simulator as directed.This simulator supports 5-valued logic.
2. To design the circuit we need 3 full adder, 1 half adder, 8 Bit switch(to give input), 3 Digital display(2 for seeing input and 1 for seeing output sum), 1 Bit display(to see the carry output), wires.
3. The pin configuration of a component is shown whenever the mouse is hovered on any canned component of the palette or press the 'show pin config' button. Pin numbering starts from 1 and from the bottom left corner(indicating with the circle) and increases anticlockwise.
4. For half adder input is in pin-5,8 output sum is in pin-4 and carry is pin-1, For full adder input is in pin-5,6,8 output sum is in pin-4 and carry is pin-1
5. Click on the half adder component(in the Adder drawer in the pallet) and then click on the position of the editor window where you want to add the component(no drag and drop, simple click will serve the purpose), likewise add 3 full adders(from the Adder drawer in the pallet), 8 Bit switches, 3 digital display and 1 bit Displays(from Display and Input drawer of the pallet,if it is not seen scroll down in the drawer)
6. To connect any two components select the Connection menu of Palette, and then click on the Source terminal and click on the target terminal. According to the circuit diagram connect all the components, connect 4 bit switches to the 4 terminals of a digital display and another set of 4 bit switches to the 4 terminals of another digital display. connect the pin-1 of the full adder which will give the final carry output. connect the sum(pin-4) of all the adders to the terminals of the third digital display(according to the circuit diagram shown in screenshot). After the connection is over click the selection tool in the pallete.
7. To see the circuit working, click on the Selection tool in the pallet then give input by double clicking on the bit switch, (let it be 0011(3) and 0111(7)) you will see the output on the output(10) digital display as sum and 0 as carry in bit display.

After building the circuit press the simulate button in the top toolbar to get the output

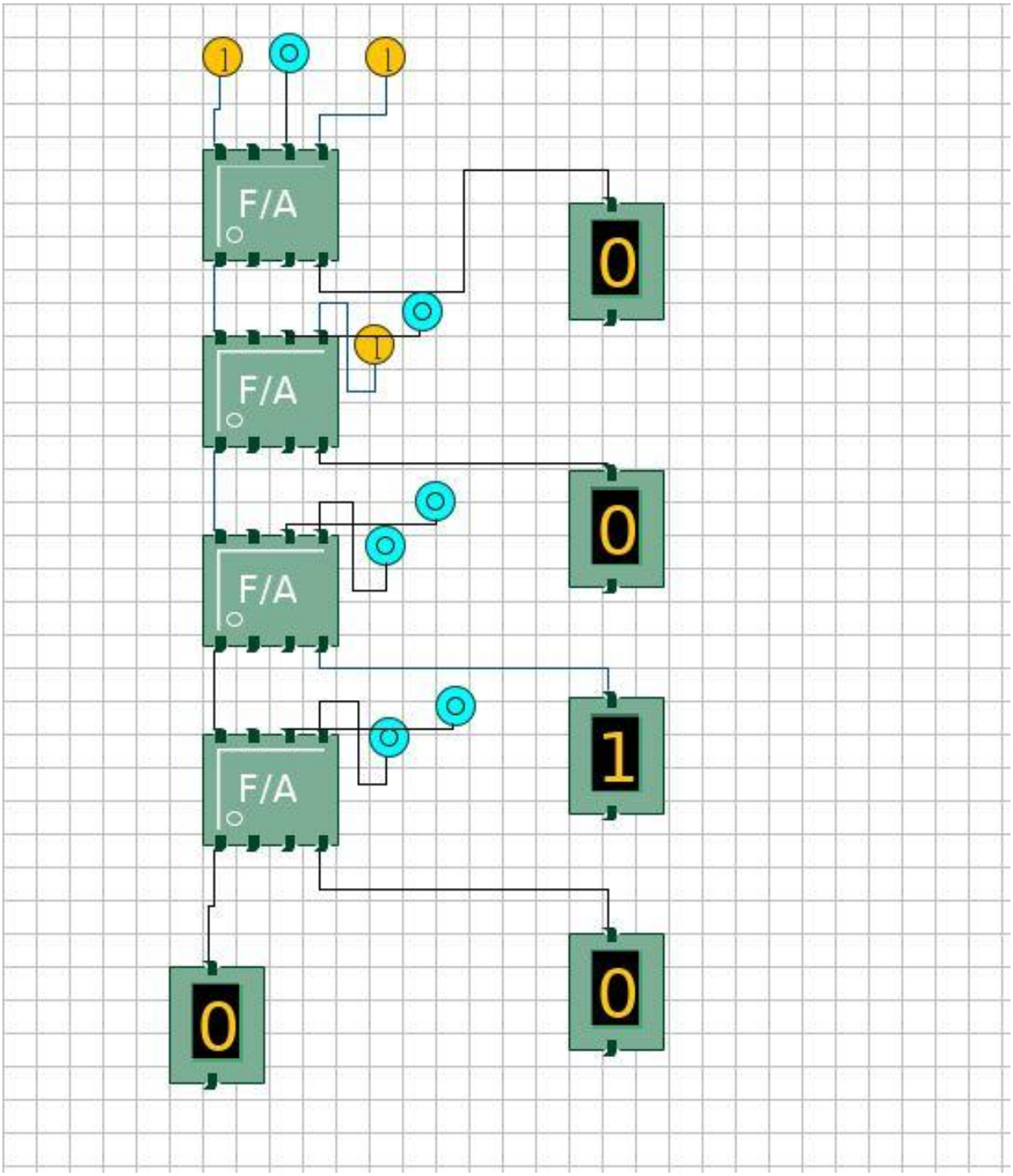
7.Components :

The components needed to create 4 bit ripple carry adder is listed here -

- 4 full-adders
- wires to connect
- LED display to obtain the output

8. Conclusion

An n-bit ripple carry adder can be made by cascading (n-1) full adder. The carry is forwarded to the next adder, thus creating a ripple effect. A demonstration can be seen in the below diagram:



9. Post-lab:

Explain Carry Look Ahead Adder .Give its advantage.

⇒A carry look-ahead adder (CLA) is a type of adder that can add two binary numbers much faster than a ripple-carry adder. A ripple-carry adder generates the carry bit for each stage of addition one at a time, which can take a long time if the numbers are large. A CLA, on the other hand, generates all of the carry bits at the same time, which can significantly reduce the overall addition time.This makes CLAs ideal for applications where speed is critical, such as digital signal processing and computer arithmetic.

Here are some of the advantages of a carry look-ahead adder:

- It is much faster than a ripple-carry adder.
- It can be used to add any number of bits.
- It is relatively easy to implement.
- It is reliable and has a low error rate.
- It is efficient for large additions.
- It has a regular and predictable structure making it easier to design and optimize.