1. Introduction

In this lab you will be designing the 4-bit adder circuit which will form one stage of the combinational logic required to build the complete 8-bit pipelined adder.

2. 4-bit Adder.

Making this design will be easier than that of 1-bit full adder since there is very little routing to be performed.

- After completing the design of the 1-bit full adder, please create another layout view where you will place 4-bit adder layouts.

- Repeat the same procedure as in the previous sections by placing the blocks and routing the appropriate nets to make the required connections. (**Please try not to use metal layers higher than M4.**). Then, complete the DRC check, perform LVS, and then verify the circuit operation by performing post-layout simulations.

Report Requirements:

1. The report should contain the schematic, layout, and LVS reports of your 4-bit adder.

2. Please turn in the waveforms of the outputs of your 4-bit adder after post-layout simulation for the following inputs. Please make sure if your output results are logically correct, and try to clearly show the results.

    - A=0000, B=1111, Carry In=1
    - A=1010, B=0101, Carry In=0
    - A=1010, B=0101, Carry In=1
    - A=1100, B=1000, Carry In=0

    For each input vector, please configure all pulse voltage sources at inputs to be switching. For example, given an input vector A=0000, please set the initial voltages of pulses at the 4-bit input A as all '1's (VDD). Then, A will switch from A=1111 to A=0000 in the waveform plot. In this way, we can correctly measure delay from each vector. Please apply this to all inputs: A, B, and Carry In. Please set all inputs to switch at the same time.

    Following the above direction, all the inputs will be switching in each case. So, when you plot waveforms to include it in your report, you don't need to include all the input signals in the waveform plot, since every input will switch. Please do verify if the results are yielding correct answers after every input switches.

    Measure delay on every output pin for each case. Also measure the power consumption from VDD for each case.