Additional Instructions for Lab 7

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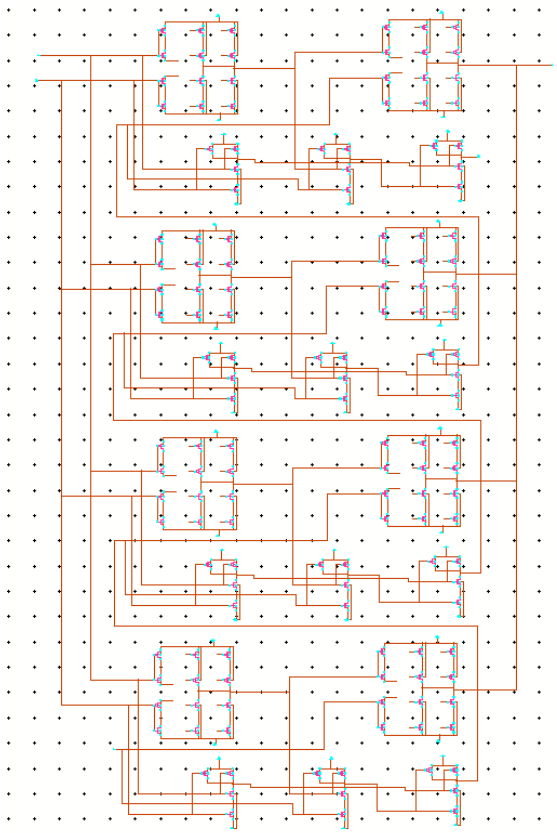
1 Identify the critical path

This is a sample of the transistor level schematic of the 4-bit adder:



First, you should design your own transistor level schematic by substituting the blocks in your previous 4-bit adder design with the schematics of NAND2 and XOR2. You can put the new schematic in a new cell and create a symbol for it. Once you complete the design of the schematic, you can design and perform

pre-layout simulations to verify if the design is logically or functionally correct. Please refer to Lab 4 for the instructions of the simulation. The only difference between pre-layout and post-layout simulation is the environment setup. You shouldn't add the "extracted" in your simulator environment settings.

Second, please identify the critical path on your schematic. The critical path is a logical path from an input pin to an output pin on your circuit that involves most logic gates. In the sample above, the critical path starts from one XOR2 and goes through 8 NAND2.

2 Logical Effort Calculation and Optimization

(Complete the following equations and decisions. It is the process of logical effort calculation and optimization.)

According to the sink capacitance measurement in Lab 3, look up the values of C_{xor} and C_{nand2} for your gate designs.

Compute g_i for the gates on the critical path: $g_1 = g_{xor} = 4$, $g_{2,3,...,9} = g_{nand2} = (w_p + w_n)/(w_p + w_n/2)$. Here w_p and w_n are the width of PMOS and NMOS in NAND2, respectively.

Compute $G = \prod g_i$.

Compute $H = C_{load}/C_{xor}$. According to the lab manual, $C_{load} = 30fF$.

Compute the branching effort: $b_i = \frac{C_{on-path}+C_{off-path}}{C_{on-path}}$, and $B = \prod b_i$.

(Hint:$b_2 = b_4 = b_6 = b_8$ and $b_3 = b_5 = b_7 = b_9$)

Compute $F = GBH$ and $\hat{f} = F^{1/9}$.

If $\hat{f} < 2.7$ or $\hat{f} > 4$, manipulate F (mainly B) by theoretically resizing either NAND2 or XOR2. (Hint: derive F in terms of C_{xor} and C_{nand2} and assume that sink capacitance is proportional to the transistor size.)

If $2.7 \leq \hat{f} \leq 4$, perform the following resizing:

For the i-th gate, i=9,8,7,...,1, calculate: $C_{in,i} = g_i C_{out,i}/\hat{f}$

If $C_{in,i} \leq C_{gate}$, keep the size. Otherwise resize the i-th gate by $C_{in,i}/C_{gate}$ times the old size. (Update the sizes in your schematic only.)

3 Report

Include your transistor level schematic and draw a line on it to indicate the critical path.

Please report 4 optimized *pre-layout* simulation waveforms for the following input vectors:

A=0000, B=1111, CarryIn=1:
A=1010, B=0101, CarryIn=0:
A=1010, B=0101, CarryIn=1:
A=1100, B=1000, CarryIn=0:

And complete the following tables:

Delays:

Case	Pin	Non-optimized (ps)	Optimized (ps)
A=0000 B=1111 Carry In=1	SUM.0		
	SUM.1		
	SUM.2		
	SUM.3		
	CARRY		
A=1010 B=0101 Carry In=0	SUM.0		
	SUM.1		
	SUM.2		
	SUM.3		
	CARRY		
A=1010 B=0101 Carry In=1	SUM.0		
	SUM.1		
	SUM.2		
	SUM.3		
	CARRY		
A=1100 B=1000 Carry In=0	SUM.0		
	SUM.1		
	SUM.2		
	SUM.3		
	CARRY		

Power consumptions:

Case	Optimized (uW)	Non-optimized (uW)
A=0000, B=1111, CarryIn=1		
A=1010, B=0101, CarryIn=0		
A=1010, B=0101, CarryIn=1		
A=1100, B=1000, CarryIn=0		

Area:

Optimized (u^2m^2)	Non-optimized (u^2m^2)