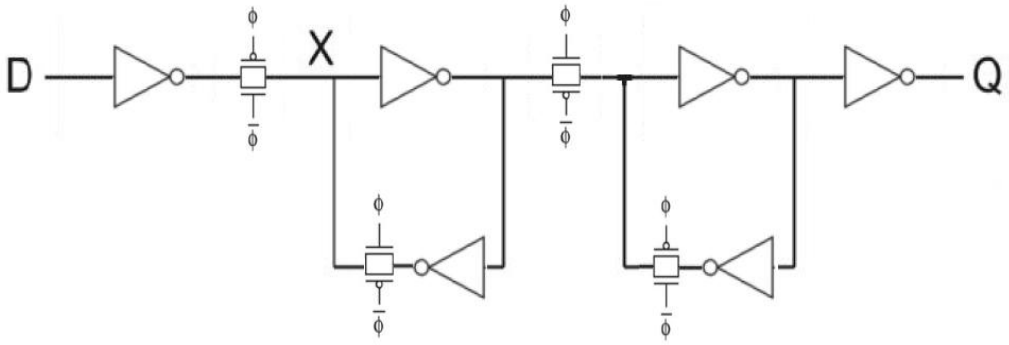
1. Introduction

After completing the design of a single combinational stage of the design, you will next design the basic sequential element that will be used in the design, i.e., the Flip-Flop (FF). In this lab you will be required to design Flip-Flop and also characterize its delay, input capacitance and its setup and hold time.

2. Design of a Flip-Flop

- A Flip-Flop is built from a pair of back-to-back latches. These latches operate on the opposite edges of the clock signal and are called the Master and Slave respectively. The Master latch is the one that receives the input at one edge of the clock (negative/positive) and the Slave latch will transfer the output of the Master latch to the output on the opposite phase (positive/negative) of the clock.

- A sample schematic of static Flip-Flop is given below. Please clearly see how the clock signals, $CLK(\phi) or\ \overline{CLK}(\bar{\phi})$ and pass gates are connected.



- Design and implement the layout of the above schematic. Clearly observe how the pass gates are controlled through $CLK(\phi) or\ \overline{CLK}(\bar{\phi})$.
- In both schematic & layout, be sure to **connect the substrate contact of each transistor to VDD/GND**, even though the transistor composes pass gate where neither of drain and source of the transistor is connected to VDD/GND.
- **A symbol of Flip-Flop will have both** $CLK(\phi) and\ \overline{CLK}(\bar{\phi})$ **inputs**, so you don't need an inverter inside to generate $\overline{CLK}(\bar{\phi})$.
- Simulate (thru analog simulation) the transistor level schematic first before designing layout in order to verify in advance if your schematic is working correctly. As you implement the layout design, please make sure you continuously check for DRC errors.

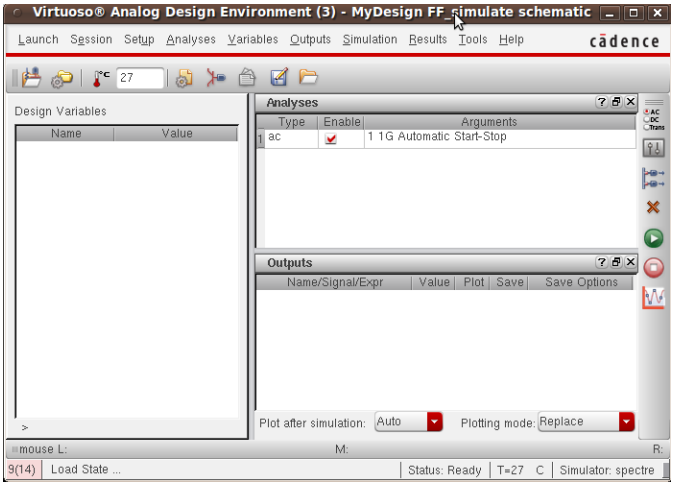
- Perform DRC and LVS checks. Then do the post-layout simulations on your design. Provide a rising D input and a clock (with its complement) to your FF to see if you get the corresponding rising Q output. Check for the falling D input as well. This will ensure that your design is working fine.

3. Characterization

To characterize your Filp-Flop design, you may use the test circuit that you use to perform the post-layout simulations.

- **Cell Delay Table:** Vary the load at the output of the FF from 1fF to 100fF and find the rising and falling delays of the FF. Note that you have to find the **clock-to-Q** delay of the circuit, since the FF latches the new value only at the active edge of the clock. Also size the transistors such that the rising and falling delays when the output load is 100fF may not have a difference of more than 10%.

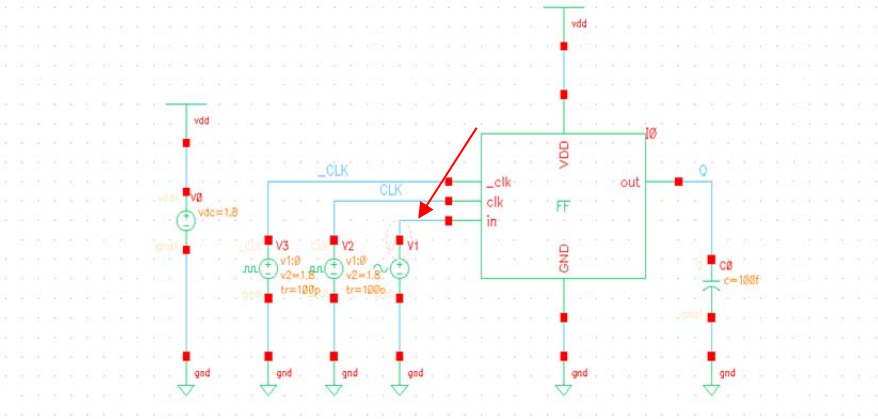
- **Input Capacitance:** Use the method we used in Lab3 to find the input capacitance of the FF. This may be done by placing **vsin**, a sinusoidal voltage source (Vdc=0V, magnitude=1) at the D input of the circuit. Then instead of performing a transient analysis of the circuit, we perform an **ac** analysis which can be chosen by Analyses > Choose. Then select "**ac**" and type in start frequency of 1 and end frequency of 1G. (Make sure that this is the only kind of analyses performed. You may get rid of the transient analysis by choosing the Analyses type in the simulation window and then selecting Analyses > Delete. The Analog Design Environment window will now look as below.



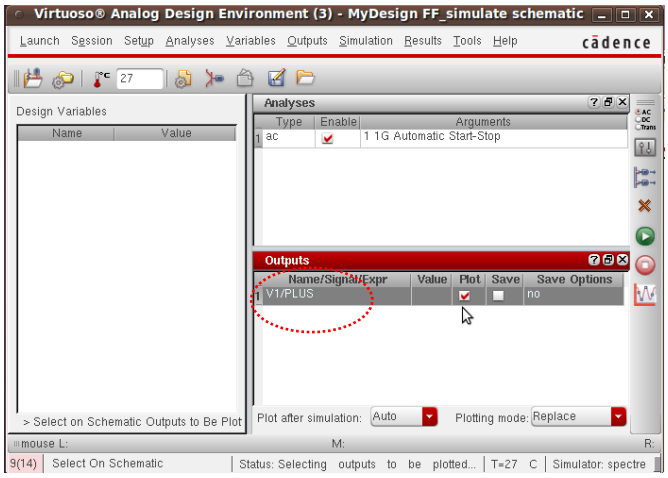
To calculate input sink capacitance, we need to get current waveform which depicts current following into the input D. In your schematic, the sinusoidal voltage source (**vsin**) is attached to the input D, therefore we need to see the current from **vsin**.

In the Analog Design Environment window, select "Outputs > To Be Plotted > Select On Schematic". In the schematic window, click on the "+" terminal of **vsin** which is connected to the input D. A circle will be marked on the terminal as seen in the figure

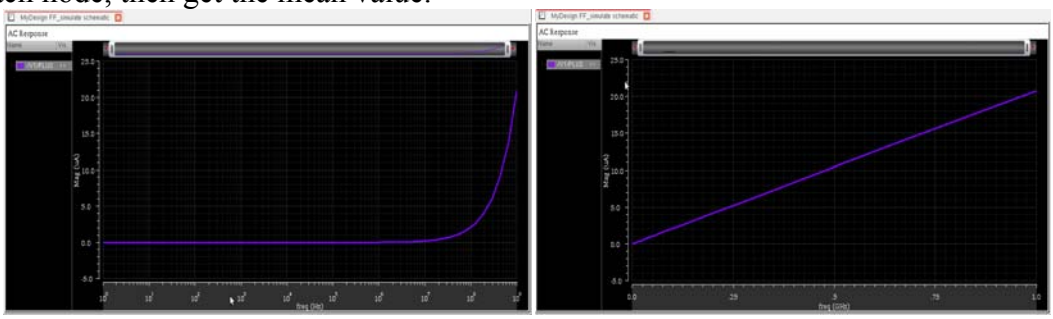
below.



The output list in Analog Design Environment window will look as below. If you want to keep the simulation results, please also check the *Save* option in the *Output* panel.



Run simulation, and you will see a waveform which shows current into the input D vs. frequency. Then the waveform would show like left picture below, single click x axis "freq(Hz)" and choose Axis->Log to make it looks linear as shown right. Next step to calculate input sink capacitance is as given in Lab 3 manual. You need to choose 10 points, get frequency, current for each point, calculate capacitance using $C=I/2\pi f$ for each node, then get the mean value.



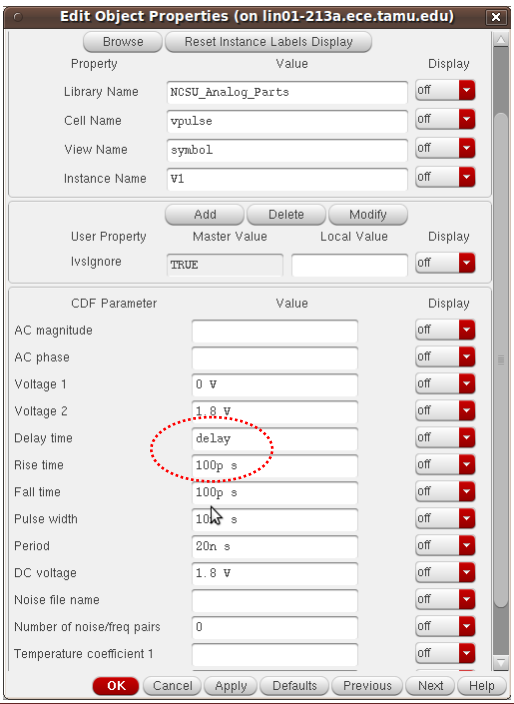
- **Setup Time:** It is the time required for the input data signal at a Flip-Flop to be valid before the incoming clock edge arrives. To measure the setup time of your device you will have to measure the **clock-to-Q** delay of the flip-flop by varying the time gap between the D input and the clock's rising edge. You will have to begin with the D input arriving much earlier than the clock rising input and measure the delay for this case, following which you have to **bring in the D input closer to the 'CLK' input and measure the delay at each step**. Continue this until the FF reaches a meta-stable state, i.e., the FF will give an erroneous output. This can be simply observed when either:
  a) The D input does not cause a change in output in the present clock cycle
  b) Or the **clock-to-Q** delay increases drastically
  c) Or there are oscillations in the output between 0 and 1.

  You are more likely to observe either a) or b).

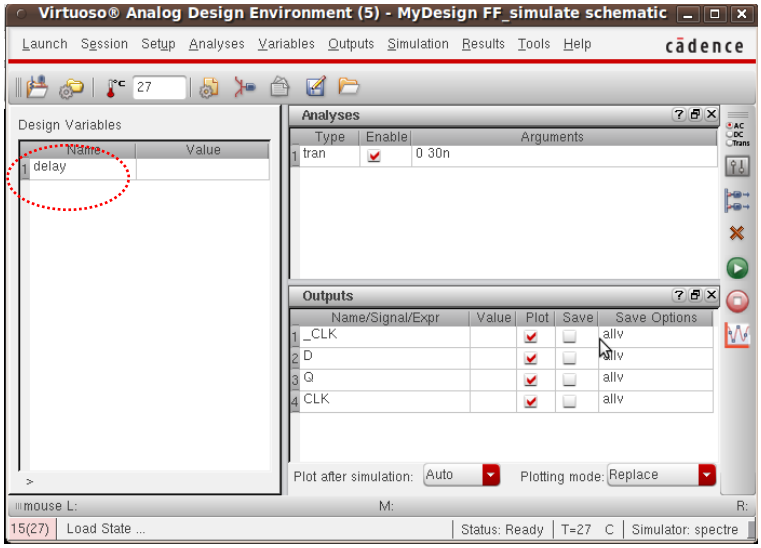
  Now measure the setup time at this point by finding the time difference between the D input and clock input.

  Repeat this procedure for both the D input rising and falling cases. The longer of the two setup times obtained will be the setup time of the FF. (*Optional: You can do **parametric simulations** to view multiple results. Use a parameter for whatever value you would be changing. Set up analog environment as before. Copy variables from cell view. Then go to tools->parametric analysis. Enter the variable name, variable limits and number of steps. Choose Analysis-start to begin the simulations. You can view the simulation results as before*)

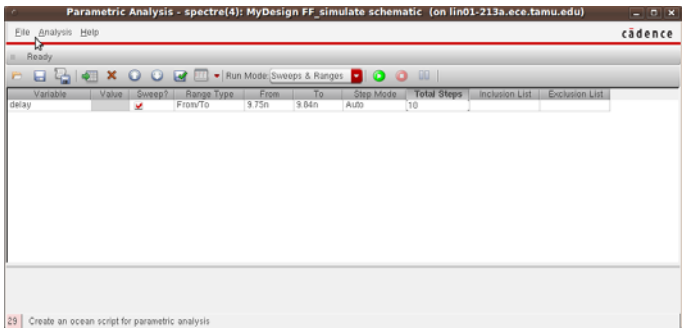
  Follow the steps below to run parametric simulation.
  - Open property window of the **vpulse** connected to the input D. In the "Delay time" option, please type "delay". The property window will resemble as below.



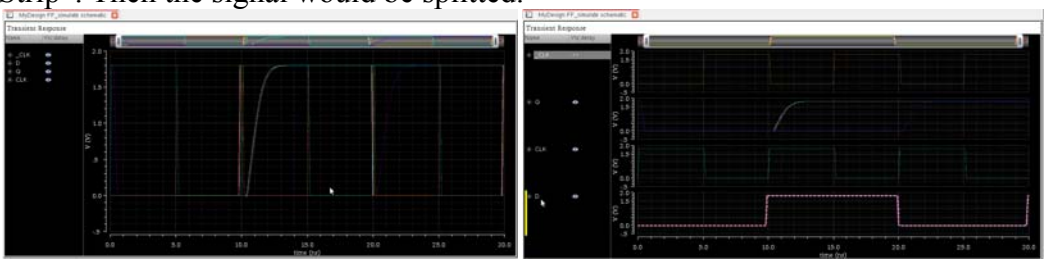
- Setup Analog Design Environment window as before to run transient simulation. Just run simulation, and "**delay**" will be automatically added into "**Design Variables**" list as below.



- In the Analog Design Environment window, select "Tools > Parametric Analysis". Then, type "delay" in the "Variable Name" option. The Parametric Analysis window will look as below. You need to adjust sweep ranges (from & to) and simulation steps by yourself to control the input D timing to see how the timings of input D affects the output Q. Select "Analysis > Start" in Parametric Analysis window to run sweep simulations.



- Then you waveform would be similar as belows. In order to split these group signals, you need to click the signal you want to choose, then right click "Move to ->New Strip". Then the signal would be splitted.



- **Hold Time:** It is the time required for the input data signal to be valid after the transition on the clock edge. We will not be measuring the hold time in this lab.

Report Requirements:

1. Schematic, layout, and LVS report of your design of Flip-Flop
2. Report a plot sufficiently verifying the correctness of your design. (CLK, _CLK, falling & rising of D and Q).
3. Report the rising and falling **clock-to-Q** delays of the FF in table format with respect to output loads (10 points from 1fF to 100fF).
4. Report the input capacitance of input D with the plot from AC simulation.
5. Report the setup time for both the D rising and falling in a delay table format where in the **clock-to-Q** delay is measured for varying separations between the D input and the CLK rising edge. Please **clarify** how you determine the setup time of your design.