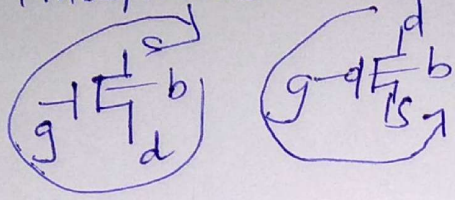
Circuit Simulation

Library file :- model.spi

Schematic description file :- cell18.spi

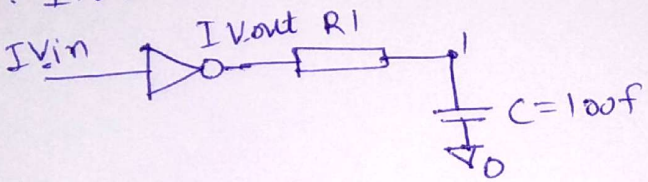
[Need to put INV/NAND2/XOR2 definition here]

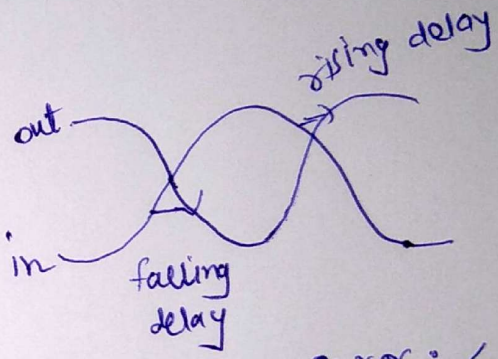
PMOS/NMOS – "Drain - Gate - Source - Body"



I) Simulate circuit

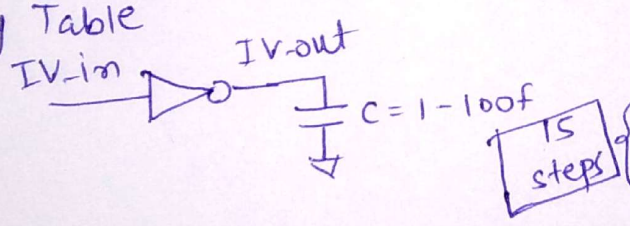
Ex: INV





II) Delay Table

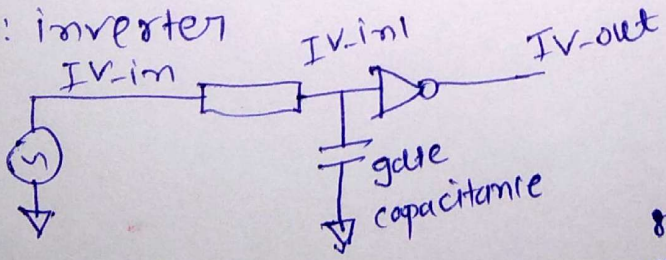
error : < 10%.

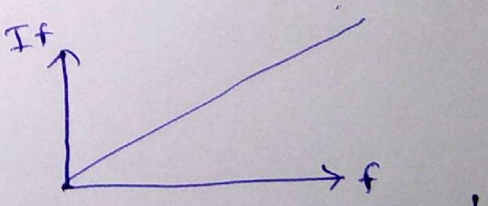


C	falling delay	Rising delay	err
⋮			
100			<10%

III) Gate capacitance (freqn domain)

Ex: inverter





8 points

f	If	C = If / 2πf