1. Introduction

In this lab you have to identify the critical path in your design (4 bit adder), and reduce the delay of this path by determining the optimal number of devices and sizes of the gates that lie along this path. You have to use the Logical Effort and Gate sizing techniques you learn in the course.

2. General Procedure

- The minimum delay of an N-stage path is

$$\mathbf{D = NF^{1/N} + P}$$

Where

D = delay of the path.
N = number of stages in the path.
F = Path Effort = **GBH**
P = Total parasitic delay for the path.

And,

F = GBH

G = Path Logical Effort. $= \prod g_i$

B = Path Branching Effort. $= \prod b_i = \prod \left(\frac{C_{on-path} + C_{off-path}}{C_{on-path}} \right)_i$

H = Path Electrical Effort. $= \frac{C_{out-path}}{C_{in-path}}$

- Identify the critical path in the circuit. Determine the path effort (**F**) for the path. Using F and the number of stages (**N**), we can obtain the required stage effort ($\hat{f} = F^{\frac{1}{N}}$). Note here, **N** is a fixed number because you do not change your design.

- For your calculations you may use an optimal value of stage effort to be **2.7 to 4**. Remember that this is a chicken and egg kind of problem. Although it is an optimization problem which in reality needs to be solved using iterative techniques, in this lab, we only use Lab5 as the starting point and perform only one optimization iteration. If your Lab 5 design produces a reasonable $\hat{f}$, you can resize the gates along the critical path with it. Otherwise, before the resizing along the critical path, you need to manipulate $\hat{f}$ which may involve gate resizing on or off the critical path.

  1. You can get the stage effort $\hat{f}$ from the un-optimized circuit, and if $2.7 \le \hat{f} \le 4$, use it to do gate-sizing for the transistors on the critical path.
  2. If your stage effort is not within the range, you can pick any value between 2.7 and 4

as your target. You may fix both the logical effort (**G**) and number of stages (**N**) and then manipulate your branching effort (**B**) to get to the target. Note that branches should be considered in the manipulation of **B**.

- Once you find both $\hat{f}$ and **N**, find the input capacitances of all the stages (i.e. each gate) beginning from the last stage in the path ($C_{in,i} = \frac{g_i C_{out,i}}{\hat{f}}$). This input capacitance should in turn be used to size the pmos and nmos transistors of the gate.

- Use the capacitance values you obtained from lab 3 to get an idea about sizing. Make sure you put **Capacitance values** in ***C***s in the formula above, **not** widths of transistors. You can estimate input capacitance of transistors by scaling with the ratio between capacitance and width of transistor you acquired at lab 3. For example, if a transistor of 400nm width shows 1fF of gate capacitance, you can assume that a transistor of 800nm width will have 2fF of gate capacitance.

- Considering the mobility ratio, the logical effort of your gates may differ from the lecture notes since your Wp/Wn in Lab 5 may be a value different from the lecture notes. **Make C_{out} = 30fF**.

3. **Procedure in detail**

(1) Draw transistor level schematic for 4bit adder

(2) Calculate best stage effort

- Decide number of stages, and mark critical path on your schematic
- Calculate G= $\prod g_i$

  $g_{xor} = \frac{C_{in}}{C_{in}of\ equivalent\ inverter} = \frac{2Wp+2Wn}{Wp/2+Wn/2} = 4$

  $g_{nand2} = \frac{C_{in}}{C_{in}of\ equivalent\ inverter}$

- Calculate H= $\frac{C_{out-path}}{C_{in-path}} = \frac{30fF}{C_{in}of\ XOR}$

  We assume that the relationship between **input transistor sizes and gate capacitance are linear.**

  According to lab3, you may find input transistor sizes you used to do spectre simulation, and gate capacitance you got for XOR/NAND gate. Then you could get related **capacitance per micron**. Using these values, you could get capacitance value of NAND/XOR in your schematic design as well as the equivalent inverters. Remember there are 4 input transistors for XOR gate.
- Calculate B= $\prod b_i = \prod \frac{C_{on-path}+C_{off-path}}{C_{on-path}}$

  For example, at the beginning of critical path, b= $\frac{C_{xor}+C_{nand}}{C_{nand}}$
- Best stage effort $\hat{f} = F^{\frac{1}{N}}$ while F=GBH

  If $2.7 \le \hat{f} \le 4$, that is fine; if not, you could consider to resize gates in noncritical paths

in order to change B and make $\hat{f}$ fall in such range.

(3) Resize transistors from last stage to first stage in the critical path

Always use $C_{in,i} = \frac{g_i C_{out,i}}{\hat{f}}$ to resize

Three things you need to pay attention:

i) When you get new Cin, get new transistor size through $\frac{C_{in}}{\text{Cap per micron}}$ and get pmos/nmos sizes by keeping the size ratio.

ii) Since sizing down the gates in your design may cause troubles like insufficient current or bias between rising and falling delays, for simplicity, if new sizes are smaller than old ones, keep the old ones. That is to say after resizing, new sizes should always be greater than or equal to old sizes.

iii) To compute $\mathbf{b_i}$ for each stage, if there is no branches, $C_{out} = C_{in}$ of the next stage and hence $\mathbf{b_i} = 1$. Otherwise branches should be considered.

4. Simulations and Comparison

- Create or modify your earlier schematic to reflect the changes from the logical effort calculation. You may also choose to write a spice netlist instead of a schematic view as in lab 3. There is no layout drawing in this lab!

- Simulate your new circuit and measure the delay the same way you did in lab 4 and lab 5. Compare this value to the number obtained from lab 5. Also report if there is any increase in area. Get a rough idea about the area using the sizes of the transistors (sum of the transistors' W times L)

5. Report Requirements

1. Print out the schematic of your circuit and **draw a line along the critical path**. Include your calculations to determine the number of stages in the circuit, the path effort, and the transistor sizes. You need to **clearly show your calculation steps**. If you wrote a spice netlist, include a drawing of the critical path.

2. Turn in the waveforms for **the same input vectors given in the lab 5**. Make a **table comparing** the **delays** and the **VDD Power consumption** of **both** the **non-optimized** and the **optimized** circuits for all cases (you need to calculate improvement). Please switch all inputs at the same time as you did in the lab 5.

3. Make a **table comparing** the **Area** (sum of all the transistors' W*L).