2020

Application Note

DODO

BK4819(V3)

Table of contents

MCU Interface - 3 Wire SPI

Parameter	Symbol	Min.	Type.	Max.
SCK Frequency	fSCK	0 MHz —		8 MHz
SCK High Time	tHIGH	25 ns —		–
SCK Low Time	tLOW	25 ns —		–
SDATA Input, SCN to SCK ÿ Setup	tS	20 ns —		–
SDATA Input to SCK ÿ Hold	tHSDATA	10 ns —		–
SCN Input to SCK ÿ Hold	tHSCN	10 ns —		–
SCK to SDATA Output Valid	tCDV	2 ns —		25 ns
SCK ÿÿto next SCK ÿ after Address In	tNXT	1 us —		–
SCK, SCN, SDATA, Rise/Fall Time	tR,tF	–	–	10 ns

SCK

SCN

SDATA

tS   tR   tF   tS tHSDIO   tHIGH tLOW   tHSENB

R/W   A6-1   A0   D15   D14-1   D0

3-wire Control Interface
Write Timing Diagram   **Address In**   **Data In**

SCK

SCN

SDATA

tNXT

tS   tCDV   tHSENB

R/W   A6-1   A0   D15   D14-1   D0

3-wire Control Interface
Read Timing Diagram   **Address In**   **Bus Turnaround**   **Data Out**
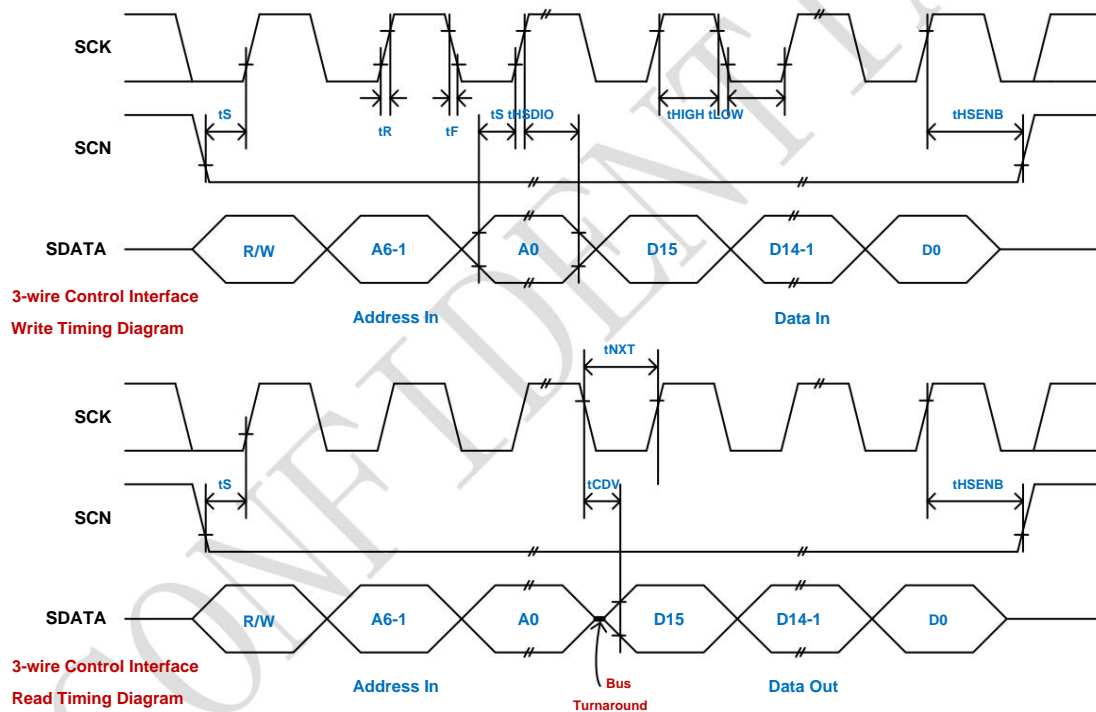
Reigster Initialization

Perform SoftReset, internal PowerUp and other initialization settings after the chip is powered on. Use RF_Initial(), in RF_Initail()

Set squelch threshold, receive volume, receive AGC, MIC sensitivity, VoX threshold, modulation depth, transmit

power, sub-audio, etc.

Tx/Rx Audio

1. After initialization, the default state is the normal Speech mode, which can send and receive voice (300~3kHz).

2. To enable companding, you need to set RF_EnterCompander(), and to disable companding, use RF_ExitCompander()

Register	Default	Description
REG_31<3>	0	Enable Compander Function. 1= Enable; 0=Disable
REG_28<15:14> 0b01		Expander (AF Rx) Ratio. 00=Disable; 01=1:2; 10=1:3; 11=1:4 Expander
REG_28<13:7>	0x56	(AF Rx) 0 dB point(dB)
REG_28<6:0>	0x38	Expander (AF Rx) noise point(dB)
REG_29<15:14> 0b10		Compress (AF Tx) Ratio. 00=Disable; 01=1.333:1; 10=2:1; 11=4:1 Compress
REG_29<13:7>	0x56	(AF Tx) 0 dBpoint(dB)
REG_29<6:0>	0x40	Compress (AF Tx) noise point(dB)
REG_6F<6:0>		Read Only AF Tx/Rx Input Amplitude(dB)

3. You need to set RF_EnterScramble() to enable scrambling, and use RF_ExitScramble() to disable scrambling

Register	Default	Description
REG_31<1>	0	Enable Scramble Function. 1=Enable; 0=Disable
REG_71<15:0>	0x8517	Scramble/Tone1FrequencyControlWord. =3300(Hz)*10.32444 for XTAL 13M/26M or =3300(Hz)* for 12.8M/19.2M/25.6M/38.4M. 10.48576 XTAL - The scrambler inversion mixing frequency should be kept between 2.6kHz and 3.5kHz

4. Filter switch enable

Register	Default	Description
REG_2B<10>	0	Disable AFRxHPF300filter. 0=Enable; 1=Disable
REG_2B<9>	0	Disable AF RxLPF3K filter. 0=Enable; 1=Disable
REG_2B<8>	0	Disable AF Rx de-emphasisfilter. 0=Enable; 1=Disable
REG_2B<2>	0	Disable AFTxHPF300filter.

Register	Default	Description
		0=Enable; 1=Disable
REG_2B<1>	0	Disable AFTxLPF1filter. 0=Enable; 1=Disable
REG_2B<0>	0	Disable AFTxpre-emphasisfilter. 0=Enable; 1=Disable
REG_43<8:6>	0b001	AFTxLPF2 filter Band Width(Apass=1dB) Selection. 100 = 4.5 kHz 101 = 4.25 kHz 110 =4kHz 111 = 3.75 kHz 000 = 3 kHz (for 25k Channel Space) 001 = 2.5 kHz (for 12.5k Channel Space) 010 = 2.75 kHz 011 =3.5 kHz

5. Audio response adjustment uses RF_SetAfResponse(u8 tx, u8 f3k, u8 db), where the parameter tx=1 transmits/tx=0 receives,

f3k=1 adjusts 3kHz/f3k=0 adjusts 300Hz, db=adjustment range -1~+4dB. For example:

Transmit 300Hz increase 2dB: RF_SetAfResponse(1,0,2);

Receive 3kHz decrease 3dB: RF_SetAfResponse(0,1,-3);

6. Receive volume setting

Register	Default	Description
REG_48<11:10> 0b00		OF Rx Gain1. 00=0dB;01=-6dB;10=-12dB;11=-18dB
REG_48<9:4>	0x3C	OF Rx Gain2. -26dB~5.5dB, 0.5dB/step. 0x00=mute
REG_48<3:0>	0b1111	AF DAC Gain (after Gain1 and Gain2). 1111=max; 0000=min; about 2dB/step

7. Transmit modulation setting and transmit mute

Register	Default	Description
REG_40<12>	1	Enable RF TxDeviation. 1=Enable; 0=Disable
REG_40<11:0>	0x4D0	RF Tx Deviation Tuning (Apply for both in-band signal and sub-audio signal). 0=min; 0xFFF=max Enable AF Tx Mute (for
REG_50<15>	0	DTMF Tx or other applications). 1=Mute; 0=Normal

8. MIC sensitivity setting

Register	Default	Description
REG_7D<4:0>	0x10	MIC Sensitivity Tuning. 0x00=min; 0x1F=max; 0.5dB/step

9. Use RF_SetAf(u8 mode) for AF output to generate local key tone and prompt tone, please refer to RF_Key() to generate bell

  Tone and launch can refer to RF_Call()

Register	Default	Description
REG_47<13>	1	AF Output Inverse Mode. 1=Inverse
REG_47<11:8>	0x1	AFOutputSelection. 0x0=Mute; 0x1=Normal AF Out; 0x2=Tone Out for Rx (Should enable Tone1 first); 0x3=Beep Out for Tx (Should enable Tone1 first and set REG_03[9]=1 to enable AF; 0x6=CTCSS/CDCSS Out for Rx Test; 0x8=FSK Out for Rx Test; Others=Reserved;

CTCSS/CDCSS

1. To enable CTCSS, you need to set RF_SetCtcss() and RF_SetCtc2(), the latter is only used for receiving frequency 55Hz (or

  Other frequencies within 100Hz) CTCSS tail tone; the former is used to receive and transmit normal CTCSS.

2. To enable CDCSS, you need to set RF_SetCdcss(), and you need to set 134.4Hz code rate and CDCSS code.

3. Close the sub-audio using RF_ExitSubau()

4. Use RF_GenTail() to generate tail at the end of transmission, and use parameters CTC120/CTC180/CTC240 for phase tail, such as

  RF_GenTail(CTC180); change frequency tail tone (such as 55Hz) using parameter CTC55, such as RF_GenTail(CTC55); in CDCSS

  In this mode, 134.4Hz tail tone is generated using parameter CTC134, such as RF_GenTail(CTC134)

5. Use RF_GetCtcss() to read the CTCSS status, return 1 means received CTC1 (main CTC), return 2 means received

  CTC2 (such as 55Hz tail tone); use RF_GetCdcss() to read CDCSS status, return 1 to indicate positive CDC code received,

  Return 2 means receive CDC inverse code; use RF_GetTail() to read phase tail status, return 1 means receive 120°

  Phase change tail, return 2 means receive 180° phase change tail, return 3 means receive 240° phase change

  end sound.

Register	Default	Description
REG_51<15>	0	1=Enable TxCTCSS/CDCSS; 0=Disable
REG_51<14>	0	1= GPIO6(PIN2)Input for CDCSS; 0=Normal Mode.(for BK4819v3)
REG_51<13>	0	1=Transmit negative CDCSS code 0=Transmit positive CDCSScode
REG_51<12>	0	CTCSS/CDCSS mode selection. 1=CTCSS, 0=CDCSS
REG_51<11>	0	CDCSS 24/23bit selection. 1=24bit, 0=23bit
REG_51<10>	0	1050HzDetectionMode. 1=1050/4 Detect Enable, CTC1 should be set to 1050/4 Hz
REG_51<9>	0	Auto CDCSS Bw Mode. 1=Disable; 0=Enable.
REG_51<8>	0	Auto CTCSS Bw Mode. 0=Enable; 1=Disable
REG_51<6:0>	0	CTCSS/CDCSS Tx Gain1 Tuning. 0=min; 0x7F=max
REG_2E<9:8>	0x10	CTCSS/CDCSS Tx Gain2 Tuning (after Gain1). 00=12dB; 01=6dB; 10=0dB; 11=-6dB
REG_07<15:0>		When <15:13>=0 for CTC1 <12:0>=CTC1 frequencycontrolword = freq(Hz)*20.64888 for XTAL 13M/26M or =freq(Hz)*20.97152 for XTAL 12.8M/19.2M/25.6M/38.4M When<15:13>=1 for CTC2(Tail 55Hz Rx detection) <12:0>=CTC2(should below 100Hz)frequencycontrolword = 25391/freq(Hz) for XTAL 13M/26M or = 25000/ freq(Hz)for XTAL 12.8M/19.2M/25.6M/38.4M When <15:13>=2 for CDCSS 134.4Hz <12:0>=CDCSS baud rate frequency(134.4Hz) controlword = freq(Hz)*20.64888 for XTAL 13M/26M or =freq(Hz)*20.97152 for XTAL 12.8M/19.2M/25.6M/38.4M
REG_08<15:0>		<15>=1 for CDCSS high 12bit <15>=0 for CDCSS low 12bit <11:0>=CDCSShigh/low 12bit code
REG_52<15>	0	Enable 120/180/240 degree shift CTCSS or 134.4Hz Tail when CDCSS mode. 0=Normal, 1=Enable
REG_52<14:13> 0b00		CTCSS tail modeselection (only valid when REG_52<15>=1).

		00= for 134.4Hz CTCSS Tail when CDCSS mode. 01=CTCSS0 120° phase shift, 10= CTCSS0 180° phase shift 11= CTCSS0 240° phase shift
REG_52<12>	0	CTCSSDetectionThreshold Mode, 1=~0.1%; 0=0.1 Hz
REG_52<11:6>	0x0A	CTCSS found detect threshold.
REG_52<5:0>	0x0F	CTCSS lost detect threshold.
REG_0C<15:14> Read Only		<14>:CDCSS positive code received <15>:CDCSS negative code received
REG_0C<13:12> Read Only		CTCSS Phase Shift Received. 00=No phase shift 01=CTCSS0 120° phase shift, 10= CTCSS0 180° phase shift 11= CTCSS0 240° phase shift
REG_0C<10:11> Read Only		<11>:CTC2(55Hz) received <10>:CTC1 received

SELCALL

1. Turn on the SELCALL(5Tone) mode and use RF_Enter5tone(), this function is only for the receiving frequency coefficient, receiving threshold,

   The transmission path has been set so that it will not affect normal audio listening.

2. Exit SELCALL(5Tone) mode using RF_Exit5tone()

3. Use RF_5toneTransmit() to transmit SELCALL (5Tone), and use MCU timing to replace the transmission according to the transmission code Frequency of SELCALL (5Tone) (Tone1).

4. Use RF_5toneReceive() to receive SELCALL (5Tone), return 1 for failure, return 0 for success

DTMF

1. Open the DTMF mode and use RF_EnterDtmf(), this function is only for DTMF receiving frequency coefficient, receiving threshold, sending

   The firing path is set and will not affect normal audio listening.

2. Exit DTMF mode using RF_ExitDtmf()

3. Transmit DTMF Use RF_DtmfTransmit(), use MCU timing to change the frequency of transmitting DTMF according to the transmission code

ÿTone1+Tone2ÿÿ

4. Use RF_DtmfReceive() to receive DTMF, return 1 for failure, return 0 for success

Register	Default	Description
REG_70<15>	0	Enable TONE1 1=Enable; 0=Disable.
REG_70<14:8>	0	TONE1tuninggain
REG_70<7>	0	Enable TONE2 1=Enable; 0=Disable.
REG_70<6:0>	0	TONE2/FSK tuninggain TONE1/
REG_71<15:0>	0x8517	Scramblefrequencycontrolword. =freq(Hz)*10.32444 for XTAL 13M/26M or =freq(Hz)* 10.48576 for XTAL 12.8M/ 19.2M/25.6M/38.4M.
REG_72<15:0>	0x2854	TONE2/FSK frequencycontrolword =freq(Hz)*10.32444 for XTAL 13M/26M or =freq(Hz)* 10.48576 for XTAL 12.8M/19.2M/25.6M/38.4M.
REG_50<15>	0	Enable AF Tx Mute (for DTMF Tx or other applications). 1=Mute; 0=Normal
REG_0B<11:8>		Read Only DTMF/5Tone Code Received.

FSK

1. Turn on FSK mode and use RF_EnterFsk(), which will not affect normal audio listening, and can enter at the same time

DTMF/SELCALL mode for reception. The FSK rate register is multiplexed with the Tone2 register. Use 2400bps mode

Need to open the macro definition FSK2400

2. Exit using RF_ExitFsk()

3. Use RF_FskTransmit() to transmit FSK, return 1 for failure, return 0 for success

4. FSK frame format (CRC is optional), if you want to be compatible with BK4815/BK4818, you need to complete it in the Data part

Addr/Type/Size/CRCA/Payload/CRCB data framing in BK4815/BK4818FSK frame structure, and turn off

For the CRC part of the BK4819 FSK frame structure, set the same Preamble and SyncWord.

Preamble	Sync Word	Data	CRC(opt)
1~16 bytes	2 or 4 bytes	Config (maximum 1024 words)	2 bytes
		1 word = 2 bytes	

5. Use RF_FskReceive() to receive FSK, return 1 for failure, return 0 for success

Register	Default	Description
REG_58<15:13>	000	FSK Tx Mode Selection. 000 for FSK1.2K and FSK2.4K Tx; 001 for FFSK1200/1800 Tx; 011 for FFSK1200/2400 Tx; 101 for NOAA SAME Tx
REG_58<12:10>	000	FSK Rx Mode Selection. 000 for FSK1.2K, FSK2.4K Rx and NOAA SAME Rx; 111 for FFSK1200/1800 Rx; 100 for FFSK1200/2400 Rx;
REG_58<9:8>	00	FSK Rx Gain.
REG_58<5:4>	00	FSK Preamble Type Selection. 11=0xAA; 10=0x55; 00=0xAA or 0x55 due to the MSB of FSK Sync Byte 0.
REG_58<3:1>	000	FSK Rx BandWidth Setting. 100 for FSK 2.4K and FFSK1200/2400; 000 for FSK 1.2K; 001 for FFSK1200/1800; 010 for NOAA SAME Rx
REG_58<0>	0	FSK Enable. 1=Enable; 0=Disable.
REG_59<15>	0	Clear TX FIFO, 1=clear
REG_59<14>	0	Clear RX FIFO, 1=clear
REG_59<13>	0	1=Enable FSK Scramble
REG_59<12>	0	1=Enable FSK RX
REG_59<11>	0	1=Enable FSK TX
REG_59<10>	0	1=Invert FSK data when RX
REG_59<9>	0	1=Invert FSK data when TX
REG_59<7:4>	0	FSK Preamble Length Selection 0=1 byte; 1=2 bytes; 2=3 bytes; …; 15=16 bytes.
REG_59<3>	0	FSK SyncLength Selection. 1=4 bytes (FSK Sync Byte 0,1,2,3) 0=2 bytes (FSK Sync Byte 0,1)
REG_5A<15:8>	0x85	FSK Sync Byte 0 (Sync Byte 0 first, then 1,2,3)
REG_5A<7:0>	0xCF	FSK Sync Byte 1

REG_5B<15:8>	0xAB	FSK Sync Byte 2
REG_5B<7:0>	0x45	FSK Sync Byte 3
REG_5C<6>	1	CRC Option Enable. 1=Enable; 0=Disable.
REG_5D<15:8>	0x0F	FSK Data Length(Byte) **Low 8bits(Total 11 bits for BK4819v3).** **For example, 0xF means 16 bytes length.**
REG_5D<7:5>	**0**	**FSK Data Length(Byte)** **High 3bits(Total 11 bits for BK4819v3).**
REG_5E<9:3>	64	FSK Tx FIFO (Total 128 Words) Almost Empty Threshold.
REG_5E<2:0>	4	FSK Rx FIFO (Total 8 Words) Almost Full Threshold.
REG_5F<15:0>	x	FSK Word Input/Output.
REG_70<6:0>	0	TONE2/FSK tuninggain
REG_72<15:0>	0x2854	TONE2/FSK frequencycontrolword =freq(Hz)*10.32444 for XTAL 13M/26M or =freq(Hz)* 10.48576 for XTAL 12.8M/19.2M/25.6M/38.4M.
REG_0B<7>	Read Only	FSK Rx SyncN Fround.
REG_0B<6>	Read Only	FSK Rx SyncP Fround.
REG_0B<4>	Read Only	FSK Rx CRC Indicator. 1=CRC Pass; 0=CRC Fail.

MDC1200

1. Turn on the MDC mode and use RF_EnterMdc(), which will not affect normal audio listening and can be entered at the same time DTMF/SELCALL mode for reception. The MDC rate register is multiplexed with the Tone2 register. The default mode is 1200/1800, if you want to use 1200/2400 mode, you need to open the macro definition MDC2400

2. Exit using RF_ExitMdc()

3. Use RF_MdcTransmit() to transmit MDC, return 1 for failure, return 0 for success

4. Use RF_MdcReceive() to receive MDC, return 1 for failure, return 0 for success

5. Can support HDC1200 mode

NOAA SAME

1. Use RF_EnterNoaa () to receive the NOAASAME code, which will not affect normal audio listening and can be entered at the same time

    NOAA mode for reception. NOAA rate register is multiplexed with Tone2 register

2. Exit using RF_ExitNoaa()

3. Use RF_NoaaReceive() to receive FSK, return 1 for failure, return 0 for success, and the MCU will negotiate according to the received code

    Discussion

VoX

1. Open VoX using RF_EnterVox(); close using RF_ExitVox()

2. Use RF_GetVox() to get the VoX status, return 1 if the MIC voice is received, and return 0 if the voice is not received.

3. Use RF_GetVoxAmp() to obtain the VoX amplitude, and the return value is the voice amplitude of the MIC, which can be used by the MCU to judge VoX by itself.

    use.

Register	Default	Description
REG_31<2>	0	Enable VOX detection. 1=Enable; 0=Disable
REG_7A<15:12> 8		VoX=0 Detection delay, *128ms
REG_46<10:0> 0x50		Voice AmplitudeThreshold for VOX=1 detect
REG_79<15:11> 8		VoX Detection Interval Time.
REG_79<10:0> 0x40		Voice Amplitude Threshold for VOX=0 detect Voice
REG_64<15:0> Read Only		AmplitudeOut.
REG_0C<2>	Read Only	VoX Indicator 0: No 1: Yes

Power Saving

1. Use RF_Slee() to go to sleep, use RF_WakeUp() to wake up, or directly enter RF_Txon() to transmit

    Or receive RF_Rxon()

2. Current 200uA in sleep state? (to be improved); IDLE current 3mA after wake-up?

Register	Default	Description
REG_37<14:12> 0b001		DSP Voltage Setting.
REG_37<11>	1	ANA LDO Selection. 1=2.7v, 0=2.4v
REG_37<10>	1	VCO LDO Selection. 1=2.7v, 0=2.4v
REG_37<9>	1	RF LDO Selection. 1=2.7v, 0=2.4v
REG_37<8>	1	PLL LDO Selection. 1=2.7v, 0=2.4v
REG_37<7>	0	ANA LDO Bypass. 1=Bypass, 0=Enable.
REG_37<6>	0	VCO LDO Bypass. 1=Bypass, 0=Enable.
REG_37<5>	0	RF LDO Bypass. 1=Bypass, 0=Enable.
REG_37<4>	0	PLL LDO Bypass. 1=Bypass, 0=Enable.
REG_37<3>	0	Reserved.
REG_37<2>	0	DSP Enable. 1=Enable, 0=Disable.
REG_37<1>	0	XTAL Enable. 1=Enable, 0=Disable.
REG_37<0>	0	Band-Gap Enable. 1=Enable, 0=Disable.

Tx/Rx Mode Switch

1. Use RF_Txon() to transmit

2. Use RF_Rxon() to receive 3.

Use RF_Txon_Beep() when transmitting with side tone (such as sending a ring tone)

Register	Default	Description
REG_30<15>	0	VCO Calibration Enable. 1=Enable, 0=Disable Rx
REG_30<13:10> 0		Link Enable (include LNA/MIXER/PGA/ADC). 1111=Enable, 0000=Disable
REG_30<9>	0	AF DAC Enable. 1=Enable, 0=Disable.
REG_30<7:4>	0	PLL/VCO Enable.

		1111=Enable, 0000=Disable
REG_30<3>	0	PA Gain Enable. 1=Enable, 0=Disable
REG_30<2>	0	MIC ADC Enable. 1=Enable, 0=Disable
REG_30<1>	0	Tx DSP Enable. 1=Enable, 0=Disable
REG_30<0>	0	Rx DSP Enable. 1=Enable, 0=Disable

Squelchuelch,RSSI,Ex-Noise, Gltich

The corresponding parameters can be obtained through RF_GetRssi(), RF_GetNoise(), RF_GetGlitch(), which is convenient for setting the squelch level

Register	Default	Description
REG_78<15:8>	0x48	RSSI threshold for Squelch=1, 0.5dB/step RSSI
REG_78<7:0>	0x46	threshold for Squelch =0, 0.5dB/step Ex-noise
REG_4F<14:8>	0x2F	threshold for Squelch =0 Ex-noise threshold
REG_4F<6:0>	0x2E	for Squelch =1 Glitch threshold for Squelch
REG_4D<7:0>	0x20	=0 Glitch threshold for Squelch =1
REG_4E<7:0>	0x08	Squelch=1 Delay Setting.
REG_4E<13:11>	0b101	
REG_4E<10:9>	0b111	Squelch=0 Delay Setting.
REG_67<8:0>	Read Only 0.5dB/step, RSSI (dBm) ~= REG_67<8:0>/2 – 160.	
REG_65<6:0>	Read Only Ex-noiseindicator, dB/step.	
REG_63<7:0>	Read Only Glitch indicator.	
REG_0C<1>	Read Only Squelch resultoutput. 1=Link; 0=Loss	

AFC, ALC, MIC AGC

MIC PGA gain automatic control can expand the dynamic range of MIC signal, so that larger amplitude MIC signal can be transmitted without distortion. used in

In the DMR scheme, this function should be turned off (REG_19<15>=1), and the ALC function should also be turned off (REG_4B<5>=1).

Register	Default	Description
REG_73<13:11>	0b000	Automatic Frequency Correction(AFC) Range Selection. 000=max; 111=min
REG_73<4>	0	Automatic Frequency Correction(AFC) Disable. 1=Disable; 0=Enable.

REG_19<15>	1	Automatic MIC PGA Gain Controller(MIC AGC) Disable. 1=Disable; 0=Enable.
REG_4B<5>	0	AF Level Controller(ALC) Disable. 1=Disable; 0=Enable.

Frequency Setting

Use RF_SetFreq(u16 freq_hi16, u16 freq_lo16) to set the frequency, pay attention to the conversion formula:

Frequency(Hz)= (freq_hi16<<16 + freq_lo16)*10

Register	Default	Description
REG_38<15:0>	0x3A98	Frequency(Hz)= (freq_hi16<<16 + freq_lo16)*10
REG_39<15:0>	0x0271	

If the frequency point of 409.75MHz is set, RF_SetFreq((40975000>>16)&0xFFFF, 40975000&0xFFFF)

Tx Output Power

Register	Default	Description
REG_36<15:8>	0	PA Biasoutput 0~3.2V 0x00=0V ... 0xFF=3.2V
REG_36<7>	0	1=Enable PACTLoutput; 0=Disable(Output 0 V)
REG_36<5:3>	0b111	PA Gain1 Tuning. 111(max)->000(min)
REG_36<2:0>	0b111	PA Gain2 Tuning. 111(max)->000(min)

Power Output Table (Approximate)

Power(dBm)	PA Gain1							
PA Gain2	111	110	101	100	011	010	001	000
111	7.26	7.01	6.67	6.17	5.39	4.10	1.52	-5.02
110	6.38	6.08	5.67	6.06	4.12	2.53	-0.72	-9.45
101	5.65	5.30	4.82	4.13	3.03	1.18	-2.58	-13.4
100	5.01	4.62	4.08	3.30	2.08	0.01	-4.16	-16.9
011	4.19	3.73	3.11	2.21	0.84	-1.48	-6.11	-20.5
010	2.60	2.04	1.24	0.13	-1.56	-4.25	-9.50	-22.9
001	1.04	0.35	-0.63	-1.98	-3.90	-6.80	-12.3	-23.7

| 000 | -0.70 | -1.51 | -2.65 | -4.16 | -6.20 | -9.35 | -14.9 | -24.3 |

Interrupt

The interrupt signal can be sent by any GPIO (see GPIO setting function), or poll the REG_0C<0> bit, active high, default Low.

The interrupt can be output by any GPIO port of the chip, and the interrupt can be cleared by writing any value to the REG_02 register, such as

RF_Write (0x02,0x0000); //clear interrupt

The interrupt high level (or the interrupt register REG_0C<0> is 1) is valid, when the interrupt is received, the interrupt must be cleared before reading

Fetch the interrupt vector table.

Register	Default	Description
REG_0C<0>	Read Only	Interrupt Indicator. 1=Interrupt Request; 0=No Request.
REG_3F<15>	0	FSK Tx Finished Interrupt Enable. 1=Enable; 0=Disable.
REG_3F<14>	0	FSK FIFO Almost Empty Interrupt Enable. 1=Enable; 0=Disable.
REG_3F<13>	0	FSK Rx Finished Interrupt Enable. 1=Enable; 0=Disable.
REG_3F<12>	0	FSK FIFO Almost FullInterrupt Enable. 1=Enable; 0=Disable.
REG_3F<11>	0	DTMF/5TONE Found Interrupt Enable. 1=Enable; 0=Disable.
REG_3F<10>	0	CTCSS/CDCSSTail Found InterruptEnable. 1=Enable; 0=Disable.
REG_3F<9>	0	CDCSS Found InterruptEnable. 1=Enable; 0=Disable.
REG_3F<8>	0	CDCSS Lost InterruptEnable. 1=Enable; 0=Disable.
REG_3F<7>	0	CTCSS Found InterruptEnable. 1=Enable; 0=Disable.
REG_3F<6>	0	CTCSS Lost InterruptEnable. 1=Enable; 0=Disable.
REG_3F<5>	0	VoX Found InterruptEnable. 1=Enable; 0=Disable.
REG_3F<4>	0	VoX Lost InterruptEnable. 1=Enable; 0=Disable.

REG_3F<3>	0	Squelch Found InterruptEnable. 1=Enable; 0=Disable.
REG_3F<2>	0	Squelch Lost InterruptEnable. 1=Enable; 0=Disable.
REG_3F<1>	0	FSK Rx Sync Interrupt Enable. 1=Enable; 0=Disable.
REG_02<15>	Read Only	FSK Tx Finished Interrupt.
REG_02<14>	Read Only	FSK FIFO Almost Empty Interrupt Enable.
REG_02<13>	Read Only	FSK Rx Finished Interrupt Enable.
REG_02<12>	Read Only	FSK FIFO Almost FullInterrupt.
REG_02<11>	Read Only	DTMF/5TONE Found Interrupt.
REG_02<10>	Read Only	CTCSS/CDCSSTail Found Interrupt.
REG_02<9>	Read Only	CDCSS Found Interrupt.
REG_02<8>	Read Only	CDCSS Lost Interrupt.
REG_02<7>	Read Only	CTCSS Found Interrupt.
REG_02<6>	Read Only	CTCSS Lost Interrupt.
REG_02<5>	Read Only	VoX Found Interrupt.
REG_02<4>	Read Only	VoX Lost Interrupt.
REG_02<3>	Read Only	Squelch Found Interrupt.
REG_02<2>	Read Only	Squelch Lost Interrupt.
REG_02<1>	Read Only	FSK Rx Sync Interrupt.

GPIO

1. Use RF_SetGpioOut(u8 num, u8 type, u8 val) according to the corresponding PIN and output mode, where num is

GPIO serial number, type is the output mode, val is the output value in GPIO output mode. The output mode is detailed in the reference code

drive.c

2. Use RF_GetGpioIn(u8 num) to get the GPIO input value, where num is the GPIO serial number.

Register	Default	Description
REG_0A<6>	Read Only	GPIO0 (PIN28) Input Indicator. 1=High; 0=Low.
REG_0A<5>	Read Only	GPIO1(PIN29) Input Indicator. 1=High; 0=Low.
REG_0A<4>	Read Only	GPIO2 (PIN30) Input Indicator. 1=High; 0=Low.
REG_0A<3>	Read Only	GPIO3 (PIN31) Input Indicator. 1=High; 0=Low.
REG_0A<2>	Read Only	GPIO4 (PIN32) Input Indicator.

		1=High; 0=Low.
REG_0A<1>	Read Only	GPIO5 (PIN1) Input Indicator. 1=High; 0=Low.
REG_0A<0>	Read Only	GPIO6(PIN2) Input Indicator. 1=High; 0=Low.
REG_33<14>	1	GPIO0(PIN28) Output Disable. 1=Output Disable; 0=Output Enable.
REG_33<13>	1	GPIO1(PIN29) Output Disable. 1=Output Disable; 0=Output Enable.
REG_33<12>	1	GPIO2(PIN30) Output Disable. 1=Output Disable; 0=Output Enable.
REG_33<11>	1	GPIO3(PIN31) Output Disable. 1=Output Disable; 0=Output Enable.
REG_33<10>	1	GPIO4(PIN32) Output Disable. 1=Output Disable; 0=Output Enable.
REG_33<9>	1	GPIO5(PIN1) Output Disable. 1=Output Disable; 0=Output Enable.
REG_33<8>	1	GPIO6(PIN2) Output Disable. 1=Output Disable; 0=Output Enable.
REG_33<6>	0	GPIO0(PIN28) Output Value. 1= High when Output Enable; 0=Low when Output Enable.
REG_33<5>	0	GPIO1(PIN29) Output Value. 1= High when Output Enable; 0=Low when Output Enable.
REG_33<4>	0	GPIO2(PIN30) Output Value. 1= High when Output Enable; 0=Low when Output Enable.
REG_33<3>	0	GPIO3(PIN31) Output Value. 1= High when Output Enable; 0=Low when Output Enable.
REG_33<2>	0	GPIO4(PIN32) Output Value. 1= High when Output Enable; 0=Low when Output Enable.
REG_33<1>	0	GPIO5(PIN1) Output Value. 1= High when Output Enable; 0=Low when Output Enable.
REG_33<0>	0	GPIO6(PIN2) Output Value. 1= High when Output Enable; 0=Low when Output Enable.
REG_34<15:12> 0x0		GPIO3(PIN31) Output Type Selection. The Definitions is the same as REG_34<3:0>.
REG_34<11:8>	0x0	GPIO4(PIN32) Output Type Selection. The Definitions is the same as REG_34<3:0>.
REG_34<7:4>	0x0	GPIO5(PIN1) Output Type Selection. The Definitions is the same as REG_34<3:0>.
REG_34<3:0>	0x0	GPIO6(PIN2)Output Type Selection. 0=High/Low 1=Interrupt

		2=Squelch
		3=VoX
		4=CTCSS/CDCSS Compared Result
		5=CTCSS Compared Result
		6=CDCSS Compared Result
		7=Tail Detected Result
		8=DTMF/5Tone Symbol Received Flag
		9=CTCSS/CDCSS Digital Wave
		Others=Reserved
REG_35<11:8>	0x0	GPIO0(PIN28)Output Type Selection. The Definitions is the same as REG_34<3:0>.
REG_35<7:4>	0x0	GPIO1(PIN29) Output Type Selection. The Definitions is the same as REG_34<3:0>.
REG_35<3:0>	0x0	GPIO2(PIN30) Output Type Selection. The Definitions is the same as REG_34<3:0>.

XTAL

1. The chip supports 26M, 25.6M, 13M, 12.8M, 19.2M and 38.4M crystals or temperature compensation. The default is 26M, if

Use other frequency crystals other than 26M or use RF_SetXtal(u8 mode) for temperature compensation, such as RF_SetXtal(XTAL19M2)

Frequency Scan

1. Use RF_FreqScan() to obtain the RF frequency of the LNAIN pin (requires a larger amplitude>-40dBm) and return 1.

indicates failure, and returns 0 for success. The frequency is written to the global variables FRQ_HI16 and FRQ_LO16

2. After scanning the frequency, set the receiving frequency to this frequency point, and use RF_CtcDcsScan() to obtain the CTCSS frequency or CDCSS

code, return 0 for failure, return 1 for receiving CTCSS and write the frequency into the global variable CtC_FREQ, return 2

Indicates that 23bit CDCSS is received, return 3 indicates that 24bitCDCSS is received, 23 or 24bitCDCSS are both written into global variables

DCS_HI12 and DCS_LO12 ,

Register	Default	Description
REG_32<15:14> 0b00		FrequencyScan Time. 00=0.2 Sec; 01=0.4 Sec; 10=0.8 Sec; 11=1.6 Sec
REG_32<0>	0	FrequencyScanEnable. 1=Enable; 0=Disable.
REG_0D<15>	Read Only	Frequency Scan Indicator. 1=Busy; 0=Finished.
REG_0D<10:0>	Read Only	Frequency Scan High 16 bits.

REG_0E<15:0>	Read Only	Frequency Scan Low 16 bits. = REG_0D<10:0><<16 + REG_0E<15:0>, unit is 10Hz
REG_68<15>	Read Only	CTCSS Scan Indicator. 1=Busy; 0=Found.
REG_68<12:0>	Read Only	CTCSS Frequency. Frequency(Hz) = REG_68<12:0>/20.64888 for 13M/26M XTAL and = REG_68<12:0>/20.97152 for 12.8M/19.2M/25.6M/38.4M XTAL
REG_69<15>	Read Only	CDCSS Scan Indicator. 1=Busy; 0=Found.
REG_69<14>	Read Only	23 or 24 bit CDCSS Indicator.(for BK4819v3) 1=24 bit; 0=23 bit.
REG_69<11:0>	Read Only	CDCSS High 12 bits.
REG_6A<11:0>	Read Only	CDCSS Low 12 bits.

Channel Spacing

The chip supports multiple bandwidths, including common 12.5k/25k/6.25k/20k, use RF_SetChnSpace(u8 space), input

The parameter SPACE_12K5/SPACE_25K/SPACE_6K25/SPACE_20K is enough. The transmitting and receiving band can be set according to actual needs

Width.

Register	Default	Description
REG_43<14:12> 0b100		RF filter bandwidth (Apass=0.1dB) 000 = 1.7 kHz 001 = 2 kHz 010 = 2.5 kHz 011 = 3 kHz 100 = 3.75 kHz 101 = 4 kHz 110 = 4.25 kHz 111 = 4.5 kHz if REG_43<5>=1, RF filter bandwidth *=2; RF
REG_43<11:9>	0b000	filter bandwidth when signal is weak (Apass=0.1dB) 000 = 1.7 kHz 001 = 2 kHz 010 = 2.5 kHz 011 = 3 kHz 100 = 3.75 kHz 101 = 4 kHz

		110 = 4.25 kHz
		111 = 4.5 kHz
		if REG_43<5>=1, RF filter bandwidth *=2;
REG_43<8:6>	0b001	AFTxLPF2 filter Band Width (Apass=1dB) Selection.
		100 = 4.5 kHz
		101 = 4.25 kHz
		110 =4kHz
		111 = 3.75 kHz
		000 = 3 kHz (for 25k Channel Space) 001 =
		2.5 kHz (for 12.5k Channel Space)
		010 = 2.75 kHz
		011 =3.5 kHz
REG_43<5:4>	0b00	BW Mode Selection.
		00=12.5k; 01=6.25k; 10 = 25k/20k

Digital Walkie-Talkie

When used as a digital transceiver, all audio filters need to be bypassed, use RF_EnterBypass(), and exit this mode to enable
Use RF_ExitBypass()

Hardware Design

SeeBK4819Datasheet.