VerilogBoy Handheld

Reference Manual

Hardware and Software Interface

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DRAFT

Preface

This documentation is mainly about the internal design of VerilogBoy Handheld. This document is intended to serve as a reference manual for developers. This is not a tutorial or a user manual or a service manual.

How to read this document

This is a warning about something.

0.1 Formatting of numbers

When a single bit is discussed in isolation, the value looks like this: `0`, `1`.

Binary numbers are prefixed with `0b` like this: `0b0101101`, `0b11011`, `0b00000000`. Values are prefixed with zeroes when necessary, so the total number of digits always matches the number of digits in the value.

Hexadecimal numbers are prefixed with `0x` like this: `0x1234`, `0xDEADBEEF`, `0xFF04`. Values are prefixed with zeroes when necessary, so the total number of characters always matches the number of nibbles in the value.

Examples:

	4-bit	8-bit	16-bit
Binary	`0b0101`	`0b10100101`	`0b0000101010100101`
Hexadecimal	`0x5`	`0xA5`	`0x0AA5`

0.2 Register definitions

Register 0.1: `0x1234` - This is a hardware register definition

`R/W-0`	`R/W-1`	`U-1`	`R-0`	`R-1`	`R-x`	`W-1`	`U-0`
`VALUE<1:0>`		`-`	`BIGVAL<7:5>`			`FLAG`	`-`
bit 7	6	5	4	3	2	1	bit 0

Top row legend:

R Bit can be read.

W Bit can be written. If the bit cannot be read, reading returns a constant value defined in the bit list of the register in question.

U Unimplemented bit. Writing has no effect, and reading returns a constant value defined in the bit list of the register in question.

-n Value after system reset: `0`, `1`, or x.

`1` Bit is set.

`0` Bit is cleared.

x Bit is unknown (e.g. depends on external things such as user input).

Middle row legend:

`VALUE<1:0>`	Bits 1 and 0 of VALUE
`-`	Unimplemented bit
`BIGVAL<7:5>`	Bits 7, 6, 5 of BIGVAL
`FLAG`	Single-bit value FLAG

In this example:

- After system reset, VALUE is `0b01`, BIGVAL is either `0b010` or `0b011`, FLAG is `0b1`.
- Bits 5 and 0 are unimplemented. Bit 5 always returns `1`, and bit 0 always returns `0`.
- Both bits of VALUE can be read and written. When this register is written, bit 7 of the written value goes to bit 1 of VALUE.
- FLAG can only be written to, so reads return a value that is defined elsewhere.
- BIGVAL cannot be written to. Only bits 5-7 of BIGVAL are defined here, so look elsewhere for the low bits 0-4.

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Chapter 1

MIPI DSI controller (DSIC)

1.1 DSIC introduction

The display serial interface (DSI) is part of a group of communication protocols defined by the MIPI®Alliance. The DSIC implements a MIPI®DSI host controller and MIPI®D-PHY to provide an interface between the system and a DSI-compliant display.

Since the DSI specification is non-public and requires an NDA, the core was built using bits and pieces available throughout the Web: presentations, display controller/SOC datasheets, various application notes and Android kernel drivers. The author is not associated in any way with the MIPI Alliance. The core has never been verified for compliance with the DSI standard and it probably lacks many of its features.

1.2 DSIC main features

- Implement MIPI®D-PHY
- Transmission of command mode packets through the MMPB interface
- Transmission of video mode packets through the simple pixel FIFO interface
- Support up to one D-PHY data lanes by default
- Uni-direction transmission only
- Support non-continuous clock in D-PHY clock lane
- ECC and checksum capabilities
- Support 24-bit RGB mode

1.3 DSIC registers

Register 1.1: `0x10` - DSIC_CTL - MIPI DSI Control

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
–	RST_OUT	FORCE_LP	TIM_EN	DATA_INV	CLK_INV	LP_REQ	CLK_EN
bit 7	6	5	4	3	2	1	bit 0

bit 7 **Unimplemented**: Read as `0`

bit 6 **RST_OUT**: Set output level of LCD reset line

bit 5 **FORCE_LP**: Force timing generator to stop and switch to LP mode

bit 4 **TIM_EN**: Timing generator enable bit

bit 3 **DATA_INV**: Set data lane inversion

bit 2 **CLK_INV**: Set clock lane inversion

bit 1 **LP_REQ**: Request to switch to LP mode Write `0b1` to this bit will request the controller to switch to LP mode. Upon reading, this bit indicate if the controller is currently in the LP mode.

bit 0 **CLK_EN**: DSI clock lane output enable bit

Register 1.2: `0x11` - DSIC_TICK - DSI Tick Divider Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TICK<7:0>							
bit 7	6	5	4	3	2	1	bit 0

bit 7-0 **TICK**: Tick divider value. $f_{TICK} = f_{DSI}$ / TICK. f_{TICK} decides the speed of LP mode transmission.

Register 1.3: `0x12` - DSIC_TXDR - DSI LP Mode Transmission Data Register

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TXDR<7:0>							
bit 7	6	5	4	3	2	1	bit 0

bit 7-0 **TXDR**: Raw byte to be sent in the LP mode.
Writing to this register will trigger the transmission immediately.

Register 1.4: `0x13` - DSIC_HFP - DSI Timing HFP Length Register

W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
HFP<7:0>							
bit 7	6	5	4	3	2	1	bit 0

bit 7-0 **HFP**: Horizontal front porch length

Register 1.5: `0x14` - DSIC_HBP - DSI Timing HBP Length Register

W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
HBP<7:0>							
bit 7	6	5	4	3	2	1	bit 0

bit 7-0 **HFP**: Horizontal back porch length

Register 1.6: `0x15` - DSIC_HACTL - DSI Timing HACT Length Low Register

W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
HACT<7:0>							
bit 7	6	5	4	3	2	1	bit 0

bit 7-0 **HACT**: Horizontal active pixel length (This register only contain low 8 bits)

Register 1.7: `0x16` - DSIC_HTL - DSI Timing HTotal Length Low Register

W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
HT<7:0>							
bit 7	6	5	4	3	2	1	bit 0

bit 7-0 **HT**: Horizontal total length (This register only contain low 8 bits)

Register 1.8: `0x17` - DSIC_HATH - DSI Timing HACT and HTotal Length High Register

W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
HACT<11:8>				HT<11:8>			
bit 7	6	5	4	3	2	1	bit 0

bit 7-4 **HACT**: Horizontal active pixel length (This register only contain high 4 bits)

bit 3-0 **HT**: Horizontal total length (This register only contain high 4 bits)

Register 1.9: `0x18` - DSIC_VFP - DSI Timing VFP Length Register

W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
VFP<7:0>							
bit 7	6	5	4	3	2	1	bit 0

bit 7-0 **VFP**: Vertical front porch length

Register 1.10: `0x19` - DSIC_VBP - DSI Timing VBP Length Register

W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
VBP<7:0>							
bit 7	6	5	4	3	2	1	bit 0

bit 7-0 **VFP**: Veritcal back porch length

Register 1.11: `0x1A` - DSIC_VACTL - DSI Timing VACT Length Low Register

`W-0`	`W-0`	`W-0`	`W-0`	`W-0`	`W-0`	`W-0`	`W-0`
`VACT<7:0>`							
bit 7	6	5	4	3	2	1	bit 0

bit 7-0 **VACT**: Vertical active pixel length (This register only contain low 8 bits)

Register 1.12: `0x1B` - DSIC_VTL - DSI Timing VTotal Length Low Register

`W-0`	`W-0`	`W-0`	`W-0`	`W-0`	`W-0`	`W-0`	`W-0`
`VT<7:0>`							
bit 7	6	5	4	3	2	1	bit 0

bit 7-0 **VT**: Vertical total length (This register only contain low 8 bits)

Register 1.13: `0x1C` - DSIC_VATH - DSI Timing VACT and VTotal Length High Register

`W-0`	`W-0`	`W-0`	`W-0`	`W-0`	`W-0`	`W-0`	`W-0`
`VACT<11:8>`				`VT<11:8>`			
bit 7	6	5	4	3	2	1	bit 0

bit 7-4 **VACT**: Vertical active pixel length (This register only contain high 4 bits)

bit 3-0 **VT**: Vertical total length (This register only contain high 4 bits)

Appendices