A mm-Wave MIMO Transmitter with a Digital Beam Steering Capability Using CMOS All-Digital Phase-Locked Loop Chips

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***Abstract*— In this paper, we propose a mm-wave transmitter architecture intended for radar and 5G MIMO applications with beam steering over 57-63 GHz frequency band. Each transmitter chain comprises an all-digital phase-locked loop (ADPLL) CMOS IC chip intended to be dictated to a single antenna unit within an array. For demonstration purposes, each IC is embedded on a printed circuit board (PCB) to provide beam steering using highly accurate digital approach. The overall transmitter is connected to an antenna array with half wavelength spaced elements to maximize the beam scanning coverage. The ADPLL boards are fabricated and a calibration technique is carried out to align amplitude-phase of all transmitter channels at the input of the antenna array for beamforming goal. It is demonstrated that phase noise performance of the ADPLLs has considerable impact on the phase-alignment accuracy.**

Keywords—5G MIMO communication; ADPLL; Digital beam steering; Phase alignment; Phase noise; 60GHz

I. Introduction

Nowadays, agile 60 GHz wireless access circuitry is in high demand for various applications, such as future multi-gigabit 5G services and high-resolution FMCW radars. However, this mm-wave frequency band suffers from a higher propagation loss and is more vulnerable to obstacle blockages especially in indoor environments. Hence, multiple-input multiple-output (MIMO) systems with beam steering capability are considered an attractive solution which improves capacity of wireless channels and reduces the impact of blockage-interference through steering the beam of antenna array to the desired direction [1], [2]. So, it is specifically considered as a key technology for the emerging generation of mobile radio networks (5G Massive MU-MIMO communications) [3], [4]. Since mm-wave antennas are directional with capability of narrow beams, the accuracy of beam scanning is very crucial to assure a wireless communication with suitable link budget. In this work, we propose and develop a 60 GHz beam steering unit (BSU) with MIMO capabilities based on a digitally-intensive manner using an all-digital phase-locked loop (ADPLL). In principle, ADPLL is exploited as a phase steering component and a compact transmitter to provide full-range (360°) superior phase shift resolution of much finer than 3° at 60GHz. This accuracy is comparable to state-of-the-art CMOS phase shifters [5], [6]. It is noteworthy that the above concept has been expressed but not investigated in the literature [7]. In Section II, the architecture of the new proposed MIMO transmitter is explained. Section III introduces the utilized ADPLL chip and describes the theory of operation for MIMO beam steering. The experimental results for the demonstrator are represented in Section IV and the effect of phase noise on phase alignment of multiple ADPLLs is examined. Finally, Section V draws the conclusion and future activities to realize the complete demonstration system.

II. MIMO Transmitter Architecture

Fig. 1 illustrates the block diagram of the new proposed paradigm of mm-wave digital BSU with MIMO capabilities based on an array of ADPLLs and antennas whereby each ADPLL is dedicated to a separate antenna. Continual advancements in CMOS technology and digitally-intensive mm-wave front-end architectures make this solution quite compact and inexpensive. Being able to place an IC chip very close to an antenna avoids issues with mm-wave interconnect power losses. As viewed, a common reference crystal oscillator locks all ADPLLs at one frequency and phase whereas the transmitter chains are digitally controlled by a host controller i.e. FPGA or micro-controller through a simple SPI interface for frequency locking and time synchronization. Once locked-synchronized, the output phases of different ADPLLs are aligned by monitoring this parameter via both 60GHz and a test 2GHz outputs to collect more data for comparison and calibrate the unwanted phase offsets. When all channels are phase-aligned, the transmitter beam can be steered very accurately by applying the desired digital phase differences.

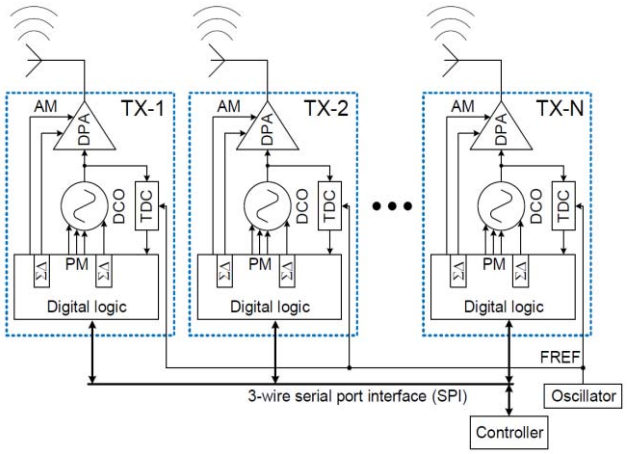

Fig. 1. The proposed 60GHz MIMO transmitter with digital beam steering.

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III. ADPLL Structure and Theory of Operation

The transmitter RF-SoC is an all-digital PLL (ADPLL) realized in 65nm CMOS technology aimed for 60GHz FMCW radar applications, e.g., as in [8]. Fig. 2 exhibits the detailed block diagram of the 60GHz digitally-intensive loop. Besides the 60GHz GSG output, the RF pads consist of a reference signal from an external crystal oscillator and a 2GHz output for monitoring purposes which is a low frequency replica (divide-by-32; CKV/32) of the 60GHz output. The output power of the ADPLL is 5dBm ± 1dB on a 50Ω load in the tuning range of 56.4-63.4 GHz using a 3-stage power amplifier (PA).

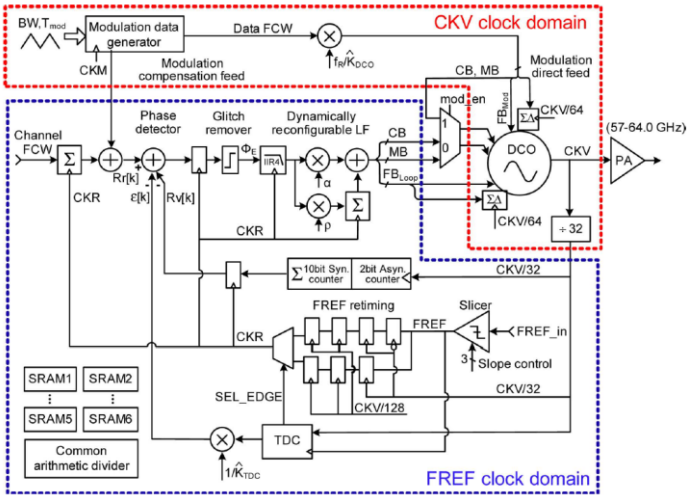

Fig. 2. Block diagram of the 60GHz all-digital loop with controllable phase.

The modulation data is injected by a 2-point scheme in both the reference path and the digitally-controlled oscillator (DCO) to support a wideband behavior (MIMO mode). To adjust the output phase of the overall loop, two solutions can be conducted either by a digital phase offset register or by a 2-point single-pulse frequency modulation. In the former, the phase error (Φ_E in Fig. 2) is altered by an intentional phase offset applied in the digital loop filter leading to change the loop output phase. The latter is performed by varying the frequency control word (FCW) for a short while (single-pulse shape) in the 2-point modulation path. The produced phase difference $\Delta\Phi_0$ is

$$\Delta\Phi_0 = 2\pi f_r M \int_{\tau_0}^{\tau_0+\Delta\tau} \Delta(FCW)d\tau \qquad (1)$$

wherein f_r is the reference frequency (40MHz) and M = 32 is the loop frequency division factor. For simple implementation, the method of phase offset register is adopted in this system.

IV. Measurement Results and Performance

To target a demonstrator and to evaluate the beam steering performance, each ADPLL chip is assembled on an individual board as the single chain of the MIMO transmitter.

A. Single transmitter chain

The picture of the fabricated board is shown in Fig. 3. The white board is on-board matching network with 1dB loss in the whole frequency range, including the 60GHz wire bonding.

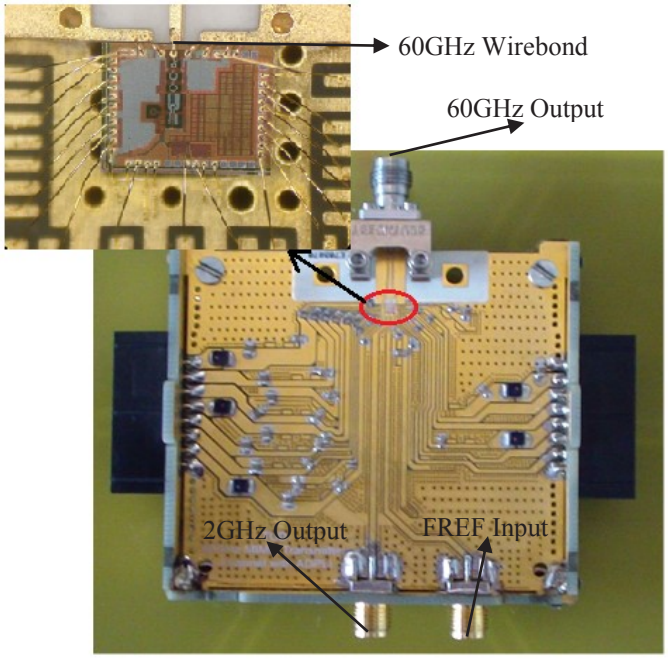

Fig. 3. The fabricated ADPLL board with the IC directly wirebonded.

B. Calibration and phase alignment

In order to execute very precise beam steering, a calibration technique is required to align the amplitude-phase of all transmitter channels (ADPLLs). This strategy is established based on alignment with a reference channel (round robin procedure) in which the outputs of two chains (the reference and under test ADPLLs) are combined to observe cancellation point where the out-of-phase condition (the same amplitude and 180° phase difference) is achieved. The measurement setup for validation is depicted in Fig. 4. The 60GHz and 2GHz outputs of the two ADPLLs are combined by a Magic-T and a stripline power combiner, respectively to monitor the combined output power on a spectrum analyzer. When two chips are frequency-locked and time-synchronized by a common 40MHz crystal oscillator and an Virtex-5 FPGA evaluation board, the relative phase offset is swept to acquire the cancellation curve at the two outputs, as reported by Fig. 5.

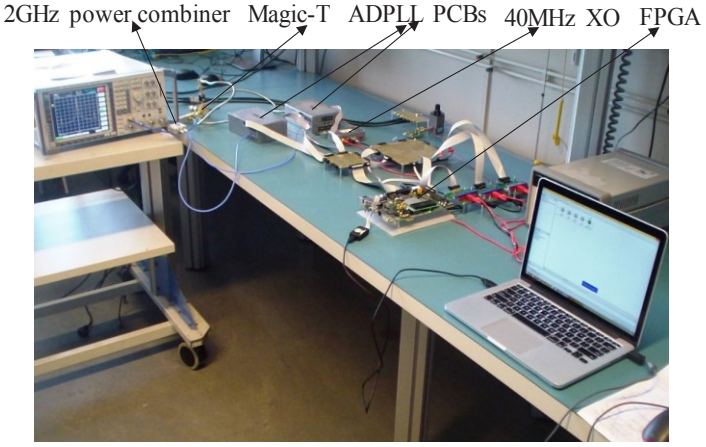

Fig. 4. The experiment setup to verify the calibration phase-alignment.

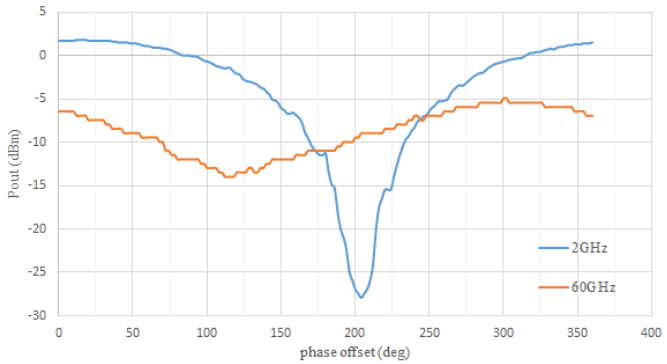

Fig. 5. The measured cancellation curve at the two outputs for f = 62GHz.

It is noticeable that the cancellation level at the 60GHz output is much less than the 2GHz one (30dB and 9dB for the 2GHz and 60GHz outputs, respectively) implying that the phase alignment of the two ADPLLs at 60GHz is not as accurate as at 2GHz. Because of amplitude balance at the two outputs, the only reason of this issue is the phase noise difference as the 2GHz path is equal to the 60GHz output of the loop before PA divided by 32. Therefore, the phase noise will be degraded by 20log32 = 30.1dB at 60GHz with respect to 2GHz. The measured phase noise at the 2GHz output is plotted in Fig. 6 revealing a residual PM value of about 1.3° which will increase to 1.3° x 32 = 42° for the 60GHz output. Obviously, this phase variation arising from ADPLL phase noise destroys the phase-alignment accuracy significantly.

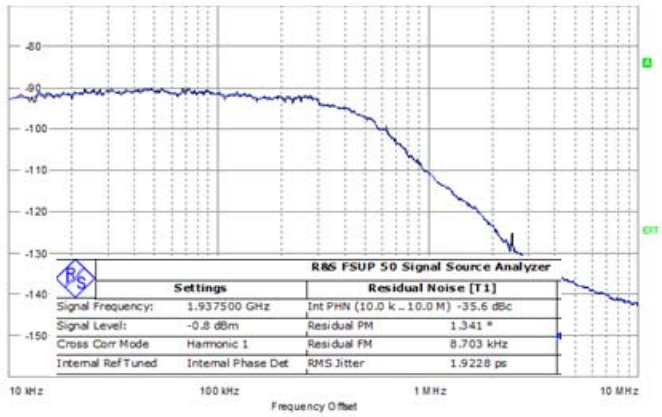

Fig. 6. The measured phase noise profile at the 2GHz output for f = 62GHz.

C. Suggestions and solutions

The phase noise performance at the 60GHz output should be improved as good as the current 2GHz profile to fulfil the required accuracy for phase alignment. The effective factors include time resolution of the time-to-digital converter (TDC) (currently 12ps), reference frequency (now limited to 40MHz), loop filter parameters and phase noise of reference and DCO. The calibration process is simulated by MATLAB using the time-domain model of ADPLL. Fig. 7 presents the normalized cancellation graph for various ADPLL settings. The required accuracy (like 2GHz) at 60GHz is attained with Δt_{TDC} = 5ps, f_r = 250MHz, L_{REF} = -150dBc/Hz and L_{DCO} = -125dBc/Hz.

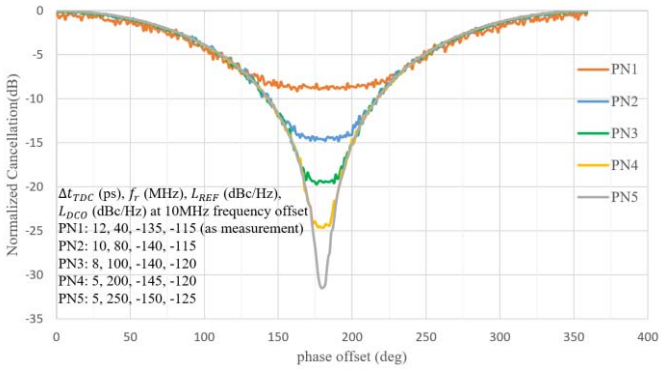

Fig. 7. The simulated cancellation graph at the 60GHz output for various ADPLL settings (computed by the ADPLL time-domain model in MATLAB).

V. Conclusion and Future Work

A new MIMO transmitter architecture with a digital beam steering capability across 57-63 GHz band has been proposed in this paper. To provide high accuracy for beam scanning, all-digital phase-locked loop (ADPLL) system has been opted as the transmitter chain. As a proof-of-concept, the ADPLL chain has been fabricated and assembled on a board, then measured to verify the performance. A calibration strategy has been explored to align the phase of all ADPLL chains for beamforming and validated by an experimental setup. It has been demonstrated that phase-alignment precision at 60GHz is much worse than 2GHz due to much higher phase noise (about 30dB). Thus, some solutions have been suggested to improve the phase noise performance for ADPLL which should be implemented as future work to allow a 60GHz MIMO transmitter with highly accurate beam steering capability required in 5G wireless communications.

Acknowledgment

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