



LimeNet-Micro v2.0

CONTROLLED IMPEDANCE				STACKUP AND LAYER DESCRIPTION																	
GENERAL PARAMETERS				<div><div>GERBER LAYER NAMES:</div><div><div><div>GTP Top solder paste</div><div>GTO Silkscreen</div><div>GTS Soldermask (halogen free)</div><div>GTL 0.5oz+plating</div></div><div><div>PP 6.8mil</div><div>CORE</div><div>PP</div><div>CORE</div><div>PP 6.8mil</div></div><div><div>GBL 0.5oz+plating</div><div>GBS Soldermask (halogen free)</div><div>GBD Silkscreen</div><div>GBP Bottom solder paste</div></div></div><div><div>TH via</div><div>Top-Bot</div></div><div><div>ELECTRICAL LAYERS:</div><div>Top: RF/PWR/GND</div><div>L2: GND</div><div>L3: Signal/PWR/GND</div><div>L4: PWR/Signal/GND</div><div>L5: GND</div><div>Bottom: RF/Signal/PWR/GND</div><div>ADDITIONAL LAYERS:</div><div>Mechanical 1: Board cutout</div><div>ASM TOP: Assembly top</div><div>ASM BOT: Assembly bottom</div><div>Mechanical 13: Component 3D body</div><div>Notes: Board shape and frame</div></div></div>																	
Parameter	Layer /Layers	Value																			
Copper foil thickness	Top	17.5um																			
Dielectric thickness between layers	Top-L2	173um (6.8 mils)																			
Dielectric permittivity between layers (Er)		4.2																			
Copper foil thickness	Bottom	17.5um																			
Dielectric thickness between layers	Bottom-L11	173um (6.8 mils)																			
Dielectric permittivity between layers (Er)		4.2																			
CALCULATIONS																					
RF (Top)	Target impedance	Single-ended	50R																		
	Additional comments	Top layer, no side GND plane																			
	Top layer copper foil thickness	17.5 um																			
	Track width	0.325 mm (12.795 mils)																			
	Top layer copper foil thickness	173um (6.8 mils)																			
	Dielectric thickness between layers	Top-L2	173um (6.8 mils)																		
	Dielectric permittivity between layers (Er)		4.2																		
	Approximate microstrip line impedance	49.99 Ohms (+/- 10% tolerance)																			
RF (Top)	Target impedance	Differential	100R																		
	Additional comments	Top layer, no side GND plane																			
	Top layer copper foil thickness	17.5 um																			
	Track width	0.2 mm (7.874 mils)																			
	Track spacing	0.14 mm (5.511 mils)																			
	Top layer copper foil thickness	173um (6.8 mils)																			
	Dielectric thickness between layers	Top-L2	173um (6.8 mils)																		
	Dielectric permittivity between layers (Er)		4.2																		
Approximate microstrip line impedance	100.6 Ohms (+/- 10% tolerance)																				
RF (Bottom)	Target impedance	Single-ended	50R																		
	Additional comments	Bottom layer, no side GND plane																			
	Top layer copper foil thickness	17.5 um																			
	Track width	0.325 mm (12.795 mils)																			
	Top layer copper foil thickness	173um (6.8 mils)																			
	Dielectric thickness between layers	Bottom-L5	173um (6.8 mils)																		
Dielectric permittivity between layers (Er)	4.2																				
Approximate microstrip line impedance	49.99 Ohms (+/- 10% tolerance)																				
HDMI (Bottom)	Target impedance	Differential	100R																		
	Additional comments	Bottom layer, no side GND plane																			
	Top layer copper foil thickness	17.5 um																			
	Track width	0.2 mm (7.874 mils)																			
	Track spacing	0.14 mm (5.511 mils)																			
	Top layer copper foil thickness	173um (6.8 mils)																			
	Dielectric thickness between layers	Bottom-L5	173um (6.8 mils)																		
	Dielectric permittivity between layers (Er)		4.2																		
Approximate microstrip line impedance	100.6 Ohms (+/- 10% tolerance)																				
				VERY IMPORTANT NOTES																	
				GENERAL PCB SPECS		ADDITIONAL REQUIREMENTS															
				Minimum copper to copper spacing		0.1mm (3.9mil)		● All 0.2mm vias including 0.35mm ring and 0.2mm drill via-in-pads (IC1) must be resin filled with metal cap.													
				Minimum track width		0.1mm (3.9mil)															
				PCB thickness		1.6mm +/-10%		IC1 thermal pad vias with 0.4mm ring and 0.2mm drill must be resin filled with metal cap. IC1 thermal pad vias with 0.5mm ring and 0.2mm drill must be left open (NO resin fill with metal cap). 4 vias in total, marked with note.													
				PCB material		IT-180A preferred or equivalent RF-rated material (up to 3 GHz or higher)															
				Copper weight		External layer	0.5 oz+plating	● Electrical test : 100 % netlist.													
						Internal layer	1 oz														
				Solder mask		DARK BLUE		● Boards are to be individually bagged.													
						Both sides															
						Halogen free															
						Glossy finish (NOT matte)															
				Silkscreen		White epoxy ink		PCB vendor to silkscreen UL and RoHS compliance marks, vendor logo and date code on bottom where shown (ignore if none of the info will be placed on PCB) Assembly note: Assembly house MUST provide notes in paper with shipped board if there were any changes during assembly and the board is not assembled 100% according to BOM and P&P files. Note example: <table><tr><th>Part</th><th>Initial BOM asm. note</th><th>Current PCB status</th><th>Comment</th></tr><tr><td>R1</td><td>FIT</td><td>NF</td><td>Not mounted due to bad footprint</td></tr><tr><td>IC5</td><td>FIT</td><td>NF</td><td>Not mounted due to part shortage</td></tr></table>		Part	Initial BOM asm. note	Current PCB status	Comment	R1	FIT	NF	Not mounted due to bad footprint	IC5	FIT	NF	Not mounted due to part shortage
						Part	Initial BOM asm. note			Current PCB status	Comment										
						R1	FIT			NF	Not mounted due to bad footprint										
						IC5	FIT			NF	Not mounted due to part shortage										
				Hole types on the PCB and information		Plated <input checked="" type="checkbox"/>	Non-plated <input checked="" type="checkbox"/>														
						Hole diameters are final ● manufactured diameters INCLUDING HOLE METALIZATION.															
				Route process		V-score <input type="checkbox"/>	Tab route <input checked="" type="checkbox"/>														
						V-score and tab route <input type="checkbox"/>															
Panel		Yes <input type="checkbox"/>	No <input checked="" type="checkbox"/>																		
Surface finish (both sides)		HASL lead free <input type="checkbox"/>																			
		HASL with lead <input type="checkbox"/>																			
		Immersion gold 0.05-0.10um of gold over 2.50-5.00um of nickel <input checked="" type="checkbox"/>																			
		OSP <input type="checkbox"/>																			
		Hard gold <input type="checkbox"/>																			