IT6604/IT6605 Register Table V1.03

Term:

RO: Read Only W/R: Read/Write

W/IX.	Read/Write					
Reg Offset	Reg_Name	W/R	Bits	Status	Defau lt	Description
	VID_L	RO	7:0		0x00	
	Backup_reg2	WR		Reserved	0x00	
	DEVID_L	RO	7:0			Device ID (Low word)
	DEVID_H	RO	7:0			Device ID (High word)
	DevRev	RO	7:0			Device Revision Number
	Rst_Ctrl	W/R	7	REG_CDR_RST	0	1: reset CDR.
OAOS	KSt_Ctf1	VV/1C		Reserved	0	1. Teset CDR.
				REG_AUTO_CDR_RST	0	1: Auto reset CDR
				REGRST	0	1: Software reset the clock domain include
					U	control registers to default
			3	Reserved(not used)	0	
			2	AUDRST	0	1: Software reset audio logic
			1	VDORST	0	1: Software reset video logic
			0	SWRST	0	1: Software reset all logic
0x06	Pwd_Ctrl0	W/R	7	PWD_Ch2	0	1: Power down channel2
			6	PWD_Ch1	0	1: Power down channel1
			5	PWD_Ch0	0	1: Power down channel0
			4	PWD ACLK	0	1: Power down Audio clock domain
			3	PWD_PCLK	0	1: Power down Pixel clock domain
			2	PWD_APLL	0	1: Power down Audio PLL
			1	PWD_RXPLL	0	1: Power down Pixel PLL
				PWD_ALL	0	1: Power down all AFEs and Logic blocks
0x07	Pwd_Ctrl1	W/R		Sel_port	0	Select active port:
OAO7	r wa_curr	VV/1C	_	Bei_port	ľ	0: portA
						1: portB (IT6605 only)
			3	PWD_AFEall	0	1: Power down all AFEs
			-	PWDC_ETC	0	1: Power down certain AFE blocks
			1	PWDC_SRV	0	1: Power down AFE equalizer
			0	EN_AutoPWD	0	1: Auto Power down whole chip when no
			0	EN_Autor WD	ľ	clock is detected
0x08	VIO_Ctrl	W/R	7	VIO Slew		Video data Slew rate
UAUU	VIO_Cui	W/IX	,	VIO_SICW	1	Slew rate: 0:Fast; 1:Slow
			6.4	VIO_ST		VDATA Driving Strength
			0.4	V10_51		000:2mA; 001:4mA;
					001	010:6mA; 011:8mA;
					001	100:10mA;101:12mA;
						110:14mA;111:16mA;
			3	Vclk_Slew		VCLK Slew rate
			3	V CIK_SIC W	1	Slew rate: 0:Fast; 1:Slow
			2.0	Vclk_ST		VCLK Driving Strength
			2.0	VCIK_ST		000:2mA; 001:4mA;
					011	010:6mA; 011:8mA;
					011	100:10mA;101:12mA;
						110:14mA;111:16mA;
0x09	AIO_Ctrl	W/R	7	AIO_Slew	1	Audio data Slew rate
		.,,,,,	′	<u>-</u>	[Slew rate: 0:Fast ; 1:Slow
			6.4	AIO_ST	001	
			0.7		001	
						Audio data Driving Strength
						000:2mA; 001:4mA;
<u> </u>	1		1	<u> </u>		010:6mA; 011:8mA;

010:6mA; 011:8mA; 100:10mA;101:12mA;

		ı	1			140.44 . 444.45 . 4
						110:14mA;111:16mA;
			3	Mclk_Slew	1	Audio clock Slew rate
						Slew rate: 0:Fast; 1:Slow
			2:0	Mclk_ST	001	Audio Driving Strength
						000:2mA; 001:4mA;
						010:6mA; 011:8mA;
						100:10mA;101:12mA;
						110:14mA;111:16mA;
	Reserved	W/R			0x2A	
	Reserved	W/R			0xA5	
0x0C	BIST_Ctrl	W/R	0	ARAM_BIST_EN	0	Internal Audio FIFO BIST test circuits
0x0D	BIST_Result1	RO	7	ARAM_bo_faultHQ		Audio FIFO BIST status
			6:0	ARAM_D6FaulStauHQ		
0x0E	Reserved					
0x0F	Block_Sel	W/R	0	Block_ID	0	Register block select
	_			_		0: block 0 is select for Reading and writing
						1: block 1 is select for Reading and writing
0x10	Sys_state	RO	7	RXPLL_LOCK	X	1: RX PLL is lock
	<i>,</i> –		_	RXCK_Speed	X	1: RX clock is lower than 80Mhz
				RXCK_VALID	X	1: Clock is valid
				HDMI_MODE	X	1: HDMI mode or DVI mode (value:0)
				P1_PWR5V_DET	X	1: Port-1 5V is detect
				SCDT	X	1: Video Sync is stable
				VCLK_DET	X	1: Video clock is detect
				PWR5V_DET	X	1: Port-0 5V is detect
0x11	HDCP_Ctrl	W/R		ExtROM		1: select internal OTP as HDCP key ROM
UXII	IIDCI_Cui	VV/IX		reserved	UAG	1: Disable external ROM write function
				reserved		1: Select 0x76 as DDC address.(default is
				reserved		0x74)
				HDCP_RomDisWr		1: Enable HDCP
				HDCP_A0		1. Eliable TIDCF
				reserved		
				HDCP_en		
0x12	HDCP_Status	RO		reserved		Show the HDCP authentication stauts
UX12	HDCr_Status	KU		HDCP_ADVCipher		Show the HDCF authentication status
				HDCP_EESS		
				HDCP_KeyRd_Fail_Flag		
				Hdcp_on_Flag		
0x13	IntomuntO	RO	_	WidMode Che		'1': Video mode change
UX13	Interrupt0	KO		VidMode_Chg		'1': HDMI/DVI mode swap change
				HDMIMode_Chg SCDTOFF		'1': Video stable is off
				SCDTOFF		'1': Video stable is on
			ľ	Pwr5VOff		'1': Selected port 5V is off '1': Selected port 5V is on
Ov 1.4	Interment 1	DO		Pwr5Von	-	'1': Left Mute Packet is received
0x14	Interrupt1	RO		PktLeftMute		
				NewAudioPkt_Det		'1': New Audio Packet detect
				NewACPPkt_Det		'1': New ACP Packet detect
				NewSPDPkt_Det		'1': New SPD Packet detect
				NewMPEGPkt_Det		'1': New MPEG Packet detect
				NewAVIPkt_Det		'1': New AVI Packet detect
				NoAVI_Rcv		'1': No AVI Packet is received
0-: 1.7	Into amount 2	DC		PktSetMute		'1': Set Mute Packet is received
0x15	Interrupt2	RO		ROMFault		'1': ROM access Fault Flag
				AutoAudMute		'1': Audio Auto Mute Flag
				AudFIFOErr		'1': Audio FIFO error Flag
				ECCERR		'1': EDD error Flag
				Auth_done		'1': Authentication Done Flag
0.15	T	111/F	0	Auth_start	0.25	'1': Authentication Start Flag
0x16	Interrupt_MASK0	W/R	5:0		0x3F	Mask of interrupts defined in reg0x13

1		1	1	1	T		1 771 1
							1: The Interrupt is effective
1: The Interrupt is effective	0.17	T MACIZI	XX/D	7.0		0.00	
0x18	OX1/	Interrupt_MASK1	W/R	7:0		OXOO	
	0-10	L. C. MACKO	XX/D	7	Ch. HDCD in	0	
Signals Wilden	0X18	Interrupt_MASK2	W/K	/	CIr_HDCP_int	U	
District Section District				5.0		0**00	
Description of the content of the				3.0		UXUU	
Dk 19 Interrupt_ctr W/R 7 Clr_SetMute_int 0 1.Clear interrupts generated by set mute packet 5 IntrOutType 1 Interrupt pin output type 1.0pen drain 0.push pull 1 Interrupt pin output type 1.0pen drain 0.push pull 0.push pull 1 Interrupt pin output polarity 1.dow active 0.pin pull 0.push pull							
	0x19	Interrupt ctr	W/R	7	Clr SetMute int	0	
Simple	01112		,				
South Sout				6	Clr LeftMute int	0	
				5	IntrOutType	1	Interrupt pin output type
A IntPol							1:open drain
Served							
Ochigh active CIr_Audio_int Ochigh CIr_Clear interrupts generated by Audio FIFO CIr_Audio_int Ochigh CIr_Clear interrupts generated by Packet Signals Ochigh CIr_Mode_int Ochigh CIr_Audio_int CIr_Audio_i				4	IntPol	1	
3 Clr_Audio_int							
				3	Clr_Audio_int	0	
1 Clr_Pkt_int 0 F.Clear interrupts generated by Packet signals				_	G. Pag.		V
Signals Sign							
O Clr_Mode_int				1	Clr_Pkt_int	0	
Ox1A Misc_ctrl W/R 7 reserved 0 0							signais
Ox1A Misc_ctrl W/R 7 reserved 0 0				0	Clr Mode int	0	1. Clear interrupts generated by mode
Misc_ctrl				0	CII_iviouc_iiit	U	1
6 reserved 0 1 1 2 2 3 2 5 7 2 5 2 5 2 5 2 5 2 5 5	0x1A	Misc ctrl	W/R	7	reserved	0	Change
Served 1 1:auto timeout when no DE detected	071111	1,1150_011	11772				
A Timeout_en 1 1:auto timeout when no DE detected 3 reserved 0 2 SelDebugHL 1 1:For Debug signals selecting 1 Vsync_Out_pol 0 Vsync output polarity 0 0: Negitave 1: Positive 0 Hsync_Out_pol 0 Hsync output polarity 0: Negitave 1: Positive 0 Reserve 0: Reserve 0: Negitave 1: Positive 0 ChSyncpol 0 Video output data configuration, refer the datasheet and programming guide. 1: output sync signal polarity from 1: we no output sync signal polarity as the input. 5 Swap_O16b 0 1: when output 16-bit video data format, the other 8 bits will be forced to low 4 Swap_Ch422 Channel Swap used in YUV422 mode. 0 0: Cr/Cb assigned to Data[23:16] 1: Cr/Cb assigned to Data[7:0] 3 Swap_OutRB 0 1: swap output channel 0 and channel 2 2 Swap_ML 0 1: swap output direction(MSB/LSB) 1 Swap_Pol 0 1: swap input data polarity							
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1 Swap_Pol 0 1: swap input data polarity				2		0	
0 Swap_RB 0 1: swap input channel 0 and channel 2				1		0	
				0		0	

0x1C	Video_Ctrl1	W/R	7	DNFreeGo	0	'1': Dither Noise Pattern Select
OXIC	video_cuii	VV / IX			0	'1': Sync Embedded output
				EN_Dither	0	'1': Enable dither function
				En_Dither EnUdFilt		
					0	'1': Enable color up/down filter
			3	OutDDR	0	'1': Double data rate output
			2		0	'1': CCIR6565 output
			1		0	'1': CCIR656 Output FIFO reset
			0	EnAVMuteRst	0	'1': Enable Output FIFO reset when
0.10	77 II G. 1	XXI/D		x 11 1 ·	0.20	AVMUTE is set.
0x1D	Vclk_Ctrl	W/R			0x30	'1': Invert internal video clock phase
			4	Velk_inv		'1': Invert video output clock phase
			3:2	VclkbDly		Fine tune internal video clock delay (1ns for 1 step)
			1.0	VelkDly		Fine tune video output clock delay.
			1.0	VERDIY		(1ns for 1 step)
0x1E	I2CIO_Ctrl	W/R	7	DSda_Slew	OvDA	Slew rate of command I2C pins:
OXIL	12010_011	VV / IX	,	DSda_Siew		0:Fast; 1:Slow
			6	DDCSda_Slew		Slew rate of HDCP I2C pins:
				BB CSuu_Sie W		0:Fast; 1:Slow
			5:4	RomI2C_ST		Current strength of ROM I2C pins:
						00:4mA; 01:8mA;
						10:12mA;11:16mA;
			3:2	DataI2C_ST		Current strength of command I2C pins:
						00:4mA; 01:8mA;
						10:12mA;11:16mA;
			1:0	DDC_ST		Current strength of HDCP I2C pins:
						00:4mA; 01:8mA;
						10:12mA;11:16mA;
0x1F	RegPktFlag_ctrl	W/R	4	ACP	0	0: interrupt only when first receiving or a
				SPD	0	new value is updated
				Audio	0	1: interrupt each time a packet is received
			1	MPEG	0	
020	CCC CTDI	W/D		AVI	0	Eachle autout data action to according
0x20	CSC_CTRL	W/R	7	VDGatting	0	Enable output data gating to zero when no Video display.
			6	VDIOLDisable	0	Disable video low bits data(D3~D0)
				EN_TriVDIO	0	1: Enable Tristate Video Data Only
			3	EN_INVDIO		0: Tristate Video Data with Video Sync
			4	ForceColMod	0	0: Input color mode auto detect
			-	Torceconviou		1: Force input color mode as bit[3:2] setting
			3.2	ColMod_Set	00	Input color mode set
			_	Conviou_set		00: RGB mode
						01: YUV422 mode
						10: YUV444 mode
			1:0	CSCSel	00	00: no color space change (bypass)
		ľ				10: RGB to YUV
						11: YUV to RGB
0x21	CSC_YOFF	W/R	7:0		0x10	Color Space conversion parameters
						matrix tables, refer the programming guide
						Y blank level
	CSC_COFF	W/R	7:0			C blank level
	CSC_RGBOFF	W/R	7:0			R/G/B blank level
0x24	CSC_MTX11_L	W/R	7:0			Color space conversion Matrix
0x25	CSC_MTX11_H	W/R	5:0			Color space conversion Matrix
0x26	CSC_MTX12_L	W/R	7:0			Color space conversion Matrix
0x27	CSC_MTX12_H	W/R	5:0			Color space conversion Matrix
0x28	CSC_MTX13_L	W/R	7:0			Color space conversion Matrix
0x29	CSC_MTX13_H	W/R	5:0		0x00	Color space conversion Matrix

	T					
	CSC_MTX21_L	W/R	7:0			Color space conversion Matrix
	CSC_MTX21_H	W/R	5:0			Color space conversion Matrix
	CSC_MTX22_L	W/R	7:0			Color space conversion Matrix
	CSC_MTX22_H	W/R	5:0			Color space conversion Matrix
	CSC_MTX23_L	W/R	7:0			Color space conversion Matrix
	CSC_MTX23_H	W/R	5:0			Color space conversion Matrix
	CSC_MTX31_L	W/R	7:0		0x49	Color space conversion Matrix
0x31	CSC_MTX31_H	W/R	5:0		0x1D	Color space conversion Matrix
0x32	CSC_MTX32_L	W/R	7:0		0x9f	Color space conversion Matrix
0x33	CSC_MTX32_H	W/R	5:0		0x1E	Color space conversion Matrix
0x34	CSC_MTX33_L	W/R	7:0		0x16	Color space conversion Matrix
0x35	CSC_MTX33_H	W/R	5:0			Color space conversion Matrix
0x3B	Deskew Setting		7:0	Deskew setting, suggestion value is 0x40.	0x00	Suggest Initial Value: 0x40
0x3C	reserve	W/R	7		0	
	reserve	W/R	6		0	
	reserve	W/R	5		0	
	reserve	W/R	4		0	
	reserve	W/R	3		0	
	DE_Bypass	R/W		DE Bypass	0	0: DE regenerated
	DL_Dypuss	10, 11	_	DE Dypuss		1: DE bypassed from TMDS input.
	reserve	W/R	1		0	1. DE by bassed from TVIDS input.
	reserve	W/R	0		0	
0x3D	PG_CTRL2	W/R		OutColMod	10	Output color mode
UASD	TO_CTKL2	VV/IX	7.0	Outconviou		00: RGB
						01:YUV422
						10:YUV444
				reserved	00	10.10 (444
				reserved	00	
				reserved	00	
0v56	CDR Setting		0		0	should set as '1'
0x58	Vid mode	RO		PxVideoStable	U	Indicate if video signal is stable
UAJO	VIu_IIIouc	KO		vidfield		Video field number in interlaced mode
			1	vidinterlacemode		Indicate video is in interlaced mode
				VidModeChg		Indicate video is in interfaced mode Indicate if a video mode change occurs
0x59	Vid_HTotal_L	RO	7:0	Vidiviodeeng		The total pixel count of a line [7:0]
	Vid_HTotal_H	RO		Vid HAct[11:8]		The active pixel count of a line [7.0]
UXJA	Viu_IIIOtai_II	KO				
Ov 5 D	Vid_HAct_L	RO	_	Vid_Htotal[11:8] Vid_HAct[7:0]		The total pixel count of a line [11:8]
						The active pixel count of a line[7:0]
0x5C				Vid_Hsync_Wid[7:0]		The width of Hsync [7:0]
0x5D		RO		Vid_H_Ft_Porch[11:8]		The width of Hsync front porch [11:8]
0.55	H Wilder D. 1	DO		Vid_Hsync_Wid[11:8]		The width of Hsync [11:8]
0x5E	Vid_H_Ft_Porch_ L	RO		Vid_H_Ft_Porch[7:0]		The width of Hsync front porch [7:0]
0x5F	Vid_VTotal_L	RO		Vid_VTotal[7:0]		The total line count of a field [7:0]
0x60	Vid_VTotal_H	RO		Vid_Vact[11:8]		The active line count of a field [11:8]
				Vid_Vtotal[11:8]		The total line count of a field [11:8]
0x61	Vid_Vact_L	RO		Vid_Vact[7:0]		The active line count of a field [7:0]
0x62	Vid_Vsync2DE	RO		Video sync to DE[7:0]		The width of vsync back porch
0x63	Vid_V_Ft_Porch	RO	7:0	Vid_V_Ft_Porch[7:0]		The width of vsync front porch
0x64	Vid_pixel_CNT	RO	7:0			Count of crystal clock on each 128 pixels
0x65	Vid_input_st	RO				Video input status
			7:4	Pix_rep		0000 : no repetition
				_		0001: pixel sent 2 times
						0011: pixel sent 4 times
			3	HDCP_DISABLE		HDCP Disable:
				_		1: HDCP Disabled
						0: HDCP no activated or enabled
	1	1			l	

			Τ.	Τ.		14 7773 67 1
			2	Avmute		1: HDMI is in Avmute state
			1	Vsync_in_po		Vsync input polarity
						0: Negative Polarity
						1: Positive Polarity
			0	Hsync_in_po		Hsync input polarity
						0: Negative Polarity
						1: Positive Polarity
68	PLL_Ctrl	W/R	7	RXPLL_ENI1	0x04	SelPXCK:
			6	RXPLL_ENI0B		0: Default select locked clock to core
			5	RXPLL_ER1		1: select unlocked clock
			4	RXPLL_ENFC		
			3	RXPLL_DEI		
			2	RXPLL_GAIN		
			1	RXPLL_EC1		
			0	RXPLL_ER0		
6B	CCtrl	W/R	7:6	DATA_RXAMP	0x10	EnCCTRL_REF: default disable manually
				CLK_RXAMP		set CCTRL
				CCTRL_SEL		
			0	ENCCTRL_REF		
6C	Equal_Ctrl2	W/R		VCMSEL	0x03	
	24441_0412	,,,,,	5	VSETRH	0.102	
			4	VSETRL		
				EQ_ZR		
0x73	HDCP_Ctrl	W/R	7	Enable repeater	0x20	Enable repeater function
OX13	IIDCI_Cui	VV/IX	6	KSV ready	UAZU	Set KSV ready when CAT6023 is reapeter
			5	Enable feature 1.1		Enable HDCP 1.1 feature
			4	enable fast authentication		Enable fast authetication
0x75	I2S_Ctrl	W/R	7	Ws_sel	0	1:invert channel A and channel B select
0.7.7	125_CIII	W/IX		I2S_Width		I2S word length, only effective in right
			0:2	12S_WIGHT	0	justified mode;
					U	Maximum value is 24 means of 24 bits,
			1.0	TOC M. I.	00	value is the length of word length
			1:0	I2S_Mode	00	I2S output mode:
						00:32 bit I2S left justified mode, 1T delay
						01:32 bit I2S right justified mode
						10:32 bit I2S left justified mode, 0T delay
0.56	TOG 16	****		100 CI 00 I		11:undefined
0x76	I2S_Map	W/R	7:6	I2S_Ch3Sel		I2S channel 6 and channel 7 map:
						00: map to HDMI channel 0 and channel 1
					11	01: map to HDMI channel 2 and channel 3
						10: map to HDMI channel 4 and channel 5
						11: map to HDMI channel 6 and channel 7
			5:4	I2S_Ch2Sel		I2S channel 4 and channel 5 map:
						00: map to HDMI channel 0 and channel 1
					10	01: map to HDMI channel 2 and channel 3
						10: map to HDMI channel 4 and channel 5
						11: map to HDMI channel 6 and channel 7
			3:2	I2S_Ch1Sel		I2S channel 2 and channel 3 map:
	_	1				00: map to HDMI channel 0 and channel 1
					104	
1					01	01: map to HDMI channel 2 and channel 3
					01	10: map to HDMI channel 4 and channel 5
					01	10: map to HDMI channel 4 and channel 5 11: map to HDMI channel 6 and channel 7
			1:0	I2S_Ch0Sel	01	10: map to HDMI channel 4 and channel 5
			1:0	I2S_Ch0Sel	01	10: map to HDMI channel 4 and channel 5 11: map to HDMI channel 6 and channel 7
			1:0	I2S_Ch0Sel	00	10: map to HDMI channel 4 and channel 5 11: map to HDMI channel 6 and channel 7 I2S channel 0 and channel 1 map:
			1:0	I2S_Ch0Sel		10: map to HDMI channel 4 and channel 5 11: map to HDMI channel 6 and channel 7 I2S channel 0 and channel 1 map: 00: map to HDMI channel 0 and channel 1
			1:0	I2S_Ch0Sel		10: map to HDMI channel 4 and channel 5 11: map to HDMI channel 6 and channel 7 I2S channel 0 and channel 1 map: 00: map to HDMI channel 0 and channel 1 01: map to HDMI channel 2 and channel 3
0x77	Audio_Ctrl	W/R	1:0	I2S_Ch0Sel Reg_Audck_BBen		10: map to HDMI channel 4 and channel 5 11: map to HDMI channel 6 and channel 7 I2S channel 0 and channel 1 map: 00: map to HDMI channel 0 and channel 1 01: map to HDMI channel 2 and channel 3 10: map to HDMI channel 4 and channel 5
0x77	Audio_Ctrl	W/R			00	10: map to HDMI channel 4 and channel 5 11: map to HDMI channel 6 and channel 7 I2S channel 0 and channel 1 map: 00: map to HDMI channel 0 and channel 1 01: map to HDMI channel 2 and channel 3 10: map to HDMI channel 4 and channel 5 11: map to HDMI channel 6 and channel 7

6 Force_FS 0 1: Force Andio FS mode		1	1			1_	T
Seserved				6	Force_FS	0	1: Force Audio FS mode
Aud_info_force							0: Audio FS from decode
3 Avmute_value				5	Reserved	1	
Armute value when software Armute is enabled 2 Force_avmute 0 1. Software forced-Avmute mode 1. Dis_vdo_mute 0 1. Disable Video mute 0. Dis_aud_mute 0. Disable Video mute 0. Dis_aud_mute 0. Disable Video mute 0				4	Aud info force	0	Force Audio setting from Aud info frame
Comparison							8
Comparison				3	Aymute value	0	Aymute value when software Aymute is
2					TVIIIuce_varae		
1 Dis_volo_mute 0 1: Disable Video mute 0 Dis_and_mute 0 1: Disable Audio mute 0 Dis_and_mute 0 1: Disable Audio mute 1: Disable Audio mute 0 Dis_and_mute 0 1: Disable Audio mute 0 Dis_and_mute Dis_and_mute Dis_and_mute Dis_and_mute Dis_and_mute Dis_and_mute Dis_and_mute Dis_and_or Fire Audio Fi				2	Force avmute	0	
0 Dis_aud_mute 0 1: Disable Audio mute 1: Disable Audio PLL reference 0: Disable PLL reference							
0x78 MCLK_Ctrl W/R 7 OSC_En							
	0.70	MCLV Cul	XV/D				
	0x / 8	MCLK_Ctrl	W/K	/	OSC_En	1	
A Force_CTS							
A Force_CTS O Software force to set CTS value 3 Force_CTSMODE O use CTS for audio FIFO adjustment Mclk output clock multiple number 000:128FS_001;256FS; 001 00:334FS_011:512FS; 100:640FS_101:768FS; 110:894FS_111:1024FS; 100:640FS_101:768FS; 110:894FS_111:1024FS; 110:894FS_111:1024FS; 100:640FS_110:768FS; 110:894FS_111:1024FS; 110:894FS_111:1024FS; 110:894FS_111:1024FS; 110:894FS_111:1024FS; 001:32 KHz_1 100:088.2KHz; 001:32 KHz_1 100:888.2KHz; 001:32 KHz_1 100:888.2KHz; 101:92KHz available only reg/77[6] = '1' 110:92KHz available only reg/77[6] = '1' Audio CTS parameter decoder value [15:8] Audio N parameter decoder value [15:8] Audio N parameter decoder value [15:8] Audio CTS parameter decoder value [16:8] 110:92KHz 1					0000	1	
3 Force_CTSMODE 0 use CTS for audio FIFQ adjustment Mclk outpit clock multiple number 000:128FS; 001:256FS; 010:256FS; 0							
Mclk output clock multiple number 000:128FS, 201,256FS; 101:312FS; 100:48FS; 101:312FS; 100:460FS; 101:768FS; 100:460FS; 101:768FS; 110:894FS; 111:1024FS; 100:48KHz; 100:44.1KHz; 100:44.1KHz; 100:44.1KHz; 100:44.1KHz; 100:176.4KHz; 110:192KHz available only reg77[6] = '1' 200:48KHz; 200:44.1KHz; 200:44.1KH							
2.0 Mclksel 001 000:128FS 001:256FS; 010:384FS 011:512FS; 100:640FS 101:768FS; 110:894FS 111:1024FS; 110:954FKI; 100:96 KHz; 100:176.4KHz; 110:192KHz 110:192KHz 110:192KHz 110:192KHz 110:192KHz 110:192KHz 110:192KHz 110:192KHz 110:192FS 11:192FS 11:				3	Force_CTSMODE	0	
2:0 Mclksel							
0x7E							
No. No.				2:0	Mclksel	001	
Ox7E							
FS_SET							
0000:44.1KHz; 0010:48KHz; 0011:32 KHz; 100:176.4KHz; 1010:176.4KHz; 1010:176.4KHz; 1010:176.4KHz; 1110:192KHz available only reg77[6] = '1'	0x7E						
0011:32 KHz; 1000:88.2KHz; 1010:96 KHz; 110:176.4KHz; 1110:192KHz available only reg77[6] = '1'		FS_SET	W/R	3:0	FS_SET	0010	
1010:96 KHz; 1100:176.4KHz; 1110:192KHz available only reg77[6] = '1'							0000:44.1KHz; 0010:48KHz;
1110:192KHz available only reg77[6] = '1'							0011:32 KHz; 1000:88.2KHz;
available only reg77[6] = '1'							1010:96 KHz; 1100:176.4KHz;
0x7F N_Rev1 RO 7:0 N_DEC[7:0] Audio N parameter decoder value [7:0] 0x80 N_Rev2 RO 7:0 N_DEC[15:8] Audio N parameter decoder value [15:8] 0x81 N_Rev3 RO 7:4 CTS_DEC[3:0] Audio N parameter decoder value [19:0] 0x82 CTS_Rev2 RO 7:0 CTS_DEC[11:4] Audio CTS parameter decoder value [11:4] 0x83 CTS_Rev3 RO 7:0 CTS_DEC[19:12] Audio CTS parameter decoder value [11:4] 0x84 CD RO 7:4 GCP_CD Color depth decoder value in GCP 0: default (24bits) 6 24bits 5:30bits 5:30bits 5:30bits 6:36bits 7:4 48bits 4:24bits 4:24bits 5:30bits 6:36bits 7:4 48bits 4:24bits 6:36bits 7:4 48bits 4:24bits 4:24bits							1110:192KHz
0x7F N_Rev1 RO 7:0 N_DEC[7:0] Audio N parameter decoder value [7:0] 0x80 N_Rev2 RO 7:0 N_DEC[15:8] Audio N parameter decoder value [15:8] 0x81 N_Rev3 RO 7:4 CTS_DEC[3:0] Audio N parameter decoder value [19:0] 0x82 CTS_Rev2 RO 7:0 CTS_DEC[11:4] Audio CTS parameter decoder value [11:4] 0x83 CTS_Rev3 RO 7:0 CTS_DEC[19:12] Audio CTS parameter decoder value [11:4] 0x84 CD RO 7:4 GCP_CD Color depth decoder value in GCP 0: default (24bits) 6 24bits 5:30bits 5:30bits 5:30bits 6:36bits 7:4 48bits 4:24bits 4:24bits 5:30bits 6:36bits 7:4 48bits 4:24bits 6:36bits 7:4 48bits 4:24bits 4:24bits							available only reg77[6] = '1'
0x80 N_Rcv2 RO 7:0 N_DEC[15:8] Audio N parameter decoder value [15:8] 0x81 N_Rcv3 RO 7:4 CTS_DEC[3:0] Audio CTS parameter decoder value [19:0] 0x82 CTS_Rcv2 RO 7:0 CTS_DEC[11:4] Audio CTS parameter decoder value [11:4] 0x83 CTS_Rcv3 RO 7:0 CTS_DEC[19:12] Audio CTS parameter decoder value [11:4] 0x84 CD RO 7:4 GCP_CD Color depth decoder value in GCP 0: default (24bits) 6 3:0 F_DEC Audio FS(sample Freq.) decoder value 0000:44.1KHz; 0010:48KHz; 0011:48KHz; 0011:48KHz; 1010:96 KHz; 1100:176.4KHz; 1110:196 KHz; 110:176.4KHz; 1110:192 KHz 0x85 Channel_Err RO 7 Pkt_2berr 2-bit BCH error is detected and automatically corrected a decode error is detected on channel 2 a decode error is detected on channel 1 a decode error is detected on channel 0 0x87 HWMute_Ctrl W/R 6 HWForceMute 0 HWForceMute: 0: mute control by channel status 1: mute anyway 5 HWAudFFMuteClr 0 1: FIFO mut	0x7F	N_Rcv1	RO	7:0	N_DEC[7:0]		Audio N parameter decoder value [7:0]
3:0 N_DEC[19:16] Audio N parameter decoder value [19:6] 0x82 CTS_Rcv2	0x80	N_Rcv2	RO	7:0	N_DEC[15:8]		Audio N parameter decoder value [15:8]
3:0 N_DEC[19:16] Audio N parameter decoder value [19:6] 0x82 CTS_Rcv2			RO				
0x82 CTS_Rev2 RO 7:0 CTS_DEC[11:4] Audio CTS parameter decoder value [11:4] 0x83 CTS_Rev3 RO 7:0 CTS_DEC[19:12] Audio CTS parameter decoder value [19:12] 0x84 CD RO 7:4 GCP_CD Color depth decoder value in GCP 0: default (24bits) 4: 24bits 5: 30bits 6: 36bits 7: 48bits FS RO 3:0 F_DEC Audio FS(sample Freq.) decoder value 0000:44.1KHz; 0010:48KHz; 0011:32 KHz; 1100:176.4KHz; 1110:192KHz 0x85 Channel_Err RO 7 Pkt_2berr 2-bit BCH error is detected and packet is discarded a 1-bit BCH error is detected and automatically corrected a decode error is detected on channel 2 a decode error is detected on channel 1 a decode error is detected on channel 1 a decode error is detected on channel 0 0x87 HWMute_Ctrl W/R 6 HWForceMute 0 HWForceMute: 0: mute control by channel status 1: mute anyway 1: FIFO mute clear		_					
Ox84 CD	0x82	CTS Rcv2	RO				
The content of the							
CD	0.100	015_10.0	110				
O: default (24bits) 4: 24bits 5: 30bits 6: 36bits 7: 48bits 7: 48b	0x84	CD	RO	7.4	GCP CD		
4: 24bits 5: 30bits 6: 36bits 7: 48bits FS RO 3:0 F_DEC Audio FS(sample Freq.) decoder value 0000:44.1KHz; 0010:48KHz; 0011:32 KHz; 1000:88.2KHz; 1010:96 KHz; 1100:176.4KHz; 1110:192KHz 0x85 Channel_Err RO 7 Pkt_2berr 2-bit BCH error is detected and packet is discarded a 1-bit BCH error is detected and automatically corrected 5:4 CH2_Err 3:2 CH1_Err 1:0 CH0_Err 1:0 CH0_Err 0x87 HWMute_Ctrl W/R 6 HWForceMute 0 HWForceMute: 0: mute control by channel status 1: mute anyway 1: FIFO mute clear	ONO I	CD	110	1.	Ger_GD		
S: 30bits 6: 36bits 7: 48bits Audio FS(sample Freq.) decoder value 0000:44.1KHz; 0010:48KHz; 0011:32 KHz; 1000:88.2KHz; 1010:96 KHz; 1100:176.4KHz; 1110:192KHz 2-bit BCH error is detected and packet is discarded a 1-bit BCH error is detected and automatically corrected a decode error is detected on channel 2 a decode error is detected on channel 1 1:0 CH0_Err a decode error is detected on channel 0 0x87 HWMute_Ctrl W/R 6 HWForceMute 0 HWForceMute: 0: mute control by channel status 1: mute anyway 5 HWAudFFMuteClr 0 1: FIFO mute clear							` ′
FS RO 3:0 F_DEC Audio FS(sample Freq.) decoder value 0000:44.1KHz; 0010:48KHz; 0011:32 KHz; 1000:88.2KHz; 1010:96 KHz; 1100:176.4KHz; 1110:192KHz Ox85 Channel_Err RO 7 Pkt_2berr 2-bit BCH error is detected and packet is discarded a 1-bit BCH error is detected and automatically corrected a decode error is detected on channel 2 a decode error is detected on channel 1 1:0 CH0_Err a decode error is detected on channel 0 Ox87 HWMute_Ctrl W/R 6 HWForceMute 0 HWForceMute: 0: mute control by channel status 1: mute anyway 5 HWAudFFMuteClr 0 1: FIFO mute clear							
FS RO 3:0 F_DEC Audio FS(sample Freq.) decoder value 0000:44.1KHz; 0010:48KHz; 0011:32 KHz; 1000:88.2KHz; 1010:96 KHz; 1100:176.4KHz; 1110:192KHz Ox85 Channel_Err RO 7 Pkt_2berr 6 Pkt_1berr 2-bit BCH error is detected and packet is discarded a 1-bit BCH error is detected and automatically corrected a decode error is detected on channel 2 a decode error is detected on channel 1 1:0 CH0_Err a decode error is detected on channel 0 Ox87 HWMute_Ctrl W/R 6 HWForceMute 0 HWForceMute: 0: mute control by channel status 1: mute anyway 5 HWAudFFMuteClr 0 1: FIFO mute clear							
FS RO 3:0 F_DEC Audio FS(sample Freq.) decoder value 0000:44.1KHz; 0010:48KHz; 0011:32 KHz; 1000:88.2KHz; 1010:96 KHz; 1100:176.4KHz; 1110:192KHz Ox85 Channel_Err RO 7 Pkt_2berr 2-bit BCH error is detected and packet is discarded a 1-bit BCH error is detected and automatically corrected a decode error is detected on channel 2 a decode error is detected on channel 1 a decode error is detected on channel 1 a decode error is detected on channel 0 Ox87 HWMute_Ctrl W/R 6 HWForceMute 0 HWForceMute: 0: mute control by channel status 1: mute anyway 1: FIFO mute clear							
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1010:96 KHz; 1100:176.4KHz; 1110:192KHz							
1110:192KHz 1110:192KHz 2-bit BCH error is detected and packet is discarded 2 -bit BCH error is detected and packet is discarded 3 1-bit BCH error is detected and automatically corrected 3 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected on channel 2 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected and automatically corrected 4 -bit BCH error is detected on channel 4							
Ox85 Channel_Err RO 7 Pkt_2berr 6 Pkt_1berr 6 Pkt_1berr 5:4 CH2_Err 3:2 CH1_Err 1:0 CH0_Err Ox87 HWMute_Ctrl W/R 6 HWForceMute 7 Pkt_2berr 2-bit BCH error is detected and packet is discarded a 1-bit BCH error is detected and automatically corrected a decode error is detected on channel 2 a decode error is detected on channel 1 a decode error is detected on channel 0 HWForceMute: 0: mute control by channel status 1: mute anyway 5 HWAudFFMuteClr 0 1: FIFO mute clear			•				
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6 Pkt_1berr a 1-bit BCH error is detected and automatically corrected a decode error is detected on channel 2 a decode error is detected on channel 1 a decode error is detected on channel 1 a decode error is detected on channel 0 Ox87 HWMute_Ctrl W/R 6 HWForceMute 0 HWForceMute: 0: mute control by channel status 1: mute anyway 5 HWAudFFMuteClr 0 1: FIFO mute clear	UX83	Channel_Err	KU	/	PKI_2DEIT		
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3:2 CH1_Err a decode error is detected on channel 1 a decode error is detected on channel 0 0x87 HWMute_Ctrl W/R 6 HWForceMute 0 HWForceMute: 0: mute control by channel status 1: mute anyway 5 HWAudFFMuteClr 0 1: FIFO mute clear				E . 4	CH2 F		
1:0 CH0_Err a decode error is detected on channel 0							
0x87 HWMute_Ctrl W/R 6 HWForceMute 0 HWForceMute: 0: mute control by channel status 1: mute anyway 5 HWAudFFMuteClr 0 1: FIFO mute clear							
0: mute control by channel status 1: mute anyway 5 HWAudFFMuteClr 0 1: FIFO mute clear	0.07	INVIDA - C. 1	XX / / / /			0	
5 HWAudFFMuteClr 1: mute anyway 1: FIFO mute clear	0x87	HW Mute_Ctrl	W/R	6	HWForceMute	U	
5 HWAudFFMuteClr 0 1: FIFO mute clear							
				l _			
4 HWMuteClr 0 1: Clear H/W mute						0	
		ĺ	1	1 /	IHWMuteClr	1()	11. Clear H/W mute
3 HWMuteEn 1 1: H/W Mute enable							

6	1': Video output Auto Mute Disable 1': tristate video Data output buffer 1': tristate video Control output buffer 1': tristate Audio SPDIF output buffer 1': tristate Audio I2S3 output buffer 1': tristate Audio I2S2 output buffer 1': tristate Audio I2S1 output buffer 1': tristate Audio I2S0 output buffer 1': tristate Audio I2S0 output buffer 1': tristate Audio I2S0 output buffer 1': Audio I2
6 Tri_VDIO 11 12 13 14 15 15 15 16 15 16 16 16	1': tristate video Data output buffer 1': tristate video Control output buffer 1': tristate Audio SPDIF output buffer 1': tristate Audio I2S3 output buffer 1': tristate Audio I2S2 output buffer 1': tristate Audio I2S1 output buffer 1': tristate Audio I2S0 output buffer 1': tristate Audio I2S0 output buffer 1': tristate Audio I2S0 output buffer 1': Audio received status 1': Audio is ON 1': Audio is ON 1': Audio type is High Bit rate 1': Audio type is DSD 1': Audio layout is 1 or 0 1': HDMI Audio source 3 valid Flag 1': HDMI Audio source 2 valid Flag 1': HDMI Audio source 1 valid Flag 1': HDMI Audio source 0 valid Flag 1': Rx clock change detect Int 1': Rx clock on detect Int 1': CDR symbol error detect Int 1': CDR symbol error detect Int 1': Genaral packet detect Int 1': ISRC2 packet detect Int 1': ISRC1 packet detect Int Mask of interrupts defined in reg0x8B 1: The Interrupt is effective
S Tri_VIO 1 1 1 1 1 1 1 1 1	1': tristate video Control output buffer 1': tristate Audio SPDIF output buffer 1': tristate Audio I2S3 output buffer 1': tristate Audio I2S2 output buffer 1': tristate Audio I2S1 output buffer 1': tristate Audio I2S0 output buffer 1': tristate Audio I2S0 output buffer 1': tristate Audio I2S0 output buffer 1': Audio received status 1': Audio is ON 1': Audio type is High Bit rate 1': Audio type is DSD 1': Audio layout is 1 or 0 1': HDMI Audio source 3 valid Flag 1': HDMI Audio source 2 valid Flag 1': HDMI Audio source 1 valid Flag 1': HDMI Audio source 0 valid Flag 1': Rx clock change detect Int 1': Rx clock on detect Int 1': CDR symbol error detect Int 1': CDR symbol error detect Int 1': Genaral packet detect Int 1': ISRC2 packet detect Int 1': ISRC1 packet detect Int Mask of interrupts defined in reg0x8B 1: The Interrupt is effective
4 Tri_SPDIF '1	1': tristate Audio SPDIF output buffer 1': tristate Audio I2S3 output buffer 1': tristate Audio I2S2 output buffer 1': tristate Audio I2S1 output buffer 1': tristate Audio I2S0 output buffer 1': tristate Audio I2S0 output buffer 1': Audio received status 1': Audio is ON 1': Audio type is High Bit rate 1': Audio type is DSD 1': Audio layout is 1 or 0 1': HDMI Audio source 3 valid Flag 1': HDMI Audio source 2 valid Flag 1': HDMI Audio source 1 valid Flag 1': HDMI Audio source 0 valid Flag 1': Rx clock change detect Int 1': Rx clock on detect Int 1': CDR symbol error detect Int 1': CDR symbol error detect Int 1': Genaral packet detect Int 1': ISRC2 packet detect Int 1': ISRC1 packet detect Int Mask of interrupts defined in reg0x8B 1: The Interrupt is effective
3 Tri_12S3 '1 2 Tri_12S2 '1 3 Tri_12S2 '1 4 Tri_12S1 '1 5 Tri_12S0 '1 6 Tri_12S0 '1 7 Audio_on '1 8 Audio_chanSt RO Audio_on '1 9 Audio_layout '1 1 Audio_src3_valid '1 2 Audio_src2_valid '1 3 Audio_src2_valid '1 4 Audio_src1_valid '1 5 Audio_src0_valid '1 6 Xckon_Det '1 5 HDCPoff_det '1 4 Symerr_det '1 5 Genpkt_det '1 1 ISRC2_Det '1 0 Ox8C Int_mask3 W/R M Ox8E Pkt_type_H RO 7:4 Pkt_type_H R Ori_sampF RO Ori_sampF Ori	1': tristate Audio I2S3 output buffer 1': tristate Audio I2S2 output buffer 1': tristate Audio I2S1 output buffer 1': tristate Audio I2S0 output buffer 1': tristate Audio I2S0 output buffer 1': Audio received status 1': Audio is ON 1': Audio type is High Bit rate 1': Audio type is DSD 1': Audio layout is 1 or 0 1': HDMI Audio source 3 valid Flag 1': HDMI Audio source 2 valid Flag 1': HDMI Audio source 1 valid Flag 1': HDMI Audio source 0 valid Flag 1': Rx clock change detect Int 1': Rx clock on detect Int 1': CDR symbol error detect Int 1': CDR symbol error detect Int 1': Genaral packet detect Int 1': ISRC2 packet detect Int 1': ISRC1 packet detect Int Mask of interrupts defined in reg0x8B 1: The Interrupt is effective
2 Tri_I2S2 '1 Tri_I2S1 '1	1': tristate Audio I2S2 output buffer 1': tristate Audio I2S1 output buffer 1': tristate Audio I2S0 output buffer Audio received status 1': Audio is ON 1': Audio type is High Bit rate 1': Audio type is DSD 1': Audio layout is 1 or 0 1': HDMI Audio source 3 valid Flag 1': HDMI Audio source 2 valid Flag 1': HDMI Audio source 1 valid Flag 1': HDMI Audio source 0 valid Flag 1': Rx clock change detect Int 1': Rx clock on detect Int 1': Rx clock on detect Int 1': CDR symbol error detect Int 1': Color Depth change Int 1': ISRC2 packet detect Int 1': ISRC2 packet detect Int 1': ISRC1 packet detect Int Mask of interrupts defined in reg0x8B 1: The Interrupt is effective
1 Tri_I2S1 '1 '1 '1 '1	1': tristate Audio I2S1 output buffer 1': tristate Audio I2S0 output buffer Audio received status 1': Audio is ON 1': Audio type is High Bit rate 1': Audio type is DSD 1': Audio layout is 1 or 0 1': HDMI Audio source 3 valid Flag 1': HDMI Audio source 2 valid Flag 1': HDMI Audio source 1 valid Flag 1': HDMI Audio source 0 valid Flag 1': Rx clock change detect Int 1': Rx clock on detect Int 1': CDR symbol error detect Int 1': CDR symbol error detect Int 1': Genaral packet detect Int 1': ISRC2 packet detect Int 1': ISRC1 packet detect Int Mask of interrupts defined in reg0x8B 1: The Interrupt is effective
0 Tri_I2SO	1': tristate Audio I2S0 output buffer Audio received status 1': Audio is ON 1': Audio type is High Bit rate 1': Audio type is DSD 1': Audio layout is 1 or 0 1': HDMI Audio source 3 valid Flag 1': HDMI Audio source 2 valid Flag 1': HDMI Audio source 1 valid Flag 1': HDMI Audio source 0 valid Flag 1': Rx clock change detect Int 1': Rx clock on detect Int 1': Rx clock on detect Int 1': CDR symbol error detect Int 1': CDR symbol error detect Int 1': Genaral packet detect Int 1': ISRC2 packet detect Int 1': ISRC1 packet detect Int Mask of interrupts defined in reg0x8B 1: The Interrupt is effective
0x8A Audio_chanSt RO 7 Audio_on '1 <td>Audio received status 1': Audio is ON 1': Audio type is High Bit rate 1': Audio type is DSD 1': Audio layout is 1 or 0 1': HDMI Audio source 3 valid Flag 1': HDMI Audio source 2 valid Flag 1': HDMI Audio source 1 valid Flag 1': HDMI Audio source 0 valid Flag 1': Rx clock change detect Int 1': Rx clock on detect Int 1': CDR symbol error detect Int 1': CODR symbol error detect Int 1': Genaral packet detect Int 1': ISRC2 packet detect Int 1': ISRC1 packet detect Int Mask of interrupts defined in reg0x8B 1: The Interrupt is effective</td>	Audio received status 1': Audio is ON 1': Audio type is High Bit rate 1': Audio type is DSD 1': Audio layout is 1 or 0 1': HDMI Audio source 3 valid Flag 1': HDMI Audio source 2 valid Flag 1': HDMI Audio source 1 valid Flag 1': HDMI Audio source 0 valid Flag 1': Rx clock change detect Int 1': Rx clock on detect Int 1': CDR symbol error detect Int 1': CODR symbol error detect Int 1': Genaral packet detect Int 1': ISRC2 packet detect Int 1': ISRC1 packet detect Int Mask of interrupts defined in reg0x8B 1: The Interrupt is effective
0x8A Audio_chanSt RO 7 Audio_on '1 <td>Audio received status 1': Audio is ON 1': Audio type is High Bit rate 1': Audio type is DSD 1': Audio layout is 1 or 0 1': HDMI Audio source 3 valid Flag 1': HDMI Audio source 2 valid Flag 1': HDMI Audio source 1 valid Flag 1': HDMI Audio source 0 valid Flag 1': Rx clock change detect Int 1': Rx clock on detect Int 1': CDR symbol error detect Int 1': CODR symbol error detect Int 1': Genaral packet detect Int 1': ISRC2 packet detect Int 1': ISRC1 packet detect Int Mask of interrupts defined in reg0x8B 1: The Interrupt is effective</td>	Audio received status 1': Audio is ON 1': Audio type is High Bit rate 1': Audio type is DSD 1': Audio layout is 1 or 0 1': HDMI Audio source 3 valid Flag 1': HDMI Audio source 2 valid Flag 1': HDMI Audio source 1 valid Flag 1': HDMI Audio source 0 valid Flag 1': Rx clock change detect Int 1': Rx clock on detect Int 1': CDR symbol error detect Int 1': CODR symbol error detect Int 1': Genaral packet detect Int 1': ISRC2 packet detect Int 1': ISRC1 packet detect Int Mask of interrupts defined in reg0x8B 1: The Interrupt is effective
7 Audio_on	1': Audio is ON 1': Audio type is High Bit rate 1': Audio type is DSD 1': Audio type is DSD 1': Audio layout is 1 or 0 1': HDMI Audio source 3 valid Flag 1': HDMI Audio source 2 valid Flag 1': HDMI Audio source 1 valid Flag 1': RX clock change detect Int 1': Rx clock on detect Int 1': CDR symbol error detect Int 1': Color Depth change Int 1': Genaral packet detect Int 1': ISRC2 packet detect Int 1': ISRC1 packet detect Int Mask of interrupts defined in reg0x8B 1: The Interrupt is effective
6 HBRAudio '1 5 DSDAudio '1 4 Audio_layout '1 3 Audio_src3_valid '1 2 Audio_src2_valid '1 4 Audio_src1_valid '1 5 Ox8B Interrupt3 RO 7 CLKCHG_DET '1 6 Txckon_Det '1 7 Txckon_Det '1 8 Txckon_Det '1 9 Txckon_Det '1 1 Txckon_Det '1 2 Genpkt_det '1 3 CD_det '1 4 Symerr_det '1 5 HDCPoff_det '1 6 Txckon_Det '1 7 Txckon_Det '1 8 Txckon_Det '1 9 Txckon_Det '1 1 Txckon_Det '1 2 Txckon_Det '1 3 Txckon_Det '1 4 Txckon_Det '1 5 Txckon_Det '1 6 Txckon_Det '1 7 Txckon_Det '1 9 Txckon	1': Audio type is High Bit rate 1': Audio type is DSD 1': Audio layout is 1 or 0 1': HDMI Audio source 3 valid Flag 1': HDMI Audio source 2 valid Flag 1': HDMI Audio source 1 valid Flag 1': HDMI Audio source 0 valid Flag 1': Rx clock change detect Int 1': Rx clock on detect Int 1': Rx clock on detect Int 1': CDR symbol error detect Int 1': Color Depth change Int 1': Genaral packet detect Int 1': ISRC2 packet detect Int 1': ISRC1 packet detect Int Mask of interrupts defined in reg0x8B 1: The Interrupt is effective
5 DSDAudio '1 '1 '1 '1 '1 '1 '1 '	1': Audio type is DSD 1': Audio layout is 1 or 0 1': HDMI Audio source 3 valid Flag 1': HDMI Audio source 2 valid Flag 1': HDMI Audio source 1 valid Flag 1': HDMI Audio source 0 valid Flag 1': Rx clock change detect Int 1': Rx clock on detect Int 1': CDR symbol error detect Int 1': Color Depth change Int 1': Genaral packet detect Int 1': ISRC2 packet detect Int 1': ISRC1 packet detect Int 1': ISRC1 packet defined in reg0x8B 1: The Interrupt is effective
4 Audio_layout '1 3 Audio_src3_valid '1 2 Audio_src2_valid '1 Audio_src1_valid '1 Audio_src0_valid '1 Audio_src0_valid '1 Ox8B Interrupt3 RO 7 CLKCHG_DET '1 CLKCHG_DE	1': Audio layout is 1 or 0 1': HDMI Audio source 3 valid Flag 1': HDMI Audio source 2 valid Flag 1': HDMI Audio source 1 valid Flag 1': HDMI Audio source 0 valid Flag 1': Rx clock change detect Int 1': Rx clock on detect Int 1': CDR symbol error detect Int 1': Color Depth change Int 1': Genaral packet detect Int 1': ISRC2 packet detect Int 1': ISRC1 packet detect Int Mask of interrupts defined in reg0x8B 1: The Interrupt is effective
3 Audio_src3_valid '1 2 Audio_src2_valid '1 3 Audio_src2_valid '1 4 Audio_src1_valid '1 5 CLKCHG_DET '1 6 rxckon_Det '1 7 CLKCHG_DET '1 8 For excession of the properties of the propertie	1': HDMI Audio source 3 valid Flag 1': HDMI Audio source 2 valid Flag 1': HDMI Audio source 1 valid Flag 1': HDMI Audio source 0 valid Flag 1': Rx clock change detect Int 1': Rx clock on detect Int 1': HDCP off detect Int 1': CDR symbol error detect Int 1': Color Depth change Int 1': Genaral packet detect Int 1': ISRC2 packet detect Int 1': ISRC1 packet detect Int 1': ISRC1 packet detect Int 1': The Interrupt is effective
2 Audio_src2_valid '1 Audio_src1_valid '1 Audio_src0_valid '1 Ox8B Interrupt3 RO 7 CLKCHG_DET '1 CLKCHG_DET	1': HDMI Audio source 2 valid Flag 1': HDMI Audio source 1 valid Flag 1': HDMI Audio source 0 valid Flag 1': Rx clock change detect Int 1': Rx clock on detect Int 1': HDCP off detect Int 1': CDR symbol error detect Int 1': Color Depth change Int 1': Genaral packet detect Int 1': ISRC2 packet detect Int 1': ISRC1 packet detect Int 1': ISRC1 packet detect Int 1': The Interrupt is effective
1 Audio_src1_valid '1	1': HDMI Audio source 1 valid Flag 1': HDMI Audio source 0 valid Flag 1': Rx clock change detect Int 1': Rx clock on detect Int 1': HDCP off detect Int 1': CDR symbol error detect Int 1': Color Depth change Int 1': Genaral packet detect Int 1': ISRC2 packet detect Int 1': ISRC1 packet detect Int Mask of interrupts defined in reg0x8B 1: The Interrupt is effective
0 Audio_src0_valid '1	1': HDMI Audio source 0 valid Flag 1': Rx clock change detect Int 1': Rx clock on detect Int 1': HDCP off detect Int 1': CDR symbol error detect Int 1': Color Depth change Int 1': Genaral packet detect Int 1': ISRC2 packet detect Int 1': ISRC1 packet detect Int Mask of interrupts defined in reg0x8B 1: The Interrupt is effective
0x8B Interrupt3 RO 7 CLKCHG_DET '1 6 rxckon_Det '1 5 HDCPoff_det '1 4 Symerr_det '1 3 CD_det '1 2 Genpkt_det '1 1 ISRC2_Det '1 0x8C Int_mask3 W/R 0x8E Pkt_type_H RO Ori_sampF 3:0 Ori_sampF O	1': Rx clock change detect Int 1': Rx clock on detect Int 1': HDCP off detect Int 1': CDR symbol error detect Int 1': Color Depth change Int 1': Genaral packet detect Int 1': ISRC2 packet detect Int 1': ISRC1 packet detect Int Mask of interrupts defined in reg0x8B 1: The Interrupt is effective
6 rxckon_Det '1 '1 '1 '1 '1 '1 '1 '	1': Rx clock on detect Int 1': HDCP off detect Int 1': CDR symbol error detect Int 1': Color Depth change Int 1': Genaral packet detect Int 1': ISRC2 packet detect Int 1': ISRC1 packet detect Int Mask of interrupts defined in reg0x8B 1: The Interrupt is effective
5 HDCPoff_det '1 '1 '1 '1 '1 '1 '1 '	1': HDCP off detect Int 1': CDR symbol error detect Int 1': Color Depth change Int 1': Genaral packet detect Int 1': ISRC2 packet detect Int 1': ISRC1 packet detect Int Mask of interrupts defined in reg0x8B 1: The Interrupt is effective
4 Symerr_det 3 CD_det 1 1 1 1 1 1 1 1 1	1': CDR symbol error detect Int 1': Color Depth change Int 1': Genaral packet detect Int 1': ISRC2 packet detect Int 1': ISRC1 packet detect Int Mask of interrupts defined in reg0x8B 1: The Interrupt is effective
3 CD_det '1 2 Genpkt_det '1 ISRC2_Det '1 Ox8C Int_mask3 W/R M M Ox8E Pkt_type_H RO 7:4 Pkt_type_H RO Ori_sampF O Ori_sampF Ori_sampF	1': Color Depth change Int 1': Genaral packet detect Int 1': ISRC2 packet detect Int 1': ISRC1 packet detect Int Mask of interrupts defined in reg0x8B 1: The Interrupt is effective
3 CD_det '1 2 Genpkt_det '1 1 ISRC2_Det '1 0 ISRC1_Det '1 0x8C Int_mask3 W/R M 0x8E Pkt_type_H RO 7:4 Pkt_type_H Ro Ori_sampF 3:0 Ori_sampF O	1': Color Depth change Int 1': Genaral packet detect Int 1': ISRC2 packet detect Int 1': ISRC1 packet detect Int Mask of interrupts defined in reg0x8B 1: The Interrupt is effective
0x8C Int_mask3 W/R Int_mask3 W/R M 0x8E Pkt_type_H RO 7:4 Pkt_type_H RO 0ri_sampF 3:0 Ori_sampF O	1': Genaral packet detect Int 1': ISRC2 packet detect Int 1': ISRC1 packet detect Int Mask of interrupts defined in reg0x8B 1: The Interrupt is effective
0x8C Int_mask3 W/R M 0x8E Pkt_type_H RO 7:4 Pkt_type_H RO 0ri_sampF 3:0 Ori_sampF O	1': ISRC2 packet detect Int 1': ISRC1 packet detect Int Mask of interrupts defined in reg0x8B 1: The Interrupt is effective
0x8C Int_mask3 W/R M 0x8E Pkt_type_H RO 7:4 Pkt_type_H R 0ri_sampF 3:0 Ori_sampF O	1': ISRC1 packet detect Int Mask of interrupts defined in reg0x8B 1: The Interrupt is effective
0x8C Int_mask3 W/R M 0x8E Pkt_type_H RO 7:4 Pkt_type_H R Ori_sampF 3:0 Ori_sampF O	Mask of interrupts defined in reg0x8B 1: The Interrupt is effective
0x8E Pkt_type_H RO 7:4 Pkt_type_H R Ori_sampF 3:0 Ori_sampF O	1: The Interrupt is effective
Ori_sampF 3:0 Ori_sampF O	
Ori_sampF 3:0 Ori_sampF O	
Ori_sampF 3:0 Ori_sampF O	0: The Interrupt is ineffective
	Received packet type high bits
	Original sampling frequency
	111:44.1KHz; 1101:48KHz;
	100:32 KHz; 0111:88.2KHz;
	0101:96 KHz; 0011:176.4KHz;
	0001:192KHz
	f this byte is not 9 in normal operation,
	eading ROM failed.
	1': ROM data decode valid
	1': ROM data decode fail
	1': No ACK received when access ROM
	1': Acquire ROM data done
93 W/R 7:0 0x03 Fe	For revised loop this byte should be set to
)x43
	When '1' Vrctrl of the 1st EQ block is set to
	vdd.
	When '1' Vrctrl of the 1st EQ block is set to
	VSS.
	OR0 of the 1st EQ block.
4 REG_AFEDR0(moved from 0	
reg56(5))	7D 64 1 FOLL 1
	ZR of the 1st EQ block
	When using revised loop, this byte should
	pe set to 0x1f
7 rsvd	
6 SAME_ZR 1 1:	:ZR_1ST=ZR
5 EN_RCTRL 1 1:):ZR_1ST=REG_ZR_1ST

						0: R of the 1st EQ block depends on EN_RVD, EN_RVS (and on DER_1st)
			4	LOOP_MUX	0	When '0', use prior loop version(A1,T1) When '1' the revised loop is adopted
			3:0	DER_1st	0000	Registers to decrease the value of resister at the source node of amplifier in the clock
						channel.
95		W/R	7:0		0x8f	Suggest Default value: 0x87
			7	REG_FILTCKCHG	1	
				EQK_RLSBIN	0	Register of the LSB value when manually setting EQK_RIN
			5:0	EQK_RIN	00111 1	Registers to manually control dc gain of clock and data channels
96		W/R	5	REGPWD_COMP	1	power down the comparing circuit for DFIX mode comparing circuit of selected port works
			4	Reg_DFIX_CFIX	1	1: Fix C to Register value in DFIX mode
			3	EQK_DATASEL	0	'0':RDATA are the same as RCLK when RLSB='0' '1': possible codes of RDATA are limited to
						be 000000, 000011, 001101,010101, or 001111.
			2	REG_RSamp50K	0	When '0', Vrctrl sampling frequency is Fosc/2^8=100KHz When'1',the frequency is Fosc/2^9=50KHz
			1	EQK_AUTO_DIS	0	When'0', RCLK[5:0] are decided automatically. When'1',RCLK[5:0] are assigned
						manually.
			0	REG_DFIX	0	When '1', dc gain is controlled by
				REG_DI IX		reg_r[5:0] When '0' ,dc gain is controlled by loop
97	Reset Control	W/R	7	REG_PWDRXPLL2	0	when o , ac gain is controlled by loop
71	Reset Control	11710		REG RSTRXPLL2	0	
			5	REG_RSTRXPLL	0	
			4	REG ENHDCPOFF	0	
				REG_ENHDCPRST	0	
				REG_ENCKRST	0	
			1	REGEN_AutoVDORST	0	
	. <		0	REGEN_AutoAUDRST	0	
0x9B	Backup_Regs	W/R	7	Force Romscl		1:Select clock from register setting
	1-3					0:default.
			6	Forced Romscl value		1:clock set to 1. 0:clock set to 0.
			5	CLKRST_SEL		
			4	HDCP_NOAVMUTE		1: force HDCP avmute=0
9C	Audio_Ch_status0	RO	7:6	'00' – mode 0 for following byte.		Audio Channel status decoder value [7:0]
			5:3	Other – reserved. D[1] = 0 '000' – 2 channel without		
				pre-emphasis '001' – 2 channel with		
				50μs/15μs pre-emphasis. '010' – reserved '011' – reserved		
				D[1] = 1 '000' – Default state for other		

2 2 2 2 2 2 2 2 2 2							
2 0 - Software for copyright asserted. 1 - Software for no copyright is asserted. 1 - Audio word world represents linear PEM samples. 1 - Audio word world represents linear PEM samples. 1 - Audio word used for other purpose 0 0 0 0 0 0 0 0 0					application than linear PCM.		
				2			
1				-	1.0		
Copyright is asserted.							
1							
Part				١.			
Samples 1				1			
Part							
Other purpose					samples.		
D					1 – Audio word used for		
D					other purpose		
Section Sect				0			
Number	9D	Audio Ch status1	RO	_	-	0x00	Audio Channel status decoder value [15:8]
"0000" - Do not take into account.				7.1		OAOO	
account.)L	Audio_Cii_status2	KO	7.4			Audio Chainiei status decodei value [23.10]
"0001" - 1 "0010" - 2 "0011" - 3 "1111" - 15							
"0010" - 2 "0011" - 3							
"1111" - 15 3:0 Source Number 10001" - do not take into account 10001" - left channel for stereo format 10010 - right channel for stereo format							
Sample S					"0010" – 2		
3:0 Source Number					"0011" – 3		
3:0 Source Number							
3:0 Source Number					"1111" – 15		
				3.0			
Secont South Sou				3.0			
Second Communication Second Communication							
Stereo format '0010 - right channel for stereo format.							
Second Community Second Comm							
Stereo format. Sample Word Length Sample Word Length Sample frequency is indicated in reg84[3:0]							
Sample Word Length					'0010 – right channel for		
Sample Word Length					stereo format.		
Sample frequency is indicated in reg84[3:0]	9F	Audio Ch status3	RO	7:4		R	Audio Channel status decoder value [35:28]
3:2 reserved 1:0 Clock accurance Received packet type low byte Pkt_type_L RO		110010_011_0101000	110	' ' '	Sumpre word Bengun		
1:0 Clock accurance Received packet type low byte Received packet type low byte Received packet type low byte Received packet type is cleared each time it's read.				3.7	reserved		sumple frequency is maleuted in rego ([3.0]
Received packet type low byte Pkt_type is cleared each time it's read.							
Name	0 10	Di	D.O.	1:0	Clock accurance		D : 1 1 1
0xA1 BKSV0 RO HDCP BKSV value readback [7:0] 0xA2 BKSV1 RO HDCP BKSV value readback [15:8] 0xA3 BKSV2 RO HDCP BKSV value readback [23:16] 0xA4 BKSV3 RO HDCP BKSV value readback [31:24] 0xA5 BKSV4 RO HDCP BKSV value readback [39:32] 0xA6 Pkt_ctrl 5 REG_GENPKT_HL 0 GenPkt registers latch data selector 1 4 REG_ISRC2_HL 0 ISRC2 registers latch data selector 1 1 newpkt_sel [3] 0 ISRC2 1 1 newpkt_sel [2] 0 ISRC1 1 1 newpkt_sel [2] 0 ISRC1 1 1 newpkt_sel [1] 0 ACP 0 0 0 Generanl Packet 0xA7 Pkt_rec_typeH W/R 7:0 0x0A Decide which kind of packet to be recorded on General PKT registers. 0xA8 Pkt_rec_typeL W/R 7:0 0x83 Decide which kind of packet to be ful	0xA0	Pkt_type_L	RO				
0xA2 BKSV1 RO HDCP BKSV value readback [15:8] 0xA3 BKSV2 RO HDCP BKSV value readback [23:16] 0xA4 BKSV3 RO HDCP BKSV value readback [31:24] 0xA5 BKSV4 RO HDCP BKSV value readback [39:32] 0xA6 Pkt_ctrl W/R 5 REG_GENPKT_HL 0 GenPkt registers latch data selector 4 REG_ISRC2_HL 0 ISRC2 1: latch unsupport packet data 0: latch normal data 2 newpkt_sel [3] 0 ISRC1 1 newpkt_sel [1] 0 ACP 0 newpkt_sel [0] 0 Generanl Packet 0xA7 Pkt_rec_typeH W/R 7:0 0xA8 Pkt_rec_typeL W/R 7:0 0xA8 Pkt_rec_typeL W/R 7:0 0xA8 Pkt_rec_typeL W/R 7:0 0xA9 SRC_ver RO 0xA9 SRC_ver RO 0xA9 SRC_pb25 RO 0xAB AVI infoFrame Data Byte 25 0xAB AVI infoFrame Data Byte 0							
DXA3 BKSV2 RO	0xA1	BKSV0	RO				HDCP BKSV value readback [7:0]
DXA4 BKSV3 RO HDCP BKSV value readback [31:24] DXA5 BKSV4 RO HDCP BKSV value readback [39:32] DXA6 Pkt_ctrl W/R S REG_GENPKT_HL O GenPkt registers latch data selector	0xA2	BKSV1	RO				HDCP BKSV value readback [15:8]
DXA4 BKSV3 RO HDCP BKSV value readback [31:24] DXA5 BKSV4 RO HDCP BKSV value readback [39:32] DXA6 Pkt_ctrl W/R S REG_GENPKT_HL O GenPkt registers latch data selector	0xA3	BKSV2	RO		·		HDCP BKSV value readback [23:16]
OxA5 BKSV4 RO HDCP BKSV value readback [39:32] OxA6 Pkt_ctrl W/R 5 REG_GENPKT_HL 0 GenPkt registers latch data selector 4 REG_ISRC2_HL 0 ISRC2 registers latch data selector 3 newpkt_sel [3] 0 ISRC2 1 latch unsupport packet data 2 newpkt_sel [2] 0 ISRC1 1 newpkt_sel [1] 0 ACP 0 newpkt_sel [0] 0 Generanl Packet OxA7 Pkt_rec_typeH W/R 7:0 Ox0A Decide which kind of packet to be recorded on General PKT registers. OxA8 Pkt_rec_typeL W/R 7:0 Ox83 Decide which kind of packet to be fully recorded on General PKT registers. OxA9 SRC_ver RO SPD infoFrame Version OxAA SRC_pb25 RO SPD infoFrame Data Byte 25 OxAB AVI_leng RO AVI infoFrame Data Byte 0 OxAC AVI_DB0 RO AVI infoFrame Data Byte 0 OxAE AVI_DB1 RO AVI infoFrame Data Byte 1							
OxA6							
4 REG_ISRC2_HL 0 ISRC2 registers latch data selector 3 newpkt_sel [3] 0 ISRC2 1: latch unsupport packet data 0: latch normal data 2 newpkt_sel [2] 0 ISRC1 1 newpkt_sel [1] 0 ACP 0 newpkt_sel [0] 0 Generanl Packet 0xA7 Pkt_rec_typeH W/R 7:0 0xA8 Pkt_rec_typeL W/R 7:0 0xA8 Pkt_rec_typeL W/R 7:0 0xA8 Pkt_rec_typeL W/R 7:0 0xA9 SRC_ver RO 0xA4 SRC_pb25 RO 0xAA SRC_pb25 RO 0xAB AVI_leng RO 0xAC AVI_VER RO 0xAC AVI_VER RO 0xAC AVI_DB1 RO 4VI infoFrame Data Byte 0 AVI infoFrame Data Byte 0 AVI infoFrame Data Byte 0 AVI infoFrame Data Byte 1					DEG GENDYE III	0	
3 newpkt_sel [3] 0 ISRC2 1: latch unsupport packet data 0: latch normal data 2 newpkt_sel [2] 0 ISRC1 1 newpkt_sel [1] 0 ACP 0 newpkt_sel [0] 0 Generanl Packet 0xA7 Pkt_rec_typeH W/R 7:0 0xA8 Pkt_rec_typeL W/R 7:0 0xA8 Pkt_rec_typeL W/R 7:0 0x83 Decide which kind of packet to be recorded on General PKT registers. 0xA9 SRC_ver RO 0xA9 SRC_ver RO 0xA0 SPD infoFrame Version 0xAA SRC_pb25 0xAB AVI_leng RO 0xAC AVI_VER RO 0xAC AVI_VER RO 0xAC AVI_VER RO 0xAC AVI_DB0 RO 0xAC AVI_DB1 RO 0 AVI infoFrame Data Byte 0 0xAC AVI_DB1 RO 0 AVI infoFrame Data Byte 1	0xA6	Pkt_ctrl	W/R	5	REG_GENPKT_HL	0	GenPkt registers latch data selector
3 newpkt_sel [3] 0 ISRC2 1: latch unsupport packet data 0: latch normal data 2 newpkt_sel [2] 0 ISRC1 1 newpkt_sel [1] 0 ACP 0 newpkt_sel [0] 0 Generanl Packet 0xA7 Pkt_rec_typeH W/R 7:0 0xA8 Pkt_rec_typeL W/R 7:0 0xA8 Pkt_rec_typeL W/R 7:0 0x83 Decide which kind of packet to be recorded on General PKT registers. 0xA9 SRC_ver RO 0xA9 SRC_ver RO 0xA0 SPD infoFrame Version 0xAA SRC_pb25 0xAB AVI_leng RO 0xAC AVI_VER RO 0xAC AVI_VER RO 0xAC AVI_VER RO 0xAC AVI_DB0 RO 0xAC AVI_DB1 RO 0 AVI infoFrame Data Byte 0 0xAC AVI_DB1 RO 0 AVI infoFrame Data Byte 1				4	REG ISRC2 HL	0	ISRC2 registers latch data selector
1: latch unsupport packet data 0: latch normal data 2 newpkt_sel [2] 0 ISRC1 1 newpkt_sel [1] 0 ACP 0 newpkt_sel [0] 0 Generanl Packet 0xA7 Pkt_rec_typeH W/R 7:0 0x0A Decide which kind of packet to be recorded on General PKT registers. 0xA8 Pkt_rec_typeL W/R 7:0 0x83 Decide which kind of packet to be fully recorded on General PKT registers. 0xA9 SRC_ver RO SPD infoFrame Version 0xAA SRC_pb25 RO SPD infoFrame Data Byte 25 0xAB AVI_leng RO AVI infoFrame Length 0xAC AVI_VER RO AVI infoFrame Data Byte 0 0xAE AVI_DB1 RO AVI infoFrame Data Byte 1							
0: latch normal data 2 newpkt_sel [2] 0 ISRC1 1 newpkt_sel [1] 0 ACP 0 newpkt_sel [0] 0 Generanl Packet 0xA7 Pkt_rec_typeH W/R 7:0 0x0A Decide which kind of packet to be recorded on General PKT registers. 0xA8 Pkt_rec_typeL W/R 7:0 0x83 Decide which kind of packet to be fully recorded on General PKT registers. 0xA9 SRC_ver RO SPD infoFrame Version 0xAA SRC_pb25 RO SPD infoFrame Data Byte 25 0xAB AVI_leng RO AVI infoFrame Length 0xAC AVI_VER RO AVI infoFrame Version 0xAD AVI_DB0 RO AVI infoFrame Data Byte 0 0xAE AVI_DB1 RO AVI infoFrame Data Byte 1				3	newpkt_sel [3]	O	
2 newpkt_sel [2] 0 ISRC1 1 newpkt_sel [1] 0 ACP 0 newpkt_sel [0] 0 Generanl Packet 0xA7 Pkt_rec_typeH W/R 7:0 0x0A Decide which kind of packet to be recorded on General PKT registers. 0xA8 Pkt_rec_typeL W/R 7:0 0x83 Decide which kind of packet to be fully recorded on General PKT registers. 0xA9 SRC_ver RO SPD infoFrame Version 0xAA SRC_pb25 RO SPD infoFrame Data Byte 25 0xAB AVI_leng RO AVI infoFrame Length 0xAC AVI_VER RO AVI infoFrame Version 0xAD AVI_DB0 RO AVI infoFrame Data Byte 0 0xAE AVI_DB1 RO AVI infoFrame Data Byte 1							
1 newpkt_sel [1] 0 ACP 0 newpkt_sel [0] 0 Generanl Packet 0xA7 Pkt_rec_typeH W/R 7:0 0x0A Decide which kind of packet to be recorded on General PKT registers. 0xA8 Pkt_rec_typeL W/R 7:0 0x83 Decide which kind of packet to be fully recorded on General PKT registers. 0xA9 SRC_ver RO SPD infoFrame Version 0xAA SRC_pb25 RO SPD infoFrame Data Byte 25 0xAB AVI_leng RO AVI infoFrame Length 0xAC AVI_VER RO AVI infoFrame Version 0xAD AVI_DB0 RO AVI infoFrame Data Byte 0 0xAE AVI_DB1 RO AVI infoFrame Data Byte 1							0: latch normal data
1 newpkt_sel [1] 0 ACP 0 newpkt_sel [0] 0 Generanl Packet 0xA7 Pkt_rec_typeH W/R 7:0 0x0A Decide which kind of packet to be recorded on General PKT registers. 0xA8 Pkt_rec_typeL W/R 7:0 0x83 Decide which kind of packet to be fully recorded on General PKT registers. 0xA9 SRC_ver RO SPD infoFrame Version 0xAA SRC_pb25 RO SPD infoFrame Data Byte 25 0xAB AVI_leng RO AVI infoFrame Length 0xAC AVI_VER RO AVI infoFrame Version 0xAD AVI_DB0 RO AVI infoFrame Data Byte 0 0xAE AVI_DB1 RO AVI infoFrame Data Byte 1				2	newpkt_sel [2]	0	ISRC1
0 newpkt_sel [0] 0 Generanl Packet 0xA7 Pkt_rec_typeH W/R 7:0 0x0A Decide which kind of packet to be recorded on General PKT registers. 0xA8 Pkt_rec_typeL W/R 7:0 0x83 Decide which kind of packet to be fully recorded on General PKT registers. 0xA9 SRC_ver RO SPD infoFrame Version 0xAA SRC_pb25 RO SPD infoFrame Data Byte 25 0xAB AVI_leng RO AVI infoFrame Length 0xAC AVI_VER RO AVI infoFrame Version 0xAD AVI_DB0 RO AVI infoFrame Data Byte 0 0xAE AVI_DB1 RO AVI infoFrame Data Byte 1			I		_		
0xA7Pkt_rec_typeHW/R7:00x0ADecide which kind of packet to be recorded on General PKT registers.0xA8Pkt_rec_typeLW/R7:00x83Decide which kind of packet to be fully recorded on General PKT registers.0xA9SRC_verROSPD infoFrame Version0xAASRC_pb25ROSPD infoFrame Data Byte 250xABAVI lengROAVI infoFrame Length0xACAVI_VERROAVI infoFrame Version0xADAVI_DB0ROAVI infoFrame Data Byte 00xAEAVI_DB1ROAVI infoFrame Data Byte 1			P	_1	•		ACP
0xA7Pkt_rec_typeHW/R7:00x0ADecide which kind of packet to be recorded on General PKT registers.0xA8Pkt_rec_typeLW/R7:00x83Decide which kind of packet to be fully recorded on General PKT registers.0xA9SRC_verROSPD infoFrame Version0xAASRC_pb25ROSPD infoFrame Data Byte 250xABAVI lengROAVI infoFrame Length0xACAVI_VERROAVI infoFrame Version0xADAVI_DB0ROAVI infoFrame Data Byte 00xAEAVI_DB1ROAVI infoFrame Data Byte 1				0	newpkt_sel [0]	0	Generanl Packet
on General PKT registers. 0xA8 Pkt_rec_typeL W/R 7:0 0x83 Decide which kind of packet to be fully recorded on General PKT registers. 0xA9 SRC_ver RO SPD infoFrame Version 0xAA SRC_pb25 RO SPD infoFrame Data Byte 25 0xAB AVI_leng RO AVI infoFrame Length 0xAC AVI_VER RO AVI infoFrame Version 0xAD AVI_DB0 RO AVI infoFrame Data Byte 0 0xAE AVI_DB1 RO AVI infoFrame Data Byte 1	0- 47	Dist man to TI	W/D	7.0			
0xA8Pkt_rec_typeLW/R7:00x83Decide which kind of packet to be fully recorded on General PKT registers.0xA9SRC_verROSPD infoFrame Version0xAASRC_pb25ROSPD infoFrame Data Byte 250xABAVI_lengROAVI infoFrame Length0xACAVI_VERROAVI infoFrame Version0xADAVI_DB0ROAVI infoFrame Data Byte 00xAEAVI_DB1ROAVI infoFrame Data Byte 1	UXA/	rkt_rec_typeH	W/K	7:0		UXUA	
recorded on General PKT registers. 0xA9 SRC_ver RO SPD infoFrame Version 0xAA SRC_pb25 RO SPD infoFrame Data Byte 25 0xAB AVI_leng RO AVI infoFrame Length 0xAC AVI_VER RO AVI infoFrame Version 0xAD AVI_DB0 RO AVI infoFrame Data Byte 0 0xAE AVI_DB1 RO AVI infoFrame Data Byte 1				<u> </u>		_	
0xA9SRC_verROSPD infoFrame Version0xAASRC_pb25ROSPD infoFrame Data Byte 250xABAVI_lengROAVI infoFrame Length0xACAVI_VERROAVI infoFrame Version0xADAVI_DB0ROAVI infoFrame Data Byte 00xAEAVI_DB1ROAVI infoFrame Data Byte 1	0xA8	Pkt_rec_typeL	W/R	7:0		0x83	
0xA9SRC_verROSPD infoFrame Version0xAASRC_pb25ROSPD infoFrame Data Byte 250xABAVI_lengROAVI infoFrame Length0xACAVI_VERROAVI infoFrame Version0xADAVI_DB0ROAVI infoFrame Data Byte 00xAEAVI_DB1ROAVI infoFrame Data Byte 1							recorded on General PKT registers.
0xAASRC_pb25ROSPD infoFrame Data Byte 250xABAVI_lengROAVI infoFrame Length0xACAVI_VERROAVI infoFrame Version0xADAVI_DB0ROAVI infoFrame Data Byte 00xAEAVI_DB1ROAVI infoFrame Data Byte 1	0xA9	SRC ver	RO				
0xAB AVI_leng RO AVI infoFrame Length 0xAC AVI_VER RO AVI infoFrame Version 0xAD AVI_DB0 RO AVI infoFrame Data Byte 0 0xAE AVI_DB1 RO AVI infoFrame Data Byte 1							
0xAC AVI_VER RO AVI infoFrame Version 0xAD AVI_DB0 RO AVI infoFrame Data Byte 0 0xAE AVI_DB1 RO AVI infoFrame Data Byte 1		•				 	·
0xAD AVI_DB0 RO AVI infoFrame Data Byte 0 0xAE AVI_DB1 RO AVI infoFrame Data Byte 1		•		-		-	
0xAE AVI_DB1 RO AVI infoFrame Data Byte 1				ļ			
							•
OxAF AVI DB2 RO AVI infoFrame Data Byte 2							•
		ATH DDA	DO		l		AVI infoFrame Data Ryte 2

0 00 1111 000	In o			LIVIII OF DO DO DO
0xB0 AVI_DB3	RO			AVI infoFrame Data Byte 3
0xB1 AVI_DB4	RO			AVI infoFrame Data Byte 4
0xB2 AVI_DB5	RO			AVI infoFrame Data Byte 5
0xB3 AVI_DB6	RO			AVI infoFrame Data Byte 6
0xB4 AVI_DB7	RO			AVI infoFrame Data Byte 7
0xB5 AVI_DB8	RO			AVI infoFrame Data Byte 8
0xB6 AVI_DB9	RO			AVI infoFrame Data Byte 9
0xB7 AVI_DB10	RO			AVI infoFrame Data Byte 10
0xB8 AVI_DB11	RO			AVI infoFrame Data Byte 11
0xB9 AVI_DB12	RO			AVI infoFrame Data Byte 12
0xBA AVI_DB13	RO			AVI infoFrame Data Byte 13
0xBB AVI_DB14	RO			AVI infoFrame Data Byte 14
0xBC AVI_DB15	RO			AVI infoFrame Data Byte 15
0xBD GENPKT_HB0	RO			This is a general-purpose register recording
				one kind of the packets.
				RegA8 is the recorder header to catch.
				Genaral Packet Header Byte 0
0xBE GENPKT_HB1	RO			Genaral Packet Header Byte 1
0xBF GENPKT_HB2	RO			Genaral Packet Header Byte 2
0xC0 GENPKT_DB0	RO			Genaral Packet Data Byte 0
0xC1 GENPKT_DB1	RO			Genaral Packet Data Byte 1
0xC2 GENPKT_DB2	RO			Genaral Packet Data Byte 2
0xC3 GENPKT_DB3	RO			Genaral Packet Data Byte 3
0xC4 GENPKT_DB4	RO			Genaral Packet Data Byte 4
0xC5 GENPKT_DB5	RO			Genaral Packet Data Byte 5
0xC6 GENPKT_DB6	RO			Genaral Packet Data Byte 6
0xC7 GENPKT_DB7	RO			Genaral Packet Data Byte 7
0xC8 GENPKT_DB8	RO			Genaral Packet Data Byte 8
0xC9 GENPKT_DB9	RO			Genaral Packet Data Byte 9
0xCA GENPKT_DB10	RO			Genaral Packet Data Byte 10
0xCB GENPKT_DB11	RO			Genaral Packet Data Byte 11
0xCC GENPKT_DB12	RO			Genaral Packet Data Byte 12
0xCD GENPKT_DB13	RO			Genaral Packet Data Byte 13
0xCE GENPKT_DB14	RO			Genaral Packet Data Byte 14
0xCF GENPKT_DB15	RO			Genaral Packet Data Byte 15
0xD0 GENPKT_DB16	RO			Genaral Packet Data Byte 16
0xD1 GENPKT_DB17	RO			Genaral Packet Data Byte 17
0xD2 GENPKT_DB18	RO			Genaral Packet Data Byte 18
0xD3 GENPKT_DB19	RO			Genaral Packet Data Byte 19
0xD4 GENPKT_DB20	RO			Genaral Packet Data Byte 20
0xD5 GENPKT_DB21	RO	_		Genaral Packet Data Byte 21
0xD6 GENPKT_DB22	RO			Genaral Packet Data Byte 22
0xD7 GENPKT_DB23	RO			Genaral Packet Data Byte 23
0xD8 GENPKT_DB24	RO			Genaral Packet Data Byte 24
0xD9 GENPKT_DB25	RO			Genaral Packet Data Byte 25
0xDA GENPKT_DB26	RO			Genaral Packet Data Byte 26
0xDB GENPKT_DB27	RO			Genaral Packet Data Byte 27
0xDC Audio_Ver	RO			Audio infoFrame Version
0xDD Audio_DB0	RO			Audio infoFrame Data Byte 0
0xDE Audio_DB1	RO			Audio infoFrame Data Byte 1
0xDF Audio_DB2	RO			Audio infoFrame Data Byte 2
0xE0 Audio_DB3	RO			Audio infoFrame Data Byte 3
0xE1 Audio_DB4	RO			Audio infoFrame Data Byte 4
0xE2 Audio_DB5	RO			Audio infoFrame Data Byte 5
0xE3 Audio_leng	RO			Audio infoFrame Length
0xE4 MPEG_Ver	RO			MPEG infoFrame Version
0xE5 MPEG_leng	RO			MPEG infoFrame Length
0xE6 MPEG_DB0	RO			MPEG infoFrame Data Byte 0

		1		1	T
	MPEG_DB1	RO			MPEG infoFrame Data Byte 1
	MPEG_DB2	RO			MPEG infoFrame Data Byte 2
0xE9	MPEG_DB3	RO			MPEG infoFrame Data Byte 3
	MPEG_DB4	RO			MPEG infoFrame Data Byte 4
0xEB	MPEG_DB5	RO			MPEG infoFrame Data Byte 5
0xEC	ACP_HB0	RO			ACP packet Header Byte 0
0xED	ACP_HB1	RO			ACP packet Header Byte 1
0xEE	ACP_HB2	RO			ACP packet Header Byte 2
0xEF	ACP_DB0	RO			ACP packet Data Byte 0
0xF0	ACP_DB1	RO			ACP packet Data Byte 1
0xF1	ACP_DB2	RO			ACP packet Data Byte 2
0xF2	ACP_DB3	RO			ACP packet Data Byte 3
0xF3	ACP_DB4	RO			ACP packet Data Byte 4
	ACP_DB5	RO			ACP packet Data Byte 5
0xF5	ACP_DB6	RO			ACP packet Data Byte 6
0xF6	ACP_DB7	RO			ACP packet Data Byte 7
0xF7	ACP_DB8	RO			ACP packet Data Byte 8
0xF8	ACP_DB9	RO			ACP packet Data Byte 9
0xF9	ACP_DB10	RO			ACP packet Data Byte 10
0xFA	ACP_DB11	RO			ACP packet Data Byte 11
0xFB	ACP_DB12	RO			ACP packet Data Byte 12
0xFC	ACP_DB13	RO			ACP packet Data Byte 13
0xFD	ACP_DB14	RO			ACP packet Data Byte 14
0xFE	ACP_DB15	RO			ACP packet Data Byte 15
0xFF	ACP_rec_type	W/R	7:0	0x04	The packet type will be stored to ACP
					register

Block2 (reg0F[0] = '1')

DIUCKA	z (regurtu) = 1	,				
	Reg_Name	W/R	Bits	Status	Default	Description
Offset	MON FIEO 40	XX/D			0.00	THE CD MOVERED VIZ. 01
	KSV_FIFO40	W/R			0x00	HDCP KSVFIFO4 [7:0]
0x81	KSV_FIFO41	W/R			0x00	HDCP KSVFIFO4 [15:8]
0x82	KSV_FIFO42	W/R			0x00	HDCP KSVFIFO4 [23:16]
0x83	KSV_FIFO43	W/R			0x00	HDCP KSVFIFO4 [31:24]
0x84	KSV_FIFO44	W/R			0x00	HDCP KSVFIFO4 [39:32]
0x85	KSV_FIFO50	W/R			0x00	HDCP KSVFIFO5 [7:0]
0x86	KSV_FIFO51	W/R			0x00	HDCP KSVFIFO5 [15:8]
0x87	KSV_FIFO52	W/R			0x00	HDCP KSVFIFO5 [23:16]
	KSV_FIFO53	W/R			0x00	HDCP KSVFIFO5 [31:24]
0x89 0x8A	KSV_FIFO54	W/R W/R			0x00	HDCP KSVFIFO5 [39:32]
	KSV_FIFO60	W/R			0x00	HDCP KSVFIFO6 [7:0]
	KSV_FIFO61	W/R			0x00 0x00	HDCP KSVFIFO6 [15:8]
0x8D	KSV_FIFO62	W/R			0x00	HDCP KSVFIFO6 [23:16]
0x8E	KSV_FIFO63	W/R			0x00	HDCP KSVFIFO6 [31:24]
0x8F	KSV_FIFO64	W/R			0x00	HDCP KSVFIFO6 [39:32]
0x90	KSV_FIFO70	W/R			0x00	HDCP KSVFIFO7 [7:0]
0x90 $0x91$	KSV_FIFO71	W/R			0x00	HDCP KSVFIFO7 [15:8]
0x91 0x92	KSV_FIFO72 KSV_FIFO73	W/R			0x00	HDCP KSVFIFO7 [23:16]
0x92 0x93	KSV_FIFO74	W/R			0x00	HDCP KSVFIFO7 [31:24] HDCP KSVFIFO7 [39:32]
0x93 0x94	Pkt_type_maskL	W/R			UXUU	Received packet type mask
	Pkt_type_maskH		3:0			Received packet type mask Received packet type mask
	ISRC1_HB0	RO	3.0			ISRC1 packet Header Byte 0
	ISRC1_HB1	RO				ISRC1 packet Header Byte 0
	ISRC1_HB2	RO				ISRC1 packet Header Byte 1
	ISRC1_DB0	RO				ISRC1 packet Data Byte 0
	ISRC1_DB1	RO				ISRC1 packet Data Byte 0
	ISRC1_DB1	RO				ISRC1 packet Data Byte 1
	ISRC1_DB3	RO				ISRC1 packet Data Byte 2
	ISRC1_DB4	RO				ISRC1 packet Data Byte 3
	ISRC1_DB5	RO				ISRC1 packet Data Byte 5
	ISRC1_DB6	RO				ISRC1 packet Data Byte 6
	ISRC1_DB7	RO				ISRC1 packet Data Byte 7
	ISRC1_DB8	RO				ISRC1 packet Data Byte 8
	ISRC1_DB9	RO				ISRC1 packet Data Byte 9
	ISRC1_DB10	RO				ISRC1 packet Data Byte 10
-	ISRC1_DB11	RO				ISRC1 packet Data Byte 11
	ISRC1_DB12	RO				ISRC1 packet Data Byte 12
	ISRC1_DB13	RO				ISRC1 packet Data Byte 13
	ISRC1_DB14	RO				ISRC1 packet Data Byte 14
	ISRC1_DB15	RO				ISRC1 packet Data Byte 15
	ISRC1_rec_type	W/R			0x05	The packet type will be stored to ISRC1
0.120	isite1_io_iypt	,20			0.100	register
0xB4	ISRC2_HB0	RO				ISRC2 packet Header Byte 0
-	ISRC2_HB1	RO				ISRC2 packet Header Byte 1
0xB6	ISRC2_HB2	RO				ISRC2 packet Header Byte 2
	ISRC2_DB0	RO				ISRC2 packet Data Byte 0
	ISRC2_DB1	RO				ISRC2 packet Data Byte 0
	ISRC2_DB1	RO				ISRC2 packet Data Byte 1
	ISRC2_DB3	RO				ISRC2 packet Data Byte 3
	ISRC2_DB4	RO				ISRC2 packet Data Byte 4
	ISRC2_DB5	RO				ISRC2 packet Data Byte 5
	ISRC2_DB6	RO				ISRC2 packet Data Byte 6
	ISRC2_DB7	RO				ISRC2 packet Data Byte 7
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0xBF	ISRC2_DB8	RO			ISRC2 packet Data Byte 8
0xC0	ISRC2_rec_type	W/R		0x06	The packet type will be stored to ISRC2
					register
0xC1	KSV_FIFO00	W/R		0x00	HDCP KSVFIFO0 [7:0]
0xC2	KSV_FIFO01	W/R		0x00	HDCP KSVFIFO0 [15:8]
0xC3	KSV_FIFO02	W/R		0x00	HDCP KSVFIFO0 [23:16]
0xC4	KSV_FIFO03	W/R		0x00	HDCP KSVFIF00 [31:24]
0xC5	KSV_FIFO04	W/R		0x00	HDCP KSVFIF00 [39:32]
0xC6	KSV_FIFO10	W/R		0x00	HDCP KSVFIFO1 [7:0]
0xC7	KSV_FIFO11	W/R		0x00	HDCP KSVFIFO1 [15:8]
0xC7	KSV_FIFO12	W/R		0x00	HDCP KSVFIFO1 [23:16]
0xC8	KSV_FIFO13	W/R		0x00	HDCP KSVFIFO1 [23.10]
	KSV_FIFO14	W/R		0x00	HDCP KSVFIFO1 [31:24]
	_				
-	KSV_FIFO20	W/R		0x00	HDCP KSVFIFO2 [7:0]
0xCC	KSV_FIFO21	W/R		0x00	HDCP KSVFIFO2 [15:8]
-	KSV_FIFO22	W/R		0x00	HDCP KSVFIFO2 [23:16]
0xCE	KSV_FIFO23	W/R		0x00	HDCP KSVFIFO2 [31:24]
0xCF	KSV_FIFO24	W/R		0x00	HDCP KSVFIFO2 [39:32]
0xD0	KSV_FIFO30	W/R		0x00	HDCP KSVFIFO3 [7:0]
0xD1	KSV_FIFO31	W/R		0x00	HDCP KSVFIFO3 [15:8]
0xD2	KSV_FIFO32	W/R		0x00	HDCP KSVFIFO3 [23:16]
0xD3	KSV_FIFO33	W/R		0x00	HDCP KSVFIFO3 [31:24]
0xD4	KSV_FIFO34	W/R		0x00	HDCP KSVFIFO3 [39:32]
0xD5	BstatusL		7:0	0x00	HDCP BStatus[7:0]
0xD6	BstatusH	W/R	3:0	0x0	HDCP Bstatus[11:8]
					The HDCP BStatus[12] refer to HDMI status
					represented in Reg10[4].
	SHA1_H00	W/R		0x00	HDCP SHA1_H0 [7:0]
	SHA1_H01	W/R		0x00	HDCP SHA1_H0 [15:8]
	SHA1_H02	W/R		0x00	HDCP SHA1_H0 [23:16]
	SHA1_H03	W/R		0x00	HDCP SHA1_H0 [31:24]
	SHA1_H10	W/R		0x00	HDCP SHA1_H1 [7:0]
0xDC	SHA1_H11	W/R		0x00	HDCP SHA1_H1 [15:8]
	SHA1_H12	W/R		0x00	HDCP SHA1_H1 [23:16]
0xDE	SHA1_H13	W/R		0x00	HDCP SHA1_H1 [31:24]
0xDF	SHA1_H20	W/R		0x00	HDCP SHA1_H2 [7:0]
0xE0	SHA1_H21	W/R		0x00	HDCP SHA1_H2 [15:8]
0xE1	SHA1_H22	W/R		0x00	HDCP SHA1_H2 [23:16]
0xE2	SHA1_H23	W/R		0x00	HDCP SHA1_H2 [31:24]
0xE3	SHA1_H30	W/R		0x00	HDCP SHA1_H3 [7:0]
0xE4	SHA1_H31	W/R		0x00	HDCP SHA1_H3 [15:8]
0xE5	SHA1_H32	W/R		0x00	HDCP SHA1_H3 [23:16]
0xE6	SHA1_H33	W/R		0x00	HDCP SHA1_H3 [31:24]
0xE7	SHA1_H40	W/R		0x00	HDCP SHA1_H4 [7:0]
0xE8	SHA1_H41	W/R		0x00	HDCP SHA1_H4 [15:8]
0xE9	SHA1_H42	W/R		0x00	HDCP SHA1_H4 [23:16]
0xEA	SHA1_H43	W/R		0x00	HDCP SHA1_H4 [31:24]
0xEB	M0_B0	RO			HDCP Mi value readback [7:0]
0xEC	M0 B1	RO			HDCP Mi value readback [15:8]
0xED	M0 B2	RO			HDCP Mi value readback [23:16]
0xEE	M0_B3	RO			HDCP Mi value readback [31:24]
0xEF	M0_B3	RO			HDCP Mi value readback [39:32]
0xF0	M0_B4 M0_B5	RO			HDCP Mi value readback [47:40]
0xF1	M0_B3 M0_B6	RO			HDCP Mi value readback [47.40]
0xF1 0xF2	M0_B7	RO			HDCP Mi value readback [53:46]
OVI.7	1410_D /	NU		I .	TIDET IVII VAIUC ICAUDACK [US.JU]