IT6604/IT6605 Register Table V1.03

Term:

RO: Read Only

W/R: Read/Write

Reg Offset	Reg_Name	W/R	Bits	Status	Default	Description
0x00	VID_L	RO	7:0		0x00	
0x01	Backup_reg2	WR	7:0	Reserved	0x00	
0x02	DEVID_L	RO	7:0		0x23	Device ID (Low word)
0x03	DEVID_H	RO	7:0		0x60	Device ID (High word)
0x04	DevRev	RO	7:0		0xa3	Device Revision Number
0x05	Rst_Ctrl	W/R	7	REG_CDR_RST	0	1: reset CDR.
			6	Reserved	0	
			5	REG_AUTO_CDR_RST	0	1: Auto reset CDR
			4	REGRST	0	1: Software reset the clock domain include control registers to default
			3	Reserved(not used)	0	
			2	AUDRST	0	1: Software reset audio logic
			1	VDORST	0	1: Software reset video logic
			0	SWRST	0	1: Software reset all logic
0x06	Pwd_Ctrl0	W/R	7	PWD_Ch2	0	1: Power down channel2
			6	PWD_Ch1	0	1: Power down channel1
			5	PWD_Ch0	0	1: Power down channel0
			4	PWD_ACLK	0	1: Power down Audio clock domain
			3	PWD_PCLK	0	1: Power down Pixel clock domain
			2	PWD_APLL	0	1: Power down Audio PLL
			1	PWD_RXPLL	0	1: Power down Pixel PLL
			0	PWD_ALL	0	1: Power down all AFEs and Logic blocks
0x07	Pwd_Ctrl1	W/R	4	Sel_port	0	Select active port: 0: portA 1: portB (IT6605 only)
			3	PWD_AFEall	0	1: Power down all AFEs
			2	PWDC_ETC	0	1: Power down certain AFE blocks
			1	PWDC_SRV	0	1: Power down AFE equalizer
			0	EN_AutoPWD	0	1: Auto Power down whole chip when no clock is detected
0x08	VIO_Ctrl	W/R	7	VIO_Slew	1	Video data Slew rate Slew rate: 0:Fast ; 1:Slow
			6:4	VIO_ST	001	VDATA Driving Strength 000:2mA ; 001:4mA; 010:6mA ; 011:8mA; 100:10mA;101:12mA; 110:14mA;111:16mA;
			3	Vclk_Slew	1	VCLK Slew rate Slew rate: 0:Fast ; 1:Slow
			2:0	Vclk_ST	011	VCLK Driving Strength 000:2mA ; 001:4mA; 010:6mA ; 011:8mA; 100:10mA;101:12mA; 110:14mA;111:16mA;
0x09	AIO_Ctrl	W/R	7	AIO_Slew	1	Audio data Slew rate Slew rate: 0:Fast ; 1:Slow
			6:4	AIO_ST	001	Audio data Driving Strength 000:2mA ; 001:4mA; 010:6mA ; 011:8mA; 100:10mA;101:12mA;

						110:14mA;111:16mA;
			3	Mclk_Slew	1	Audio clock Slew rate Slew rate: 0:Fast ; 1:Slow
			2:0	Mclk_ST	001	Audio Driving Strength 000:2mA ; 001:4mA; 010:6mA ; 011:8mA; 100:10mA;101:12mA; 110:14mA;111:16mA;
0x0A	Reserved	W/R			0x2A	
0x0B	Reserved	W/R			0xA5	
0x0C	BIST_Ctrl	W/R	0	ARAM_BIST_EN	0	Internal Audio FIFO BIST test circuits
0x0D	BIST_Result1	RO	7 6:0	ARAM_bo_faultHQ ARAM_D6FaulStauHQ		Audio FIFO BIST status
0x0E	Reserved					
0x0F	Block_Sel	W/R	0	Block_ID	0	**Register block select** 0: block 0 is select for Reading and writing 1: block 1 is select for Reading and writing
0x10	Sys_state	RO	7	RXPLL_LOCK	x	1: RX PLL is lock
			6	RXCK_Speed	x	1: RX clock is lower than 80Mhz
			5	RXCK_VALID	x	1: Clock is valid
			4	HDMI_MODE	x	1: HDMI mode or DVI mode (value:0)
			3	P1_PWR5V_DET	x	1: Port-1 5V is detect
			2	SCDT	x	1: Video Sync is stable
			1	VCLK_DET	x	1: Video clock is detect
			0	PWR5V_DET	x	1: Port-0 5V is detect
0x11	HDCP_Ctrl	W/R	7 6 5 4 3 2 1 0	ExtROM reserved reserved reserved HDCP_RomDisWr HDCP_A0 reserved HDCP_en	0x89	1: select internal OTP as HDCP key ROM 1: Disable external ROM write function 1: Select 0x76 as DDC address.(default is 0x74) 1: Enable HDCP
0x12	HDCP_Status	RO	7-4 3 2 1 0	reserved HDCP_ADVCipher HDCP_EESS HDCP_KeyRd_Fail_Flag Hdcp_on_Flag		Show the HDCP authentication stauts
0x13	Interrupt0	RO	5 4 3 2 1 0	VidMode_Chg HDMIMode_Chg SCDTOFF SCDTON Pwr5VOff Pwr5Von		'1': Video mode change '1': HDMI/DVI mode swap change '1': Video stable is off '1': Video stable is on '1': Selected port 5V is off '1': Selected port 5V is on
0x14	Interrupt1	RO	7 6 5 4 3 2 1 0	PktLeftMute NewAudioPkt_Det NewACPPkt_Det NewSPDPkt_Det NewMPEGPkt_Det NewAVIPkt_Det NoAVI_Rcv PktSetMute		'1': Left Mute Packet is received '1': New Audio Packet detect '1': New ACP Packet detect '1': New SPD Packet detect '1': New MPEG Packet detect '1': New AVI Packet detect '1': No AVI Packet is received '1': Set Mute Packet is received
0x15	Interrupt2	RO	5 4 3 2 1 0	ROMFault AutoAudMute AudFIFOErr ECCERR Auth_done Auth_start		'1': ROM access Fault Flag '1': Audio Auto Mute Flag '1': Audio FIFO error Flag '1': EDD error Flag '1': Authentication Done Flag '1': Authentication Start Flag
0x16	Interrupt_MASK0	W/R	5:0		0x3F	Mask of interrupts defined in reg0x13

						1: The Interrupt is effective 0: The Interrupt is ineffective
0x17	Interrupt_MASK1	W/R	7:0		0x00	Mask of interrupts defined in reg0x14 1: The Interrupt is effective 0: The Interrupt is ineffective
0x18	Interrupt_MASK2	W/R	7	Clr_HDCP_int	0	1:Clear interrupts generated by HDCP authenticate start and done
			5:0		0x00	Mask of interrupts defined in reg0x15 1: The Interrupt is effective 0: The Interrupt is ineffective 1:Clear interrupts generated by HDCP signals
0x19	Interrupt_ctr	W/R	7	Clr_SetMute_int	0	1:Clear interrupts generated by set mute packet
			6	Clr_LeftMute_int	0	1:Clear interrupts generated by left mute packet
			5	IntrOutType	1	Interrupt pin output type 1:open drain 0:push pull
			4	IntPol	1	Interrupt pin output polarity 1:low active 0:high active
			3	Clr_Audio_int	0	1:Clear interrupts generated by Audio FIFO error
			2	Clr_ECC_int	0	1:Clear interrupts generated by ECC error
			1	Clr_Pkt_int	0	1:Clear interrupts generated by Packet signals
			0	Clr_Mode_int	0	1:Clear interrupts generated by mode change
0x1A	Misc_ctrl	W/R	7	reserved	0	
			6	reserved	0	
			5	reserved	0	
			4	Timeout_en	1	1:auto timeout when no DE detected
			3	reserved	0	
			2	SelDebugHL	1	1:For Debug signals selecting
			1	Vsync_Out_pol	0	Vsync output polarity 0: Negitave 1: Positive
			0	Hsync_Out_pol	0	Hsync output polarity 0: Negitave 1: Positive
0x1B	Video_map	W/R	7	Reserve	0	Reserve
			6	chSyncpol	0	Video output data configuration, refer the datasheet and programming guide. 1: output sync signal polarity from Reg1A[1:0] 0: output sync signal polarity as the input.
			5	Swap_O16b	0	1: when output 16-bit video data format, the other 8 bits will be forced to low
			4	Swap_Ch422	0	Channel Swap used in YUV422 mode. 0:Cr/Cb assigned to Data[23:16] 1:Cr/Cb assigned to Data[7:0]
			3	Swap_OutRB	0	1: swap output channel 0 and channel 2
			2	Swap_ML	0	1: swap output direction(MSB/LSB)
			1	Swap_Pol	0	1: swap input data polarity
			0	Swap_RB	0	1: swap input channel 0 and channel 2

0x1C	Video_Ctrl1	W/R	7	DNFreeGo	0	'1': Dither Noise Pattern Select
			6	SyncEmb	0	'1': Sync Embedded output
			5	EN_Dither	0	'1': Enable dither function
			4	EnUdFilt	0	'1': Enable color up/down filter
			3	OutDDR	0	'1': Double data rate output
			2	2x656CLK	0	'1': CCIR6565 output
			1	656FFRst	0	'1': CCIR656 Output FIFO reset
			0	EnAVMuteRst	0	'1': Enable Output FIFO reset when AVMUTE is set.
0x1D	Vclk_Ctrl	W/R	5	Vclkb_inv	0x30	'1': Invert internal video clock phase
			4	Vclk_inv		'1': Invert video output clock phase
			3:2	VclkbDly		Fine tune internal video clock delay (1ns for 1 step)
			1:0	VclkDly		Fine tune video output clock delay. (1ns for 1 step)
0x1E	I2CIO_Ctrl	W/R	7	DSda_Slew	0xDA	Slew rate of command I2C pins: 0:Fast ; 1:Slow
			6	DDCSda_Slew		Slew rate of HDCP I2C pins: 0:Fast ; 1:Slow
			5:4	RomI2C_ST		Current strength of ROM I2C pins: 00:4mA ; 01:8mA ; 10:12mA;11:16mA;
			3:2	DataI2C_ST		Current strength of command I2C pins: 00:4mA ; 01:8mA ; 10:12mA;11:16mA;
			1:0	DDC_ST		Current strength of HDCP I2C pins: 00:4mA ; 01:8mA ; 10:12mA;11:16mA;
0x1F	RegPktFlag_ctrl	W/R	4	ACP	0	0: interrupt only when first receiving or a new value is updated
			3	SPD	0	
			2	Audio	0	1: interrupt each time a packet is received
			1	MPEG	0	
			0	AVI	0	
0x20	CSC_CTRL	W/R	7	VDGatting	0	Enable output data gating to zero when no Video display.
			6	VDIOLDisable	0	Disable video low bits data(D3~D0)
			5	EN_TriVDIO	0	1: Enable Tristate Video Data Only 0: Tristate Video Data with Video Sync
			4	ForceColMod	0	0: Input color mode auto detect 1: Force input color mode as bit[3:2] setting
			3:2	**ColMod_Set**	00	**Input color mode set** **00: RGB mode** **01: YUV422 mode** **10: YUV444 mode**
			1:0	**CSCSel**	00	**00: no color space change (bypass)** **10: RGB to YUV** **11: YUV to RGB**
0x21	CSC_YOFF	W/R	7:0		0x10	Color Space conversion parameters matrix tables, refer the programming guide Y blank level
0x22	CSC_COFF	W/R	7:0		0x80	C blank level
0x23	CSC_RGBOFF	W/R	7:0		0x00	R/G/B blank level
0x24	CSC_MTX11_L	W/R	7:0		0xb2	Color space conversion Matrix
0x25	CSC_MTX11_H	W/R	5:0		0x04	Color space conversion Matrix
0x26	CSC_MTX12_L	W/R	7:0		0x64	Color space conversion Matrix
0x27	CSC_MTX12_H	W/R	5:0		0x02	Color space conversion Matrix
0x28	CSC_MTX13_L	W/R	7:0		0xE9	Color space conversion Matrix
0x29	CSC_MTX13_H	W/R	5:0		0x00	Color space conversion Matrix

0x2A	CSC_MTX21_L	W/R	7:0		0x93	Color space conversion Matrix
0x2B	CSC_MTX21_H	W/R	5:0		0x1c	Color space conversion Matrix
0x2C	CSC_MTX22_L	W/R	7:0		0x16	Color space conversion Matrix
0x2D	CSC_MTX22_H	W/R	5:0		0x04	Color space conversion Matrix
0x2E	CSC_MTX23_L	W/R	7:0		0x56	Color space conversion Matrix
0x2F	CSC_MTX23_H	W/R	5:0		0x1F	Color space conversion Matrix
0x30	CSC_MTX31_L	W/R	7:0		0x49	Color space conversion Matrix
0x31	CSC_MTX31_H	W/R	5:0		0x1D	Color space conversion Matrix
0x32	CSC_MTX32_L	W/R	7:0		0x9f	Color space conversion Matrix
0x33	CSC_MTX32_H	W/R	5:0		0x1E	Color space conversion Matrix
0x34	CSC_MTX33_L	W/R	7:0		0x16	Color space conversion Matrix
0x35	CSC_MTX33_H	W/R	5:0		0x04	Color space conversion Matrix
0x3B	Deskew Setting		7:0	Deskew setting, suggestion value is 0x40.	0x00	Suggest Initial Value: 0x40
0x3C	reserve	W/R	7		0	
	reserve	W/R	6		0	
	reserve	W/R	5		0	
	reserve	W/R	4		0	
	reserve	W/R	3		0	
	DE_Bypass	R/W	2	DE Bypass	0	**0: DE regenerated** **1: DE bypassed from TMDS input.**
	reserve	W/R	1		0	
	reserve	W/R	0		0	
0x3D	PG_CTRL2	W/R	**7:6**	**OutColMod**	10	**Output color mode** **00: RGB** **01:YUV422** **10:YUV444**
				reserved	00	
				reserved	00	
				reserved	00	
0x56	CDR Setting		0	CDR setting	0	should set as ‘1’
0x58	Vid_mode	RO	3 2 1 0	PxVideoStable vidfield vidinterlacemode VidModeChg		Indicate if video signal is stable Video field number in interlaced mode Indicate video is in interlaced mode Indicate if a video mode change occurs
0x59	Vid_HTotal_L	RO	7:0			The total pixel count of a line [7:0]
0x5A	Vid_HTotal_H	RO	7:4 3:0	Vid_HAct[11:8] Vid_Htotal[11:8]		The active pixel count of a line[11:8] The total pixel count of a line [11:8]
0x5B	Vid_HAct_L	RO	7:4	Vid_HAct[7:0]		The active pixel count of a line[7:0]
0x5C	Vid_Hsync_Wid_L	RO	7:4	Vid_Hsync_Wid[7:0]		The width of Hsync [7:0]
0x5D	Vid_HSync_Wid_H	RO	7:4 3:0	Vid_H_Ft_Porch[11:8] Vid_Hsync_Wid[11:8]		The width of Hsync front porch [11:8] The width of Hsync [11:8]
0x5E	Vid_H_Ft_Porch_L	RO	7:0	Vid_H_Ft_Porch[7:0]		The width of Hsync front porch [7:0]
0x5F	Vid_VTotal_L	RO	7:0	Vid_VTotal[7:0]		The total line count of a field [7:0]
0x60	Vid_VTotal_H	RO	7:4 3:0	Vid_Vact[11:8] Vid_Vtotal[11:8]		The active line count of a field [11:8] The total line count of a field [11:8]
0x61	Vid_Vact_L	RO	7:0	Vid_Vact[7:0]		The active line count of a field [7:0]
0x62	Vid_Vsync2DE	RO	7:0	Video sync to DE[7:0]		The width of vsync back porch
0x63	Vid_V_Ft_Porch	RO	7:0	Vid_V_Ft_Porch[7:0]		The width of vsync front porch
0x64	Vid_pixel_CNT	RO	7:0			Count of crystal clock on each 128 pixels
0x65	Vid_input_st	RO	7:4 3	Pix_rep HDCP_DISABLE		Video input status 0000 : no repetition 0001: pixel sent 2 times 0011: pixel sent 4 times HDCP Disable: 1: HDCP Disabled 0: HDCP no activated or enabled

			2 1 0	Avmute Vsync_in_po Hsync_in_po		1: HDMI is in Avmute state Vsync input polarity 0: Negative Polarity 1: Positive Polarity Hsync input polarity 0: Negative Polarity 1: Positive Polarity
68	PLL_Ctrl	W/R	7 6 5 4 3 2 1 0	RXPLL_ENI1 RXPLL_ENI0B RXPLL_ER1 RXPLL_ENFC RXPLL_DEI RXPLL_GAIN RXPLL_EC1 RXPLL_ER0	0x04	SelPXCK: 0: Default select locked clock to core 1: select unlocked clock
6B	CCtrl	W/R	7:6 5:4 3:1 0	DATA_RXAMP CLK_RXAMP CCTRL_SEL ENCCTRL_REF	0x10	EnCCTRL_REF: default disable manually set CCTRL
6C	Equal_Ctrl2	W/R	7:6 5 4 3:0	VCMSEL VSETRH VSETRL EQ_ZR	0x03	
0x73	HDCP_Ctrl	W/R	7 6 5 4	Enable repeater KSV ready Enable feature 1.1 enable fast authentication	0x20	Enable repeater function Set KSV ready when CAT6023 is reapeter Enable HDCP 1.1 feature Enable fast authetication
0x75	I2S_Ctrl	W/R	7	Ws_sel	0	1:invert channel A and channel B select
			6:2	I2S_Width	1100 0	I2S word length, only effective in right justified mode; Maximum value is 24 means of 24 bits, value is the length of word length
			1:0	**I2S_Mode**	00	**I2S output mode:** **00:32 bit I2S left justified mode, 1T delay** **01:32 bit I2S right justified mode** **10:32 bit I2S left justified mode, 0T delay** **11:undefined**
0x76	I2S_Map	W/R	7:6	I2S_Ch3Sel	11	I2S channel 6 and channel 7 map: 00: map to HDMI channel 0 and channel 1 01: map to HDMI channel 2 and channel 3 10: map to HDMI channel 4 and channel 5 11: map to HDMI channel 6 and channel 7
			5:4	I2S_Ch2Sel	10	I2S channel 4 and channel 5 map: 00: map to HDMI channel 0 and channel 1 01: map to HDMI channel 2 and channel 3 10: map to HDMI channel 4 and channel 5 11: map to HDMI channel 6 and channel 7
			3:2	I2S_Ch1Sel	01	I2S channel 2 and channel 3 map: 00: map to HDMI channel 0 and channel 1 01: map to HDMI channel 2 and channel 3 10: map to HDMI channel 4 and channel 5 11: map to HDMI channel 6 and channel 7
			1:0	I2S_Ch0Sel	00	I2S channel 0 and channel 1 map: 00: map to HDMI channel 0 and channel 1 01: map to HDMI channel 2 and channel 3 10: map to HDMI channel 4 and channel 5 11: map to HDMI channel 6 and channel 7
0x77	Audio_Ctrl	W/R	7	Reg_Audck_BBen	0	1: Enable NLPCM audio output from I2S channel

			6	Force_FS	0	1: Force Audio FS mode 0: Audio FS from decode
			5	Reserved	1	
			4	Aud_info_force	0	Force Audio setting from Aud info frame
			3	Avmute_value	0	Avmute value when software Avmute is enabled
			2	Force_avmute	0	1: Software forced-Avmute mode
			1	Dis_vdo_mute	0	1: Disable Video mute
			0	Dis_aud_mute	0	1: Disable Audio mute
0x78	MCLK_Ctrl	W/R	7	OSC_En	1	1:use crystal clock input as audio PLL reference 0:use pixel clock as audio PLL reference
			6	**OSCSel**	1	**1:selected when crystal is of 27MHz**
			4	Force_CTS	0	Software force to set CTS value
			3	Force_CTSMODE	0	use CTS for audio FIFO adjustment
			2:0	Mclksel	001	Mclk output clock multiple number 000:128FS ;001:256FS; 010:384FS ;011:512FS; 100:640FS ;101:768FS; 110:894FS ;111:1024FS;
0x7E	Aud_Jitter_CTRL	W/R	6:4	AUD_JIT_CTRL	000	suggestion setting as '111'
	FS_SET	W/R	3:0	FS_SET	0010	Software set sampling frequency 0000:44.1KHz; 0010:48KHz; 0011:32 KHz; 1000:88.2KHz; 1010:96 KHz; 1100:176.4KHz; 1110:192KHz available only reg77[6] = '1'
0x7F	N_Rcv1	RO	7:0	N_DEC[7:0]		Audio N parameter decoder value [7:0]
0x80	N_Rcv2	RO	7:0	N_DEC[15:8]		Audio N parameter decoder value [15:8]
0x81	N_Rcv3	RO	7:4 3:0	CTS_DEC[3:0] N_DEC[19:16]		Audio CTS parameter decoder value [3:0] Audio N parameter decoder value [19:6]
0x82	CTS_Rcv2	RO	7:0	CTS_DEC[11:4]		Audio CTS parameter decoder value [11:4]
0x83	CTS_Rcv3	RO	7:0	CTS_DEC[19:12]		Audio CTS parameter decoder value [19:12]
0x84	CD	RO	7:4	GCP_CD		Color depth decoder value in GCP 0: default (24bits) 4: 24bits 5: 30bits 6: 36bits 7: 48bits
	FS	RO	3:0	F_DEC		Audio FS(sample Freq.) decoder value 0000:44.1KHz; 0010:48KHz; 0011:32 KHz; 1000:88.2KHz; 1010:96 KHz; 1100:176.4KHz; 1110:192KHz
0x85	Channel_Err	RO	7 6 5:4 3:2 1:0	Pkt_2berr Pkt_1berr CH2_Err CH1_Err CH0_Err		2-bit BCH error is detected and packet is discarded a 1-bit BCH error is detected and automatically corrected a decode error is detected on channel 2 a decode error is detected on channel 1 a decode error is detected on channel 0
0x87	HWMute_Ctrl	W/R	6 5 4 3	HWForceMute HWAudFFMuteClr HWMuteClr HWMuteEn	0 0 0 1	HWForceMute: 0: mute control by channel status 1: mute anyway 1: FIFO mute clear 1: Clear H/W mute 1: H/W Mute enable

			2:0	reserve	000	
0x89	TriState_Ctrl	W/R	7	DisVAutomute	0x80	'1': Video output Auto Mute Disable
			6	Tri_VDIO		'1': tristate video Data output buffer
			5	Tri_VIO		'1': tristate video Control output buffer
			4	Tri_SPDIF		'1': tristate Audio SPDIF output buffer
			3	Tri_I2S3		'1': tristate Audio I2S3 output buffer
			2	Tri_I2S2		'1': tristate Audio I2S2 output buffer
			1	Tri_I2S1		'1': tristate Audio I2S1 output buffer
			0	Tri_I2S0		'1': tristate Audio I2S0 output buffer
0x8A	Audio_chanSt	RO				Audio received status
			7	Audio_on		'1': Audio is ON
			6	HBRAudio		'1': Audio type is High Bit rate
			5	DSDAudio		'1': Audio type is DSD
			4	Audio_layout		'1': Audio layout is 1 or 0
			3	Audio_src3_valid		'1': HDMI Audio source 3 valid Flag
			2	Audio_src2_valid		'1': HDMI Audio source 2 valid Flag
			1	Audio_src1_valid		'1': HDMI Audio source 1 valid Flag
			0	Audio_src0_valid		'1': HDMI Audio source 0 valid Flag
0x8B	Interrupt3	RO	7	CLKCHG_DET		'1': Rx clock change detect Int
			6	rxckon_Det		'1': Rx clock on detect Int
			5	HDCPoff_det		'1': HDCP off detect Int
			4	Symerr_det		'1': CDR symbol error detect Int
			3	CD_det		'1': Color Depth change Int
			2	Genpkt_det		'1': Genaral packet detect Int
			1	ISRC2_Det		'1': ISRC2 packet detect Int
			0	ISRC1_Det		'1': ISRC1 packet detect Int
0x8C	Int_mask3	W/R				Mask of interrupts defined in reg0x8B 1: The Interrupt is effective 0: The Interrupt is ineffective
0x8E	Pkt_type_H	RO	7:4	Pkt_type_H		Received packet type high bits
	Ori_sampF		3:0	Ori_sampF		Original sampling frequency 1111:44.1KHz; 1101:48KHz; 1100:32 KHz; 0111:88.2KHz; 0101:96 KHz; 0011:176.4KHz; 0001:192KHz
0x92	Rdrom_status	RO				If this byte is not 9 in normal operation, reading ROM failed.
			3	RomDecValid		'1' : ROM data decode valid
			2	RomDecFail		'1' : ROM data decode fail
			1	RomAcq_NoAck		'1' : No ACK received when access ROM
			0	RomAcq_done		'1' : Acquire ROM data done
93		W/R	7:0		0x03	For revised loop this byte should be set to 0x43
			7	EN_RVD	0	When '1' Vrctrl of the 1st EQ block is set to vdd.
			6	EN_RVS	0	When '1' Vrctrl of the 1st EQ block is set to vss.
			5	DR0_1ST	0	DR0 of the 1st EQ block.
			4	REG_AFEDR0(moved from reg56(5))	0	
			3:0	ZR_1ST	0011	ZR of the 1st EQ block
94		W/R	7:0		0x60	When using revised loop, this byte should be set to 0x1f
			7	rsvd		
			6	SAME_ZR	1	1:ZR_1ST=ZR 0:ZR_1ST=REG_ZR_1ST
			5	EN_RCTRL	1	1: Enable Rctrl of the 1st EQ block

						0: R of the 1st EQ block depends on EN_RVD, EN_RVS (and on DER_1st)
			4	LOOP_MUX	0	When ‘0’,use prior loop version(A1,T1) When ‘1’ the revised loop is adopted
			3:0	DER_1st	0000	Registers to decrease the value of resister at the source node of amplifier in the clock channel.
95		W/R	7:0		0x8f	Suggest Default value: 0x87
			7	REG_FILTCKCHG	1	
			6	EQK_RLSBIN	0	Register of the LSB value when manually setting EQK_RIN
			5:0	EQK_RIN	001111	Registers to manually control dc gain of clock and data channels
96		W/R	5	REGPWD_COMP	1	1: power down the comparing circuit for DFIX mode 0: comparing circuit of selected port works
			4	Reg_DFIX_CFIX	1	1: Fix C to Register value in DFIX mode
			3	EQK_DATASEL	0	‘0’:RDATA are the same as RCLK when RLSB=’0’ ‘1’: possible codes of RDATA are limited to be 000000, 000011, 001101,010101, or 001111.
			2	REG_RSamp50K	0	When ‘0’, Vrctrl sampling frequency is Fosc/2^8=100KHz When’1’,the frequency is Fosc/2^9=50KHz
			1	EQK_AUTO_DIS	0	When’0’, RCLK[5:0] are decided automatically. When’1’,RCLK[5:0] are assigned manually.
			0	REG_DFIX	0	When ‘1’ ,dc gain is controlled by reg_r[5:0] When ‘0’ ,dc gain is controlled by loop
97	Reset Control	W/R	7	REG_PWDRXPLL2	0	
			6	REG_RSTRXPLL2	0	
			5	REG_RSTRXPLL	0	
			4	REG_ENHDCPOFF	0	
			3	REG_ENHDCPRST	0	
			2	REG_ENCKRST	0	
			1	REGEN_AutoVDORST	0	
			0	REGEN_AutoAUDRST	0	
0x9B	Backup_Regs	W/R	7 6 5 4	Force Romscl Forced Romscl value CLKRST_SEL HDCP_NOAVMUTE	0x00	1:Select clock from register setting 0:default. 1:clock set to 1. 0:clock set to 0. 1: force HDCP avmute=0
9C	Audio_Ch_status0	RO	7:6 5:3	‘00’ – mode 0 for following byte. Other – reserved. D[1] = 0 ‘000’ – 2 channel without pre-emphasis ‘001’ – 2 channel with 50μs/15μs pre-emphasis. ‘010’ – reserved ‘011’ – reserved D[1] = 1 ‘000’ – Default state for other		Audio Channel status decoder value [7:0]

			2 1 0	application than linear PCM. 0 - Software for copyright asserted. 1 - Software for no copyright is asserted. 0 – Audio word world represents linear PCM samples. 1 – Audio word used for other purpose 0		
9D	Audio_Ch_status1	RO		Category code.	0x00	Audio Channel status decoder value [15:8]
9E	Audio_Ch_status2	RO	7:4 3:0	Channel Number “0000” – Do not take into account. “0001” – 1 “0010” – 2 “0011” – 3 …. “1111” – 15 Source Number ‘0000’ – do not take into account ‘0001’ – left channel for stereo format ‘0010 – right channel for stereo format.		Audio Channel status decoder value [23:16]
9F	Audio_Ch_status3	RO	7:4 3:2 1:0	Sample Word Length reserved Clock accurance		Audio Channel status decoder value [35:28] Sample frequency is indicated in reg84[3:0]
0xA0	Pkt_type_L	RO				Received packet type low byte Pkt_type is cleared each time it’s read.
0xA1	BKSV0	RO				HDCP BKSV value readback [7:0]
0xA2	BKSV1	RO				HDCP BKSV value readback [15:8]
0xA3	BKSV2	RO				HDCP BKSV value readback [23:16]
0xA4	BKSV3	RO				HDCP BKSV value readback [31:24]
0xA5	BKSV4	RO				HDCP BKSV value readback [39:32]
0xA6	Pkt_ctrl	W/R	5	REG_GENPKT_HL	0	GenPkt registers latch data selector
			4	REG_ISRC2_HL	0	ISRC2 registers latch data selector
			3	newpkt_sel [3]	0	ISRC2 1: latch unsupport packet data 0: latch normal data
			2	newpkt_sel [2]	0	ISRC1
			1	newpkt_sel [1]	0	ACP
			0	newpkt_sel [0]	0	Generanl Packet
0xA7	Pkt_rec_typeH	W/R	7:0		0x0A	Decide which kind of packet to be recorded on General PKT registers.
0xA8	Pkt_rec_typeL	W/R	7:0		0x83	Decide which kind of packet to be fully recorded on General PKT registers.
0xA9	SRC_ver	RO				SPD infoFrame Version
0xAA	SRC_pb25	RO				SPD infoFrame Data Byte 25
0xAB	AVI_leng	RO				AVI infoFrame Length
0xAC	AVI_VER	RO				AVI infoFrame Version
0xAD	AVI_DB0	RO				AVI infoFrame Data Byte 0
0xAE	AVI_DB1	RO				AVI infoFrame Data Byte 1
0xAF	AVI_DB2	RO				AVI infoFrame Data Byte 2

0xB0	AVI_DB3	RO				AVI infoFrame Data Byte 3
0xB1	AVI_DB4	RO				AVI infoFrame Data Byte 4
0xB2	AVI_DB5	RO				AVI infoFrame Data Byte 5
0xB3	AVI_DB6	RO				AVI infoFrame Data Byte 6
0xB4	AVI_DB7	RO				AVI infoFrame Data Byte 7
0xB5	AVI_DB8	RO				AVI infoFrame Data Byte 8
0xB6	AVI_DB9	RO				AVI infoFrame Data Byte 9
0xB7	AVI_DB10	RO				AVI infoFrame Data Byte 10
0xB8	AVI_DB11	RO				AVI infoFrame Data Byte 11
0xB9	AVI_DB12	RO				AVI infoFrame Data Byte 12
0xBA	AVI_DB13	RO				AVI infoFrame Data Byte 13
0xBB	AVI_DB14	RO				AVI infoFrame Data Byte 14
0xBC	AVI_DB15	RO				AVI infoFrame Data Byte 15
0xBD	GENPKT_HB0	RO				This is a general-purpose register recording one kind of the packets. RegA8 is the recorder header to catch. Genaral Packet Header Byte 0
0xBE	GENPKT_HB1	RO				Genaral Packet Header Byte 1
0xBF	GENPKT_HB2	RO				Genaral Packet Header Byte 2
0xC0	GENPKT_DB0	RO				Genaral Packet Data Byte 0
0xC1	GENPKT_DB1	RO				Genaral Packet Data Byte 1
0xC2	GENPKT_DB2	RO				Genaral Packet Data Byte 2
0xC3	GENPKT_DB3	RO				Genaral Packet Data Byte 3
0xC4	GENPKT_DB4	RO				Genaral Packet Data Byte 4
0xC5	GENPKT_DB5	RO				Genaral Packet Data Byte 5
0xC6	GENPKT_DB6	RO				Genaral Packet Data Byte 6
0xC7	GENPKT_DB7	RO				Genaral Packet Data Byte 7
0xC8	GENPKT_DB8	RO				Genaral Packet Data Byte 8
0xC9	GENPKT_DB9	RO				Genaral Packet Data Byte 9
0xCA	GENPKT_DB10	RO				Genaral Packet Data Byte 10
0xCB	GENPKT_DB11	RO				Genaral Packet Data Byte 11
0xCC	GENPKT_DB12	RO				Genaral Packet Data Byte 12
0xCD	GENPKT_DB13	RO				Genaral Packet Data Byte 13
0xCE	GENPKT_DB14	RO				Genaral Packet Data Byte 14
0xCF	GENPKT_DB15	RO				Genaral Packet Data Byte 15
0xD0	GENPKT_DB16	RO				Genaral Packet Data Byte 16
0xD1	GENPKT_DB17	RO				Genaral Packet Data Byte 17
0xD2	GENPKT_DB18	RO				Genaral Packet Data Byte 18
0xD3	GENPKT_DB19	RO				Genaral Packet Data Byte 19
0xD4	GENPKT_DB20	RO				Genaral Packet Data Byte 20
0xD5	GENPKT_DB21	RO				Genaral Packet Data Byte 21
0xD6	GENPKT_DB22	RO				Genaral Packet Data Byte 22
0xD7	GENPKT_DB23	RO				Genaral Packet Data Byte 23
0xD8	GENPKT_DB24	RO				Genaral Packet Data Byte 24
0xD9	GENPKT_DB25	RO				Genaral Packet Data Byte 25
0xDA	GENPKT_DB26	RO				Genaral Packet Data Byte 26
0xDB	GENPKT_DB27	RO				Genaral Packet Data Byte 27
0xDC	Audio_Ver	RO				Audio infoFrame Version
0xDD	Audio_DB0	RO				Audio infoFrame Data Byte 0
0xDE	Audio_DB1	RO				Audio infoFrame Data Byte 1
0xDF	Audio_DB2	RO				Audio infoFrame Data Byte 2
0xE0	Audio_DB3	RO				Audio infoFrame Data Byte 3
0xE1	Audio_DB4	RO				Audio infoFrame Data Byte 4
0xE2	Audio_DB5	RO				Audio infoFrame Data Byte 5
0xE3	Audio_leng	RO				Audio infoFrame Length
0xE4	MPEG_Ver	RO				MPEG infoFrame Version
0xE5	MPEG_leng	RO				MPEG infoFrame Length
0xE6	MPEG_DB0	RO				MPEG infoFrame Data Byte 0

0xE7	MPEG_DB1	RO				MPEG infoFrame Data Byte 1
0xE8	MPEG_DB2	RO				MPEG infoFrame Data Byte 2
0xE9	MPEG_DB3	RO				MPEG infoFrame Data Byte 3
0xEA	MPEG_DB4	RO				MPEG infoFrame Data Byte 4
0xEB	MPEG_DB5	RO				MPEG infoFrame Data Byte 5
0xEC	ACP_HB0	RO				ACP packet Header Byte 0
0xED	ACP_HB1	RO				ACP packet Header Byte 1
0xEE	ACP_HB2	RO				ACP packet Header Byte 2
0xEF	ACP_DB0	RO				ACP packet Data Byte 0
0xF0	ACP_DB1	RO				ACP packet Data Byte 1
0xF1	ACP_DB2	RO				ACP packet Data Byte 2
0xF2	ACP_DB3	RO				ACP packet Data Byte 3
0xF3	ACP_DB4	RO				ACP packet Data Byte 4
0xF4	ACP_DB5	RO				ACP packet Data Byte 5
0xF5	ACP_DB6	RO				ACP packet Data Byte 6
0xF6	ACP_DB7	RO				ACP packet Data Byte 7
0xF7	ACP_DB8	RO				ACP packet Data Byte 8
0xF8	ACP_DB9	RO				ACP packet Data Byte 9
0xF9	ACP_DB10	RO				ACP packet Data Byte 10
0xFA	ACP_DB11	RO				ACP packet Data Byte 11
0xFB	ACP_DB12	RO				ACP packet Data Byte 12
0xFC	ACP_DB13	RO				ACP packet Data Byte 13
0xFD	ACP_DB14	RO				ACP packet Data Byte 14
0xFE	ACP_DB15	RO				ACP packet Data Byte 15
0xFF	ACP_rec_type	W/R	7:0		0x04	The packet type will be stored to ACP register

Block2 (reg0F[0] = '1')

Reg Offset	Reg_Name	W/R	Bits	Status	Default	Description
0x80	KSV_FIFO40	W/R			0x00	HDCP KSVFIFO4 [7:0]
0x81	KSV_FIFO41	W/R			0x00	HDCP KSVFIFO4 [15:8]
0x82	KSV_FIFO42	W/R			0x00	HDCP KSVFIFO4 [23:16]
0x83	KSV_FIFO43	W/R			0x00	HDCP KSVFIFO4 [31:24]
0x84	KSV_FIFO44	W/R			0x00	HDCP KSVFIFO4 [39:32]
0x85	KSV_FIFO50	W/R			0x00	HDCP KSVFIFO5 [7:0]
0x86	KSV_FIFO51	W/R			0x00	HDCP KSVFIFO5 [15:8]
0x87	KSV_FIFO52	W/R			0x00	HDCP KSVFIFO5 [23:16]
0x88	KSV_FIFO53	W/R			0x00	HDCP KSVFIFO5 [31:24]
0x89	KSV_FIFO54	W/R			0x00	HDCP KSVFIFO5 [39:32]
0x8A	KSV_FIFO60	W/R			0x00	HDCP KSVFIFO6 [7:0]
0x8B	KSV_FIFO61	W/R			0x00	HDCP KSVFIFO6 [15:8]
0x8C	KSV_FIFO62	W/R			0x00	HDCP KSVFIFO6 [23:16]
0x8D	KSV_FIFO63	W/R			0x00	HDCP KSVFIFO6 [31:24]
0x8E	KSV_FIFO64	W/R			0x00	HDCP KSVFIFO6 [39:32]
0x8F	KSV_FIFO70	W/R			0x00	HDCP KSVFIFO7 [7:0]
0x90	KSV_FIFO71	W/R			0x00	HDCP KSVFIFO7 [15:8]
0x91	KSV_FIFO72	W/R			0x00	HDCP KSVFIFO7 [23:16]
0x92	KSV_FIFO73	W/R			0x00	HDCP KSVFIFO7 [31:24]
0x93	KSV_FIFO74	W/R			0x00	HDCP KSVFIFO7 [39:32]
0x94	Pkt_type_maskL	W/R				Received packet type mask
0x95	Pkt_type_maskH	W/R	3:0			Received packet type mask
0xA0	ISRC1_HB0	RO				ISRC1 packet Header Byte 0
0xA1	ISRC1_HB1	RO				ISRC1 packet Header Byte 1
0xA2	ISRC1_HB2	RO				ISRC1 packet Header Byte 2
0xA3	ISRC1_DB0	RO				ISRC1 packet Data Byte 0
0xA4	ISRC1_DB1	RO				ISRC1 packet Data Byte 1
0xA5	ISRC1_DB2	RO				ISRC1 packet Data Byte 2
0xA6	ISRC1_DB3	RO				ISRC1 packet Data Byte 3
0xA7	ISRC1_DB4	RO				ISRC1 packet Data Byte 4
0xA8	ISRC1_DB5	RO				ISRC1 packet Data Byte 5
0xA9	ISRC1_DB6	RO				ISRC1 packet Data Byte 6
0xAA	ISRC1_DB7	RO				ISRC1 packet Data Byte 7
0xAB	ISRC1_DB8	RO				ISRC1 packet Data Byte 8
0xAC	ISRC1_DB9	RO				ISRC1 packet Data Byte 9
0xAD	ISRC1_DB10	RO				ISRC1 packet Data Byte 10
0xAE	ISRC1_DB11	RO				ISRC1 packet Data Byte 11
0xAF	ISRC1_DB12	RO				ISRC1 packet Data Byte 12
0xB0	ISRC1_DB13	RO				ISRC1 packet Data Byte 13
0xB1	ISRC1_DB14	RO				ISRC1 packet Data Byte 14
0xB2	ISRC1_DB15	RO				ISRC1 packet Data Byte 15
0xB3	ISRC1_rec_type	W/R			0x05	The packet type will be stored to ISRC1 register
0xB4	ISRC2_HB0	RO				ISRC2 packet Header Byte 0
0xB5	ISRC2_HB1	RO				ISRC2 packet Header Byte 1
0xB6	ISRC2_HB2	RO				ISRC2 packet Header Byte 2
0xB7	ISRC2_DB0	RO				ISRC2 packet Data Byte 0
0xB8	ISRC2_DB1	RO				ISRC2 packet Data Byte 1
0xB9	ISRC2_DB2	RO				ISRC2 packet Data Byte 2
0xBA	ISRC2_DB3	RO				ISRC2 packet Data Byte 3
0xBB	ISRC2_DB4	RO				ISRC2 packet Data Byte 4
0xBC	ISRC2_DB5	RO				ISRC2 packet Data Byte 5
0xBD	ISRC2_DB6	RO				ISRC2 packet Data Byte 6
0xBE	ISRC2_DB7	RO				ISRC2 packet Data Byte 7

0xBF	ISRC2_DB8	RO				ISRC2 packet Data Byte 8
0xC0	ISRC2_rec_type	W/R			0x06	The packet type will be stored to ISRC2 register
0xC1	KSV_FIFO00	W/R			0x00	HDCP KSVFIFO0 [7:0]
0xC2	KSV_FIFO01	W/R			0x00	HDCP KSVFIFO0 [15:8]
0xC3	KSV_FIFO02	W/R			0x00	HDCP KSVFIFO0 [23:16]
0xC4	KSV_FIFO03	W/R			0x00	HDCP KSVFIFO0 [31:24]
0xC5	KSV_FIFO04	W/R			0x00	HDCP KSVFIFO0 [39:32]
0xC6	KSV_FIFO10	W/R			0x00	HDCP KSVFIFO1 [7:0]
0xC7	KSV_FIFO11	W/R			0x00	HDCP KSVFIFO1 [15:8]
0xC8	KSV_FIFO12	W/R			0x00	HDCP KSVFIFO1 [23:16]
0xC9	KSV_FIFO13	W/R			0x00	HDCP KSVFIFO1 [31:24]
0xCA	KSV_FIFO14	W/R			0x00	HDCP KSVFIFO1 [39:32]
0xCB	KSV_FIFO20	W/R			0x00	HDCP KSVFIFO2 [7:0]
0xCC	KSV_FIFO21	W/R			0x00	HDCP KSVFIFO2 [15:8]
0xCD	KSV_FIFO22	W/R			0x00	HDCP KSVFIFO2 [23:16]
0xCE	KSV_FIFO23	W/R			0x00	HDCP KSVFIFO2 [31:24]
0xCF	KSV_FIFO24	W/R			0x00	HDCP KSVFIFO2 [39:32]
0xD0	KSV_FIFO30	W/R			0x00	HDCP KSVFIFO3 [7:0]
0xD1	KSV_FIFO31	W/R			0x00	HDCP KSVFIFO3 [15:8]
0xD2	KSV_FIFO32	W/R			0x00	HDCP KSVFIFO3 [23:16]
0xD3	KSV_FIFO33	W/R			0x00	HDCP KSVFIFO3 [31:24]
0xD4	KSV_FIFO34	W/R			0x00	HDCP KSVFIFO3 [39:32]
0xD5	BstatusL	W/R	7:0		0x00	HDCP BStatus[7:0]
0xD6	BstatusH	W/R	3:0		0x0	HDCP Bstatus[11:8] The HDCP BStatus[12] refer to HDMI status represented in Reg10[4].
0xD7	SHA1_H00	W/R			0x00	HDCP SHA1_H0 [7:0]
0xD8	SHA1_H01	W/R			0x00	HDCP SHA1_H0 [15:8]
0xD9	SHA1_H02	W/R			0x00	HDCP SHA1_H0 [23:16]
0xDA	SHA1_H03	W/R			0x00	HDCP SHA1_H0 [31:24]
0xDB	SHA1_H10	W/R			0x00	HDCP SHA1_H1 [7:0]
0xDC	SHA1_H11	W/R			0x00	HDCP SHA1_H1 [15:8]
0xDD	SHA1_H12	W/R			0x00	HDCP SHA1_H1 [23:16]
0xDE	SHA1_H13	W/R			0x00	HDCP SHA1_H1 [31:24]
0xDF	SHA1_H20	W/R			0x00	HDCP SHA1_H2 [7:0]
0xE0	SHA1_H21	W/R			0x00	HDCP SHA1_H2 [15:8]
0xE1	SHA1_H22	W/R			0x00	HDCP SHA1_H2 [23:16]
0xE2	SHA1_H23	W/R			0x00	HDCP SHA1_H2 [31:24]
0xE3	SHA1_H30	W/R			0x00	HDCP SHA1_H3 [7:0]
0xE4	SHA1_H31	W/R			0x00	HDCP SHA1_H3 [15:8]
0xE5	SHA1_H32	W/R			0x00	HDCP SHA1_H3 [23:16]
0xE6	SHA1_H33	W/R			0x00	HDCP SHA1_H3 [31:24]
0xE7	SHA1_H40	W/R			0x00	HDCP SHA1_H4 [7:0]
0xE8	SHA1_H41	W/R			0x00	HDCP SHA1_H4 [15:8]
0xE9	SHA1_H42	W/R			0x00	HDCP SHA1_H4 [23:16]
0xEA	SHA1_H43	W/R			0x00	HDCP SHA1_H4 [31:24]
0xEB	M0_B0	RO				HDCP Mi value readback [7:0]
0xEC	M0_B1	RO				HDCP Mi value readback [15:8]
0xED	M0_B2	RO				HDCP Mi value readback [23:16]
0xEE	M0_B3	RO				HDCP Mi value readback [31:24]
0xEF	M0_B4	RO				HDCP Mi value readback [39:32]
0xF0	M0_B5	RO				HDCP Mi value readback [47:40]
0xF1	M0_B6	RO				HDCP Mi value readback [55:48]
0xF2	M0_B7	RO				HDCP Mi value readback [63:56]