Indian Institute of Information Technology Sri City, Chittoor

Date: 10th April 2024

SCHEDULED QUIZ - III

Name of the Subject: **CA** Duration: 15 mins Max Marks: 10

Roll Number: _____ Section:_____

Answers(enter the options in the given table) :Q1

1	2	3	4	5	6	7	8	9	10

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1. What is the capacity of a disk with 3 platters, 15,000 cylinders, an average of 500 sectors per track, and 1,024 bytes per sector?
   a. 23.04GB b. 46.08GB c. 24.04GB d. 48.08GB

2. Match the following and choose the correct option

A. TLB	P. recently reference items likely to reference again
B. DRAM	Q. Items with nearby addresses tend to referenced
C. Temporal Locality	R. Main memory and frame buffers
D. SRAM	S. Used for address translations
	T. Cache Memory

   a. A-T, B-S, C-Q, D-R
   b. A-S, B-R,C-P, D-R
   c. A-S, B-R,C-P, D-T
   d. A-T, B-S, C-Q, D-T

3. Which type of cache miss occurs when multiple data objects map to the same cache block, leading to repeated misses?
   a. Compulsory miss
   b. Conflict miss
   c. Capacity miss
   d. Cold miss

4. Which of the following statements is/are correct in terms of Caller Saved?
   a. Caller saves temporary values in its frame before the call
   b. Callee saves temporary values in its frame before the call
   c. Caller saves permanent values in its RAM before the call
   d. None of the above

5. Which of the following statements is/are correct in terms of Callee Saved?
   a. Caller saves permanent values in its RAM before the call

b. Callee saves temporary values in its frame before using
c. Caller saves temporary values in its frame after the call
d. Both (a) and (b)

6. Between cache and main memory, the data is copied in _____ sized transfer units.
   a. Bits
   b. Bytes
   c. Block
   d. Cells

7. A larger cache will tend to_____ the hit rate.
   a. Decrease
   b. Increase
   c. No effect
   d. May increase or decrease

8. Determine the tag size for the given configuration.
   Main memory M = 16 bytes, B = 2 bytes/block, S = 4 sets, E = 1 block/set.
   a. 1
   b. 2
   c. 3
   d. 4

9. Assume register rax has the base address of the array char A[10]. Which of the following instruction has A[4] as the valid source operand?
   a. movq 4(%rax), %rdx
   b. movq (,%rax,4), %rdx
   c. movq 1(1,%rax,4), %rdx
   d. movq (4,%rax), %rdx

10. int arr [20]; For the given array declaration, what does the following machine operand represent: (%rdi, %rdx, 4). Assume rdi = arr and rdx = 3.
   a. arr[12]
   b. arr[3]
   c. arr[4]
   d. pointer error