DLD, End Term Exam

Indian Institute of Information Technology, Sri city, Chittoor, AP

(An Institute of National Importance)

Date: 8-Dec-2023 Time: 90 Mins Maximum Marks: 25 M

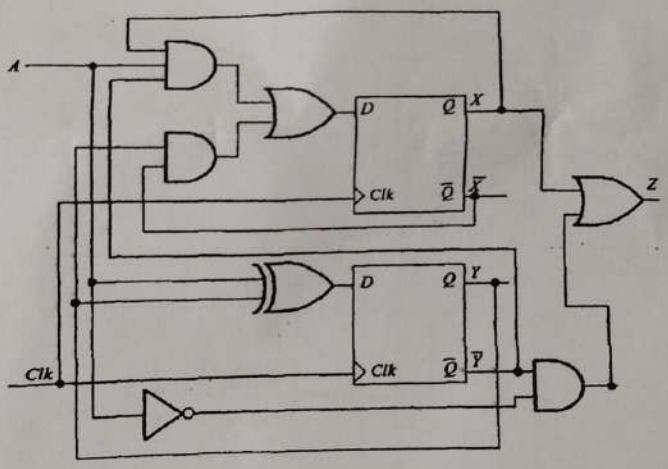
Instructions:

A. *All questions are compulsory. There is a internal choice for question 5.*
B. *Each question carries equal marks (5M).*
C. *Electronic gadgets including calculators are not allowed in the examination.*
D. *If required, consider the necessary assumptions.*
E. *It is compulsory to write the roll number and section number on the question paper.*
F. *Attach the question paper to the answer script.*

Roll Number..... ~~S20231015~~ S20230010153 Section: 2

1. Design an Asynchronous down counter that counts from 15 to 0 and then repeats itself.

2. Determine the state equation, state table, and draw the state diagram for the following sequential circuit. Assume that A and Z indicate the input and output, respectively.

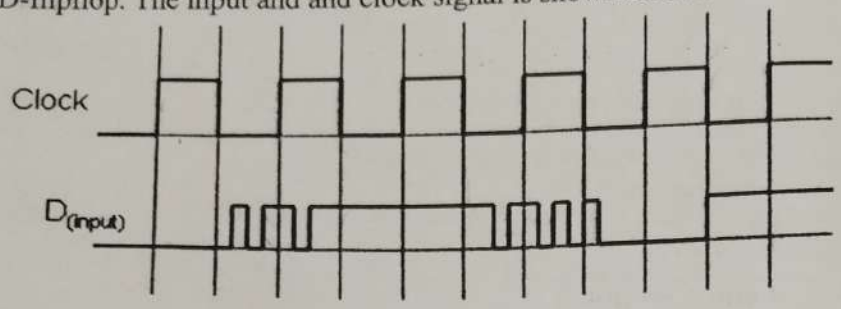


3. Design a mod-5 synchronous counter using T-flip flop.

(P.T.O)

4. a. Draw the state diagram of J-K flipflop and convert D Flipflop to J-K Flipflop (3M)

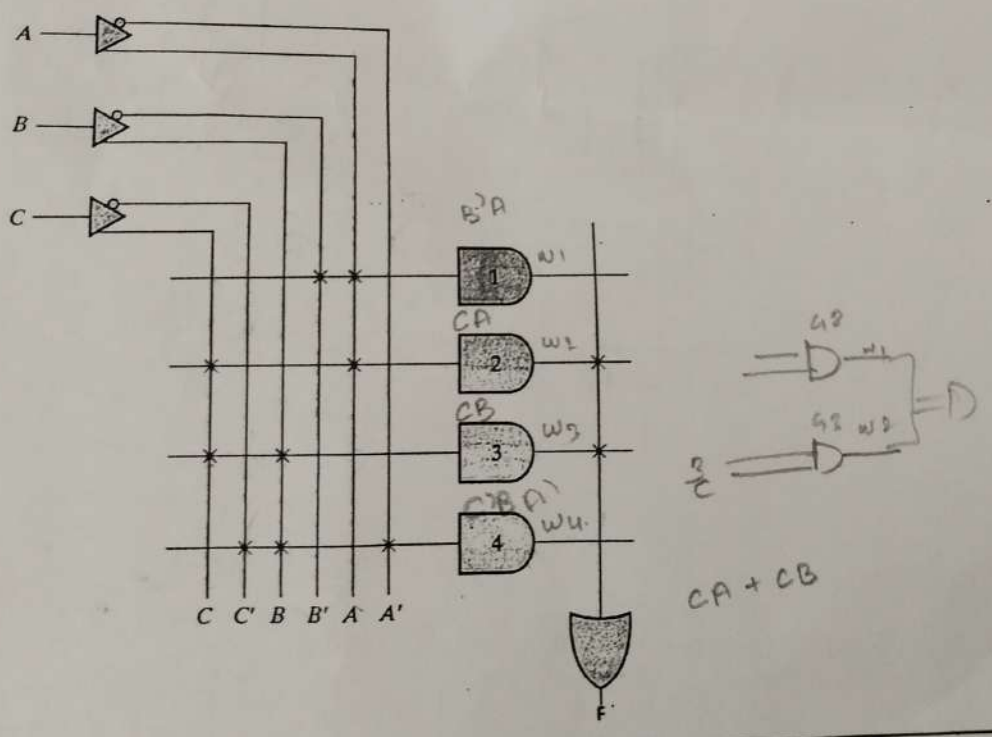
4.b. Draw the output waveform of a D-latch enable at positive level and positive edge triggered D-flipflop. The input and and clock signal is shown below. (2M)



5. Draw the circuit diagram of a 4-bit PISO register using D-FFs and explain the operation. (5M)

(or)

Write a Verilog HDL program to implement the following digital circuit where A, B and C are inputs and F denotes the output. (5M)



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