Digital Logic Design

Mid-2 Semester Exam

Indian Institute of Information Technology Sri City, Chittoor

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Date: 23/01/2023   Time 90 Mins   Maximum Marks 25M

Instructions

A. All questions are compulsory
B. Each question carries equal marks (5M).
C. If required, consider the necessary assumptions.

1. Simplify the Boolean function F1=P+Q using K-map and draw the circuits using NAND gates where $P = \Sigma(1,4,6,7,9,10,13,14)$,

$Q = \Sigma(2,3,8,9,13,14,15)$ **[5 M]**

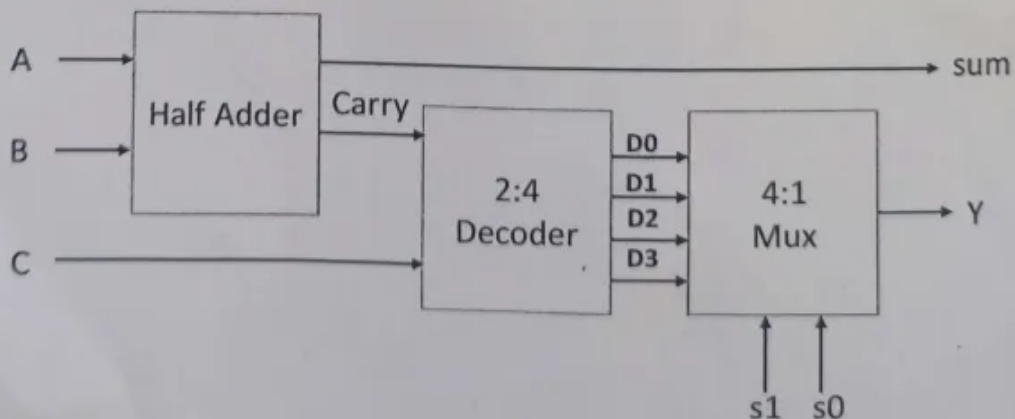2. Write the truth table of full subtractor and implement using Multiplexers.   **[5 M]**

3. Write truth table and the Boolean expressions for equal, greater and lesser of a 1-bit magnitude comparator and draw the circuit.   **[5 M]**

4. Write the Boolean expressions for all internal wires (carry, DO, D1, D2, D3) and outputs (Sum and Y).   **[5 M]**

5. Design 4-bit BCD adder assuming a 4-bit binary adder is available.   **[5 M]**