

👋 FOSDEM 2026 🎉

Open source firmware for high assurance confidential infrastructure

FOSDEM 2026 - Confidential Computing devroom

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Kudos

- Andrew Cooper - XenServer, Xen maintainer
- Demi Marie Obenour - Spectrum OS
- Paul Grimes - AMD
- Rich Persaud - Platform Security Summit
- Sid Hussmann - CTO & Co-Founder, Gapfruit
- Tim Ansell - wafer.space
- Zir Blazer - Dasharo Community Top Contributor



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- coreboot core developer
- Maintainer: Braswell, PC Engines, Protectli, MSI
- AMD OpenSIL contributor

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3mdeb Founder

- Open-source firmware evangelist
- Conference speaker and organizer
- OpenSecurityTraining2 Instructor

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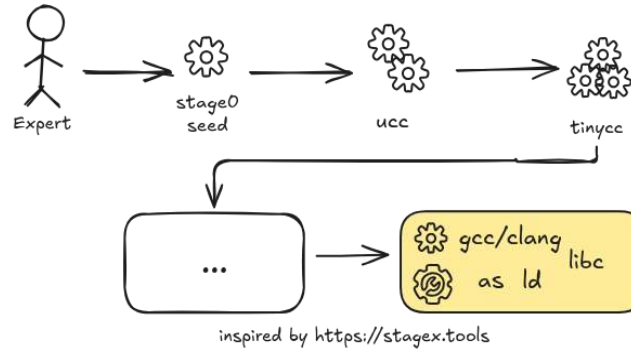
🐦 [@pietrushnic](https://twitter.com/pietrushnic) · 💻 [GitHub](https://github.com/pietrushnic)

What We Will Cover

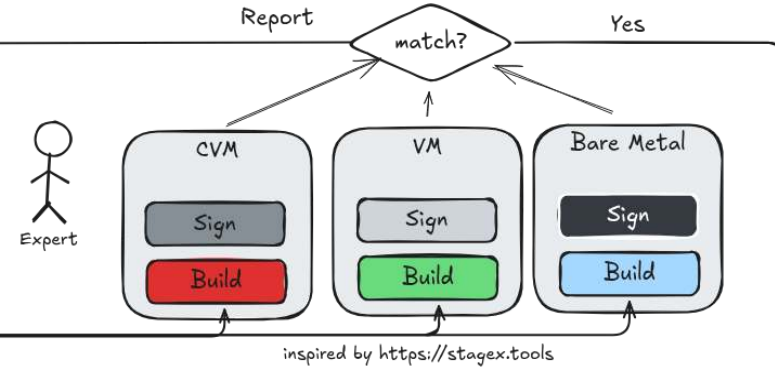
- Why do we need high assurance confidential infrastructure?
- High assurance architects have serious concerns about how responsibilities concentrate in various components of modern platforms
- Open-source firmware **complements** CC features to deliver together platform which helps grow open ecosystem in building such infrastructure
- Why home/SME environments matter:
 - Educational space for motivated engineers to build CC expertise
 - Open ecosystems thrive in home/SME as sovereign alternative
 - Retail hardware, not cloud unobtainium (RAMpocalypse pricing aside 📦)
- What we will show:
 - The firmware trust problem: who audits the foundation?
 - OpenSIL + coreboot on retail EPYC with SEV-SNP (live demo!)
 - Before/after: from proprietary to auditable stack

High Assurance Confidential Infrastructure 2026

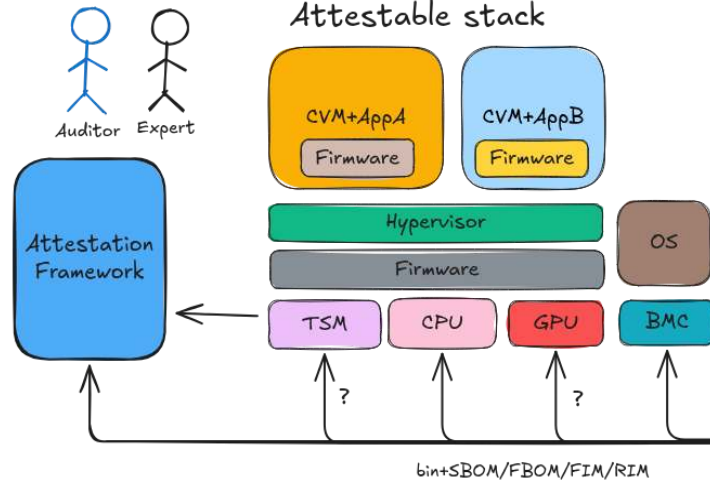
Bootstrappable toolchain



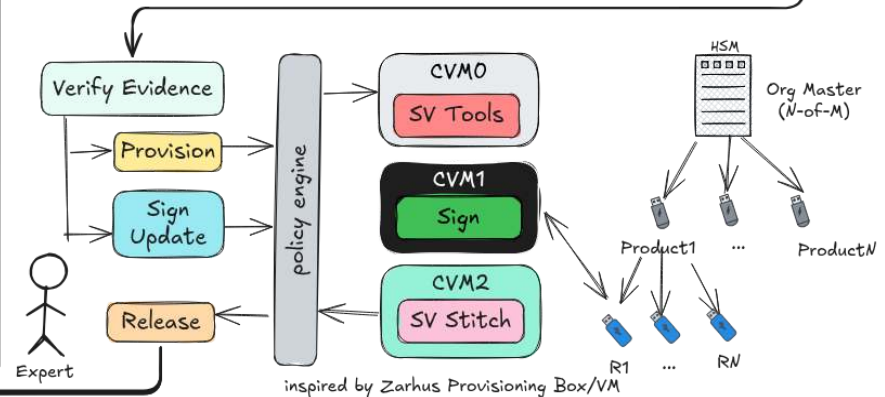
Distributed reproducibility quorum



Attestable stack



Owner-controlled RoT/CoT





tianocore



AMD openSIL



openSFI



Caliptra



opentitan



TrustedFirmware



OpenBMC

Firmware

- Era 1 (1975-1994): Proprietary
 - IBM BIOS → Phoenix
- Era 2 (1994-2014): Openness
 - LinuxBIOS, U-Boot
- Era 3 (2014+): Standardization
 - Intel FSP, openSIL, openSFI

Confidential Computing

- Era 1 (2015-2019): Proprietary
 - Intel SGX, AMD SEV
- Era 2 (2019+): Opening Up
 - IBM PEF, Keystone, ARM CCA
- Era 3 (2024+): Standardization
 - SEV-TIO, TDX, SPDM/IDE/TDISP

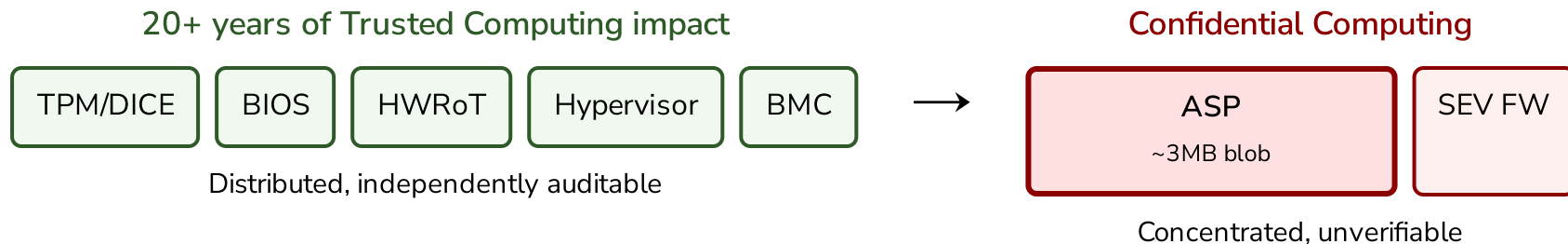
AMD SEV Evolution: A Decade of Iteration



Generation	Key Addition	Threat Addressed	CVEs
Naples (2017)	SME/SEV + SEV-ES	Cold boot, hypervisor introspection	n/a
Rome (2019)	GPA salting, ring buffer	Memory remapping attacks	n/a
Milan (2021)	SEV-SNP, RMP, attestation	Memory replay, integrity, aliasing	22
Genoa (2022)	SNP hardening, VLEK	SPL enforcement, CVE mitigation	28
Turin (2024+)	SEV-TIO (TDISP/SPDM)	Malicious PCIe/CXL devices	15+

CVE counts from AMD SEV firmware release notes analysis

The Firmware Trust Problem



- Intel ME history proves single co-processor concentration is risky
- BIOS reached openness (coreboot, openSIL) - ASP remains opaque ~3MB blob
- Years of boot chain transparency work at risk for centralized single point of failure
- AMD co-founded Caliptra (open RoT) yet ASP contradicts its principles

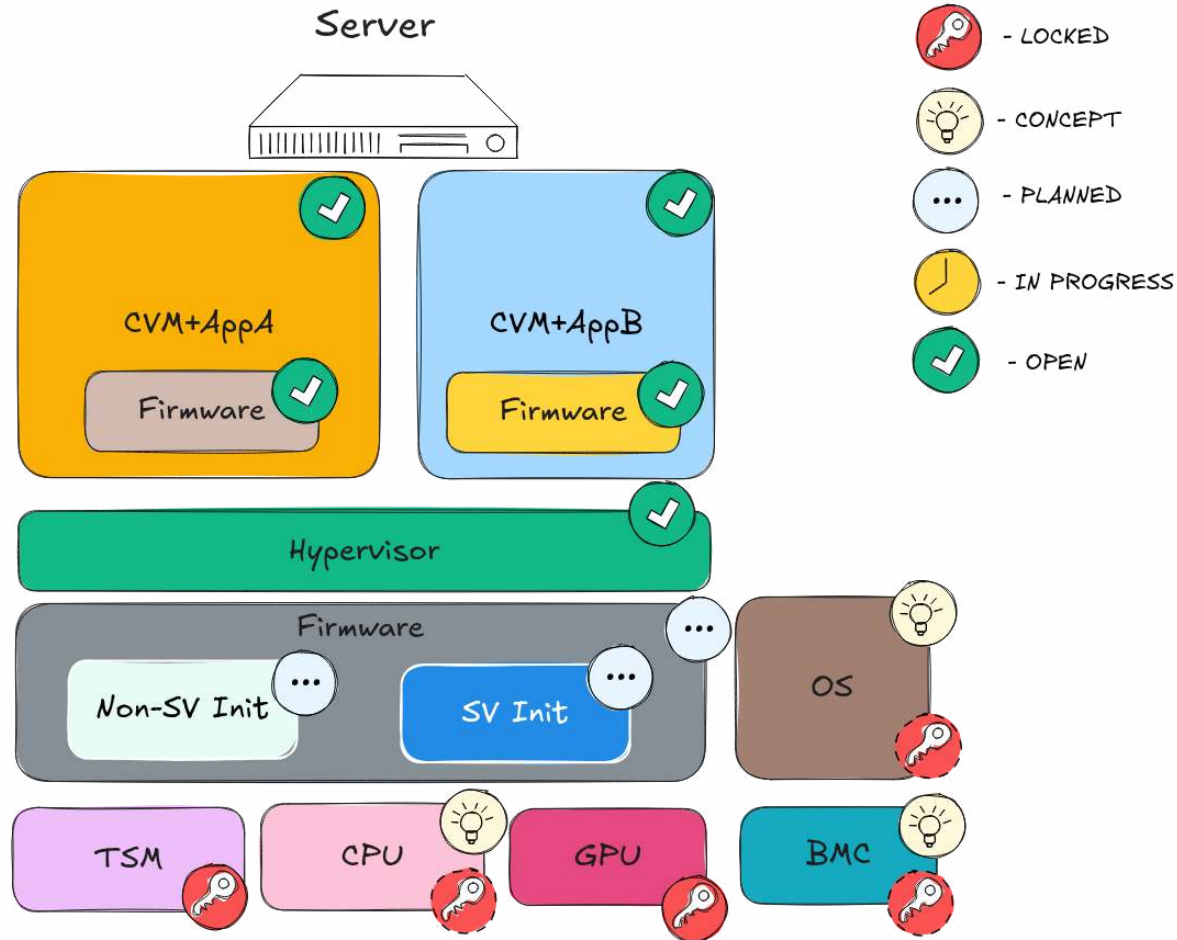
"Great security compromised by other great ideas ... starts to weaken its security posture ... want to keep it very clean."

Bryan Kelly (Microsoft), Caliptra architect — OCP 2022

The background is a dark gray with abstract, light gray lines in the corners that resemble circuit traces or a stylized grid. These lines are composed of straight segments connected at right angles, with some ending in small circular nodes. They are located in the top-left, top-right, and bottom-right corners, framing the central text.

What We Built

State of HACHI - FOSDEM'25



openSIL: Open Source Silicon Initialization

Approach	Source	Integration	Auditable
AGESA	Closed	UEFI-only	✗
Intel FSP	Binary blob	API mode (coreboot) / Dispatch (EDKII)	✗
openSIL	Full source	Static linking	✓

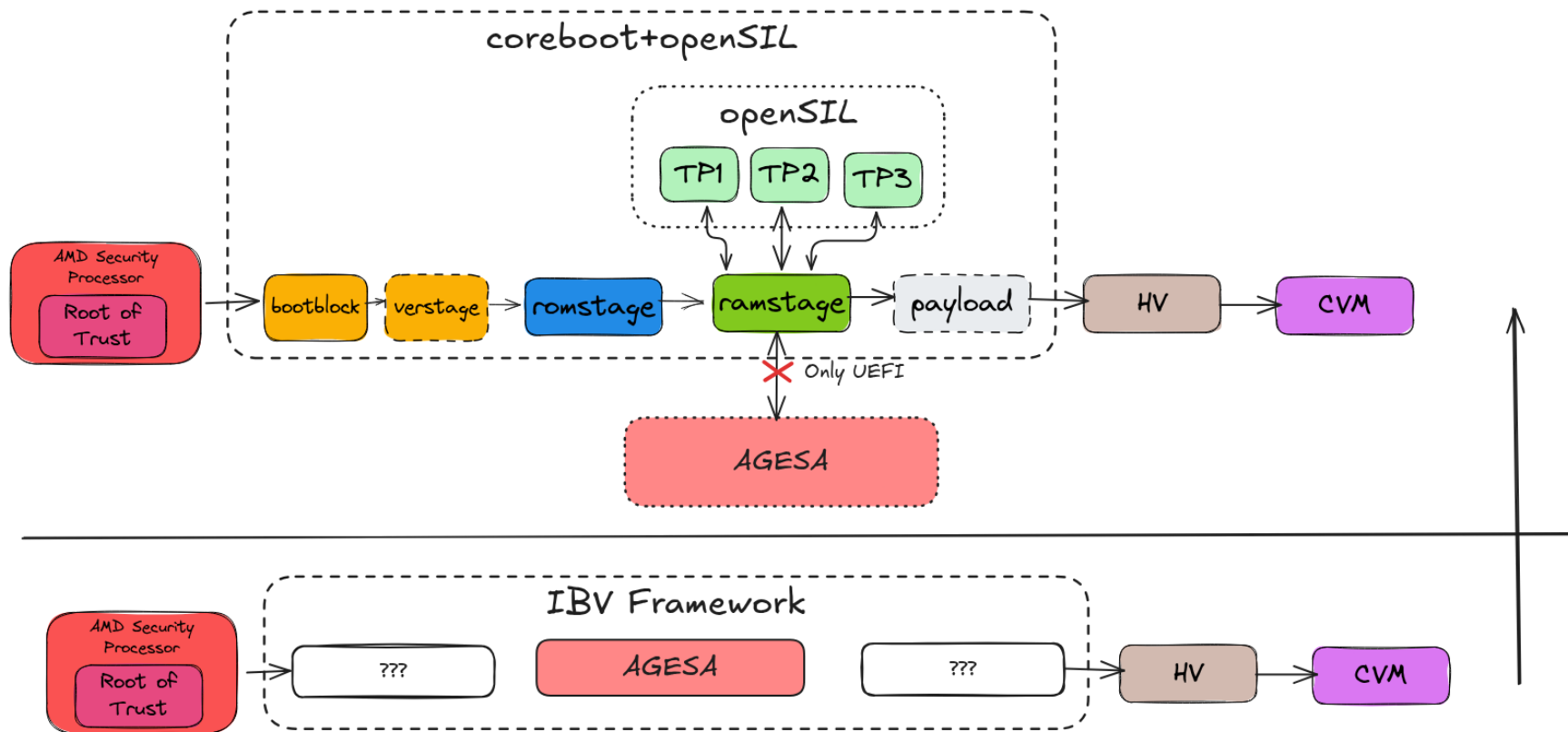
What OpenSIL opens:

- xSIM - Silicon Init (memory, CPU)
- xPRF - Platform Reference FW
- xUSL - Utilities & Services

What remains closed:

- ASP firmware (~3MB blob)
- SEV firmware
- ⚠ "ASP is outside the scope"

OCP contribution (Sept 2025): [Spec v1.0](#) — industry standardization path






GIGABYTE MZ33-AR1

AMD EPYC 9005 Series (Turin) · 5th Gen · Up to 192 cores

Why this board?

- First retail Turin board with coreboot+openSIL
- Retail server hardware
- Building on successful Genoa PoC
- AMD PSB unlikely provisioned
- OpenBMC potential (no ASPEED secure boot)

Implementation Journey

Funded by  — documented in 6 blog posts at blog.3mdeb.com

Month	Milestone	Blog Post
Aug	First serial output	Part 1: Initial porting
Sep	I/O initialization	Part 2: Blob analysis
Oct	PCIe working	Part 4: PCIe mapping
Nov	OS boots	Part 5: ACPI & bugfixes
Dec	Upstream ready	Part 6: Upstream & BMC

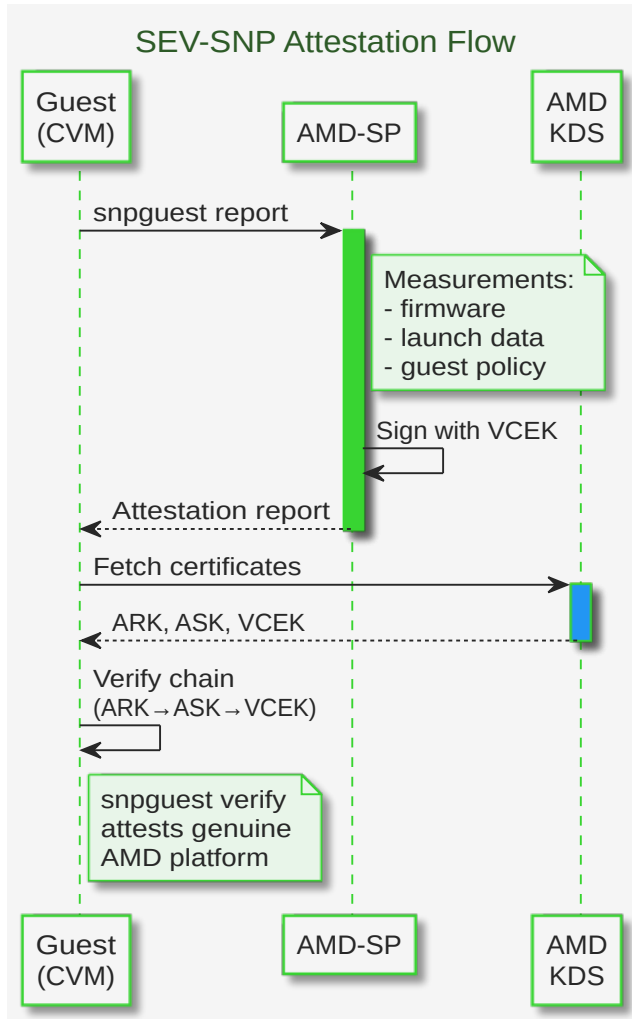
Statistics (w/o SEV-SNP): ~13k LOC · 84 coreboot patches · 7 openSIL PRs · ~3.7% of openSIL codebase

SEV-SNP on Open-Source Firmware

- First retail server board with open-source firmware + SEV-SNP
- No proprietary UEFI BIOS - only ASP blobs remain closed
- Changes pending upstream to coreboot mainline
- Enables cryptographic proof of platform state → attestation

Key Changes (~950 SLOC added):

Component	Change	Purpose
openSIL	PSP MMIO in NBIO init	Enable PSP mailbox for SEV
coreboot	RMP table reservation	Memory integrity protection
coreboot	SEV NVRAM data	PSP SEV initialization
coreboot	AP bring-up mods	Multi-core SEV support
coreboot	ASPT ACPI table	SEV platform info for OS



AMD KDS (Key Distribution Service):

- Public AMD service hosting certificate chain
- Provides ARK, ASK, and per-chip VCEK


Certificate Chain:

- ARK - AMD Root Key (self-signed)
- ASK - AMD SEV Key (signed by ARK)
- VCEK - per-chip key (signed by ASK)

Attestation Report:

- TCB versions, guest measurements
- Platform info & policy
- Signed by chip-unique VCEK

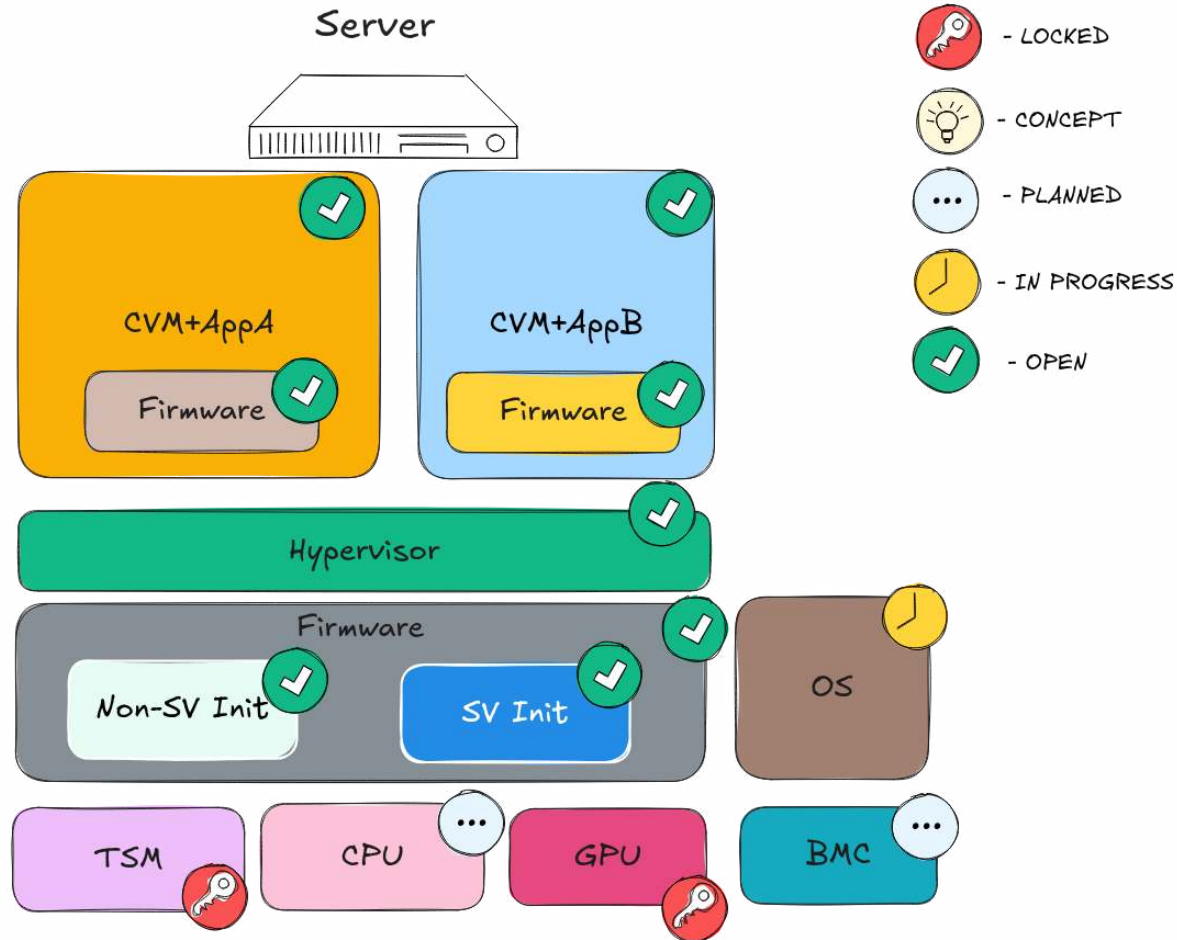
Demo: SEV-SNP on Open-Source Firmware

A terminal window titled 'ubuntu@ubuntu: ~/Downloads' showing the output of a system boot sequence. The logs indicate the successful startup of various systemd services and the reaching of several targets. The services listed include 'systemd-tmpfiles-setup-dev', 'sys-fs-fuse-connections.mount', 'sys-kernel-config.mount', 'systemd-udev-trigger.service', 'systemd-random-seed.service', 'systemd-sysctl.service', 'multipathd.service', 'systemd-resolved.service', 'systemd-timesyncd.service', 'systemd-tmpfiles-setup-dev', 'systemd-journal-flush.service', 'systemd-timesyncd.service', 'systemd-resolved.service', 'systemd-udev.service', 'systemd-ask-password-console.service', and 'systemd-cryptsetup.service'. The targets reached are 'local-fs-pre.target', 'time-set.target', 'nss-lookup.target', and 'cryptsetup.target'. The terminal also shows the creation of static device nodes in /dev and the discovery of the 'dev-ttyS0.device' at '/dev/ttyS0'.

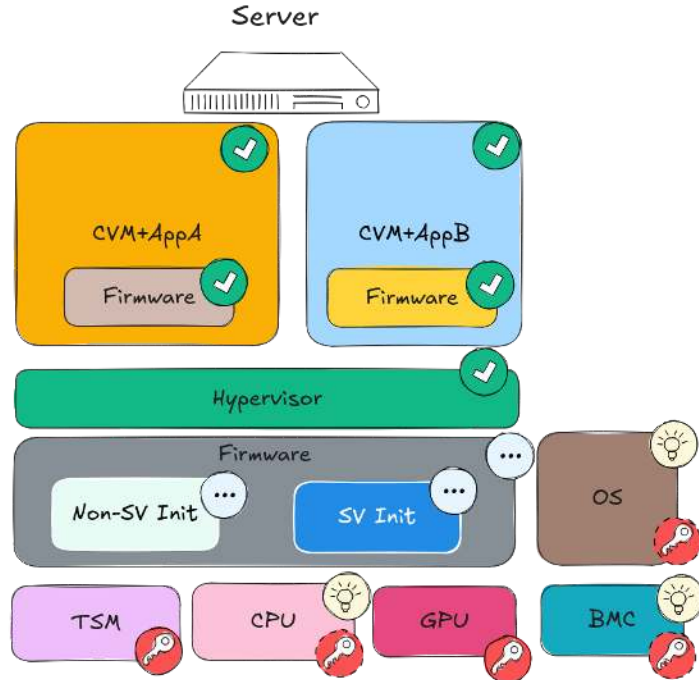
```
ubuntu@ubuntu: ~/Downloads
Starting systemd-tmpfiles-setup-dev... Device Nodes in /dev gracefully...
[ OK ] Mounted sys-fs-fuse-connections.mount - FUSE Control File System.
[ OK ] Mounted sys-kernel-config.mount - Kernel Configuration File System.
[ OK ] Finished systemd-udev-trigger.service - Coldplug All udev Devices.
[ OK ] Finished systemd-random-seed.service - Load/Save OS Random Seed.
[ OK ] Finished systemd-sysctl.service - Apply Kernel Variables.
[ OK ] Finished systemd-tmpfiles-setup-dev...ic Device Nodes in /dev gracefully.
[ OK ] Started multipathd.service - Device...Mapper Multipath Device Controller.
Starting systemd-resolved.service - Network Name Resolution...
Starting systemd-timesyncd.service - Network Time Synchronization...
Starting systemd-tmpfiles-setup-dev...eate Static Device Nodes in /dev...
[ OK ] Finished systemd-tmpfiles-setup-dev...Create Static Device Nodes in /dev.
[ OK ] Reached target local-fs-pre.target...Preparation for Local File Systems.
Starting systemd-udev.service - R...anager for Device Events and Files...
[ OK ] Finished systemd-journal-flush.ser...lush Journal to Persistent Storage.
[ OK ] Started systemd-timesyncd.service - Network Time Synchronization.
[ OK ] Reached target time-set.target - System Time Set.
[ OK ] Started systemd-resolved.service - Network Name Resolution.
[ OK ] Started systemd-udev.service - Ru...anager for Device Events and Files.
[ OK ] Reached target nss-lookup.target - Host and Network Name Lookups.
[ OK ] Started systemd-ask-password-conso...equests to Console Directory Watch.
[ OK ] Reached target cryptsetup.target - Local Encrypted Volumes.
[ OK ] Found device dev-ttyS0.device - /dev/ttyS0.
```

Watch: youtube.com/watch?v=dy_sCNIXEBy

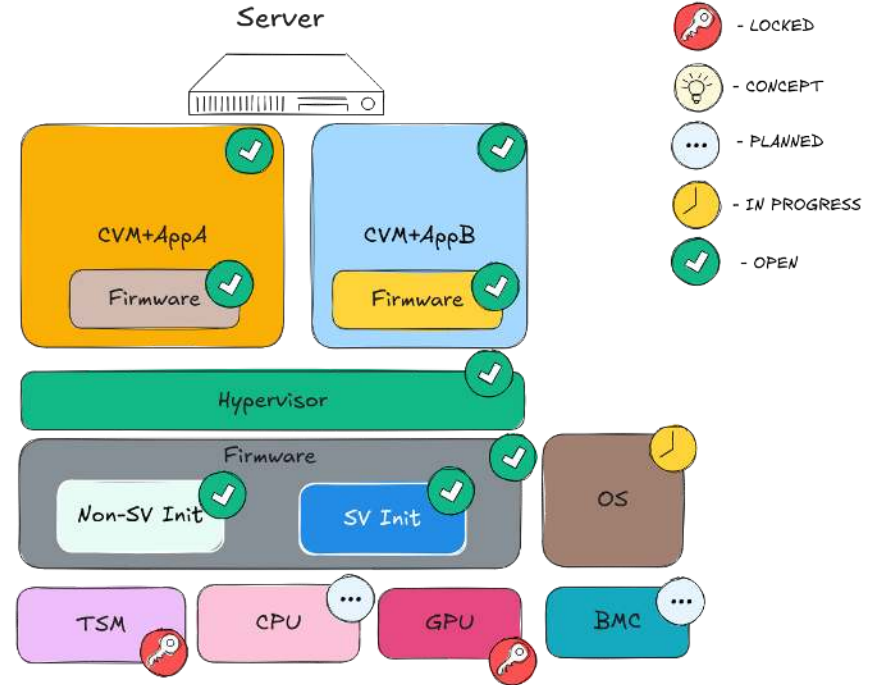
State of HACHI - FOSDEM'26



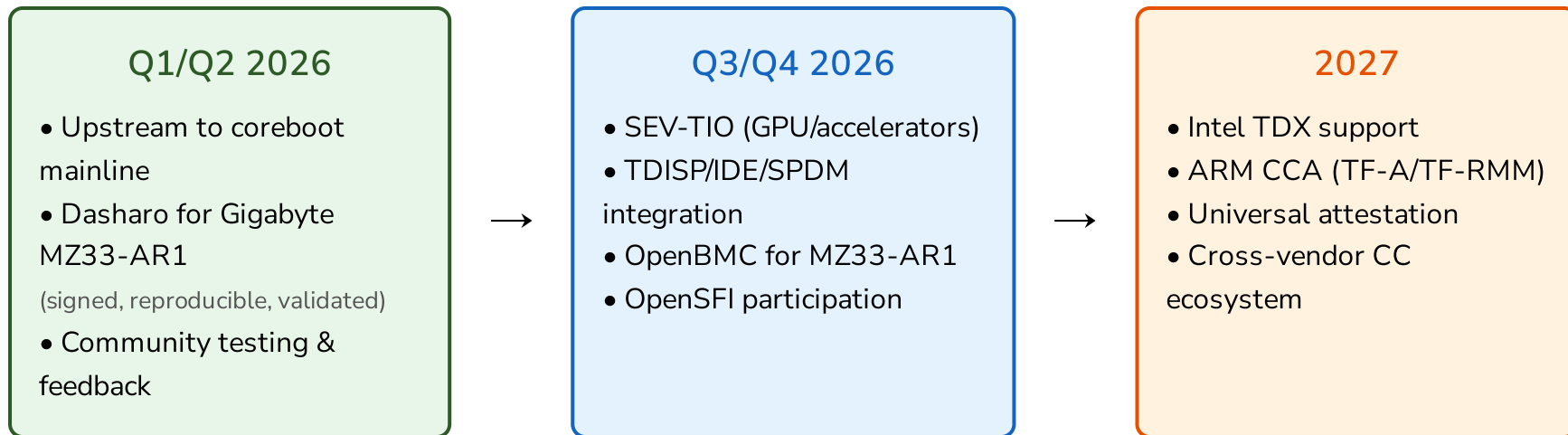
State of HABI - FOSDEM'25



State of HABI - FOSDEM'26



Roadmap: Open-Source Firmware for Confidential Computing



Goal: Auditable firmware foundation for all confidential computing platforms



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AUTUMN 2026, MAJOR EUROPEAN CITY
TALKS, WORKSHOPS,
REAL-WORLD BOOT SECURITY

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3MDEB

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The background is a dark gray with faint, light gray circuit-like lines. These lines are composed of straight segments and right-angle turns, resembling a printed circuit board (PCB) layout. Some lines terminate in small solid gray circles, which could represent solder pads or vias. The lines are distributed across the frame, with a denser concentration on the left side and more sparse, diagonal lines on the right.

Questions?

Backup Slides

The background is a dark gray with faint, light gray circuit-like lines. These lines are composed of straight segments and right-angle turns, ending in small circular nodes. They are positioned in the corners of the slide, creating a technical or digital aesthetic.

The Trust Paradox

The accepted mindset:

"We cannot do anything about firmware. Let the vendor be responsible."

But history proves otherwise: Proprietary BIOS → coreboot+FSP → coreboot+openSIL → openSFI (future)

The responsibility shift:

Component	Trend
CPU BIOS	Responsibilities moving → ASP
Hypervisor	Responsibilities moving → SEV firmware
OS	Cooperates with silicon vendor, extends trust primitives

Historical pattern: OS complained about BIOS, then hypervisor...

When will OS start questioning silicon vendor firmware?

AMD SEV-SNP Architecture

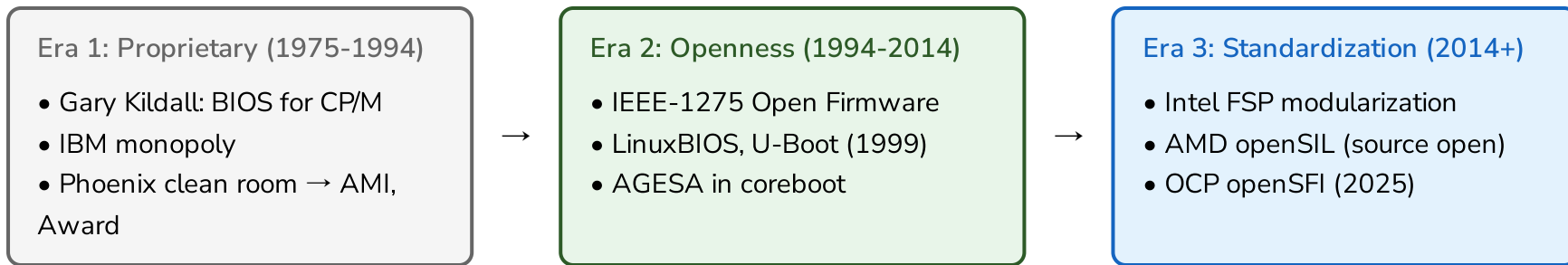
- Memory encryption: AES-128, per-VM keys, C-bit page control
- RMP: Hardware-enforced page ownership (prevents remapping attacks)
- Attestation: Cryptographic proof of VM launch state

What's in the TCB?

Component	Role	Open?
ASP	Key mgmt, attestation	✗ ~3MB blob
CPU BIOS*	HW init, ASP communication	✓ coreboot+OpenSIL
Hypervisor	VM management	✓ KVM/QEMU, Xen

*AMD nomenclature for system firmware. CPU BIOS openness is our key contribution.

Firmware History: A Lesson for CC?



Pattern: Proprietary → Openness → Standardization → *IP shifts to new proprietary component*

Research: Supply Chain Proof

Vulnerability Spectrum Analysis

Analyze CC stack to provide evidence for supply chain claims:

- Turin SEV firmware release notes - compare with other platforms
- AMD Product Security: <https://www.amd.com/en/resources/product-security.html>
- Hypervisor CVEs - KVM, Xen XSAs
- Linux kernel SEV-related issues

Goal: Create chart showing vulnerability distribution by component and which parts are auditable vs black boxes.

Backup: Security Analysis Tools

Platform	Tool	Purpose
AMD PSP	<u>PSPTool</u>	Extract, analyze PSP firmware
AMD SEV	<u>AMD-ASPFW</u>	PSP SEV FW source (Genoa)
Intel ME	<u>MEAnalyzer</u>	Parse ME firmware

Backup: Systemd CC Integration

- `systemd 255+`: Measured boot, UKI with PCR measurements
- `systemd-creds`: TPM2-bound secrets for services
- `systemd-cryptenroll`: LUKS with TPM2 policies