UNIVERSITY OF TORONTO

Winter 2015 Midterm Solutions

CSC258: Computer Organization

Duration: 2 hours

February 23rd, 2015

Last Name: ______________________________________

First Name: ______________________________________

Student Number: __________________________________

Instructor (circle one): **Steve Engels (L0101)**

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Instructions:

- **Write your name on the back of this exam paper.**
- **Do not open this exam until you hear the signal to start.**
- Have your student ID on your desk.
- No aids permitted other than writing tools. If you write in pencil, we reserve the right to deny any remark requests.
- Keep all bags and notes far from your desk before the exam begins.
- There are 4 parts on 8 pages. When you hear the signal to start, make sure that your exam is complete before you begin.
- Read over the entire exam before starting.
- If you use any space for rough work or have to user the overflow page, clearly indicate the section(s) that you want marked.

Mark Breakdown

Part A:	**/ 20**
Part B:	**/ 30**
Part C:	**/ 13**
Part D:	**/ 12**
Total:	**/ 75**

Part A: Short Answer (20 marks)

Answer the following questions in the space provided. When providing a written answer, write **<u>as clearly and legibly as possible</u>**. Marks will not be awarded to unreadable answers.

1. Assume that A is the 8-bit signed binary number shown below. In the spaces below, provide the 2's complement of A, and the equivalent decimal value for both A and its complement. **(2 marks)**

A = 10110100 **Decimal value:** -76

2's complement of A: 01001100 **Decimal value:** 76

2. In order to make the depletion layer of a pn junction wider, a positive voltage must be applied to what part(s) of the junction? **(1 mark)**

a) the p side **b)** the n side **c)** both **d)** neither

3. What direction do the electrons travel in the depletion later of a pn junction, as a result of the electric field in that depletion layer? **(1 mark)**

a) toward the p side **b)** toward the n side

c) in both directions **d)** in neither direction

4. If you want a wire to be included in the Technology Viewer in Quartus, what Verilog syntax term do you need to use? **(1 mark)**

```
/* synthesis keep*/
```

5. Which of the following Verilog statements cause `Y` to have a low value when inputs `A` and `B` are both low? Circle all that apply. **(2 marks)**

a) `assign Y = A && B;` **b)** `xor(Y, A, B);`

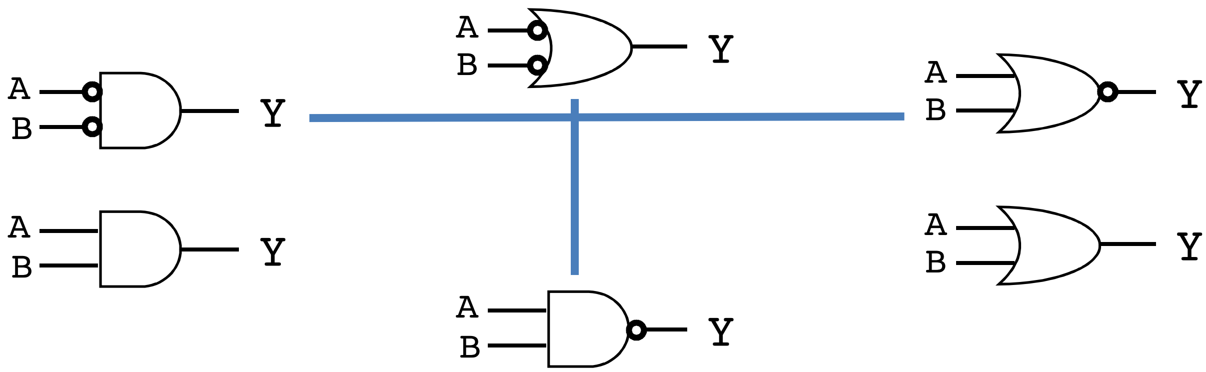
c) `assign Y = A || B;` **d)** `nand(Y, A, B);`

6. Given inputs A, B, C and D, which of the following are valid minterms? **(2 marks)**

a) $A \cdot B + C \cdot D$ **b)** $A + B + C + D$

c) $D \cdot C \cdot B \cdot A$ **d)** $\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D}$

7. De Morgan's Law states that certain gates are logically equivalent. Draw lines between the gates that are logically equivalent, according to de Morgan. **(2 marks)**



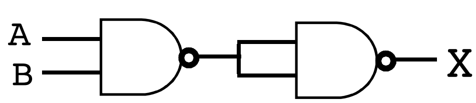
8. What is the decimal value for the lowest 8-bit unsigned binary number? **(1 mark)**

0

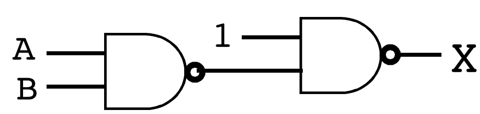
9. For a clocked SR latch, what are the output values on Q and $\overline{Q}$ when C, R and S are all high? **(2 marks)**

Q: 1   **$\overline{Q}$:** 1

10. In the space below, draw a circuit with a single output X and inputs A and B, where $X = A \cdot B$ and the circuit is made entirely of NAND gates. For full marks, use the fewest NAND gates possible. **(2 marks)**



or



11. In the spaces below, list the four items that are provided in the kits for the lab. **(4 marks)**

Logic probe

Chip puller

Ribbon cable

Wire stripper

Part B: Slightly Longer Answer (30 marks)

Answer the following questions in the space provided. The final answer is all that is necessary, but showing your work can help if your final answer isn't correct. Again, make sure to write legibly here.

1. Draw lines to connect the Verilog modules that have equivalent behaviour. **(16 marks)**

```
module theta(A, B, C);
  input A, B;
  output C;
  assign C = (~A & ~B) | ~A;
endmodule
```

```
module epsilon(A, B, C);
  input A, B;
  output C;
  assign C = A ^ B;
endmodule
```

```
module beta(A, B, C);
  input A, B;
  output C;
  wire D, E;
  or (C, A, E);
  and (E, D, B);
  not (D, A);
endmodule
```

```
module alpha(A, B, C);
  input A, B;
  output C;
  wire D, E, F, G;
  not (D, A);
  not (E, B);
  and (F, D, B);
  and (G, E, A);
  or (C, F, G);
endmodule
```

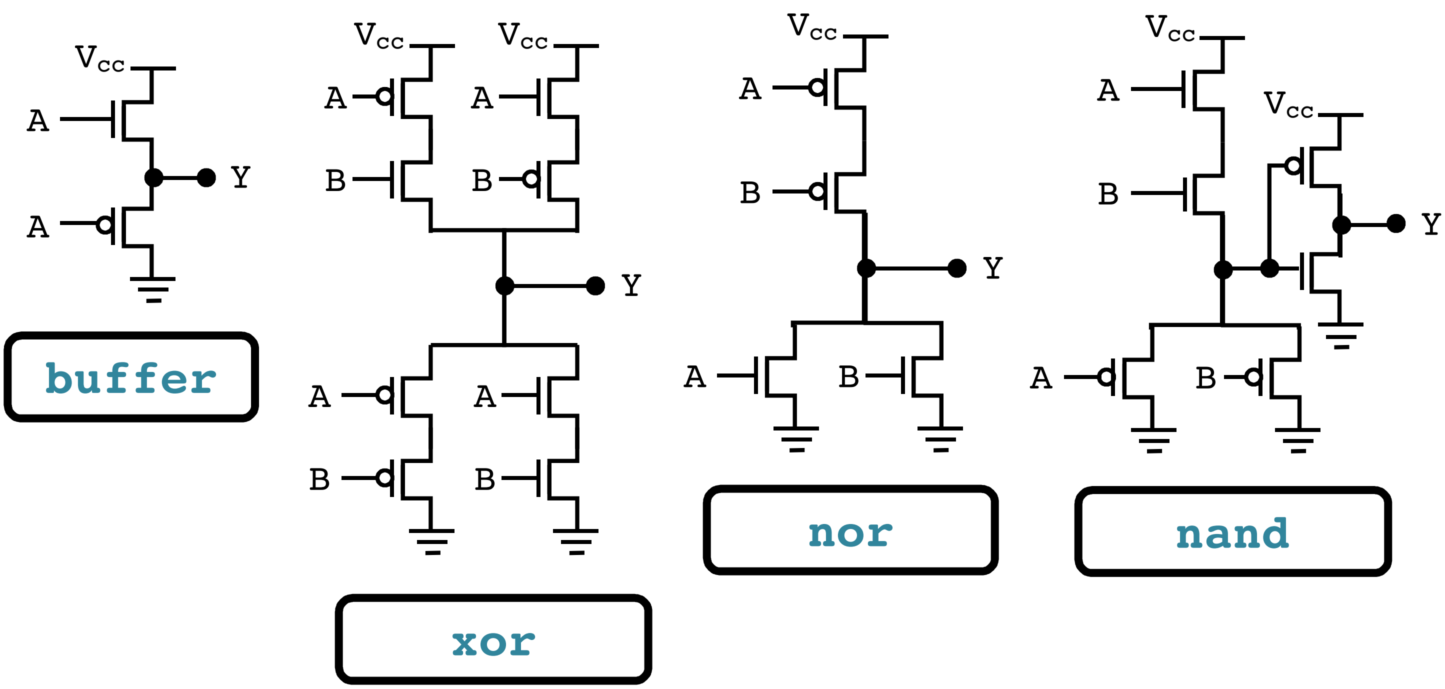
```
module gamma(A, B, C);
  input A, B;
  output C;
  wire D, E;
  and (D, A, B);
  nor (E, A, B);
  or (C, D, E);
endmodule
```

```
module delta(A, B, C);
  input A, B;
  output C;
  wire D;
  or (D, A, B);
  nand (C, A, D);
endmodule
```

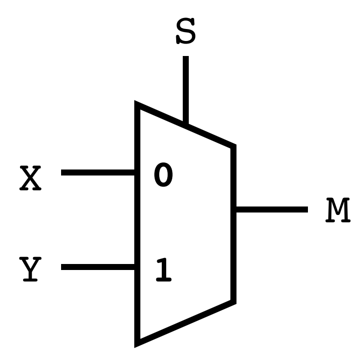
```
module sigma(A, B, C);
  input A, B;
  output C;
  assign C = (A == B);
endmodule
```

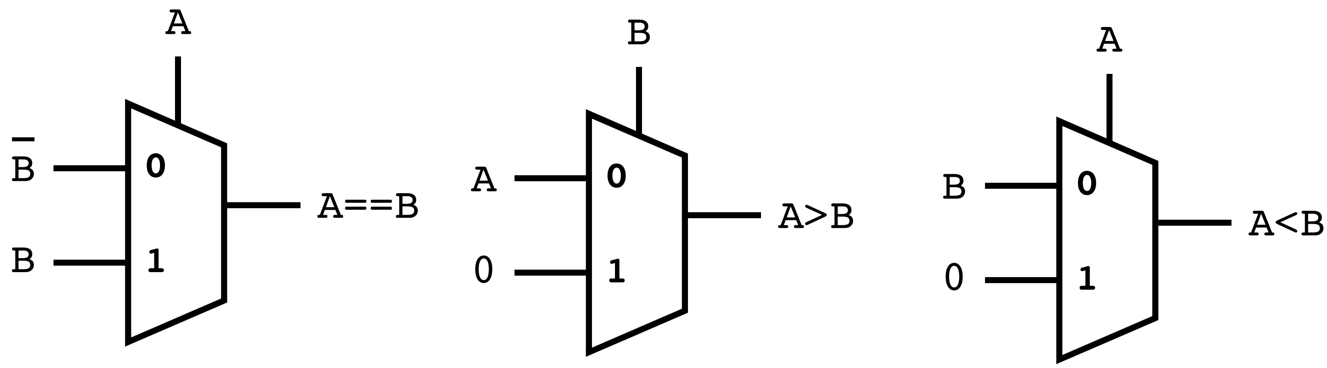
```
module omega(A, B, C);
  input A, B;
  output C;
  assign C = A | (~A & B);
endmodule
```

2. In the spaces below, name the gate implemented by each transistor circuit. **(8 marks)**



3. Consider the 2-input mux diagram on the right. In the space below, implement the three outputs of a **one-bit comparator**, using only the 2-input muxes and NOT gates. For full marks, use the minimal number of muxes and NOT gates possible. **(6 marks)**





Part C: Circuit Design and Analysis (13 marks)

1. Larry, Myrto and Steve have designed a frozen yogurt machine, where customers select whether they want vanilla (V) or chocolate (C) yogurt, or a combination of both. There are also two optional toppings that customers can select: butterscotch (B) and strawberry sauce (S).

Customers get discounts if any of the owners' favourite combinations are selected:

- Larry likes everything except the combination of butterscotch and chocolate together.
- Myrto also hates butterscotch, and never mixes vanilla and chocolate.
- Steve likes any combination of 3 or more items at the same time.

Assuming the machine forces you to select at least one flavour of yogurt, fill in the Karnaugh maps below to indicate the behaviour of the circuitry that would activate the Larry, Myrto and Steve discounts. **(6 marks)**

Larry:

	$\bar{S}\bar{B}$	$\bar{S}B$	SB	$S\bar{B}$
$\bar{V}\bar{C}$	X	X	X	X
$\bar{V}C$	1	0	0	1
VC	1	0	0	1
$V\bar{C}$	1	1	1	1

Myrto:

	$\bar{S}\bar{B}$	$\bar{S}B$	SB	$S\bar{B}$
$\bar{V}\bar{C}$	X	X	X	X
$\bar{V}C$	1	0	0	1
VC	0	0	0	0
$V\bar{C}$	1	0	0	1

Steve:

	$\bar{S}\bar{B}$	$\bar{S}B$	SB	$S\bar{B}$
$\bar{V}\bar{C}$	X	X	X	X
$\bar{V}C$	0	0	1	0
VC	0	1	1	1
$V\bar{C}$	0	0	1	0

2. On the Karnaugh maps above, provide the groupings for each map that will result in circuits with the lowest gate cost. Write the most reduced equivalent boolean expressions in the spaces below. **(6 marks)**

Larry: $\bar{B} + \bar{C}$

Myrto: $\bar{B}\bar{V} + \bar{B}\bar{C}$

Steve: $SB + VCB + VCS$

3. Whose discount results in the circuit with the lowest gate cost? **(1 mark)**

Larry's

Part D: Verilog (12 marks)

Consider the piece of Verilog code on the right.

```
module midterm (Q, D, L, E, C, R);
  input [7:0] D;
  input L, E, C, R;
  output reg [7:0] Q;

  always @ (posedge C, negedge R)
  if (~R)
    Q <= 0;
  else if (L)
    Q <= D;
  else if (E)
    Q <= Q + 1;

endmodule
```

1. What does this piece of code do? **(4 marks)**

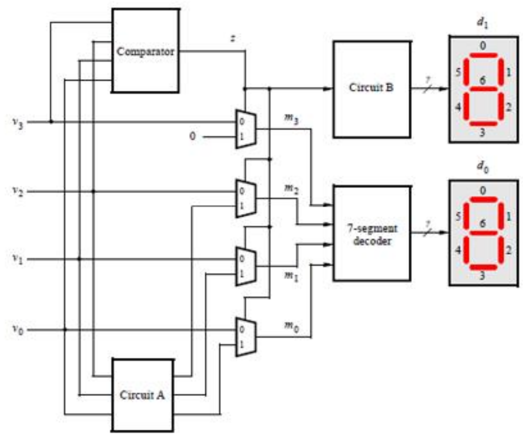
Counter with parallel load (and asynchronous negative clear)

2. What do the signals L and R stand for here (or, what function to they perform)? **(2 marks)**

L : Load

R : Reset

3. Consider the diagram on the right, taken from Lab 2. In the space below, complete the Verilog code that implements the comparator from this diagram. NOTE: for full marks, you may not use arithmetic or comparison operators in your solution. **(6 marks)**




```
module lab2_comparator (v, z);

    input [3:0] v;
    output z;

    assign z = v[3] & (v[2] + v[1]);

    endmodule
```

Bonus Question: ***In the labs, Cyclone II is the device family you select when creating a new project. What is the name of the actual device that you select next? (1 mark)***

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Please enter your first and last name in the space below. Do NOT write your student number here.