Week 4 tutorial

Question #1

a) How do you write the number 78 as an 8-bit binary number?

128	64	32	16	8	4	2	1
0	1	0	0	1	1	1	0

b) What is the two's complement of 01101101?

10010011

c) What is the sum of 01101101 and 01101101?

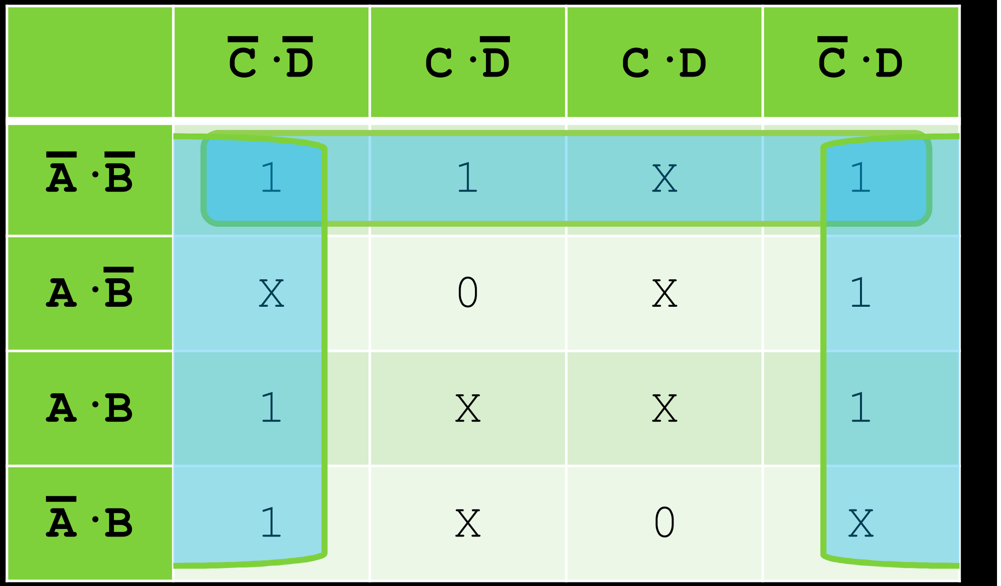
11011010

← Note what's happening here!

overflow, two positive number adds up to a negative number if the number is unsigned with 2s complement

Question #2

- What groupings are in the K-map on the right?

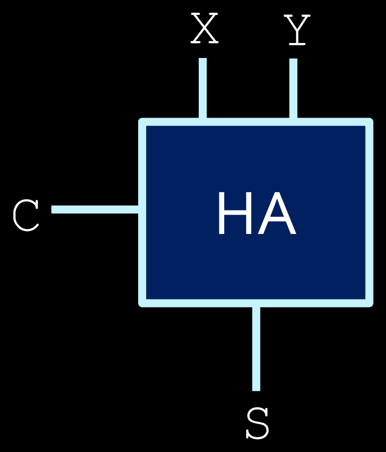


	$\overline{C} \cdot \overline{D}$	$C \cdot \overline{D}$	$C \cdot D$	$\overline{C} \cdot D$
$\overline{A} \cdot \overline{B}$	1	1	X	1
$A \cdot \overline{B}$	X	0	X	1
$A \cdot B$	1	X	X	1
$\overline{A} \cdot B$	1	X	0	X

- What logic equations do these groupings represent?

$$\overline{A} \cdot \overline{B} + \overline{C}$$

Question #3



- Implement a half adder in Verilog.
- Step 1: What is the half adder logic equation?

$$\mathbf{C} = X \cdot Y \qquad \mathbf{S} = X \cdot \overline{Y} + \overline{X} \cdot Y$$

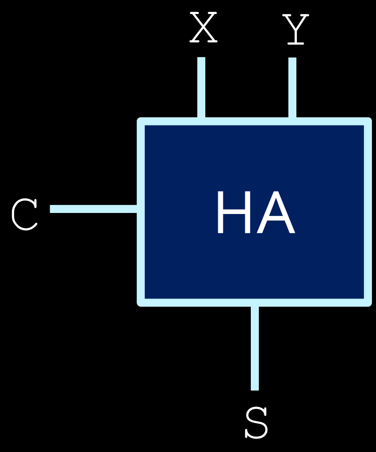
$$= X \oplus Y$$

- Step 2: Equivalent Verilog components.

```
assign C = X & Y;
assign S = X & ~Y | ~X & Y;
```

Question #3 (cont'd)

- Step 3: What is the complete Verilog code for this device?



```
module half_adder(X, Y, C, S);
   input X, Y;
   output C, S;

   assign C = X & Y;
   assign S = X & ~Y | ~X & Y;
endmodule
```