```
# Loading work.Integer_ClkDiv_tb
# Loading work.Integer_ClkDiv
#
# Name : Ahmed Mohamed Afifi
# Name : Integer_ClkDiv
#
#
# Test Case ( 1 ) : Dividing by 8
#
# Test Case ( 2 ) : Dividing by 5
#
# Test Case ( 3 ) : Dividing by 1
#
# Test Case ( 4 ) : Dividing by 0
#
# Test Case ( 5 ) : Dividing by 127
#
# Test Case ( 6 ) : Dividing by 255
#
# Test Case ( 7 ) : From high i_dev_ratio to low corner case
#
# Break in Module Integer_ClkDiv_tb at Integer_ClkDiv_tb.v line 119
# Simulation Breakpoint: Break in Module Integer_ClkDiv_tb at Integer_ClkDiv_tb.v line 119
# MACRO ./run.do PAUSED at line 5

VSIM(paused)>
```

Msgs

i_dev_ratio_tb 1 — 5 / 1
i_clk_en_tb 1
i_rst_n_tb -1
i_ref_clk_tb 0
New_clk 1
o_div_clk_tb St0
Module internal signals — (Module internal signals)
En St0
Type St1
Half_Div -1 — 1 / -1
Half_Div_p1 0 — 2 / 0
Count 0 — 0 / 1 / 2 / 0
Flag 0

Msgs

i_dev_ratio_tb 1 — 1 / 0
i_clk_en_tb 1
i_rst_n_tb -1
i_ref_clk_tb 0
New_clk 1
o_div_clk_tb St0
Module internal signals — (Module internal signals)
En St0
Type St1
Half_Div -1 — -1
Half_Div_p1 0 — 0
Count 0 — 0
Flag 0

Msgs

i_dev_ratio_tb 1 — 0 / 127
i_clk_en_tb 1
i_rst_n_tb -1
i_ref_clk_tb 0
New_clk 1
o_div_clk_tb St0
Module internal signals — (Module internal signals)
En St0
Type St1
Half_Div -1 — -1 / 62
Half_Div_p1 0 — 0 / 63
Count 0 — 0
Flag 0

Msgs

i_dev_ratio_tb 1 — 127 / 255
i_clk_en_tb 1
i_rst_n_tb -1
i_ref_clk_tb 0
New_clk 1
o_div_clk_tb St0
Module internal signals — (Module internal signals)
En St0
Type St1
Half_Div -1 — 62 / -2
Half_Div_p1 0 — 63 / -1
Count 0 — 0
Flag 0